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Lab Assignment - 1

Title: Design of Pass 1 of a Pass Assembler

Aim: Design suitable data structures & implement pass 1 of a pass assembler pseda machine.

Objective: Design suitable data structure & implement pass 1 of a pass assembler pseda machine. Subset should consist of a few instruction from each category in few assembler directive

Theory:

→ Assembler: It translate assembly ~~lan~~ language program to binary language. Input for assembler is language generated by compiler. For Pass 1 assembler defines symbols & literals & save them in symbolic opcode table. It assigns machine address to symbolic labels.
It performs assembler service required by pseda operations & saves files for future use

→ Design specification of Assembler

⇒ Analysis Phase
It seperates label, memonic, opcode & operand from instruction statement.
If label is present, it made entry in symbol table thus builds symbol table
Performs LC processing & constructs IC.

⇒ Synthesis Phase.
It obtains machine code corresponding to memonics from opcode table

It obtains address of memory operand from symbol table
Synthesizes a machine instruction

→ Algorithm for Pass I

1 loccntr = 0 (default value)
2 while next statement is not an END statement
(a) If lable is present then
this label = symbol in label field
Enter (this-label, loccntr) in SYMTAB.
(b) If a START or ORIGIN statement then
loccntr = value specified in operand field
(c) If an EQU statement then
(i) this addr = value of <address spec>
(ii) Correct the symtab entry for this label to (this label, this addr)
(d) If a declaration statement then
(i) code = code of the declaration statement.
(ii) size = size of memory area required by DC/DS
(iii) loccntr = loccntr + size.
(iv) Generate IC '(DL, code)
(e) If an imperative statement then
(i) code = machine opcode from OPTAB
(ii) loccntr = loccntr + instruction length from OPTAB
(iii) If operand is a symbol then.
this-entry = SYMTAB entry number of operand
Generate IC (IS, code) (S, this-entry)

3 Processing of END statement
(b) Generate IC
(c) Go to Pass II.

Input: ALP1 intermediate code generated by Pass 1

Output:

OPTAB

Mnemonic	OP-code
Start	01, AD
MOVER	01, IS
SUB	02, IS
MOVER	04, IS
ORIGIN	03, AD
MOVER	04, IS
DS	01, DL
DC	02, DL
END	02, AD

Symbol Table

Sym-id	Sym-name	Sym-addr	length
1	A1	301	3
2	LOOP	401	1
3	B1	304	1

Intermidiate from (After Pass 1) / Final output.

Add. (LC value)	Opcode	Operand 1	Operand 2
	(AD,01)		(C,400)
400	(IS,04)	1	(S,01)
401	(IS,02)	2	(S,01)
402	(IS,04)	2	(S,03)
	(AD,03)		(C,300)
300	(IS,04)	2	(S,01)
301	(DL,02)		(C,3)
304	(DL,01)		(C,3)
305	(AD,02)		

Conclusion: The function of Pass I in assembler are ~~schedu~~ studied along with errors coming in each pass.

Platform: Linux (JAVA)