

304184 : MICROCONTROLLER.

CREDITS : 03

IN-SEM : 36 MARKS

END SEM : 70 MARKS

304188 : MICROCONTROLLER LAB

CREDITS : 01

PRACTICAL : 50 MARKS.

### THEORY SYLLABUS

UNIT 1 : Introduction to Microcontroller Architecture

UNIT 2 : IO Port interfacing - I

UNIT 3 : PIC 18Fxxxx Microcontroller Architecture

UNIT 4 : Peripheral support in PIC 18Fxxxx

UNIT 5 : Real word Interfacing with PIC 18Fxxxx

UNIT 6 : SERIAL PORT Programming interfacing with 18Fxxxx

### Books to Refer:

"The 8051 Microcontroller and Embedded Systems" by  
Mahumad Ali Mazadi, Janice Grillispie Mazadi, Rolin D  
McKinlay , PHI 2<sup>nd</sup> Edition .

"PIC Microcontroller & Embedded System" , by Mahumad Ali Mazadi  
Rolin D McKinlay and Danny Causey , Pearson Education , 3<sup>rd</sup>  
Edition.

## UNIT 1 : INTRODUCTION TO MICROCONTROLLER

## ARCHITECTURE

Syllabus :

Difference between microprocessor and microcontroller  
Introduction to the microcontroller classification  
Features and Block diagram of 8051 and explanation  
Program Status Word (PSW)

8051 : overview of Instruction set, Memory organization,  
Interrupt structure, timers and its Mode.

Serial Communication : concept of baud rate, Data  
transmission and reception using serial port, sample  
programs of data transfer.

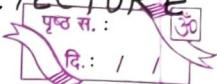
Delay using Timer (0 & 1) and interrupt.

Data transmission and reception using serial port.

I/O port programming

All programs in C language.

# UNIT 1 : INTRODUCTION TO MICROCONTROLLER ARCHITECTURE



**Ques 1.** Difference between MP and MC with General Architecture and Features.

Ans	Microprocessor	Microcontroller
1.	MP chip depends on many MC is a chip that has other chip for many functions everything inbuilt.	
2.	A MP contains ALU, General purpose registers, stack pointer, program counter, timing and Control circuit and interrupt circuit.	A MC contains the circuitry of MP and has built in RAM, ROM, I/O devices, timers and counters.
3.	It has one or two bit manipulation instruction	It has many bit manipulation instruction.
4.	It has less nos of multifunction pins	It has more nos of multifunction pins
5.	It has a single memory map for data and code	It has separate memory map for data and code
6.	MP based system requires more hardware	MC based system requires less hardware reducing PCB size and increase flexibility.
7.	Design is very flexible	Design is less flexible
8.	It has many instructions to move data, memory and CPU between	It has one or two instructions to move data between memory and CPU

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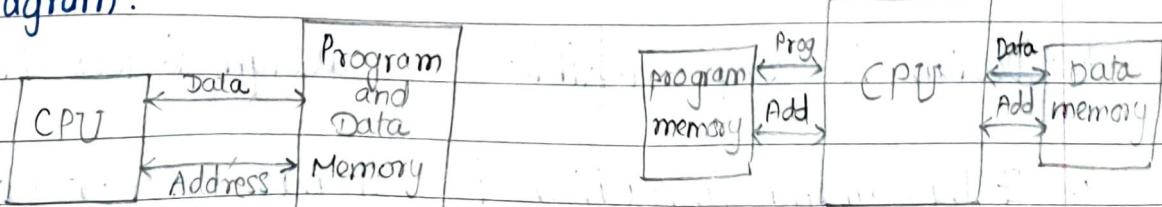
Ques 2 Difference between Harvard and Von Neuman Architecture.

Ans

Von Neumann

Harvard

1. Uses single Memory for Code and Data uses physically separated memory for Code and Data
2. Requires single bus for Code and instruction and Data Requires separate and dedicated bus for code and Data
3. Microcontroller with Von-Neumann Architecture are called CISC uc Microcontroller with Harvard Architecture are called RISC
4. It's Design is simple. Its design is Complex.
5. Codes and Data have to be fetched in sequential order Codes and data can be fetched simultaneously
6. Time Division multiplexing is used to fetch Codes and Data No need to use TDM
7. Eg: MC68HC11 Eg: mcs-51 family of uc and PIC uc
8. Diagram:



Que 15. Compare CISC and RISC processors.

Ans:

CISC

RISC

- |   |  |
|---|--|
| 1. Complex Instruction set Computer.                  | Reduced Instruction set Computer.  |
| 2. Instruction size is Variable                       | Instruction size is fixed.   |
| 3. Emphasis on hardware.                              | emphasis on software   |
| 4. No of Inst <sup>n</sup> : 120 to 350               | less than 100  |
| 5. Not pipelined or less pipelined.                   | Highly pipelined   |
| 6. Instruction requires multiple cycles for execution | single clock for execution   |
| 7. single register set                                | Multiple register set.   |
| 8. Addressing modes: 12-24                            | Limited to 3-5   |
| 9. Most of the instructions refer to memory           | Very Few instructions refers to memory.  |
| 10. Instructions are executed by a micro - program    | Instructions are executed by a hardware.   |
| 11. complexity is in micro - program.                 | Compiler is complex.   |
| 12. Clock rate → 33 to 50 MHz                         | Clock rate → 50 - 150 MHz.<br>जिसे प्राप्त प्रोसेसर कोई भी कार्य आरभ करते समय सदृश्यता का ध्यान अवश्य करो। |

Ques 3. Explain selection criteria for choosing a uc

Ans i) The first and important criterion i.e primary criteria in choosing a uc is that it should meet the requirement and cost effectively.

While analyzing the requirements of uc based project we must decide whether an 8, 16 or 32 bit uc is capable of handling the project efficiently. Other features:

- (i) Data size : 8, 16, 32 Bit uc
- (ii) clock speed : As per needed speed to complete operations in specified time
- (iii) Memory size : As per the required size of program and estimate of space needed for live data
- (iv) Power Consumption : As per the availability of power & type of power available.
- (v) Parallel & serial I/O port : As per the nos. & type of devices to be interfaced in sys
- (vi) Interrupts and Timers : As per need of application and device interfaced and controlled.
- (vii) One time Development cost : Meeting the budget & financial constraints.
- (viii) Packaging : Package is imp in terms of space, assembling and prototyping the end product. fg 40 pin DIP or QFP (quad flat package)
- (ix) Cost per unit : The final cost of product in which a uc is used.

ii) The second criterion in selecting a uc is how easy it is to develop product around it. The important factor to be considered are availability of an assembler, debugger, a code efficient c/c++ language

compiler, emulator, technical support and both in-house and outside expertise.

- Availability: of uc and other System Components current and over a period of time.
- Upgradability: of uc and other system Components ease, incremental cost & value addition
- Maintainability: of uc and other system components on site and component level repairs.

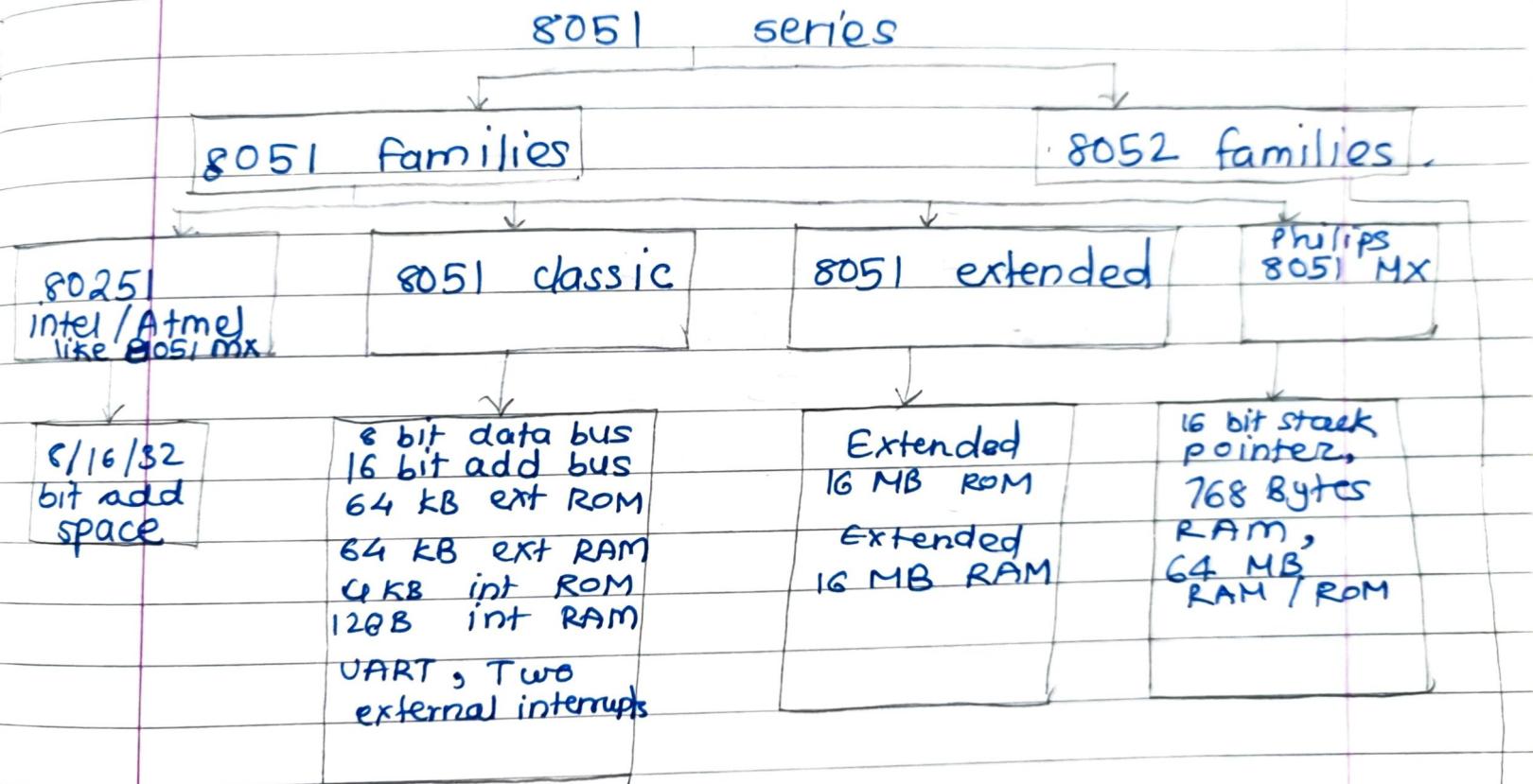
iii) The third criterion in selecting a uc is its ready availability in required quantities presently & in future. This criterion is important for some designers than first two criteria. Presently for the 8 bit uc, the 8051 family has the largest number of suppliers. It was originated by intel, but today Atmel, AMD, philips/ signetics, Infineon, sil labs, Matra and Dallas semiconductor.

Que 4. state features of 8051 uc.

- Ans.
1. 8 bit CPU optimized for control application
  2. 4 kbytes of on chip program memory
  3. 128 bytes of on chip data memory
  4. 64 kbytes of external ROM and 64 kbytes of external RAM addressability.
  5. 82 bidirectional I/O port lines  
i.e 4 - 8 bit ports (P0 - P3)
  6. Two 16 bit Timer/counter.
  7. full Duplex serial data transmitter / receiver.
  8. four register Banks
  9. on chip oscillator and clock circuit.
  10. 8 bit Data bus  
16 bit Address lines.

## Classification

### ① families of 8051 series.



8051 with  
256 bytes RAM  
& T2 Timer

## Ques: Architecture of 8051

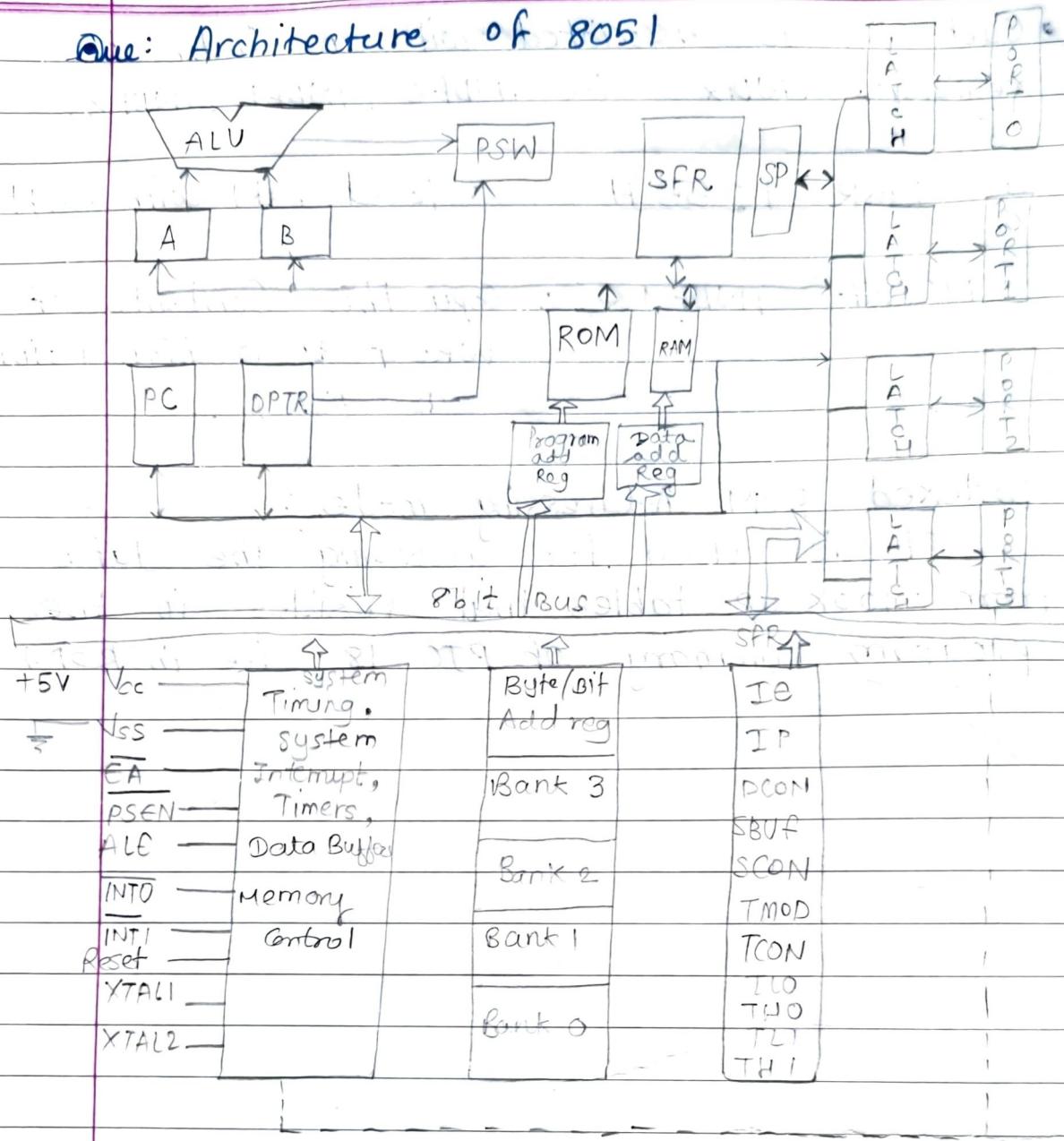
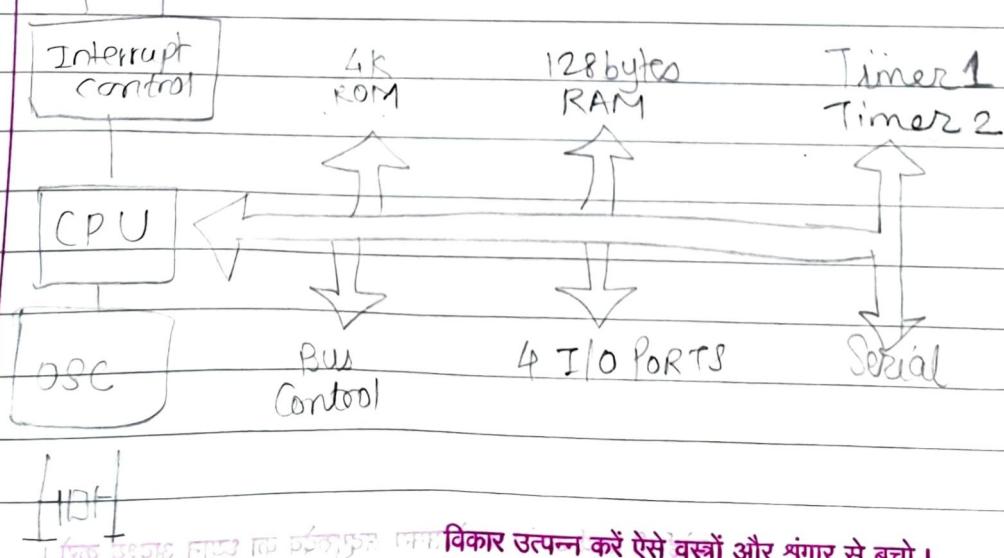


fig: Architecture of 8051 mc.



# PIN DIAGRAM of 8051

P <sub>1.0</sub>	1		40	V <sub>cc</sub>
P <sub>1.1</sub>	2		39	P <sub>0.0</sub> (AD <sub>0</sub> )
P <sub>1.2</sub>	3		38	P <sub>0.1</sub> (AD <sub>1</sub> )
P <sub>1.3</sub>	4		37	P <sub>0.2</sub> (AD <sub>2</sub> )
P <sub>1.4</sub>	5		36	P <sub>0.3</sub> (AD <sub>3</sub> )
P <sub>1.5</sub>	6		35	P <sub>0.4</sub> (AD <sub>4</sub> )
P <sub>1.6</sub>	7		34	P <sub>0.5</sub> (AD <sub>5</sub> )
P <sub>1.7</sub>	8		33	P <sub>0.6</sub> (AD <sub>6</sub> )
RESET	9	8051	32	P <sub>0.7</sub> (AD <sub>7</sub> )
P <sub>3.0</sub>	10		31	<u>EA / V<sub>PP</sub></u>
P <sub>3.1</sub>	11		30	ALE / PROG
P <sub>3.2</sub>	12		29	<u>PSEN</u>
P <sub>3.3</sub>	13		28	P <sub>2.7</sub> (A <sub>15</sub> )
P <sub>3.4</sub>	14		27	P <sub>2.6</sub> (A <sub>14</sub> )
P <sub>3.5</sub>	15		26	P <sub>2.5</sub> (A <sub>13</sub> )
P <sub>3.6</sub>	16		25	P <sub>2.4</sub> (A <sub>12</sub> )
P <sub>3.7</sub>	17		24	P <sub>2.3</sub> (A <sub>11</sub> )
XTAL 2	18		23	P <sub>2.2</sub> (A <sub>10</sub> )
XTAL 1	19		22	P <sub>2.1</sub> (A <sub>9</sub> )
V <sub>ss</sub>	20		21	P <sub>2.0</sub> (A <sub>8</sub> )

fig: PIN Diagram of  
8051.

V<sub>cc</sub>:

Supply Voltage

V<sub>ss</sub>:

Ground.

Port 0:

Port 0 is an 8 bit open drain bidirectional I/O port.

As an output port each pin can sink eight TTL inputs. When 1's are written to port 0 pins, the pin can be used as high impedance inputs.

Port 0 may also be configured to be multiplexed low order Address / Data bus during access to external program and data memory.

Port 0 also receives the code bytes during flash programming and output the code bytes during program verification.

#### Port 1 :

Port 1 is an 8 bit bidirectional I/O port with internal pull-ups.

The port 1 output buffers can sink/source four TTL inputs.

When 1's are written to port 1 pins are pulled high by internal pull ups and can be used as inputs.

#### Port 2 :

Port 2 is a 8 bit bidirectional I/O port with internal pull ups.

Port 2 output buffers can sink/source four TTL inputs. Port 2 can also be configured to be multiplexed high order Address / Data bus.

#### Port 3 :

Port 3 is a 8 bit bidirectional I/O port

The port 3 output buffers can sink/source 4 TTL inputs. Port 3 also serves various other functions

P <sub>3.0</sub>	RXD	(serial input port)
P <sub>3.1</sub>	TXD	(serial output Port)
P <sub>3.2</sub>	INT0	(external interrupt)
P <sub>3.3</sub>	INT1	(external interrupt)
P <sub>3.4</sub>	T0	(Timer/counter0 external i/p)
P <sub>3.5</sub>	T1	(Timer/Counter1 external i/p)
P <sub>3.6</sub>	WR	(External Data Memory Write strobe)
P <sub>3.7</sub>	RD	(External Data Memory Read strobe)

Port 3 also receives some control signals for flash programming and program verification.

#### RESET (RST) :

A high on this input pin for two Machine cycle, while the Oscillator is running resets the device.

#### ALE / PROG

ALE (Address Latch Enable) output pulse for latching the low byte of address during the access to external memory.

This pin is also program pulse input (PROG) during flash programming.

When 8051 is switched ON (or reset) it checks this pin (i.e ALE/PROG)

If pin is given logic 0 externally, it enters into flash programming mode else it enters into normal execution mode.

#### PSEN :

Program store enable is read strobe to external program memory.

When 8051 is executing code from external program memory, PSEN is activated twice each machine cycle except that two PSEN activations are skipped during each access to external data memory.

EA / V<sub>pp</sub> :

EA : external Access Enable .

EA must be strapped to ground in order to enable the device to fetch from external program memory locations starting from 0000H to OFFFH.

EA should be strapped to Vcc for fetching from internal program memory.

This pin also receives 12 V, programming enable voltage (V<sub>pp</sub>) during flash programming.

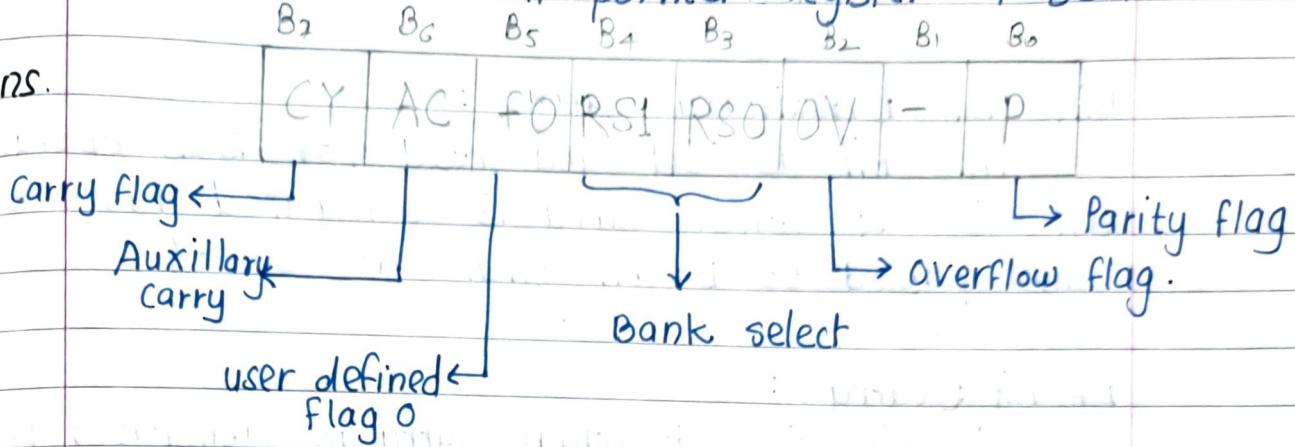
XTAL1 and XTAL2 :

XTAL1 is an input to inverting oscillator Amplifier and input to internal clock operating circuit.

XTAL2 is an output from inverting oscillator Amplifier A crystal is connected between XTAL1 and XTAL2

Ques 5: Explain PSW register of 8051 also explain stack operation and stack pointer register of 8051

Ans.



Program status Word is a 8 bit register.

The 8051 has four math flags: > carry

> Auxillary Carry

> overflow

> parity.

B<sub>0</sub> bit (Parity flag):

The parity flag is set when the result has even parity i.e. even nos. of 1's.

B<sub>1</sub> bit : user defined bit.

B<sub>2</sub> bit (overflow flag):

This flag is set if the result of single arithmetic operation is too large i.e. requires more than two registers to store data.

B<sub>3</sub> bit & B<sub>4</sub> bit [ Register Bank select bit ]:

Rsi	Rso	Bank selection
-----	-----	----------------

0	0	Bank 0
---	---	--------

0	1	Bank 1
---	---	--------

1	0	Bank 2
---	---	--------

1	1	Bank 3
---	---	--------

प्राप्ति कोई भी कार्य आरंभ करते समय सद्गुरुदेव का ध्यान अवश्य करो।

B<sub>5</sub> bit: This is a general purpose bit available to user.

Bits B<sub>6</sub> (Auxillary carry) :

This bit is set and reset for BCD operation. Bit is set when carry is generated from B<sub>3</sub> and passed to B<sub>4</sub> bit then AC bit = 1.

B<sub>7</sub> bit (carry) :

This bit is set when carry is generated from D<sub>7</sub> bit.

Stack pointer :

Stack pointer of the uc indicates the next value to be taken from the stack at address in internal RAM.

The Stack pointer point out Top of memory location of program. By starting each sub program the value in stack pointer is incremented by '1' and by ending sub program this value is decremented by '1'.

If another value is written to this register the entire stack is moved to new location in the memory.

Stack operation :

PUSH : In push operation the SP is incremented and then the data is stored at address pointed by the SP.

POP : In POP operation the data is taken from the location whose address is pointed currently by SP and then the SP is decremented.

विकार उत्पन्न करे ऐसे वस्त्रों और शृंगार से बचो।

Ques 14. Explain memory organization of 8051 microcontroller.

Ans.

Program Memory

Data Memory

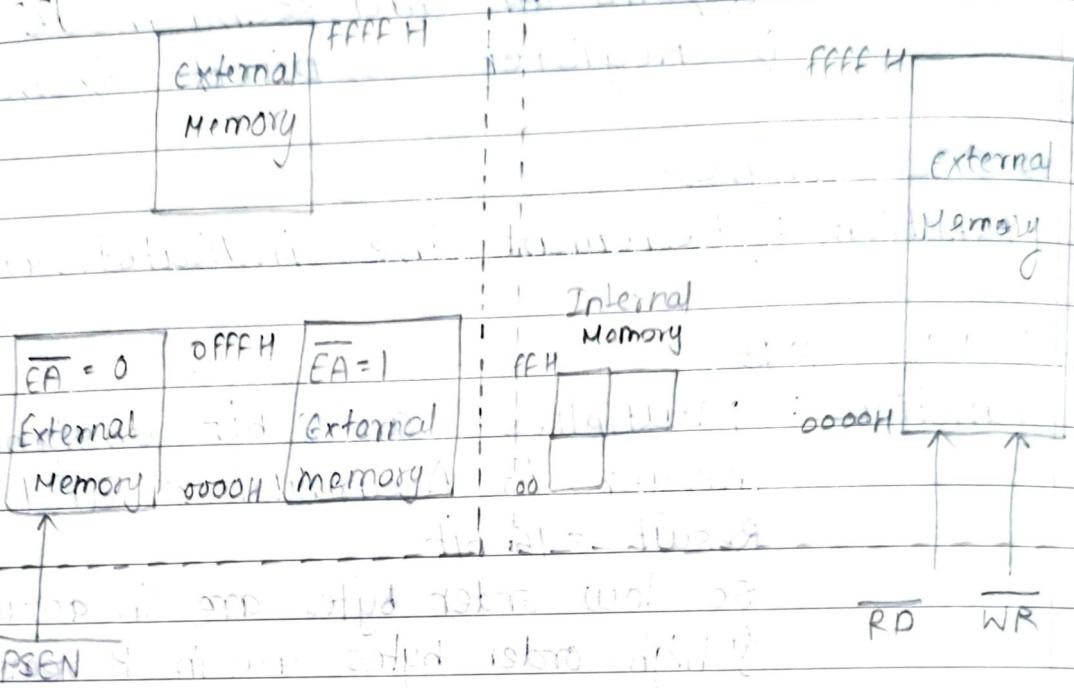
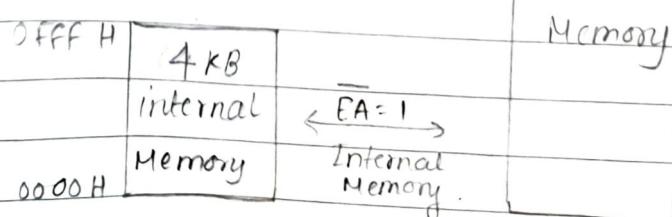
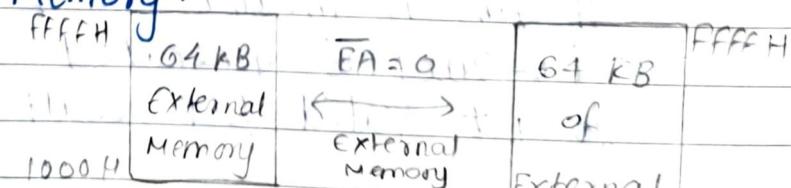


Fig: Memory structure of 8051 microcontroller

The figure shows basic memory structure of 8051 microcontroller. It can access 64 kbytes of program memory and 64 kbytes of Data memory.

- It has 4 kB of internal program memory & 256 bytes of internal Data memory.

Program Memory:



- The 8051 has 4KB of on chip program memory and can be expanded upto 64 KBytes. This extended memory is used to store program only.
- When  $\overline{EA} = 0$  i.e. Grounded the external memory from 1000 H to FFFF H can be accessed i.e. program from external memory is executed.
- When  $\overline{EA} = 1$  i.e. connected to Vcc the internal memory from 0000 H to 0FFF H can be accessed i.e. program can be executed from internal memory.
- The PSEN signal activates the o/p Enable signal for ROM/EPROM bank.

### Data Memory:

Internal Memory		External Memory	
(SFR's)		64 KB of External Memory	
FFH	Accessible by Indirect Addressing	FFFFH	
FFH	Accessible by Direct & Indirect Add mode		External Memory
00H		0000H	

- 8051 mc can address upto 64 KB of external Data memory and 256 bytes of internal Data memory.
- To access the external Data memory 'MOVX' instruction is used
- the internal Data memory is divided into 3 blocks
  - lower 128 bytes (00H to 7FH)
  - Upper 128 bytes (80H to FFH)
  - SFR's
- The upper 128 bytes and SFRs occupy the same block of Address space although both are separate.
- Internal RAM has 3 distinct areas:
  - four register Banks of 8 byte each.
  - Bit addressable area of 16 bytes
  - General purpose RAM area

## TIMER :

8051 has two 16 bit programmable UP Timers/Counters. They can be configured to operate either as timer or as an event counters.

Names of Two Counters are T0 and T1 respectively. The Timer counter is available in four 8 bit special function Registers, viz, TLO, THO, TL1 and TH1. The operation of timer /counters is controlled by two Special function Registers, TMOD and TCON respectively.

### TMOD (Timer Mode Control) :

Gate	C/F	M1	M0	Gate	C/F	M1	M0
Timer 1				Timer 0			

fig: TMOD register.

TMOD register is not bit addressable.

TMOD Address : 89H.

#### Gate :

This is an OR gate enabled bit which control the effect of INT1/I/O on START/STOP of Timer.

It is set to (1) by program to enable the interrupt to start/stop the timer.

If TR1/I/O in TCON is set and signal on INT1/I/O pin is high then the timer starts counting using either internal clock (timer mode) or external pulses (Counter mode)

c/F : It is used for selection of Counter/Timer mode

$c/F = 1 \rightarrow$  Counter

$c/F = 0 \rightarrow$  Timer.

Mode Select Bits : M<sub>1</sub> and M<sub>0</sub> are Mode select bits.

M <sub>1</sub>	M <sub>0</sub>	Mode
0	0	Mode 0
0	1	Mode 1
1	0	Mode 2
1	1	Mode 3

Mode 0 : 13 bit UP Counter.

$$\begin{array}{l} \text{TLX } 5 \text{ bit} \\ \text{THX } 8 \text{ bit} \\ 5 + 8 = 13 \text{ bit} \end{array}$$

Mode 1 : Timer operates in 16 bit mode

$$\begin{array}{l} \text{TLX } 8 \text{ bit} \\ \text{THX } 8 \text{ bit} \\ 8 + 8 = 16 \text{ bit} \end{array}$$

Mode 2 (Auto Reload Mode) :

Mode 2 configures Timer register as an 8 bit Counter (TL1) with automatic reload.

Mode 3 :

Timer 1 in mode 3 simply holds its count.

The effect is same as setting TR1 = 0.

Timer 0 in mode 3 establishes TLO and THO as two separate counters.

Control bits TR1 and TF1 are used by Timer 0 THO in mode 3 while TR0 and TF0 are available to Timer 0 (TLO).

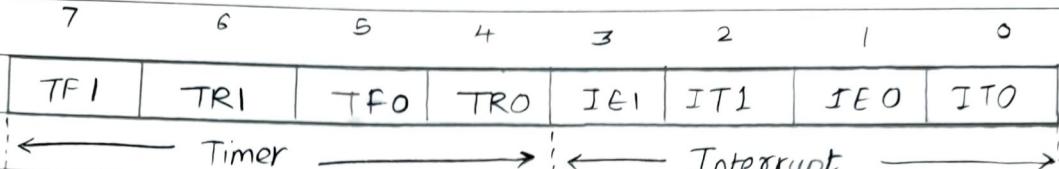


fig : TCON Register.

TF1 : Timer 1 overflow flag.

It is set when timer rolls from all 1s to 0s. It is cleared when processor vectors to execute an ISR Located at address 001BH.

TRI : Timer 1 run Control bit.

Set to 1 to start the timer / counter.

TFO : Timer 0 overflow flag

TRO : Timer 0 run Control bit.

IE1 : Interrupt 1 edge flag.

Set by hardware when an external interrupt edge is detected. It is cleared when interrupt is processed.

IEO : Interrupt 0 edge flag.

IT1 : interrupt 1 type Control bit.

set / cleared by software to specify falling edge / low level triggered external interrupt.

ITO : Interrupt 0 type Control bit

Ques 7 Explain with example addressing mode of 8051

Ans Types :

- 1) Immediate addressing mode
- 2) Direct addressing mode
- 3) Indirect addressing mode
- 4) Register addressing mode
- 5) External addressing mode

Immediate addressing mode :

- This is simplest method to get data
- The sign # indicate data followed is immediate operand

Eg : MOV A, #30H ; copy 30H immediately to accumulator.

MOV P1, #FFH ; copy FFH immediately to Port 1.

MOV DPTR, #123H ; copy 123H immediately to DPTR.

### Direct Addressing mode:

- In this addressing mode the address from the internal RAM is given and the data is to be retrieved from that memory location.

Eg: MOV A, 40H ; copy data from address 40H to the accumulator.

### Indirect addressing mode :

- In this addressing mode the register holds the actual address that will be used in data move operation.
- This address may be 8 bit or 16 bit.
- The R<sub>1</sub>, R<sub>0</sub> of each register used as an index or pointer register.
- @ sign indicate the register act as a pointer to memory.

Eg : MOV A, @R1

Copy the content of memory whose address is specified in R1.

Register Addressing mode :

Each Register bank consist of register R0 to R7. To access the register there are special instructions. In the instruction opode, 3 bits are reserved for specifying one of the eight registers from the Selected Register Bank. The users have to modify the two bits in the PSW, for selecting register Bank.

Eg : MOV A, R2 ; copy the data from register R2 to register A.

External Addressing Mode

(a) Code Access (External ROM access).

- Using these instruction only external program memory can be accessed.
- This addressing mode is preferred for reading look up table in the program memory.
- Either the DPTR or PC can be used as pointer.

Eg : MOVC A, @A+DPTR; This instruction will load accumulator with byte from program memory. The byte from program memory is fetched from the sum of the unsigned 8 bit Accumulator contents & DPTR.

### (b) Data Access (External ROM access):

using this addressing mode the programmer can access the external data memory.

Eg: `MOV @R0, A`; This instruction will copy the data from accumulator to the external memory location, whose address is given by register R0.

- Using R0 and R1 programmer can access external data memory from location 00 H to ff H.
- To Access beyond this limit DPTR is used.

Ques 8 Explain the following instructions:

- 1) JNZ
- 2) PUSH
- 3) ACALL
- 4) RLC
- 5) CJNE.

Ans JNZ → Jump if not Zero.

Mnemonic :: JNZ

Machine Cycles: 2 branch point

Bytes : 2

Function: Jump if accumulator not zero.

operation: This instruction will branch i.e jump to indicated address if the bits in the accumulator are non zero otherwise it will continue with next instruction.

Eg: `JNZ L1`; if  $A \neq 0$ , then jump to L1 and continue execution

⇒ PUSH :

Mnemonic : PUSH <direct>

Machine cycles : 2

Bytes : 2

function : push onto stack.

operation : This instruction copies the data from the source destination onto the stack. The stack pointer is incremented by one and then the data is stored at address pointed by stack pointer.

Eg : PUSH 00H ; if SP = 30H and Data pointer = AC H ∴ after PUSH operation SP = 31H

⇒ ACALL

Mnemonic : ACALL addr11

Machine cycles : 2

Bytes : 2

function : Absolute Call

operation : This instruction unconditionally calls a subroutine at the indicated address. At the end of subroutine the program will resume operation at the opcode address following the call instruction.

Eg : ACALL 200H

; let SP = 0AH . PC = 0239H  
The Label "add" is at program memory location 0200H. After the execution of instruction, ACALL 200H, SP will contain 0CH, the internal RAM location 0BH will contain 39H and 0CH will contain 02H & the PC will contain 0200H.

#### 4) RLC

Mnemonic : RLC A

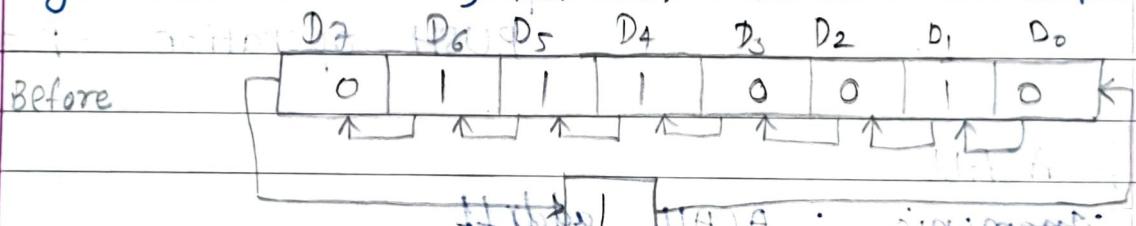
Machine Cycle : 1

Byte : 1

function : Rotate accumulator left through Carry

operation : • This instruction will rotate the eight bit in the accumulator and the Carry flag together by one bit to the left.  
• The 7 bit will move into the Carry register and the original Carry will move in the Bit 0 position.

Eg.: RLC A ; let  $A = 72H$  CY = 1



After the execution of instruction and

$A = 11110010H$  CY = 0

CY = 0

After the execution of instruction and CY = 0

After the execution of instruction and CY = 0

After the execution of instruction and CY = 0

After the execution of instruction and CY = 0

After the execution of instruction and CY = 0

$11110010H = 72H$

After the execution of instruction and CY = 0

5) CJNE : compare Jump not equal.

Mnemonic : CJNE A, direct, rel

Machine Cycles : 2  
Bytes : 3.

function : Compare and Jump if not equal.

operation : This instruction compares the magnitude of Accumulator and magnitude of memory location whose direct address is provided in instruction and jump to the indicated address if magnitudes are unequal.

function Eg: CJNE A, 60H, L5

let  $A = 75H$  and Content of memory location  $60H = 44H$  then the inst<sup>n</sup> will jump to L5 as  $A \neq 60H$ ; i.e. Contents of Accumulator  $>$  content of memory location  $60H$ .

Ques 9. Explain Interrupt structure in 8051.

Ans. • The mc 8051 supports 5 interrupts. These interrupts are automatically generated by internal operations and two interrupts are generated by external signal provide.  
• 8051 has 2 hardware interrupt :  $\overline{INT0}$   $\overline{INT1}$

3 software interrupt : TFO  
TFI

R<sub>I</sub> and T<sub>I</sub>

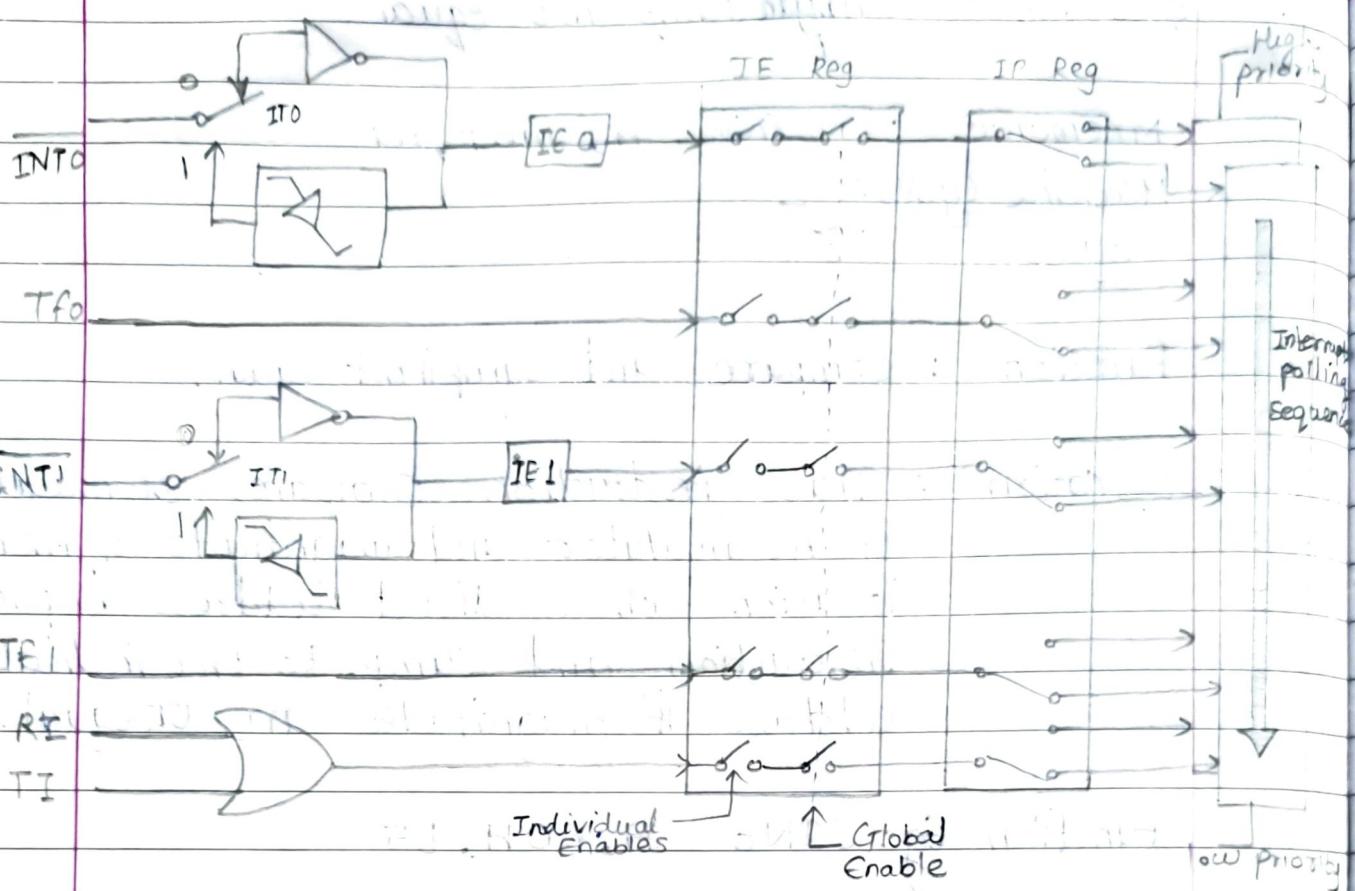


Fig: 8051 b) Interrupt structure and control system

The programmer is able to change the control bits in the Interrupt Enable register (IE), Interrupt priority register (IP) and Timer control register (TCON). By setting or clearing the bits in these register the program can block any or all the interrupts.

- Timer flag interrupt:

When the timer/ counter overflows, the corresponding timer flag TFO and TFI is set to 1

The flag is cleared to 0 when the interrupt generates program call to subroutine in the memory.



### • serial port Interrupt :

The serial port interrupt is generated because of RI and TI. These bits are logically ORed, to provide a single interrupt to the processor.

The TI bit in the SCON register is set when a data byte is Transmitted and RI bit in the SCON register is set when a data byte is received.

The Serial port Interrupts RI and TI are not cleared like the Timer interrupts. When interrupt generates program call. so the program that deals with serial communication must reset or clear the RI and TI bit to 0 to enable next data communication operation.

### • External Interrupts :

The Two interrupts that are generated by external circuits are INT0 and INT1. The inputs on the pins of these interrupts sets the interrupt flags IE0 and IE1 in TCON register. This interrupt may be edge triggered or level Triggered.

### - Interrupt Vector Address :

source	Interrupt Vector Add (ROM location)
① RESET	0000 H
② INT0	0003 H
③ TFO	000B H
④ INT1	0013 H
⑤ TFI	001B H
⑥ RI and TI	0023 H

○ IE register :

D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
EA	-	-	ES	ETI	EXI	ETO	EXO

EA [IE.7]  $\rightarrow$  EA = 0, no interrupt will be acknowledged

EA = 1, each interrupt source is individually enable or disable by setting or clearing its enable bit

ES [IE.4]  $\rightarrow$  serial port interrupt enable bit

ETI [IE.3]  $\rightarrow$  Timer 1 interrupt 1 enable bit

EXI [IE.2]  $\rightarrow$  External interrupt 1 enable bit

ETO [IE.1]  $\rightarrow$  Timer 0 interrupt enable bit

EXO [IE.0]  $\rightarrow$  External interrupt 0 enable bit

○ IP register :

D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
-	-	-	PS	PTI	PX1	PT0	PX0

IP. 7, IP. 6, IP. 5  $\rightarrow$  Reserved

[IP. 4] PS  $\rightarrow$  serial port interrupt priority bit

[IP. 3] PTI  $\rightarrow$  Timer 1 interrupt priority bit

[IP. 2] PX1  $\rightarrow$  External interrupt 1 priority bit

[IP.1] PTO  $\rightarrow$  Timer 0 interrupt priority bit

[IP.0] PX0  $\rightarrow$  External interrupt 0 priority bit.

Ques 10. Explain Timer / Counter mode of 8051 uc in Detail.

Ans: Mode 0 :

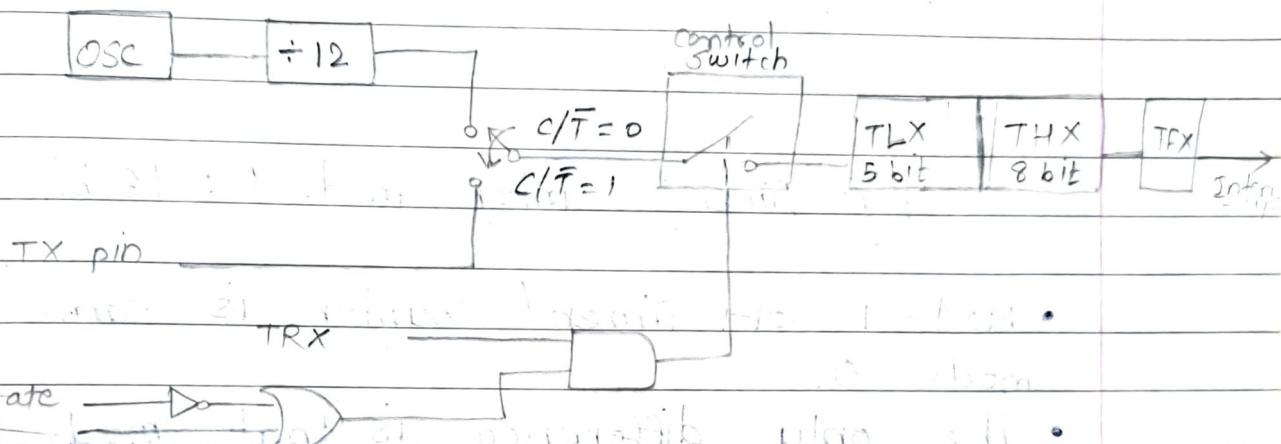


Fig: Timer/ Counter mode 0 : 13 bit counter.

- In this mode timer operates as a 13 bit register (TL - 5 bits and TH - 8 bits)
- The above figures shows Timer / counter in mode 0.
- The Timer is enabled when  $TR = 1$ ,  
 $Gate = 0$ ,  $\overline{INTX} = 1$

Mode 1 :

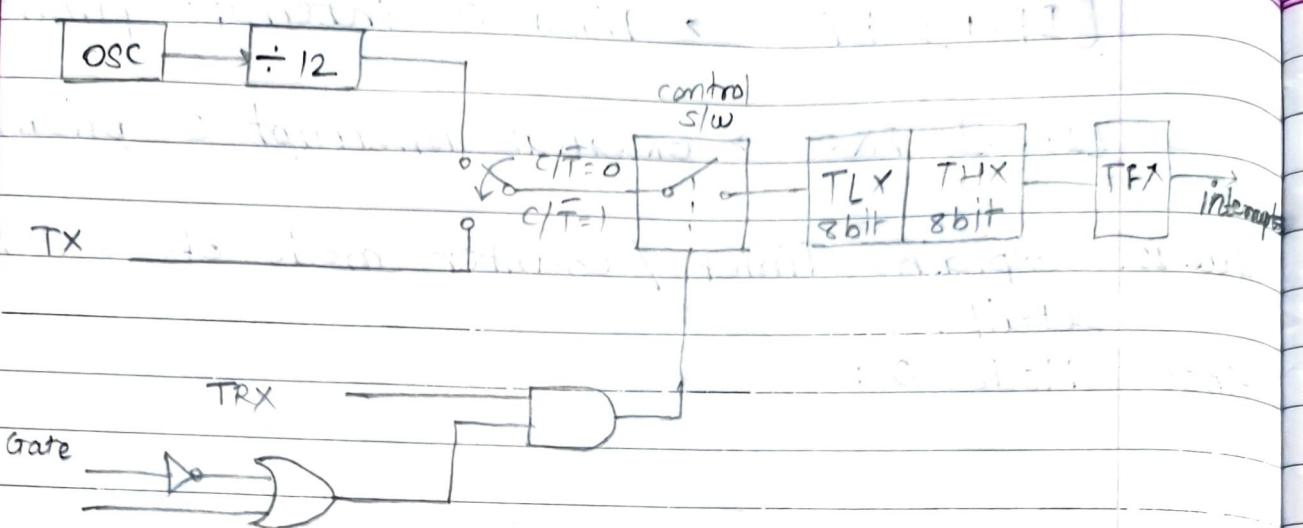


Fig: Timer / Counter mode 1 : 16 bit Counter.

- Mode 1 of Timer / Counter is same as mode 0.
- The only difference is that mode 1 has 16 bit timer / counter.  $TLX = 8 \text{ bit}$  and  $TRX = 8 \text{ bit}$ .

Mode 2: 8 bit timer + 8 bit auto reload.

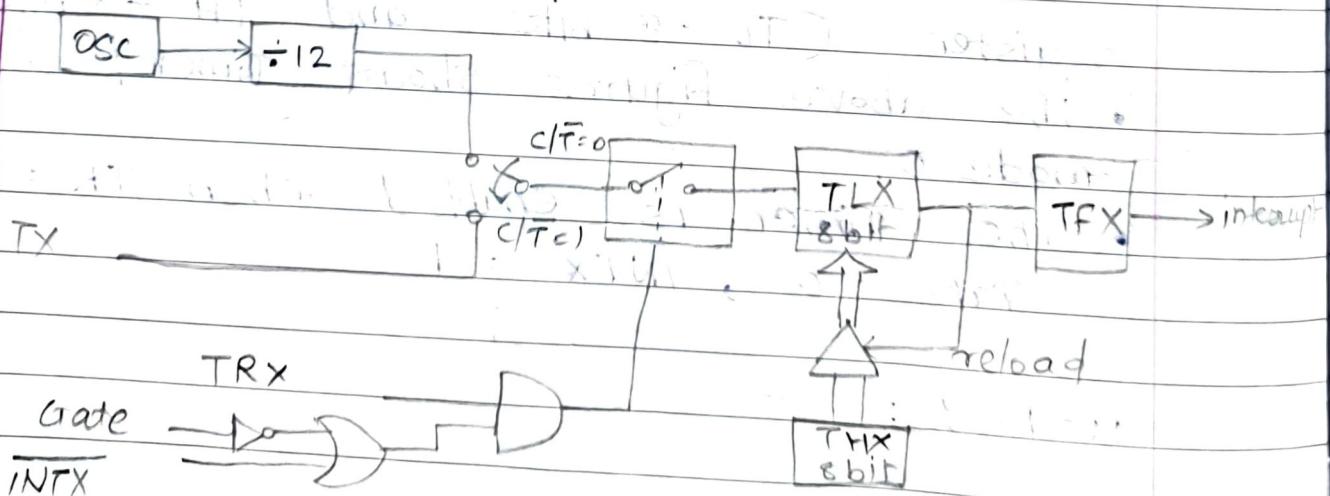


Fig: Timer / Counter mode 2 : 8 bit Auto reload

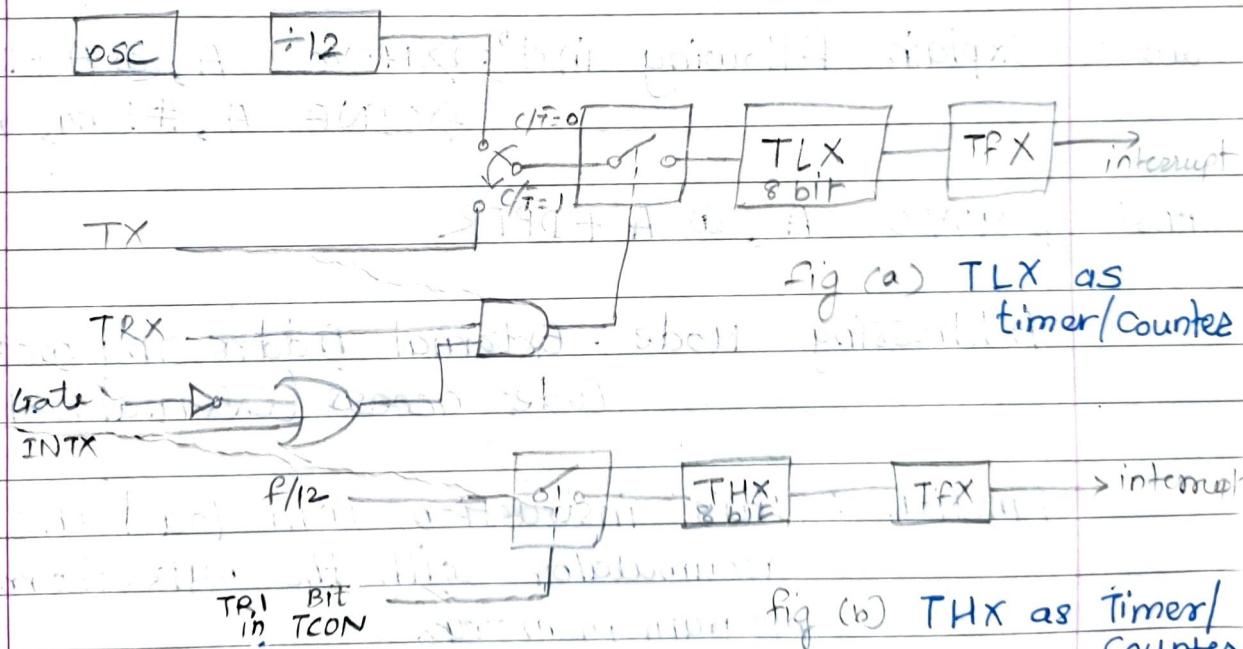
- The Timer/ Counter register is configured as an 8-bit counter with Auto reload facility.

- The TLX act as a basic timer/ counter.
- In autoreload mode TH is loaded.

- When the timer starts working it keeps on incrementing and it will overflow. This will set the timer interrupt flag TFX and it also reloads the contents of THX to TLX.

- The reloading operation will not alter the content of THX.

### Mode 3 :



- In mode 3 timer 1 is not used.
  - The timer 0 register TLO and THO are configured as two separate 8 bit Counter.
  - When Timer 0 is in mode 3, the timer 1 may be used in modes 0, 1, 2.
- प्राप्ति कोई भी कार्य आरभ करते समय सद्गुरुदेव का ध्यान अवश्य करो।

## Summary :

Mode	Description
Mode 0	13 bit timer ( $TL = 5$ bit, $TH = 8$ bits)
Mode 1	16 bit timer ( $TL = 8$ bit, $TH = 8$ bits)
Mode 2	Reload mode: 8 bit counter. ( $TL = 8$ bit) overflow from $TL$ will set, then reload $TL$ with content of $TH$ .
Mode 3	Configures $TLO$ , $THO$ as two separate counters.

Ques 11 Explain following inst':

- 1)  $\text{MOVC A}, @A + \text{DPTR}$
- 2)  $\text{CJNE A}, \# \text{Data}, \text{code add}$

Ans: 1)  $\text{MOVC A}, @A + \text{DPTR}$

Addressing Mode : External Addressing mode  
Code access [External ROM access]

function : This instruction will load the accumulator with the byte from program memory.

The byte from program memory is fetched from the sum of unsigned 8 bit accumulator contents and contents of DPTR.

2) CJNE A, #data, Code Add:

Addressing mode : Immediate addressing Mode.

Function : Compare and jump if not equal.

Operation : This instruction compares the magnitude of accumulator with magnitude of data specified in the instruction and jump to the indicated relative address if contents / magnitudes are unequal.

Eg: CJNE A, #77H, L1.

suppose A = 44H.

Here 44H < 77H ie not equal.  
so it will jump to the relative address L1.

Que 12. Explain Rotate and swap.

Ans: ① Rotate : 4 Types → 1) RL A  
2) RLC A  
3) RR A  
4) RRC A.

Addressing Mode : Register specific mode  
Machine Cycle : 1  
Bytes : 1