

MPCA LAB8-PARACACHE-DIRECT MAPPING

Q) Consider a direct mapped cache of size 16 bytes with block size 4 bytes. The size of main memory is 256 bytes. Find Number of bits in tag, index and offset. The processor generates requests as follow .1,4,8,5,14,11,13,38,9,B,4,2B,5,6,9,11.Find hit rate and miss rate.

Screenshots:

Write Policies

☒ Write Back ☐ Write Through

☒ Write On ☐ Write Around

Allocate

Cache Size (power of 2)

Memory Size (power of 2)

Offset Bits

DIRECT MAPPED CACHE

➔ Instruction Breakdown

0001	00	01
4 bit	2 bit	2 bit

▣ Memory Block

B. 4 W. 0	B. 4 W. 1	B. 4 W. 2	B. 4 W. 3
B. 5 W. 0	B. 5 W. 1	B. 5 W. 2	B. 5 W. 3
B. 6 W. 0	B. 6 W. 1	B. 6 W. 2	B. 6 W. 3
B. 7 W. 0	B. 7 W. 1	B. 7 W. 2	B. 7 W. 3
B. 8 W. 0	B. 8 W. 1	B. 8 W. 2	B. 8 W. 3
B. 9 W. 0	B. 9 W. 1	B. 9 W. 2	B. 9 W. 3

▣ Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	0001	BLOCK 4 WORD 0 - 3	0
1	1	0000	BLOCK 1 WORD 0 - 3	0
2	1	0000	BLOCK 2 WORD 0 - 3	0
3	0	-	0	0

Instruction

(in hex)#

List of next 10 Instructions

Information

The cycle has been completed.
Please submit another instructions

Next Fast Forward

Statistics

Hit Rate : 38%

Miss Rate : 63%

List of Previous Instructions :

- Load 1 [Miss]
- Load 4 [Miss]
- Load 8 [Miss]
- Load 5 [Hit]
- Load 14 [Miss]
- Load 11 [Miss]
- Load 13 [Hit]
- Load 38 [Miss]
- Load 9 [Miss]
- Load B [Hit]
- Load 4 [Miss]
- Load 2B [Miss]
- Load 5 [Hit]
- Load 6 [Hit]
- Load 9 [Miss]
- Load 11 [Hit]

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Date: 16-03-2023