Course Name: EMBEDDED SYSTEMS I / III

Course Number and Section: **14:332:493:03 / 16:332:579:05**

Year: Spring 2023

Lab Report #: 4

Lab Instructor: Milton Diaz

Student Name and RUID: Atharva Pandhare 203003207

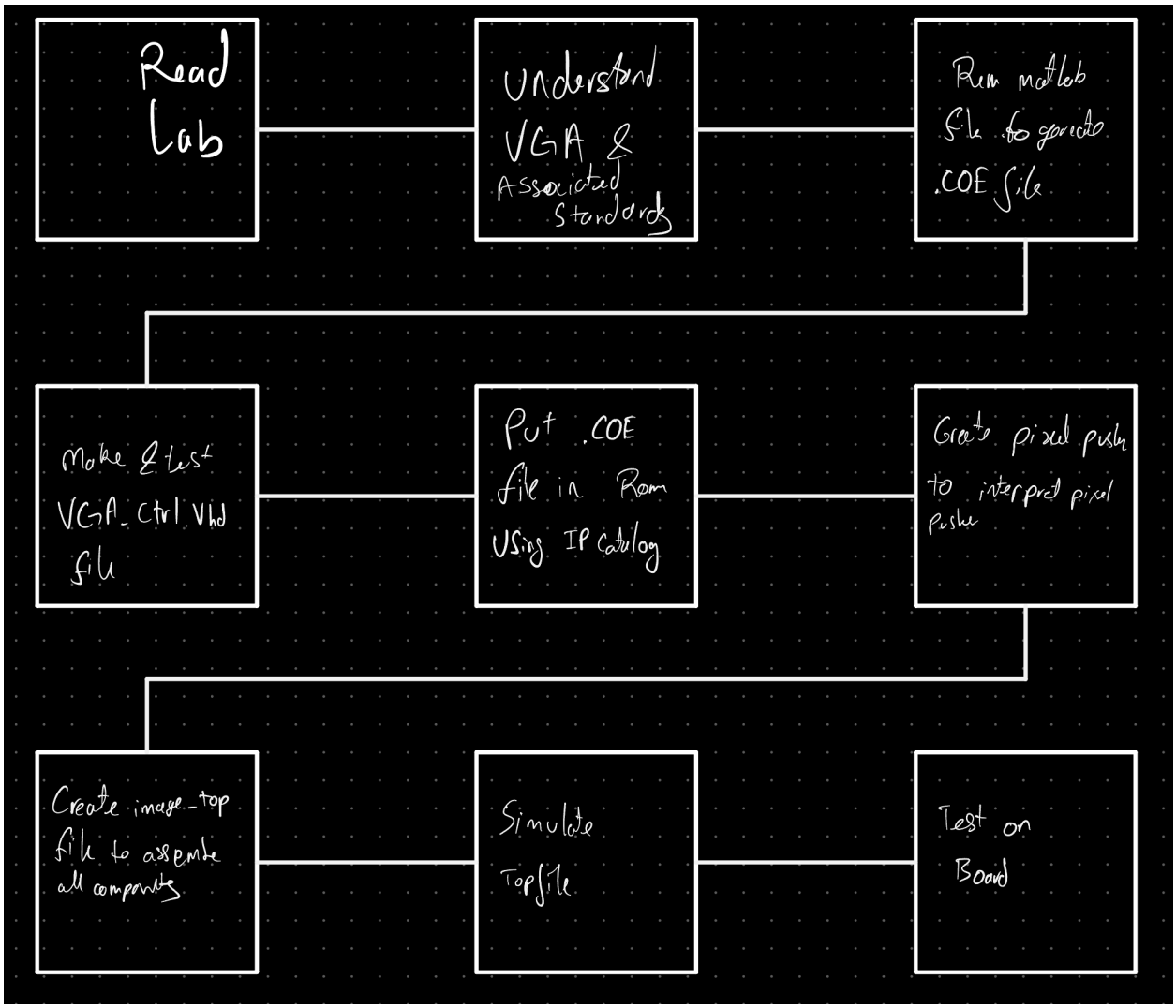
Date Submitted: 04/07/2023

GitHub Link: https://github.com/embedded-systems-1-spring-2023-labs/lab-4-AtharvaPan265

Purpose/Objective:

The purpose of of this lab is to utilize the VGA analog video standard in order to produce a static image on a display. The timing signals and ROM addressing will all be driven by a combination of counters, which prove to be one of the most versatile components in digital design. This is to be done by creating components that use protocols to convert 8 bit data from the ROM into RGB values for the VGA analog standard.

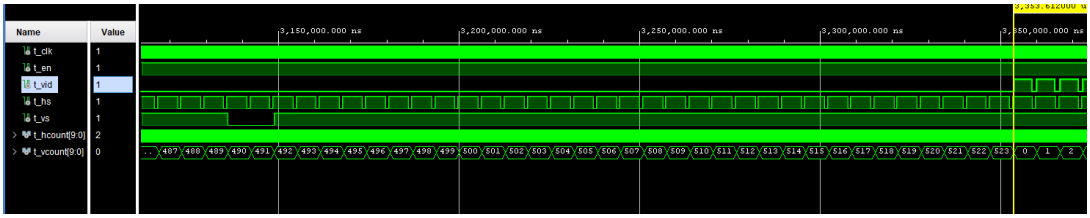
Theory of Operation:



Simulation Waveforms: <screenshots of simulation results/waveforms>

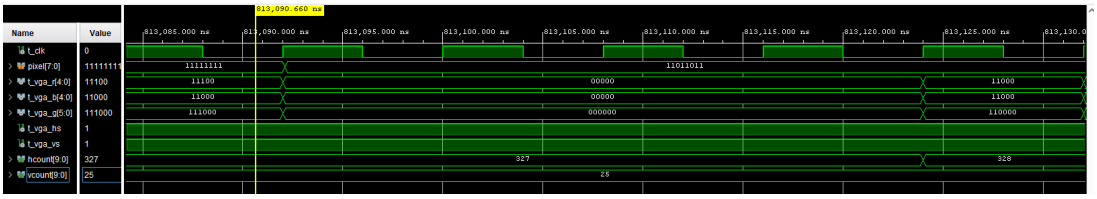
a) VGA_CTRL

i)



b) IMAGE_TOP

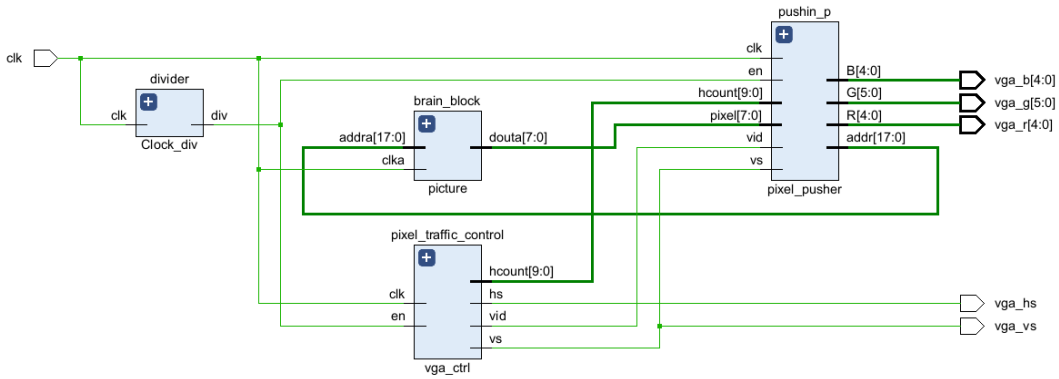
i)



Vivado Schematics: <Note: If there are multiple parts of the lab, submit the required **Schematics** and Utilization **Table** for each part of the lab.>

c) Vivado Elaboration Schematic

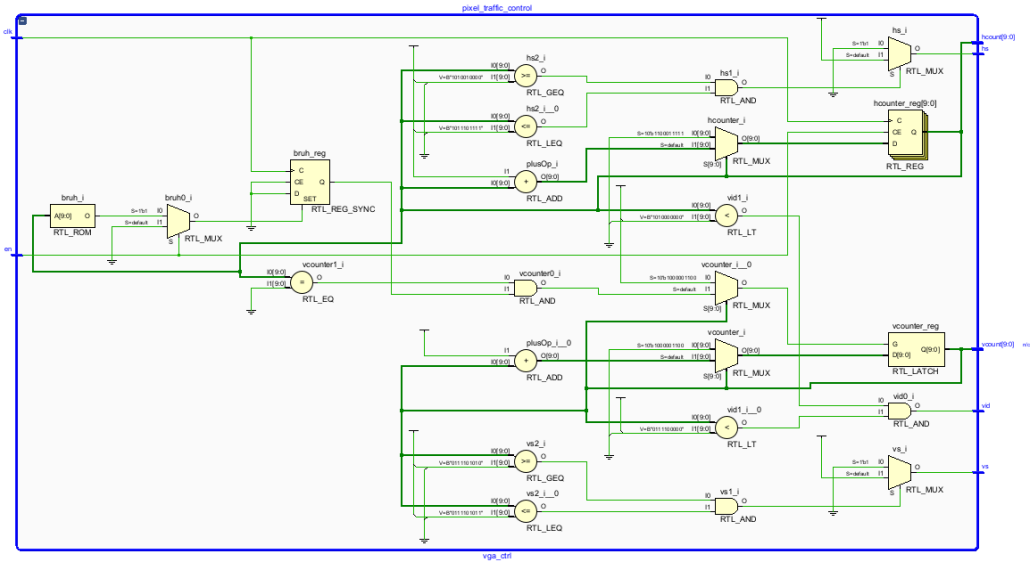
i) IMAGE_TOP



1)

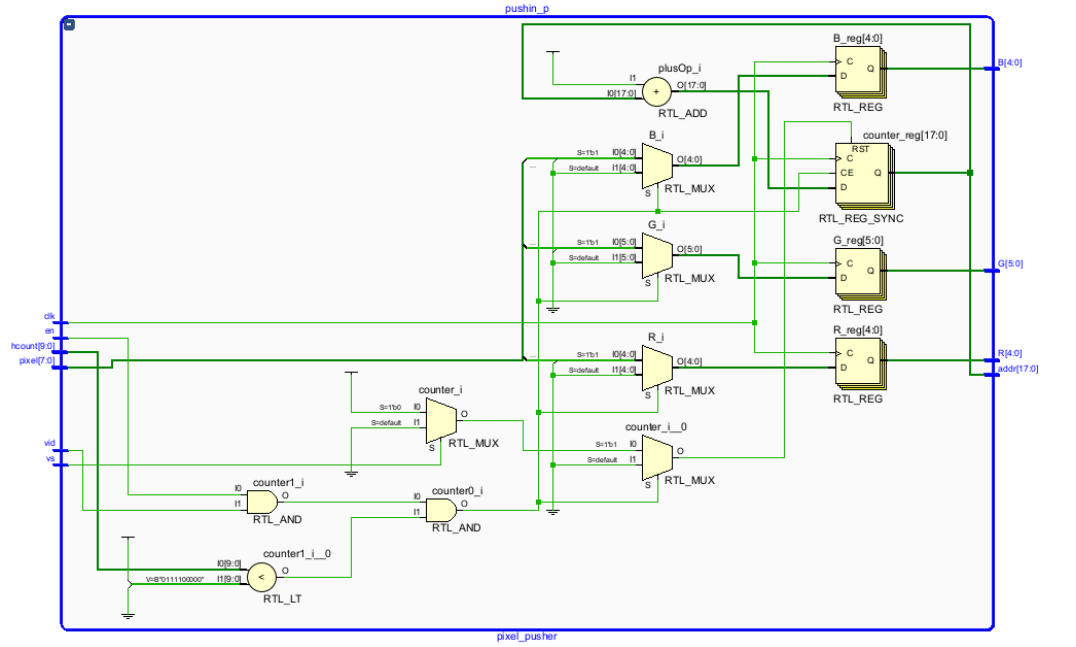
ii) VGA_CTRL

1)

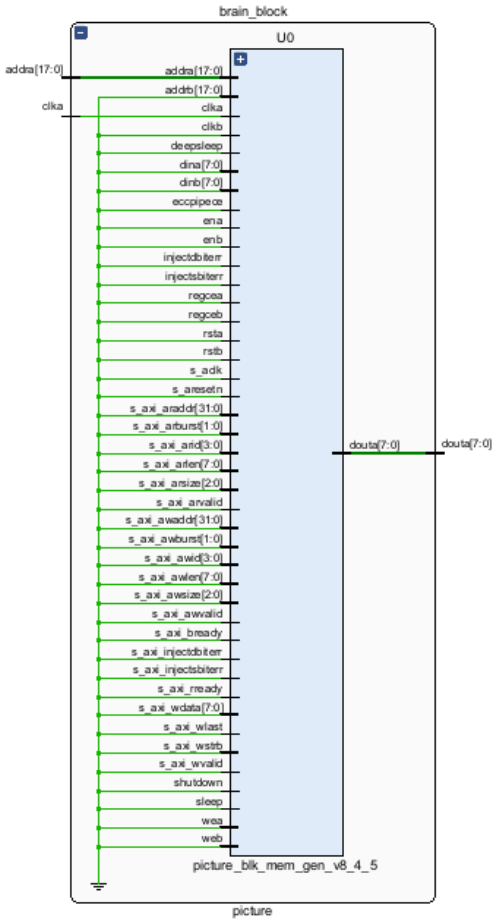


iii) PIXEL_PUSHER

1)

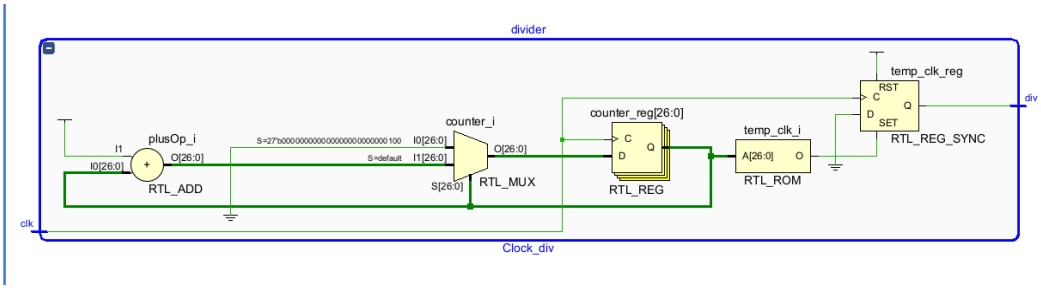


iv) PICTURE



1)

v) CLOCK_DIV

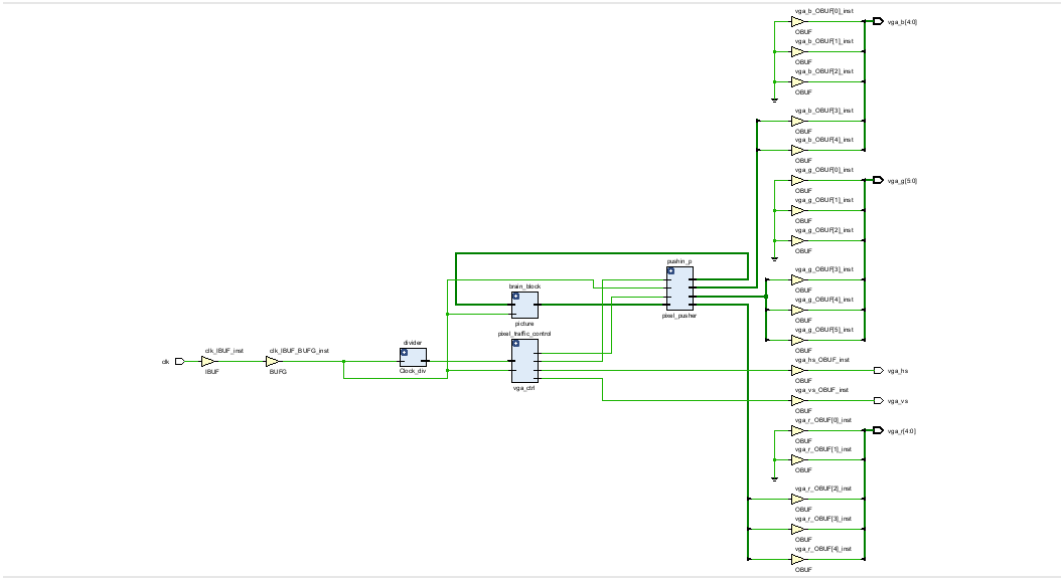


1)

d) Vivado Synthesis Schematic

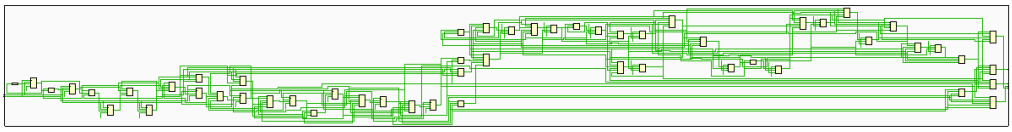
i) IMAGE_TOP

1)

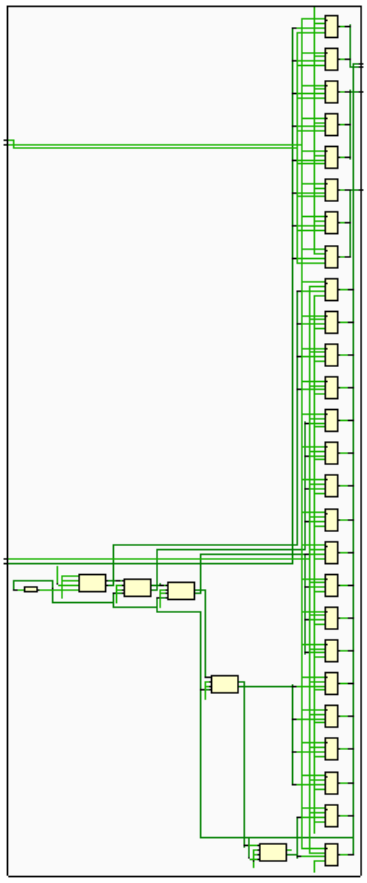


ii) VGA_CTRL

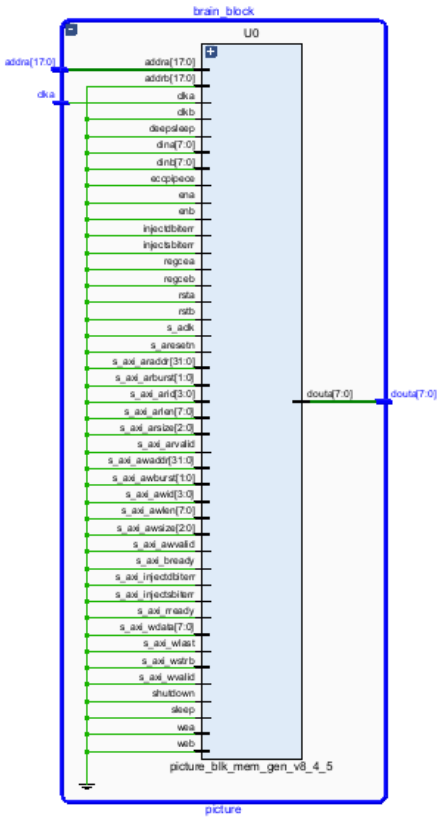
1)



iii) PIXEL_PUSHER

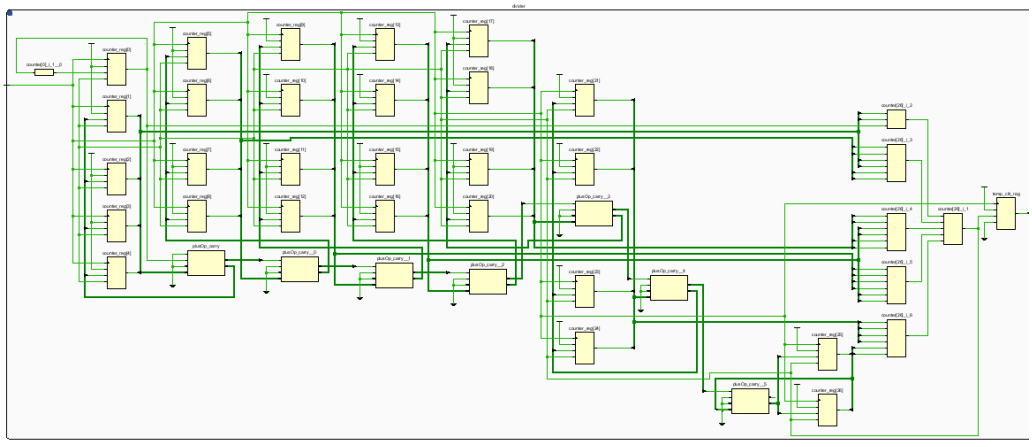
1) 

iv) PICTURE



1)

v) CLOCK_DIV



1)

e) Post- Synthesis Utilization Table

i) IMAGE_TOP

1)

Utilization — Post-Synthesis | Post-Implementation

Graph | Table

Resource	Estimation	Available	Utilization %
LUT	30	17600	0.17
FF	64	35200	0.18
IO	19	100	19.00
BUFG	1	32	3.13

ii) VGA_CTRL

1)

Utilization — Post-Synthesis | Post-Implementation

Graph | Table

Resource	Estimation	Available	Utilization %
LUT	24	17600	0.14
FF	10	35200	0.03
IO	25	100	25.00
BUFG	1	32	3.13

iii) PIXEL_PUSHER

1)

Utilization — Post-Synthesis | Post-Implementation

Graph | Table

Resource	Estimation	Available	Utilization %
LUT	5	17600	0.03
FF	26	35200	0.07
IO	51	100	51.00
BUFG	1	32	3.13

iv) CLOCK_DIV

1)

Utilization — Post-Synthesis | Post-Implementation

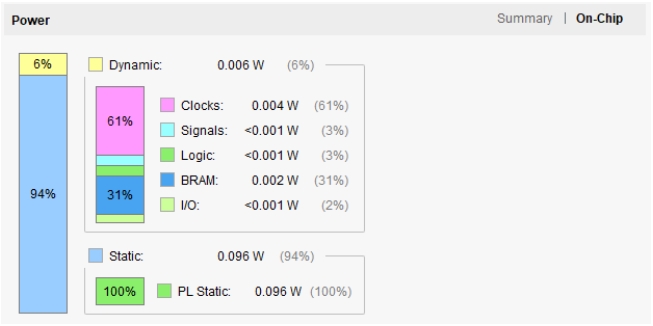
Graph | Table

Resource	Estimation	Available	Utilization %
LUT	6	17600	0.03
FF	28	35200	0.08
IO	2	100	2.00
BUFG	1	32	3.13

f) On-Chip Power Graphs

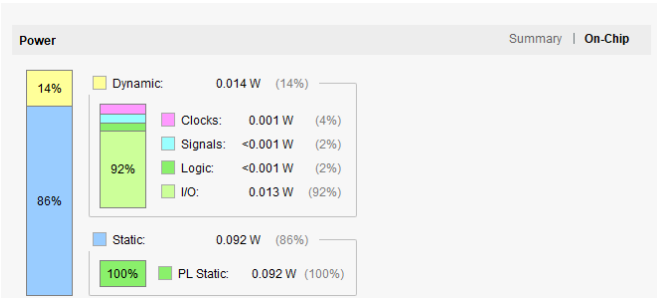
i) IMAGE_TOP

1)



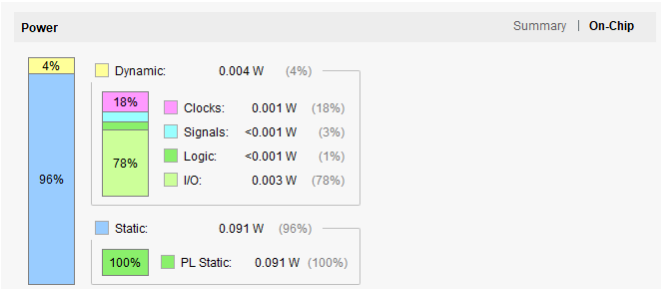
ii) VGA_CTRL

1)



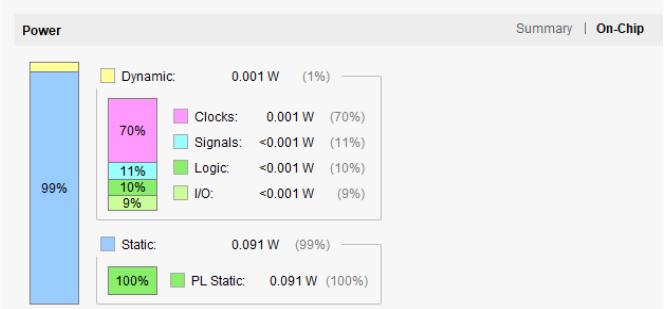
iii) PIXEL_PUSHER

1)



iv) CLOCK_DIV

1)



g) Xdc changes

i) I had to uncomment the clock and the vga parts of the constraints

Conclusion:

I learned about how VGA protocols are used to output images to screens and how to modify 8 bits into RGB for the VGA protocol by doing a lab and reading the associated materials. During the lab, I created a VGA output using the zybo and modifying the 8 bits from the coe file generated by the MATLAB script and outputting it into RGB values. This combined with the diligent docs I was able to get an understanding of how VGA connectors work.

Follow Up:

I had some trouble with the printing because I was having trouble with vertical framing, I believe I fixed it, this will be tested in the lab on monday.