The operation or task that must perform by CPU are:

Fetch Instruction: The CPU reads an instruction from memory.

Interpret Instruction: The instruction is decoded to determine what action is required.

Fetch Data: The execution of an instruction may require reading data from memory or I/O module.

The operation or task that must perform by CPU are

Process data: The execution of an instruction may require performing some arithmetic or logical operation on data.

Write data: The result of an execution may require writing data to memory or an I/O module.

- To do these tasks, the **CPU needs to store** some data temporarily.
- It must remember **the location of the last instruction** so that it can know where to get the next instruction.
- It needs to **store instructions and data temporarily while an instruction is being executed.**
- i.e., the **CPU needs a small internal memory**. These storage location are generally referred as **registers.**

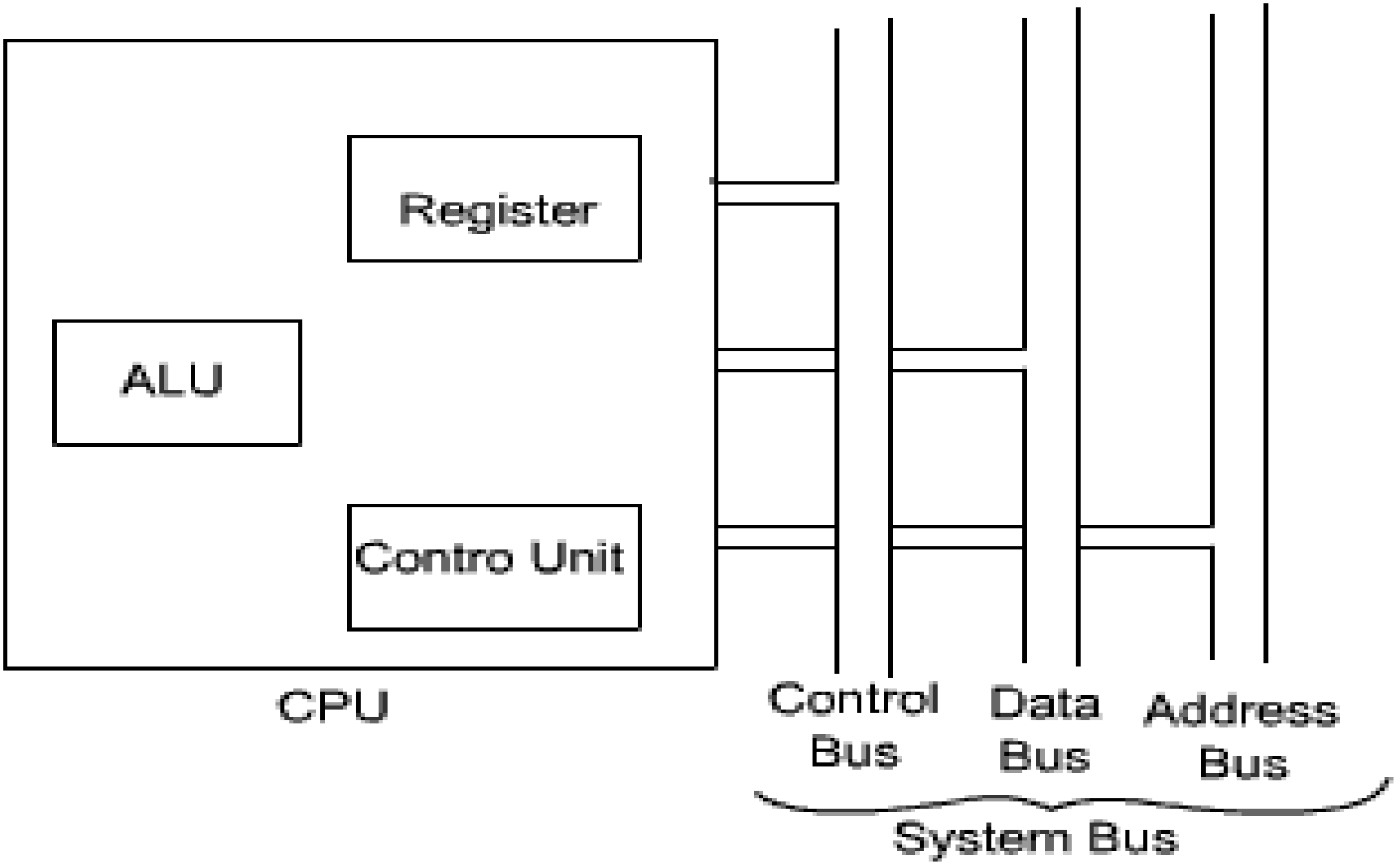
- The major components of the CPU are an ***arithmetic and logic unit (ALU)*** and a ***control unit (CU).***
  - The ALU does the ***actual computation or processing of data.***
  - The CU controls ***the movement of data and instruction into and out of the CPU and controls the operation of the ALU.***

- The CPU is connected to the rest of the system through ***system bus.***
- Through system bus, data or information gets transferred between the CPU and the other component of the system.

The system bus may have three components:

1.Data Bus
2.Address Bus
3.Control Bus

The internal organization of CPU in more abstract level is shown in the Figure



Register Organization

- At the highest level of memory hierarchy, ***memory is faster, smaller and more expensive***.
- Within the CPU, there is a set of registers which can be treated as a memory in the highest level of hierarchy.

The user-visible registers can be categorized as follows:

General Purpose Registers
Data Registers
Address Registers
Condition Codes

Different machines will have different register organizations and use different terminology.

The most commonly used registers which are part of most of the machines and are essential for instruction execution:

Program Counter (PC)
Instruction Register (IR)
Memory Address Register (MAR)

Program Counter (PC)

Program Counter (PC): Contains the address of an instruction to be fetched.

Typically, the PC is updated by the CPU after each instruction fetched so that it always points to the next instruction to be executed.

A branch or skip instruction will also modify the contents of the PC.

Instruction Register (IR)

Instruction Register (IR): Contains the instruction most recently fetched.

The fetched instruction is loaded into an IR, where the opcode and operand specifiers are analysed.

Memory Address Register (MAR)

Memory Address Register (MAR): Contains the address of a location of main memory from where information has to be fetched or information has to be stored.

Contents of MAR is directly connected to the address bus.

□

Memory Buffer Register (MBR)

Memory Buffer Register (MBR): Contains a word of data to be written to memory or the word most recently read.

Contents of MBR is directly connected to the data bus.

It is also known as Memory Data Register(MDR).

Processor Status Word

All CPU designs include a register or set of registers, often known as the ***processor status word (PSW)***, that contains status information.

The PSW typically contains condition codes plus other status information.
Common fields or flags include the following
Sign: Contains the sign bit of the result of the last arithmetic operation.
Zero: Set when the result is zero.
Carry: Set if an operation resulted in a carry (addition) into or borrow (subtraction) out of a high order bit.

Equal: Set if a logical compare result is equal.

Overflow: Used to indicate arithmetic overflow.

Interrupt enable/disable: Used to enable or disable interrupts.

Supervisor: Indicate whether the CPU is executing in supervisor or user mode

Execution of one instruction requires the following three steps to be performed by the CPU

1.Fetch the contents of the memory location pointed at by the PC. The contents of this location are interpreted as an instruction to be executed.
Hence, they are stored in the instruction register (IR).
Symbolically this can be written as:

$$IR = [\,[PC]\,]$$

2. Increment the contents of the PC by 1.

$$PC = [PC] + 1$$

3.Carry out the actions specified by the instruction stored in the IR.

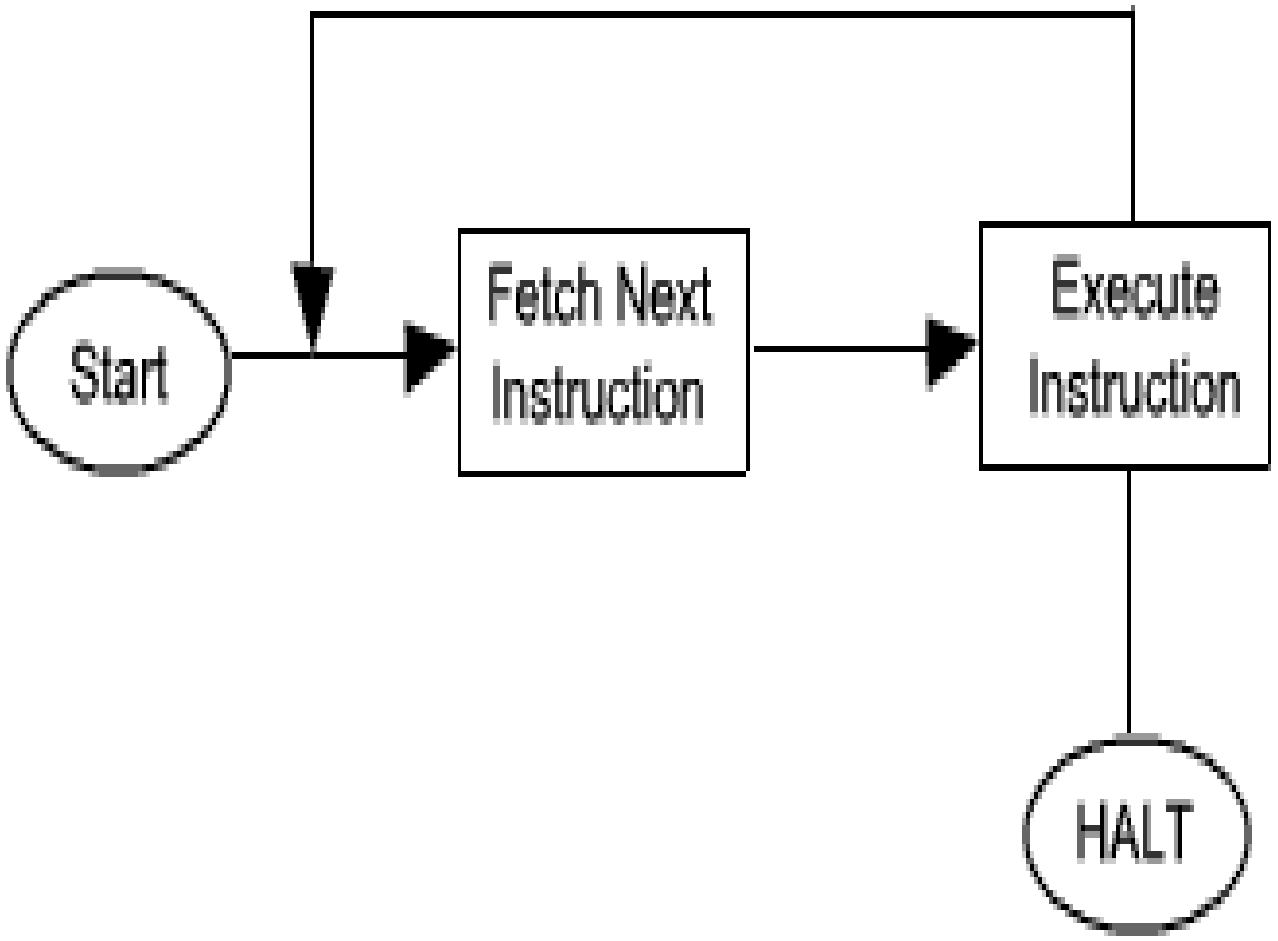
The first two steps are usually referred to as the fetch phase and the step 3 is known as the execution phase.

Fetch cycle basically involves read the next instruction from the memory into the CPU and along with that update the contents of the program counter.

In the execution phase, it interprets the opcode and perform the indicated operation.

The instruction fetch and execution phase together known as instruction cycle.

The basic instruction cycle

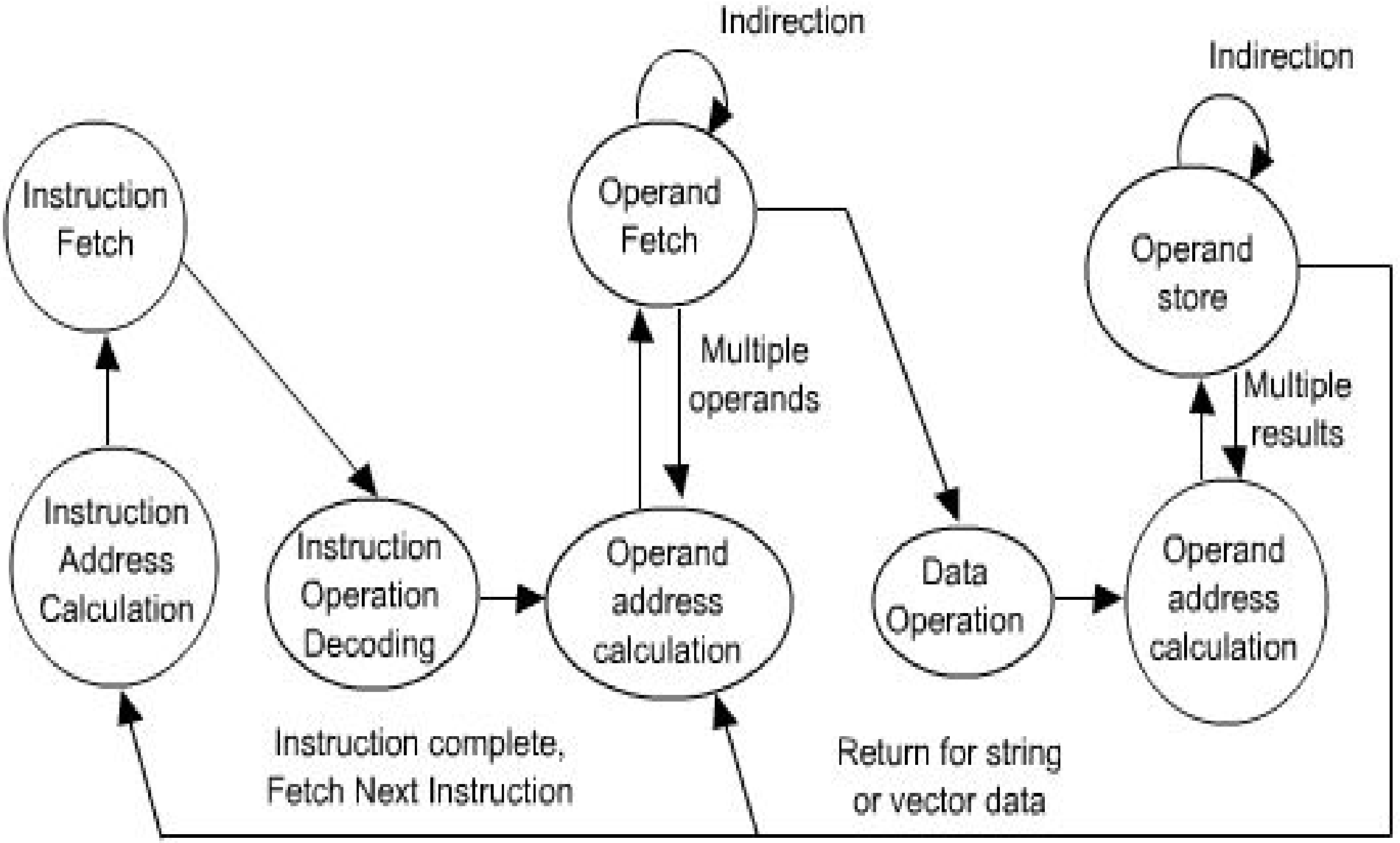


In cases, where an instruction occupies more than one word, step 1 and step 2 can be repeated as many times as necessary to fetch the complete instruction.

In these cases, the execution of a instruction may involve one or more operands in memory, each of which requires a memory access.

Further, if indirect addressing is used, then additional memory access are required.

State Diagram



Design of Control Unit

To execute an instruction, the control unit of the CPU must generate the required control signal in the proper sequence.

To generate the control signal in proper sequence, a wide variety of techniques exist. Most of these techniques, however, fall into one of the two categories

Hardwired Control
Microprogrammed Control.

Hardwired Control

In this hardwired control techniques, the control signals are generated by means of hardwired circuit.

The main objective of control unit is to generate the control signal in proper sequence.