EE518 Analog IC design

Design the schematic of a Low Power 2-stage Operational Transconductance Amplifier (OTA) with RC compensation in GPDK 45nm technology (differential input, single ended output) to meet the following specifications:

- DC gain ≥ 48 dB
- Unity gain frequency ≥ 70 MHz
- Output voltage swing ≥ 0.6 Vpk−pk
- Slew rate ≥ 60 V/µs
- Phase Margin ≥ 60^0
- Input referred spot noise (at 10 MHz) ≤ 80 nV/√Hz
- Input referred spot noise (at 0.1 MHz) ≤ 90 nV/√Hz
- Input Common mode voltage = 0.6 V
- Output load capacitance = 1 pF (From analogLib)
- VDD = 1.2 V
- Power consumption ≤ 0.25 mW

Please note the following:

Use native MOS transistor "nmos1v_nat" for the input differential pair.

Use four terminal transistors in your schematic.

Use DC parameter "betaeff" from DC analysis. betaeff = $\mu_n C_{ox}(W/L)$

λ_n for Low VT transistor 45 nm channel length = 0.585 V^{-1}

λ_p for Low VT transistor 45 nm channel length = 0.41 V^{-1}

λ_n for native VT transistor 300 nm channel length = 0.694 V^{-1}

For generation of bias voltages of the current sources in both stages, use current mirror circuits. You are allowed to use **only one** ideal current source provided in the test bench.

You must prepare a detailed report with clear screenshots, annotations and explanations wherever required. Follow the steps below and include below mentioned details.

1. Hand calculations

- Do proper hand calculations to meet the given specifications for the initial design.
- Show all the hand calculations and equations in your report.
- Tabulate all the aspect ratios and resistor, capacitor values.

2. DC Operating point

- Open the testbench TB_DC_OP and run the simulation from it'sADE-XL window
- Take a screenshot of the schematic with Operating point annotation of each transistor.
- Please note that all transistors should be in saturation.

- Take a screenshot of the schematic showing **region** of operation of all the transistors

3. Stability Analysis

- Open the testbench TB_STB_LG and run the simulation from it's ADE-XL window.
- Plot the Bode magnitude and phase plot. Take a screenshot clearly showing the DC Gain, f-3dB (-3dB frequency) and unity-gain frequency and phase margin.
- In the ADE-XL window, under the Output column right click on Loop Gain dB20 -> Print -> Stability Summary. Attach a clear screenshot of the same.

4. AC analysis: Differential Gain

- Open the testbench TB_AC_DM and run the simulation from it's ADE-XL window.
- Plot the Closed Loop gain and phase plot.
- Using this testbench, Run DC analysis and show the input referred systematic offset.
- Take a screenshot of the schematic with DC operating points annotated for each transistor.

5. AC analysis: Common mode gain

- Open the testbench TB_AC_CM and run the simulation from it'sADE-XL window.
- Plot the open loop CM gain of the OTA with clear labels. Report the CMRR of the OTA by using the differential gain simulated earlier.

6. Transient analysis: Sinusoidal input

- Open the testbench TB_TRAN_SIN and run the simulation from it's ADE-XL window.
- With the OTA in unity gain feedback mode, a sinusoidal signal of 0.6 Vpk-pk, 1 MHz frequency is applied. Plot the input and output transient waveform clearly annotating the peak voltages and take a screenshot of the same.

7. Transient analysis: Step input

- Open the testbench TB_TRAN_SLEW and run the simulation from it's ADE-XL window.
- Measure the slew rate and clearly show the output plot in the slewing region with cursors.
- Measure and report the settling time, ts for 1% accuracy.

8. Noise analysis

- Open the testbench TB_NOISE and run the simulation from it's ADE-XL window.
- Show the input referred noise PSD from 10kHz to 300MHz band. Clearly show the input referred noise in the plot (with marker) at 1MHz and 10 MHz.
- Report the integrated noise and noise contributions. (Under output column (Right Click) Print -> Noise Summary. Scroll down and take a screenshot of the summary only. **Use the settings shown below**

9. Summary of results obtained

Tabulate all the OTA Specifications achieved by your design from Q2 to Q8 in typical corner as shown below: [Typical corner: TT, 27^0C]

Q.No	Parameters	Value (Unit)
2	Power Consumption	
3	DC gain	
	f-3dB	
	Unity Gain frequency	
	Phase margin	
4	Closed Loop Gain	
	f-3dB	
	Input referred offset (DC analysis)	
5	Common-mode gain	
	CMRR	
6	Output Swing (Vpk−pk)	
7	Slew rate	
	Settling Time (1% accuracy)	
8	Input referred spot noise (at 1 MHz)	
	Input referred spot noise (at 10 MHz)	
	Total summarized Noise	
	Total input referred Noise	