The Stochastic-Decay Bit (sd-bit):
Athermal Probabilistic Computing via Controlled Quantum Decay

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November 4, 2025

Abstract

Modern artificial intelligence, particularly in stochastic modeling and generative tasks, is increasingly constrained by the energy and time costs of deterministic (von Neumann) architectures. While probabilistic computing, embodied by the "p-bit," offers a path forward, current implementations rely on classical thermal noise (Johnson-Nyquist noise) as a source of randomness. This approach suffers from significant temperature dependency, requiring active calibration and stabilization against thermal drift.

We propose a novel probabilistic hardware device, the **Stochastic-Decay Bit (sd-bit)**, which harnesses a quantum-mechanical process: controlled radioactive decay. This concept reframes the infamous 1970s Intel soft-error "bug"—where alpha particles from packaging impurities corrupted memory—as a controllable feature.

An sd-bit consists of an intentionally unstable memory cell coupled to a microscopic, low-activity radioisotope. The constant, random emission of particles provides an **athermal (temperature-independent)** source of fluctuation. An applied bias voltage controls the energy barrier for bit-flips, allowing the sd-bit to rapidly sample states '0' and '1' with a tunable probability.

This paper outlines the architecture, mechanism of action, and theoretical advantages of the sd-bit. We posit that this device can serve as the foundation for a new class of Probabilistic Processing Units (PPUs) that are more stable, scalable, and energy-efficient than their thermal-based counterparts, enabling hardware-native Bayesian networks, Boltzmann machines, and large-scale combinatorial optimization.

1 Introduction

The computational demands of generative AI, Bayesian inference, and complex system simulation are fundamentally probabilistic. Traditional deterministic hardware (CPUs, GPUs) must expend significant energy to simulate randomness using pseudo-random number generators (PRNGs). This simulation is a core bottleneck.

A promising alternative is the **p-bit (probabilistic bit)** [1], a hardware device that rapidly fluctuates between 0 and 1, where the time-averaged value represents a tunable probability $p \in [0, 1]$. An interconnected fabric of p-bits can form a **Probabilistic Processing Unit (PPU)**, a hardware accelerator capable of natively solving optimization and sampling problems [2].

1.1 The "Thermal Problem"

Current p-bit designs are typically implemented by amplifying the classical thermal noise (Johnson-Nyquist noise) in a resistor or magnetic tunnel junction (MTJ) [3]. The power spectral density of this noise is directly proportional to temperature T.

This dependency, even at room temperature, creates a significant engineering challenge:

- **Thermal Drift:** As the chip heats up from its own operation, the "noise level" changes, skewing the probabilities.

- **Calibration:** Each p-bit must be continuously calibrated to compensate for temperature variations across the die.
- **Energy Overhead:** The amplification and constant calibration circuits consume significant power to manage and compensate for this temperature-dependent noise.

1.2 Inspiration: From Soft Error to Stochastic Engine

In the late 1970s, Intel discovered that trace amounts of Uranium and Thorium in its ceramic chip packaging were emitting alpha particles [4]. These particles, upon striking a DRAM cell, would generate enough charge to flip the bit, causing random, uncorrectable "soft errors."

We propose to turn this bug into a feature. What if the random particle strike was not a high-energy error, but a low-energy, controlled "nudge"? By designing a circuit around this principle, we can harness a quantum-mechanical process that is fundamentally **athermal**.

2 The Stochastic-Decay Bit (sd-bit) Model

The **Stochastic-Decay Bit (sd-bit)** is a three-component device designed to function as a hardware p-bit, using radioactive decay as its source of fluctuation.

2.1 Hardware Architecture

1. **The Fluctuation Core:** A bistable memory element, such as a modified SRAM cell or a CMOS latch, that is designed with an intentionally low energy barrier (ΔE) separating its two stable states (logical '0' and '1').
2. **The Stochastic Source:** A microscopic, low-activity, solid-state alpha or beta emitter (e.g., a dopant of Americium-241 or Polonium-210) integrated into the substrate or packaging directly adjacent to the Fluctuation Core. Its decay events are governed by a Poisson process with a stable, mean decay rate λ.
3. **The Bias Input (V_{bias}):** A standard voltage input that controls the relative energy levels of the '0' and '1' states, "tilting" the energy landscape.

2.2 Mechanism of Action

The sd-bit operates in a continuous sampling mode:

1. V_{bias} is applied, setting the desired probability. A high V_{bias} lowers the energy of state '1' (E_1) and raises the energy of state '0' (E_0).
2. This "tilt" creates an asymmetric barrier. The barrier to flip from the unfavorable state to the favorable one ($E_{barrier,0\to1}$) is now low, while the barrier to flip back ($E_{barrier,1\to0}$) is high.
3. The Stochastic Source provides a constant, random stream of decay events. Each event imparts a quantum of energy, E_d.
4. If the bit is in the unfavorable state ('0'), even a low-energy E_d is likely sufficient to overcome the low $E_{barrier,0\to1}$, causing a flip.
5. If the bit is in the favorable state ('1'), it will remain there until a rare, higher-energy event (or a constructive summation of events) provides enough energy to overcome the high $E_{barrier,1\to0}$.

2.3 Probabilistic Behavior

The bit rapidly flickers between states. The fraction of time it spends in state '1', $P(S = 1)$, will be proportional to the input V_{bias}. By reading the bit's value at any given moment, we draw a true random sample from a Bernoulli distribution.

The relationship between the bias and the probability follows a sigmoidal (logistic) function, analogous to the Boltzmann distribution in thermal systems:

$$P(S = 1) = \frac{1}{1 + e^{-\beta_{eff}(V_{bias} - V_{offset})}}$$

The crucial difference is the "effective inverse temperature" β_{eff}. In a thermal p-bit, $\beta = 1/kT$. In an sd-bit, β_{eff} is a function of the mean decay rate λ and the average decay energy E_d. It is a characteristic of the device's physical construction, **not its operating temperature**.

3 Advantages over Thermal p-bits

The sd-bit model presents several fundamental advantages, summarized in Table 1.

Table 1: Comparison of Thermal p-bits vs. Stochastic-Decay (sd-bits)

Property	**Thermal p-bit (e.g., MTJ-based)**	**Stochastic-Decay bit (sd-bit)**
Source of Randomness	Classical thermal (Johnson-Nyquist) noise	Quantum-mechanical radioactive decay
Temperature Dependency	**High.** Noise $\propto T$.	**None.** Decay rate λ is a physical constant.
Core Principle	Amplified classical noise	Controlled quantum events
Randomness Quality	High-quality noise	True, non-deterministic randomness
Calibration	Continuous calibration required	Factory-set β_{eff}; no thermal drift
Energy Cost	Amplification + Stabilization + Calibration Overhead	Latch bias + Passive decay

The primary advantage is **athermal operation**. The sd-bit's probabilistic behavior is governed by λ, a fundamental constant of nature, not the chip's ambient temperature. This eliminates thermal drift, simplifies calibration, and dramatically reduces the energy overhead associated with noise management.

4 Applications in Stochastic AI

A PPU built from sd-bits would serve as a powerful co-processor for tasks intractable for deterministic hardware.

- **Bayesian Neural Networks:** Weights can be represented by sd-bits, allowing the network to natively model uncertainty and perform inference through sampling, rather than costly techniques like variational inference.
- **Combinatorial Optimization:** An sd-bit array can physically implement a Boltzmann Machine or Ising model. The solution to a complex problem (e.g., Traveling Salesman,

portfolio optimization) is found by ”annealing” the bias inputs and allowing the system to physically settle into its lowest-energy ground state.

- **Generative Models:** Ideal for sampling-heavy models like Generative Adversarial Networks (GANs) or diffusion models, providing a massive source of parallel, high-quality randomness.

5 Implementation Challenges and Future Work

While conceptually powerful, the physical realization of the sd-bit carries significant engineering challenges.

1. **Fabrication and Integration:** The primary hurdle is the safe and clean integration of radioactive isotopes within a standard CMOS fabrication process. This requires novel packaging and material science, with extreme attention to safety and regulatory compliance.

2. **Source Stability:** The isotope's half-life must be long enough to ensure a stable decay rate λ over the chip's lifetime (e.g., Am-241, $t_{1/2} \approx 432$ years).

3. **Micro-Shielding and Crosstalk:** The device must be designed so that a decay particle from one sd-bit affects *only* its target Fluctuation Core. Any particle escaping to strike adjacent logic would re-Dintroduce the original ”soft error” problem. This requires precise, micro-scale shielding.

Future work will focus on simulation of particle-matter interactions at the nanoscale to determine optimal device geometry, materials, and isotope selection.

6 Conclusion

The **Stochastic-Decay Bit (sd-bit)** is a paradigm for probabilistic computing that leverages a fundamental quantum process as its stochastic engine. By re-imagining a 1970s hardware bug as a core feature, we propose a device that is inherently athermal, stable, and energy-efficient.

This approach moves beyond simulating randomness and instead builds a computational fabric that is natively stochastic. The sd-bit offers a potential path to scalable probabilistic hardware capable of solving the next generation of problems in artificial intelligence.

References

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