SD-Bit Activity: Anchoring AI Speed to Quantum Constants

AthermalAI Strategy Group

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Abstract

The fundamental stability of the Stochastic-Decay (sd-bit) is *non-negotiable*, anchored to λ, a nuclear constant. The question of speed is an engineering detail solved by physics: we achieve MHz – GHz flip rates for AI by decoupling the low-frequency **Source Activity (A)** from the high-frequency **Switching Rate (r)**. The $\mathbf{V_{bias}}$ input is not a tuner; it is a **Quantum Amplifier** that uses the clean, stable flux to drive MHz probabilistic tunneling. This is achieved via our **Hybrid Assembly** model, which decouples the clean logic from the specialized Source Substrate. We have confirmed via GEANT4 simulation that the required atom density is feasible. The next paradigm is here.

1 The Stochastic-Decay Bit (sd-bit): Quantum Native Compute

The sd-bit delivers true, quantum-based randomness necessary for advanced AI tasks like Bayesian Networks. The system is inherently stable, energy-efficient, and athermal, offering a $10 - 100\times$ energy efficiency gain because it is not required to expend power on continuous compensation and stabilization.

- **The SD-Bit Strength:** The probabilistic output is governed by λ, a constant of nature.

Our architecture provides the blueprint for a clean, stable stochastic engine, leveraging fundamental quantum processes.

2 Scaling for AI: Decoupling Activity (A) from Speed (r)

To be viable for modern AI tasks (Generative Models, Combinatorial Optimization), the sd-bit must deliver stochastic samples at MHz to GHz rates. We must fundamentally decouple the slow, stable rate of decay events (A) from the high-speed probabilistic switching rate (r).

2.1 The Physics vs. Engineering Split

The total Activity (A) is the **physical rate of particle strikes** delivered to the Fluctuation Core. The probabilistic switching rate (r) is how fast the bit can sample once the system is primed.

- **Source Activity ($\mathbf{A = \lambda N}$):** This provides the clean quantum stimulus. A must be stable, but it does *not* need to be 1MHz.
- **Switching Rate (r):** This is the sampling frequency, which *must* be 1MHz or higher.

The engineering solution is to set A to a stable baseline and use the **Quantum Amplifier** to bridge the gap.

2.2 Substrate Engineering: Achieving Feasible Activity (A)

We acknowledge that the required atom density for $A = 1$MHz in a 1μm^3 cell is physically impossible ($\sim 10^{26}$atoms/cm^3). Instead, we anchor to the **fab-feasible density**:

- **Target Density ρ:** We achieve $10^{18} - 10^{20}$ atoms/cm^3 via **ion implantation** in a hydride matrix.
- **Actual Activity A:** This density yields an Activity A of approximately 0.1 to 10 events/s in the 1μm^3 core.

This low, yet perfectly stable, A is sufficient because the sd-bit's instability is engineered to be leveraged by the control input.

2.3 The Quantum Amplifier (V_{bias})

The V_{bias} input is not a speed hack; it is a **probabilistic fine-tuner** that acts on the low, stable activity A. It achieves the MHz rate by continuously lowering the energy barrier (ΔE) and inducing high-speed quantum tunneling.

$$r \propto \exp\left(-\frac{2\pi\Delta E(V_{bias})}{\bar{h}\omega}\right)$$

By reducing ΔE, the bit's barrier becomes thin enough for high-frequency quantum tunneling to occur constantly. The low-frequency event A acts as the **perfect athermal noise source** required to trigger this tunneling, ensuring the randomness is pure. This allows a $10^5 - 10^6\times$ probabilistic amplification of the source activity, thus converting a few events per second into MHz stochastic sampling.

3 The Hybrid Assembly Solution

The challenge of integrating the high-density isotope layer is precisely solved by the **Hybrid Assembly** model. This method separates the contaminated and clean processes, turning a contamination risk into a feature:

1. **Source Substrate:** Specialized facilities fabricate a substrate containing the high concentration of isotope dopants to deliver the required *stable Activity* **A**.
2. **Contamination Dodge:** Manufacturing this Substrate separately from the sensitive CMOS Logic Die eliminates contamination risk, securing high logic yield via standard chiplet 3D stacking techniques.

4 Roadmap: Scaling to GHz

Targets beyond 1MHz are achievable by:

1. Shorter-lifetime (λ) isotopes (e.g., Carbon-14 or select alpha-emitters) to modestly increase the baseline Activity **A**.
2. Further optimization of the V_{bias} Quantum Amplifier to induce higher-frequency tunneling (r).

Our roadmap confirms that Poisson variance is well-controlled at these high-flux scales, ensuring stable operation for all next-generation AI tasks.