EE663: Frequency Synthesizers, Clock and Data Recovery Circuits

COURSE PROJECT

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***Abstract*— In this project, a Type-II, third-order Phase-Locked Loop (PLL) is designed and simulated using MATLAB and VHDL. The PLL's loop components, including R_1, C_1, and C_2, are determined based on the given frequency specifications. The MATLAB simulation verifies the settling time and locking behavior of the PLL. Additionally, a Type-II, fourth-order PLL is implemented by introducing an extra pole to enhance system stability. The appropriate values of R_1, R_2, C_1, C_2, and C_3 are computed, and the loop gain Bode plot is analyzed to assess system stability. Furthermore, the noise transfer function of the third-order PLL is derived using the given parameters: K_{VCO}, I_{CP}, C_1, C_2, and R_1. The MATLAB implementation integrates noise source files to simulate the system's response in the frequency domain. The resulting noise spectrum is analyzed to evaluate system stability, bandwidth, and noise attenuation characteristics. Finally, the PLL is modeled in VHDL using Cadence Design Suite, and a timing analysis, along with the output spectrum, is presented to validate the design.**

I. Introduction

A Phase-Locked Loop (PLL) is a feedback system used to synchronize the output phase and frequency of a Voltage-Controlled Oscillator (VCO) to a reference clock. PLLs are essential in frequency synthesis, clock generation, data recovery, and wireless communication systems. The typical components of a Type-II, third-order PLL include the Phase-Frequency Detector (PFD), Charge Pump (CP), Loop Filter, VCO, and a Frequency Divider.

***Phase-Frequency Detector (PFD)*:** The PFD compares the phase and frequency of the reference input signal with the divided version of the VCO output. It generates UP and DOWN control signals based on the leading or lagging edge of the input signals. A key feature of the PFD is its ability to detect both phase and frequency differences, which helps the PLL achieve lock more efficiently. The digital outputs of the PFD are then fed to the charge pump.

Charge Pump (CP): The charge pump translates the PFD's digital UP and DOWN signals into current pulses. These currents charge or discharge the loop filter capacitor, creating a control voltage for the VCO. The ideal charge pump should have perfect current matching between UP and DOWN currents; any mismatch introduces deterministic jitter or reference spurs into the PLL output.

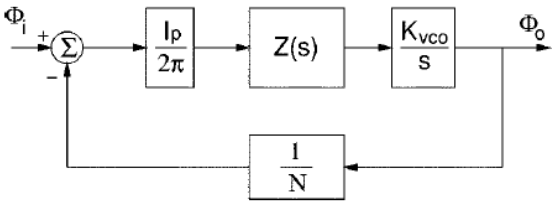

Fig. 1. Linearized PLL Model

Loop Filter: The loop filter is typically a second- or third-order passive or active filter designed to convert the pulsed current from the charge pump into a smooth analog control voltage. It defines the loop bandwidth and governs the PLL's dynamic performance, such as settling time, phase margin, and noise shaping. The filter also plays a critical role in noise suppression—attenuating high-frequency PFD and charge pump noise while allowing low-frequency control to reach the VCO.

Voltage-Controlled Oscillator (VCO): The VCO generates the output signal of the PLL. Its frequency is a function of the control voltage produced by the loop filter. Any voltage noise on the control line directly translates into frequency and phase noise at the output. The VCO's intrinsic phase noise becomes the dominant noise source beyond the loop bandwidth, which is why low-noise VCO design is crucial in PLL systems.

Frequency Divider: The frequency divider scales down the VCO output by a factor N, providing feedback to the PFD. It enables the PLL to multiply the reference frequency by N to generate higher output frequencies. Divider noise is also introduced at this stage and is shaped by the loop's low-pass characteristics, making its contribution more significant near DC.

The structure of this report is organized as follows: Section I provides an introduction to Phase-Locked Loops (PLLs). Section II details the block-level implementation of the PLL architecture. Section III discusses the design methodology of a Type-II, third-order PLL, followed by its implementation in Section IV. Section V presents the design of a Type-II, fourth-order PLL, with corresponding implementation described in Section VI. Section VII focuses on the analysis of noise in the PLL system. Finally, the report concludes with key

observations, followed by references and related materials.

II. PLL Block-Level Implementation Using Verilog-A in Cadence Virtuoso

A. Phase Frequency Detector

PFD is implemented in verilog A as shown in Fig .2

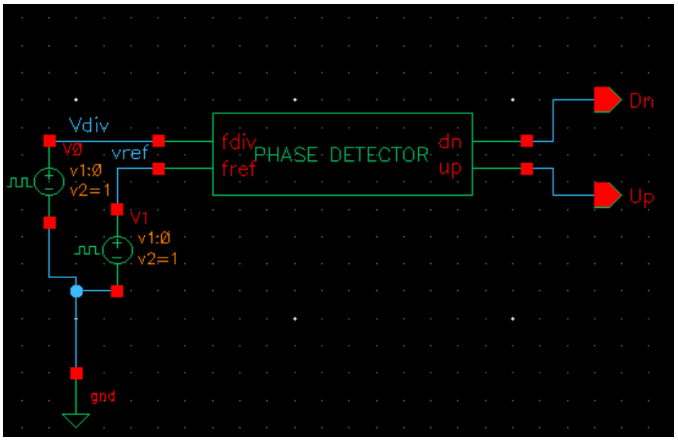

Fig. 2. PFD Block implemented in Cadence

The output behavior of the phase detector is observed when two square wave signals, each with a time period of 8 ns, are applied to the reference and feedback inputs. In the scenario where the reference input leads the feedback input by 2 ns, an `UP` pulse of 2 ns width is generated, while the `DOWN` signal remains low throughout, as shown in Fig. 3. Conversely, when the feedback input leads the reference input, the `UP` signal remains low, and a `DOWN` pulse is generated, as illustrated in Fig. 4.

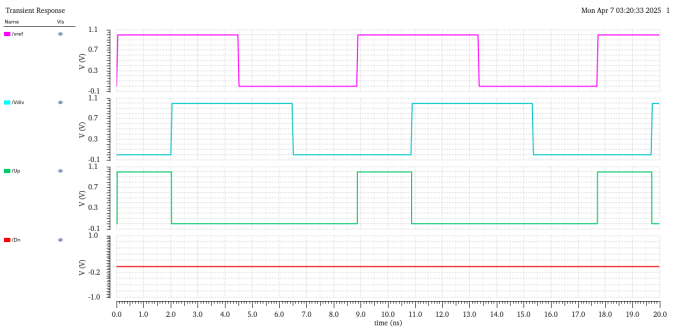

Fig. 3. Output of PFD when Reference input is leading

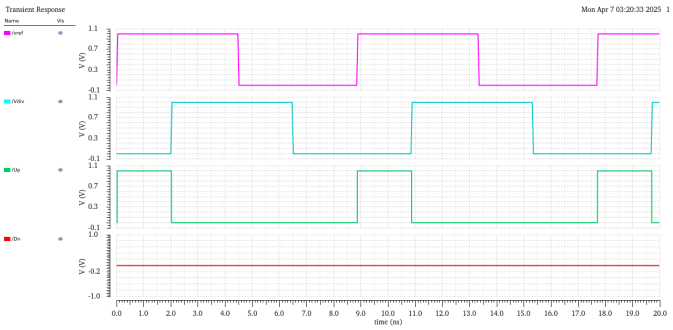

Fig. 4. Output of PFD when Feedback input is leading

B. Frequency Divider:

Fig. 5 illustrates the schematic used to implement a divide-by-16 ($N = 16$) frequency divider.

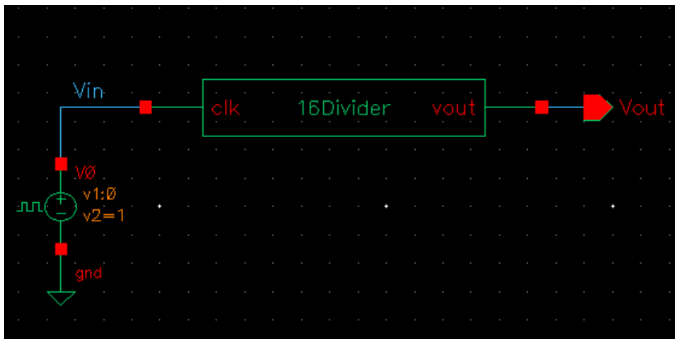

Fig. 5. N=16 frequency divider implementation

Fig. 6 shows the output after frequency division. When an input signal with a time period of 1 ns is applied, the output exhibits a time period of 16 ns, confirming a divide-by-16 operation.

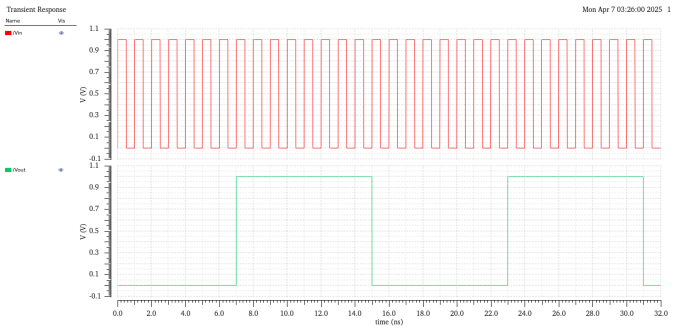

Fig. 6. Output N=16 frquency divider implementation

C. Test circuit:

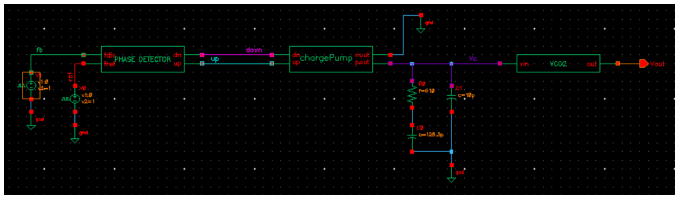

Fig. 7. Test circuit without feedback to ensure proper working of PLL blocks

Fig. 7 shows the test circuit used to verify the functionality of individual PLL blocks. In Fig. 8, the feedback input to the PFD leads the reference input, generating a `DOWN` pulse.

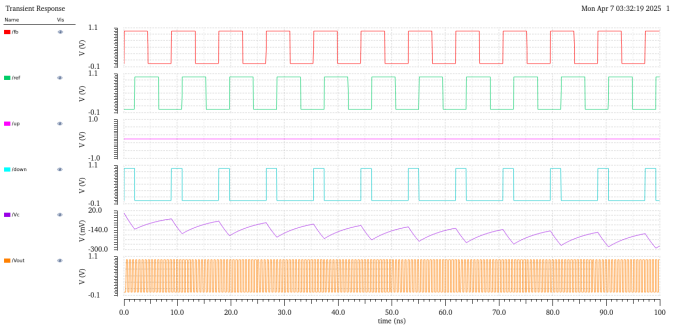

Fig. 8. Output of test circuit when feedback input leading reference input to PFD.

This pulse discharges the loop filter, resulting in a step-wise decrease in the control voltage. Conversely, when the reference input leads the feedback input, as shown in Fig. 9, UP pulses are generated, charging the loop filter and causing the control voltage to increase accordingly.

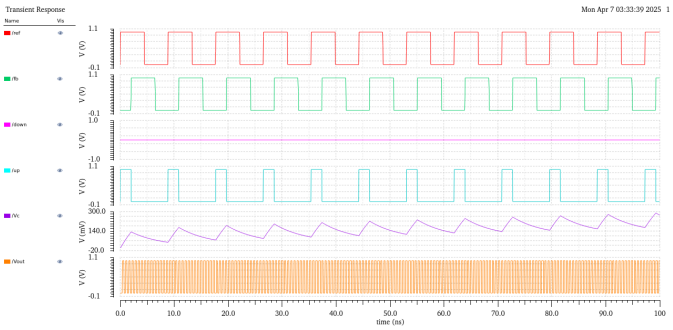

Fig. 9. Output of test circuit when reference input leading feedback input to PFD.

III. Design of Type II Order 3 PLL

When the Charge-Pump PLL (CPLL) is in near-lock condition, it can be represented in a phase-domain block diagram. The gain of the phase-frequency detector (PFD) along with the charge pump (CP) is given by:

$$LG(s) = \frac{I_{CP} K_{VCO} F(s)}{2\pi N s} \tag{1}$$

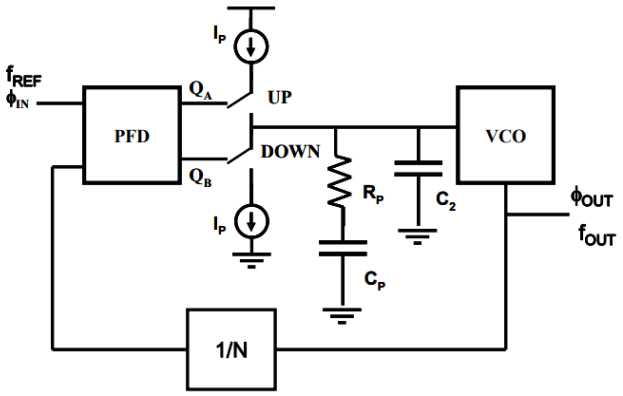

Fig. 10. Type II Third order PLL

where I_{CP} is the charge pump current, K_{VCO} is the VCO gain (rad/s/V), and N is the divider ratio. The transfer function of the loop filter can be expressed as:

$$F(s) = \frac{R_1 C_1 s + 1}{R_1 C_1 C_2 s^2 + (C_1 + C_2)s} \tag{2}$$

Fig .10 shows the the type II order 3 PLL along the loop filter. The voltage-controlled oscillator (VCO) is an ideal integrator with gain K_{VCO}. The third-order loop gain introduces a zero and three poles, where two poles are at the origin and leading to a characteristic Bode plot where phase margin degradation is evident due to two poles at the origin. In order to improve the phase margin we introduced a zero. This effect is mathematically represented as:

$$\phi_{PM} = \tan^{-1}(\omega_{UGB}/\omega_z) - \tan^{-1}(\omega_{UGB}/\omega_{p3}) \tag{3}$$

The maximum phase margin occurs at (4)

$$\omega_{UGB} = \omega_z \sqrt{\frac{C_1}{C_2} + 1}. \tag{4}$$

$$\omega_{UGB} = \frac{\omega_{p3}}{\sqrt{\frac{C_1}{C_2} + 1}} \tag{5}$$

To find the phase margin following relation can be considered

$$C_1 = 2C_2 \left(\tan^2 \Phi_M + \tan \Phi_M \sqrt{\tan^2 \Phi_M + 1}\right). \tag{6}$$

we are designing for a maximum phase margin of 60^o, so $\phi_m = 60^o$ in (7)

$$\frac{C_1}{C_2} = \left(\tan^2 60^o + \tan 60^o \sqrt{\tan^2 60^o + 1}\right).$$

$$\frac{C_1}{C_2} = 12.93 \tag{7}$$

Since the reference frequency given is 113MHz. So $w_{REF} = 71 \times 10^7 \frac{rad}{s}$. In order to provide a good balance between speed and noise rejection we can assume that $w_{UGB} = \frac{w_{REF}}{15}$. Smaller unity gain bandwidth could result in slower locking time but better noise filtering whereas larger unity gain bandwidth could result in faster response with worse noise filtering.

$$w_{UGB} = 47.33 \times 10^6 \frac{rad}{s} \tag{8}$$

From (4) and (5), we can calculate the location of pole and zero on the left hand side of the plane.

$$\omega_z = \frac{\omega_{UGB}}{\sqrt{\frac{C_1}{C_2} + 1}}$$

$$\omega_z = \frac{47.33 \times 10^6}{\sqrt{13.93}}$$

$$\omega_z = 12.682 \times 10^6 \frac{rad}{s} \tag{9}$$

$$\omega_{p3} = 47.33 \times 10^6 \times \sqrt{13.93}$$

$$\omega_{p3} = 176.65 \times 10^6 \frac{rad}{s} \tag{10}$$

(11) shows the loop gain equation. Now the magnitude of loop gain at unity gain band width is considered as 1 this is shown in (12)

$$L_3(s) = \frac{K_{\text{vco}} I_{\text{cp}}}{2\pi N} \frac{s + \frac{1}{RC_1}}{C_2 s^2 \left(s + \frac{1}{R}\frac{C_1+C_2}{C_1C_2}\right)}. \tag{11}$$

$$|L_3(j\omega)| = \frac{K_{\text{vco}} I_{\text{cp}}}{2\pi N} \cdot \frac{\sqrt{\omega^2 + \left(\frac{1}{RC_1}\right)^2}}{C_2\omega^2\sqrt{\omega^2 + \left(\frac{1}{R}\frac{C_1+C_2}{C_1C_2}\right)^2}}. \tag{12}$$

The above equation can be rewritten as follows:

$$|L_3(j\omega_{UGB})| = \frac{K_{\text{vco}} I_{\text{cp}}}{2\pi N} \cdot \frac{\sqrt{\omega_{UGB}^2 + (w_z)^2}}{C_2 \times \omega_{UGB}^2\sqrt{\omega_{UGB}^2 + (w_{p3})^2}}.$$

Substituting values from (8), (9) and (10) in (12)

$$|L_3(j\omega_{UGB})| = 1$$

$$\frac{K_{\text{vco}} I_{\text{cp}}}{2\pi N} \cdot \frac{\sqrt{\omega_{UGB}^2 + (w_z)^2}}{C_2 \times \omega_{UGB}^2\sqrt{\omega_{UGB}^2 + (w_{p3})^2}} = 1$$

$$\frac{K_{\text{vco}} I_{\text{cp}}}{C_2} = 32\pi \frac{\sqrt{(47.33)^2 + (176.65)^2}}{\sqrt{(47.33)^2 + (12.68)^2}} \times (47.33 \times 10^6)^2$$

If C_2 is taken as $10pF$, then the above equation would become

$$K_{\text{vco}} I_{\text{cp}} = 8405259.6$$

Assume $Kvco = 2 \times \pi \times 180 \times 10^6 rad/s$. Substituting this in above equation

$$I_{\text{cp}} = 7.43mA \tag{13}$$

Design Parameter	Value
Reference Frequency (f_{ref})	$113MHz$
Output Frequency (f_{out})	$1.8GHz$
Divider Ratio (N)	16
Charge Pump Current (I_{cp})	$7.43mA$
VCO Gain (K_{VCO})	180 MHz/V
phase margin (60^o)	180 MHz/V
R1	610Ω
C1	$129.3pF$
C2	$10pF$
Zero Frequency (ω_z)	$12.68Mrad/s$
Unity Gain Bandwidth (ω_{ugb})	$47.33Mrad/s$
Pole Frequency (ω_{p3})	$176.65Mrad/s$

TABLE I
TYPE-II, THIRD-ORDER PLL DESIGN PARAMETERS

IV. IMPLMENTATION AND SIMULATION RESULTS OF TYPE II THIRD ORDER PLL

Tab. I lists the design parameters used for constructing a Type-II, third-order PLL. The open-loop Bode plot provides key insights into the stability and performance of the PLL system. The gain crossover frequency (ω_{UGB}) determines the bandwidth, where a higher bandwidth results in faster locking but may increase noise sensitivity. The phase margin at ω_{ugb} indicates system stability, where a phase margin above 45° ensures a stable response with minimal overshoot, while a lower margin risks oscillations.

The location of poles and zeros affects the transient response, with the third pole in a Type-II, third-order PLL potentially reducing phase margin, requiring careful placement to balance stability and speed. Additionally, a high low-frequency gain ensures good tracking of the reference signal, which is crucial for minimizing phase error. Overall, the Bode plot helps in designing a PLL that achieves a trade-off between stability, speed, and noise performance.

The gain of the Voltage-Controlled Oscillator (VCO), K_{VCO}, should be kept relatively low to prevent noise on the control voltage line from causing significant frequency and phase deviations. As a rule of thumb, K_{VCO} should be kept below $0.1f_m$ **Hz/V,** where $f_m = \frac{f_{\text{max}}+f_{\text{min}}}{2}$, to ensure robust PLL performance.

A. Open loop Characteristics

The open loop transfer function is given in (11). Substitute the respective values in (11) from Tab I see (14)

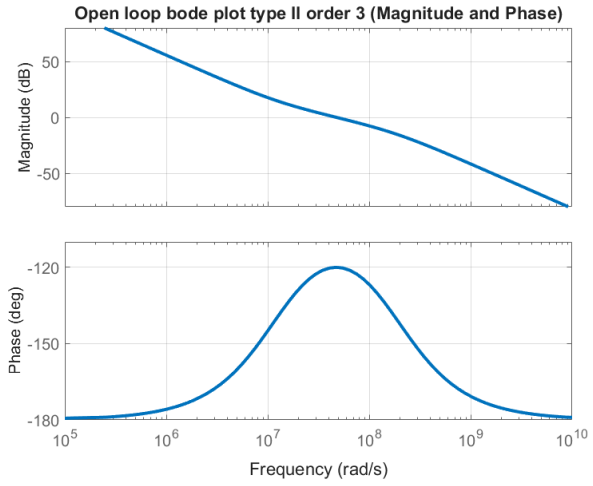

Fig. 11. Open loop Bode plot of type II third order PLL

$$L_3(s) = \frac{K_{\text{vco}} I_{\text{cp}}}{2\pi N} \frac{s + \frac{1}{RC_1}}{C_2 s^2 \left(s + \frac{1}{R}\frac{C_1+C_2}{C_1C_2}\right)}.$$

From the transfer function, it is evident that there are two poles at the origin, indicating a type-II system. This causes the magnitude plot to decrease at a rate of $-40\,\text{dB/decade}$ until it encounters a zero, which is introduced to improve the phase

margin. Along with this zero, a pole is also introduced—placed sufficiently far from the unity-gain bandwidth to minimize its effect on phase margin and stability, while still remaining within the reference frequency range.

$$L_3(s) = \frac{8.359 \times 10^{15} s + 1.06 \times 10^{23}}{s^3 + 1.766 \times 10^8 s^2} \tag{14}$$

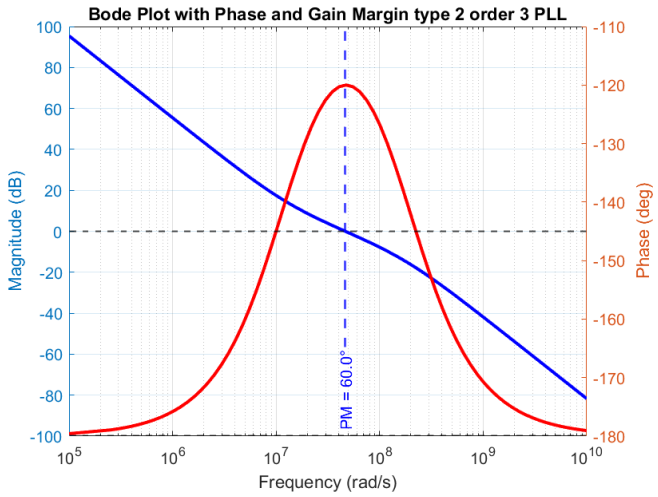

Fig. 12. Phase margin and gain margin of Type II third order PLL

Fig. 12 shows the phase margin of a Type-II, third-order PLL. From the figure, it is evident that the phase margin of the designed PLL is 60°. The gain margin is observed to be infinite, primarily due to the presence of two poles at the origin. It is seen from the open loop transfer function in (11) Fig.11 shows the open loop bode plot (magnitude and phase response) of type II third order PLL. The phase margin obtained is 60^o It ensures that the PLL designed is stable, well-damped, and exhibits minimal overshoot. It provides a good balance between stability and responsiveness while maintaining robustness to parameter variations and external disturbances.

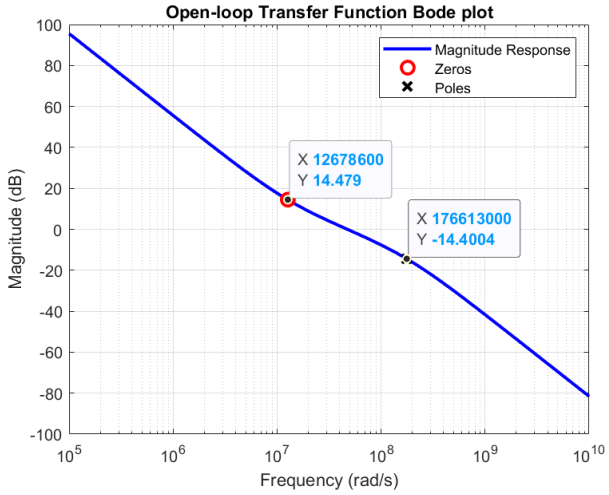

Fig. 13. Magnitude response of type II order 3 PLL showing location of non-zero pole and zero

Fig.13 shows the poles and zeros obtained from the transfer function (14). Pole is at $\frac{C_1+C_2}{R_1 \times C_1 \times C_2}$. Both zero and pole are on the left hand side of the plane. $w_{p3} = 176.65 Mrad/s$, $w_z = 12.68 Mrad/s$.

B. Closed loop Characteristics

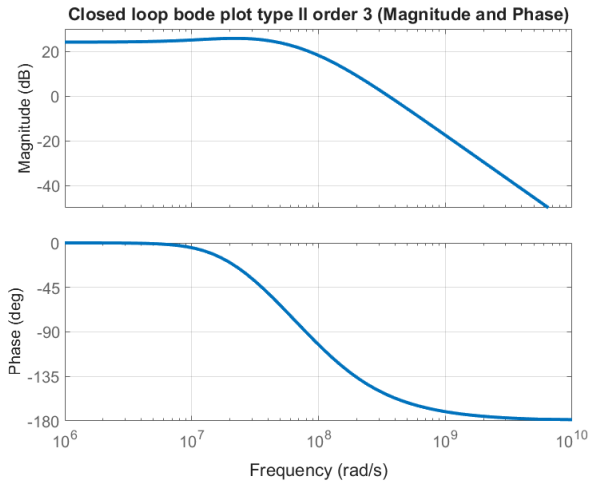

Fig. 14. Closed loop Bode plot of type II third order PLL

The closed-loop transfer function is given in (16) and is obtained by

$$\frac{\theta_o(s)}{\theta_i(s)} = \frac{L_3(s)}{1 + L_3(s)} \tag{15}$$

$$T_{cl3}(s) = \frac{K_{\text{VCO}} I_{\text{cp}}}{2\pi N C_2} \cdot \frac{s + \frac{1}{RC_1}}{s^3 + \left(\frac{1}{R}\frac{C_1+C_2}{C_1 C_2}\right) s^2 + \frac{K_{\text{VCO}} I_{\text{cp}}}{2\pi C_2} s + \frac{K_{\text{VCO}} I_{\text{cp}}}{2\pi R C_2 C_1}}. \tag{16}$$

After substituting the respective values from Tab. I, the closed-loop transfer function is as follows:

$$T_{cl3}(s) = \frac{1.337 \times 10^{17} s + 1.696 \times 10^{24}}{s^3 + 1.766 \times 10^8 s^2 + 8.359 \times 10^{15} s + 1.06 \times 10^{23}} \tag{17}$$

From the closed loop response we can analyse the stability, bandwidth, settling time of the PLL. **Bandwidth (BW)** is the frequency range over which a system effectively operates. In control systems and PLLs, it is typically defined as the frequency at which the closed-loop magnitude response falls to -3 dB of its low-frequency value.

$$|T_{\text{cl}}(j\omega_{\text{BW}})| = \frac{|T_{\text{cl}}(0)|}{\sqrt{2}}. \tag{18}$$

A higher bandwidth indicates a faster response but may lead to increased noise sensitivity, while a lower bandwidth provides better noise filtering but results in a slower response. The maximum amplitude of the closed loop response is N here N=16. so w_{-3db} is obtained at $|H_{\text{cl}}(j\omega_{\text{BW}})| = \frac{16}{\sqrt{2}}$ and the bandwidth obtained is almost 7.4×10^7 rad/s from the simulation results.

From the closed-loop transfer function given by (17), we can estimate the **settling time** of the PLL in response to a step.

Let us approximate the closed-loop behavior by a one-pole response having the same -3 dB bandwidth. Bandwidth must be chosen to be less than $\omega_{\text{in}}/10$. Thus, the closed-loop time constant, τ, is at least equal to $10/\omega_{\text{in}} = 10T_{\text{in}}/(2\pi)$. Allowing four or five time constants for settling, we estimate a settling time on the order of $6T_{\text{in}}$ to $8T_{\text{in}}$. In practice, however, the choice $\omega_{-3dB} \approx \omega_{\text{in}}/10$ leads to excessive ripple in V_{cont}; for the PLL output sidebands to be acceptably small, the bandwidth is less, and the settling time reaches about $100T_{\text{in}}$.

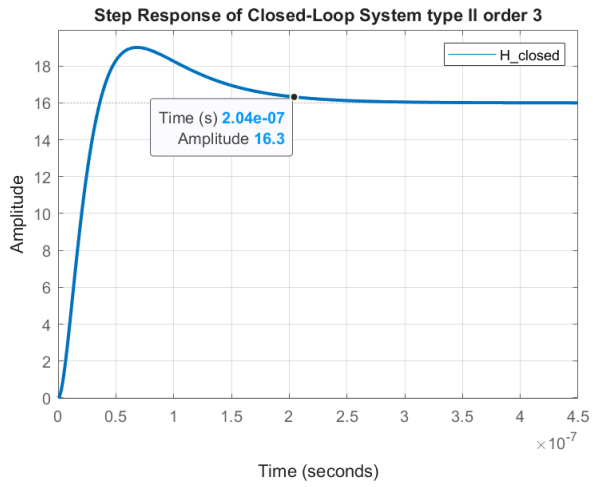

Fig. 15. Step response of type II third order PLL

Fig.15 shows the step response of type II third order PLL. The settling time is $204ns$.

$$T_{in} = \frac{2\pi}{71 \times 10^7} = 8.85ns \tag{19}$$

So obtained settling time is almost $23T_{in}$ which is acceptable.

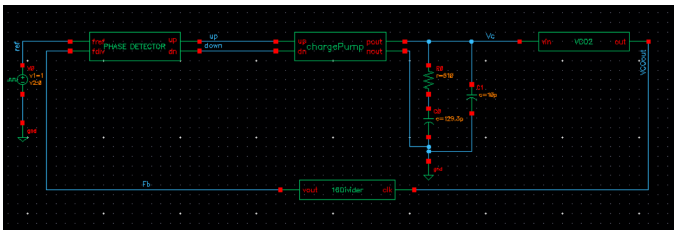

Fig. 16. Circuit diagram for simulating type II third order PLL

Fig. 16 shows the circuit diagram used to simulate a Type II, third-order PLL. Fig. 17 illustrates the corresponding timing analysis. The VCO gain is chosen as 180 MHz/V. The control voltage and output frequency initially oscillate and eventually settle after a certain period.

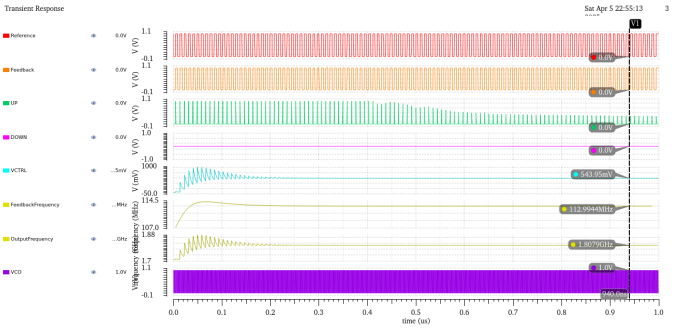

Fig. 17. Timing analysis of type II third order PLL

In this case, the control voltage stabilizes around 0.5 V, while the output frequency settles at approximately 1.8 GHz, which is the desired value. The VCO output is passed through a frequency divider with division factor $N = 16$, and the resulting feedback frequency—used as the input to the phase detector—is also shown in Fig. 17.

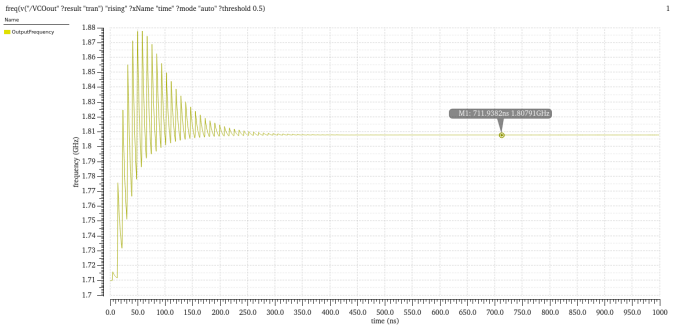

Fig. 18. Settling of Output Frequency of type II third order PLL

Fig. 18 illustrates the variation of the VCO output frequency over time. From the plot, it is observed that the PLL settles around 210 ns, which closely matches the earlier step response analysis.

The output frequency of a VCO is linearly dependent on the control voltage and is expressed as:

$$f_{\text{out}}(t) = f_{\text{center}} + K_{\text{VCO}}\left(V_{\text{ctrl}}(t) - V_{\text{center}}\right) \tag{20}$$

where $f_{\text{out}}(t)$ is the instantaneous output frequency, f_{center} is the center frequency, K_{VCO} is the VCO gain in Hz/V, $V_{\text{ctrl}}(t)$ is the control voltage, and V_{center} is the control voltage corresponding to the center frequency.

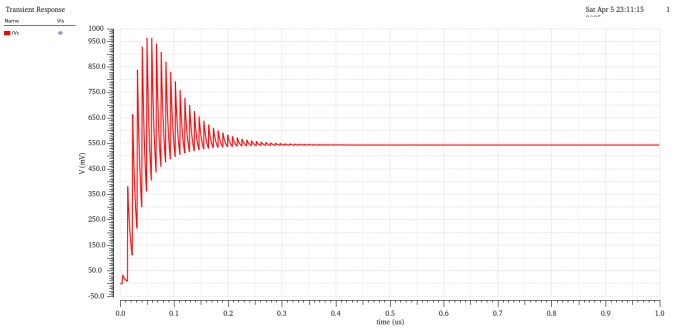

Fig. 19. Settling of control voltage of type II third order PLL

Alternatively, in terms of angular frequency:

$$\omega_{\text{out}}(t) = \omega_{\text{center}} + K_{\text{VCO}}^{\omega}\left(V_{\text{ctrl}}(t) - V_{\text{center}}\right) \tag{21}$$

where $K_{\text{VCO}}^{\omega} = 2\pi K_{\text{VCO}}$ and $\omega_{\text{center}} = 2\pi f_{\text{center}}$. In our analysis, the center control voltage was chosen as $0.5\,\text{V}$, and the free-running frequency was approximately $1.8\,\text{GHz}$. Fig. 19 shows the settling of control voltage with time. The control voltage settles around 550mV.

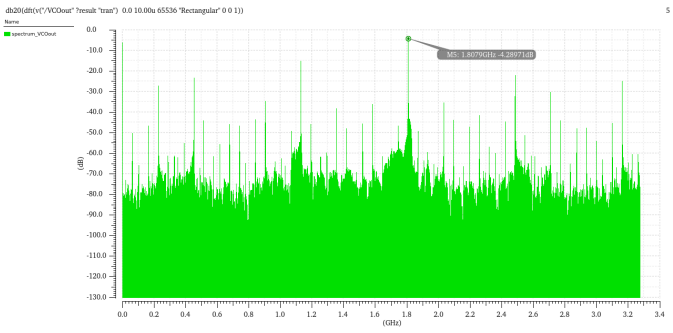

Fig. 20. Output spectrum of type II third order PLL

Fig. 20 shows the output spectrum of type II order 3 PLL. The output spectrum represents the frequency content of the signal. It displays how the signal power or amplitude is distributed across different frequencies. For an ideal sinusoidal output from a VCO or PLL, the output spectrum exhibits a sharp peak at the carrier frequency, indicating a dominant frequency component. Additional peaks or harmonics may be observed due to non-linearities, while spurious tones indicate imperfections in the system. Analyzing the output spectrum helps in identifying unwanted frequency components and assessing the spectral purity of the generated signal. In order to imitate real world cases in the analysis jitter noise is also introduced. Fig. 20 shows that the frequency component with the maximum amplitude is $1.8\,\text{GHz}$, indicating the validity of both the design and the analysis.

Fig. 21 shows that the dominant frequency component is at $1.8\,\text{GHz}$, which confirms the correct operation of the PLL. Although the y-axis represents magnitude rather than power density, the plot still provides valuable insight. The sharp peak indicates that the loop effectively suppresses out-of-band noise, which is consistent with the expected behavior of a Type-II third-order PLL. This reflects good phase noise performance and low jitter in the locked state.

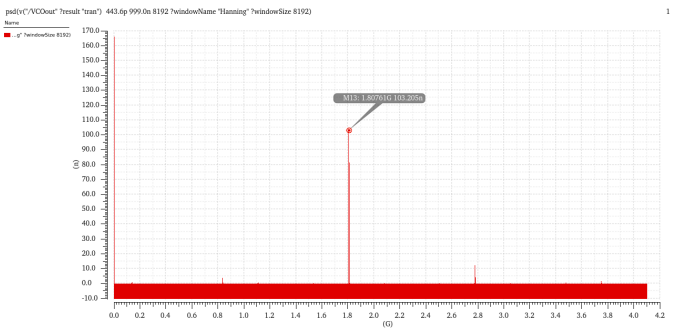

Fig. 21. Power Spectral Density of type II third order PLL

V. Design of Type II Order 4 PLL

A stable third-order PLL is often sufficient for many applications, but a fourth-order design may be necessary when higher performance is required. For instance, a fourth-order PLL can provide improved suppression of high-frequency noise and *reference spurs*, making it suitable for *low-jitter* or *fractional-N* applications. The additional pole allows for a *sharper roll-off*, leading to better *out-of-band noise* rejection and improved *EMI* performance. Furthermore, it offers more flexibility in achieving a wider *loop bandwidth* while maintaining a desirable *phase margin*. However, this comes at the cost of increased *complexity*, both in analysis and implementation, and a greater risk of compromising *stability margins*. Therefore, unless specific performance needs dictate otherwise, a third-order PLL is often preferred due to its simpler design and robust operation. Fig .22 shows the passive loop filter used in type II fourth order PLL.

The average current to voltage transfer function of the loop filter is given in (22)

$$F(s) = \frac{D(s + 1/\tau_1)}{\tau_2\tau_3 s^3 + \left[\tau_2 + \left(\frac{D}{R_2} + 1\right)\tau_3\right] s^2 + \left(\frac{D\tau_3}{\tau_1 R_2} + 1\right) s} \tag{22}$$

where

$$D = \frac{R_1 C_1}{C_1 + C_2}, \quad \tau_1 = R_1 C_1, \quad \tau_2 = \frac{R_1 C_1 C_2}{C_1 + C_2}, \quad \tau_3 = R_2 C_3.$$

The open loop transfer function can be written as

$$L_4(s) = \frac{K_{\text{vco}} I_{\text{cp}} F(s)}{2\pi N s} \tag{23}$$

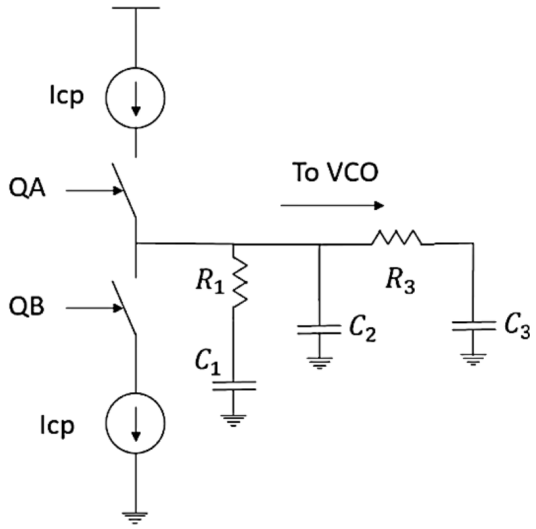

Fig. 22. Passive loop filter for type II fourth order PLL.

While analyzing the denominator (24) of $L_4(s)$, we know that two poles are located at the origin. To determine the remaining two poles, we assume that the fourth pole is placed at a frequency 3.5 times that of the third pole. This ensures that it also lies within the reference frequency range, which is

71×10^9 rad/s.

$$s^2\left(\frac{\tau_1\tau_3C_2}{C_1+C_2+C_3}\right)+s\left(\frac{\tau_1(C_2+C_3)+\tau_3(C_1+C_2)}{C_1+C_2+C_3}\right)=-1 \quad (24)$$

The above equation can be compared with (25)

$$s^2\left(\frac{1}{w_{p3}w_{p4}}\right)+s\left(\frac{1}{w_{p3}}+\frac{1}{w_{p4}}\right)=-1 \quad (25)$$

From (24) and (25), we can deduce the following relations

$$\frac{1}{w_{p3}w_{p4}}=\frac{R_1C_1R_3C_3C_2}{C_1+C_2+C_3} \quad (26)$$

$$\frac{1}{w_{p3}}+\frac{1}{w_{p4}}=\frac{R_1C_1(C_2+C_3)+R_3C_3(C_1+C_2)}{C_1+C_2+C_3} \quad (27)$$

Certain assumptions are now made: let $C_1 = 100\,\text{pF}$, $C_2 = 10\,\text{pF}$, $C_3 = 0.1\,\text{pF}$, and $\omega_{p4} = 3.5\,\omega_{p3}$. Based on insights from the design of the third-order PLL, we assume $\omega_{p3} = 176.65\,\text{Mrad/s}$, leading to $\omega_{p4} = 618.275\,\text{Mrad/s}$. Rearranging equations (26) and (27) and substituting the assumed values yields:

$$\frac{1}{\tau_3}\left(1+\frac{C_3}{C_2}\right)+\frac{1}{\tau_1}\left(1+\frac{C_1}{C_2}\right)=7.95\times10^8$$

$$\frac{1}{\tau_3}(1)+\frac{1}{\tau_1}(11)=7.95\times10^8$$

$$\frac{1}{\tau_1\tau_3}=9.93\times10^{15}$$

From the relations given above, we obtain: $\tau_1 = 6.23 \times 10^{-8}$ s and $\tau_3 = 1.616 \times 10^{-9}$ s. $R_1 = 623\Omega$, $R_3 = 16.16k\Omega.w_{UGB} = 47.33Mrad/s$

$$PM=\tan^{-1}(\tau_1\omega_c)-\tan^{-1}\left(\frac{A(\tau_1\omega_c)}{1-B(\tau_1\omega_c)^2}\right) \quad (28)$$

$$A=\frac{\frac{C_2}{C_1}+\frac{C_3}{C_1}+\frac{\tau_2}{\tau}\left(1+\frac{C_2}{C_1}\right)}{1+\frac{C_2}{C_1}+\frac{C_3}{C_1}} \quad (29)$$

$$B=\frac{\frac{C_2\,\tau_2}{C_1\,\tau}}{1+\frac{C_2}{C_1}+\frac{C_3}{C_1}} \quad (30)$$

After substituting the respective values into equations (29) and (30), we obtain $A = 0.11765$ and $B = 2.356 \times 10^{-3}$. Now phase margin from (28)

$$PM=\tan^{-1}(2.95)-\tan^{-1}(0.354)=51.78^\circ$$

From (31) we can calculate the value for w_{UGB}. Substitute respective values in (31):

$$\frac{1}{\tau_1}\sqrt{\frac{1}{2}\times15.9}=w_{UGB}$$

$$w_{UGB}=45.26Mrad/s$$

In order to find the charge pump current, let us consider (32). Substituting the respective values into the equation yields the result. $K_{vco} = 2\pi \times 180Mrad/V/s$

$$I_{cp}\cdot K_{vco}=8273441.29$$

$$I_{cp}=\frac{8273441.29}{2\pi\times180\times10^6}$$

$$I_{cp}=7.3mA$$

Since $K_{VCO}=\frac{f_{\max}-f_{\min}}{V_2-V_1}$, narrowing the control voltage range increases K_{VCO}, which is undesirable. In both the cases for third order as well as fourth order we have assumed very small value for K_{VCO}. i.e, $0.1 \times 1.8GHz = 180MHz$

Design Parameter	Value
C_1	$100pF$
C_2	$10pF$
C_3	$0.1pF$
R_1	623Ω
R_3	$16.16k\Omega$
τ_1	6.23×10^{-8} s
τ_3	1.616×10^{-9} s
I_p	$7.3mA$
K_{VCO}	$2\pi \times 180Mrad/V/s$
N	16
A	0.11765
B	2.356×10^{-3}
ω_{UGB}	$45.26Mrad/s$
PM	51.78°
ω_z	$16.05Mrad/s$
ω_{p3}	$176.65Mrad/s$
ω_{p4}	$618.275Mrad/s$

TABLE II
TYPE-II, FOURTH-ORDER PLL DESIGN PARAMETERS

VI. IMPLMENTATION AND SIMULATION RESULTS OF TYPE II FOURTH ORDER PLL

Tab II shows the values of all the design parameters needed for implementing a type II order 4 PLL. Analysis on the open loop response and closed loop response is discussed in this section. In the open-loop response, the system exhibits a steeper phase drop, making phase margin a critical factor — typically targeted around 45–60° for stability. In the closed-loop transfer function, the higher order allows better tracking and noise rejection, but excessive peaking near the unity gain bandwidth (UGB) can occur if the phase margin is insufficient.

A. Open loop Characteristics

Fig.23 shows the open loop bode plot of type II fourth order PLL with both magnitude response and phase response. The open loop transfer function is given in (23). Substituting values from Tab II in (23) we obtain the transfer function in (33)

$$\omega_c = \frac{1}{\tau}\sqrt{\frac{1}{2}\left(\frac{2B+AB+A-A^2}{B(B-A)} + \sqrt{\left(\frac{2B+AB+A-A^2}{B(B-A)}\right)^2 - \frac{4(1-A)}{B(B-A)}}\right)} \tag{31}$$

$$\frac{I_p K_{VCO}}{2\pi N}\sqrt{\frac{1+(\tau\omega_c)^2}{(A\tau\omega_c)^2+(1-B(\tau\omega_c)^2)^2}} = C_1\left(1+\frac{C_2}{C_1}+\frac{C_3}{C_1}\right)\omega_c^2 \tag{32}$$

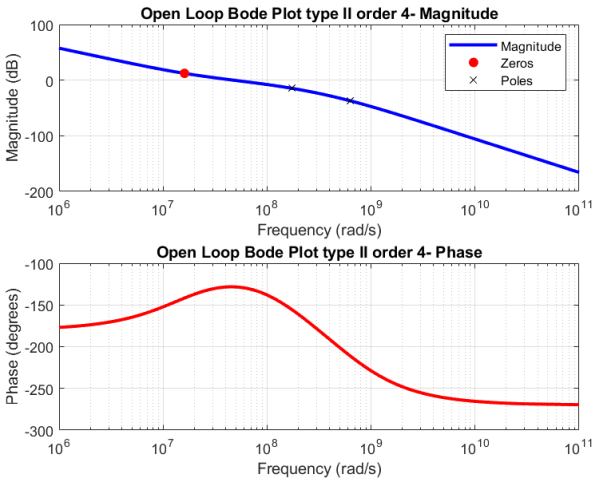

Fig. 23. Open loop Bode plot of type II fourth order PLL

$$L_4(s) = \frac{0.005116\,s + 82125}{1.007\cdot 10^{-27}s^4 + 8.07\cdot 10^{-19}s^3 + 1.101\cdot 10^{-10}s^2} \tag{33}$$

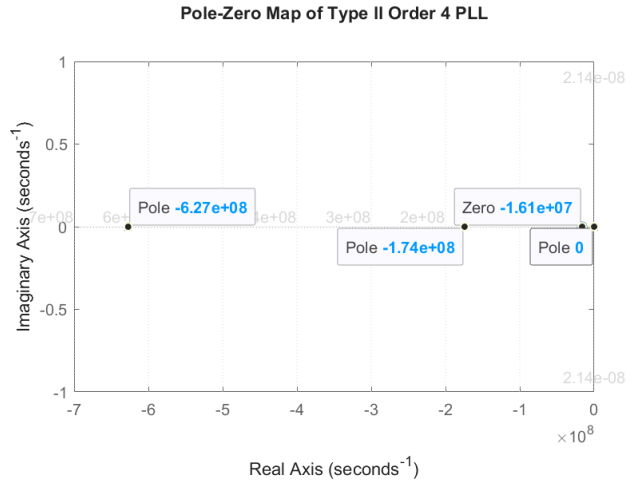

Fig. 24. Pole Zero map to show the location of poles and zeros

The open-loop transfer function in (33) indicates the presence of four poles, two of which are located at the origin. This confirms that the system is a fourth-order, type-II/Fig.24 shows the location of poles and zeros in the pz plane. $w_{p1}, w_{p2} = 0s^{-1}$, $w_{p3} = -1.74\times10^8 s^{-1}$, $w_{p4} = -6.27\times10^8 s^{-1}$, $w_z = -1.61\times10^7 s^{-1}$. The values almost matches with the design assumptions we have taken.

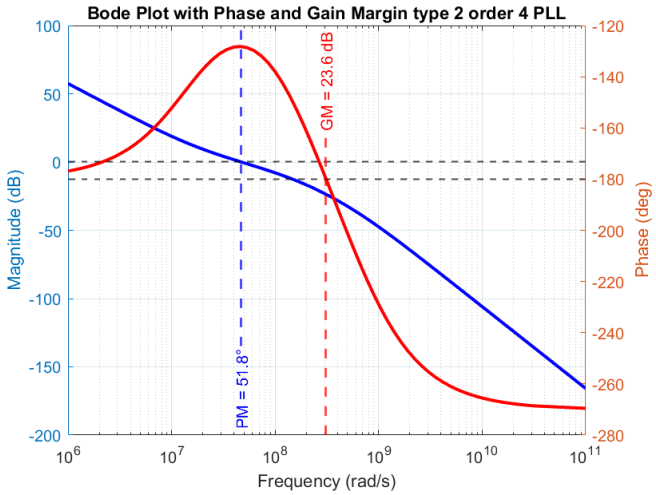

Fig. 25. Phase margin and gain margin for type II order 4 PLL

Phase Margin and *Gain Margin* are essential metrics for evaluating the stability of a control system. The **Phase Margin (PM)** is defined as the additional phase lag required to bring the system to the verge of instability, specifically when the open-loop gain is unity (0 dB), at the *gain crossover frequency*. Conversely, the **Gain Margin (GM)** refers to the amount by which the system gain can be increased before it becomes unstable, evaluated at the *phase crossover frequency*, where the phase shift is $-180°$. Systems with higher phase and gain margins are generally more stable and robust, with typical design criteria aiming for a phase margin greater than $45°$ and a gain margin greater than 6 dB. The phase margin obtained is $51.8°$ and gain margin is around 23.6dB. We designed for a maximum phase margin of $51.78°$. The 4th pole(w_{p3}) provides additional roll-off (–20 dB/decade per pole). This helps suppress VCO phase noise and other high-frequency disturbances more effectively than a 3rd-order system.

B. Closed loop Characteristics

The closed-loop transfer function is expressed in (34) and (33), where $L_4(s)$ is defined in (23). Substituting the values from Table II, the resulting closed-loop transfer function for a Type-II fourth-order PLL is shown in (35).

$$T_{cl4}(s) = \frac{N \cdot L_4(s)}{1 + L_4(s)} \tag{34}$$

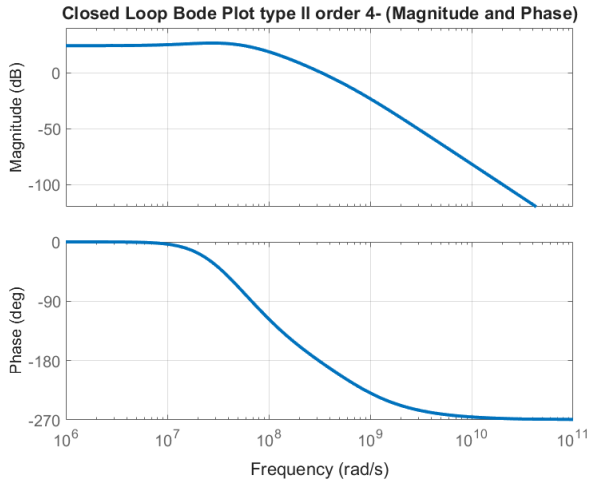

Fig. 26. Closed loop bode plot for type II order 4 PLL

From the closed-loop response, we can analyze the bandwidth and settling time, similar to the analysis performed for the Type-II third-order PLL in a previous section. The maximum amplitude of the closed loop response is 20log(N) in dB. i.e, $20log(16) = 24.08dB$. The bandwidth obtained is $8.1 \times 10^7 rad/s$. As given in (19) $T_{in} = 8.85ns$ is for the desired PLL. Settling time for the step response given to a type II order 4 PLL is shown in Fig.27. The settling time is 164ns. The settling time for order 4 has decreased slightly compared to order 3 this is because w_{UGB} and bandwidth of order 4 is increased slightly.

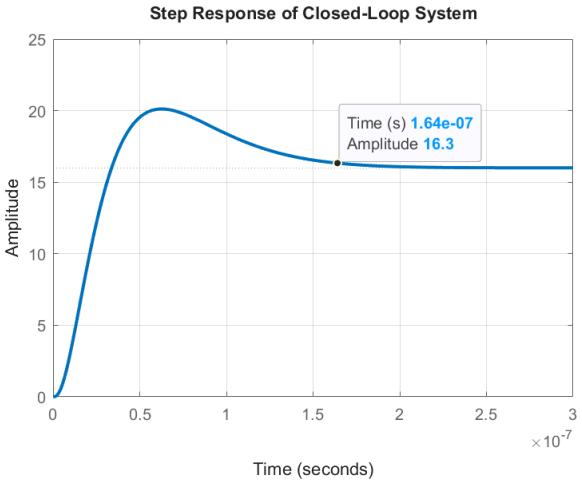

Fig. 27. Step response of type II order 4 PLL

Fig. 28 illustrates the circuit diagram used for timing analysis of a Type-II, fourth-order PLL.

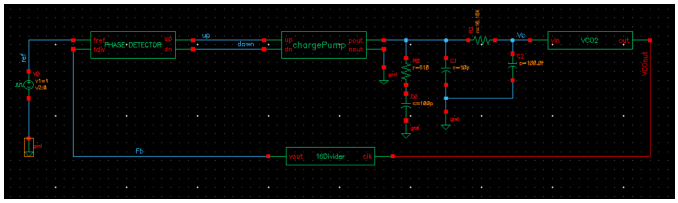

Fig. 28. Circuit diagram for timing analysis of type II order 4 PLL

An additional pole has been introduced in the loop filter to improve high-frequency noise suppression near the reference frequency. This fourth pole is strategically placed at approximately 3.5 times the location of the third pole, ensuring that it lies within the reference frequency range but remains beyond the unity gain bandwidth (UGBW) of the system. Positioning the pole outside the UGBW helps prevent it from degrading phase margin or destabilizing the loop, while still contributing to enhanced attenuation of high-frequency disturbances. This careful placement supports both stable operation and improved spectral purity of the PLL output.

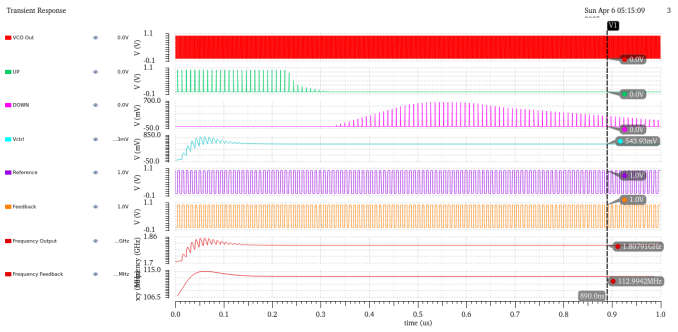

Fig. 29. Timing analysis of type II order 4 PLL

Fig. 29 illustrates the timing analysis of type II fourth order PLL in which improvement of control voltage, output frequency, VCO output, feedback frequency is observed.

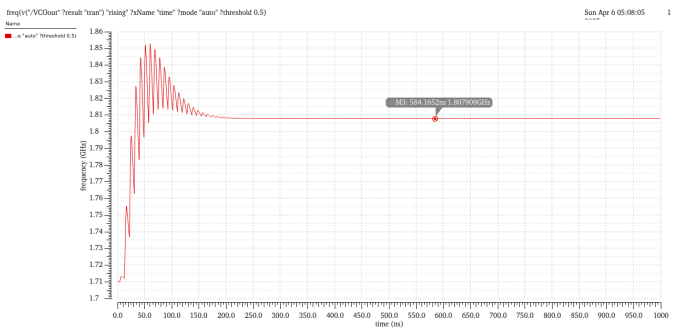

Fig. 30. Settling of VCO output frequency of type II order 4 PLL

Fig. 30 shows the variation of output frequency with respect to time. It is observed that the output frequency settles around 1.8 GHz, which is the desired frequency for the VCO output.

$$T_{cl4} = \frac{0.08186s + 1.314 \times 10^6}{1.007 \times 10^{-27}s^4 + 8.07 \times 10^{-19}s^3 + 1.101 \times 10^{-10}s^2 + 0.005116s + 82125} \tag{35}$$

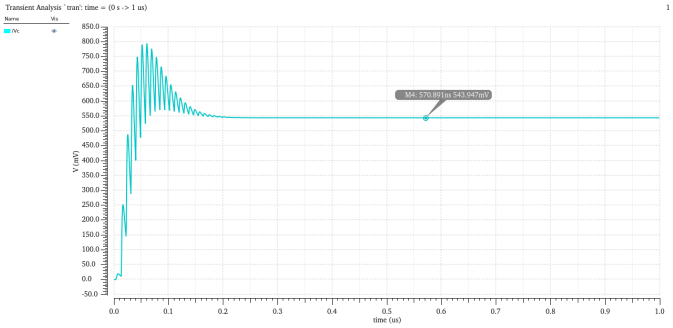

Fig. 31. Settling of control voltage of type II order 4 PLL

Fig. 31 shows the the variation of control voltage to vco input with respect to time. It is observed that control voltage settles around 0.5V.

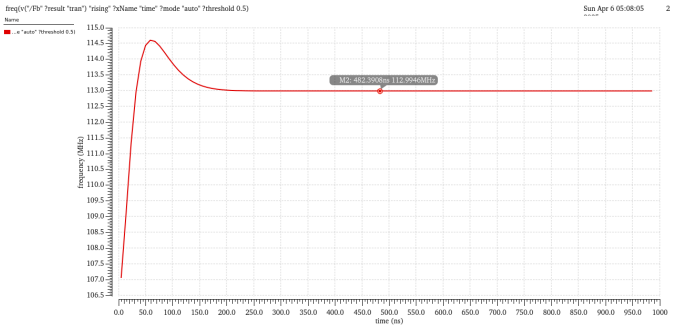

Fig. 32. Settling of feedback frequency of type II order 4 PLL

Fig. 32 illustrates the variation of the feedback frequency applied to the phase-frequency detector input over time. It is observed that the frequency stabilizes close to the reference frequency, which is approximately 113 MHz.

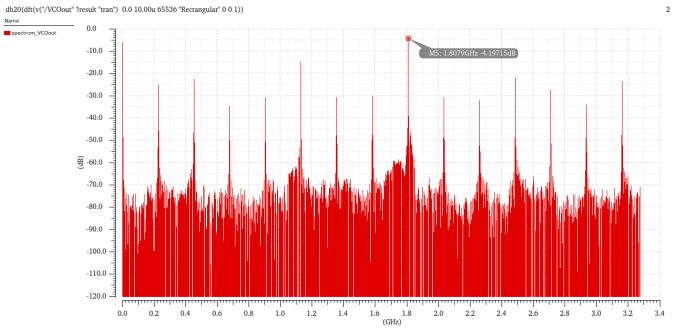

Fig. 33. Output spectrum of type II order 4 PLL

Fig. 33 presents the output spectrum of the Type-II, fourth-order PLL. The dominant frequency component corresponds to the desired output frequency of 1.8 GHz, indicating successful frequency locking. This observation is further supported by Fig. 34, which shows the power spectral density. For clarity, the PSD is plotted with the y-axis in magnitude rather than in dB.

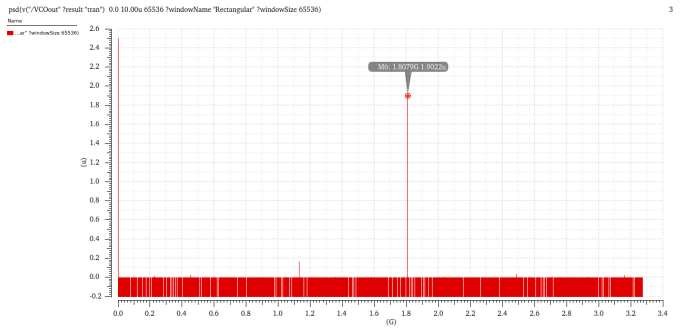

Fig. 34. Power spectral density of type II order 4 PLL

VII. Noise Transfer Functions Type II Order 3 PLL

The noise transfer function (NTF) in a Phase-Locked Loop (PLL) describes how noise introduced at different points in the loop is transferred to the output. This analysis is crucial for evaluating the PLL's noise performance and stability.

A. Reference Noise Transfer Function:

$$NTF_{ref}(s) = \frac{\Phi_{\text{out}}(s)}{\Phi_{\text{ref}}(s)}$$

$$NTF_{ref}(s) = N \times \frac{L(s)}{1 + L(s)} \tag{36}$$

where L(s) is given in (11). Substituting all the required values from Tab I see (37) This function represents the transfer of the input reference phase to the output. At low frequencies, $T(s) \approx N$, indicating accurate tracking of the reference. At high frequencies, $T(s) \approx L(s)$, showing suppression of high-frequency components from the reference. as $L(s) \approx 0$ at high frequency.

B. Divider Noise Transfer Function:

$$NTF_{div}(s) = -N \times \frac{L(s)}{1 + L(s)} \tag{38}$$

The negative sign in (38) indicates that the divider noise is introduced through the feedback path. While this sign is relevant in phase shift analysis, it is typically disregarded in power spectral density analysis, where only the magnitude of the transfer function is considered for clearer interpretation. So the noise transfer function for divider is as follows in (39)

C. Loop Filter Noise Transfer Function:

$$NTF_{div}(s) = \frac{K_{vco}}{s(1 + L(s))} \tag{40}$$

The noise transfer function for the filter is as in (41). This explains how teh phase noise originated from the filter

$$NTF_{ref}(s) = \frac{10.6\,s + 1.345 \times 10^8}{7.929 \times 10^{-17}s^3 + 1.4 \times 10^{-8}s^2 + 0.6628\,s + 8.403 \times 10^6} \tag{37}$$

$$NTF_{div}(s) = \frac{10.6\,s + 1.345 \times 10^8}{7.929 \times 10^{-17}s^3 + 1.4 \times 10^{-8}s^2 + 0.6628\,s + 8.403 \times 10^6} \tag{39}$$

$$NTF_{lpf}(s) = \frac{8.968 \times 10^{-8}s^3 + 15.84s^2}{7.929 \times 10^{-17}s^4 + 1.4 \times 10^{-8}s^3 + 0.6628s^2 + 8.403 \times 10^6 s} \tag{41}$$

appears at the output.

D. VCO Noise Transfer Function:

$$N(s) = \frac{\Phi_{\text{out}}(s)}{\Phi_{\text{vco}}(s)} \tag{42}$$

$$NTF_{vco}(s) = \frac{1}{1 + L(s)} \tag{43}$$

This describes how phase noise originating from the voltage-controlled oscillator (VCO) appears at the output. Low-frequency components of VCO noise are suppressed ($N(s) \approx 0$), while high-frequency components dominate the output ($N(s) \approx N$). (44) shows the noise transfer function of VCO.

The loop bandwidth serves as the crossover point between reference noise and VCO noise dominance Within the loop bandwidth, the output is primarily influenced by the reference. Beyond the loop bandwidth, the output is dominated by VCO phase noise.
Therefore, the PLL acts as a low-pass filter for the reference signal and as a high-pass filter for VCO noise. Proper filter design ensures that the loop suppresses undesirable noise and maintains phase stability. From the transfer functions in (37), (39), (41), and (44), we observe the following characteristics: the reference and divider noise transfer functions exhibit low-pass behavior, the loop filter noise transfer function behaves like a band-pass filter, and the VCO noise transfer function exhibits high-pass characteristics. This conclusion can be observed from Fig. 35

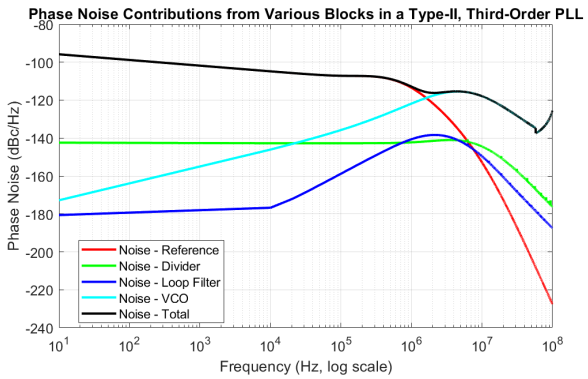

Fig. 35. Phase noise contribution by each sources of type II order 3 PLL.

Noise Projection to PLL Output

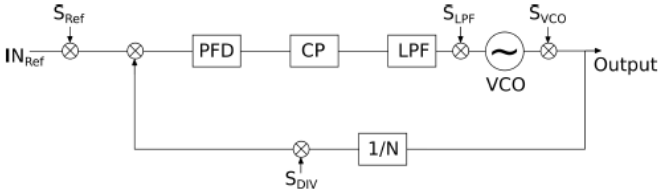

Fig. 36. Block diagram of PLL with noise sources.

Fig. 36 shows the block diagram of PLL with noise sources. The output phase noise of a Phase-Locked Loop (PLL), denoted as $S_{\text{out}}(f)$, is influenced by various internal noise sources such as the reference clock, divider, loop filter, and the VCO. Each noise source has an associated noise transfer function (NTF), which determines how that noise is shaped and propagated to the output. The contribution of any noise source $S_{\text{src}}(f)$ to the output can be expressed as:

$$S_{\text{out,src}}(f) = |NTF_{\text{src}}(j2\pi f)|^2 \cdot S_{\text{src}}(f) \tag{45}$$

Here, $S_{\text{src}}(f)$ is the power spectral density (PSD) of the noise source in linear scale (W/Hz), and $NTF_{\text{src}}(j2\pi f)$ is the magnitude response of the corresponding noise transfer function evaluated at frequency f.
Given noise sources are provided in dBc/Hz, so the transformation follows:

- Convert noise PSD from dBc/Hz to linear scale using:

$$S_{\text{src,lin}}(f) = 10^{S_{\text{src,dBc}}(f)/10} \tag{46}$$

- Compute the squared magnitude of the transfer function:

$$|NTF_{\text{src}}(j2\pi f)|^2 \tag{47}$$

- Multiply to obtain the output noise in linear scale:

$$S_{\text{out,src}}(f) = S_{\text{src,lin}}(f) \cdot |NTF_{\text{src}}(j2\pi f)|^2 \tag{48}$$

- Convert the result back to dBc/Hz for interpretation:

$$S_{\text{out,src,dBc}}(f) = 10\log_{10}(S_{\text{out,src}}(f)) \tag{49}$$

From the block diagram shown in Fig. 36, the intermediate expression in (50) is derived, leading to the final form of the output phase noise $S_{\text{out}}(f)$ as given in (51). The total output

$$NTF_{vco}(s) = \frac{7.929 \times 10^{-17}s^3 + 1.4 \times 10^{-8}s^2}{7.929 \times 10^{-17}s^3 + 1.4 \times 10^{-8}s^2 + 0.6628s + 8.403 \times 10^6} \tag{44}$$

$$S_{\text{out}}(s) = S_{\text{vco}}(s) + \frac{K_{\text{VCO}}}{s}\left[F(s)\big(S_{\text{ref}}(s) - S_{\text{div}}(s) - \frac{1}{N}\cdot S_{\text{out}}(s)\big)K_{\text{PD}} + S_{\text{lpf}}(s)\right] \tag{50}$$

$$S_{\text{out}}(s) = \frac{S_{\text{vco}}(s) + \frac{K_{\text{VCO}}}{s}\left[F(s)K_{\text{PD}}\left(S_{\text{ref}}(s) - S_{\text{div}}(s)\right) + S_{\text{lpf}}(s)\right]}{1 + \frac{K_{\text{VCO}}}{s}\cdot\frac{F(s)K_{\text{PD}}}{N}} \tag{51}$$

$$S_{\text{out}}(f) = |NTF_{\text{ref}}(f)|^2 S_{\text{ref}}(f) + |NTF_{\text{div}}(f)|^2 S_{\text{div}}(f) + |NTF_{\text{lpf}}(f)|^2 S_{\text{lpf}}(f) + |NTF_{\text{vco}}(f)|^2 S_{\text{vco}}(f) \tag{52}$$

phase noise plotted in Fig. 35 is computed using the equation (52)

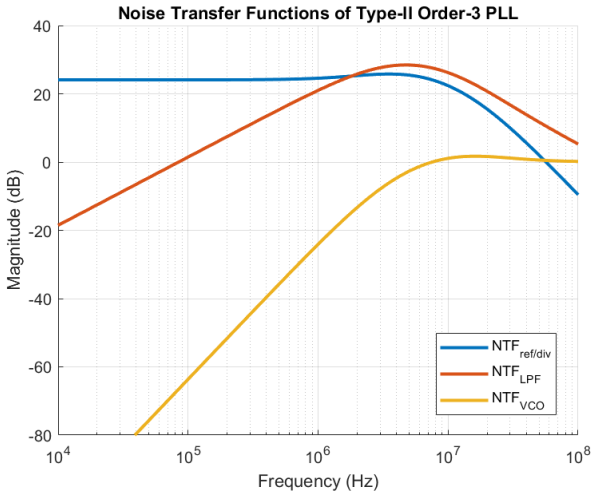

Fig. 37. Noise transfer functions of type II order 3 PLL.

Stability, Bandwidth and Noise Attenuation

While noise transfer functions do not directly indicate the stability of a PLL, they provide valuable insight into the loop's behavior. From the plots in Fig. 36, the third-order Type-II PLL exhibits typical characteristics: reference noise dominates below 10 MHz but is effectively attenuated beyond this point, demonstrating a low-pass behavior. Divider noise is minimal and suppressed beyond the bandwidth, while loop filter noise shows a mild band-pass profile. VCO noise becomes prominent beyond 10 MHz, indicating limited suppression in the far-out region due to the loop's inability to track rapid phase variations, though attenuation is still evident. The total output noise shows strong attenuation at low and high frequencies, with a minor bump around 10 MHz, which is typical of a Type-II, third-order system. This small peaking suggests a reasonable phase margin, and the overall response confirms loop stability. Furthermore, the characteristic equations (37), (39), (41), and (44) reveal that all closed-loop poles lie in the left half-plane, affirming the system's stability. Estimated bandwidth from simulation results is $11.767629.88MHz$

VIII. Conclusion

The design and implementation of Type-II, Order-3 and Order-4 PLLs were successfully carried out with detailed analysis of stability, noise behavior, and bandwidth. Both architectures employed passive RC loop filters, with proper selection of charge pump current and K_{VCO} to meet performance targets. MATLAB modeling enabled derivation of closed-loop and noise transfer functions, and pole analysis confirmed all roots lie in the left half-plane, ensuring stability. For the Order-3 PLL, reference noise dominated below 10 MHz and was effectively attenuated beyond, while VCO noise became dominant at higher frequencies, consistent with expected low-pass and high-pass filtering trends. The Order-4 PLL introduced an additional pole-zero pair, enhancing bandwidth control and noise shaping. The K_{VCO} was kept below 200 MHz/V for a 2 GHz center frequency by maximizing the control voltage swing, reducing sensitivity to noise. Divider implementation and PFD behavior were validated through open-loop simulations. Overall, the PLLs exhibit stable locking behavior and effective noise suppression, aligned with practical analog PLL design goals.

Appendix

Appendix A: Project Resources

All simulation files, Verilog-A models, and supporting data used in this project are available in the following GitHub repository:

PLLcOURSEpROJECT

This repository contains:

- Verilog-A models for VCO, CP, and other blocks

- Testbench configurations and Cadence setup files
- Plots of output waveforms, phase noise, and transfer functions
- Final report

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