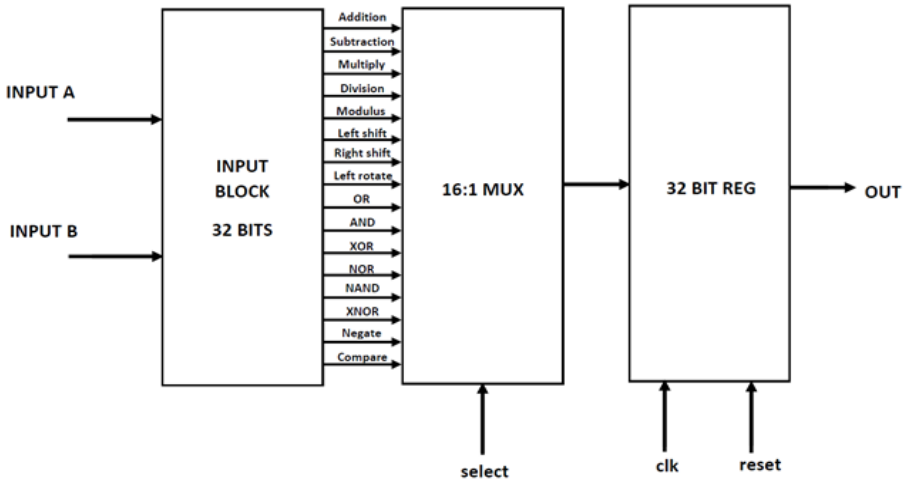
General Description

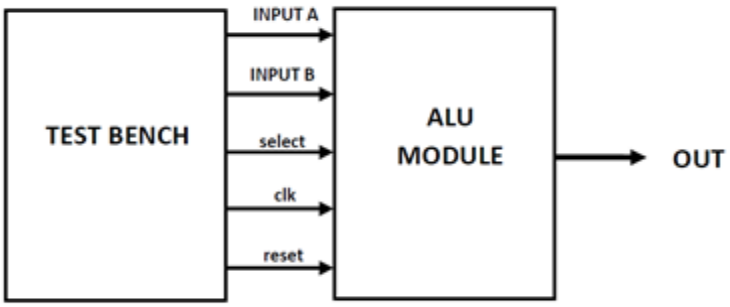
An Arithmetic Logic Unit (ALU) is the core component of the Central Processing Unit (CPU). ALU comprises the combinational logic circuit that performs arithmetic and logic operations.

32-bit ALU is designed to perform 16 operations which include both logical and arithmetic operations. The Verilog implementation of 32-bit ALU is done using the Modelsim tool. The two inputs and the output of the ALU are 32bit binary numbers. If the reset is high, the output is set to zero. One select line (4 bits) is used to perform the operations.

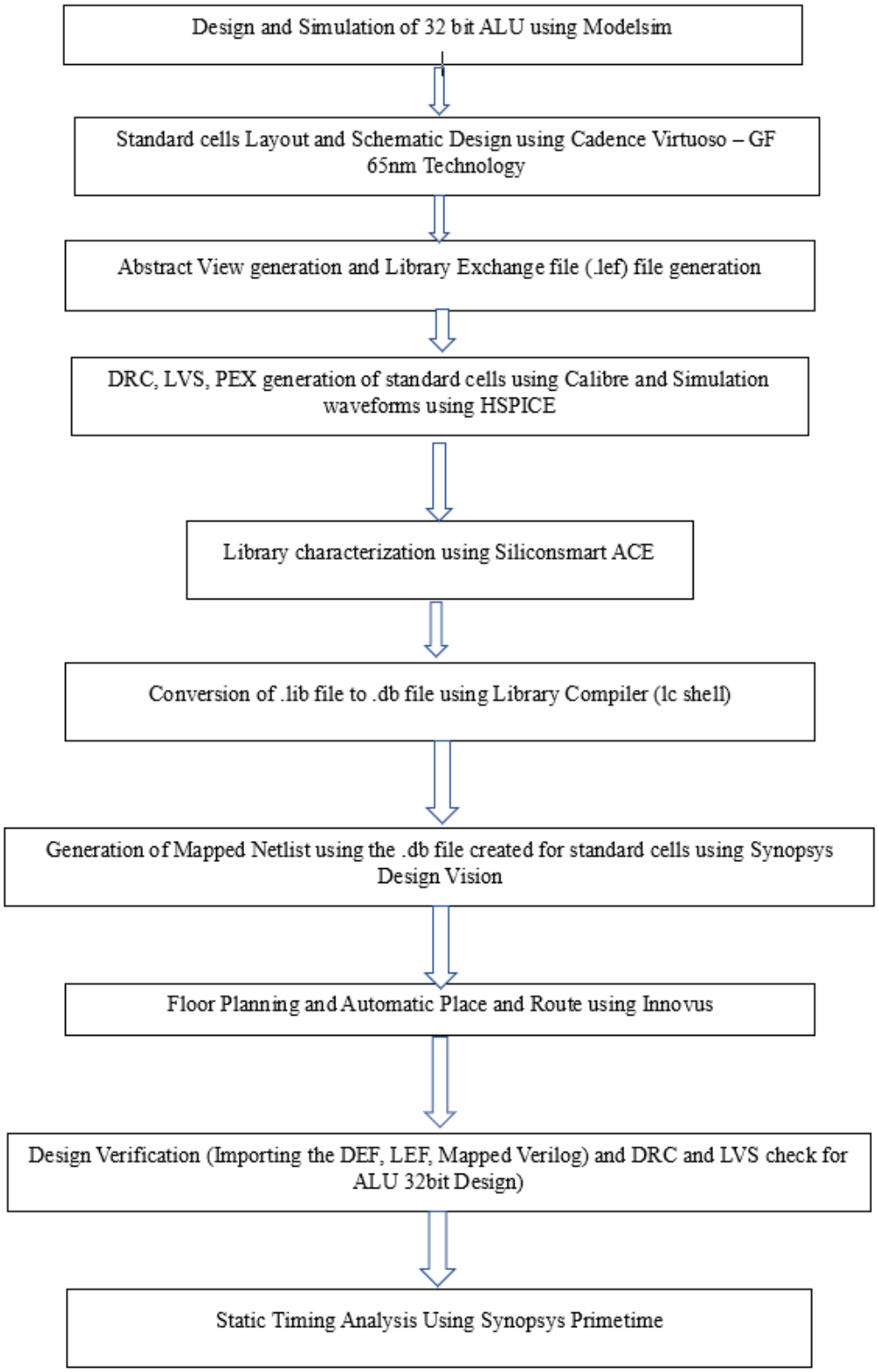
Block Diagram of 32-Bit ALU



Block Diagram with Test Bench



Complete Design Process



STANDARD CELL LIBRARY DESIGN

We designed standard cell layout using GF65nm technology in Cadence Virtuoso. The goal during the design phase was to minimize area. Along with the standard cells, the layout for positive edge triggered D-Flipflop was also designed to have only one diffusion break in order to achieve minimum area. We tested the cells by generating a clean DRC, LVS, PEX and also by simulating the waveforms using HSPICE.

The height of the standard cells = 5.46um

pin pitch= 0.26um.

Width of PMOS is such that it has minimum of 5 contacts- 1.13um

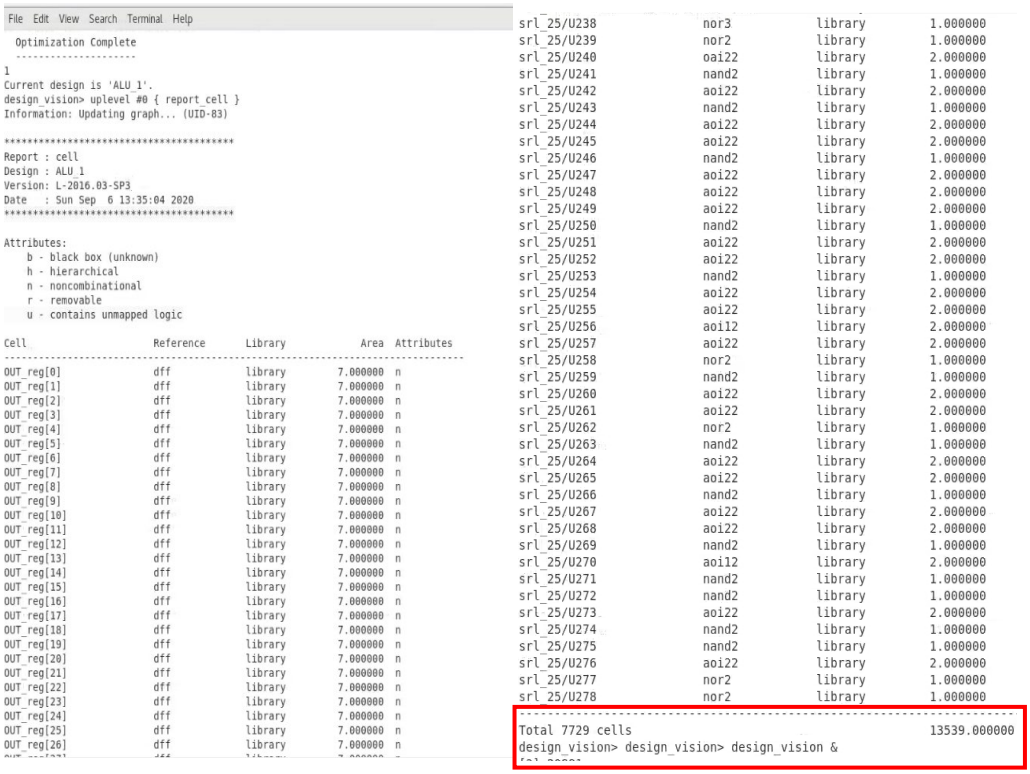
Width of NMOS is such that it has minimum of 3 contacts- 540nm.

The area of the cells is as shown below.

Cell Name	Area
INV	5.6784
NAND2	9.9372
NOR2	9.0980
MUX	15.6156
XOR	11.3568
AOI22	9.9372
AOI211	9.9372
OAI21	8.5176
DFF	28.3920

LIBRARY CHARACTERIZATION

Using the PEX files generated from each of the cell, library characterization was performed using Synopsys Silicon Smart. The Library files were combined to generated gf65.db using Library Compiler. The gf65.db file was used for setup in Design Vision for synthesis and created the mapped netlist of the ALU Verilog file. The design vision tool generated a cell report with 7729 cells.



```
File  Edit  View  Search  Terminal  Help

  Optimization Complete
  ---------------------
1
Current design is 'ALU_1'.
design_vision> uplevel #0 { report_cell }
Information: Updating graph... (UID-83)

****************************************
Report : cell
Design : ALU_1
Version: L-2016.03-SP3
Date   : Sun Sep  6 13:35:04 2020
****************************************

Attributes:
    b - black box (unknown)
    h - hierarchical
    n - noncombinational
    r - removable
    u - contains unmapped logic

Cell                    Reference       Library            Area  Attributes
--------------------------------------------------------------------------------
OUT_reg[0]              dff             library         7.000000  n
OUT_reg[1]              dff             library         7.000000  n
OUT_reg[2]              dff             library         7.000000  n
OUT_reg[3]              dff             library         7.000000  n
OUT_reg[4]              dff             library         7.000000  n
OUT_reg[5]              dff             library         7.000000  n
OUT_reg[6]              dff             library         7.000000  n
OUT_reg[7]              dff             library         7.000000  n
OUT_reg[8]              dff             library         7.000000  n
OUT_reg[9]              dff             library         7.000000  n
OUT_reg[10]             dff             library         7.000000  n
OUT_reg[11]             dff             library         7.000000  n
OUT_reg[12]             dff             library         7.000000  n
OUT_reg[13]             dff             library         7.000000  n
OUT_reg[14]             dff             library         7.000000  n
OUT_reg[15]             dff             library         7.000000  n
OUT_reg[16]             dff             library         7.000000  n
OUT_reg[17]             dff             library         7.000000  n
OUT_reg[18]             dff             library         7.000000  n
OUT_reg[19]             dff             library         7.000000  n
OUT_reg[20]             dff             library         7.000000  n
OUT_reg[21]             dff             library         7.000000  n
OUT_reg[22]             dff             library         7.000000  n
OUT_reg[23]             dff             library         7.000000  n
OUT_reg[24]             dff             library         7.000000  n
OUT_reg[25]             dff             library         7.000000  n
OUT_reg[26]             dff             library         7.000000  n
srl_25/U238             nor3            library         1.000000
srl_25/U239             nor2            library         1.000000
srl_25/U240             oai22           library         2.000000
srl_25/U241             nand2           library         1.000000
srl_25/U242             aoi22           library         2.000000
srl_25/U243             nand2           library         1.000000
srl_25/U244             aoi22           library         2.000000
srl_25/U245             aoi22           library         2.000000
srl_25/U246             nand2           library         1.000000
srl_25/U247             aoi22           library         2.000000
srl_25/U248             aoi22           library         2.000000
srl_25/U249             aoi22           library         2.000000
srl_25/U250             nand2           library         1.000000
srl_25/U251             aoi22           library         2.000000
srl_25/U252             aoi22           library         2.000000
srl_25/U253             nand2           library         1.000000
srl_25/U254             aoi22           library         2.000000
srl_25/U255             aoi22           library         2.000000
srl_25/U256             aoi12           library         2.000000
srl_25/U257             aoi22           library         2.000000
srl_25/U258             nor2            library         1.000000
srl_25/U259             nand2           library         1.000000
srl_25/U260             aoi22           library         2.000000
srl_25/U261             aoi22           library         2.000000
srl_25/U262             nor2            library         1.000000
srl_25/U263             nand2           library         1.000000
srl_25/U264             aoi22           library         2.000000
srl_25/U265             aoi22           library         2.000000
srl_25/U266             nand2           library         1.000000
srl_25/U267             aoi22           library         2.000000
srl_25/U268             aoi22           library         2.000000
srl_25/U269             nand2           library         1.000000
srl_25/U270             aoi12           library         2.000000
srl_25/U271             nand2           library         1.000000
srl_25/U272             nand2           library         1.000000
srl_25/U273             aoi22           library         2.000000
srl_25/U274             nand2           library         1.000000
srl_25/U275             nand2           library         1.000000
srl_25/U276             aoi22           library         2.000000
srl_25/U277             nor2            library         1.000000
srl_25/U278             nor2            library         1.000000
--------------------------------------------------------------------------------
Total 7729 cells                                        13539.000000
design_vision> design_vision> design_vision &
```

Automatic Placement and Routing using Cadence Innovus

After completing standard cells, abstract view was generated for all the cells using Abstract Generator. These abstract views were used to export LEF file from Cadence Virtuoso.

Using the synthesized mapped verilog file generated from Design Vision and the LEF file, the design was imported to Cadence Innovus. Placement was completed by performing FloorPlan, Connect Ground Nets, Placement of Standard Cells and Place Physical Cell for adding filler. Automatic Routing was implemented by selecting NanoRoute. Once the routing was complete, the design was saved as Netlist and DEF files.

Final Design Verification

In order to verify the final design of the ALU 32 bit, the LEF, DEF and Mapped Netlist files were imported to Cadence virtuoso. After performing Remaster Instance and Flatten the Hierarchy, DRC and LVS was performed.

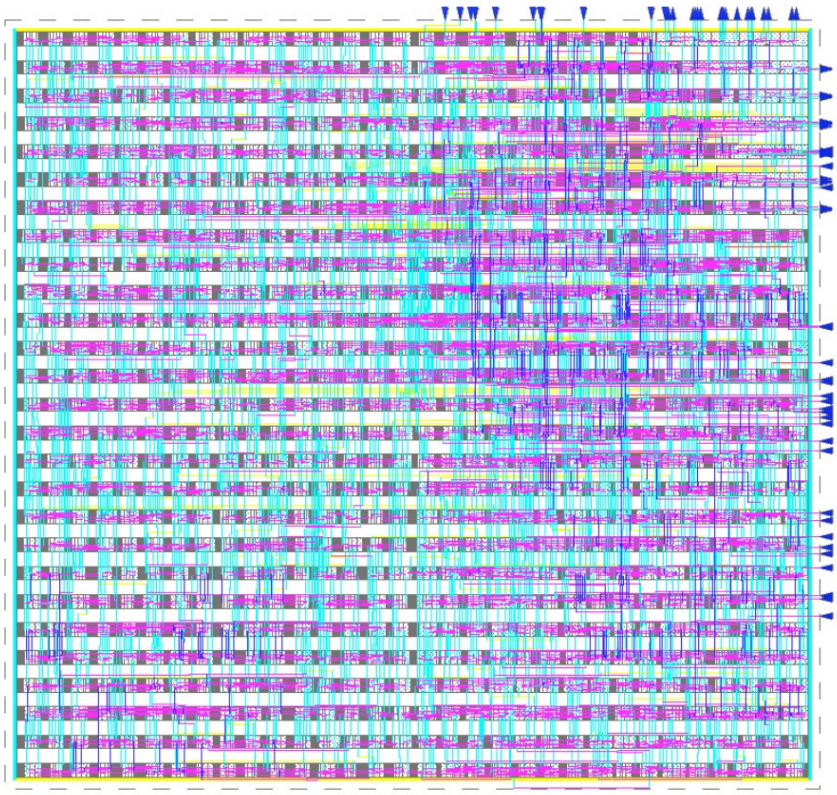


Figure 1 Design after Nanoroute

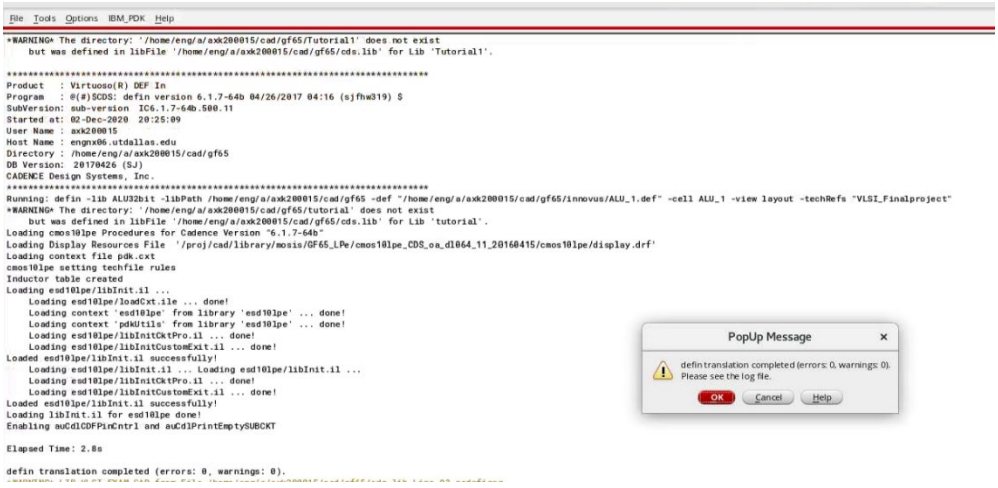
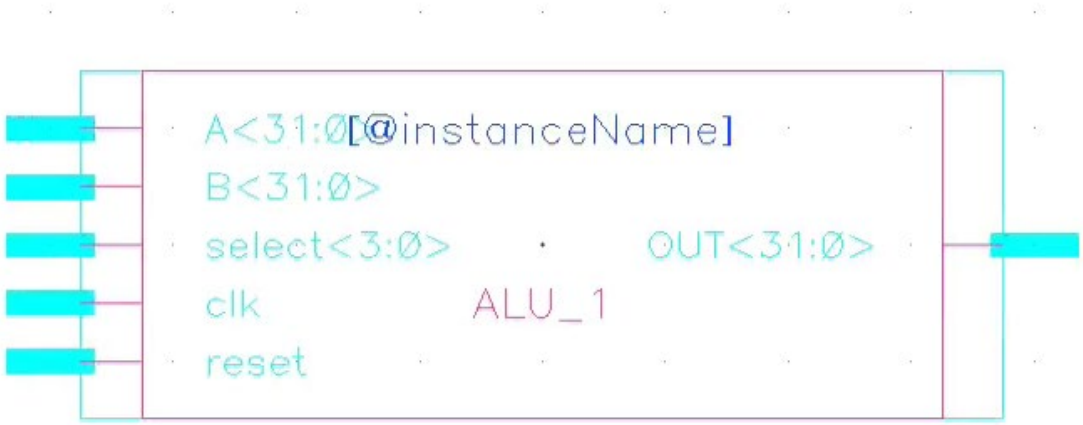
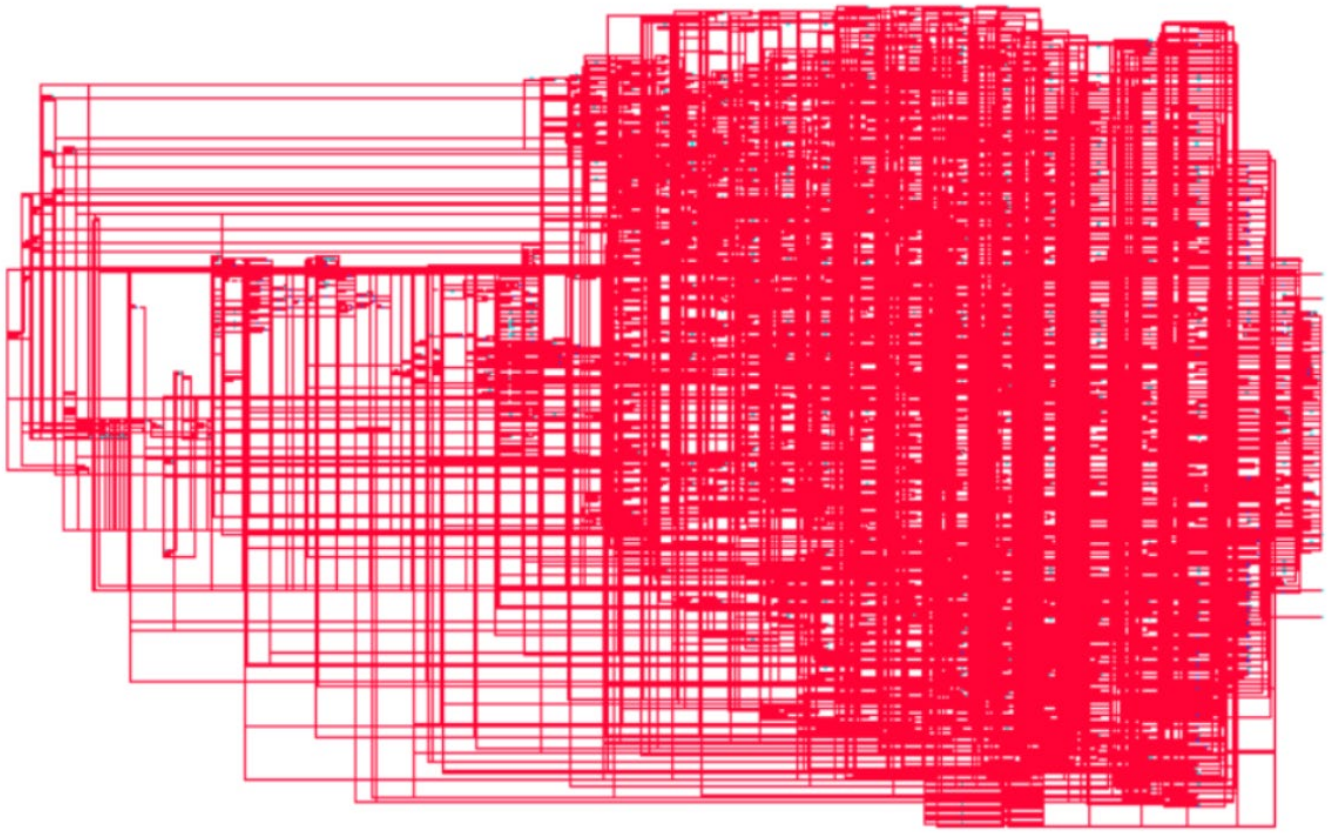


Figure 2 Successful DEF Import

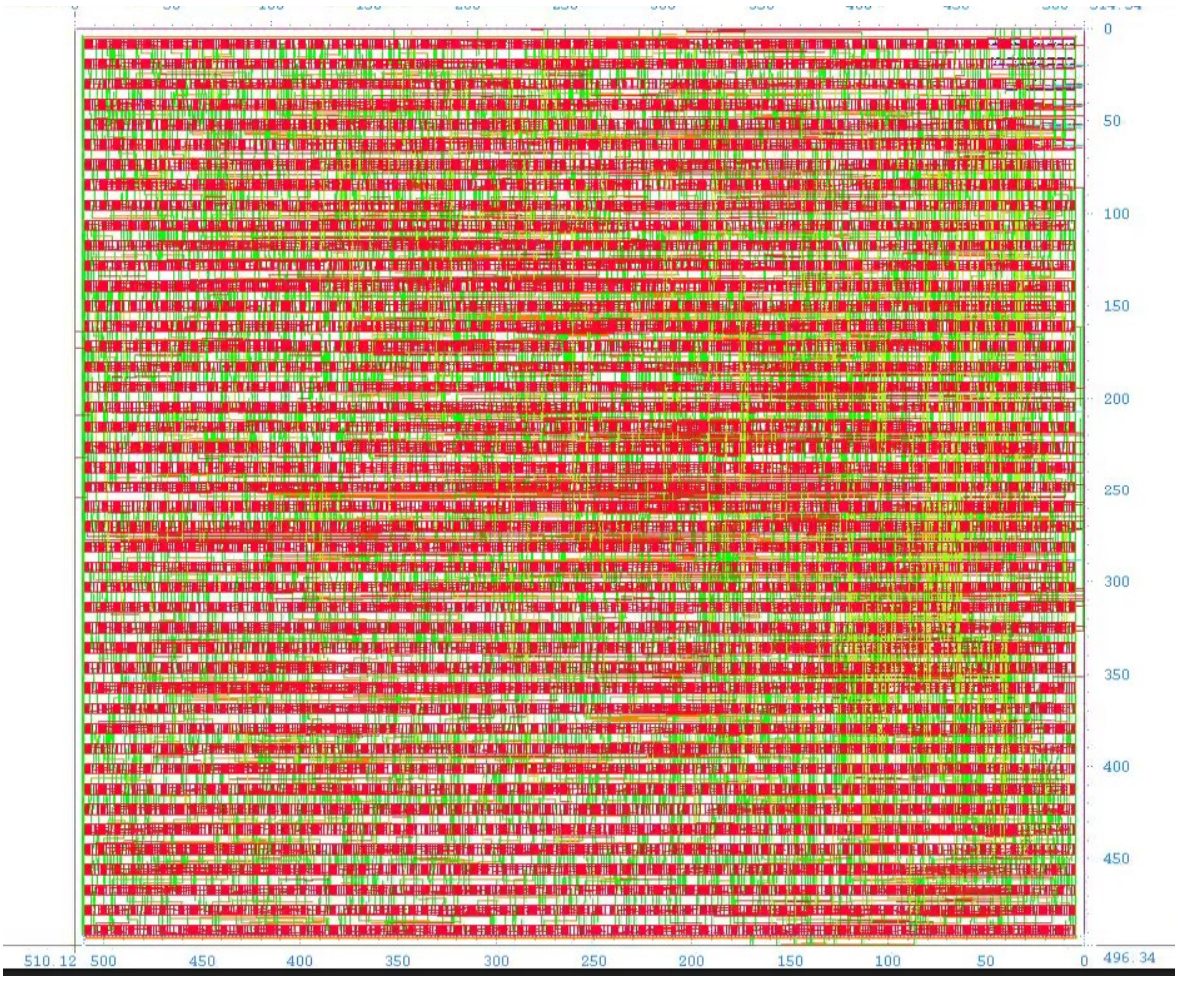
Final symbol view of the ALU design



Final schematic of ALU design



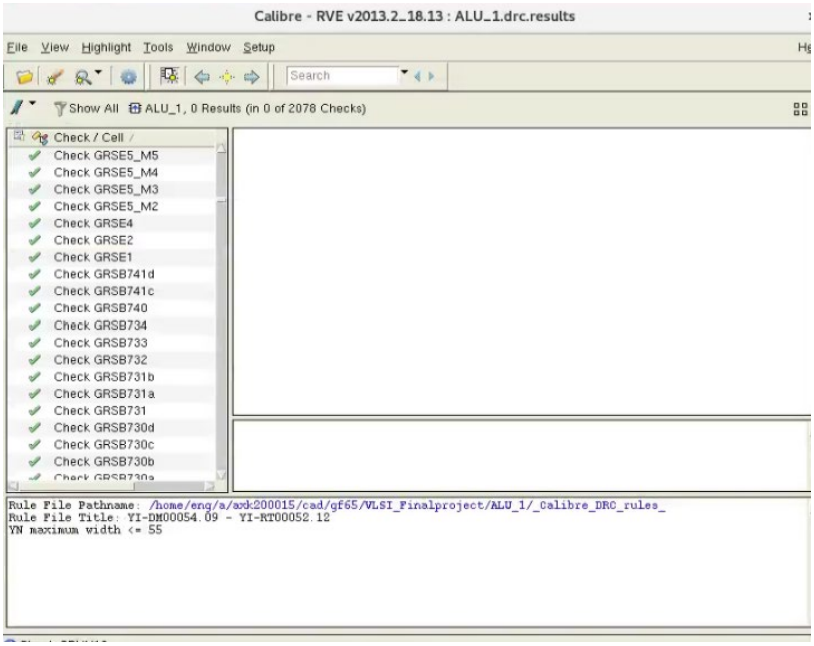
Final Layout of ALU

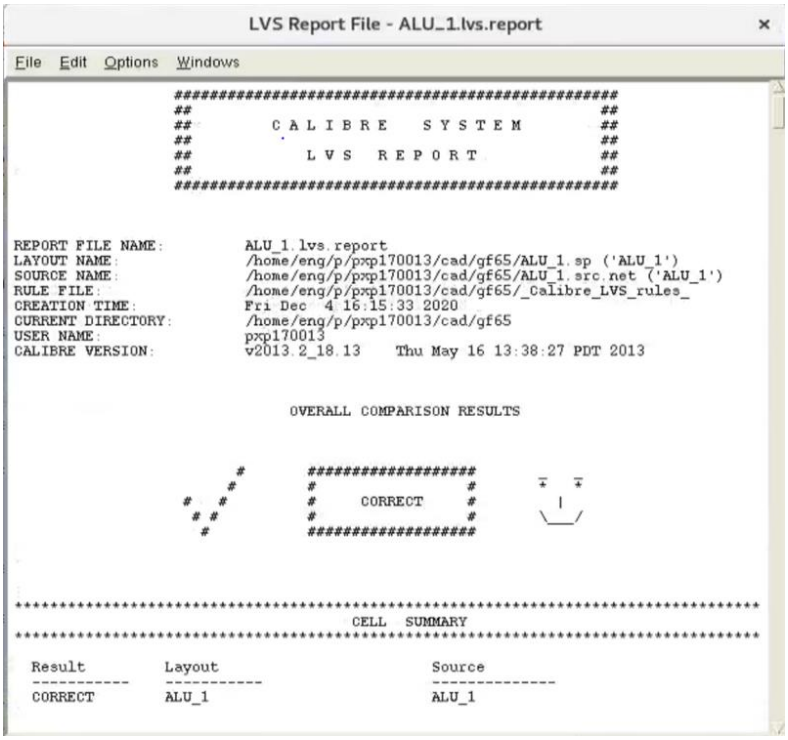


Height of the ALU layout = 496.34um
Width of the ALU layout = 510.12um

Zoomed Layout after Routing

DRC report

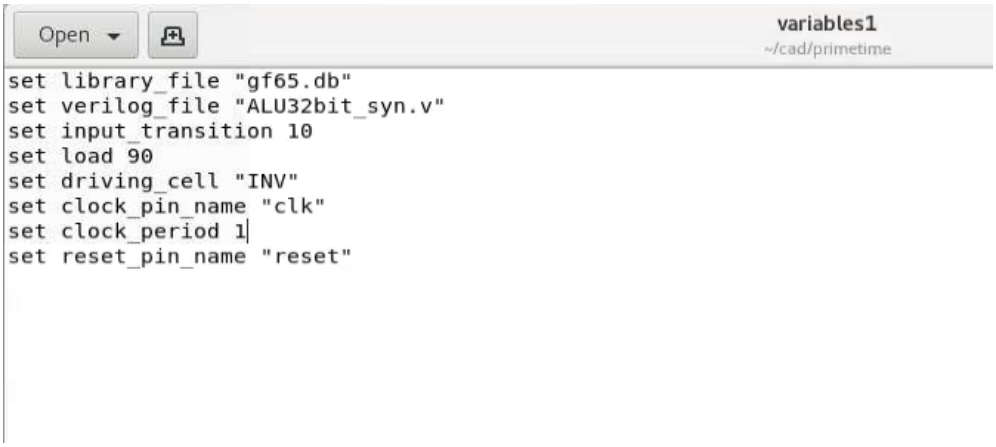

Calibre - RVE v2013.2_18.13 : ALU_1.drc.results
File View Highlight Tools Window Setup
Search
Show All ALU_1, 0 Results (in 0 of 2078 Checks)
Check / Cell
Check GRSE5_M5
Check GRSE5_M4
Check GRSE5_M3
Check GRSE5_M2
Check GRSE4
Check GRSE2
Check GRSE1
Check GRSB741d
Check GRSB741c
Check GRSB740
Check GRSB734
Check GRSB733
Check GRSB732
Check GRSB731b
Check GRSB731a
Check GRSB731
Check GRSB730d
Check GRSB730c
Check GRSB730b
Rule File Pathname: /home/eng/s/axk200015/cad/gf65/VLSI_Finalproject/ALU_1/_Calibre_DRC_rules_
Rule File Title: YI-DM00054.09 - YI-RT00052.12
YN maximum width <= 55


LVS Report File - ALU_1.lvs.report
File Edit Options Windows
C A L I B R E S Y S T E M
L V S R E P O R T
REPORT FILE NAME: ALU_1.lvs.report
LAYOUT NAME: /home/eng/p/pxp170013/cad/gf65/ALU_1.sp ('ALU_1')
SOURCE NAME: /home/eng/p/pxp170013/cad/gf65/ALU_1.src.net ('ALU_1')
RULE FILE: /home/eng/p/pxp170013/cad/gf65/_Calibre_LVS_rules_
CREATION TIME: Fri Dec 4 16:15:33 2020
CURRENT DIRECTORY: /home/eng/p/pxp170013/cad/gf65
USER NAME: pxp170013
CALIBRE VERSION: v2013.2_18.13 Thu May 16 13:38:27 PDT 2013
OVERALL COMPARISON RESULTS
CORRECT
CELL SUMMARY
Result Layout Source
CORRECT ALU_1 ALU_1

STATIC TIMING ANALYSIS

In order by validate if the design could operate at the rated clock frequency without any timing violations, we utilize Synopsys Primetime to perform Static Timing Analysis. We obtained the total power required by the design and the slack (Required Time-Arrival Time) for min and max path. We plotted the power required against Clock period to analyze the design.

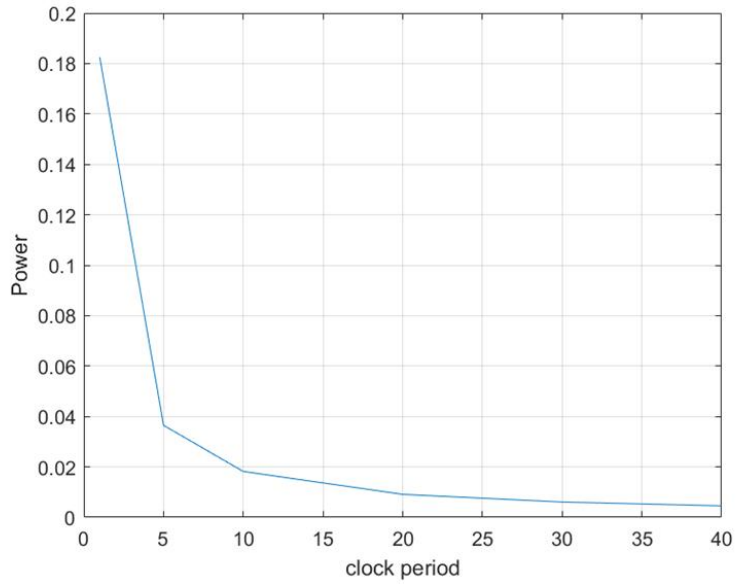
The Primetime tool requires a .db file and a verilog netlist to operate. The driving cell, clock and load variables were then defined as per the given requirement in the variable 1 file, shown below.



Power report

```
engnx06.utdallas.edu:/home/eng/a/axk200015/cad/primetime
File  Edit  View  Search  Terminal  Help
report_power
****************************************
Report : Averaged Power
Design : ALU_1
Version: M-2016.12-SP3-1
Date   : Fri Dec  4 11:39:44 2020
****************************************


  Attributes
  ----------
      i  -  Including register clock pin internal power
      u  -  User defined power group

                        Internal  Switching  Leakage    Total
Power Group             Power     Power      Power      Power   (     %)  Attrs
--------------------------------------------------------------------------------
clock_network              0.0000    0.0000    0.0000    0.0000 ( 0.00%)  i
register                1.671e-04 9.204e-04 5.667e-08 1.088e-03 ( 6.98%)
combinational           7.933e-03 6.563e-03 6.592e-07    0.0145 (93.02%)
sequential                 0.0000    0.0000    0.0000    0.0000 ( 0.00%)
memory                     0.0000    0.0000    0.0000    0.0000 ( 0.00%)
io_pad                     0.0000    0.0000    0.0000    0.0000 ( 0.00%)
black_box                  0.0000    0.0000    0.0000    0.0000 ( 0.00%)

  Net Switching Power  = 7.484e-03   (48.02%)
  Cell Internal Power  = 8.100e-03   (51.98%)
  Cell Leakage Power   = 7.159e-07   ( 0.00%)
                         ---------
Total Power            =    0.0156  (100.00%)

1
exit
Information: Defining new variable 'driving_cell'. (CMD-041)
Information: Defining new variable 'library_file'. (CMD-041)
Information: Defining new variable 'verilog_file'. (CMD-041)
Information: Defining new variable 'input_transition'. (CMD-041)
Information: Defining new variable 'timing_slew_propagation_mode'. (CMD-041)
Information: Defining new variable 'clock_period'. (CMD-041)
Information: Defining new variable 'load'. (CMD-041)
Information: Defining new variable 'reset_pin_name'. (CMD-041)
Information: Defining new variable 'clock_pin_name'. (CMD-041)

Timing updates: 1 (1 implicit, 0 explicit) (0 incremental, 1 full, 0 logical)
Noise updates: 0 (0 implicit, 0 explicit) (0 incremental, 0 full)
Maximum memory usage for this session: 790.91 MB
CPU usage for this session: 20 seconds
Elapsed time for this session: 9 seconds
Diagnostics summary: 2 warnings, 12 informationals
```

Power vs Clock Period Plot



For different values of clock period the corresponding power was noted. It was observed that the power consumption increases as the clock period decreases. The maximum power consumption happens at the first clock period.

Timing report

engnx06.utdallas.edu:/home/eng/a/axk200015/cad/primetime

File Edit View Search Terminal Help

```
update_timing
1
report_timing -transition_time -delay min_max -capacitance -input_pins
****************************************
Report : timing
        -path_type full
        -delay_type min_max
        -input_pins
        -max_paths 1
        -transition_time
        -capacitance
        -sort_by slack
Design : ALU_1
Version: M-2016.12-SP3-1
Date   : Fri Dec  4 11:39:39 2020
****************************************


  Startpoint: OUT_reg[28]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: OUT[28] (output port)
  Path Group: (none)
  Path Type: min

  Point                                   Cap      Trans       Incr       Path
  -------------------------------------------------------------------------------
  OUT_reg[28]/CLK (DFF)                            0.00       0.00       0.00 r
  OUT_reg[28]/OUT (DFF)                   0.50     1.48       1.08       1.08 r
  OUT[28] (out)                                    1.48       0.00       1.08 r
  data arrival time                                                      1.08
  -------------------------------------------------------------------------------
  (Path is unconstrained)


  Startpoint: OUT_reg[28]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: OUT[28] (output port)
  Path Group: (none)
  Path Type: max

  Point                                   Cap      Trans       Incr       Path
  -------------------------------------------------------------------------------
  OUT_reg[28]/CLK (DFF)                           10.00       0.00       0.00 r
  OUT_reg[28]/OUT (DFF)                   0.50     0.95       1.84       1.84 r
  OUT[28] (out)                                    0.95       0.00       1.84 r
  data arrival time                                                      1.84
  -------------------------------------------------------------------------------
  (Path is unconstrained)
```

TRADEOFF

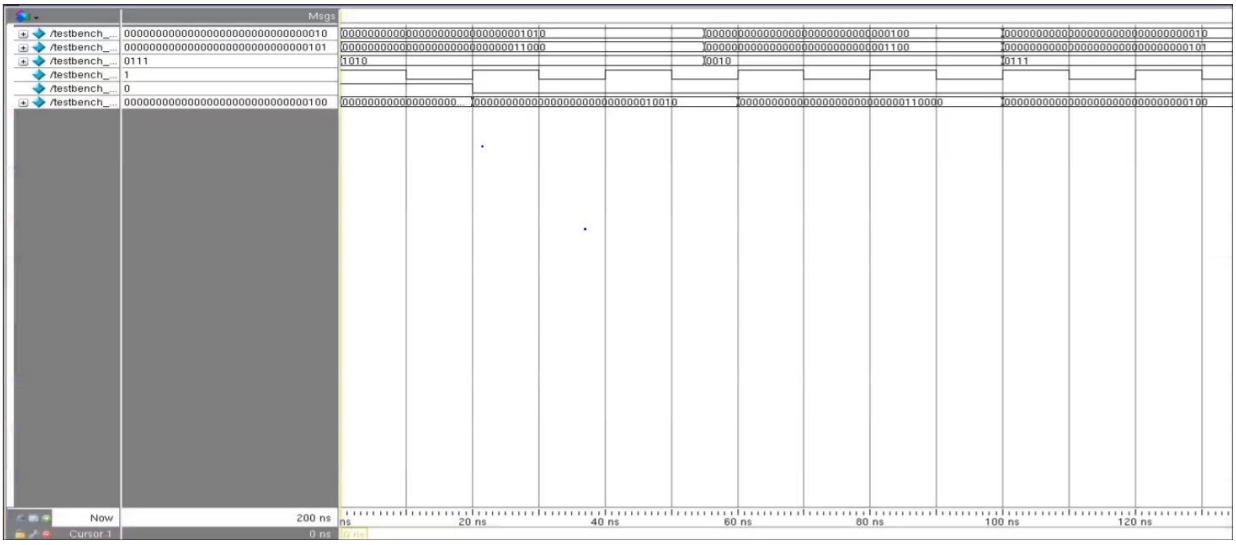
- The Energy Delay Product was decreased while increasing nMOS width. The best width was selected by sweeping the Wp and Wn values using HSPICE.
- The height of the D Flipflop standard cell increases as the total height of the cell was fixed with an odd multiple of the pin pitch size and this increased height of all other cells.
- The Total Power of the design increases as the Clock Period increases.

TESTING METHODOLOGY

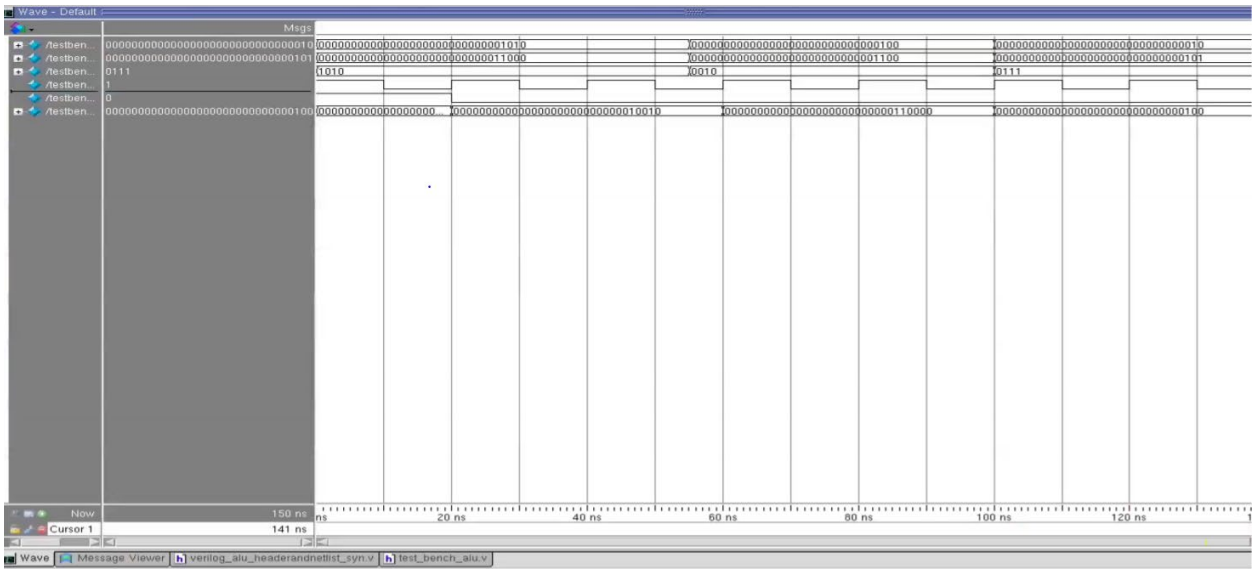
- The Synthesized Verilog netlist generated using our gf65.db file was tested with a Testbench using Modelsim. The output waveform was checked for ALU functionality.
- The standard cell layout was verified using DRC (Design Rule Checkers) to ensure that the layout satisfies the design rules.
- Layout vs Schematic Tools (LVS) checked to verify transistors in the layout are connected in the same way as in the schematic.
- The output of the standard cell was verified using HSPICE simulation.
- The DEF of the routed layout was imported into Cadence Virtuoso to perform DRC and LVS.

SIMULATION WAVEFORM

1) Behavioral Code Output Waveform



2) Mapped netlist waveform using the gf65.db library.



CONCLUSION

The 32-bit ALU was designed starting from the behavioral code to routing and laying out the entire design. All the cells were designed to have minimum diffusion breaks without using M2 layer. Also the cells were designed to have minimum area. Utilizing Cadence Innovus, the standard cells were automatically placed and route based on the mapped netlist. The final routed layout was verified by performing DRC and LVS in Cadence Virtuoso. At the end, Static Timing Analysis was done using Primetime tool which reported the power and timing characteristics of the ALU.

Parameter	**Value**
Number of Operations	16
Total Number of Cells	7729
Final Top Cell Height	496.34um
Final Top Cell Width	510.12 um
Top Cell Area	253192.961um2
Total Power	0.0156W

Header:

```
module INV(IN, OUT);
input IN;
output OUT;
assign OUT = ~IN;
endmodule

module NAND(A, B, OUT);
input A, B;
output OUT;
assign OUT = ~(A & B);
endmodule

module NOR2(A, B, OUT);
input A, B;
output OUT;
assign OUT = ~(A | B);
endmodule

module XOR(A, B, OUT);
input A, B;
output OUT;
assign OUT = (A ^ B);
endmodule

module MUX(A, B, SEL,OUT);
input A, B, SEL;
output OUT;
assign OUT = ~((A & (~(SEL))) | (B & SEL));
endmodule

module AOI211(A, B, C, D, OUT);
input A, B, C, D;
output OUT;
assign OUT = ~((A & B) | C | D);
endmodule

module AOI22(A, B, C, D, OUT);
input A, B, C, D;
output OUT;
assign OUT = ~((A & B) | (C & D));
endmodule

module OAI21(A, B, C, OUT);
input A, B, C;
output OUT;
```

```
assign OUT = ~((A | B) & C);
endmodule

module DFF( D, CLK, R, OUT);
input D, CLK, R;
output OUT;
reg OUT;
always @(posedge CLK or negedge R)
  if (R == 1'b0)
    OUT = 1'b0;
  else
    OUT = D;
endmodule
```

Behavioral Verilog Code of the ALU

```
 module ALU(

        input [31:0] A,   //Input A

        input [31:0] B,   //Input B

        input [3:0] select, /*select line will chose the appropriate operation on the input(s) which includes both arithmetic and logical operations*/

        input clk, //Clock signal

        input reset, //Reset signal

        output reg [31:0] OUT); //Output of the ALU

// D - Flip Flop

always@(posedge clk) //operations are performed on the positive edge of the clock

begin

//When the reset is 0, this part of the code runs. That means, the operations are carried out when reset is set to low.

if(!reset)

begin


//case is used for the multiplexer. Select line is used to choose the operation
```

```
case(select)
4'b0000: OUT = A+B; //addition operation
4'b0001: OUT = A-B; //subtraction operation
4'b0010: OUT =A*B; //multiplication operation
4'b0011: OUT = A/B; //division operation
4'b0100: OUT = A%B; //modulus operation
4'b0101: OUT =A<<B; //left shift operation
4'b0110: OUT = A>>B; //right shift operation
4'b0111: OUT ={A[30:0],A[31]}; //left rotate operation
4'b1000: OUT = A|B; // bitwise OR operation
4'b1001: OUT = A&B; // bitwise AND operation
4'b1010: OUT = A^B; // bitwise XOR operation
4'b1011: OUT =~(A|B); // bitwise NOR operation
4'b1100: OUT =~(A&B); //bitwise NAND operation
4'b1101: OUT = ~(A^B); // bitwise XNOR operation
4'b1110: OUT = ~B; // negate operation
4'b1111: OUT = (A==B); // comparison operation
endcase
end
else
begin
// if reset is high on the positive edge of the clock, the outputs are set to zero
OUT=0; //Reset is 1, OUT is reset to low
end
end
endmodule
```

Test Bench:

```
module testbench_ALU;
// Inputs
reg [31:0] A;
reg [31:0] B;
reg [3:0] select;
reg clk;
reg reset;

// Outputs
wire [31:0] OUT;

// Instantiate the Unit Under Test (UUT)
ALU_1 uut (
.A(A),
.B(B),
.select(select),
.clk(clk),
.reset(reset),
.OUT(OUT)
);
always begin
#10 clk = ~clk; // Toggling the clock for every 10 time units. So the clock cycle is 20 time units
end
initial begin
// Initialize Inputs
A = 32'b00000000000000000000000000001010;
B = 32'b00000000000000000000000000011000;
select = 4'b1010;  //XOR operation on A and B
clk=1;
reset=1; // The output is zero and remains zero till the reset is set to low.
#20; // The output is retained for 20 time units which is one clock cycle.
reset=0; // reset is set to low

#35; // The second arithmetic operation set after 35 time units
```

```
A = 32'b00000000000000000000000000000100;
B = 32'b00000000000000000000000000001100;
select = 4'b0010;     //Multiplication operation on A and B

#45; // The third logical operation set after 45 time units
A = 32'b00000000000000000000000000000010;
B = 32'b00000000000000000000000000000101;
select = 4'b0111;     //Left rotation operation on B
end
endmodule
```