Assignment On

Course Title: Digital Logic Design Lab

Course Code: CSEL-2104

Submitted To,

Professor Dr. Mohammed Nasir Uddin

Department of CSE

Jagannath University, Dhaka

Submitted By,

Atik Jawad

ID: B220305043

Department of Computer Science & Engineering

Jagannath University, Dhaka

Date of Submission: 23/4/2025

Table of Contents

1 Decimal to Binary

Given function: $F = \sum m\ (0,1,5,7,9,10,21,23,25,30) + D\ (4,17)$

1. $0_{10} = ?_2$

$$\begin{array}{c|l} 2 & 0 \\ \hline & 0(LSB) \end{array}$$

$$0_{10} = 00000_2$$

2. $1_{10} = ?_2$

$$\begin{array}{c|l} 2 & 1 \\ \hline & 0\text{- - - - - -}1(LSB) \end{array}$$

$$1_{10} = 00001_2$$

3. $5_{10} = ?_2$

$$\begin{array}{c|l} 2 & 5 \\ \hline 2 & 2\text{- - - - - -}1 \\ \hline & 1\text{- - - - - -}0(LSB) \end{array}$$

$$5_{10} = 00101_2$$

4. $7_{10} = ?_2$

$$\begin{array}{c|l} 2 & 7 \\ \hline 2 & 3\text{- - - - - -}1 \\ \hline 2 & 1\text{- - - - - -}1 \\ \hline & 0\text{- - - - - -}1(LSB) \end{array}$$

$$7_{10} = 00111_2$$

5. $9_{10} = ?_2$

$$\begin{array}{c|l} 2 & 9 \\ \hline 2 & 4\text{- - - - - -}1 \\ \hline 2 & 2\text{- - - - - -}0 \\ \hline & 1\text{- - - - - -}0(LSB) \end{array}$$

$$9_{10} = 01001_2$$

6. $10_{10} = ?_2$

$$\begin{array}{c|l} 2 & 10 \\ \hline 2 & 5\text{- - - - - -}0 \\ \hline 2 & 2\text{- - - - - -}1 \\ \hline & 1\text{- - - - - -}0(LSB) \end{array}$$

$$10_{10} = 01010_2$$

7. $21_{10} = ?_2$

2	21
2	10– – – – – ––1
2	5– – – – – ––0
2	2– – – – – ––1
	1– – – – – ––0(*LSB*)

$21_{10} = 10101_2$

8. $23_{10} = ?_2$

2	23
2	11– – – – – ––1
2	5– – – – – ––1
2	2– – – – – ––1
	1– – – – – ––0(*LSB*)

$23_{10} = 10111_2$

9. $25_{10} = ?_2$

2	25
2	12– – – – – ––1
2	6– – – – – ––0
2	3– – – – – ––0
2	1– – – – – ––1
	0– – – – – ––1(*LSB*)

$25_{10} = 11001_2$

10. $30_{10} = ?_2$

2	30
2	15– – – – – ––0
2	7– – – – – ––1
2	3– – – – – ––1
2	1– – – – – ––1
	0– – – – – ––1(*LSB*)

$30_{10} = 11110_2$

2 Standard Form Representation

$$F = \sum m\,(0,1,5,7,9,10,21,23,25,30) + D\,(4,17)$$

Truth table:

A	*B*	*C*	*D*	*E*	*Minterms*	*F*
0	0	0	0	0	m_0	**1**
0	0	0	0	1	m_1	**1**
0	0	0	1	0	m_2	0
0	0	0	1	1	m_3	0
0	0	1	0	0	m_4	*X*
0	0	1	0	1	m_5	**1**
0	0	1	1	0	m_6	0
0	0	1	1	1	m_7	**1**
0	1	0	0	0	m_8	0
0	1	0	0	1	m_9	**1**
0	1	0	1	0	m_{10}	**1**
0	1	0	1	1	m_{11}	0
0	1	1	0	0	m_{12}	0
0	1	1	0	1	m_{13}	0
0	1	1	1	0	m_{14}	0
0	1	1	1	1	m_{15}	0
1	0	0	0	0	m_{16}	0
1	0	0	0	1	m_{17}	*X*
1	0	0	1	0	m_{18}	0
1	0	0	1	1	m_{19}	0
1	0	1	0	0	m_{20}	0
1	0	1	0	1	m_{21}	**1**
1	0	1	1	0	m_{22}	0
1	0	1	1	1	m_{23}	**1**
1	1	0	0	0	m_{24}	0
1	1	0	0	1	m_{25}	**1**
1	1	0	1	0	m_{26}	0
1	1	0	1	1	m_{27}	0
1	1	1	0	0	m_{28}	0
1	1	1	0	1	m_{29}	0
1	1	1	1	0	m_{30}	**1**
1	1	1	1	1	m_{31}	0

Sum of products:

$$F = \bar{A}\bar{B}\bar{C}\bar{D}\bar{E} + \bar{A}\bar{B}\bar{C}\bar{D}E + \bar{A}\bar{B}C\bar{D}E + \bar{A}\bar{B}CDE + \bar{A}B\bar{C}\bar{D}E + \bar{A}B\bar{C}D\bar{E} + A\bar{B}C\bar{D}E + A\bar{B}CDE + AB\bar{C}\bar{D}E + ABCD\bar{E}$$

3 Simplification

3.1 Using Boolean Algebra

$$F = \bar{A}\bar{B}\bar{C}\bar{D}\bar{E} + \bar{A}\bar{B}\bar{C}\bar{D}E + \bar{A}\bar{B}C\bar{D}E + \bar{A}\bar{B}CDE + \bar{A}B\bar{C}\bar{D}E + \bar{A}B\bar{C}D\bar{E} + A\bar{B}C\bar{D}E + A\bar{B}CDE + AB\bar{C}\bar{D}E + ABCD\bar{E}$$

$$= \bar{A}\bar{B}\bar{C}\bar{D}\bar{E} + \bar{A}\bar{B}\bar{C}\bar{D}E + \bar{A}\bar{B}C\bar{D}E + \bar{A}\bar{B}CDE + \bar{A}B\bar{C}\bar{D}E + \bar{A}B\bar{C}D\bar{E} + A\bar{B}C\bar{D}E + A\bar{B}CDE + AB\bar{C}\bar{D}E + ABCD\bar{E}$$

$$= \bar{A}\bar{B}\bar{C}\bar{D}(\bar{E} + E) + \bar{A}\bar{B}C\bar{D}E + \bar{A}\bar{B}CDE + \bar{A}B\bar{C}\bar{D}E + \bar{A}B\bar{C}D\bar{E} + A\bar{B}C\bar{D}E + A\bar{B}CDE + AB\bar{C}\bar{D}E + ABCD\bar{E}$$

$$= \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}C\bar{D}E + \bar{A}\bar{B}CDE + \bar{A}B\bar{C}\bar{D}E + \bar{A}B\bar{C}D\bar{E} + A\bar{B}C\bar{D}E + A\bar{B}CDE + AB\bar{C}\bar{D}E + ABCD\bar{E}$$

$$= \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}C(\bar{D}E + DE) + \bar{A}B\bar{C}\bar{D}E + \bar{A}B\bar{C}D\bar{E} + A\bar{B}C\bar{D}E + A\bar{B}CDE + AB\bar{C}\bar{D}E + ABCD\bar{E}$$

$$= \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}CE + \bar{A}B\bar{C}\bar{D}E + \bar{A}B\bar{C}D\bar{E} + A\bar{B}C\bar{D}E + A\bar{B}CDE + AB\bar{C}\bar{D}E + ABCD\bar{E}$$

$$= \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}C + A\bar{B}C(\bar{D}E + DE) + \bar{A}B\bar{C}\bar{D}E + \bar{A}B\bar{C}D\bar{E} + AB\bar{C}\bar{D}E + ABCD\bar{E}$$

$$= \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}C + A\bar{B}CE + \bar{A}B\bar{C}\bar{D}E + \bar{A}B\bar{C}D\bar{E} + AB\bar{C}\bar{D}E + ABCD\bar{E}$$

$$= \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}C + A\bar{B}C + \bar{A}B\bar{C}(\bar{D}E + D\bar{E}) + AB\bar{C}\bar{D}E + ABCD\bar{E}$$

$$= \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}C + A\bar{B}C + \bar{A}B\bar{C}\bar{D}E + \bar{A}B\bar{C}D\bar{E} + AB(\bar{C}\bar{D}E + CD\bar{E})$$

$$= \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}C + A\bar{B}C + \bar{A}B\bar{C}\bar{D}E + \bar{A}B\bar{C}D\bar{E} + A\bar{B}\bar{C}DE + AB\bar{C}\bar{D}E + ABCD\bar{E}$$

$$= \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}C + \bar{A}B\bar{C}\bar{D}E + \bar{A}B\bar{C}D\bar{E} + A\bar{B}E(C\bar{D} + CD + \bar{C}D) + AB\bar{C}\bar{D}E + ABCD\bar{E}$$

$$= \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}C + \bar{A}B\bar{C}\bar{D}E + \bar{A}B\bar{C}D\bar{E} + ABCE + AB\bar{C}\bar{D}E + ABCD\bar{E}$$

$$= \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}C + \bar{A}B\bar{C}\bar{D}E + \bar{A}B\bar{C}D\bar{E} + ABCE + AB(\bar{C}\bar{D}E + CD\bar{E} + \bar{C}DE)$$

$$= \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}C + \bar{A}B\bar{C}\bar{D}E + \bar{A}B\bar{C}D\bar{E} + ABCE + ABC\bar{D}$$

$$= \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}C + \bar{A}B\bar{C}(\bar{D}E + D\bar{E}) + ABCE + ABC\bar{D}$$

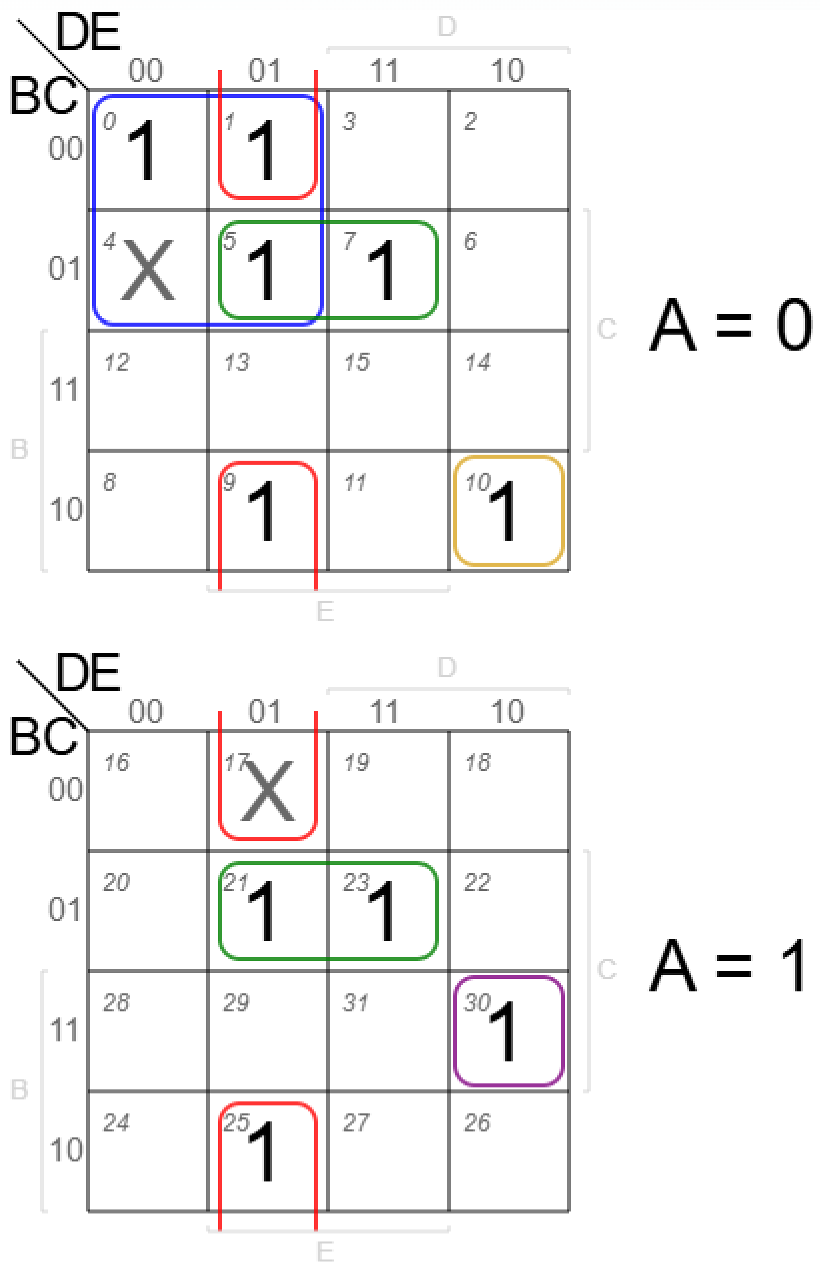
$$\boxed{F = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}C + \bar{A}B\bar{D}E + ABCE + ABC\bar{D}}$$

(Note: Boolean algebra is prone to errors; K-map is more reliable.)

3.2 Using K-map

$$F = \sum m\,(0,1,5,7,9,10,21,23,25,30) + D\,(4,17)$$

Let, X=4 & X=17 be two 'Don't Care Terms'.



From the above k-map we get,

$$F = \bar{B}CE + \bar{A}\bar{B}\bar{D} + \bar{C}\bar{D}E + \bar{A}B\bar{C}D\bar{E} + ABCD\bar{E}$$

3.3 Using Quine-McCluskey

$F = \sum m\ (0,1,5,7,9,10,21,23,25,30) + D\ (4,17)$

Step 1: Group by number of 1s:

Group	Minterms	Binary
0	0	00000
1	1	00001
	4	00100
2	5	00101
	9	01001
	10	01010
	17	10001
3	7	00111
	21	10101
	25	11001
4	23	10111
	30	11110

Step 2: Pair minterms differing by one bit:

Group	Minterms	Binary
0	0, 4	00-00
	0, 1	0000-
1	1, 17	-0001
	1, 9	0-001
	1, 5	00-01
	4, 5	0010-
2	5,21	-0101
	5, 7	001-1
	9,25	-1001
	17, 25	1-001
	17, 21	10-01
3	7,23	-0111
	21, 23	101-1

Step 3: Merging of Minterm pairs:

Groups	Minterms	Binary
0	0, 1, 4, 5	00-0-
1	1, 9, 17, 25	--001
	1, 5, 17, 21	-0-01
2	5, 7, 21, 23,	-01-1

Step 4: Prime Implicants Chart:

Minterms	0	1	5	7	9	10	21	23	25	30	Prime Implicants
10						X					$\bar{A}B\bar{C}D\bar{E}$
30										X	$ABCD\bar{E}$
0,1,4,5	X	X	X								$\bar{A}\bar{B}\bar{D}$
1,5,17,21		X	X				X				$\bar{B}\bar{D}\mathrm{E}$
1,9,17,25		X			X				X		$\bar{C}\bar{D}E$
5,7,21,23			X	X			X	X			$\bar{B}CE$

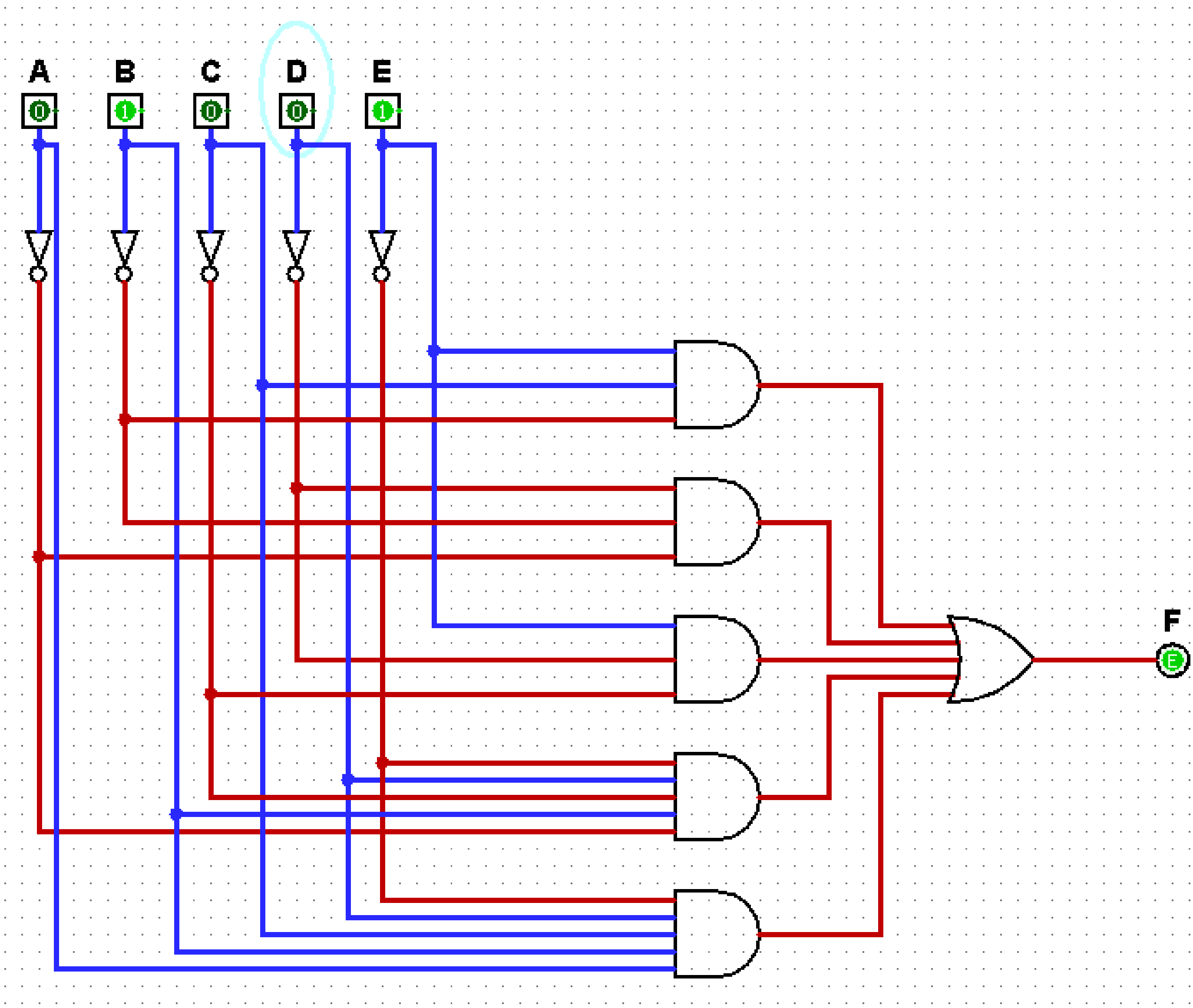
From the above Table we get,

$$F = \bar{B}CE + \bar{A}\bar{B}\bar{D} + \bar{C}\bar{D}E + \bar{A}B\bar{C}D\bar{E} + ABCD\bar{E}$$

4 Implementation

4.1 Using Primary Gates

$$F = \bar{B}CE + \bar{A}\bar{B}\bar{D} + \bar{C}\bar{D}E + \bar{A}B\bar{C}D\bar{E} + ABCD\bar{E}$$

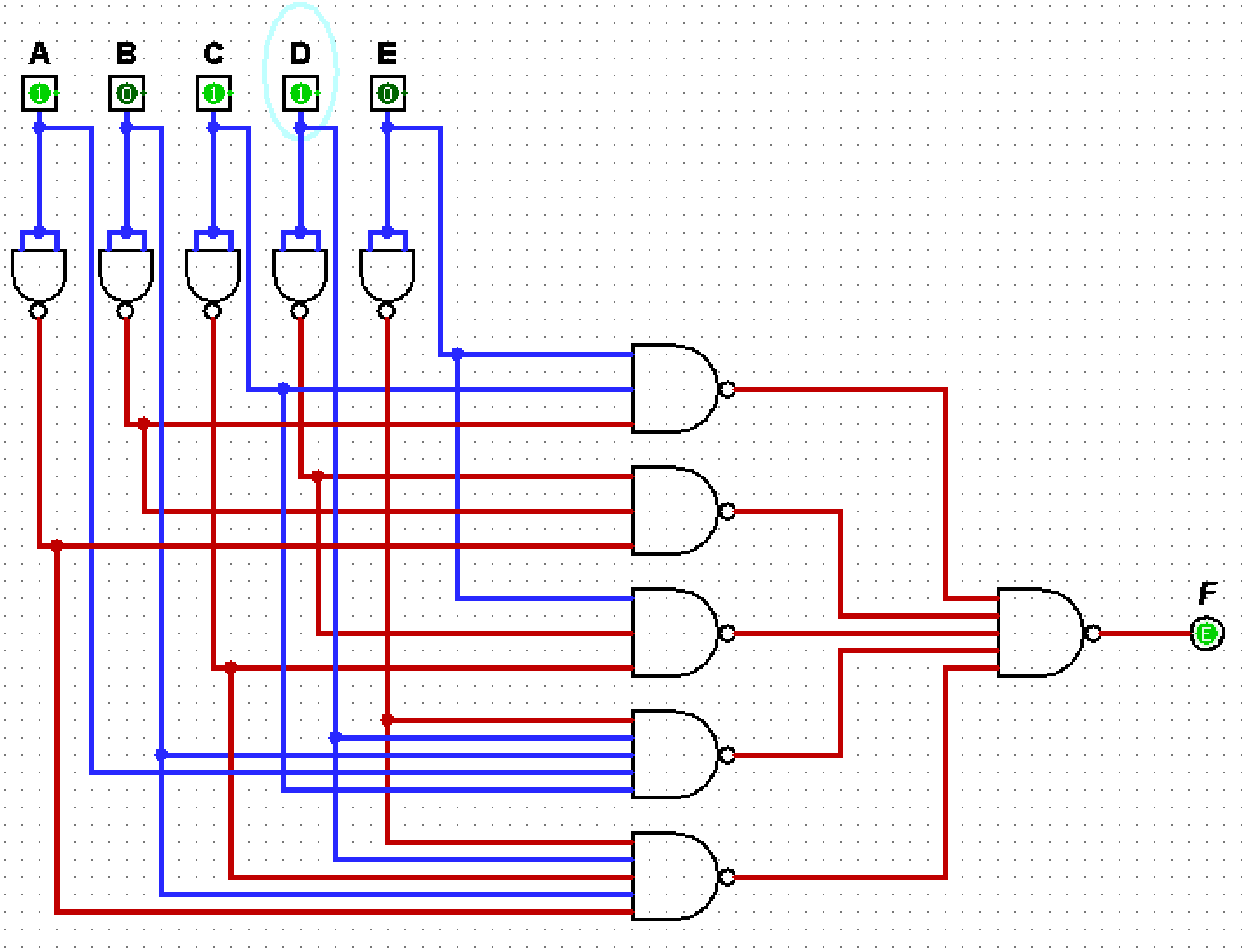


.

4.2 Using NAND Gates

Used De Morgan's Law to convert the SOP to NAND Form:

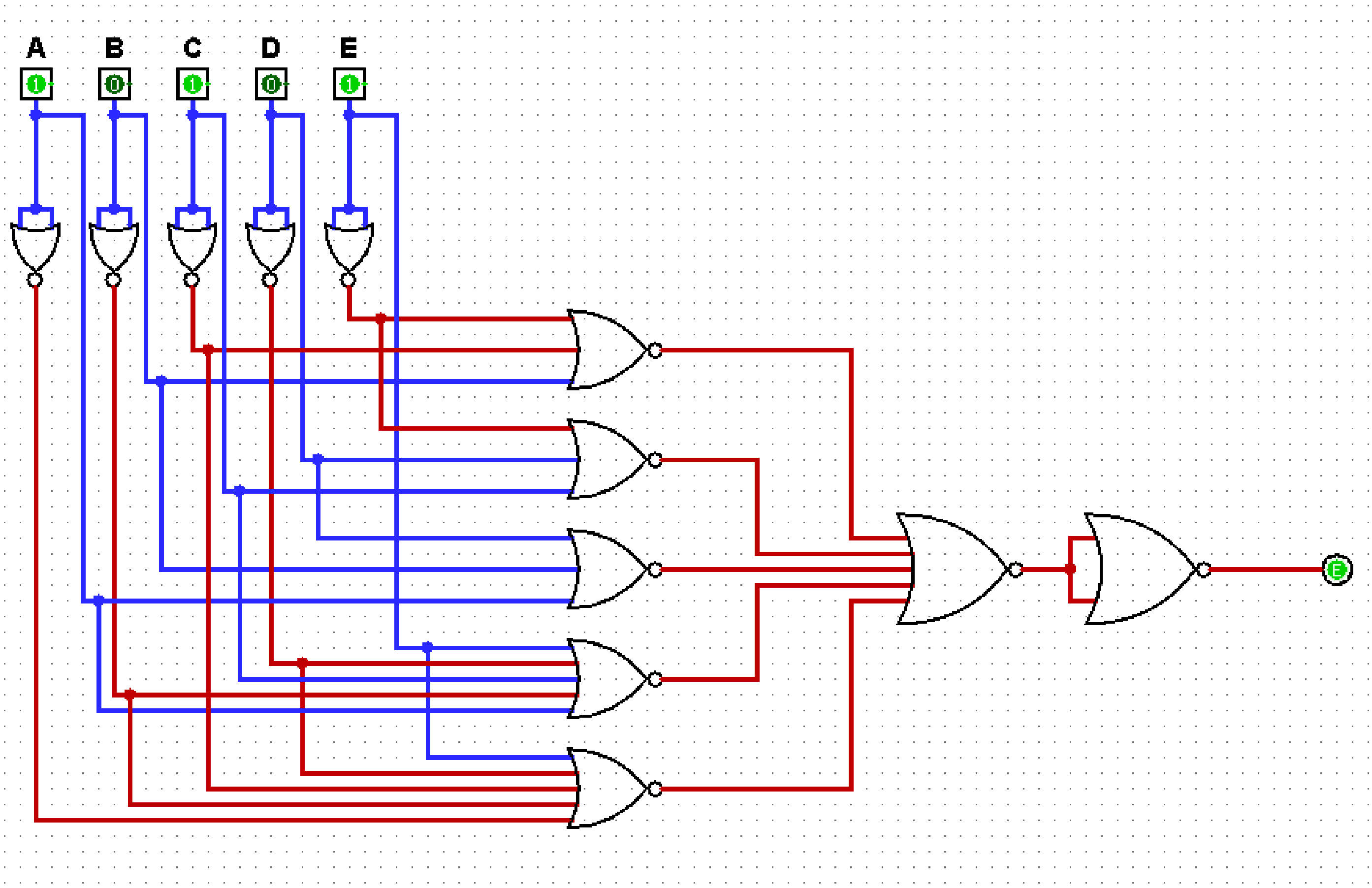
$$F = \overline{\overline{\bar{B}CE}.\ \overline{\bar{A}\bar{B}\bar{D}}\ .\ \overline{\bar{C}\bar{D}E}\ .\ \overline{\bar{A}B\bar{C}D\bar{E}}\ .\overline{ABCD\bar{E}}}$$



4.3 Using NOR Gates

Used De Morgan's Law to convert the SOP to NOR Form:

F = $\overline{(B + \bar{C} + \bar{E})}$ + $\overline{(C + D + \bar{E})}$ + $\overline{(A + B + D)}$ + $\overline{(A + \bar{B} + C + \bar{D} + E)}$ + $\overline{(\bar{A} + \bar{B} + \bar{C} + \bar{D} + E)}$



5 BCD to GRAY Code

Minterms	BCD				GRAY Code			
	B_3	B_2	B_1	B_0	G_3	G_2	G_1	G_0
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	1
2	0	0	1	0	0	0	1	1
3	0	0	1	1	0	0	1	0
4	0	1	0	0	0	1	1	0
5	0	1	0	1	0	1	1	1
6	0	1	1	0	0	1	0	1
7	0	1	1	1	0	1	0	0
8	1	0	0	0	1	1	0	0
9	1	0	0	1	1	1	0	1

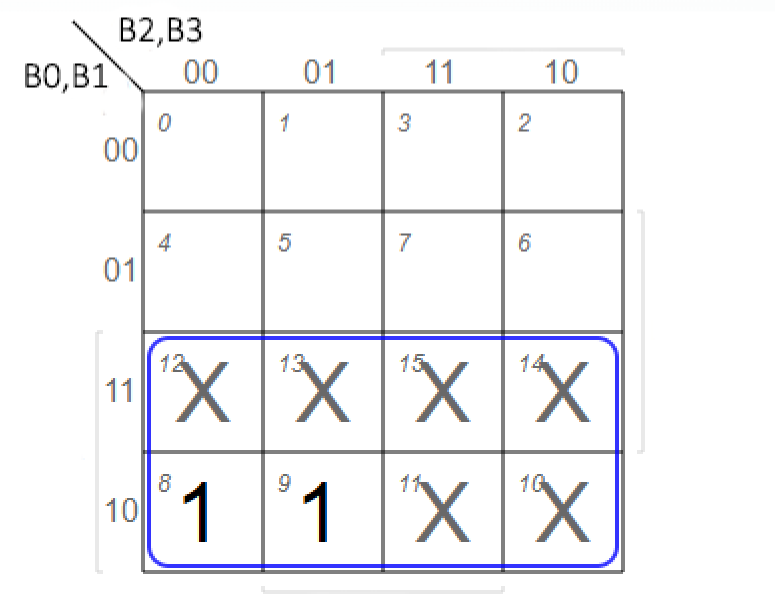
$G_3 = \sum m\ (8, 9) + d\ (10, 11, 12, 13, 14, 15)$

$G_2 = \sum m\ (4, 5, 6, 7, 8, 9) + d\ (10, 11, 12, 13, 14, 15)$

$G_1 = \sum m\ (2, 3, 4, 5) + d\ (10, 11, 12, 13, 14, 15)$

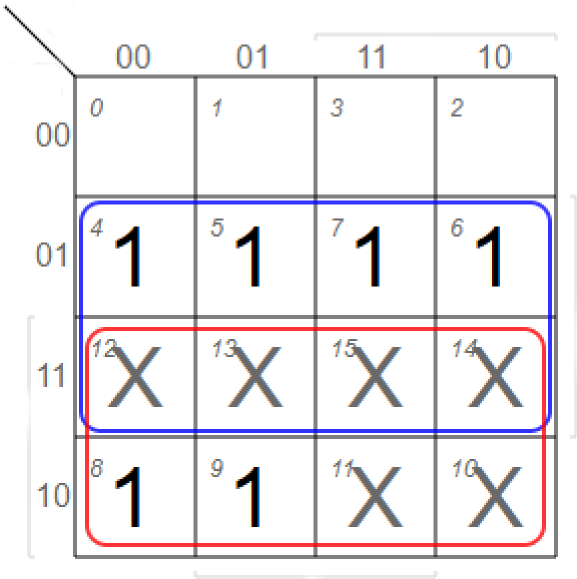
$G_0 = \sum m\ (1, 2, 5, 6, 9) + d\ (10, 11, 12, 13, 14, 15)$

K-map for G_3:



Here, $G_3 = B_3$

K-map for G_2:

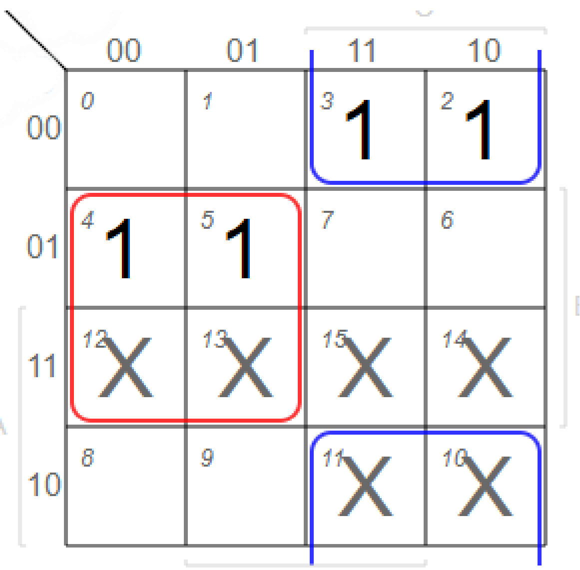


Here, $G_2 = B_2 + B_3$

K-map for G_1:

Here,

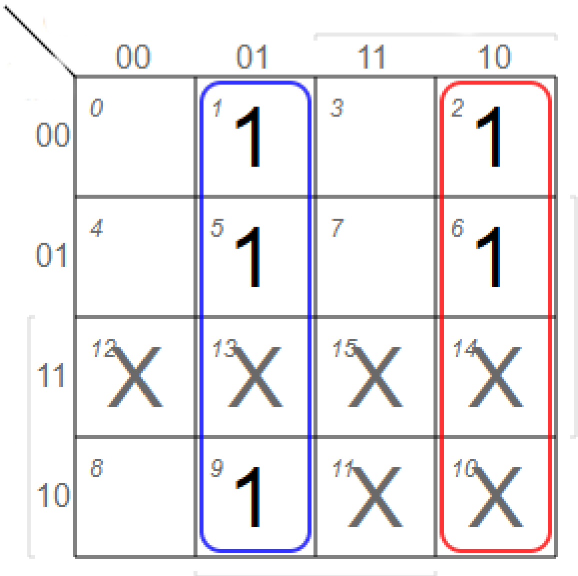
$G_1 = B_1 \oplus B_2$



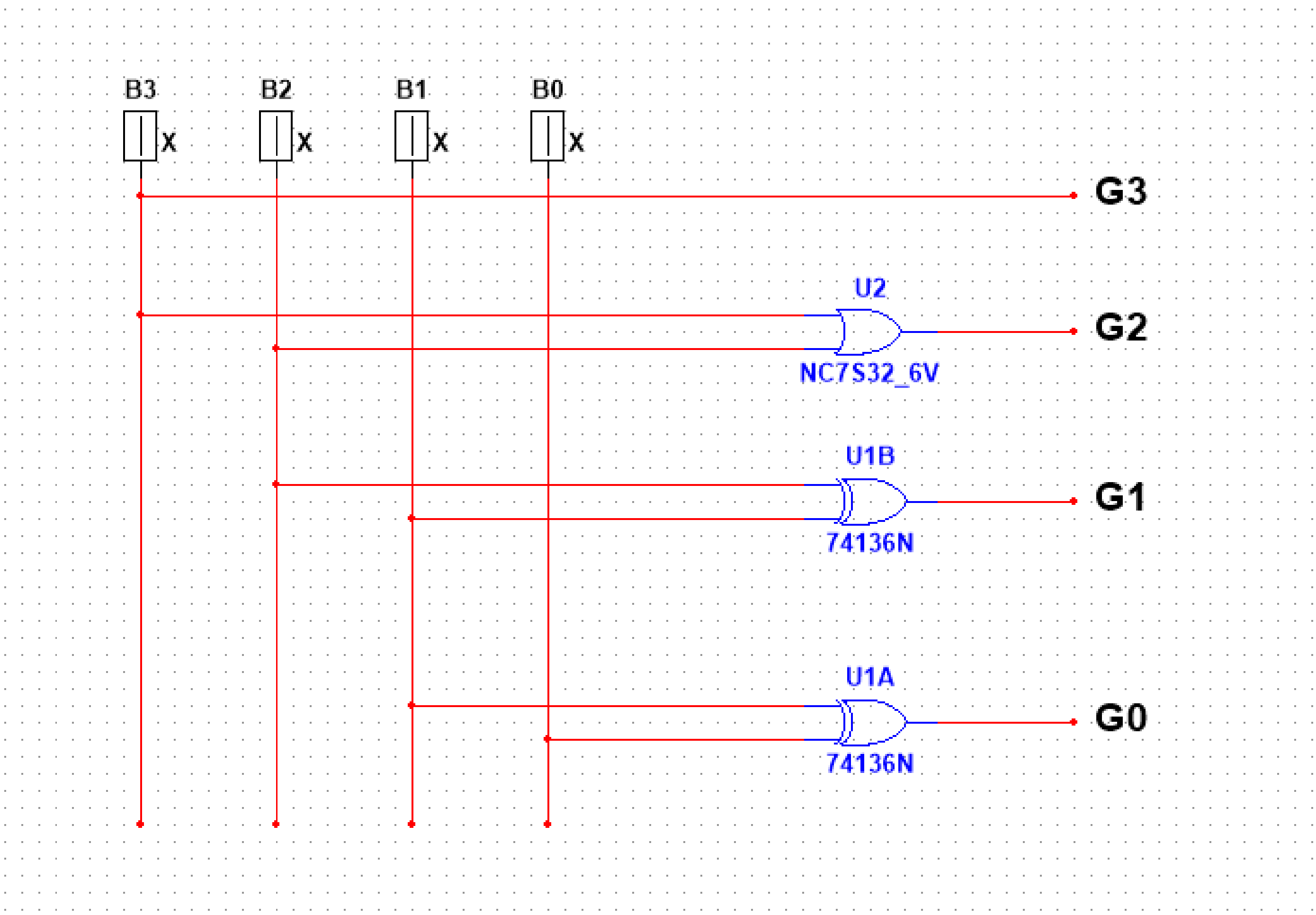
K-map for G_0:

Here,

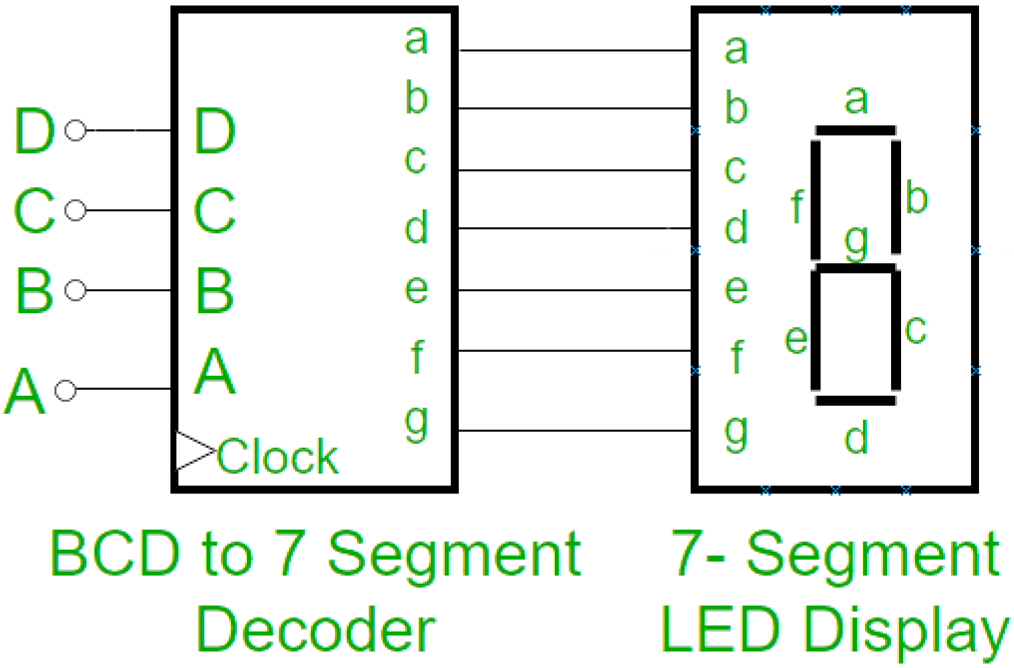
$G_0 = B_1 \oplus B_0$



The Following Figure is the Logic Diagram for converting BCD to Gray code:



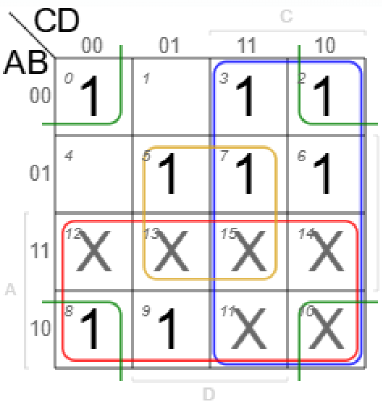
6 BCD to 7 Segment Decoder



Truth Table:

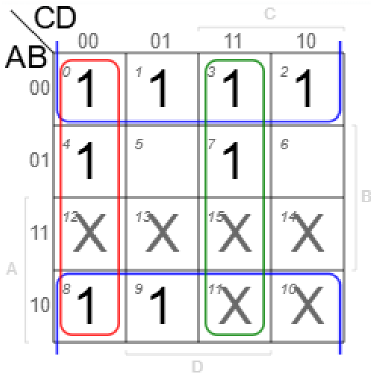
BCD Input				7 Segment Output Lines							Display
A	B	C	D	a	b	c	d	e	f	g	
0	0	0	0	1	1	1	1	1	1	0	0
0	0	0	1	0	1	1	0	0	0	0	1
0	0	1	0	1	1	0	1	1	0	1	2
0	0	1	1	1	1	1	1	0	0	1	3
0	1	0	0	0	1	1	0	0	1	1	4
0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	1	0	1	1	1	1	1	6
0	1	1	1	1	1	1	0	0	0	0	7
1	0	0	0	1	1	1	1	1	1	1	8
1	0	0	1	1	1	1	1	0	1	1	9

Kmap for a:



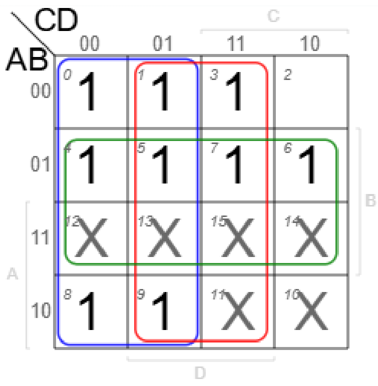
$a = \overline{B}\ \overline{D} + A + C + BD$

Kmap for b:



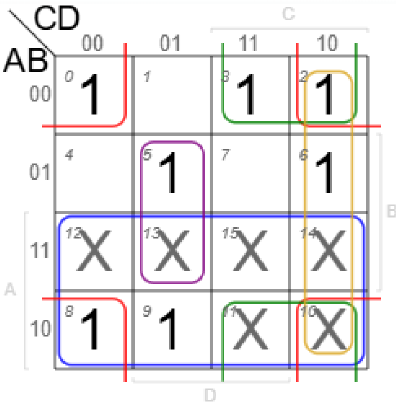
$b = \overline{B} + \overline{C}\ \overline{D} + CD$

Kmap for c:



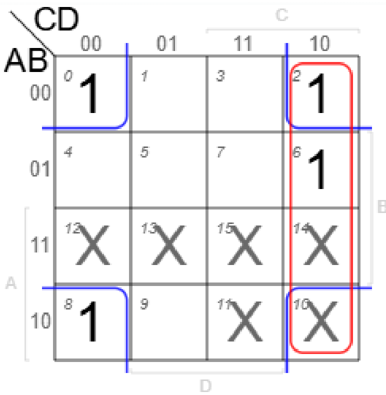
$c = \overline{C} + D + B$

Kmap for d:



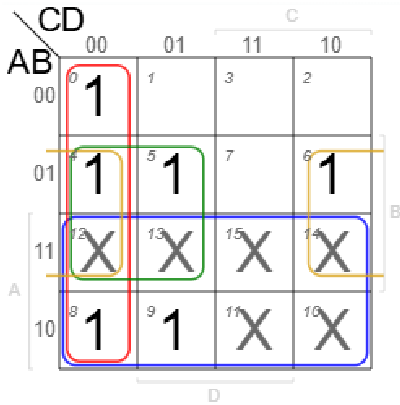
$d = \overline{B}\ \overline{D} + \overline{B}\,C + C\,\overline{D} + B\,\overline{C}\,D + A$

Kmap for e:



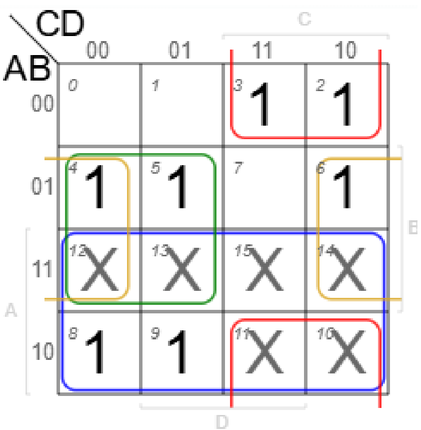
$e = \overline{B}\ \overline{D} + C\,\overline{D}$

kmap for f:



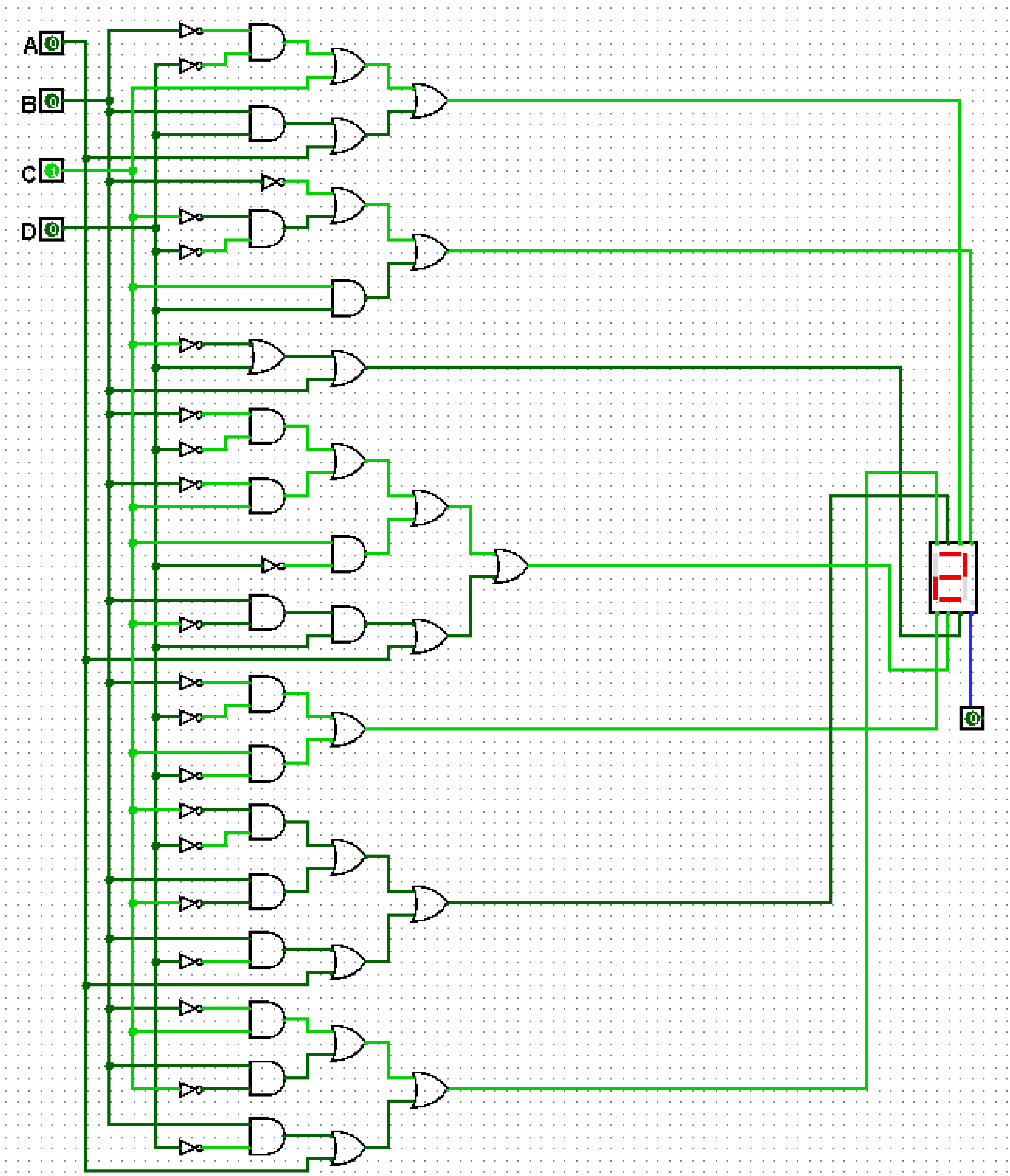
$f = \overline{C}\ \overline{D} + B\overline{C} + B\overline{D} + A$

Kmap for g:



$g = \overline{B}\,C + B\overline{C} + B\overline{D} + A$

Logic Simulation of 7 Segment Decoder is given below:



7 Implementation of Decoder and Encoder

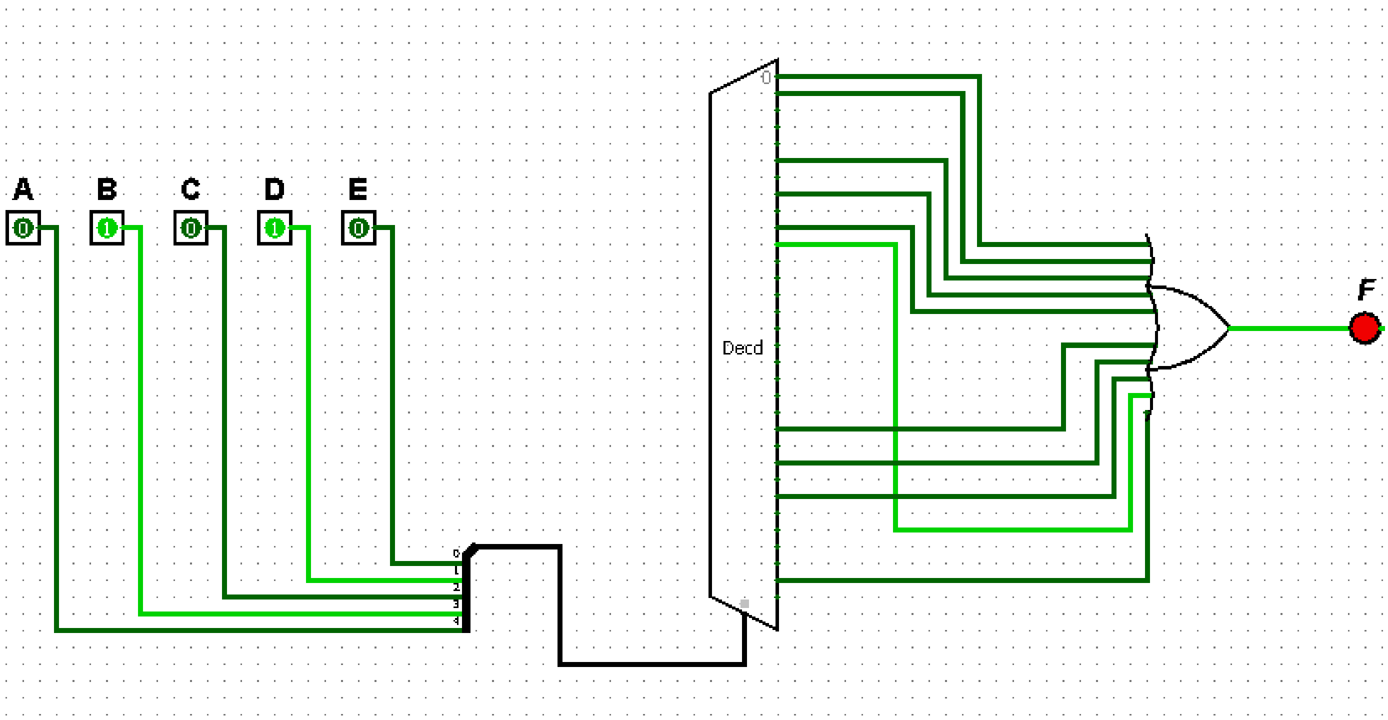
7.1 Decoder

A digital circuit that **takes a binary input** and **activates exactly one output line** based on that input — it basically *decodes* binary numbers into one-hot encoded outputs.

A **5-to-32 decoder** has:

- **2 input lines** (say, A, B ,C ,D ,E)
- **32 output lines** (O0 to O31)

$$F = \sum m\,(0,1,5,7,9,10,21,23,25,30)$$



TruthTable of the 5 to 32 Decoder

A	B	C	D	E	O0	O1	O2	O3	O4	O5	O6	O7	O8	O9	O10	O11	O12	O13	O14	O15	O16	O17	O18	O19	O20	O21	O22	O23	O24	O25	O26	O27	O28	O29	O30	O31
0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	1	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	1	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	1	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0
1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0
1	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	0

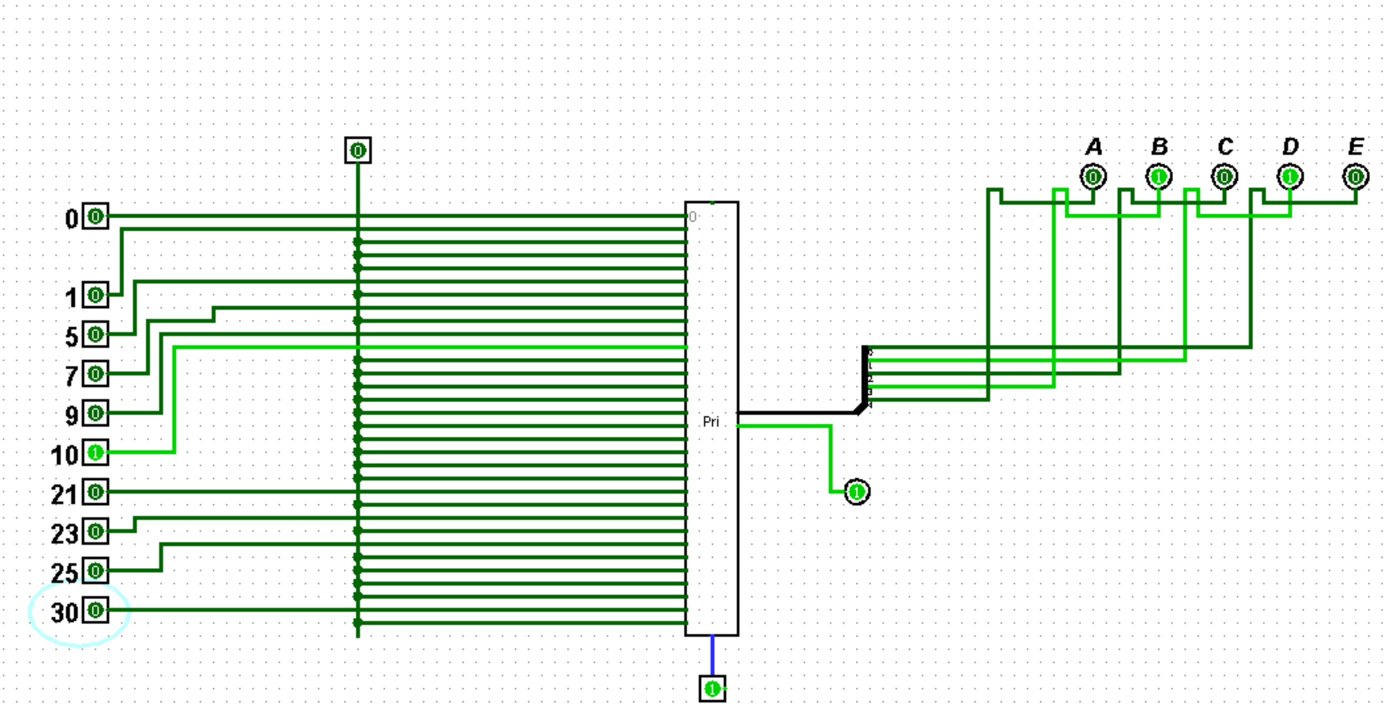
7.2 Encoder

A combinational logic circuit that converts **one active input signal** out of *2^n input lines* into an **n-bit binary output**. It performs the operation of encoding — identifying the position of the active input and generating a corresponding binary code.

A 32 –to-5 Encoder has:

- **32 inputs**:
- **5 outputs**: A, B ,C ,D ,E

$$F = \sum m\ (0,1,5,7,9,10,21,23,25,30)$$



TruthTable of the 32 to 5 Encoder

Input	Output **A**	Output **B**	Output **C**	Output **D**	Output **E**
I_0	0	0	0	0	0
I_1	0	0	0	0	1
I_2	0	0	0	1	0
I_3	0	0	0	1	1
I_4	0	0	1	0	0
I_5	0	0	1	0	1
I_6	0	0	1	1	0
I_7	0	0	1	1	1
I_8	0	1	0	0	0
I_9	0	1	0	0	1
I_10	0	1	0	1	0
I_11	0	1	0	1	1
I_12	0	1	1	0	0
I_13	0	1	1	0	1
I_14	0	1	1	1	0
I_15	0	1	1	1	1
I_16	1	0	0	0	0
I_17	1	0	0	0	1
I_18	1	0	0	1	0
I_19	1	0	0	1	1
I_20	1	0	1	0	0
I_21	1	0	1	0	1
I_22	1	0	1	1	0
I_23	1	0	1	1	1
I_24	1	1	0	0	0
I_25	1	1	0	0	1
I_26	1	1	0	1	0
I_27	1	1	0	1	1
I_28	1	1	1	0	0
I_29	1	1	1	0	1
I_30	1	1	1	1	0
I_31	1	1	1	1	1

8 Implementation of Multiplexer & DeMultiplexer

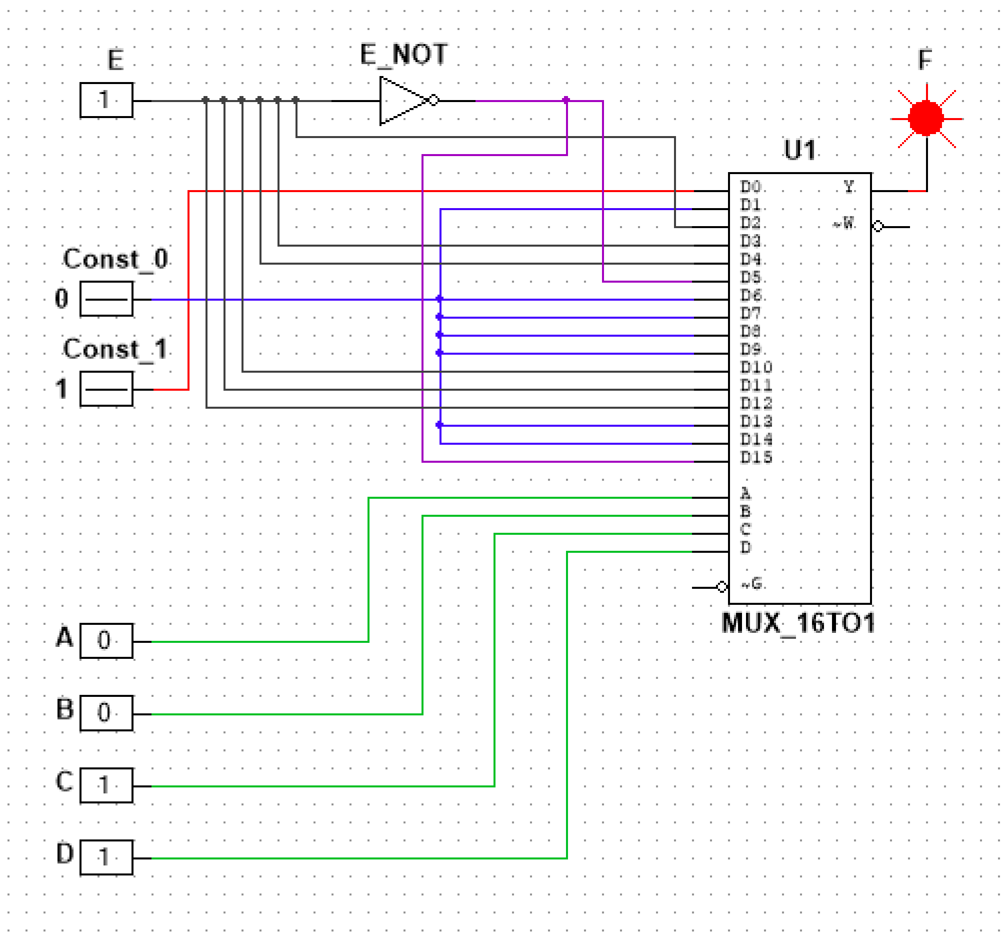
Multiplexer: Or **MUX**, is a **combinational logic circuit** that selects **one input** from **multiple input lines** and forwards it to a **single output line**, based on the values of **select lines** (control inputs).

A multiplexer has **2^n input lines**, **n select lines**, and **1 output**.

$$F = \sum m\,(0,1,5,7,9,10,21,23,25,30)$$

Multiplexer Table:

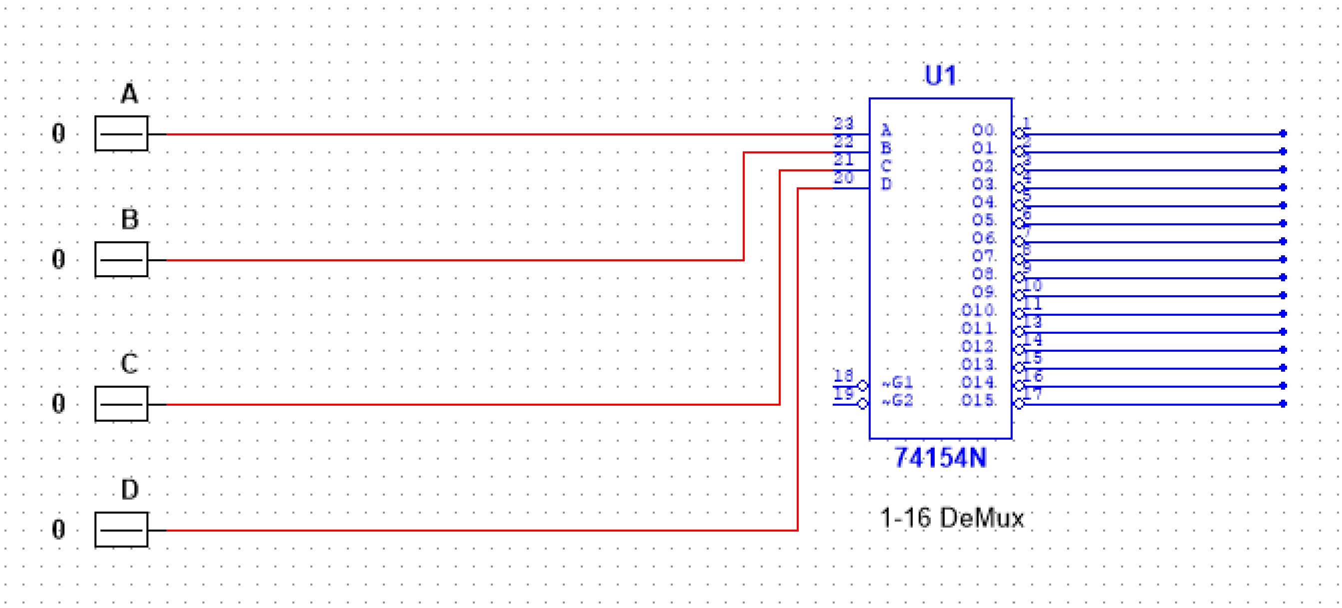
x	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
$\overline{E}$	0	2	4	6	8	10	12	14	16	18	20	22	24	26	28	30
E	1	3	5	7	9	11	13	15	17	19	21	23	25	27	29	31
F_x	1	0	E	E	E	$\overline{E}$	0	0	0	0	E	E	E	0	0	$\overline{E}$



DeMultiplexer: A demultiplexer is like a switch that takes a signal from one source and sends it to one of many destinations. It has only one input but several output.

TruthTable of the 16 to 1 DeMUX

A	B	C	D	F
0	0	0	0	D_0
0	0	0	1	D_1
0	0	1	0	D_2
0	0	1	1	D_3
0	1	0	0	D_4
0	1	0	1	D_5
0	1	1	0	D_6
0	1	1	1	D_7
1	0	0	0	D_8
1	0	0	1	D_9
1	0	1	0	D_{10}
1	0	1	1	D_{11}
1	1	0	0	D_{12}
1	1	0	1	D_{13}
1	1	1	0	D_{14}
1	1	1	1	D_{15}



9 Implementation of PLA

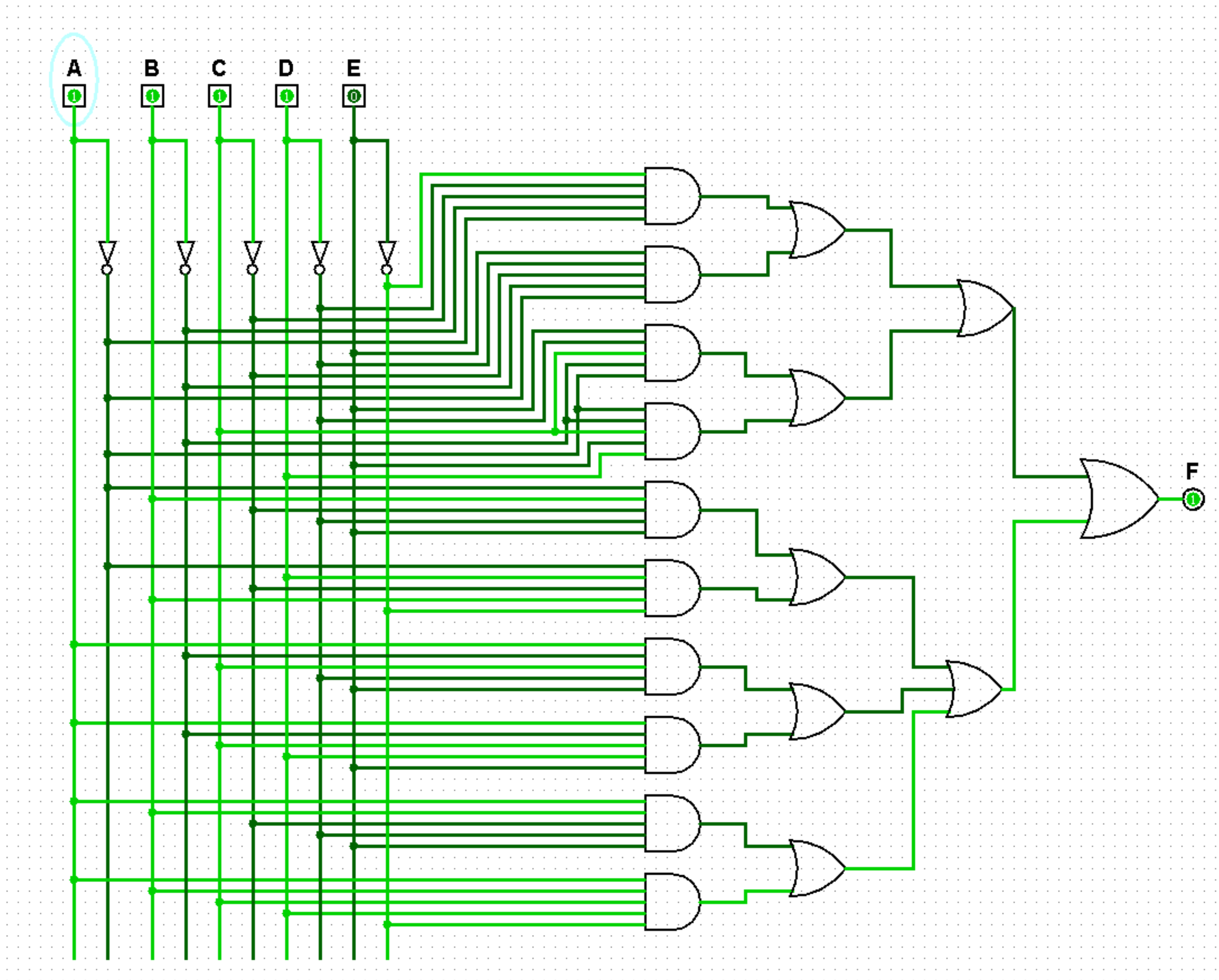
PLA: A programmable logic array (PLA) is a kind of programmable logic device used to implement combinational logic circuits. The PLA has a set of programmable AND gate planes, which link to a set of programmable OR gate planes, which can then be conditionally complemented to produce an output.

Given Function: $F = \sum m\ (0,1,5,7,9,10,21,23,25,30)$

$= m_0 + m_1 + m_5 + m_7 + m_9 + m_{10} + m_{21} + m_{23} + m_{25} + m_{30}$

$$F = \bar{A}\bar{B}\bar{C}\bar{D}\bar{E} + \bar{A}\bar{B}\bar{C}\bar{D}E + \bar{A}\bar{B}C\bar{D}E + \bar{A}\bar{B}CDE + \bar{A}B\bar{C}\bar{D}E + \bar{A}B\bar{C}D\bar{E} + A\bar{B}C\bar{D}E + A\bar{B}CDE + AB\bar{C}\bar{D}E + ABCD\bar{E}$$

PLA Design:



THANK YOU