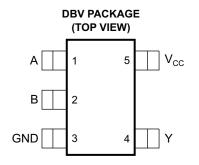


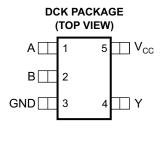
SINGLE 2-INPUT POSITIVE-AND GATE

FEATURES

- Qualified for Automotive Applications
- Supports 5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 3.6 ns at 3.3 V
- Low Power Consumption, 10-μA Max I_{CC}
- ±24-mA Output Drive at 3.3 V
- I_{off} Supports Partial-Power-Down Mode Operation

- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)





See mechanical drawings for dimensions.

DESCRIPTION/ORDERING INFORMATION

The SN74LVC1G08 performs the Boolean function $A \bullet B$ or $Y = \overline{A + B}$ in positive logic.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION(1)

T _A	PACKAG	SE ⁽²⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING ⁽³⁾
–40°C to 125°C	SOT (SOT-23) - DBV	Reel of 3000	SN74LVC1G08QDBVRQ1	C08_
-40 C to 125 C	SOT (SC-70) - DCK	Reel of 3000	SN74LVC1G08QDCKRQ1	CE_
–40°C to 85°C	SOT (SOT-23) - DBV	Reel of 3000	SN74LVC1G08IDBVRQ1	C08_
-40 C to 65 C	SOT (SC-70) - DCK	Reel of 3000	SN74LVC1G08IDCKRQ1	CE_

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
- (3) DBV/DCK: The actual top-side marking has one additional character that designates the wafer fab/assembly site.

FUNCTION TABLE

INP	UTS	OUTPUT
Α	В	Y
Н	Н	Н
L	X	L
Х	L	L



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LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT	
V_{CC}	Supply voltage range		-0.5	6.5	V	
VI	Input voltage range (2)	-0.5	6.5	V		
Vo	Voltage range applied to any output in the high-impeda	-0.5	6.5	V		
Vo	Voltage range applied to any output in the high or low	-0.5	V _{CC} + 0.5	V		
I_{IK}	Input clamp current	V _I < 0		-50	mA	
I _{OK}	Output clamp current	V _O < 0		-50	mA	
Io	Continuous output current			±50	mA	
	Continuous current through V _{CC} or GND			±100	mA	
0	Dealers thermal impedance (4)	DBV package		206		
θ_{JA}	Package thermal impedance (4)	DCK package		252	°C/W	
T _{stg}	Storage temperature range	-65	150	°C		

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

⁽²⁾ The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

⁽³⁾ The value of V_{CC} is provided in the recommended operating conditions table.

⁽⁴⁾ The package thermal impedance is calculated in accordance with JESD 51-7.



Recommended Operating Conditions⁽¹⁾

			MIN	MAX	UNIT	
.,	Complement	Operating	1.65	5.5	V	
V _{CC}	Supply voltage	Data retention only	1.5		V	
		V _{CC} = 1.65 V to 1.95 V	$0.65 \times V_{CC}$			
	I Pale Tarrel Parent college	V _{CC} = 2.3 V to 2.7 V	1.7		.,	
V_{IH}	High-level input voltage	V _{CC} = 3 V to 3.6 V	2		V	
		V _{CC} = 4.5 V to 5.5 V	$0.7 \times V_{CC}$			
		V _{CC} = 1.65 V to 1.95 V		$0.35 \times V_{CC}$		
. ,	Law lawal inner waltana	V _{CC} = 2.3 V to 2.7 V		0.7	V	
V_{IL}	Low-level input voltage	V _{CC} = 3 V to 3.6 V		0.8	V	
		V _{CC} = 4.5 V to 5.5 V		$0.3 \times V_{CC}$		
V _I	Input voltage		0	5.5	V	
Vo	Output voltage		0	V _{CC}	V	
		V _{CC} = 1.65 V		-4		
		V _{CC} = 2.3 V		-8		
I _{OH}	High-level output current	V 2V		-16	mA	
		V _{CC} = 3 V		-24		
		V _{CC} = 4.5 V		-32		
		V _{CC} = 1.65 V		4		
		V _{CC} = 2.3 V		8		
I_{OL}	Low-level output current	V 2.V		16	mA	
		V _{CC} = 3 V		24		
		V _{CC} = 4.5 V		32		
		$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}, 2.5 \text{ V} \pm 0.2 \text{ V}$		20		
Δt/Δν	Input transition rise or fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	10		ns/V	
		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$		5		
т	Operating free air temperature	Q-suffix devices	-40	125	۰,۲	
T_A	Operating free-air temperature	I-suffix devices	-40	85	°C	

⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

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Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST C	ONDITIONS	V _{cc}	MIN T	YP ⁽¹⁾ MAX	UNIT		
	1 100 1	$T_A = -40^{\circ}C \text{ to } 125^{\circ}C$	1.65 V to 5.5 V	V _{CC} - 0.15				
	$I_{OH} = -100 \mu A$	$T_A = -40^{\circ}C$ to $85^{\circ}C$	1.00 V 10 0.0 V	V _{CC} - 0.1				
	$I_{OH} = -4 \text{ mA}$		1.65 V	1.2				
V _{OH}	$I_{OH} = -8 \text{ mA}$		2.3 V	1.9		V		
	I _{OH} = -16 mA		3 V	2.4				
	$I_{OH} = -24 \text{ mA}$		3 V	2.3				
	$I_{OH} = -32 \text{ mA}$		4.5 V	3.8				
	I _{OL} = 100 μA		1.65 V to 5.5 V					
	I _{OL} = 4 mA		1.65 V		0.45	.45		
V	$I_{OL} = 8 \text{ mA}$		2.3 V		V			
V _{OL}	I _{OL} = 16 mA	3 V		V				
	I _{OL} = 24 mA	3 V						
	I _{OL} = 32 mA		4.5 V		0.55			
I _I A or B inputs	V _I = 5.5 V or GND		0 to 5.5 V		±5	μΑ		
I _{off}	V_I or $V_O = 5.5 \text{ V}$		0		±10	μΑ		
I _{CC}	V _I = 5.5 V or GND,	I _O = 0	1.65 V to 5.5 V		10	μΑ		
ΔI _{CC}	One input at V _{CC} – 0.6 V,	Other inputs at V _{CC} or GND	3 V to 5.5 V		500	μΑ		
C _i	$V_I = V_{CC}$ or GND		3.3 V		4	pF		

⁽¹⁾ All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

Switching Characteristics

over recommended operating free-air temperature range, $C_L = 30 \text{ pF}$ or 50 pF (unless otherwise noted) (see Figure 1)

					T _A	= -40°C	to 125°	С			
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = ± 0.1		V _{CC} = ± 0.2		V _{CC} = ± 0.3		V _{CC} = ± 0.5		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	Υ	1	10	1	7.5	1	6.5	1	6	ns

Switching Characteristics

over recommended operating free-air temperature range, $C_L = 30 \text{ pF}$ or 50 pF (unless otherwise noted) (see Figure 1)

				$T_A = -40^{\circ}C$ to $85^{\circ}C$							
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = ± 0.1		V _{CC} = ± 0.2		V _{CC} = ± 0.3		V _{CC} = ± 0.5		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	Υ	2.4	8	1.1	5.5	1	4.5	1	4	ns

Operating Characteristics

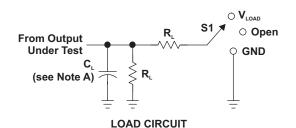
 $T_A = 25^{\circ}C$

	PARAMETER	TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	$V_{CC} = 3.3 \text{ V}$	$V_{CC} = 5 V$	UNIT	
	FARAMETER	TEST CONDITIONS	TYP	TYP	TYP	TYP		
C_{pd}	Power dissipation capacitance	f = 10 MHz	21	24	26	31	pF	

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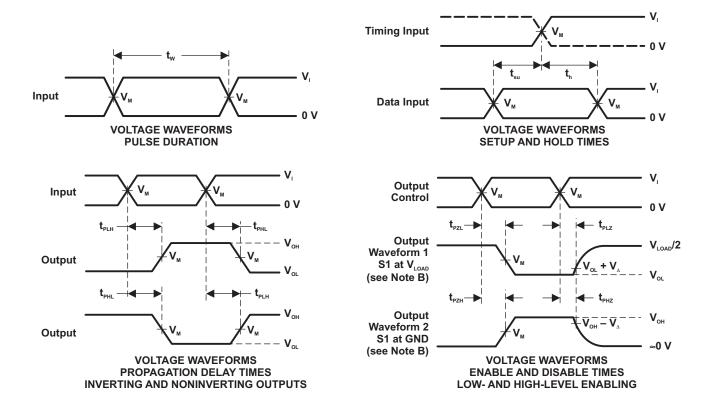


PARAMETER MEASUREMENT INFORMATION



TEST	S1
t _{PLH} /t _{PHL}	Open
t_{PLZ}/t_{PZL}	V _{LOAD}
t _{PHZ} /t _{PZH}	GND

.,	$\begin{array}{ c c c c c }\hline INPUTS & & & & & \\\hline & V_{_{I}} & & t_{_{\!\!\!f}}/t_{_{\!\!f}} & & & & \\\hline \end{array}$			v		-	.,
V _{cc}			C _L	$R_{\scriptscriptstyle L}$	$\mathbf{V}_{_{\Delta}}$		
1.8 V ± 0.15 V	V _{cc}	≤2 ns	V _{cc} /2	2 × V _{cc}	30 pF	1 k Ω	0.15 V
2.5 V ± 0.2 V	V _{cc}	≤2 ns	V _{cc} /2	2 × V _{cc}	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V _{cc}	≤2.5 ns	V _{cc} /2	2 × V _{cc}	50 pF	500 Ω	0.3 V



NOTES: A. C, includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_{o} = 50 Ω .
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and \dot{t}_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. $t_{\mbox{\tiny PLH}}$ and $t_{\mbox{\tiny PHL}}$ are the same as $t_{\mbox{\tiny pd}}.$
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGE OPTION ADDENDUM

www.ti.com 7-Dec-2009

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins F	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74LVC1G08IDCKRQ1	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G08QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G08QDCKRQ1	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN74LVC1G08-Q1:

Catalog: SN74LVC1G08

Enhanced Product: SN74LVC1G08-EP

NOTE: Qualified Version Definitions:

Catalog - TI's standard catalog product

• Enhanced Product - Supports Defense, Aerospace and Medical Applications

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-178 Variation AA.



DBV (R-PDSO-G5)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-203 variation AA.



DCK (R-PDSO-G5)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



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