Stellaris® LM3S9B96 Development Kit

User's Manual

DK-LM3S9B96-04

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CHAPTER 1

Stellaris® LM3S9B96 Development Board Overview

The Stellaris® LM3S9B96 Development Board provides a platform for developing systems around the advanced capabilities of the LM3S9B96 ARM® Cortex™-M3-based microcontroller.

The LM3S9B96 is a member of the Stellaris Tempest-class microcontroller family. Tempest-class devices include capabilities such as 80 MHz clock speeds, an External Peripheral Interface (EPI) and Audio I^2S interfaces. In addition to new hardware to support these features, the DK-LM3S9B96 board includes a rich set of peripherals found on other Stellaris boards.

The development board includes an on-board in-circuit debug interface (ICDI) that supports both JTAG and SWD debugging. A standard ARM 20-pin debug header supports an array of debugging solutions.

The Stellaris® LM3S9B96 Development Kit accelerates development of Tempest-class microcontrollers. The kit also includes extensive example applications and complete source code.

Features

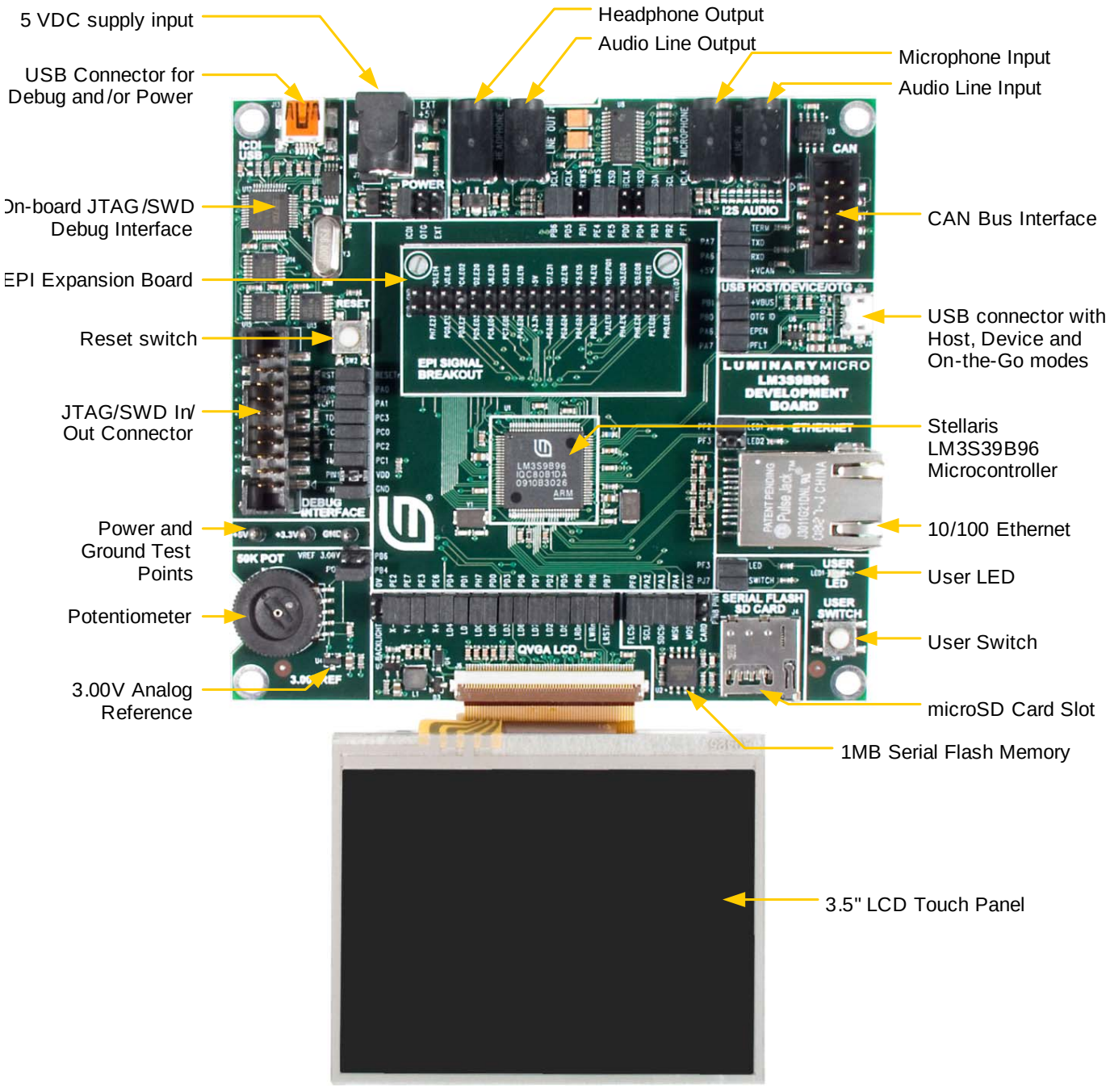
The Stellaris® LM3S9B96 Development Board includes the following features.

- Simple set-up—USB cable provides debugging, communication, and power
- Flexible development platform with a wide range of peripherals
- Color LCD graphics display
  - TFT LCD module with 320 x 240 resolution
  - Resistive touch interface
- 80 MHz LM3S9B96 microcontroller with 256 K Flash, 96 K SRAM, and integrated Ethernet MAC+PHY, USB OTG, and CAN communications
  - – 8 MB SDRAM (plug-in EPI option board)
  - – EPI break-out board (plug-in option board)
- 1 MB serial Flash memory
- Precision 3.00 V voltage reference
- SAFE**RTOS**™ operating system in microcontroller ROM
- I^2S stereo audio codec
  - Line In/Out
  - Headphone Out
  - Microphone In
- Controller Area Network (CAN) Interface
- 10/100 BaseT Ethernet
- USB On-The-Go (OTG) Connector
  - Device, Host, and OTG modes

- User LED and push button
- Thumbwheel potentiometer (can be used for menu navigation)
- MicroSD card slot
- Supports a range of debugging options
  - Integrated In-circuit Debug Interface (ICDI)
  - JTAG, SWD, and SWO all supported
  - Standard ARM® 20-pin JTAG debug connector
- USB Virtual COM Port
- Jumper shunts to conveniently reallocate I/O resources
- Develop using tools supporting Keil™ RealView® Microcontroller Development Kit (MDK-ARM), IAR Embedded Workbench, Code Sourcery GCC development tools, Code Red Technologies development tools, or Texas Instruments' Code Composer Studio™ IDE
- Supported by StellarisWare® software including the graphics library, the USB library, and the peripheral driver library
- An optional Flash and SRAM memory expansion board (DK-LM3S9B96-EXP-FS8) is also available for use with the DK-LM3S9B96 development board
  - Works with the External Peripheral Interface (EPI) of the Stellaris microcontroller
  - Provides Flash memory, SRAM, and an improved performance LCD interface

  For more information on the DK-LM3S9B96-EXP-FS8 memory expansion board, see Appendix E, "Stellaris® LM3S9B96 Flash and SRAM Memory Expansion Board," on page 41. The DK-LM3S9B96-EXP-FS8 memory expansion board is available for purchase separately.

Figure 1-1. DK-LM3S9B96 Development Board



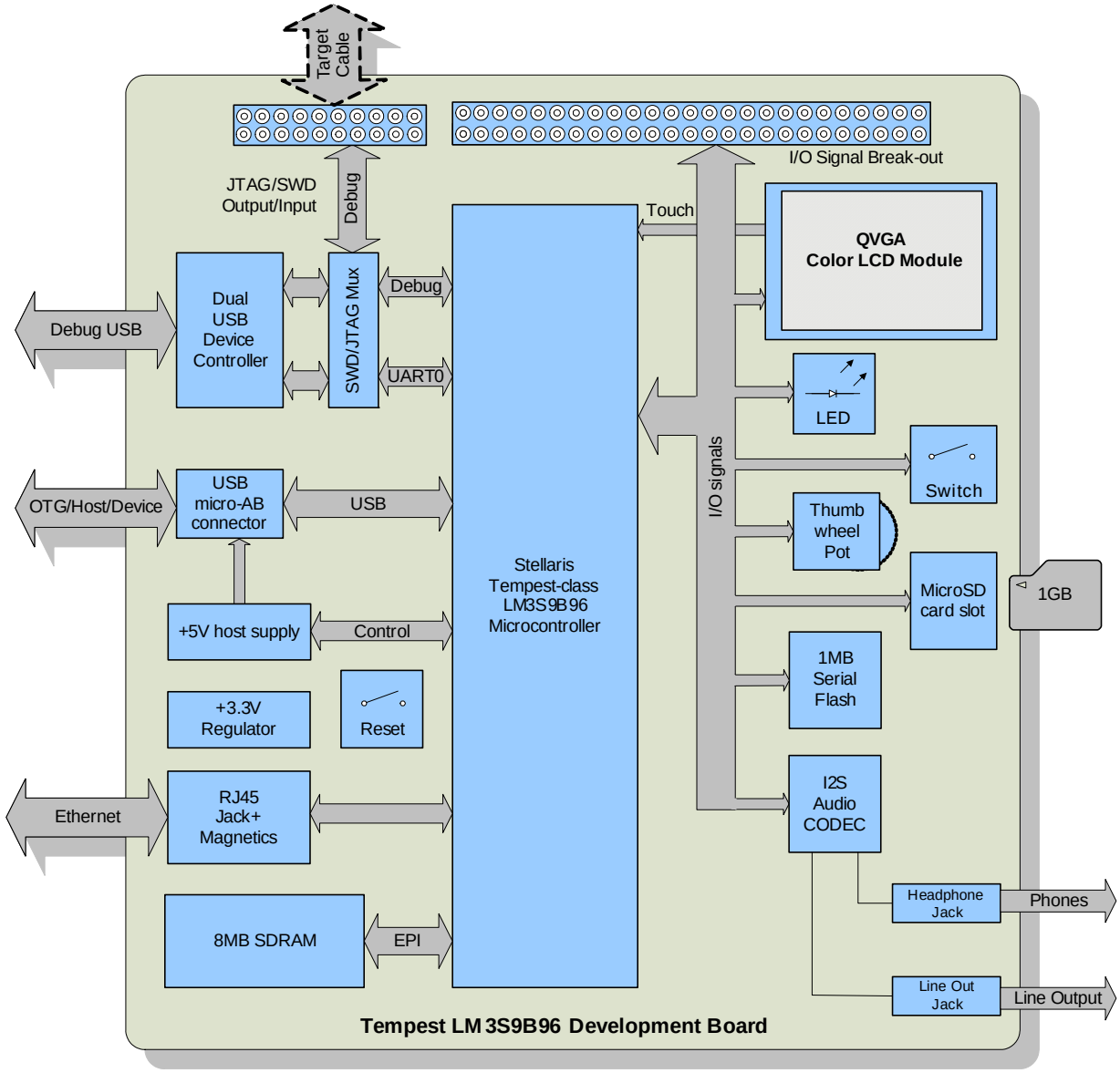
Development Kit Contents

The Stellaris® LM3S9B96 Development Kit contains everything needed to develop and run a range of applications using Stellaris microcontrollers:

- LM3S9B96 development board
- 8 MB SDRAM expansion board
- EPI signal breakout board
- Retractable Ethernet cable
- USB Mini-B cable for debugger use
- USB Micro-B cable for OTG-to-PC connection
- USB Micro-A to USB A adapter for USB Host
- USB Flash memory stick
- microSD Card
- 20-position ribbon cable
- CD containing:
  - A supported version of one of the following (including a toolchain-specific Quickstart guide):
    - Keil™ RealView® Microcontroller Development Kit (MDK-ARM)
    - IAR Embedded Workbench
    - Code Sourcery GCC development tools
    - Code Red Technologies development tools
    - Texas Instruments' Code Composer Studio™ IDE
  - Complete documentation
  - Quickstart application source code
  - Stellaris® Firmware Development Package with example source code

Block Diagram

Figure 1-2. DK-LM3S9B96 Development Board Block Diagram



Development Board Specifications

- Board supply voltage: 4.75–5.25 Vdc from one of the following sources:
  - Debugger (ICDI) USB cable (connected to a PC)
  - USB Micro-B cable (connected to a PC)
  - DC power jack (2.1 x 5.5mm from external power supply)
- Break-out power output: 3.3 Vdc (100 mA max)

- Dimensions (excluding LCD panel):
  - 4.50” x 4.25” x 0.60” (LxWxH) with SDRAM board
  - 4.50” x 4.25” x 0.75” (LxWxH) with EPI breakout board
- Analog Reference: 3.0 V +/-0.2%
- RoHS status: Compliant

NOTE: When the LM3S9B96 Development Board is used in USB Host mode, the host connector is capable of supplying power to the connected USB device. The available supply current is limited to ~200 mA unless the development board is powered from an external 5 V supply with a =600mA rating.

CHAPTER 2

Stellaris® LM3S9B96 Development Board Hardware Description

In addition to an LM3S9B96 microcontroller, the development board includes a range of useful peripheral features and an integrated in-circuit debug interface (ICDI). This chapter describes how these peripherals operate and interface to the microcontroller

LM3S9B96 Microcontroller Overview

The Stellaris LM3S9B96 is an ARM Cortex-M3-based microcontroller with 256-KB flash memory, 80-MHz operation, Ethernet, USB, EPI, SAFE**RTOS**™ in ROM, and a wide range of peripherals. See the *LM3S9B96 Microcontroller Data Sheet* (order number DS-LM3S9B96) for complete microcontroller details.

The LM3S9B96 microcontroller is factory-programmed with a quickstart demo program. The quickstart program resides in on-chip flash memory and runs each time power is applied, unless the quickstart has been replaced with a user program.

Jumpers and GPIO Assignments

Each peripheral circuit on the development board is interfaced to the LM3S9B96 microcontroller through a 0.1” pitch jumper/shunt. Figure 2-1 on page 14 shows the factory default positions of the jumpers. The jumpers must be in these positions for the quickstart demo program to function correctly.

The development board offers capabilities that the LM3S9B96 cannot support simultaneously due to pin count and GPIO multiplexing limitations. For example, as configured, the board does not support SDRAM and I^2S receive (microphone or line input) functions at the same time. The jumpers associated with I^2S receive are omitted in the default configuration.

Table 2-1 lists all features and peripherals that are disconnected in the factory default configuration. Using these peripherals requires that other peripherals be disconnected. Appendix D, “Stellaris® LM3S9B96 Development Board Microcontroller GPIO Assignments,” on page 37 lists alternative jumper configurations used in conjunction with some of the StellarisWare™ example applications for this board.

Table 2-1. Board Features and Peripherals that are Disconnected in Factory Default Configuration

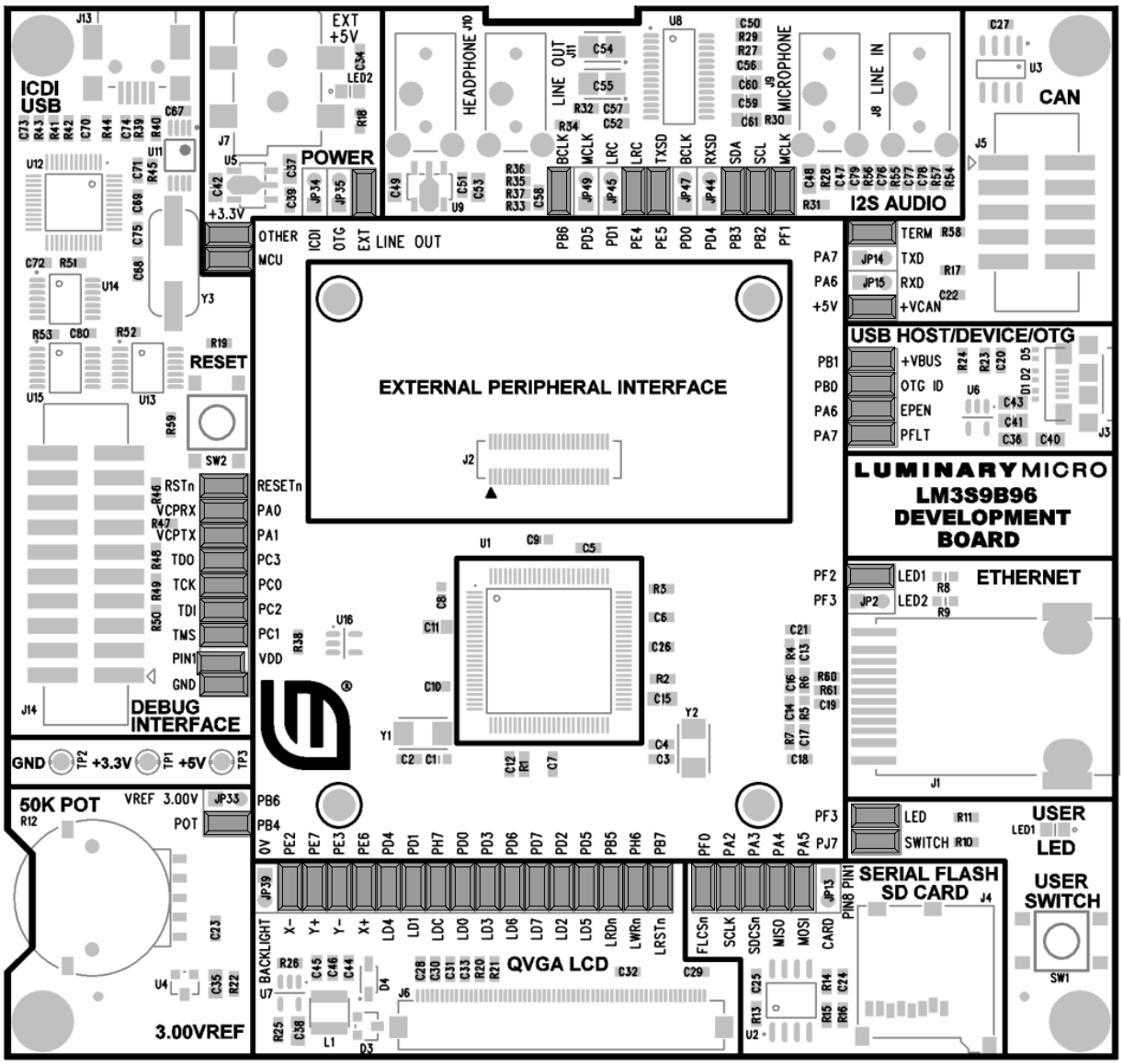
Peripheral	Jumpers
I^2S Receive (Audio Input)	JP44, 45, 47, 49
Controller Area Network (CAN)	JP14, 15
Ethernet Yellow Status LED (LED2)	JP2
Analog 3.0V Reference	JP33

See Appendix D, “Stellaris® LM3S9B96 Development Board Microcontroller GPIO Assignments,” on page 37, for a complete list of GPIO assignments. The table lists all default and alternate

assignments that are supported by the 0.1” jumpers and PCB routing. The LM3S9B96 has additional internal multiplexing that enables additional configurations which may require discrete wiring between peripherals and GPIO pins.

The ICDI section of the board has a GND-GND jumper that serves no function other than to provide a convenient place to ‘park’ a spare jumper. This jumper may be reused as required.

Figure 2-1. Factory Default Jumper Settings



Clocking

The development board uses a 16.0-MHz (Y2) crystal to complete the LM3S9B96 microcontroller's main internal clock circuit. An internal PLL, configured in software, multiples this clock to higher frequencies for core and peripheral timing.

A 25.0-MHz (Y1) crystal provides an accurate timebase for the Ethernet PHY.

Reset

The RESETn signal into the LM3S9B96 microcontroller connects to the reset switch (SW2) and to the ICDI circuit for a debugger-controlled reset.

External reset is asserted (active low) under any one of the three following conditions:

- Power-on reset (filtered by an R-C network)
- Reset push switch SW2 held down
- By the ICDI circuit (U12 FT2232, U13D 74LVC125A) when instructed by the debugger (this capability is optional, and may not be supported by all debuggers)

The LCD module has special Reset timing requirements requiring a dedicated control line from the microcontroller.

Power Supplies

The development board requires a regulated 5.0 V power source. Jumpers JP34-36 select the power source, with the default source being the ICDI USB connector. Only one +5 V source should be selected at any time to avoid conflict between the power sources.

When using USB in Host mode, the power source should be set to either ICDI or to EXT if a +5 V power supply (not included in the kit) is available.

The development board has two main power rails. A +3.3 V supply powers the microcontroller and most other circuitry. +5 V is used by the OTG USB port and In-circuit Debug Interface (ICDI) USB controller. A low drop-out (LDO) regulator (U5) converts the +5 V power rail to +3.3 V. Both rails are routed to test loops for easy access.

USB

The LM3S9B96's full-speed USB controller supports On-the-Go, Host, and Device configurations. See Table 2-2 for USB-related signals. The 5-pin microAB OTG connector supports all three interfaces in conjunction with the cables included in the kit.

The USB port has additional ESD protection diode arrays (D1, D2,D5) for up to 15 kV of ESD protection.

Table 2-2. USB-Related Signals

Microcontroller Pin	Board Function	Jumper Name
Pin 70 USB0DM	USB Data-	-
Pin 71 USB0DP	USB Data+	-
Pin 73 USB0RBIAS	USB bias resistor	-
Pin 66 USB0ID	OTG ID signal (input to microcontroller)	OTG ID
Pin 67 USB0VBUS	Vbus Level monitoring	+VBUS
Pin 34 USB0EPE	Host power enable (active high)	EPEN
Pin 35 USB0PFLT	Host power fault signal (active low)	PFLT

U6, a fault-protected switch, controls and monitors power to the USB host port. USB0EPEN, the control signal from the microcontroller, has a pull-down resistor to ensure host-port power remains off during reset. The power switch will immediately cut power if the attached USB device draws

more than 1 Amp, or if the switches' thermal limits are exceeded by a device drawing more than 500 mA. USB0PFLT indicates the over-current status back to the microcontroller.

The development board can be either a bus-powered USB device or self-powered USB device depending on the power-supply configuration jumpers.

When using the development board in USB-host mode, power to the EVB should be supplied by the In-circuit Debugger (ICDI) USB cable or by a +5 V source connected to the DC power jack.

Note that the LM3S9B96's USB capabilities are completely independent from the In-Circuit Debug Interface USB functionality.

Debugging

Stellaris microcontrollers support programming and debugging using either JTAG or SWD. JTAG uses the TCK, TMS, TDI, and TDO signals. SWD requires fewer signals (SWCLK, SWDIO, and, optionally, SWO for trace). The debugger determines which debug protocol is used.

Debugging Modes

The LM3S9B96 development board supports a range of hardware debugging configurations. Table 2-3 summarizes these configurations.

Table 2-3. Hardware Debugging Configurations

Mode	Debug Function	Use	Selected by...
1	Internal ICDI	Debug on-board LM3S9B96 microcontroller over Debug USB interface.	Default mode
2	ICDI out to JTAG/ SWD header	The development board is used as a USB to SWD/ JTAG interface to an external target.	Remove jumpers on TCk, TMS, TDI, TDO, and PIN1
3	In from JTAG/SWD header	For users who prefer an external debug interface (ULINK, JLINK, etc.) with the development board.	Connecting an external debugger to the JTAG/SWD header

Debug In Considerations

Debug Mode 3 supports board debugging using an external debug interface such as a Segger J-Link or Keil ULINK. Most debuggers use Pin 1 of the Debug connector to sense the target voltage and, in some cases, power the output logic circuit. Installing the VDD/PIN1 jumper will apply 3.3 V power to this pin in order to support external debuggers.

Debug USB Overview

An FT2232 device from Future Technology Devices International Ltd implements USB-to-serial conversion. The FT2232 is factory-configured to implement a JTAG/SWD port (synchronous serial) on channel A and a Virtual COM Port (VCP) on channel B. This feature allows two simultaneous communications links between the host computer and the target device using a single USB cable. Separate Windows drivers for each function are provided on the Documentation and Software CD.

The In-Circuit Debug Interface USB capabilities are completely independent from the LM3S9B96's on-chip USB functionality.

A small serial EEPROM holds the FT2232 configuration data. The EEPROM is not accessible by the LM3S9B96 microcontroller. For full details on FT2232 operation, go to www.ftdichip.com.

USB to JTAG/SWD

The FT2232 USB device performs JTAG/SWD serial operations under the control of the debugger. A simple logic circuit multiplexes SWD and JTAG functions and, when working in SWD mode, provides direction control for the bidirectional data line.

Virtual COM Port

The Virtual COM Port (VCP) allows Windows applications (such as HyperTerminal) to communicate with UART0 on the LM3S9B96 over USB. Once the FT2232 VCP driver is installed, Windows assigns a COM port number to the VCP channel. Table 2-4 shows the debug-related signals.

Table 2-4. Debug-Related Signals

Microcontroller Pin	Board Function	Jumper Name
Pin 77 TDO/SWO	JTAG data out or trace data out	TDO
Pin 78 TDI	JTAG data in	TDI
Pin 79 TMS/SWDIO	JTAG TMS or SWD data in/out	TMS
Pin 80 TCK/SWCLK	JTAG Clock or SWD clock	TCK
Pin 26 PA0/U0RX	Virtual Com port data to LM3S9B96	VCPRX
Pin 27 PA1/U0TX	Virtual Com port data from LM3S9B96	VCPTX
Pin 64 RSTn	System Reset	RSTn

Serial Wire Out (SWO)

The development board supports the Cortex-M3 Serial-Wire Output (SWO) trace capabilities. Under debugger control, on-board logic can route the SWO datastream to the VCP transmit channel. The debugger software can then decode and interpret the trace information received from the Virtual Com Port. The normal VCP connection to UART0 is interrupted when using SWO. Not all debuggers support SWO.

See the *Stellaris LM3S9B96 Microcontroller Data Sheet* for additional information on the Trace Port Interface Unit (TPIU).

Color QVGA LCD Touch Panel

The development board features a TFT Liquid Crystal graphics display with 320 x 240 pixel resolution. The display is protected during shipping by a thin, protective plastic film which should be removed before use.

Features

Features of the LCD module include:

- Kitronix K350QVG-V1-F display
- 320 x RGB x 240 dots
- 3.5" 262 K colors

- Wide temperature range
- White LED backlight
- Integrated RAM
- Resistive touch panel

Control Interface

The Color LCD module has a built-in controller IC with a multi-mode parallel interface. The development board uses an 8-bit 8080 type interface with GPIO Port D providing the data bus. Table 2-4 shows the LCD-related signals.

Table 2-5. LCD-Related Signals

Microcontroller Pin	Board Function	Jumper Name
PE6/ADC1	Touch X+	X+
PE3	Touch Y-	Y-
PE2	Touch X-	X-
PE7/ADC0	Touch Y+	Y+
PB7	LCD Reset	LRSTn
PD0..7	LCD Data Bus 0..7	LD0..7
PH7	LCD Data/Control Select	LDC
PB5	LCD Read Strobe	LRDn
PH6	LCD Write Strobe	LWRn
-	Backlight control	BLON

Backlight

The white LED backlight must be powered for the display to be clearly visible. U7 (FAN5331B) implements a 20 mA constant-current LED power source to the backlight. The backlight is not normally controlled by the microcontroller, however, the control signal is available on a header. A jumper may be installed to disable the backlight by connecting it to GND. Alternatively, a wire may be used to control this signal from a spare microcontroller GPIO line.

Because the FAN5331B operates in a constant current mode, its output voltage will jump up if the LCD should become disconnected. To prevent over-voltage failure of the IC or diode D3, a zener (D4) clamps the voltage. The current will limit to 20 mA, but the total board current will be higher than when the LCD panel is connected. To avoid over-heating the backlighting circuit, install the BLON jumper to completely shut-down the backlighting circuit.

Power

The LCD module has internal bias voltage generators and requires only a single 3.3 V dc supply.

Resistive Touch Panel

The 4-wire resistive touch panel interfaces directly to the microcontroller, using 2 ADC channels and 2 GPIO signals. See the StellarisWare™ source code for additional information on touch panel implementation.

I²S Audio

The LM3S9B96 development board has advanced audio capabilities using an I²S-connected Audio TLV320AIC23 CODEC. The factory default configuration has Audio output (Line Out and/or Headphone output) enabled. Four additional I²S signals are required for Audio input (Line Input and/or Microphone). All four audio interfaces are through 1/8" (3.5mm) stereo jacks. Table 2-6 shows the I²S audio-related signals.

Table 2-6. I²S Audio-Related Signals

Microcontroller Pin	Board Function	Jumper Name
I2C0SDA	CODEC Configuration Data	SDA
I2C0SCL	CODEC Configuration Clock	SCL
I2STXSD	Audio Out Serial Data	TXSD
I2STXWS	Audio Out Framing signal	TXWS
I2STXSCK	Audio Out Bit Clock	BCLK[a]
I2STXMCLK	Audio Out System Clock	MCLK
I2SRXSD	Audio In Serial Data	RXSD[b]
I2SRXWS	Audio In Framing signal	RXWS[b]
I2SRXSCK	Audio In Bit Clock	BCLK[b]
I2SRXMCLK	Audio In System Clock	MCLK[b]

a. Shares GPIO line with Analog voltage reference. Jumper installed by default.
b. Shares GPIO line with LCD data bus – Port D. Jumper omitted by default.

The Audio CODEC has a number of control registers which are configured using the I²C bus signals. CODEC settings can only be written, but not read, using I²C. See the StellarisWare™ example applications for programming information and the TLV320AIX23B data sheet for complete register details.

The Headphone output can be connected directly to any standard headphones. The Line Output is suitable for connection to an external amplifier, including PC desktop speaker sets.

User Switch and LED

The development board provides a user push-switch and LED (see Table 2-7).

Table 2-7. Navigation Switch-Related Signals

Microcontroller Pin	Board Function	Jumper Name
PJ7	User Switch	SWITCH
PF3	User LED	LED[a]

a. Shared with Ethernet Jack Yellow LED. This jumper is installed by default.

CHAPTER 3

Stellaris® LM3S9B96 Development Board External Peripheral Interface (EPI)

The External Peripheral Interface (EPI) is a high-speed 8/16/32-bit parallel bus for connecting external peripherals or memory without glue logic. Supported modes include SDRAM, SRAM, and Flash memories, as well as Host-bus and FIFO modes.

The LM3S9B96 development kit includes an 8 MB SDRAM board in addition to an EPI break-out board. Other EPI expansion boards may be available.

SDRAM Expansion Board

The SDRAM board provides 8 MB of memory (4M x 16) which, once configured, becomes part of the LM3S9B96's memory map at either 0x6000.0000 or 0x8000.0000. The SDRAM interface multiplexes DQ00..14 and AD/BA0..14 without requiring external latches or buffers. Of the 32 EPI signals, only 24 are used in SDRAM mode, with the remaining signals used for non-EPI functions on the board.

Flash and SRAM Memory Expansion Board

The optional Flash and SRAM memory expansion board (DK-LM3S9B96-EXP-FS8) is a plug-in for the DK-LM3S9B96 development board. This expansion board works with the External Peripheral Interface (EPI) of the Stellaris microcontroller and provides Flash memory, SRAM, and an improved performance LCD interface.

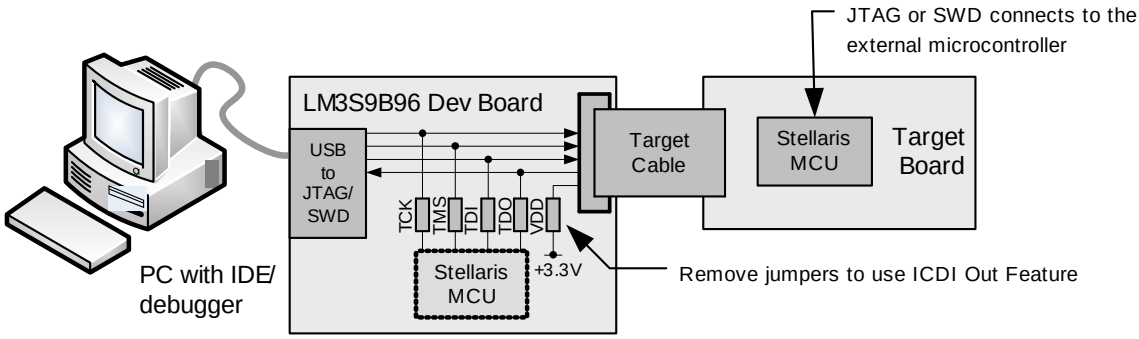
For more information on the DK-LM3S9B96-EXP-FS8 memory expansion board (sold separately), see Appendix E, "Stellaris® LM3S9B96 Flash and SRAM Memory Expansion Board," on page 41.

CHAPTER 4

Using the In-Circuit Debugger Interface

The Stellaris® LM3S9B96 Development Kit can operate as an In-Circuit Debugger Interface (ICDI). ICDI acts as a USB to the JTAG/SWD adaptor, allowing debugging of any external target board that uses a Stellaris microcontroller. See “Debugging Modes” on page 16 for a description of how to enter ICDI Out mode.

Figure 4-1. ICD Interface Out Mode



The debug interface operates in either serial-wire debug (SWD) or JTAG mode, depending on the configuration in the debugger IDE.

The IDE/debugger does not distinguish between the on-board Stellaris microcontroller and an external Stellaris microcontroller. The only requirement is that the correct Stellaris device is selected in the project configuration.

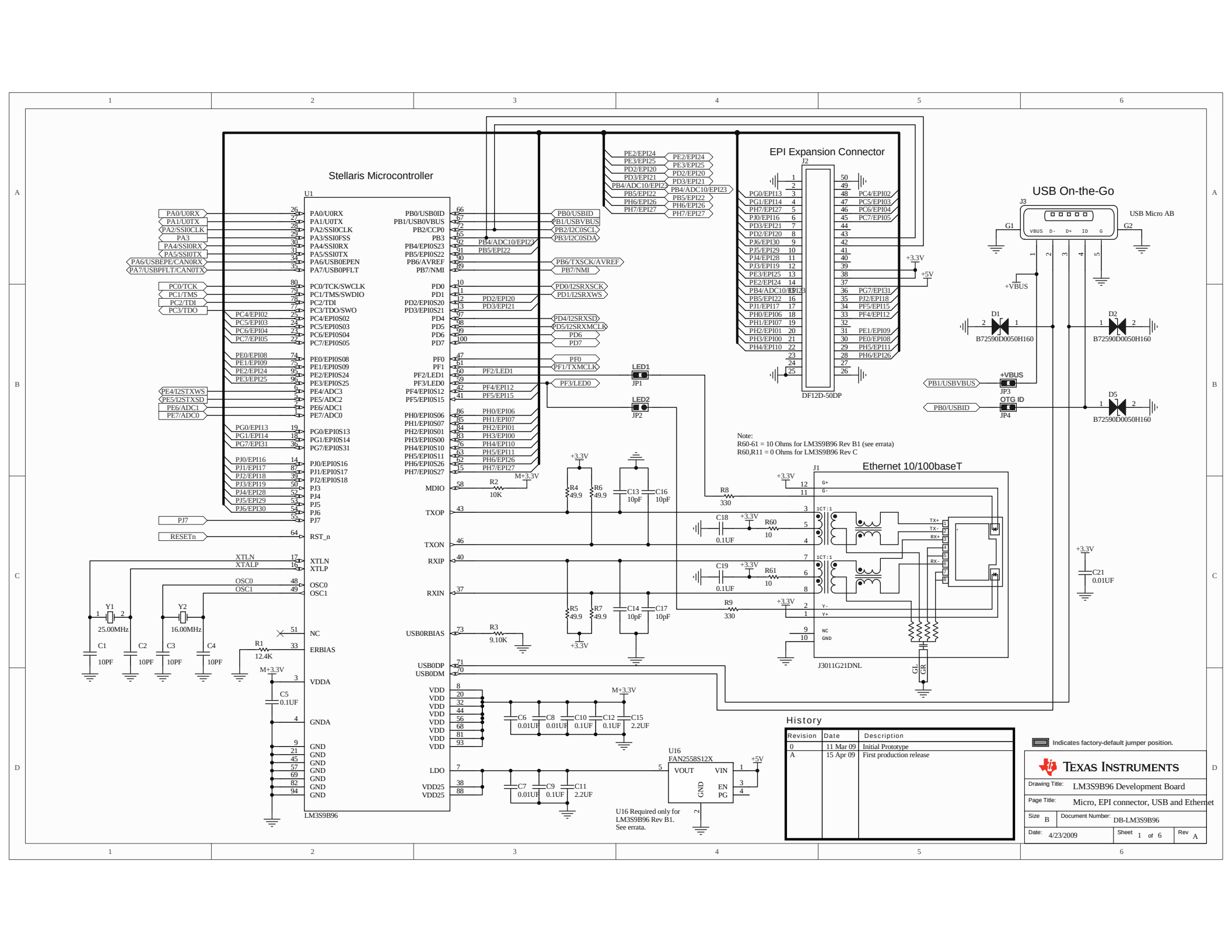
The Stellaris target board should have a 2x10 0.1” pin header with signals as indicated in Table C-1 on page 35. This applies to both an external Stellaris microcontroller target (Debug Output mode) and to external JTAG/SWD debuggers (Debug Input mode).

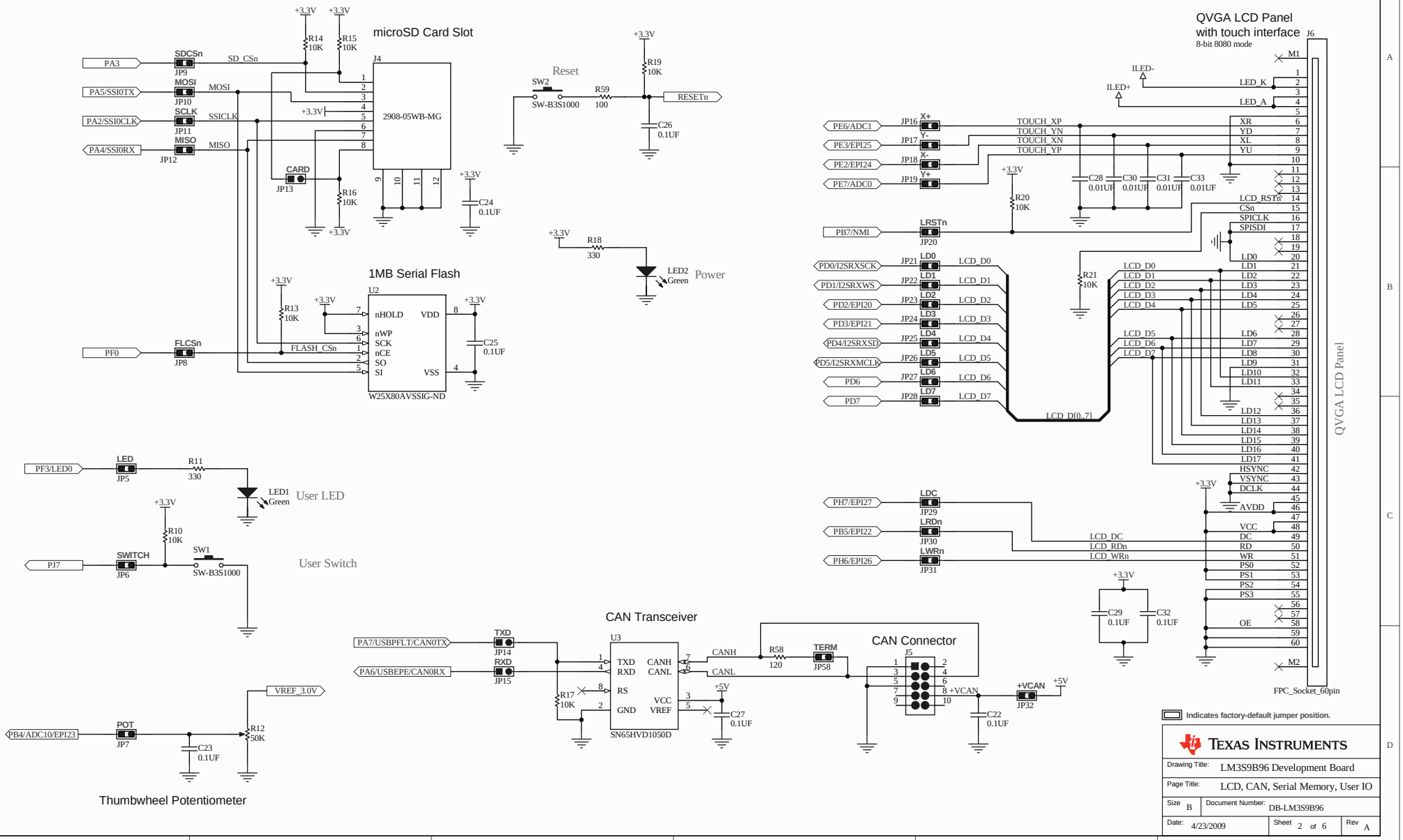
ICDI does not control RST (device reset) or TRST (test reset) signals. Both reset functions are implemented as commands over JTAG/SWD, so these signals are usually not necessary.

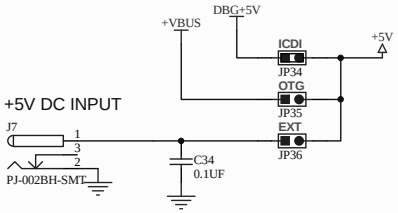
A P P E N D I X A

Stellaris® LM3S9B96 Development Board Schematics

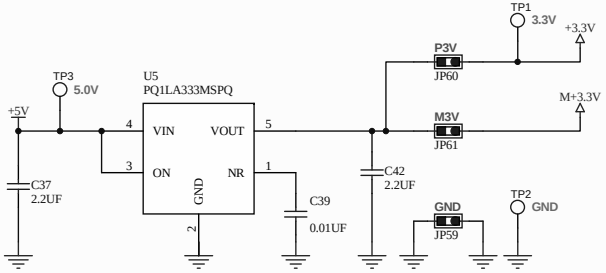
This section contains the schematics for the DK-LM3S9B96 development board.


Stellaris Microcontroller
U1
LM3S9B96
EPI Expansion Connector
J2
DF12D-50DP
USB On-the-Go
J3
USB Micro AB
B72590D0050H160
Ethernet 10/100baseT
J1
J3011G21DNL
LED1
LED2
JP1
JP2
JP3
JP4
OTG ID
+VBUS
Y1
25.00MHz
Y2
16.00MHz
U16
FAN2558S12X
U16 Required only for LM3S9B96 Rev B1. See errata.
Note:
R60-61 = 10 Ohms for LM3S9B96 Rev B1 (see errata)
R60,R11 = 0 Ohms for LM3S9B96 Rev C
History
Revision | Date | Description
0 | 11 Mar 09 | Initial Prototype
A | 15 Apr 09 | First production release
Indicates factory-default jumper position.
TEXAS INSTRUMENTS
Drawing Title: LM3S9B96 Development Board
Page Title: Micro, EPI connector, USB and Ethernet
Size: B
Document Number: DB-LM3S9B96
Date: 4/23/2009
Sheet 1 of 6
Rev A

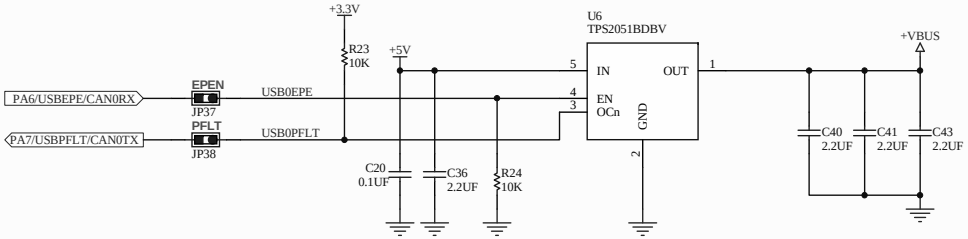

microSD Card Slot
Reset
QVGA LCD Panel
with touch interface
8-bit 8080 mode
1MB Serial Flash
Power
User LED
User Switch
CAN Transceiver
CAN Connector
Thumbwheel Potentiometer
QVGA LCD Panel
FPC_Socket_60pin
Indicates factory-default jumper position.
TEXAS INSTRUMENTS
Drawing Title: LM3S9B96 Development Board
Page Title: LCD, CAN, Serial Memory, User IO
Size B
Document Number: DB-LM3S9B96
Date: 4/23/2009
Sheet 2 of 6
Rev A



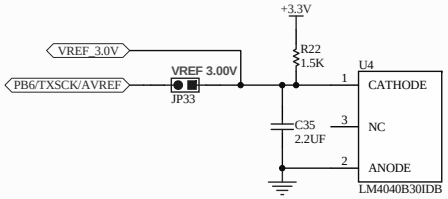
Power Source Selection



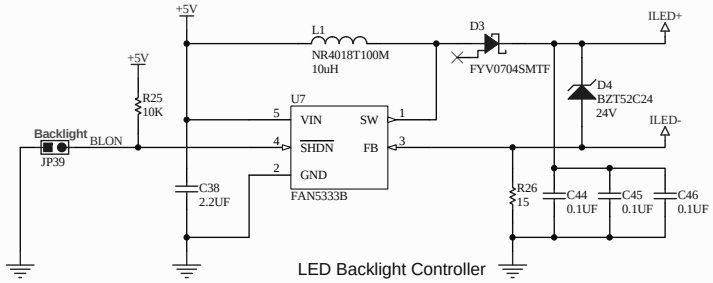
Main +3.3V Supply



VBUS Fault Protected Switch



3.0V 0.2% Voltage Reference

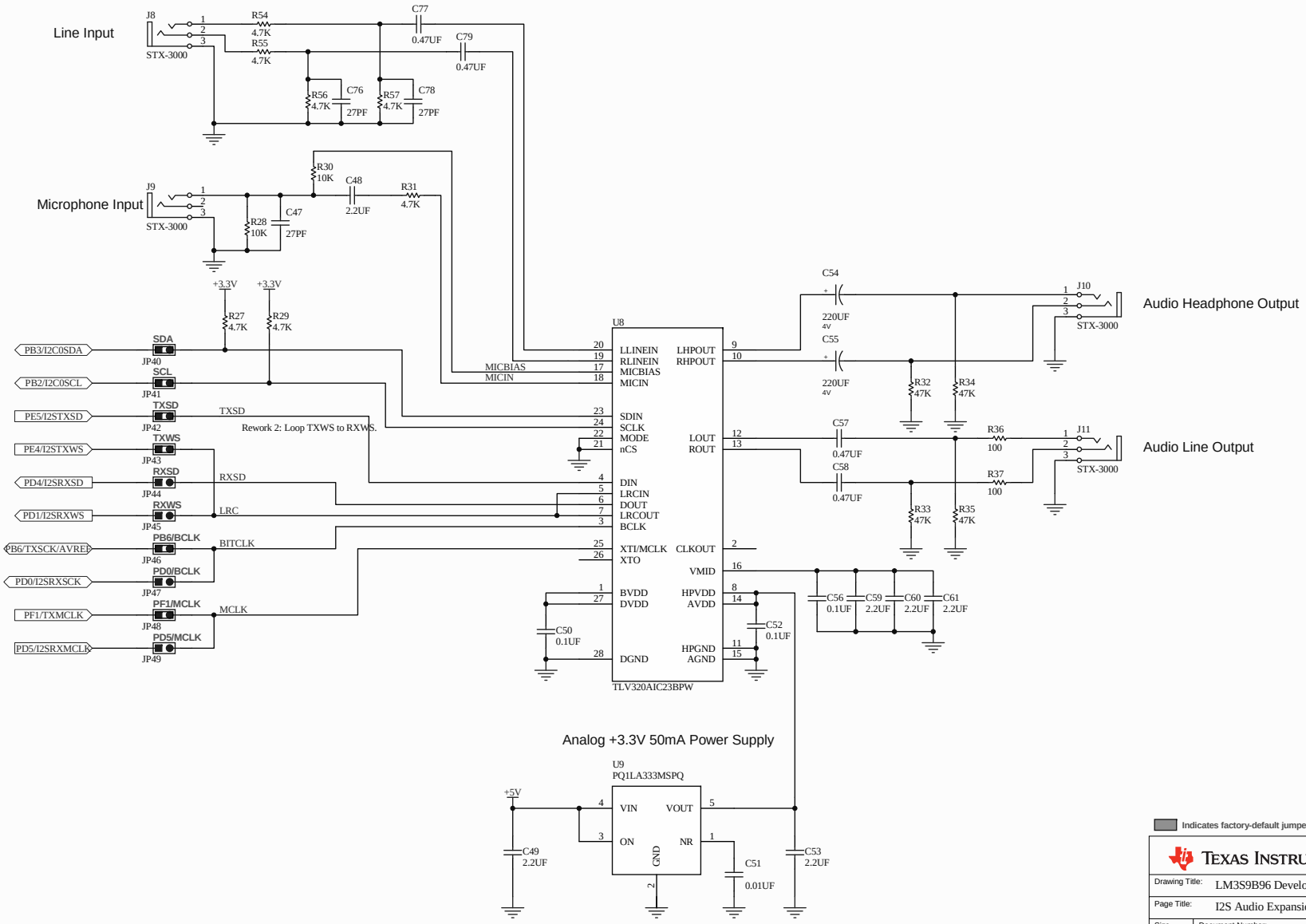


LED Backlight Controller

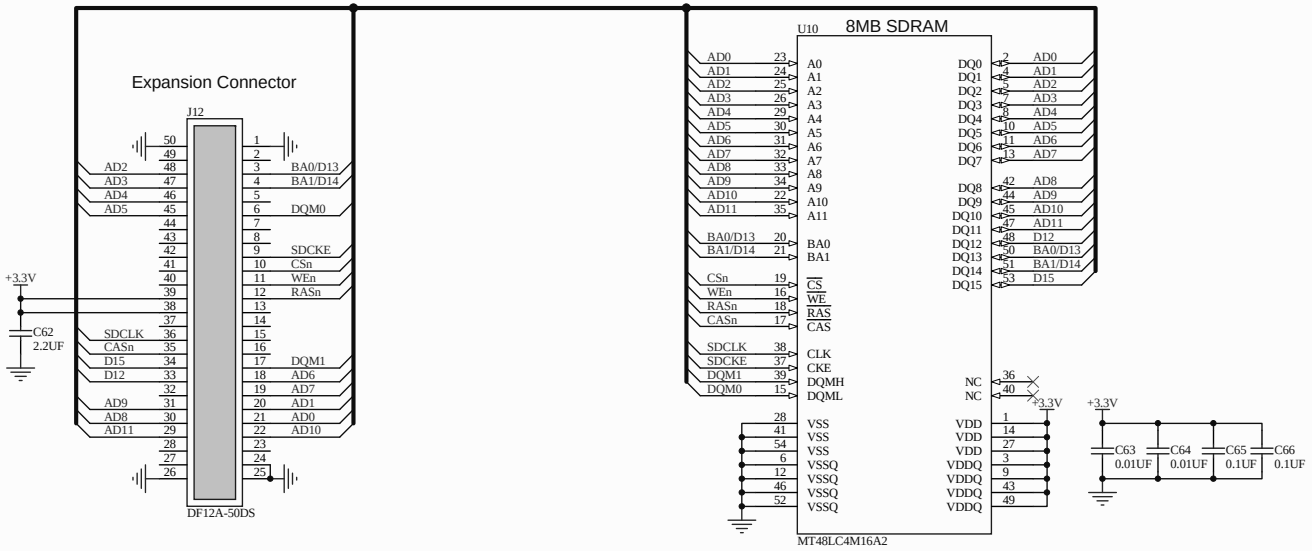
Indicates factory-default jumper position.

TEXAS INSTRUMENTS

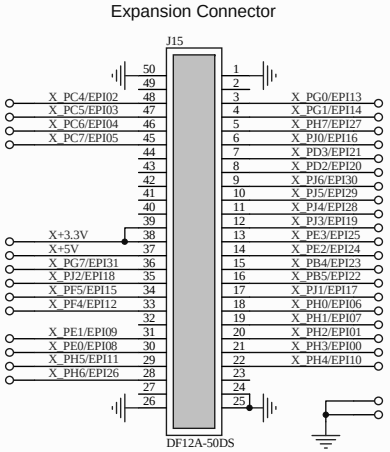
Drawing Title:	LM3S9B96 Development Board
Page Title:	Power Supplies
Size: B	Document Number: DB-LM3S9B96
Date: 4/23/2009	Sheet 3 of 6 — Rev A


Line Input
J8
STX-3000
R54 4.7K
R55 4.7K
C77 0.47UF
C79 0.47UF
R56 4.7K
C76 27PF
R57 4.7K
C78 27PF
Microphone Input
J9
STX-3000
R30 10K
C48 2.2UF
R31 4.7K
R28 10K
C47 27PF
+3.3V
R27 4.7K
R29 4.7K
SDA
SCL
TXSD
TXWS
RXSD
RXWS
PB6/BCLK
PD0/BCLK
PF1/MCLK
PD5/MCLK
JP40
JP41
JP42
JP43
JP44
JP45
JP46
JP47
JP48
JP49
PB3/I2C0SDA
PB2/I2C0SCL
PE5/I2STXSD
PE4/I2STXWS
PD4/I2SRXSD
PD1/I2SRXWS
PB6/TXSCK/AVREF
PD0/I2SRXSCK
PF1/TXMCLK
PD5/I2SRXMCLK
TXSD
Rework 2: Loop TXWS to RXWS.
RXSD
LRC
BITCLK
MCLK
MICBIAS
MICIN
U8
LLINEIN
RLINEIN
MICBIAS
MICIN
SDIN
SCLK
MODE
nCS
DIN
LRCIN
DOUT
LRCOUT
BCLK
XTI/MCLK
XTO
BVDD
DVDD
DGND
LHPOUT
RHPOUT
LOUT
ROUT
CLKOUT
VMID
HPVDD
AVDD
HPGND
AGND
TLV320AIC23BPW
C50 0.1UF
C52 0.1UF
C54 220UF 4V
C55 220UF 4V
C56 0.1UF
C59 2.2UF
C60 2.2UF
C61 2.2UF
R32 47K
R34 47K
R33 47K
R35 47K
C57 0.47UF
C58 0.47UF
R36 100
R37 100
J10
J11
STX-3000
Audio Headphone Output
Audio Line Output
Analog +3.3V 50mA Power Supply
U9
PQ1LA333MSPQ
+5V
VIN
VOUT
ON
NR
GND
C49 2.2UF
C51 0.01UF
C53 2.2UF
Indicates factory-default jumper position.
Texas Instruments
Drawing Title: LM3S9B96 Development Board
Page Title: I2S Audio Expansion Board
Size B
Document Number: DB-LM3S9B96
Date: 4/23/2009
Sheet 4 of 6
Rev A

SDRAM Expansion Board

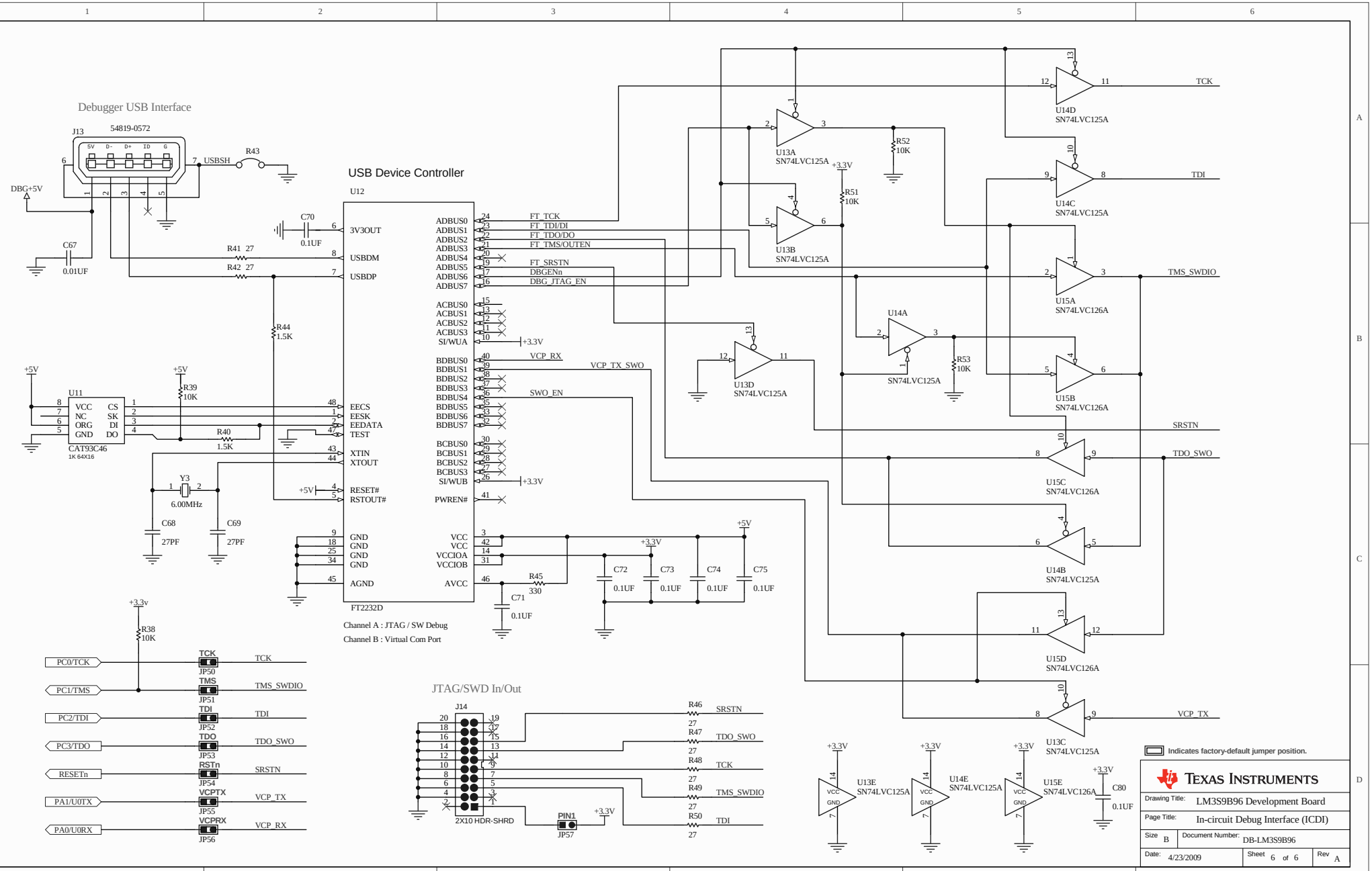


EPI Signal Breakout Board



Drawing Title:	LM3S9B96 Development Board
Page Title:	EPI and SDRAM Expansion Boards
Size: B	Document Number: DB-LM3S9B96
Date: 4/23/2009	Sheet 5 of 6
	Rev A

Texas Instruments


Debugger USB Interface
USB Device Controller
JTAG/SWD In/Out
Channel A : JTAG / SW Debug
Channel B : Virtual Com Port
Indicates factory-default jumper position.
TEXAS INSTRUMENTS
Drawing Title: LM3S9B96 Development Board
Page Title: In-circuit Debug Interface (ICDI)
Size B
Document Number: DB-LM3S9B96
Date: 4/23/2009
Sheet 6 of 6
Rev A

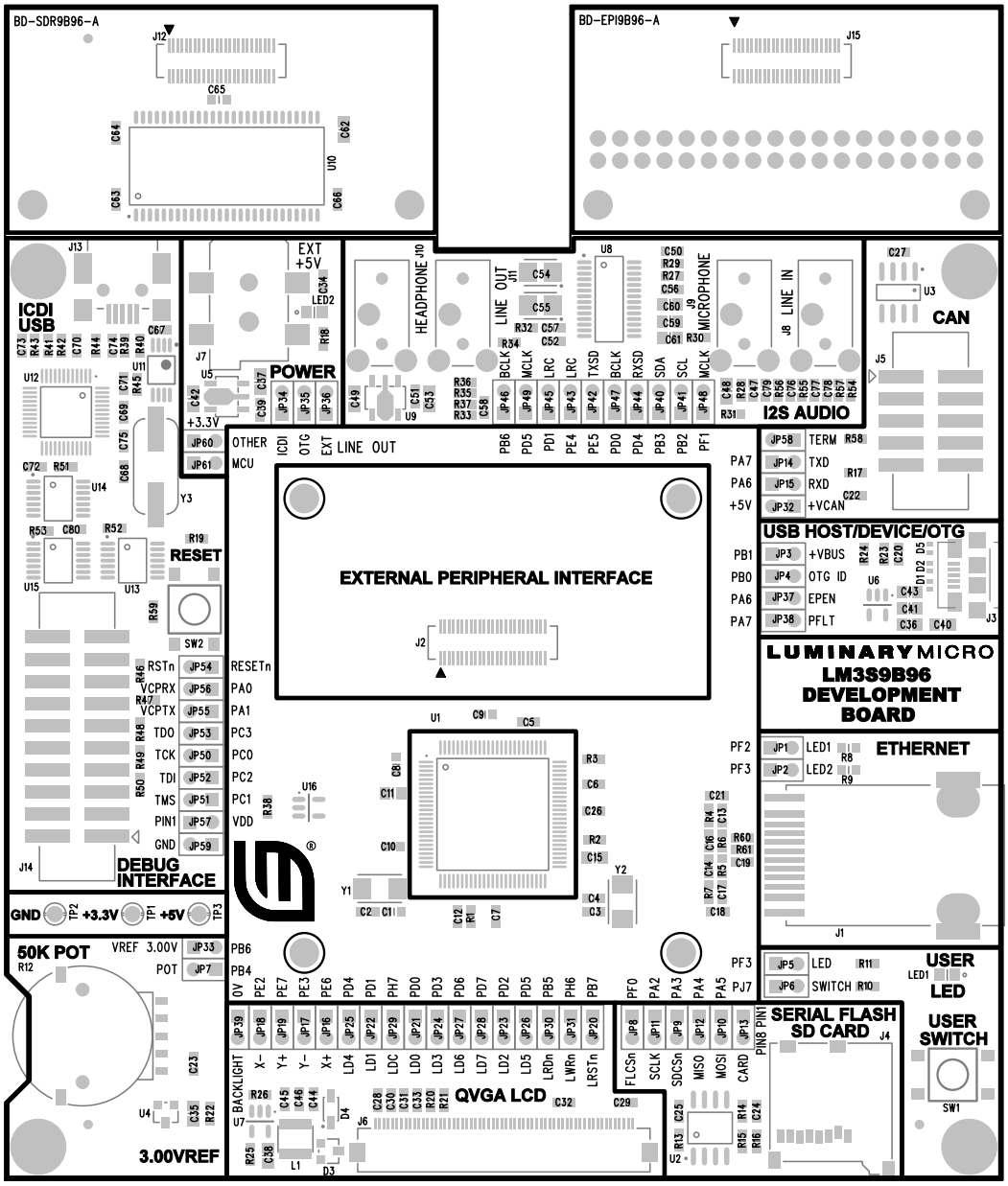
A P P E N D I X B

Stellaris® LM3S9B96 Development Board Component Locations

This appendix contains details on component locations, including:

- Component placement plot for top (Figure B-1)

Figure B-1. Component Placement Plot for Top



A P P E N D I X C

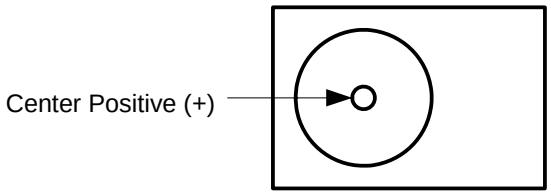
Stellaris® LM3S9B96 Development Board Connection Details

This appendix contains the following sections:

- DC Power Jack (see page 35)
- ARM Target Pinout (see page 35)

DC Power Jack

The EVB provides a DC power jack for connecting an external +5 V regulated (+/-5%) power source.



The socket is 5.5 mm dia with a 2.1 mm pin.

ARM Target Pinout

In ICDI input and output mode, the Stellaris® LM3S9B96 Development Kit supports ARM's standard 20-pin JTAG/SWD configuration. The same pin configuration can be used for debugging over serial-wire debug (SWD) and JTAG interfaces.

Table C-1. Debug Interface Pin Assignments

Function	Pin Number
TDI	5
TDO/SWO	13
TMS/SWDIO	7
TCK/SWCLK	9
System Reset	15
VDD	1
GND	4, 6, 8, 10, 12, 14, 16, 18, 20
No Connect	2, 3, 11, 17, 19

Insert Jumper VDD/PIN1 Jumper (JP57) only when using the development board with an external debug interface such as a ULINK or JLINK.

A P P E N D I X D

Stellaris® LM3S9B96 Development Board Microcontroller GPIO Assignments

Table D-1 shows the pin assignments for the LM3S9B96 microcontroller.

Table D-1. Microcontroller GPIO Assignments

LM3S9B96 GPIO Pin		Development Board Use			
Number	**Description**	**Default Function**	**Default Use**	**Alt. Function**	**Alternate Use**
26	PA0	U0Rx	Virtual Com Port		
27	PA1	U0Tx	Virtual Com Port		
28	PA2	SSI0Clk	SPI		
29	PA3	SSI0Fss	SD Card CSn		
30	PA4	SSI0Rx	SPI		
31	PA5	SSI0Tx	SPI		
34	PA6	USB0EPEN	USB Pwr Enable	CAN0RX	
35	PA7	USB0PFLT	USB Pwr Fault	CAN0TX	
66	PB0	USB0ID	USB OTG ID		
67	PB1	USB0VBUS	USB Vbus		
72	PB2	I2C0SCL	Audio I2C		
65	PB3	I2C0SDA	Audio I2C		
92	PB4	ADC10	Potentiometer	EPI0S23	EPI Breakout
91	PB5	PB5	LCD RDn	EPI0S22	EPI Breakout
90	PB6	PB6	I2STXSCK	AVREF	Ext Volt Ref
89	PB7	PB7	LCD RST		
80	PC0	TCK/SWCLK	JTAG		
79	PC1	TMS/SWDIO	JTAG		
78	PC2	TDI	JTAG		
77	PC3	TDO/SWO	JTAG		
25	PC4	EPI0S2	SDRAM D02		EPI0S02
24	PC5	EPI0S3	SDRAM D03		EPI0S03
23	PC6	EPI0S4	SDRAM D04		EPI0S04
22	PC7	EPI0S5	SDRAM D05		EPI0S05

Table D-1. Microcontroller GPIO Assignments (Continued)

LM3S9B96 GPIO Pin		Development Board Use			
Number	**Description**	**Default Function**	**Default Use**	**Alt. Function**	**Alternate Use**
10	PD0	PD0	LCD Data 0	I2SRXSCK	I2S Audio In
11	PD1	PD1	LCD Data 1	I2S0RXWS	I2S Audio In
12	PD2	PD2	LCD Data 2	EPI0S20	EPI Breakout
13	PD3	PD3	LCD Data 3	EPI0S21	EPI Breakout
97	PD4	PD4	LCD Data 4	I2SRXSD	I2S Audio In
98	PD5	PD5	LCD Data 5	I2SRXMCLK	I2S Audio In
99	PD6	PD6	LCD Data 6		
100	PD7	PD7	LCD Data 7		
74	PE0	EPI0S8	SDRAM D8		EPI0S08
75	PE1	EPI0S9	SDRAM D9		EPI0S09
95	PE2	PE2	Touch XN		EPI0S24
96	PE3	PE3	Touch YN		EPI0S25
6	PE4	I2STXWS	I2S Audio Out		
5	PE5	I2STXSD	I2S Audio Out		
2	PE6	ADC1	ADC Touch XP		
1	PE7	ADC0	ADC Touch YP		
47	PF0	PF0	Flash CSn		
61	PF1	I2STXMCLK	I2S Audio Out		
60	PF2	LED1	Green Enet LED		
59	PF3	PF3	User LED	LED0	Yw Enet LED
42	PF4	EPI0S12	SDRAM D12		
41	PF5	EPI0S15	SDRAM D15		
19	PG0	EPI0S13	SDRAM D13		
18	PG1	EPI0S14	SDRAM D14		
36	PG7	EPI0S31	SDRAM CLK		
86	PH0	EPI0S06	SDRAM D06		
85	PH1	EPI0S07	SDRAM D07		
84	PH2	EPI0S01	SDRAM D01		
83	PH3	EPI0S00	SDRAM D00		
76	PH4	EPI0S10	SDRAM D10		

Table D-1. Microcontroller GPIO Assignments (Continued)

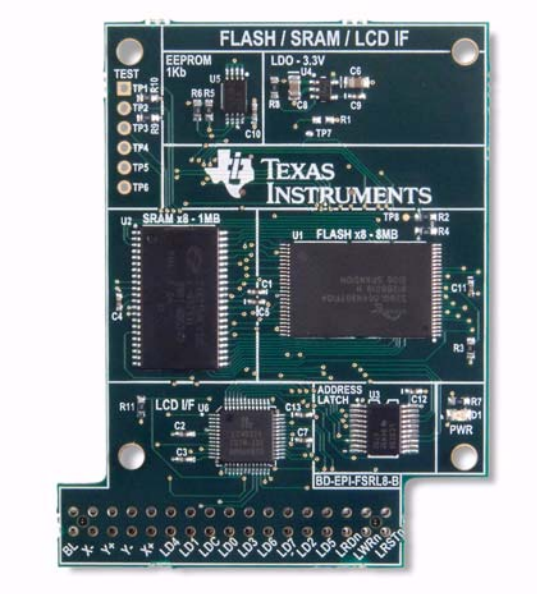
LM3S9B96 GPIO Pin		Development Board Use			
Number	**Description**	**Default Function**	**Default Use**	**Alt. Function**	**Alternate Use**
63	PH5	EPI0S11	SDRAM D11		
62	PH6	EPI0S26	LCD_WRn	EPI0S26	EPI Breakout
15	PH7	EPI0S27	LCD_DC	EPI0S27	EPI Breakout
14	PJ0	EPI0S16	SDRAM DQM		
87	PJ1	EPI0S17	SDRAM DQM		
39	PJ2	EPI0S18	SDRAM CAS		
50	PJ3	EPI0S19	SDRAM RAS		
52	PJ4	EPI0S28	SDRAM WEn		
53	PJ5	EPI0S29	SDRAM CSn		
54	PJ6	EPI0S30	SDRAM SDCKE		
55	PJ7	PJ7	User Switch		

A P P E N D I X E

Stellaris® LM3S9B96 Flash and SRAM Memory Expansion Board

This document describes the Flash and SRAM memory expansion board (DK-LM3S9B96-EXP-FS8) plug-in for the DK-LM3S9B96 development board. This expansion board works with the External Peripheral Interface (EPI) port of the Stellaris microcontroller and provides Flash memory, SRAM, and an improved performance LCD interface.

Figure E-1. DK-LM3S9B96-EXP-FS8 Board Image

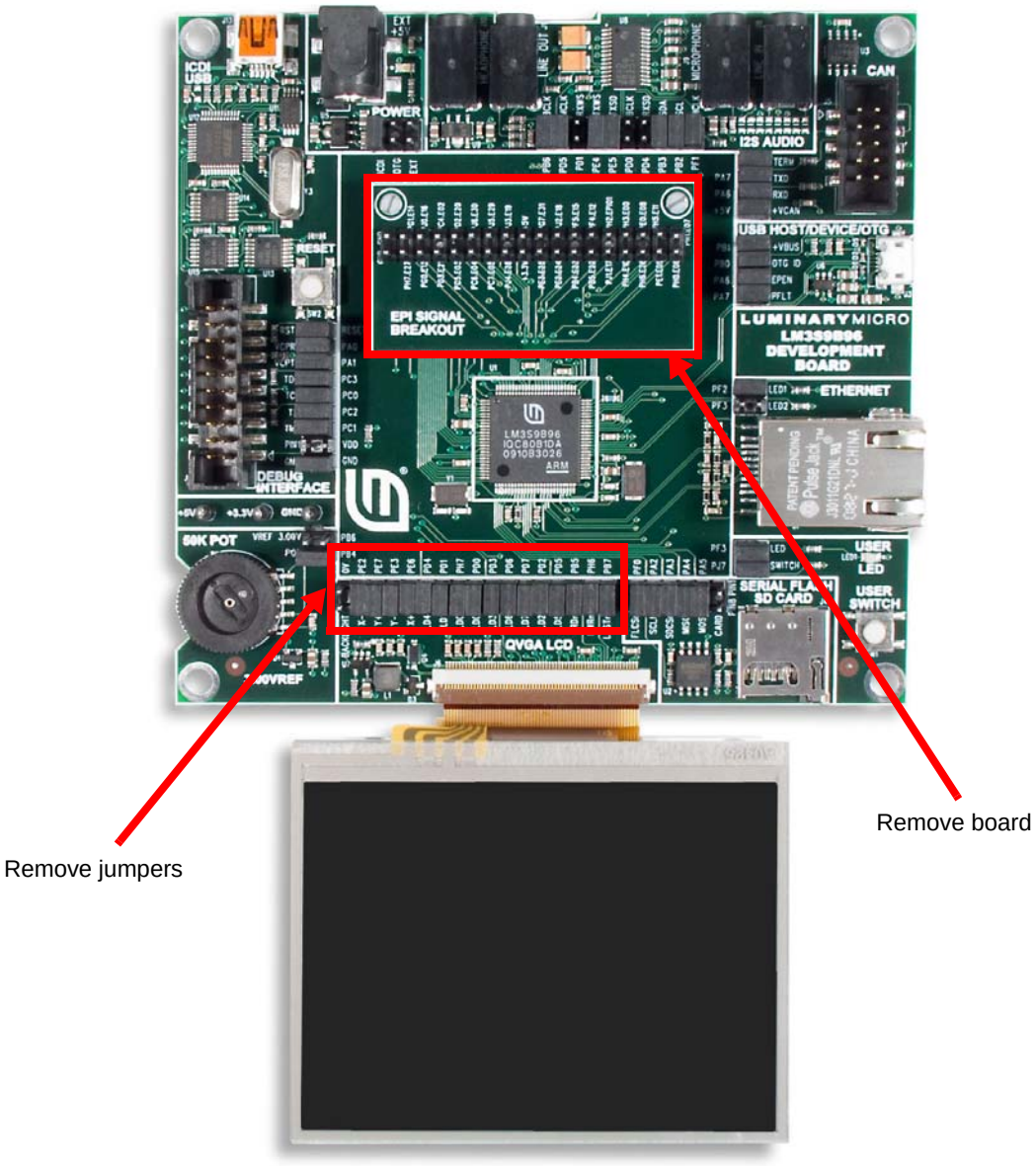


Installation

To install the expansion board on the DK-LM3S9B96 development board, do the following:

1. Remove the DK-LM3S9B96-EXP-FS8 memory expansion board from the antistatic bag.
2. On the DK-LM3S9B96 board, remove any installed board on EPI connector J2.
3. On the DK-LM3S9B96 board remove the shunt jumpers on JP16-JP31 and the JP39 headers as shown in Figure E-1 on page 41.

Figure E-2. DK-LM3S9B96 Development Board



4. Install the two snap-in nylon standoffs on mounting holes above the EPI connector J2.
5. Place the expansion board on top of the DK-LM3S9B96 board and align the standoffs, the EPI connector, and the 2x17 J2 header.
6. Press firmly downward until the board snaps in, then verify that the board is firmly seated on the EPI connector, the 2x17 header, and the standoffs.
7. When powering up the board, verify that the power indicator LED D1 is lit.

Features

The DK-LM3S9B96-EXP-FS8 memory expansion board has the following features:

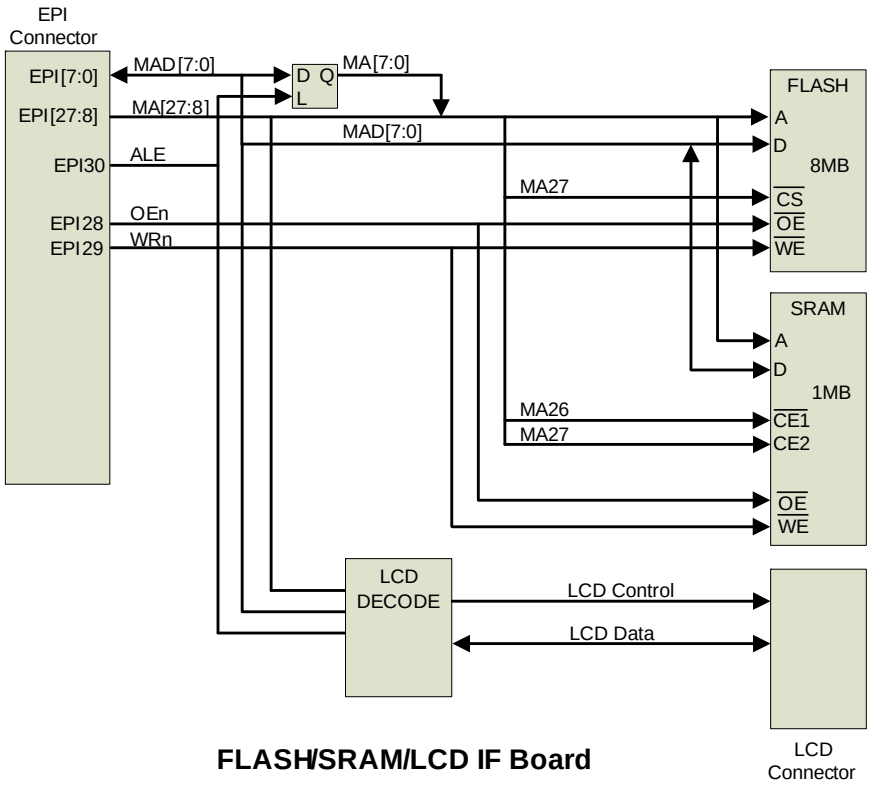
- 8 Megabytes of Flash memory

- 1 Megabyte of SRAM
- Memory-mapped LCD I/F for improved LCD performance
- 1 kilobit of I^2C memory for storing configuration data
- Power LED indicator

Hardware Description

The Flash and SRAM memory expansion board is designed for use with the Stellaris EPI module configured in Host Bus 8 address/data multiplexed mode. This mode requires the use of an external 8-bit latch for storing the lower 8 address lines `A[7:0]` transmitted during the address phase of an EPI transfer. This latch can be seen on the expansion board block diagram shown in Figure E-3.

Figure E-3. DK-LM3S9B96-EXP-FS8 Flash/SRAM/LCD IF Expansion Board Block Diagram



Functional Description

The Flash and SRAM memory expansion board schematics are described in this section. The first page of the schematics shows the memory devices and address latch part of the design. The second page shows the LCD I/F and regulator.

Flash/SRAM (Schematic 1 on page 47)

Page 1 of the schematics shows the EPI connector, address latch, and memory devices.

EPI Connector

The EPI connector J1 is a 50-pin receptacle with 0.5 mm pitch that plugs into the EPI header on the DK-LM3S9B96 board. The 32 EPI signals and the 2 I^2C0 signals from the LM3S9B96 are provided on this connector. It also provides 5 V for the on-board DC regulator. Note that not all EPI signals are used in this design.

8-bit Latch

This 8-bit latch is used to store the lower 8-bits of the address, which are transmitted during the address phase of an EPI transfer. The EPI must be configured in Host bus 8 mode 0 mode (HB8 ADMUX), with EPI30 configured as an Address Latch Enable (ALE) signal to control this latch.

Flash Memory

The Flash memory used is a 64 Mbit, 90-nsec Spansion S29GL064N90TFI040. This 8/16 bit memory is used in 8-bit mode. Note that MA27 is used as a chip select signal for this memory.

SRAM

The SRAM used is an 8 Mbit, 45 nsec Cypress Semiconductor CY62158EV30LL-45ZSX, which is an 8-bit memory. Note that MA27 and MA26 are used as chip selects for this memory.

I^2C Memory

This I^2C serial memory is used for storing configuration data. This is a 1 kilobit On-Semiconductor memory.

LCD I/F, Power (Schematic 2 on page 48)

Page 2 of the schematics shows the LCD_DECODE CPLD, LCD interface connector, and the 3.3 V regulator.

LCD_DECODE CPLD

The LCD DECODE CPLD provides address latch and decode for the LCD interface. The LCD Command and Data registers are mapped on the EPI memory space to streamline access to these registers. The LCD panel control signals L_RDn, L_RWn, and L_DC and the L_D bus are controlled by decode logic on the CPLD with timing derived from EPI signals and do not require direct control from the microcontroller. The LCD latch register is provided to control the XN and YN signals used for the touchscreen and also the reset signal to the LCD.

The LCD backlight signal L_BL is controlled by the Stellaris GPIO PE2 (`MA[24]`). PE2 can be programmed as a GPIO for ON/OFF control of the LCD. A second option is to configure PE2 for use as CCP2 or CCP4 with a PWM output for brightness control.

The TP1-TP4 testpoints connect to the CPLD JTAG signals and, along with TP5 and TP6, provide an interface for test and programming of the CPLD.

LCD Interface Connector

The LCD Interface Connector J2 is a 2x17 socket that connects to headers JP16-JP31 and JP39 on the DK-LM3S9B96. All signals previously driven to the LCD from the Stellaris MCU are replaced by equivalent signals driven from the LCD_DECODE CPLD.

DC Regulator

DC regulator U4 receives 5 V from the EPI connector and provides 3.3 V for the board. LED D1 provides a power indicator and lights when the regulator is providing power to the board.

Memory Map

The DK-LM3S9B96-EXP-FS8 expansion board memory map is shown in Table E-1 and Table E-2 shows the **LCD Latch** register.

Table E-1. Flash and SRAM Memory Expansion Board Memory Map

Device	A[27:26]	A[2:0]	Description	Access	Base address
FLASH	0X	XXX	Flash memory (8 Megabytes)	R/W	0x6000.0000
SRAM	10	XXX	SRAM (1 Megabyte)	R/W	0x6800.0000
CPLD	11	000	LCD latch set	R/W	0x6C00.0000
	11	001	LCD latch clear	R/W	0x6C00.0001
LCD	11	010	LCD command port	R[a]/W	0x6C00.0002
	11	011	LCD data port	R[a]/W	0x6C00.0003
LCD	11	110	LCD command port read start	R	0x6C00.0006
	11	111	LCD data port read start	R	0x6C00.0007

a. For reads to the **LCD Command and Data Port** registers, the corresponding **LCD Port Read Start** register must be read first, followed by a 500 nsec delay before reading this register.

Table E-2. LCD Latch Register

7	6	5	4	3	2	1	0
Reserved					RST	YN	XN
0	0	0	0	0	R/W	R/W	R/W

The **LCD Latch** register is implemented as a set/clear register. To set a bit, the corresponding bit must be set when writing to the **LCD Latch Set** register. To clear a bit, the corresponding bit must be set when writing to the **LCD Latch Clear** register.

XN When clear, the L_XN signal is set to clear. When set, the L_XN signal is tri-stated. This signal is used for the X- input to the touchscreen.

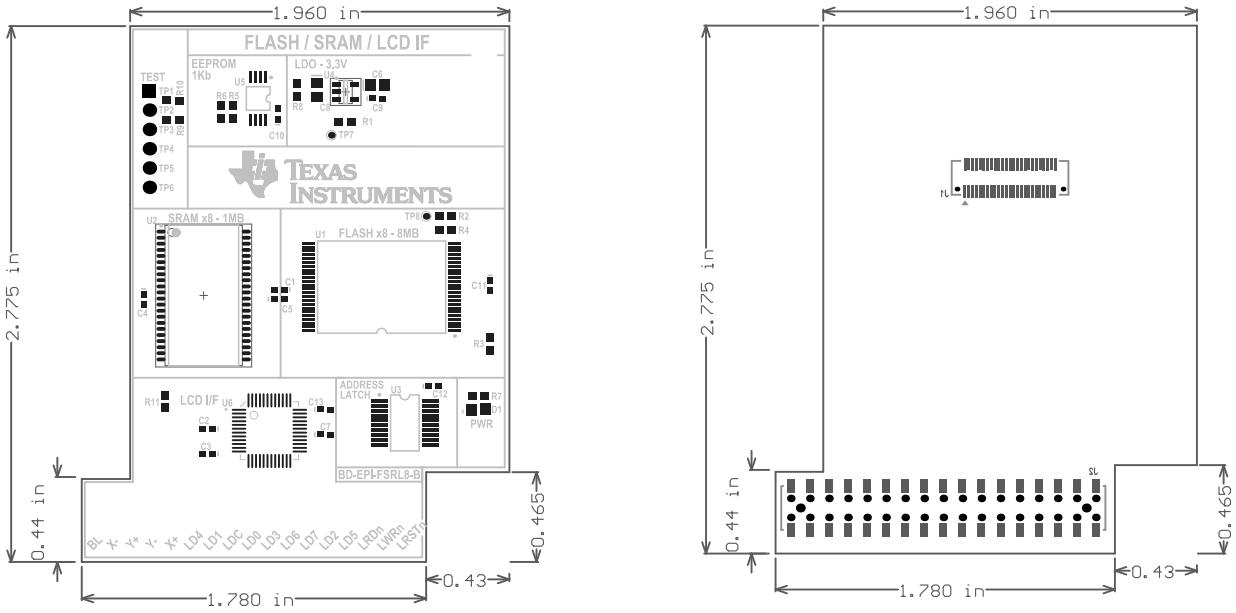
YN When clear, the L_YN signal is set to clear. When set, the L_YN signal is tri-stated. This signal is used for the Y- input to the touchscreen.

RST When clear, the L_RSTN signal is set to clear. When set, the L_RSTN signal is reset. This signal is used to reset the LCD panel.

Component Locations

Figure E-4 shows the details of the component locations.

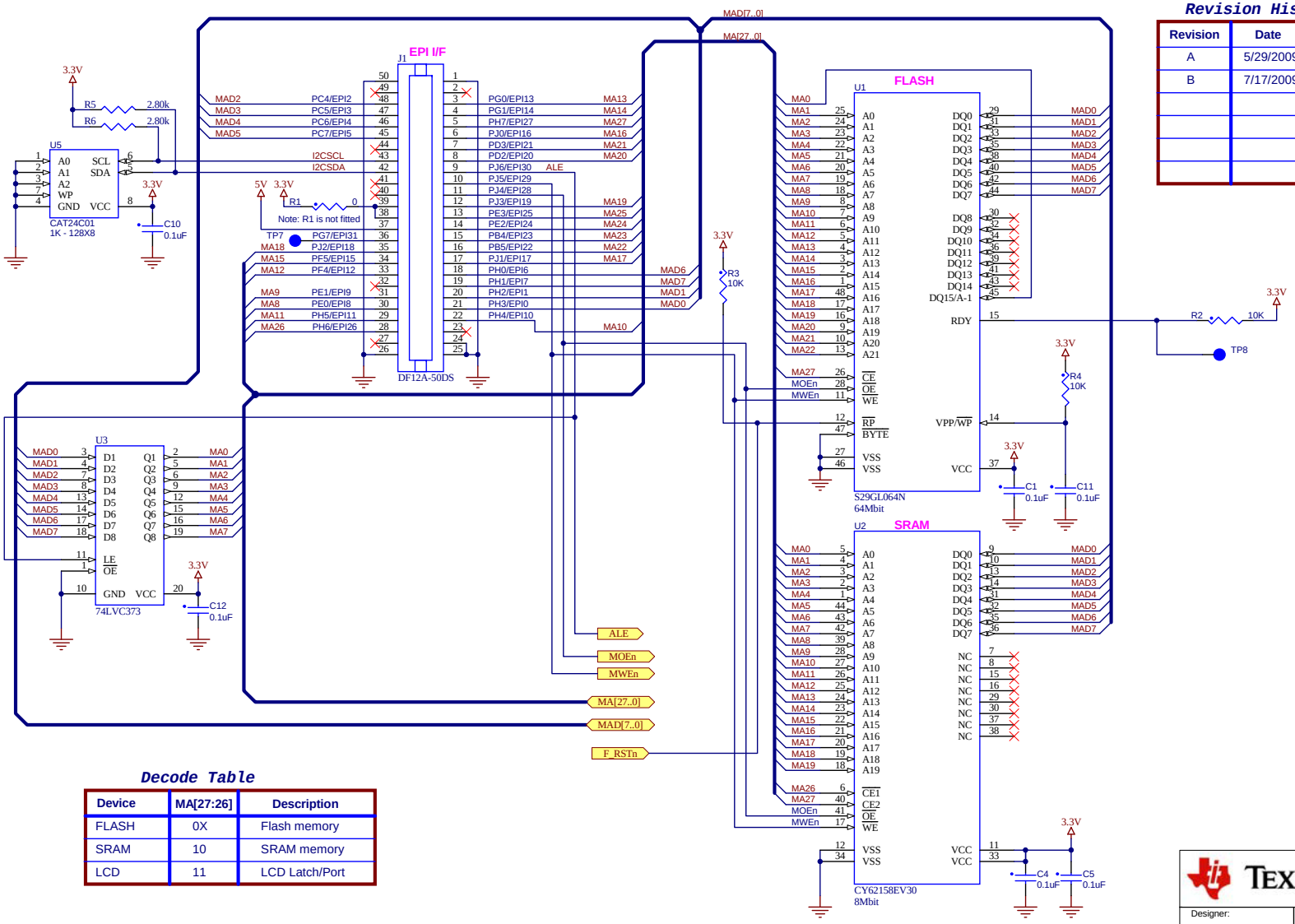
Figure E-4. Component Placement Plot for Top and Bottom



Schematics

This section shows the schematics for the DK-LM3S9B96-EXP-FS8 memory expansion board:

- Flash, SRAM on page 47
- LCD Interface on page 48



Revision History

Revision	Date	Description
A	5/29/2009	Released for manufacturing.
B	7/17/2009	Changed J2 to top entry, moved to bottom. Added R9-R11

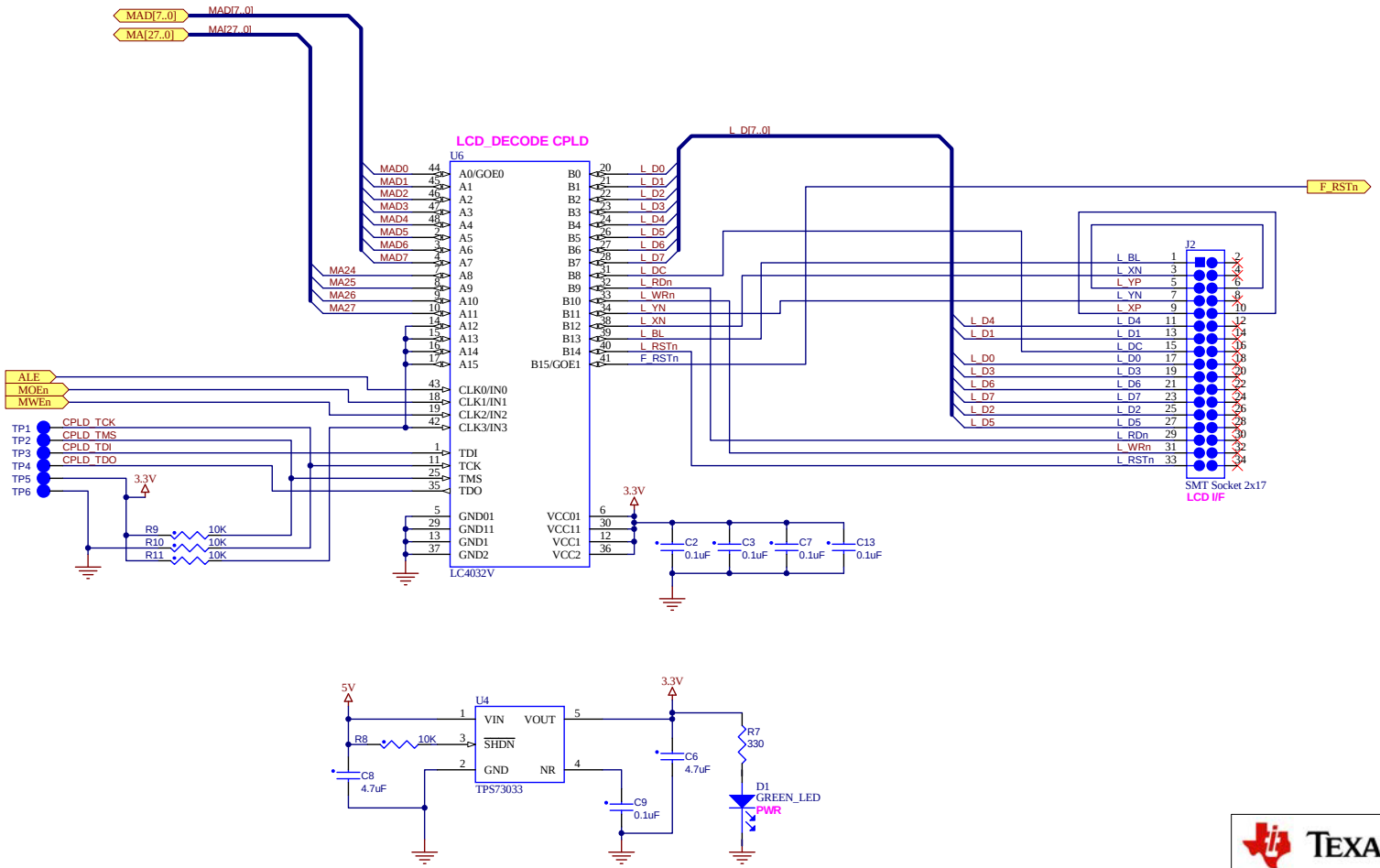
Decode Table

Device	MA[27:26]	Description
FLASH	0X	Flash memory
SRAM	10	SRAM memory
LCD	11	LCD Latch/Port

TEXAS INSTRUMENTS

TI AEC - Austin
108 Wild Basin Rd.
Suite 350
Austin, TX 78746

Designer: Arnaldo Cruz	Drawing Title: FLASH / SRAM / LCD IF board for DK-LM3S9B96		
Drawn by: Arnaldo Cruz	Page Title: FLASH, SRAM		
Approved: *	Size: B	Document Number: 0001	Rev: B
	Date: 7/21/2009	Sheet 1 of 2	



TEXAS INSTRUMENTS

Drawing Title:
FLASH / SRAM / LCD IF board for DK-LM3S9B96

Page Title:
LCD Interface

Size	Document Number:	Rev
B	0001	B

Date: 7/18/2009 Sheet 2 of 2

A P P E N D I X F

Stellaris® DK-LM3S9B96-FPGA Expansion Board

This chapter describes the FPGA expansion board for the DK-LM3S9B96 development board.The FPGA expansion board provides a quick start platform to evaluate the capabilities of the Stellaris External Peripheral Interface (EPI) using the highly integrated DK-LM3S9B96 development platform.

This combination adds full-screen motion video to the powerful, easy-to-use StellarisWare® GUI tools. Figure F-1 shows a photo of the FPGA expansion board.

Figure F-1. DK-LM3S9B96-FPGA Board Image

Features

The DK-LM3S9B96-FPGA memory expansion board has the following features:

- Xilinx Spartan 3E FPGA with 100k system gates
- 1/13" CMOS VGA (640 x 480) Color Camera Module
- 1 MB of asynchronous 10 nsec SRAM for graphics/video buffers
- Standard 1 x 6 and 2 x 5 JTAG headers for FPGA programming
- 1 kilobit of I^2C memory for storing configuration data
- 8 FPGA test pads provide 5 inputs and 3 I/Os
- All necessary power regulation

The default FPGA image adds the following features:

- EPI operation in GPM D16-A12 mode at 50 MHz, up to 100 MB/s
- Graphical on-screen-display (OSD) overlaid on moving QVGA video

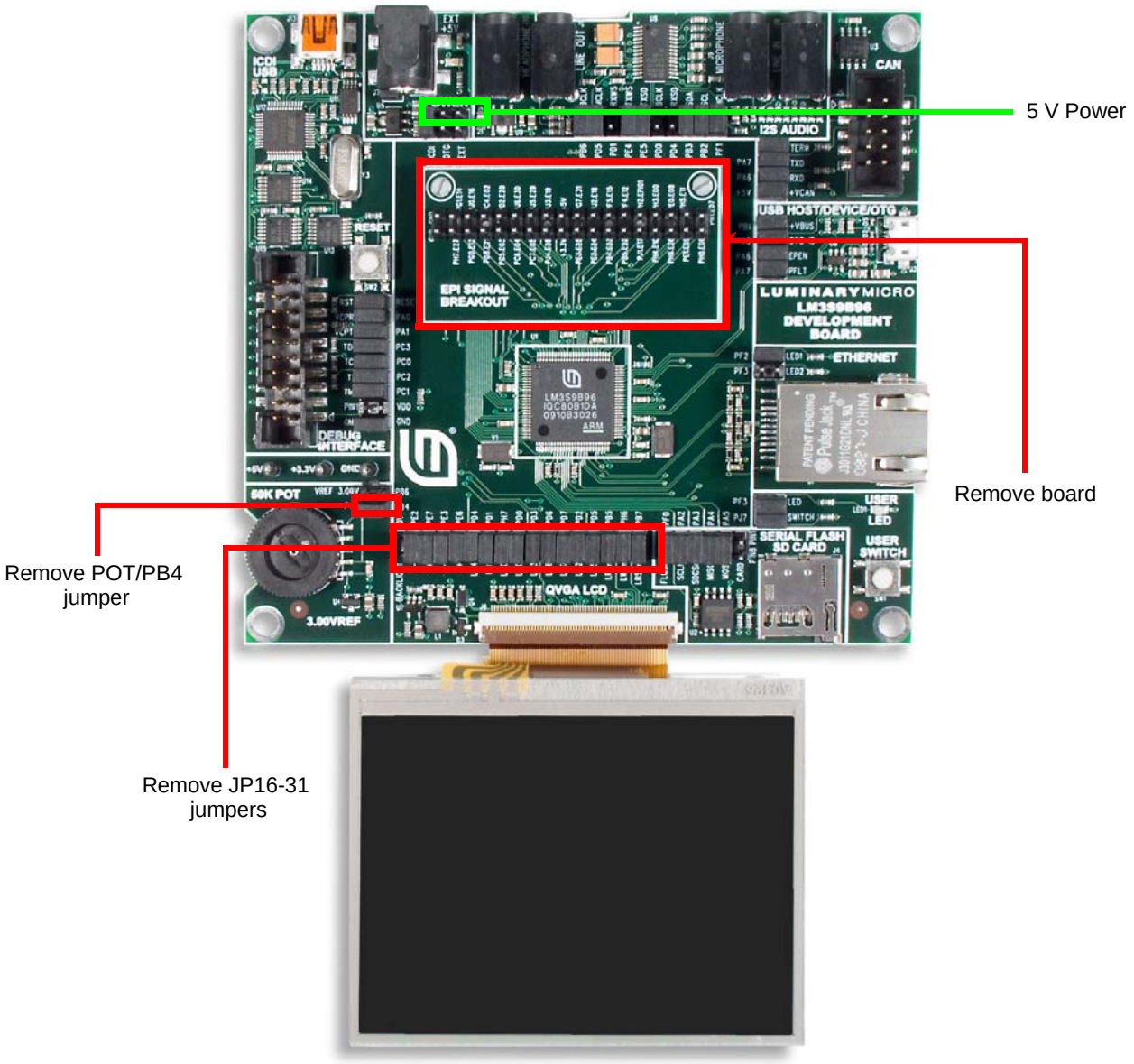
- Widget-based touchscreen user interface
- Screen capture to SDCard or USB stick in Windows bitmap (BMP) format
- Brightness, saturation, tint/hue, and sharpness picture controls
- Mirror/Flip/Normal Picture controls

Installation

To install the expansion board on the DK-LM3S9B96 development board, do the following:

1. Remove the DK-LM3S9B96-FPGA memory expansion board from the antistatic bag.
2. On the DK-LM3S9B96 board, remove any installed board on EPI connector J2.
3. On the DK-LM3S9B96 board, remove the shunt jumpers on JP16-JP31 and the JP39 headers as shown in Figure F-1 on page 49.
4. Place the expansion board on top of the DK-LM3S9B96 board and press firmly downward until the board snaps in.
5. Connect the the male EPI expansion connector on the bottom side of the FPGA expansion board to the female EPI expansion connector on the DK-LM3S9B96 development board (J2). The LCD header pins should fit through the holes on the PCB.
6. Use the included jumper wire to provide 5 V power to J5 from any of the three upper pins immediately below and to the right of the EXT+5V connector on the development board.
7. When powering up the board, verify that the power indicator LED D1 is lit.

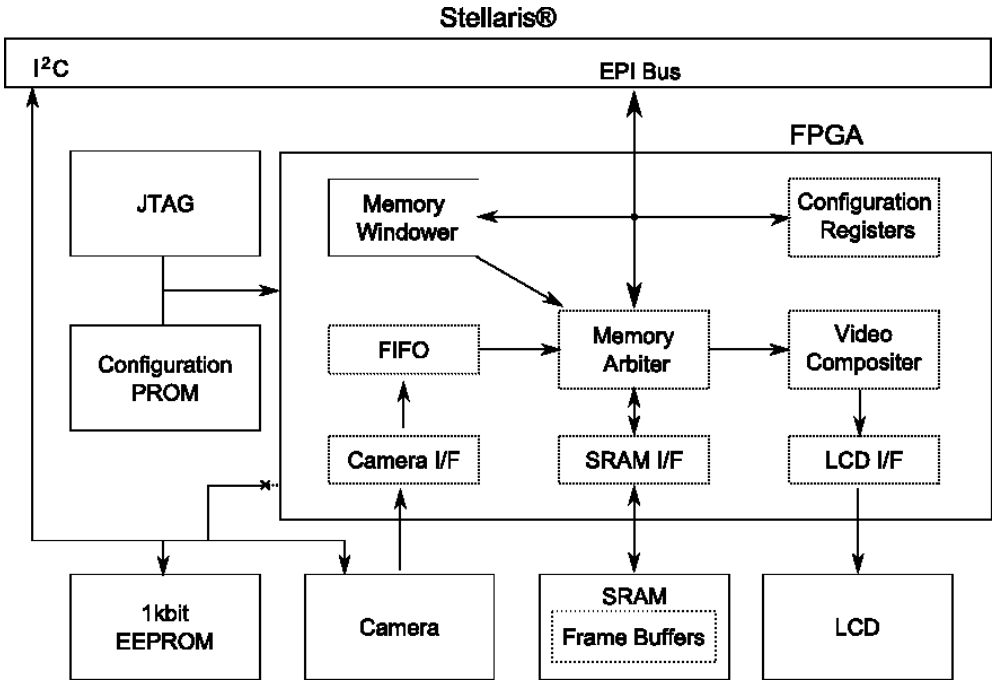
Figure F-2. DK-LM3S9B96 Development Board



Hardware Description

The FPGA expansion board is designed for use with the Stellaris EPI module. Figure F-3 shows a simplified system block diagram. Components of the default FPGA board are shown in half-tone outline.

Figure F-3. DK-LM3S9B96-FPGA Expansion Board Block Diagram



FPGA

The FPGA expansion board features a Xilinx Spartan 3e FPGA, which interfaces to the Stellaris® microcontroller through its EPI port and acts as a crossbar to the rest of the peripherals.

Camera

The Omnivision OV7690 camera provides color VGA images at up to 30 frames per second to the FPGA over an 8-bit wide parallel interface. It is configured by the Stellaris microcontroller via I^2C.

SRAM

The 1 MB, 8-bit wide, 10 ns SRAM is nominally used as a set of frame buffers. 16 bits of the 20-bit address space are latched and multiplexed with its data. Access time may be dependent on the previous address.

Configuration PROM

A Xilinx standard configuration PROM holds the default FPGA image and automatically uploads it at power-on.

Configuration Pushbutton

To reload the configuration PROM image to the FPGA, press the configuration pushbutton. This allows you to load a new image via JTAG without resetting the rest of the system.

Test Port

Eight uncommitted FPGA pins are brought to test pads. Five of the FPGA pins can only be used as inputs. The remaining three FPGA pins can be used as inputs or outputs.

Camera Connector

The camera is hosted by the FPC Connector P1 located to the left of the FPGA. To insert or remove the camera, first open the latch by grasping either side of the connector and gently lifting straight up. With the latch open, the camera moves easily; do not force. The camera faces away from the FPGA. Close the latch by pushing down on it gently before use.

Caution – Handle the camera carefully when inserting or removing it from the board. Never force the camera into a different position, doing so could damage the camera.

5 V Power Pin

J5 is used to provide 5-V power to the FPGA expansion board's regulators. This must be connected for successful board operation. Connect the the male EPI expansion connector on the bottom side of the FPGA expansion board to the female EPI expansion connector on the DK-LM3S9B96 development board (J2). The LCD header pins should fit through the holes on the PCB.

24-MHz Oscillator

The camera and the camera interface portion of the FPGA are clocked by a 24-MHz external oscillator.

External Peripheral Interface (EPI) Module

The External Peripheral Interface (EPI) module provides a slave interface for use with the Stellaris microcontroller's EPI controller configured in general-purpose mode A12-D16. The direction of the signal allocation is in relation to the FPGA (for example, a signal labeled *In* is an input to the FPGA, a signal labelled *Out* is an output from the FPGA). See Table F-8 on page 63 for a list of the EPI signals.

NOTE: Only 16-bit or 32-bit transfers are allowed for this interface.

Using the Widget Interface

This section provides information about writing your own graphics using the widget interface for the FPGA expansion board.

Writing Your Own Stellaris Application

The Stellaris microcontroller communicates with the default FPGA image through a memory-mapped interface. To get started, you must first configure the EPI port by doing the following:

1. Configure the GPIO.
2. Configure the EPI port and map it into memory at 0xA000.0000.

Code Example F-1 Configuring the EPI Port

```
EPIModeSet(EPI0_BASE, EPI_MODE_GENERAL);    //General Purpose mode
EPIDividerSet(EPI0_BASE, 1);                //Divide system clock by 2
```

```
EPIConfigGPModeSet(EPI0_BASE,
   (EPI_GPMODE_DSIZE_16                 //16 Bit data
   | EPI_GPMODE_ASIZE_12                //12 Bit address
   | EPI_GPMODE_WORD_ACCESS             //Use Word Access Mode
   | EPI_GPMODE_READWRITE               //Use read and write strobe pins
   | EPI_GPMODE_READ2CYCLE              //Reads take two cycles
   | EPI_GPMODE_CLKPIN                  //EPI outputs clock to peripheral
   | EPI_GPMODE_RDYEN ),                //Peripheral emits a ready signal
   0,                                   //Not using frame signal, so ignore
   0);                                  //Not using clock enable, so ignore
EPIAddressMapSet(EPI0_BASE,
   EPI_ADDR_PER_SIZE_64KB               //64kB memory space
   | EPI_ADDR_PER_BASE_A);              //EPI base address is 0xA0000000
```

Memory Map

The DK-LM3S9B96-FPGA expansion board memory map is shown in Table F-1. The default Stellaris code maps this into the 0xA000.0XXX memory space. Detailed descriptions for each register are provide in “Register Descriptions” on page 55.

NOTE: Ten bits are used for addressing, but the EPI controller allocates a 12-bit address space. The result is that 0x0A00.0000 is equivalent to 0x0A00.0400, 0x0A00.0800, and 0x0A00.0C00.

Table F-1. DK-LM3S9B96-FPGA Expansion Board Memory Map

Register	A[10:1]	Size	Register Name	Access	See Page
VERSION	000	[15:0]	Board and FPGA Design Version	R	55
SYSCTRL	002	[15:0]	System Control	R/W	56
IRQEN	004	[15:0]	Interrupt Enable	R/W	57
IRQSTAT	006	[15:0]	Interrupt Status	R/W	57
MEMPAGE	008	[10:0]	Memory Page	R/W	58
TPAD	00A	[7:0]	Test Pad	R/W	58
LCTRL	010	[3:0]	LCD Control Set	R/W	58
	012	[3:0]	LCD Control Clear	R/W	
CHRMKEY	022	[15:0]	Chroma Key	R/W	59
VCRM	026	[8:0]	Video Capture Row Match	R/W	59
VML	030	[15:0]	Video Memory Address Low	R/W	59
VMH	032	[4:0]	Video Memory Address High	R/W	59
VMS	034	[11:0]	Video Memory Stride	R/W	59
LRM	036	[7:0]	LCD Row Match	R/W	59
LVML	040	[15:0]	LCD Video Memory Address Low	R/W	60
LVMH	042	[4:0]	LCD Video Memory Address High	R/W	60
LVMS	044	[11:0]	LCD Video Memory Stride register (in bytes).	R/W	60

Table F-1. DK-LM3S9B96-FPGA Expansion Board Memory Map (Continued)

Register	A[10:1]	Size	Register Name	Access	See Page
LGML	050	[15:0]	LCD Graphics Memory Address Low	R/W	60
LGMH	052	[4:0]	LCD Graphics Memory Address High	R/W	60
LGMS	054	[11:0]	LCD Graphics Memory Stride	R/W	60
MPNC	056	[9:0]	Memory Port Number of Columns	R/W	60
MPR	058	[8:0]	Memory Port Current Row	R/W	60
MPC	05A	[9:0]	Memory Port Current Column	R/W	60
MPML	05C	[15:0]	Memory Port Address Low	R/W	60
MPMH	05E	[4:0]	Memory Port Address High	R/W	60
MPMS	060	[11:0]	Memory Port Stride	R/W	60
MPORT	080	[15:0]	Memory Port	R/W	61
MEMWIN	400	[15:0]	Memory Window	R/W	61

Register Descriptions

This section provides the detailed register information for the FPGA expansion board.

Version Register

The **Version** register communicates the revision numbers of the PCB, the FPGA RTL, and the Stellaris silicon. A dummy write of 0x0000 to this register determines if the Stellaris silicon is revision C (or higher) and configures the EPI clocking circuit appropriately. This is required during initialization for proper operation.

Table F-2. Version Register

VERSION: 0xA000.0000

15	14	13	12	11	10	9	8
PCB Board Version					0	0	RevC
R	R	R	R	R	R	R	R

7	6	5	4	3	2	1	0
RTL Major Version				RTL Minor Version			
R	R	R	R	R	R	R	R

Bit Name **Description**

PCB Board Version:
Revision level of the FPGA expansion board.

RevC: This bit is high if the FPGA believes it is communicating with Revision C of the silicon (or higher). This bit is only valid after being initialized as described above.

RTL Version Revision level of the code running in the FPGA expansion board.

System Control Register

The **System Control** register provides access to configuration bits for the video capture and display system. It is implemented as a read-modify-write register and includes LCD and capture modes.

Table F-3. System Control Register

SYSCTRL: 0xA000.0002

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	PCBrA
R	R	R	R	R	R	R	R/W

7	6	5	4	3	2	1	0
VCTEST	VCQVGA	MPRI	VSCALE	CMKEN	LGDEN	LVDEN	VCEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Name	Description
VCEN	Video capture DMA enable. Enables video capture to memory. Disabling this bit captures the remainder of the current frame, and then stops.
LVDEN	LCD Video DMA enable. Enables DMA from the video memory region to the LCD.
LGDEN	LCD Graphics DMA enable. Enables DMA from the graphics memory region to the LCD.
CMKEN	Chroma key enable.
VSCALE	Video scale control. Scales the video during output to the LCD. If set, the LCD DMA engine skips every other pixel and every other row during LCD video DMA output (Graphics DMA is not affected). As a result, the video object displays at ¼ its normal size.
MPRI	Memory port row increment. If set to 0, any read or write to the memory port auto increments the MPC register at the end of the transfer by 1. If MPC is at the last column (MPNR-1), then it sets to 0 and the MPR increments by 1. If the end of the row is reached, then it increments by columns. If set to 1, any read or write increments by rows.
VCQVGA	Video Capture is QVGA/VGA. If set to 0, the video capture controller assumes that the camera is configured for VGA capture. If set to 1, it assumes that the camera is configured for QVGA. This only affects video capture; the camera's I^2C and LCD settings must be reconfigured manually.
VCTEST	Video Capture Test. When set to 1, the incoming pixel stream is ignored and replaced with a test pattern.
PCBrA	PCB is Revision A. An early internal revision of the PCB had a different pin configuration for the camera data port. Setting this bit to 1 provides backwards compatibility.

Interrupt Enable Register

The **Interrupt Enable** register masks or enables interrupts from the FPGA to the Stellaris LM3S9B96 microcontroller. Masked interrupts will not assert the IRQ line, but they will still appear in the Interrupt Status Register.

Table F-4. Interrupt Enable Register

IRQEN: 0xA000.0004

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R	R	R	R	R	R	R	R

7	6	5	4	3	2	1	0
0	0	LRMIE	LTEIE	LTSIE	VRMIE	VCFEIE	VCFSIE
R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit Name	Description
VCFSIE	Video capture frame start interrupt enable.
VCFEIE	Video capture frame end interrupt enable.
VRMIE	Video capture row match interrupt enable.
LTSIE	LCD transfer start interrupt enable.
LTEIE	LCD transfer end interrupt enable.
LRMIE	LCD display row match interrupt enable.

Interrupt Status Register

The **Interrupt Status** register reports and clears interrupts from the camera and LCD systems. An interrupt latches its corresponding bit high until cleared by writing a 1 to it.

Table F-5. Interrupt Status Register

IRQSTAT: 0xA000.0006

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R	R	R	R	R	R	R	R

7	6	5	4	3	2	1	0
0	0	LRMI	LTEI	LTSI	VRMI	VCFEI	VCFSI
R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit Name	Description
VCFSI	Video capture frame start interrupt. Clear the interrupt by setting the corresponding bit to 1. Setting the bit to 0 has no effect.

VCFEI	Video capture frame end interrupt. Clear the interrupt by setting the corresponding bit to 1. Setting the bit to 0 has no effect.
VRMI	Video capture row match interrupt. Clear the interrupt by setting the corresponding bit to 1. Setting the bit to 0 has no effect.
LTSI	LCD transfer start interrupt. Clear the interrupt by setting the corresponding bit to 1. Setting the bit to 0 has no effect.
LTEI	LCD transfer end interrupt. Set to 1 to clear the corresponding bit. Clear the interrupt by setting the corresponding bit to 1. Setting the bit to 0 has no effect.
LRMI	LCD display row match interrupt. Clear the interrupt by setting the corresponding bit to 1. Setting the bit to 0 has no effect.

Memory Page Register

The **Memory Page** register selects to memory page to access.

Test PadRegister

The **Test Pad** register is used to access the on-board test pads TP1-TP8, which are connected to unused FPGA pins.

Table F-6. Test Pad Register

TXPAD: 0xA000.000A

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R	R	R	R	R	R	R	R

7	6	5	4	3	2	1	0
TP8	TP7	TP6	TP5	TP4	TP3	TP2	TP1
R	R	R	R	R	R/W	R/W	R/W

Bit Name	Description
TP1-TP3	Test Pins 1-3. These are connected to FPGA I/O pins. Writing a 1 sets the corresponding test pin output to 1. Writing a 0 sets the corresponding test pint output to 0. Reading these bits returns the value at the corresponding test pin input.

NOTE: The FPGA output driver for these signals is always enabled.

TP4-TP8	Test Pins 4-8.These are connected to FPGA input pins. Writing these bits has no effect. Reading these bits returns the value at the corresponding test pin input.

LCD Control Register

The **LCD Control** register is implemented as a set/clear register and contains four bits for LCD panel control. To set a bit, set the corresponding bit to 1 when writing to the **LCD Control Set** register. To clear a bit, set the corresponding bit when writing to the **LCD Control Clear** register.

Table F-7. LCD Control Register

LCDCTRL: 0xA000.0012

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R	R	R	R	R	R	R	R

7	6	5	4	3	2	1	0
0				BL	$\overline{RST}$	YN	XN
R	R	R	R	R/2	R/W	R/W	R/W

Bit Name	Description
XN	LCD panel touchscreen X control. When set to 0, the LCD Xn signal is set to 0. When set to 1, the LCD Xn signal is tri-stated.
YN	LCD panel touchscreen Y control. When set to 0, the LCD Yn signal is set to 0. When set to 1, the LCD Yn signal is tri-stated.
$\overline{RST}$	LCD panel reset control. When set to 0, the LCD RSTn signal is set to 0. When set to 1 the LCD RSTn signal is set to 1.
BL	LCD backlight control. When set to 0, the LCD panel backlight is turned off. When set to 1, the LCD panel backlight is turned on.

Chroma Key Register

The **CHRMKEY** register contains the RGB values to compare for graphics overlay operation. During LCD screen updates, data from graphics memory is compared with this register, if a match occurs, the corrsponding frame video pixel is sent to the output instead.

Video Capture Row Match Register

During video capture, at the start of a row, the current row value is compared with the **VCRM** register. A match generates an interrupt if enabled.

Video Memory Address Low Register

The **VML** register provides a pointer to the start of video capture memory and contains the lower 16-bits of the address.

Video Memory Address High Register

The **VMH** register provides a pointer to the start of video capture memory and contains the higher 16-bits of the address.

Video Memory Stride Register

The **VMS** register specifies the number of locations in video memory between successive array elements (stride) and is measured in bytes. Using stride enables better processing time.

LCD Row Match Register

During LCD display DMA output, at the start of each row, the current row value is compared with the **LRM** register. A match generates an interrupt if enabled.

LCD Video Memory Address Low Register

The **LVML** register provides a pointer to the start of video data for transfer to the LCD. This contains the lower 16-bits of the address.

LCD Video Memory Address High Register

The **LVMH** register provides a pointer to the start of video data for transfer to the LCD. This contains the higher 16-bits of the address.

LCD Video Memory Stride Register

The **LVMS** register specifies the number of bytes between the first pixels on adjacent rows in LCD video memory. Recommended to be either the length of a row (in bytes), or the next highest power of two.

LCD Graphics Memory Address Low Register

The **LGML** register provides a pointer to the start of graphics memory for output to the LCD and contains the lower 16-bits of the address.

LCD Graphics Memory Address High Register

The **LGMH** register provides a pointer to the start of graphics memory for output to the LCD and contains the higher 16-bits of the address.

LCD Graphics Memory Stride Register

The **LGMS** register specifies the number of bytes between the first pixels on adjacent rows in LCD graphics memory. Recommended to be either the length of a row (in bytes), or the next highest power of two.

Memory Port Number of Columns Register

The **MPNC** register specifies the number of columns (in pixels) of the memory port.

Memory Port Current Row Register

The **MPR** register identifies the selected row in the memory port.

Memory Port Current Column Register

The **MPC** register identifies the selected column in the memory port.

Memory Port Address Low Register

The **MPML** register contains the lower address bits of the memory region accessed by the memory port.

Memory Port Address High Register

The **MPMH** register contains the upper address bits of the memory region accessed by the memory port.

Memory Port Stride Register

The **MPMS** register specifies the number of bytes between the first pixels on adjacent rows in the memory port. Recommended to be either the length of a row (in bytes), or the next highest power of two.

Memory Port Register

The **MPORT** register allows sequential video/graphics memory plane access. A write (read) to this port generates a memory write (read) to the memory location calculated as follows:

```
Mem address = {MPH:MPL} + MPR x MPS + MPC.
```

After the transfer, if the MPC is not at the last pixel of the row, it automatically increments by 1. If the MPC is at the last pixel of the row, it sets to 0 and the MPR is incremented by MPS.

Memory Window Register

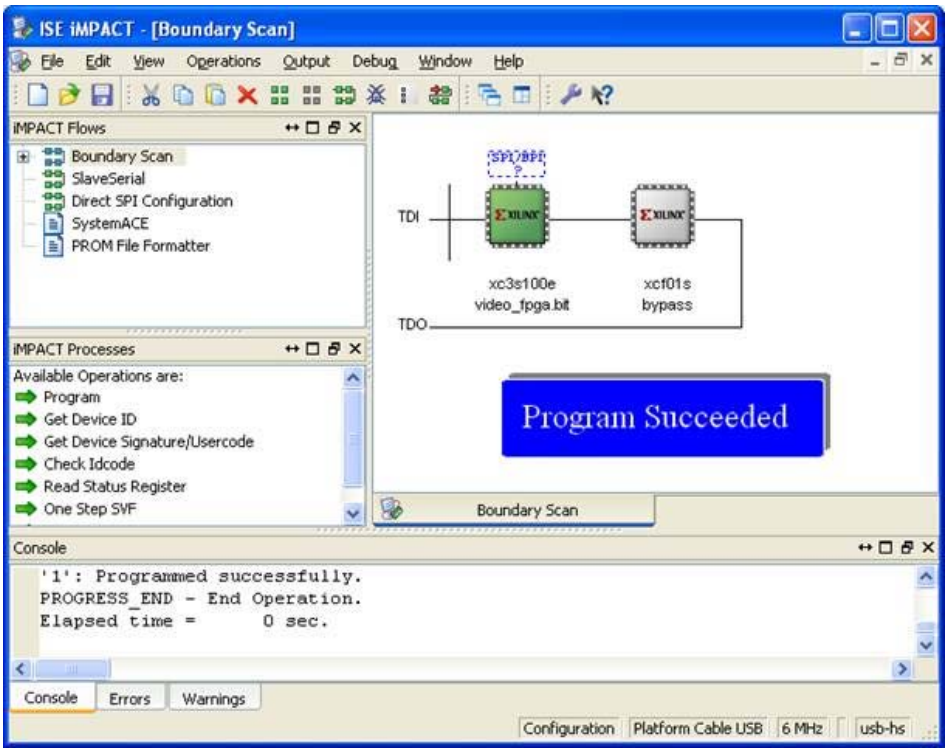
Use the MEMPAGE register to select the active page (1 Kbyte page).

Loading a New Image to the FPGA

The FPGA can be re-imaged using any of the JTAG tool chains that support the Xilinx Spartan 3e XC3S100e. Two standard JTAG interfaces are provided with the FPGA expansion board: 2 x 7 with 2mm pitch and 1 x 6 with .1" pitch. Once connected, your JTAG scan chain should show an XC3S100e FPGA and an XCF01S PROM.

NOTE: Images loaded into the PROM must be set to use CCLK as the startup clock. Images loaded direct to the FPGA may use either CCLK or JTAG CLK.

Figure F-4. DK-LM3S9B96-FPGA Boundary Scan



NOTE: The DK-LM3S9B96-FPGA boots in JTAG mode, but transitions to serial mode once configured by the PROM. If your programmer is JTAG-only, you may need to clear the PROM and power cycle before you can directly program the FPGA via JTAG. This issue is rare since most tools support both modes. Check with your tool manufacturer for updates.

Installing the Software

To install the software, do the following:

1. Plug the provided cable into J4 (on the right side of the board), taking care to ensure proper alignment and orientation. The silk-screened signal names should match, with the exception that 2.5 V corresponds to VDD. When correctly aligned, the “JTAG-SPI Full Speed" text should face in toward the FPGA.

Modifying the Default Image

This section provides the descriptions for the default FPGA image blocks.

Default FPGA Image Blocks

Configuration Registers

The configuration registers are transparently mapped into the Stellaris microcontroller's memory, and are used to control the flow of the video streams. “Register Descriptions” on page 55 provides the detailed register maps. This is contained within the vregs.v file.

Memory Windower

The memory windower allows the Stellaris microcontroller to work with a rectangular portion of a frame buffer. For example, this can be used to pull macro-cells for JPEG compression. This is contained within the mport.v file.

Memory Arbiter

The memory arbiter negotiates access to the external SRAM. The camera capture block is given highest priority. This is contained within the arb.v file.

Video Compositor

The video compositor assembles the final image from the video and graphics frame buffers, and passes it directly to the LCD Interface. It also converts the camera's VGA resolution to the LCD's QVGA resolution by either downsampling. This is contained within the vlcd.v file.

LCD I/F

The LCD interface connects to the Kitronix 3.5" LCD display using an 8-bit parallel mode. This is usually driven by the Video Compositor, but can also be driven directly by the EPI interface. This is contained within the vregs.v file.

Camera I/F

The camera interface block captures pixel data from the Omnivision OV7690's 8-bit digital video port and synchronization signals. This is contained within vcapture.v

Camera FIFO

The Camera FIFO serves two main purposes: reclocking and flow control. The camera and camera interface run in their own 12-/24-MHz clock domain, whereas the rest of the system runs off of the EPI clock or twice the EPI clock. The FIFO bridges these difference clock domains. The camera does not support any flow control functions; once triggered, it proceeds through an entire image. In order to prevent loss of pixels, this FIFO is 64 elements deep. This is contained within the vcapture.v and async_fifo_64.v files.

EPI Signal Descriptions

Table F-8 provides the EPI module's signal descriptions.

Table F-8. EPI Signal Descriptions

EPI Signal	Port	FPGA Signal	Direction	Description
EPIOS[31]	PG7	CLK	In	EPI Clock
EPIOS[30]	PJ6	E_IRQn	Out	Interrupt Signal to Microcontroller[a]
EPIOS[29]	PJ5	E_RD	In	EPI Read Strobe
EPIOS[28]	PJ4	E_WR	In	EPI Write Strobe
EPIOS[27]	PH7	E_RDY	Out	EPI Ready Signal
EPIOS[26]	PH6	E_RSTn	In	FPGA Reset Signal [b]
EPIOS[25:16]	PE3,PE2,PB4, PB5,PD3,PD2,PJ3, PJ2,PJ1,PJ0	E_ADDR[10:1]	In	EPI Address Bus
EPIOS[15:0]	PF5,PG1,PG0,PF4, PH5,PH4,PE1,PE0, PH1,PH0,PC7,PC6, PC5,PC4,PH2,PH3	E_DATA[15:0]	I/O	EPI Data Bus

a. Configure as Stellaris GPIO input with negative level sensitive interrupts. During power up/reset is used for PLL lock status.
b. Configure as Stellaris GPIO output.

Component Locations

Figure F-5 shows the details of the component locations from the top view and Figure F-6 shows the details of the component locations from the bottom view.

Figure F-5. Component Placement Plot for Top

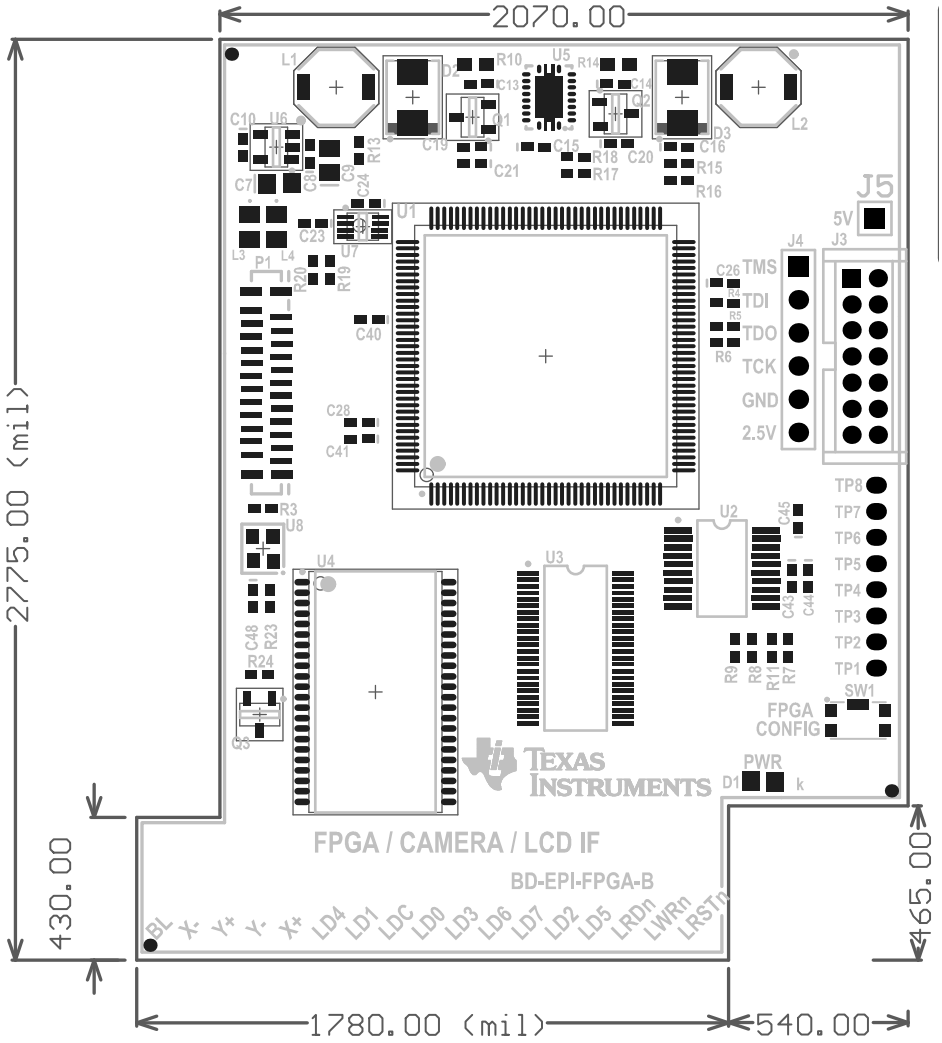
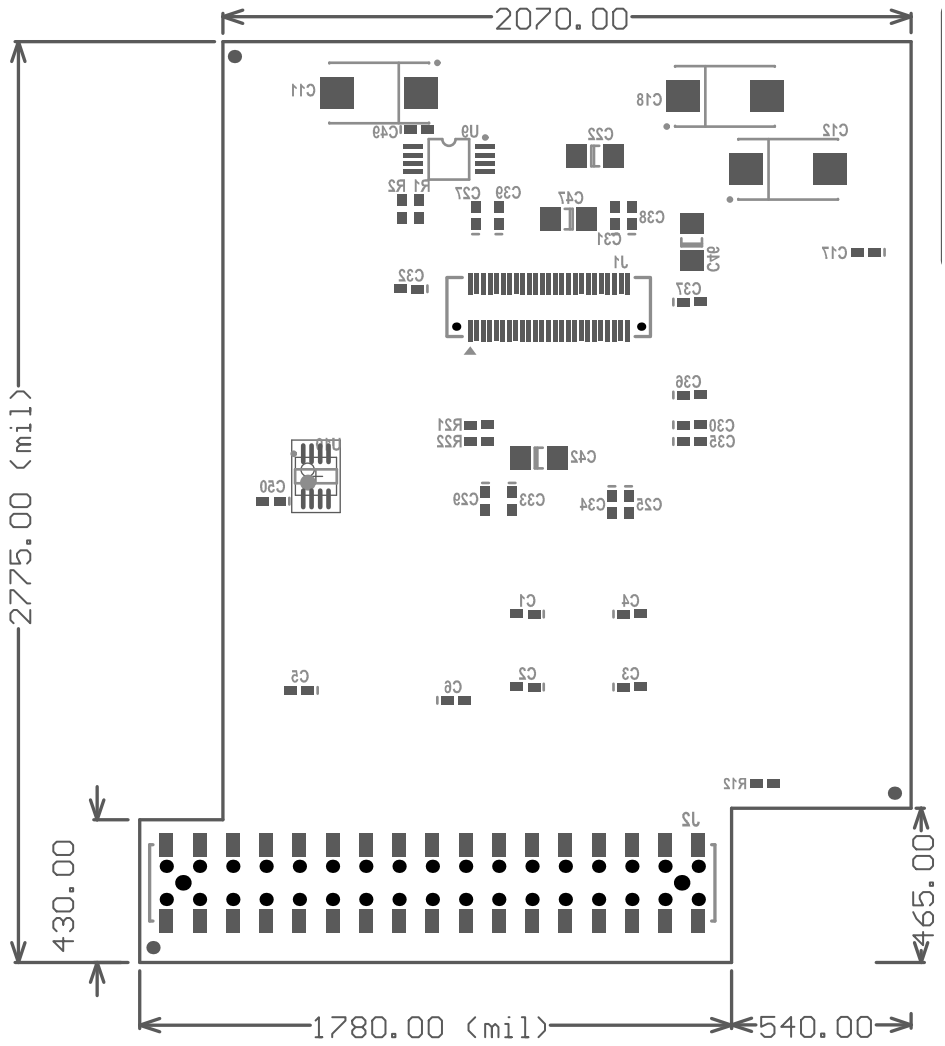


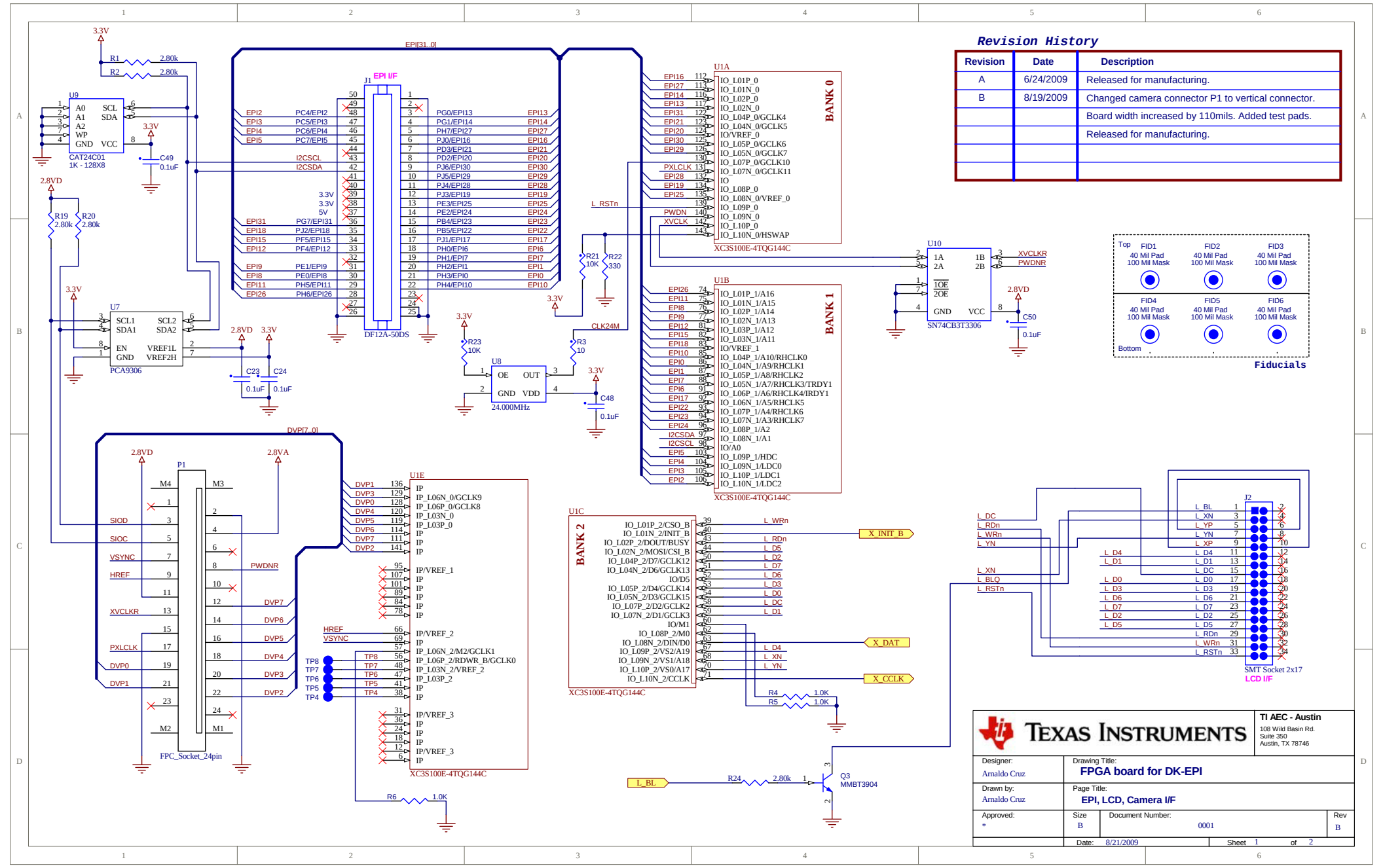
Figure F-6. Component Placement Plot for Bottom

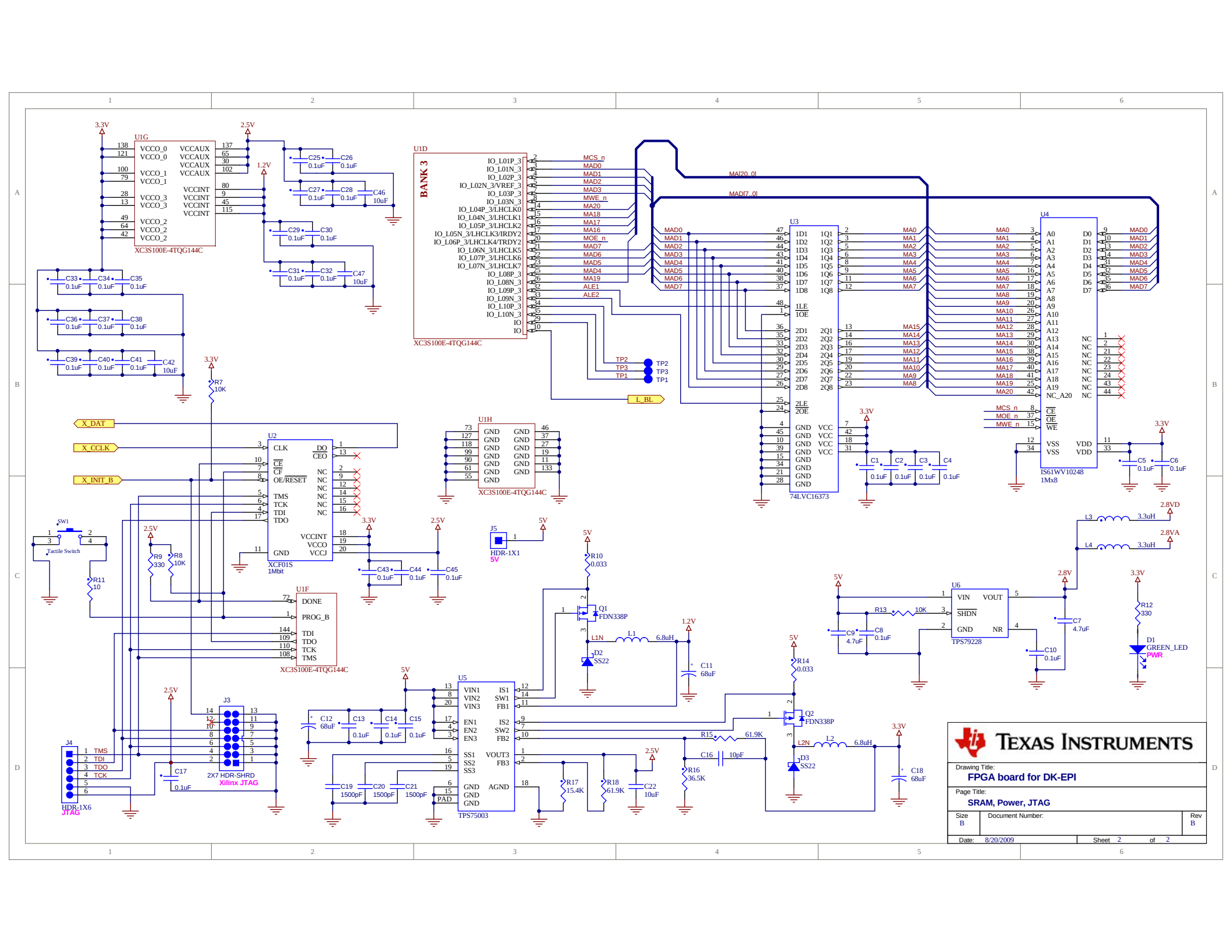


Schematics

This section shows the schematics for the DK-LM3S9B96-FPGA memory expansion board:

- EPI, LCD, Camera I/F on page 66
- SRAM, Power, JTAG on page 67


Revision History
Revision | Date | Description
A | 6/24/2009 | Released for manufacturing.
B | 8/19/2009 | Changed camera connector P1 to vertical connector.
| | Board width increased by 110mils. Added test pads.
| | Released for manufacturing.
EPI[31..0]
DVP[7..0]
EPI I/F
J1
U1A
U1B
U1C
U1D
U1E
BANK 0
BANK 1
BANK 2
XC3S100E-4TQG144C
U9
CAT24C01
1K - 128X8
U7
PCA9306
U8
24.000MHz
U10
SN74CB3T3306
P1
FPC_Socket_24pin
DF12A-50DS
J2
SMT Socket 2x17
LCD I/F
Fiducials
Top
Bottom
FID1
FID2
FID3
FID4
FID5
FID6
40 Mil Pad
100 Mil Mask
Q3
MMBT3904
TEXAS INSTRUMENTS
TI AEC - Austin
108 Wild Basin Rd.
Suite 350
Austin, TX 78746
Designer: Arnaldo Cruz
Drawn by: Arnaldo Cruz
Approved: *
Drawing Title: FPGA board for DK-EPI
Page Title: EPI, LCD, Camera I/F
Size: B
Document Number: 0001
Rev: B
Date: 8/21/2009
Sheet 1 of 2


U1G
XC3S100E-4TQG144C
U1D
BANK 3
XC3S100E-4TQG144C
U3
74LVC16373
U4
IS61WV10248
1Mx8
U2
XCF01S
1Mbit
U1H
XC3S100E-4TQG144C
U1F
XC3S100E-4TQG144C
U5
TPS75003
U6
TPS79228
J3
2X7 HDR-SHRD
Xilinx JTAG
J4
HDR-1X6
JTAG
J5
HDR-1X1
5V
SW1
Tactile Switch
Q1
FDN338P
Q2
FDN338P
D1
GREEN_LED
PWR
D2
SS22
D3
SS22
L1
6.8uH
L2
6.8uH
L3
3.3uH
L4
3.3uH
2.8VD
2.8VA
MAD[20..0]
MAD[7..0]
L_BL
X_DAT
X_CCLK
X_INIT_B
TEXAS INSTRUMENTS
Drawing Title:
FPGA board for DK-EPI
Page Title:
SRAM, Power, JTAG
Size
B
Document Number:
Rev
B
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A P P E N D I X G

References

In addition to this document, the following references are included on the Stellaris Family Development Kit documentation CD-ROM and are also available for download at www.ti.com/stellaris:

- *Stellaris LM3S9B96 Microcontroller Data Sheet*
- *Kitronix LCD Data Sheet*
- StellarisWare Driver Library
- *StellarisWare Driver Library User's Manual*, publication number SW-DRL-UG

Additional references include:

- *FT2232D Dual USB/UART FIFO IC Data sheet*, version 0.91, 2006, Future Technology Devices International Ltd.
- *Texas Instruments TLV320AIC23BPM Audio CODEC Data Sheet*
- Information on development tool being used:
  - RealView MDK web site, www.keil.com/arm/rvmdkkit.asp
  - IAR Embedded Workbench web site, www.iar.com
  - Code Sourcery GCC development tools web site, www.codesourcery.com/gnu_toolchains/arm
  - Code Red Technologies development tools web site, www.code-red-tech.com
  - Texas Instruments' Code Composer Studio™ IDE web site, www.ti.com/ccs

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