SCLS374L - MAY 1997 - REVISED FEBRUARY 2004

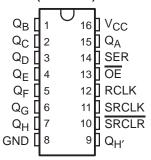
- Inputs Are TTL-Voltage Compatible
- 8-Bit Serial-In, Parallel-Out Shift
- Shift Register Has Direct Clear
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

description/ordering information

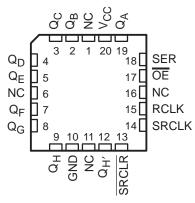
The 'AHCT595 devices contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state outputs. Separate clocks are provided for the shift and storage registers. The shift register has a direct overriding clear (SRCLR) input, serial (SER) input, and serial outputs for cascading. When the output-enable (OE) input is high, the outputs are in the high-impedance state.

Both the shift register clock (SRCLK) and storage register clock (RCLK) are positive-edge triggered. If both clocks are connected together, the shift register always is one clock pulse ahead of the storage register.

SN54AHCT595 . . . J OR W PACKAGE SN74AHCT595 . . . D, DB, N, NS, OR PW PACKAGE (TOP VIEW)



SN54AHCT595 . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

ORDERING INFORMATION

TA	PACK	AGE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	PDIP – N	Tube	SN74AHCT595N	SN74AHCT595N
−40°C to 85°C	0010 D	Tube	SN74AHCT595D	ALIOTEOE
	SOIC - D	Tape and reel	SN74AHCT595DR	AHCT595
	SOP - NS	Tape and reel	SN74AHCT595NSR	AHCT595
	SSOP – DB	Tape and reel	SN74AHCT595DBR	HB595
	TOCOD DW	Tube	SN74AHCT595PW	LIDEOE
	TSSOP – PW	Tape and reel	SN74AHCT595PWR	HB595
	CDIP – J	Tube	SNJ54AHCT595J	SNJ54AHCT595J
–55°C to 125°C	CFP – W	Tube	SNJ54AHCT595W	SNJ54AHCT595W
	LCCC - FK	Tube	SNJ54AHCT595FK	SNJ54AHCT595FK

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



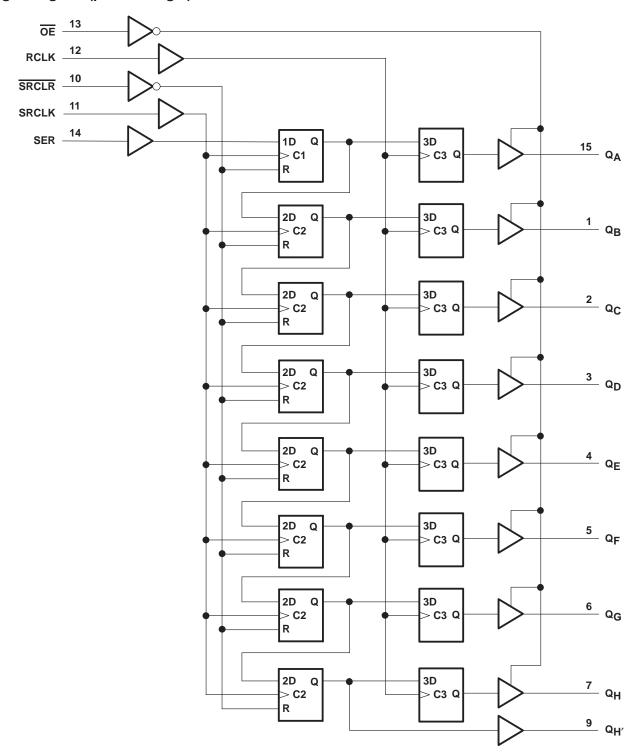
SN54AHCT595, **SN74AHCT595 8-BIT SHIFT RÉGISTERS** WITH 3-STATE OUTPUT REGISTERS SCLS374L - MAY 1997 - REVISED FEBRUARY 2004

FUNCTION TABLE

		INPUTS			FUNCTION
SER	SRCLK	SRCLR	RCLK	OE	FUNCTION
Х	Х	Х	Х	Н	Outputs Q _A –Q _H are disabled.
Х	Χ	Χ	Χ	L	Outputs Q _A –Q _H are enabled.
Х	Χ	L	Χ	Χ	Shift register is cleared.
L	↑	Н	Х	Х	First stage of the shift register goes low. Other stages store the data of previous stage, respectively.
Н	1	Н	Х	Х	First stage of the shift register goes high. Other stages store the data of previous stage, respectively.
Х	Х	Х	1	Х	Shift-register data is stored in the storage register.



logic diagram (positive logic)

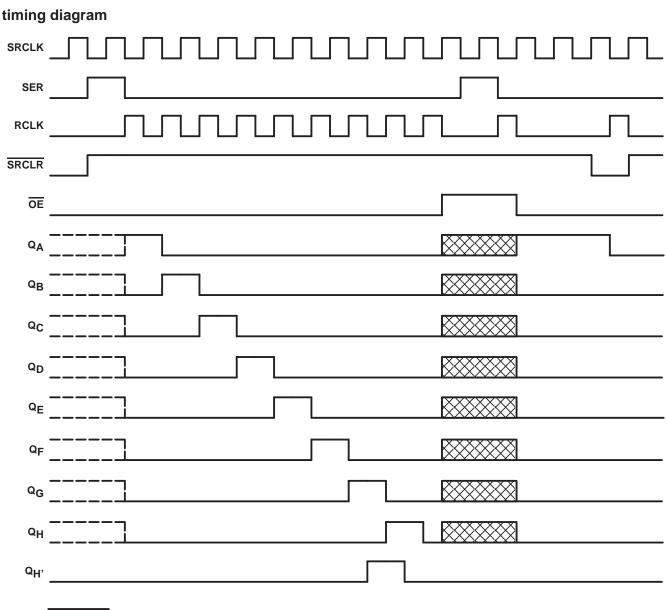


Pin numbers shown are for the D, DB, J, N, NS, PW, and W packages.



SN54AHCT595, SN74AHCT595 8-BIT SHIFT REGISTERS WITH 3-STATE OUTPUT REGISTERS

SCLS374L - MAY 1997 - REVISED FEBRUARY 2004



NOTE: implies that the output is in 3-State mode.



SCLS374L - MAY 1997 - REVISED FEBRUARY 2004

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}		–0.5 V to 7 V
Input voltage range, V _I (see Note 1)		–0.5 V to 7 V
Output voltage range, VO (see Note 1)		$1.000 - 0.5 \text{ V}$ to $V_{CC} + 0.5 \text{ V}$
Input clamp current, I_{IK} ($V_I < 0$)		–20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CO}$	c)	±20 mA
Continuous output current, $I_O(V_O = 0 \text{ to } V_{CC})$	· · · · · · · · · · · · · · · · · · ·	±25 mA
Continuous current through V _{CC} or GND		±50 mA
Package thermal impedance, θ _{JA} (see Note 2):	: D package	
	DB package	82°C/W
	N package	67°C/W
	NS package	64°C/W
	PW package	108°C/W
Storage temperature range, T _{stg}		–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		SN54AH	CT595	SN74AH	CT595	
		MIN	MAX	MIN	MAX	UNIT
VCC	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2	7	2		V
VIL	Low-level input voltage		0.8		0.8	V
VI	Input voltage	0	5.5	0	5.5	V
VO	Output voltage	0	VCC	0	VCC	V
loh	High-level output current	27/	-8		-8	mA
loL	Low-level output current	70/	8		8	mA
Δt/Δν	Input transition rise or fall rate	Q	20		20	ns/V
TA	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

SN54AHCT595, SN74AHCT595 8-BIT SHIFT RÉGISTERS WITH 3-STATE OUTPUT REGISTERS

SCLS374L - MAY 1997 - REVISED FEBRUARY 2004

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	TT0T 001/D/T/01/0		T,	ղ = 25°C	;	SN54AH	CT595	SN74AHCT595		
PARAMETER	TEST CONDITIONS	VCC	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
V	IOH = -50 μA	451/	4.4	4.5		4.4		4.4		\/
VOH	I _{OH} = -8 mA	4.5 V	3.94			3.8		3.8		V
.,	I _{OL} = 50 μA	4.5.1/			0.1		0.1		0.1	.,
VOL	I _{OL} = 8 mA	4.5 V			0.36		0.44		0.44	V
lį	V _I = 5.5 V or GND	0 V to 5.5 V			±0.1		±1*		±1	μΑ
loz	$V_O = V_{CC}$ or GND, $Q_A - Q_H$	5.5 V			±0.25	4	±2.5		±2.5	μΑ
ICC	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			4	20	40		40	μΑ
ΔICC [†]	One input at 3.4V, Other inputs at V _{CC} or GND	5.5 V			2	PRO	2.2		2.2	mA
Ci	V _I = V _{CC} or GND	5 V		3	10				10	pF
Co	VO = VCC or GND	5 V		5.5						pF

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (unless otherwise noted) (see Figure 1)

			T _A = 1	25°C	SN54AH	CT595	SN74AH	CT595	
			MIN	MAX	MIN	MAX	MIN	MAX	UNIT
		SRCLK high or low	5		5.5		5.5		
t _w	t _w Pulse duration	RCLK high or low			5.5	TEL	5.5		ns
		SRCLR low	5		5	FE	5		
		SER before SRCLK↑	3		3,4	2	3		
	0	SRCLK↑ before RCLK↑‡	5		5		5		
t _{su}	Setup time	SRCLR low before RCLK↑	5		S 5		5		ns
		SRCLR high (inactive) before SRCLK↑	3.4		3.8		3.8		
th	Hold time	SER after SRCLK↑	2		2		2		ns

[‡] This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

^{*} On products compliant to MIL-PRF-38535, this parameter is not production tested at $V_{CC} = 0 \text{ V}$. † This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or V_{CC} .

SCLS374L - MAY 1997 - REVISED FEBRUARY 2004

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (unless otherwise noted) (see Figure 1)

DADAMETER	FROM	то	LOAD	T,	չ = 25°C	;	SN54AH	CT595	SN74AH			
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT	
			C _L = 15 pF	135*	170*		115*		115		N 41 1-	
f _{max}			C _L = 50 pF	95	140		85		85		MHz	
t _{PLH}	DOLK	0 . 0 .	C. 15 pF		4.3*	7.4*	1*	8.5*	1	8.5	20	
^t PHL	RCLK	Q_A-Q_H	C _L = 15 pF		4.3*	7.4*	1*	8.5*	1	8.5	ns	
^t PLH	SDCI K	0	C. 15 pF		4.5*	8.2*	1*	9.4*	1	9.4	20	
^t PHL	SRCLK	Q _H ′	C _L = 15 pF		4.5*	8.2*	1*	9.4*	1	9.4	ns	
t _{PHL}	SRCLR	$Q_{H'}$	C _L = 15 pF		4.5*	8*	1*	9.1*	1	9.1	ns	
^t PZH	ŌĒ	0 0	C _L = 15 pF		4.3*	8.6*	1*	10*	1	10		
tPZL	OE	Q_A – Q_H			5.4*	8.6*	1*,	10*	1	10	ns	
tPLH .	BOLK	0 . 0	C. 50 pF		5.6	9.4	2	10.5	1	10.5	50	
^t PHL	RCLK	Q_A-Q_H	$C_L = 50 \text{ pF}$		5.6	9.4	Q _C	10.5	1	10.5	ns	
^t PLH	SRCLK	0	C 50 pF		6.4	10.2	2 1	11.4	1	11.4	ns	
^t PHL	SRULK	Q _H ′	C _L = 50 pF		6.4	10.2	1	11.4	1	11.4	115	
^t PHL	SRCLR	$Q_{H'}$	C _L = 50 pF		6.4	10	1	11.1	1	11.1	ns	
^t PZH			0 50 5		5.7	10.6	1	12	1	12		
tPZL	ŌE	Q_A – Q_H	C _L = 50 pF		6.8	10.6	1	12	1	12	ns	
^t PHZ	ŌĒ	0. 0. 0. 050.55	0 50 = 5	O		3.5	10.3	1	11	1	11	ns
t _{PLZ}	OE	Q _A –Q _H	$C_L = 50 pF$		3.4	10.3	1	11	1	11	115	

^{*} On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 4)

	DADAMETED	SN7	LINUT		
	PARAMETER	MIN	TYP	MAX	UNIT
VOL(P)	Quiet output, maximum dynamic VOL		1		V
V _{OL(V)}	Quiet output, minimum dynamic V _{OL}		-0.6		V
VOH(V)	Quiet output, minimum dynamic VOH		3.8		V
VIH(D)	High-level dynamic input voltage	2			V
V _{IL(D)}	Low-level dynamic input voltage			8.0	V

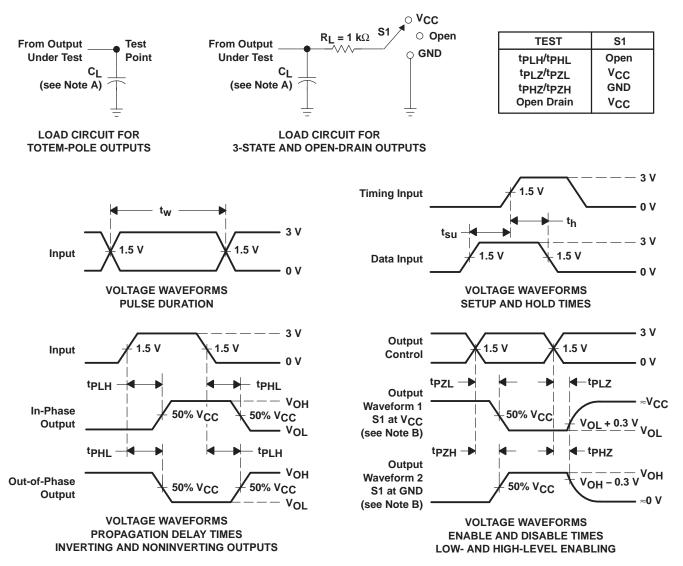
NOTE 4: Characteristics are for surface-mount packages only.

operating characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$

		PARAMETER	TEST CO	ONDITIONS	TYP	UNIT
ſ	C _{pd}	Power dissipation capacitance	No load,	f = 1 MHz	112	pF



PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_I includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_Q = 50 \Omega$, $t_f \leq 3$ ns, $t_f \leq 3$ ns.
- D. The outputs are measured one at a time, with one input transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms









PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74AHCT595D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT595DBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT595DBRE4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT595DBRG4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT595DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT595DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT595DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT595DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT595DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT595N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74AHCT595NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74AHCT595NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT595NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT595NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT595PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT595PWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT595PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT595PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT595PWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT595PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows: **ACTIVE:** Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available. **OBSOLETE:** TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.



PACKAGE OPTION ADDENDUM

18-Sep-2008

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

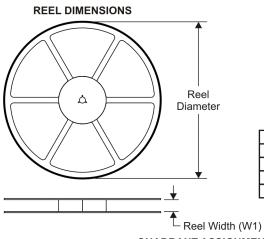
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

www.ti.com 30-Jul-2010

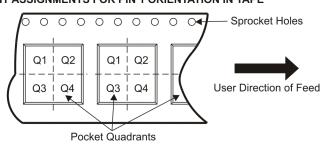
TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

All ulmensions are nominal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHCT595DBR	SSOP	DB	16	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN74AHCT595DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74AHCT595NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74AHCT595PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

www.ti.com 30-Jul-2010



*All dimensions are nominal

7 III GIITTOTTO GIO TIOTIMIGI								
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	
SN74AHCT595DBR	SSOP	DB	16	2000	346.0	346.0	33.0	
SN74AHCT595DR	SOIC	D	16	2500	333.2	345.9	28.6	
SN74AHCT595NSR	SO	NS	16	2000	346.0	346.0	33.0	
SN74AHCT595PWR	TSSOP	PW	16	2000	346.0	346.0	29.0	

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



D (R-PDS0-G16)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-150

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Audio	www.ti.com/audio	Communications and Telecom	www.ti.com/communications
Amplifiers	amplifier.ti.com	Computers and Peripherals	www.ti.com/computers
Data Converters	dataconverter.ti.com	Consumer Electronics	www.ti.com/consumer-apps
DLP® Products	www.dlp.com	Energy and Lighting	www.ti.com/energy
DSP	dsp.ti.com	Industrial	www.ti.com/industrial
Clocks and Timers	www.ti.com/clocks	Medical	www.ti.com/medical
Interface	interface.ti.com	Security	www.ti.com/security
Logic	logic.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Power Mgmt	power.ti.com	Transportation and Automotive	www.ti.com/automotive
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com	Wireless	www.ti.com/wireless-apps
RF/IF and ZigBee® Solutions	www.ti.com/lprf		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2011, Texas Instruments Incorporated

e2e.ti.com

TI E2E Community Home Page