Pre-Laboratory 5

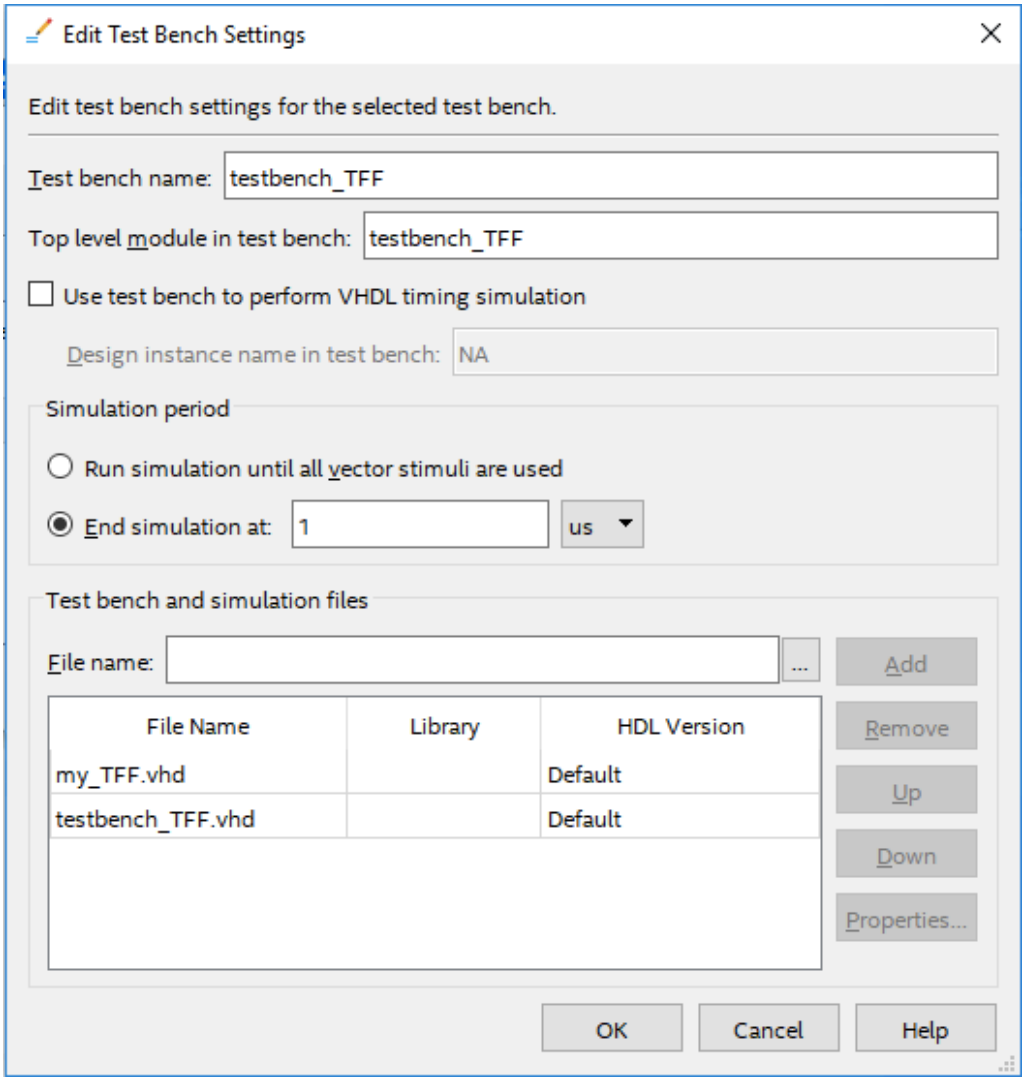
Counters

This is an exercise in using counters.

Part I

Create a Toggle flip-flop (see lecture notes). Use the template if you wish. Test this with the testbench_TFF

Note: set my_TFF.vhd when you compile. In test bench settings, include all the relevant files and run for 1 us. It should look like the following:



Part II

Consider the circuit in Figure 1. It is a 4-bit synchronous counter which uses four Toggle flip-flops (see lecture notes). The counter increments its count on each positive edge of the clock if the Enable signal is asserted. The counter is reset to 0 by using the (asynchronous) Reset (called CLEAR in diagram below) signal. You are to implement a 16-bit counter of this type.

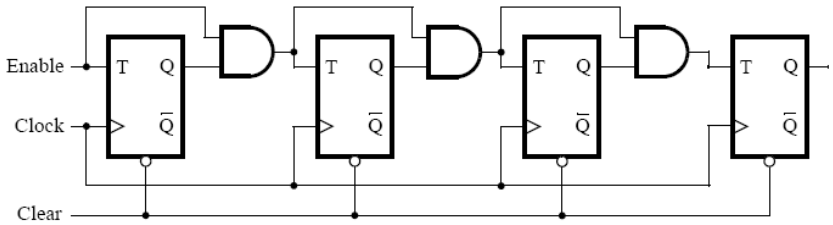


Figure 1. A 4-bit counter.

Write a VHDL file that defines a 16-bit counter by using the structure depicted in Figure 1, and compile the circuit. Use the template if you wish. Test this with the testbench_counter.vhd.

Note: set my_counter.vhd when you compile. In test bench settings, include all the relevant files and run for 1 us. It should look like the following: