12/04/14 10:07:18 /home/atmelfan/vhdl/C204/Seven_seg.vhd

```
 1  LIBRARY ieee ;
 2  USE ieee.std_logic_1164.all ;
 3  ENTITY bcd7seg IS
 4  PORT ( bcd : IN STD_LOGIC_VECTOR(3 downto 0) ;
 5  display : OUT STD_LOGIC_VECTOR(0 TO 6) ) ;
 6  END bcd7seg ;
 7  --   ___
 8  --  | 0 |
 9  -- 5|   | 1
10  --  |   |
11  --   ___
12  --  | 6 |
13  --- 4|   | 2
14  --  |   |
15  --   ___
16  --    3
17  ARCHITECTURE seven_seg OF bcd7seg IS
18  BEGIN
19      PROCESS ( bcd )
20      BEGIN
21          CASE bcd IS
22              WHEN x"0" =>
23                  display <= "0000001" ;
24              WHEN x"1" =>
25                  display <= "1001111" ;
26              WHEN x"2" =>
27                  display <= "0010010" ;
28              WHEN x"3" =>
29                  display <= "0000110" ;
30              WHEN x"4" =>
31                  display <= "1001100" ;
32              WHEN x"5" =>
33                  display <= "0100100" ;
34              WHEN x"6" =>
35                  display <= "1100000" ;
36              WHEN x"7" =>
37                  display <= "0001111" ;
38              WHEN x"8" =>
39                  display <= "0000000" ;
40              WHEN x"9" =>
41                  display <= "0001100" ;
42              WHEN x"A" =>
43                  display <= "0001000" ;
44              WHEN x"B" =>
45                  display <= "1100000" ;
46              WHEN x"C" =>
47                  display <= "0110001" ;
48              WHEN x"D" =>
49                  display <= "1000010" ;
50              WHEN x"E" =>
51                  display <= "0110000" ;
52              WHEN x"F" =>
53                  display <= "0111000" ;
54              WHEN OTHERS =>
55                  display <= "1111111" ;
56          END CASE ;
57      END PROCESS ;
58  END seven_seg ;
```