12/04/14 10:05:30 /home/atmelfan/vhdl/C204/decoder/decodey.vhd

```
 1  library ieee;
 2  use ieee.std_logic_1164.all;
 3
 4  entity decodey is
 5      port(
 6  --INSTRUCTIONz
 7      ins: in std_logic_vector(15 downto 0);
 8
 9  --select registrery
10      Asel: out std_logic_vector(3 downto 0);
11      Bsel: out std_logic_vector(3 downto 0);
12      muxsel: out std_logic; -- selects between A register and intermediate.
13
14  --Intermediate
15      Inter: out std_logic_vector(7 downto 0);
16
17      --operation
18      op: out std_logic_vector(3 downto 0)
19
20  );
21  end decodey;
22
23  architecture arch of decodey is
24  begin
25      --iccc_eeee_aaaa_bbbb
26      --c = op code
27      --e = extended op code or upper 4bit intermediate data if i=1
28      --a = A operand or lower 4bit intermediate if i=1
29      --b = B operand
30      Asel <= ins(7 downto 4);
31      Bsel <= ins(3 downto 0);
32      Inter <= ins(11 downto 4);
33      --If op = "0000" => op = eeee else op = 0ccc
34      op <= ins(11 downto 8) when ins(15 downto 12) = "0000" else "0"&ins(14 downto 12) ;
35
36      muxsel <= ins(15);
37  end arch;
```