12/04/14 10:01:51 /home/atmelfan/vhdl/C204/alu/alu.vhd

```
 1  library ieee;
 2  use ieee.std_logic_1164.all;
 3  use ieee.std_logic_unsigned.all;
 4
 5  entity alu is
 6      generic (
 7          WIDTH : integer := 8
 8      );
 9      port (
10          wr, skip: out std_logic;
11          OP: in std_logic_vector(3 downto 0);
12          A: in std_logic_vector(WIDTH-1 downto 0);
13          B: in std_logic_vector(WIDTH-1 downto 0);
14          C: out std_logic_vector(WIDTH-1 downto 0)
15      );
16  end entity ; -- alu
17
18  architecture arch of alu is
19  begin
20
21  process(OP, A, B)
22  begin
23      case OP is
24          --0x0, NOP
25          when x"0" =>
26              wr <= '0';
27              skip <= '0';
28              C <= (others => '0');
29          --0x1, ADD
30         when x"1" =>
31              wr <= '1';
32              skip <= '0';
33              C <= B + A;
34          --0x2, SUB
35          when x"2" =>
36              wr <= '1';
37              skip <= '0';
38              C <= B - A;
39          --0x3, AND
40          when x"3" =>
41             wr <= '1';
42              skip <= '0';
43              C <= B and A;
44          --0x4, OR
45          when x"4" =>
46              wr <= '1';
47              skip <= '0';
48              C <= B or A;
49          --0x5, XOR
50          when x"5" =>
51              wr <= '1';
52              skip <= '0';
53              C <= B xor A;
54          --0x6, MICKE
55          when x"6" =>
56              wr <= '1';
57              skip <= '0';
58              C <= A;
59          --0x7, SKNE
60          when x"7" =>
61              wr <= '0';
62              if(A = B) then
63                  skip <= '1';
64              else
65                  skip <= '0';
66              end if;
67              C <= (others => '0');
68          when others =>
69              wr <= '0';
70              skip <= '0';
71              C <= (others => '0');
72      end case;
73  end process;
74
75  end architecture ; -- arch
```