MODULE-1

1. Explain Basic binary logic gates with truth table and timing diagram.

2.Write the Verilog model for all basic gates.

3. Define the following a)Binary Logic b)Boolean Function c)Digital logic gates d)Truth table

4.List the theorems and properties of Boolean algebra.

5.Define K Map and Explain the procedure for four variable k map method with table.

6.Simplify the following Boolean function using K map

a) F(x,y,z)=∑(2,3,6,7)

b) F(w,x,y,z)=∑(2,3,12,13,14,15)

c) F(w,x,y,z)=∑(1,3,4,5,6,7,9,11,13,15)

d) F(A,B,C,D)=∑(3,7,11,13,14,15)

e) F(A,B,C,D)=∑(2,3,6,7,12,13,14)

f) w'z+xz+x'y+wx'z

g) ab'c+b'c'd'+bcd+acd'+a'b'c+a'bc'd

h)F(a,b,c,d) = ∑(0,6,8,13,14)+d(2,4,10)

i) F(a,b,c,d) = ∑(4,12,7,2,10)+d(0,6,8)

7.Implement the following Boolean function using NAND gates

a)Y=(AB+CD)EF

b)f(a,b,c,d)= ∑(0,1,2,5,6,7,8,9,10,13,14,15)

8. Implement the following Boolean function using NOR gates

a)Y=(A+B)(CD)(E+F)

b)f(a,b,c,d)= ∑(1,3,4,5,13,15)+ ∑d(8,9,10,11)

9.Define the following a)Hardware Description language(HDL) b)Port list c)Test Bench d)Instantiation e)Assign Statement

10.Explain the UDP With one Example

11.What is gate delay. Write gate level model with propagation delay.

12.Write a Verilog model for a simple circuit.

Y=(AB)+(CDE)

13. Explain the don't care condition with example

14.Explain Positive logic and negative logic.

Module-2

1. What is Combinational Logic Circuits? Explain the design procedure?
2. Explain the Design Procedure for the following
   a. Half Adder
   b. Full Adder
   c. Half Subtractor
   d. Full Subtractor
   e. 4-bit parallel adder
   f. 4-bit parallel subtractor
   g. 4-bit parallel adder/subtractor using exor gates
   h. Carry lookahead adder
3. Explain the design procedure for the following
   a. 2:1 MUX
   b. 4:1 MUX
   c. 8:1 MUX
   d. 3:8 Decoder
   e. 3:8 Decoder with enable
   f. 8:3 Priority Encoder
4. Using Structural model, write Verilog code for Half adder
5. Using Behavioural model, write Verilog code for full Subtractor
6. Using Behavioural model, write Verilog code for full Adder
7. Using Behavioural model, write Verilog code for Half Subtractor
8. Define the following
   a. Encoder
   b. Decoder
   c. Multiplexer
   d. Demultiplexer
9. Explain the importance of three state gates
10. Implement the following functions using 3:8 decoder
    F1(a,b,c)=∑m(0,4,6,7)
    F2(a,b,c)=∑m(1,4,5)
11. Implement the following function using 8:1 Mux
    F(a,b,c,d)=∑m(0,1,5,6,8,10,12,15)
12. Realize the following using 3:8 decoder
    (1) F(a,b,c)=∑m(1,2,3,4)
    (2) F(a,b,c)=∑m(3,5,7)
13. Write a verilog code for 4:1 MUX
14. Explain SR latch with NOR and NAND Gates.
15. Explain SR latch with Control input.
16. Explain D latch with Control input.
17. Derive the Characteristic Equations for the following.

a) SR Flip flop b) JK Flip flop c) D Flip flop d) T Flip flop

18. Explain the operation of following Flip flops.
    a) SR Flip flop b) JK Flip flop c) D Flip flop d) T Flip flop

19. Design a BCD to Excess 3 Code Converter

MODULE 3

1. Explain the functional units of computer with a diagram.
2. Explain the interconnection between memory and processor with a diagram.
3. Explain Single Bus Structure with a diagram.
4. Explain the Basic performance equation and performance measurement.
5. Differentiate between RISC and CISC Instruction set Architecture.
6. What is Byte addressability? Explain little Endian and Bid Endian byte address with a neat diagram.
7. Explain the basic instruction types with examples.
8. Explain the Condition code flag register.
9. What do you mean by Addressing mode? Explain any 5 addressing modes with example.
10. Describe the functionality of the following.
    a) MAR b) PC c) IR d) MDR e) ALU
11. Explain basic performance equation and SPEC rating?
12. Demonstrate a branching operation using a loop to add N numbers with neat block diagram.
13. The Registers R1 and R2 has decimal values 1200 and 4600. Calculate the effective address of the memory operand in each of the following instructions when they are executed in sequence.
    a) Load 20(R1),R5
    b) Move #3000,R5
    c) Store R5,30(R1,R2)
    d) Add –(R2),R5
    e) Subtract (R1)+,R5.
14. Demonstrate the Instruction execution and sequencing for C <----- [A]+[B] with block diagram
15. With relevant example explain the following modes of addressing
    a. Direct
    b. Register
    c. Index
    d. Base with Index and Offset
    e. Auto-increment
16. What are condition code flag. Mention the significance of the flags N, Z,V,C.
17. A program with 7000 machine instructions needs an average of 3 basic steps to execute one instruction . Find the Performance of the computer having a clock speed of 700KHz.