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CSC 211

## Project 1

$a[7:4] \backslash a[4:0]$	0000	0001	0011	0010	0110	0111	0101	0100	1100	1101	1111	1110	1010	1011	1001	1000
0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0001	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0011	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0010	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0110	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0111	0	0	0	0	0	0	0	0	1	1	1	1	0	1	0	0
0101	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0100	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1100	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1101	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1111	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1110	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1010	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1011	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1001	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

- This project keeps bits all bits and changes bit 5, in order to capitalize an ascii character. Non letters dont need to change.

- The sum of the terms can be:

1.  $a[7]a[5]$

4.  $na[7], a[6], a[5], a[4], a[3], na[2], a[1], a[0]$

2.  $na[7], na[6], a[5]$

5.  $na[7], a[5], na[4], na[3], na[2], na[1], na[0]$

3.  $na[7], a[6], a[5], a[4], a[3], na[2], a[1], a[0]$

- The sum of these can directly alter the 5<sup>th</sup> bit.

- Shown by the screenshots, the circuit takes 25ns to execute. Thus we need a 26ns delay to see the change.

- (base) apostolitsano@Apostolis-MacBook-Air-3 Project 1 % iverilog -o sim tb\_toUpper.v toUpper.v  
vvp sim  
VCD info: dumpfile toUpper.vcd opened for output.  
tb\_toUpper.v:53: \$finish called at 525000 (1ps)
- (base) apostolitsano@Apostolis-MacBook-Air-3 Project 1 % █

26ns







