Atsushi Koshiba

Postdoctoral researcher in Processsor Research Team,
RIKEN Center of Computational Science (R-CCS)

Nationality	Japan	**Address**	6-3-5 Minatojima-minami-macchi, Chuo-ku, Kobe, Hyogo
Date of Birth	16^{th} October 1991		
Membership	Member of ACM, IEEE, IPSJ	**Mobile Phone**	+8190 3451 8319
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Education

2016-2019 Ph.D. in Electronic and Information Engineering
Tokyo University of Agriculture and Technology, Tokyo, Japan
Supervisor: Mitaro Namiki

2014-2016 Master of Computer and Information Sciences
Tokyo University of Agriculture and Technology, Tokyo, Japan
Supervisor: Mitaro Namiki

2010-2014 Bachelor of Computer and Information Sciences
Tokyo University of Agriculture and Technology, Tokyo, Japan
Supervisor: Mitaro Namiki

Research Experience

Apr. 2019 - Present **Postdoctoral Researcher**
RIKEN Center for Computational Science, Hyogo, Japan

Engaged in a research concerned with high-performance computing with FPGAs.
Supervisors: Ying Yan and Yang Chen, Cloud & Mobile Research Group

Sep. 2017 - Jan. 2018 **Intern**
Microsoft Research Asia, Beijing, China

Engaged in a research concerned with Confidential Blockchain Framework.
Supervisors: Ying Yan and Yang Chen, Cloud & Mobile Research Group

Aug. 2016 - Mar. 2019 **Intern (Aug. 2016 - Sep. 2016) & Research Trainee (Apr.2017 - Mar. 2019)**
National Institute of Advance Industrial Science and Technology, Tsukuba, Japan

Engaged in a research concerned with an emulator for non-volatile memory.
Supervisor: Takahiro Hirofuchi

Apr. 2016 - Mar. 2019 **JSPS Research Fellow DC1**
Japan Society for the Promotion of Science, Japan

Engaged in a research concerned with parallel computing on heterogeneous SoCs.

Grants

Oct. 2019 - Mar. 2021 **Grant-in-Aid for Research Activity Start-up**
Japan Society for the Promotion of Science
2.2 Million JPY, acceptance rate: 37.7% (1,392/3,689 applicants)

Apr. 2016 - Mar. 2019 **Grant-in-Aid for JSPS Research Fellows**
Japan Society for the Promotion of Science
1.9 Million JPY, acceptance rate: 21.8% (727/3,341 applicants)

Awards and Honors

Jul. 2019 **Endorsement of Ph.D. thesis**
SIG-OS, IPSJ
My Ph.D. thesis was endorsed by an OS research community in Japan.

Jan. 2018 **Award of Excellence for Stars of Tomorrow Internship Program**
Cloud & Mobile research group, Microsoft Research Asia
given to selected students who made an outstanding contribution during the internship.

Mar. 2016 **Annual Best Research Award**
Department of Computer and Information Sciences, Tokyo University of Agriculture and Technology
One student who made most outstanding achievements was awarded out of 51 students.

Mar. 2015 **Annual Best Research Award**
Department of Computer and Information Sciences, Tokyo University of Agriculture and Technology
One student who made most outstanding achievements was awarded out of 51 students.

Research Interest

My research interest is in OS, middleware and HW/SW co-design to utilize emerging hardware for future computers (e.g., hardware accelerators, non-volatile memory, Intel SGX). I am currently working on a High-Level Synthesis (HLS) compiler and hardware abstraction layer (Shell) for efficient parallel computing on a large-scale FPGA cluster (Publication [4]). My past research projects are the followings:

(1) Light-weight software emulator for non-volatile memory (Publications [1], [6]):
Emulation tools of non-volatile memory (NVM) are widely used among researchers. However, existing tools are too slow to emulate large-scale workloads, or too simplistic to emulate the NVM read/write latency asymmetry. Our emulation model overcomes these issues by utilizing performance counters on cache controllers to estimate the number of cache misses that incur write-backs. Our model can emulate the write behavior of practical workloads more accurately than an existing emulation model.

(2) Secure immutable key-value store for Trusted Execution Environments (Publication [5]):
Trusted Execution Environments (TEEs) protects confidential apps/data running in them from any outside software including OS/VMMs. Microsoft Coco blockchain framework executes secret transactions (e.g., bank transfer) in TEEs to ensure their confidentiality/integrity, while placing a blockchain database in TEEs induces performance overhead and vulnerabilities due to limitations of TEEs (e.g., small memory size). We propose TEE-KV, a key-value store whose code is placed outside of TEEs and only a few functions are running in TEEs to verify data immutability. A prototype of TEE-KV is implemented with Intel SGX and achieves 15.1% codebase of LevelDB with 5% transaction overhead.

(3) OS-driven fine-grained power gating control for processors (Publications [2], [3]):
A processor equipped with fine-grained power gating (FGPG) saves the energy consumption by supplying power to its circuit blocks (e.g., ALU) only when they are in use. However, the energy overhead caused by switching power on/off may increase the total energy. We propose an OS process scheduler that monitors the usage of circuit blocks and disables FGPG of a block whose energy overhead is estimated to be high. Out scheduler reduces the power consumption of circuits by up to 17.2%.

(4) OS support for pipeline parallelism for heterogeneous accelerators (Publications [7]):
Pipeline processing with special-purpose accelerators improves performance of streaming applications, while traditional resource management via device drivers causes frequent user/kernel context switches that reduce the performance gain. We propose a kernel-level accelerator control model that a kernel module manages accelerators from the OS layer until all pipeline stages are done. Our model gets rid of the user/kernel interactions and improves the processing speed by up to 1.8x.

Selected Publications

Other publications are here: http://koshiba-cs.info/

International Journal (Referred)

[1] Atsushi Koshiba, Takahiro Hirofuchi, Ryousei Takano, and Mitaro Namiki: "A Software-based NVM Emulator Supporting Read/Write Asymmetric Latencies," IEICE TRANSACTIONS on Electronics, Vol.E102-D, No.12, pp.2377-2388, 2019.
[2] Atsushi Koshiba, Ryuichi Sakamoto, Mikiko Sato, Kimiyoshi Usami, Hideharu Amano, Masaaki Kondo, Hiroshi Nakamura, and Mitaro Namiki: "An Operating System Guided Fine-Grained Power Gating Control Based on Runtime Characteristics of Applications," IEICE TRANSACTIONS on Electronics, Vol.E99-C, No.8, pp.926-935, 2016.
[3] Atsushi Koshiba, Motoki Wada, Ryuichi Sakamoto, Mikiko Sato, Tsubasa Kosaka, Kimiyoshi Usami, Hideharu Amano, Masaaki Kondo, Hiroshi Nakamura, and Mitaro Namiki: "A Fine-grained Power Gating Control on Linux Monitoring Power Consumption of Processor Functional Units," IEICE TRANSACTIONS on Electronics, Vol.E98-C, No.7, pp.559-568, 2015.

International Conference (Referred)

[4] Atsushi Koshiba, Kouki Watanabe, Takaaki Miyajima, and Kentaro Sano: "Performance Evaluation and Power Analysis of Teraflop-scale Fluid Simulation with Stratix 10 FPGA," The 28th ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA 2020), poster, Feb. 2020.
[5] Atsushi Koshiba, Ying Yan, Zhongxin Guo, Mitaro Namiki, and Lidong Zhou: "TEE-KV: Secure Immutable Key-Value Store for Trusted Execution Environments," The ACM Symposium on Cloud Computing (SoCC 2018), poster, Oct. 2018.
[6] Atsushi Koshiba, Takahiro Hirofuchi, Soramichi Akiyama, Ryousei Takano, Mitaro Namiki: "Towards Write-back Aware Software Emulator for Non-Volatile Memory," The 6th IEEE Non-Volatile Memory Systems and Applications Symposium (NVMSA 2017), pp. 1-6, oral, Aug. 2017.
[7] Atsushi Koshiba, Ryuichi Sakamoto, Mitaro Namiki: "Operating System Support for Fine-grained Pipeline Parallelism on Heterogeneous Multicore Accelerators," The European Conference on Computer Systems (EuroSys'17), poster, Apr. 2017.

Other Experience

Dec. 2016 - Mar. 2017 **Research Assistant**
Tokyo University of Agriculture and Technology, Tokyo, Japan
Supervised an undergraduate student and reviewed his bachelor's degree thesis.

Apr. 2015 - Mar. 2016 **Part-time Software Engineer**
BUNNYHOP Inc.,
Engaged in developing embedded apps/OSes for IoT products.

Apr. 2014 - Feb. 2016 **Teaching Assistant for Undergraduate Students**
Tokyo University of Agriculture and Technology, Tokyo, Japan
Helped students with programming in C language.

Apr. 2014 - Sep. 2015 **Tutor for Foreign Students**
Tokyo University of Agriculture and Technology, Tokyo, Japan
Supervised two foreign students from China and Thailand.

Skills

- **Expertise**
  Operating systems, Linux device drivers, databases, Intel SGX, FPGA, embedded applications/OSes for ARM and MIPS, KVM/QEMU
- **Software Programming Skills**
  C/C++ (10+ years), Python, Java, JavaScript, shell script, x86/MIPS/ARM assembly
- **Hardware Development Skills**
  Verilog/SystemVerilog (5+ years), FPGA design tools (Vivado for Xilinx, Quartus Prime for Intel FPGA)
- **Platforms**
  Windows, Linux, Mac
- **Languages**
  Japanese (native), English (fluent, TOEIC Score 825/990 in Mar. 2016)

Scholarships

- **Scholarship Repayment Exemption Based on Outstanding Achievements**
  Sponsored by Japan Student Services Organization (Apr. 2015 - Mar. 2016)
- **Outstanding Student Scholarship**
  Sponsored by Tokyo University of Agriculture and Technology (Mar. 2015)