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Subject :- MDM (Digital Circuit)
Roll No :- 36EL

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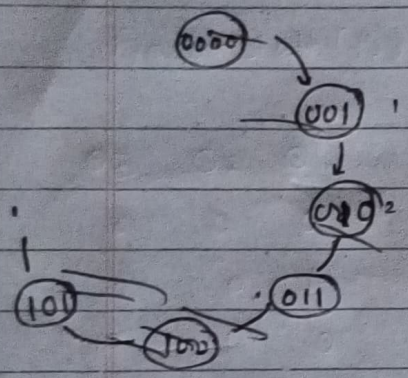
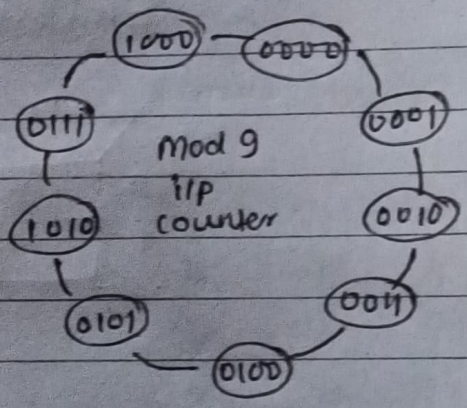
1. Design Mod 9 asynchronous counter?
2. Design mod 8 synchronous counter?

→ (1) Mod 9 asynchronous counter.

Mod 9 counts 9 stages.





After clk pulse	State				Reset (R) Reset (R)
	Q4	Q3	Q2	Q1	0
0	0	0	0	0	0
1	0	0	0	1	R = 0
2	0	0	1	0	0
3	0	0	1	1	0
4	0	1	0	0	0
5	0	1	0	1	0
6	1	0	1	0	0
7	0	1	1	1	0
8	1	0	0	0	0
9	1	0	0	1	R = 1

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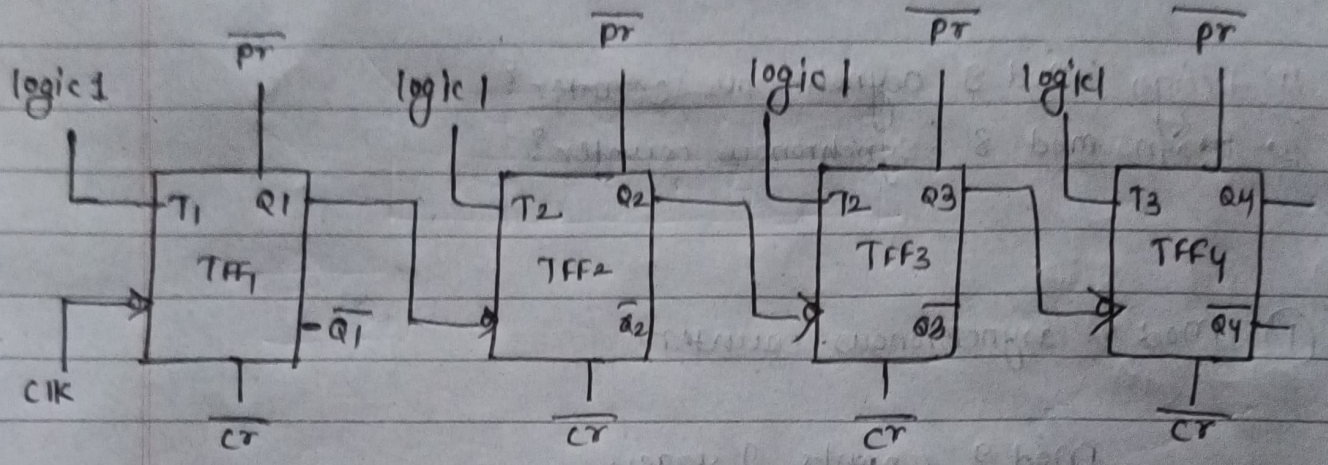
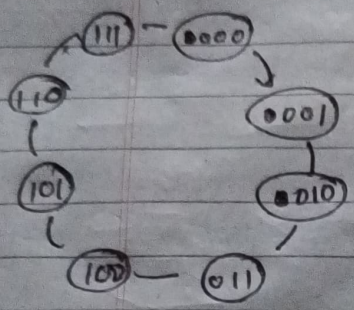


Q2. Mod 8 synchronous counter?



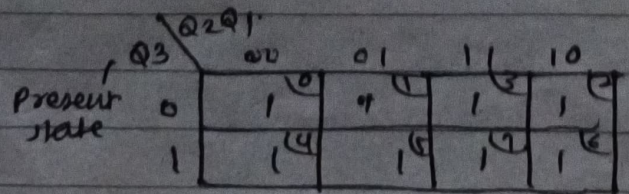
count 8 state

Present state (PS)			Next State (NS)			Require Excitation i/p		
Q3	Q2	Q1	Q3	Q2	Q1	T3	T2	T1
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	1	0	0	1
1	1	1	0	0	0	1	1	1

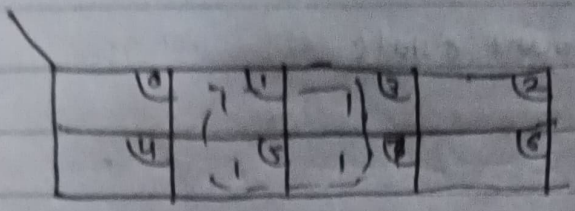
$T_1 = \Sigma m(0,1,2,3,4,5,6,7)$

$\boxed{T_1 = 1}$

Kmap for T_1

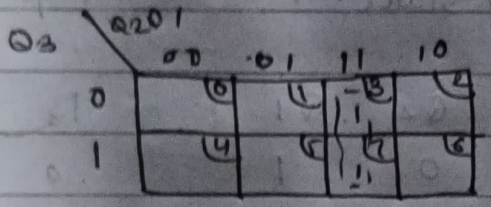


$T_2 = \Sigma m(1,3,5,7)$

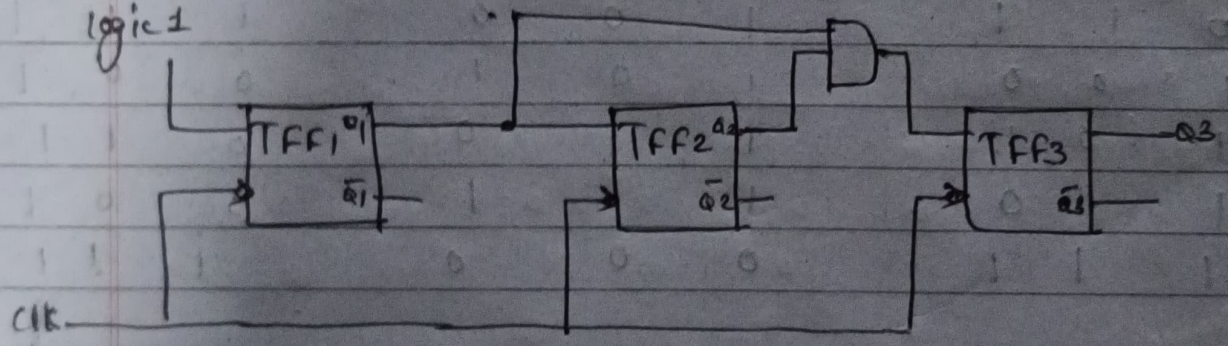


$T_2 = Q_1$

$T_3 = \Sigma m(3,7)$



$T_3 = Q_2 Q_1$



mod 8 synchronous counter