Jane Stephanie

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3A Computer Engineering
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Education

July 2011 **Master of Science in Integrated Hardware and Software Systems**, *University of Patras*, *9.5/10*.

July 2009 **Diploma in Electrical Engineering and Computer Science**, *University of Patras*, *6.92/10*.
3 years BSc(Eng) + 2 years MSc(Eng)

June 2002 **High School Diploma**, *19.2/20*.
First class honours and scholarship

Experience

Sep 2010 - Feb 2011 **IC Design Engineer**, *IMEC Netherlands*, Eindhoven.
Intern, working under minimum supervision, understanding and learning of EDA tools
DSP group meetings, conference calls and technical reports

Oct 2009 - Jun 2010 **Technical Assistant**, *University of Patras*, Patras.
Set up of laboratory equipment and experiments
Guidance and supervision of undergraduate students

Jul 2008 - Aug 2008 **Intern Student**, *Greek Public Power Corporation*, Patras.
Assistance work within the department of physical network expansion

Master Thesis

Title *Optimized SIMD scheduling and architecture exploration and implementation for ultra-low energy processor architectures*

Supervisors Francky Catthoor, Constantinos Goutis

Description Project follows the complete flow of the implementation of an ASIP from high-level processor architecture design and Test Vector generation process to power dissipation measurements

Bachelor Thesis

Title *Processor hardware implementation for Galois Counter Mode (GCM-AES) security encryption standard*

Supervisors Constantinos Goutis

Description Project based on VHDL design language; Hardware architecture design of an encryption algorithm; Validation using C programming and implementation on a Xilinx FPGA

Other Projects

Master projects

VHDL	Design and implementation of a multiply - add unit, Modeling using Octave, Testing in a Xilinx FPGA using a logic analyzer
VHDL	Architectural exploration of a LMS filter, Optimization for power, area and performance
C	Optimization of an edge - detection algorithm using compiler transformations
C	Implementation of a compression algorithm to reduce testing data
UPPAAL	Modeling and simulation of a Philips bus collision protocol

Bachelor Projects

VHDL	Implementation of Booth multiplier and MESI protocol
Assembly	Implementation of Virtual Mode for x86 processors
PSpice	Implementation of parallel multiplier based on Wallace tree adders
C	Development of a client management program implementing a hashing algorithm

Languages

Greek	**Native**	
English	**Fluent**	*ECPE Proficiency in English, University of Michigan, 2005*
French	**Basic**	*DELF A1, Ministere Francais de L'Education Nationale, 2000*

Computer skills

Basic	UML, HTML, C++, Tcl, System C
Intermediate	Matlab, Assembly(Intel x86)
Expert	C, VHDL, nML
Tools	Cadence, Xilinx, Target, UPPAAL, Simplescalar
Miscellaneous	Windows, Office, Linux

Qualities

Personal skills:	Good software engineering skills, strong analytical, problem-solving and communication skills, eager to learn and develop new skills
Experience with:	High level programming languages, RTL level development, digital design flow, validation and testing techniques, scripting languages, EDA tools, IS processors, SIMD and ultra-low power architectures
International Experience:	Lived in Eindhoven, The Netherlands for 6 months