```
1   library ieee ;
2   use ieee.std_logic_1164.all;
3
4   entity datapathMV is
5      port (clk_dmv , clr_total , ld_total: in std_logic;
6            S_mv, A_mv: in std_logic_vector(7 downto 0);
7            total_ld: out std_logic;
8            total_mv: out std_logic_vector(7 downto 0));
9   end datapathMV;
10
11  architecture ckt of datapathMV is
12     component Comparador_8Bits is
13       port (eA8,eB8: in std_logic_vector(7 downto 0);
14             AeqB8,AltB8,AgtB8: out std_logic);
15     end component;
16     component reg8Bits is
17        port (clk,preSet,clr,load: in std_logic;
18              d: in std_logic_vector(7 downto 0);
19              q : out std_logic_vector(7 downto 0));
20     end component;
21     component SUM_8Bits is
22          port (A8_in,B8_in: in std_logic_vector(7 downto 0);
23                C8_in: in std_logic;
24                S8_out: out std_logic_vector(7 downto 0);
25                C8_out: out std_logic);
26     end component;
27
28     signal result_somador, result_tot: std_logic_vector(7 downto 0);
29     signal lixo_sum, result_comp_lt: std_logic;
30     signal lixo_comp: std_logic_vector(1 downto 0);
31     begin
32        Reg: reg8Bits port map(
33           clk => clk_dmv,
34           preSet => '1',
35           clr => not clr_total,
36           load => ld_total,
37           d => result_somador,
38           q => result_tot);
39
40        SUM: SUM_8Bits port map(
41           A8_in => result_tot,
42           B8_in => A_mv,
43           C8_in => '0',
44           S8_out => result_somador,
45           C8_out => lixo_sum);
46
47        Comp: Comparador_8Bits port map(
48           eA8 => result_tot,
49           eB8 => S_mv,
50           AeqB8 => lixo_comp(1),
51           AltB8 => result_comp_lt,
52           AgtB8 =>lixo_comp(0));
53
54        total_mv <= result_tot;
55        total_ld <= result_comp_lt;
56  end ckt ;
```