```
1  library ieee;
2  use ieee.std_logic_1164 .all;
3
4  entity blocoDeControleFIFO is
5     port (clk_ff , rst_ff, rd_ff, wr_ff: in std_logic;
6           equal_cont_wd_e_rd, equal_cont_wd_1_e_rd, equal_cont_wd_e_rd_1: in std_logic;
7           led_vazio_ff, led_cheio_ff,load_wr,load_rd, clr_ff: out std_logic;
8           saida_mv_fifo: out std_logic_vector(2 downto 0));
9  end blocoDeControleFIFO;
10
11 architecture ckt of blocoDeControleFIFO is
12    type st is (start, p_leitura, escrita, p_escrita, leitura);
13    signal estado : st;
14    signal p_l,p_e: std_logic;
15    begin
16       process (clk_ff , rst_ff)
17       begin
18          if rst_ff = '1' then
19             estado <= start ;
20          elsif (clk_ff'event and clk_ff ='1') then
21             case estado is
22                when start =>
23                   estado <= p_leitura;
24                when p_leitura =>
25                   if (equal_cont_wd_e_rd='0') and (rd_ff ='1') and (wr_ff ='0') then
   estado <= leitura;
26                   elsif (wr_ff='1') then estado <= escrita;
27                   else estado <= p_leitura;
28                   end if;
29                when escrita =>
30                   if equal_cont_wd_1_e_rd='1' then estado <= p_escrita;
31                   elsif (wr_ff='1') and (rd_ff='0') then estado <= escrita;
32                   else estado <= p_escrita;
33                   end if;
34                when p_escrita =>
35                   if (equal_cont_wd_e_rd='0') and (wr_ff ='1') and (rd_ff='0') then estado
    <= escrita;
36                   elsif (rd_ff='1') then estado <= leitura;
37                   else estado <= p_escrita;
38                   end if;
39                when leitura =>
40                   if equal_cont_wd_e_rd_1='1' then estado <= p_leitura;
41                   elsif (wr_ff='0') and (rd_ff='1') then estado <= leitura;
42                   else estado <= p_leitura;
43                   end if;
44             end case ;
45          end if;
46       end process;
47       clr_ff <= '1' when estado = start else '0';
48       load_wr <= '1' when estado = escrita else '0';
49       load_rd <= '1' when estado = leitura else '0';
50       p_e <= '1' when estado = p_escrita else '0';
51       p_l <= '1' when estado = p_leitura else '0';
52
53       led_vazio_ff <= p_l and equal_cont_wd_e_rd;
54       led_cheio_ff <= p_e and equal_cont_wd_e_rd;
55
56       with estado select
57          saida_mv_fifo <= "000" when start ,
58          "001" when p_leitura,
59          "010" when escrita,
60          "011" when p_escrita,
61          "100" when leitura;
62 end ckt ;
```