```
1
                    library ieee;
                    use ieee.std logic 1164.all;
                   entity ciBitToBcd is
    4
    5
                    port (BtB in: in bit vector(3 downto 0);
    6
                                                     BtB out: out bit vector(3 downto 0));
    7
                    end ciBitToBcd;
  8
  9
                     architecture ckt of ciBitToBcd is
10
                   begin
11
                       BtB_out(3) \le (BtB_in(3) \text{ or } (BtB_in(2) \text{ and } (BtB_in(1) \text{ or } BtB_in(0))));
12
                         BtB out(2) <= ((BtB in(2) and (not BtB in(1)) and (not BtB in(0))) or (BtB in(3) and
13
                       BtB_out(1) \le ((BtB_in(3) and (not BtB_in(0))) or (BtB_in(1) and ((not BtB_in(2)) or (BtB_in(1))) or (BtB_in(1)) and ((not BtB_in(2))) or (BtB_in(1)) and ((not BtB_in(2))) or (BtB_in(1)) and ((not BtB_in(2))) or ((not 
                     BtB in(0)));
                       BtB out(0) <= (((not BtB in(3)) and (not BtB in(2)) and BtB in(0)) or ((not BtB in(0))
14
                     and (BtB_in(3) or (BtB_in(2) and BtB_in(1))));
15
                     end ckt;
16
```