```
1   library ieee ;
2   use ieee.std_logic_1164.all;
3
4   entity maquinaVendas is
5      port (CLK_mv, C, reset: in std_logic;
6            S, A: in std_logic_vector(7 downto 0);
7            D: out std_logic;
8            saida_mv: out std_logic_vector(1 downto 0);
9            Tot_mv: out std_logic_vector(7 downto 0));
10  end maquinaVendas;
11
12  architecture ckt of maquinaVendas is
13     component blocoDeControleMV is
14        port (clk_mv , rst_mv , c_mv, tot_ld: in std_logic ;
15              d_mv, load_tot, clr_tot: out std_logic;
16              saida: out std_logic_vector(1 downto 0));
17     end component;
18     component datapathMV is
19        port (clk_dmv , clr_total , ld_total: in std_logic;
20              S_mv, A_mv: in std_logic_vector(7 downto 0);
21              total_ld: out std_logic;
22              total_mv: out std_logic_vector(7 downto 0));
23     end component;
24
25     signal result_total: std_logic_vector(7 downto 0);
26     signal result_comp_lt, result_despacho, sinal_somar_tot, clear_tot: std_logic;
27     signal saida_mc: std_logic_vector(1 downto 0);
28     begin
29        BlocodeControle: blocoDeControleMV port map(
30           clk_mv => CLK_mv,
31           rst_mv => reset,
32           c_mv => C,
33           tot_ld => result_comp_lt,
34           d_mv => result_despacho,
35           load_tot => sinal_somar_tot,
36           clr_tot => clear_tot,
37           saida => saida_mc);
38
39        Datapath: datapathMV port map(
40           clk_dmv => CLK_mv,
41           clr_total => clear_tot,
42           ld_total => sinal_somar_tot,
43           S_mv => S,
44           A_mv => A,
45           total_ld => result_comp_lt,
46           total_mv => result_total);
47
48        D <= result_despacho;
49        Tot_mv <= result_total;
50        saida_mv <= saida_mc;
51  end ckt ;
```