```
1   library ieee;
2   use ieee.std_logic_1164.all;
3
4   entity SUM_2Bits is
5     port (A2_in,B2_in: in std_logic_vector(1 downto 0);
6           C2_in: in std_logic;
7           S2_out: out std_logic_vector(1 downto 0);
8           C2_out: out std_logic);
9   end SUM_2Bits;
10
11  architecture ckt of SUM_2Bits is
12    component SUM_1Bit is
13      port (A_in,B_in,C_in: in std_logic;
14            S_out, C_out: out std_logic);
15    end component;
16
17    signal Sum_01_out : std_logic;
18
19    begin
20      SUM01: SUM_1Bit port map(
21            A_in => A2_in(0),
22            B_in => B2_in(0),
23            C_in => C2_in,
24            S_out => S2_out(0),
25            C_out => Sum_01_out);
26
27      SUM02: SUM_1Bit port map(
28            A_in => A2_in(1),
29            B_in => B2_in(1),
30            C_in => Sum_01_out,
31            S_out => S2_out(1),
32            C_out => C2_out);
33
34  end ckt;
```