```
1   library ieee ;
2   use ieee.std_logic_1164.all;
3
4   entity decodificador1X16 is
5     port (ld_dec: in std_logic;
6           i_in: in std_logic_vector(3 downto 0);
7           d_out: out std_logic_vector(15 downto 0));
8   end decodificador1X16;
9
10  architecture ckt of decodificador1X16 is
11    begin
12      d_out(0) <= (not (i_in(3))) and (not(i_in(2))) and (not (i_in(1))) and (not(i_in(0)))
    and ld_dec;
13      d_out(1) <= (not (i_in(3))) and (not(i_in(2))) and (not (i_in(1))) and     (i_in(0))
    and ld_dec;
14      d_out(2) <= (not (i_in(3))) and (not(i_in(2))) and      (i_in(1)) and  (not(i_in(0)))
    and ld_dec;
15      d_out(3) <= (not (i_in(3))) and (not(i_in(2))) and      (i_in(1)) and      (i_in(0))
    and ld_dec;
16      d_out(4) <= (not (i_in(3))) and     (i_in(2)) and  (not (i_in(1))) and (not(i_in(0)))
    and ld_dec;
17      d_out(5) <= (not (i_in(3))) and     (i_in(2)) and  (not (i_in(1))) and     (i_in(0))
    and ld_dec;
18      d_out(6) <= (not (i_in(3))) and     (i_in(2)) and       (i_in(1)) and  (not(i_in(0)))
    and ld_dec;
19      d_out(7) <= (not (i_in(3))) and     (i_in(2)) and       (i_in(1)) and      (i_in(0))
    and ld_dec;
20      d_out(8) <=      (i_in(3)) and (not(i_in(2))) and  (not (i_in(1))) and (not(i_in(0)))
    and ld_dec;
21      d_out(9) <=      (i_in(3)) and (not(i_in(2))) and  (not (i_in(1))) and     (i_in(0))
    and ld_dec;
22      d_out(10) <=     (i_in(3)) and (not(i_in(2))) and       (i_in(1)) and  (not(i_in(0)))
    and ld_dec;
23      d_out(11) <=     (i_in(3)) and (not(i_in(2))) and       (i_in(1)) and      (i_in(0))
    and ld_dec;
24      d_out(12) <=     (i_in(3)) and     (i_in(2)) and   (not (i_in(1))) and (not(i_in(0)))
    and ld_dec;
25      d_out(13) <=     (i_in(3)) and     (i_in(2)) and   (not (i_in(1))) and     (i_in(0))
    and ld_dec;
26      d_out(14) <=     (i_in(3)) and     (i_in(2)) and       (i_in(1)) and  (not(i_in(0)))
    and ld_dec;
27      d_out(15) <=     (i_in(3)) and     (i_in(2)) and       (i_in(1)) and      (i_in(0))
    and ld_dec;
28
29  end ckt;
```