```
1  -- megafunction wizard: %ROM: 1-PORT%
2  -- GENERATION: STANDARD
3  -- VERSION: WM1.0
4  -- MODULE: altsyncram
5
6  -- ============================================================
7  -- File Name: romFIFO.vhd
8  -- Megafunction Name(s):
9  --          altsyncram
10 --
11 -- Simulation Library Files(s):
12 --          altera_mf
13 -- ============================================================
14 -- ************************************************************
15 -- THIS IS A WIZARD-GENERATED FILE. DO NOT EDIT THIS FILE!
16 --
17 -- 13.0.0 Build 156 04/24/2013 SJ Web Edition
18 -- ************************************************************
19
20
21 --Copyright (C) 1991-2013 Altera Corporation
22 --Your use of Altera Corporation's design tools, logic functions
23 --and other software and tools, and its AMPP partner logic
24 --functions, and any output files from any of the foregoing
25 --(including device programming or simulation files), and any
26 --associated documentation or information are expressly subject
27 --to the terms and conditions of the Altera Program License
28 --Subscription Agreement, Altera MegaCore Function License
29 --Agreement, or other applicable license agreement, including,
30 --without limitation, that your use is for the sole purpose of
31 --programming logic devices manufactured by Altera and sold by
32 --Altera or its authorized distributors.  Please refer to the
33 --applicable agreement for further details.
34
35
36 LIBRARY ieee;
37 USE ieee.std_logic_1164.all;
38
39 LIBRARY altera_mf;
40 USE altera_mf.all;
41
42 ENTITY romFIFO IS
43    PORT
44    (
45       address     : IN STD_LOGIC_VECTOR (5 DOWNTO 0);
46       clock    : IN STD_LOGIC  := '1';
47       q     : OUT STD_LOGIC_VECTOR (12 DOWNTO 0)
48    );
49 END romFIFO;
50
51
52 ARCHITECTURE SYN OF romfifo IS
53
54    SIGNAL sub_wire0  : STD_LOGIC_VECTOR (12 DOWNTO 0);
55
56
57
58    COMPONENT altsyncram
59    GENERIC (
60       clock_enable_input_a    : STRING;
61       clock_enable_output_a      : STRING;
62       init_file      : STRING;
63       intended_device_family     : STRING;
64       lpm_hint    : STRING;
65       lpm_type    : STRING;
66       numwords_a     : NATURAL;
```

```
67          operation_mode    : STRING;
68          outdata_aclr_a    : STRING;
69          outdata_reg_a     : STRING;
70          widthad_a       : NATURAL;
71          width_a     : NATURAL;
72          width_byteena_a       : NATURAL
73       );
74       PORT (
75             address_a   : IN STD_LOGIC_VECTOR (5 DOWNTO 0);
76             clock0   : IN STD_LOGIC ;
77             q_a   : OUT STD_LOGIC_VECTOR (12 DOWNTO 0)
78       );
79       END COMPONENT;
80
81    BEGIN
82       q    <= sub_wire0(12 DOWNTO 0);
83
84       altsyncram_component : altsyncram
85       GENERIC MAP (
86          clock_enable_input_a => "BYPASS",
87          clock_enable_output_a => "BYPASS",
88          init_file => "romFIFO.mif",
89          intended_device_family => "Cyclone II",
90          lpm_hint => "ENABLE_RUNTIME_MOD=NO",
91          lpm_type => "altsyncram",
92          numwords_a => 64,
93          operation_mode => "ROM",
94          outdata_aclr_a => "NONE",
95          outdata_reg_a => "UNREGISTERED",
96          widthad_a => 6,
97          width_a => 13,
98          width_byteena_a => 1
99       )
100      PORT MAP (
101         address_a => address,
102         clock0 => clock,
103         q_a => sub_wire0
104      );
105
106
107
108   END SYN;
109
110   -- ============================================================
111   -- CNX file retrieval info
112   -- ============================================================
113   -- Retrieval info: PRIVATE: ADDRESSSTALL_A NUMERIC "0"
114   -- Retrieval info: PRIVATE: AclrAddr NUMERIC "0"
115   -- Retrieval info: PRIVATE: AclrByte NUMERIC "0"
116   -- Retrieval info: PRIVATE: AclrOutput NUMERIC "0"
117   -- Retrieval info: PRIVATE: BYTE_ENABLE NUMERIC "0"
118   -- Retrieval info: PRIVATE: BYTE_SIZE NUMERIC "8"
119   -- Retrieval info: PRIVATE: BlankMemory NUMERIC "0"
120   -- Retrieval info: PRIVATE: CLOCK_ENABLE_INPUT_A NUMERIC "0"
121   -- Retrieval info: PRIVATE: CLOCK_ENABLE_OUTPUT_A NUMERIC "0"
122   -- Retrieval info: PRIVATE: Clken NUMERIC "0"
123   -- Retrieval info: PRIVATE: IMPLEMENT_IN_LES NUMERIC "0"
124   -- Retrieval info: PRIVATE: INIT_FILE_LAYOUT STRING "PORT_A"
125   -- Retrieval info: PRIVATE: INIT_TO_SIM_X NUMERIC "0"
126   -- Retrieval info: PRIVATE: INTENDED_DEVICE_FAMILY STRING "Cyclone II"
127   -- Retrieval info: PRIVATE: JTAG_ENABLED NUMERIC "0"
128   -- Retrieval info: PRIVATE: JTAG_ID STRING "NONE"
129   -- Retrieval info: PRIVATE: MAXIMUM_DEPTH NUMERIC "0"
130   -- Retrieval info: PRIVATE: MIFfilename STRING "romFIFO.mif"
131   -- Retrieval info: PRIVATE: NUMWORDS_A NUMERIC "64"
132   -- Retrieval info: PRIVATE: RAM_BLOCK_TYPE NUMERIC "0"
```

```
133   -- Retrieval info: PRIVATE: RegAddr NUMERIC "1"
134   -- Retrieval info: PRIVATE: RegOutput NUMERIC "0"
135   -- Retrieval info: PRIVATE: SYNTH_WRAPPER_GEN_POSTFIX STRING "0"
136   -- Retrieval info: PRIVATE: SingleClock NUMERIC "1"
137   -- Retrieval info: PRIVATE: UseDQRAM NUMERIC "0"
138   -- Retrieval info: PRIVATE: WidthAddr NUMERIC "6"
139   -- Retrieval info: PRIVATE: WidthData NUMERIC "13"
140   -- Retrieval info: PRIVATE: rden NUMERIC "0"
141   -- Retrieval info: LIBRARY: altera_mf altera_mf.altera_mf_components.all
142   -- Retrieval info: CONSTANT: CLOCK_ENABLE_INPUT_A STRING "BYPASS"
143   -- Retrieval info: CONSTANT: CLOCK_ENABLE_OUTPUT_A STRING "BYPASS"
144   -- Retrieval info: CONSTANT: INIT_FILE STRING "romFIFO.mif"
145   -- Retrieval info: CONSTANT: INTENDED_DEVICE_FAMILY STRING "Cyclone II"
146   -- Retrieval info: CONSTANT: LPM_HINT STRING "ENABLE_RUNTIME_MOD=NO"
147   -- Retrieval info: CONSTANT: LPM_TYPE STRING "altsyncram"
148   -- Retrieval info: CONSTANT: NUMWORDS_A NUMERIC "64"
149   -- Retrieval info: CONSTANT: OPERATION_MODE STRING "ROM"
150   -- Retrieval info: CONSTANT: OUTDATA_ACLR_A STRING "NONE"
151   -- Retrieval info: CONSTANT: OUTDATA_REG_A STRING "UNREGISTERED"
152   -- Retrieval info: CONSTANT: WIDTHAD_A NUMERIC "6"
153   -- Retrieval info: CONSTANT: WIDTH_A NUMERIC "13"
154   -- Retrieval info: CONSTANT: WIDTH_BYTEENA_A NUMERIC "1"
155   -- Retrieval info: USED_PORT: address 0 0 6 0 INPUT NODEFVAL "address[5..0]"
156   -- Retrieval info: USED_PORT: clock 0 0 0 0 INPUT VCC "clock"
157   -- Retrieval info: USED_PORT: q 0 0 13 0 OUTPUT NODEFVAL "q[12..0]"
158   -- Retrieval info: CONNECT: @address_a 0 0 6 0 address 0 0 6 0
159   -- Retrieval info: CONNECT: @clock0 0 0 0 0 clock 0 0 0 0
160   -- Retrieval info: CONNECT: q 0 0 13 0 @q_a 0 0 13 0
161   -- Retrieval info: GEN_FILE: TYPE_NORMAL romFIFO.vhd TRUE
162   -- Retrieval info: GEN_FILE: TYPE_NORMAL romFIFO.inc FALSE
163   -- Retrieval info: GEN_FILE: TYPE_NORMAL romFIFO.cmp FALSE
164   -- Retrieval info: GEN_FILE: TYPE_NORMAL romFIFO.bsf FALSE
165   -- Retrieval info: GEN_FILE: TYPE_NORMAL romFIFO_inst.vhd FALSE
166   -- Retrieval info: LIB_FILE: altera_mf
167
```