```
1   library ieee ;
2   use ieee.std_logic_1164.all;
3
4   entity datapathFIFO is
5     port (wr_data_dp: in std_logic_vector(12 downto 0);
6           ld_wr_dp, ld_rd_dp, clr_fifo_dp, clk_fifo_dp: in std_logic;
7           eq_comp_wr_rd,eq_comp_wr1_rd,eq_comp_wr_rd1: out std_logic;
8           rd_data_dp: out std_logic_vector(12 downto 0));
9   end datapathFIFO;
10
11  architecture ckt of datapathFIFO is
12     component bancoDeRegistrador16X13 is
13       port (wr_data: in std_logic_vector(12 downto 0);
14             cont_wr,cont_rd: in std_logic_vector(3 downto 0);
15             clk_br, ld_wr, ld_rd, clr_reg: in std_logic;
16             rd_data: out std_logic_vector(12 downto 0));
17     end component;
18
19     component Comparador_4Bits is
20       port (eA,eB: in std_logic_vector(3 downto 0);
21             gt,lt,eq: in std_logic;
22             AeqB,AltB,AgtB: out std_logic);
23     end component;
24
25     component contador4Bits is
26       port ( clk_c4B,ld_c4B,clr_c4B: in std_logic;
27              out_c4B: out std_logic_vector(3 downto 0));
28     end component;
29
30     component SUM_4Bits is
31       port (A4_in,B4_in: in std_logic_vector(3 downto 0);
32             C4_in: in std_logic;
33             S4_out: out std_logic_vector(3 downto 0);
34             C4_out: out std_logic);
35     end component;
36
37     signal saida_cont_wr, saida_cont_rd: std_logic_vector(3 downto 0);
38     signal saida_sum_wr, saida_sum_rd: std_logic_vector(3 downto 0);
39     signal saida_bancoRegistradores: std_logic_vector(12 downto 0);
40     signal clr_reverso_reg: std_logic;
41     signal lixo: std_logic_vector(1 downto 0);
42     signal saida_eq_comparador_wd_com_rd, saida_ld_comparador_wd_com_rd,
    saida_gt_comparador_wd_com_rd: std_logic;
43     signal saida_eq_comparador_wd1_com_rd, saida_ld_comparador_wd1_com_rd,
    saida_gt_comparador_wd1_com_rd: std_logic;
44     signal saida_eq_comparador_wd_com_rd1, saida_ld_comparador_wd_com_rd1,
    saida_gt_comparador_wd_com_rd1: std_logic;
45
46     begin
47
48        clr_reverso_reg <= not clr_fifo_dp;
49
50        BancoDeRegistradores: bancoDeRegistrador16X13 port map(
51           wr_data => wr_data_dp,
52           cont_wr => saida_cont_wr,
53           cont_rd => saida_cont_rd,
54           clk_br => clk_fifo_dp,
55           ld_wr => ld_wr_dp,
56           ld_rd => ld_rd_dp,
57           clr_reg => clr_reverso_reg,
58           rd_data => saida_bancoRegistradores);
59
60        Contador_WR: contador4Bits port map(
61           clk_c4B => clk_fifo_dp,
62           ld_c4B => ld_wr_dp,
63           clr_c4B => clr_fifo_dp,
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64            out_c4B => saida_cont_wr);
65
66         Contador_RD: contador4Bits port map(
67            clk_c4B => clk_fifo_dp,
68            ld_c4B => ld_rd_dp,
69            clr_c4B => clr_fifo_dp,
70            out_c4B => saida_cont_rd);
71
72         comparador_wr_com_rd: Comparador_4Bits port map(
73            eA => saida_cont_wr,
74            eB => saida_cont_rd,
75            gt => '0',
76            lt => '0',
77            eq => '1',
78            AeqB => saida_eq_comparador_wd_com_rd,
79            AltB => saida_ld_comparador_wd_com_rd,
80            AgtB => saida_gt_comparador_wd_com_rd);
81
82         comparador_wr1_com_rd: Comparador_4Bits port map(
83            eA => saida_sum_wr,
84            eB => saida_cont_rd,
85            gt => '0',
86            lt => '0',
87            eq => '1',
88            AeqB => saida_eq_comparador_wd1_com_rd,
89            AltB => saida_ld_comparador_wd1_com_rd,
90            AgtB => saida_gt_comparador_wd1_com_rd);
91
92         comparador_wr_com_rd1: Comparador_4Bits port map(
93            eA => saida_cont_wr,
94            eB => saida_sum_rd,
95            gt => '0',
96            lt => '0',
97            eq => '1',
98            AeqB => saida_eq_comparador_wd_com_rd1,
99            AltB => saida_ld_comparador_wd_com_rd1,
100           AgtB => saida_gt_comparador_wd_com_rd1);
101
102        somador_wr1: SUM_4Bits port map(
103           A4_in => saida_cont_wr,
104           B4_in => "0001",
105           C4_in => '0',
106           S4_out => saida_sum_wr,
107           C4_out => lixo(0));
108
109        somador_rd1: SUM_4Bits port map(
110           A4_in => saida_cont_rd,
111           B4_in => "0001",
112           C4_in => '0',
113           S4_out => saida_sum_rd,
114           C4_out => lixo(1));
115
116
117        rd_data_dp <= saida_bancoRegistradores;
118        eq_comp_wr_rd <= saida_eq_comparador_wd_com_rd;
119        eq_comp_wr1_rd <= saida_eq_comparador_wd1_com_rd;
120        eq_comp_wr_rd1 <= saida_eq_comparador_wd_com_rd1;
121
122  end ckt;
```