```
1   library ieee ;
2   use ieee.std_logic_1164.all;
3   entity divisorClock is
4      port ( clk_in : in std_logic ;
5             clk_out : out std_logic );
6   end divisorClock ;
7   architecture ckt of divisorClock is
8      signal ax : std_logic ;
9      begin
10        process ( clk_in )
11           variable cnt: integer range 0 to 13500000 := 0;
12           begin
13              if ( rising_edge ( clk_in )) then
14                 if (cnt =13500000) then
15                    cnt := 0;
16                    ax <= not ax;
17                 else
18                    cnt := cnt +1;
19                 end if;
20              end if;
21        end process ;
22        clk_out <= ax;
23  end ckt;
```