```
1
     library ieee ;
    use ieee.std_logic_1164.all;
    entity divisorClock is
 3
 4
       port ( clk_in : in std_logic ;
 5
               clk out : out std logic );
 6 end divisorClock;
 7 architecture ckt of divisorClock is
8
       signal ax : std_logic ;
9
       begin
10
          process ( clk_in )
11
             variable cnt: integer range 0 to 13500000 := 0;
12
             begin
13
                if ( rising edge ( clk in )) then
14
                    if (cnt = 13500000) then
15
                       cnt := 0;
16
                       ax <= not ax;</pre>
17
18
                       cnt := cnt +1;
19
                    end if;
20
                 end if;
21
          end process;
22
          clk_out <= ax;
23 end ckt;
```