```
1   library ieee ;
2   use ieee.std_logic_1164.all;
3
4   entity Comparador_4Bits is
5     port (eA,eB: in std_logic_vector(3 downto 0);
6           gt,lt,eq: in std_logic;
7           AeqB,AltB,AgtB: out std_logic);
8   end Comparador_4Bits;
9
10  architecture ckt of Comparador_4Bits is
11
12    component Comparador is
13      port (in_gt, in_eq, in_lt,a,b: in std_logic;
14            out_eq,out_lt,out_gt: out std_logic);
15     end component;
16
17    signal saida_gt,saida_lt,saida_eq:std_logic_vector(3 downto 0);
18    begin
19    Comp1:Comparador port map(
20          in_gt => gt,
21          in_lt => lt,
22          in_eq => eq,
23          a => eA(3),
24          b => eB(3),
25          out_eq => saida_eq(3),
26          out_gt => saida_gt(3),
27          out_lt => saida_lt(3));
28
29    Comp2:Comparador port map(
30          in_gt => saida_gt(3),
31          in_lt => saida_lt(3),
32          in_eq => saida_eq(3),
33          a => eA(2),
34          b => eB(2),
35          out_eq => saida_eq(2),
36          out_gt => saida_gt(2),
37          out_lt => saida_lt(2));
38
39    Comp3:Comparador port map(
40          in_gt => saida_gt(2),
41          in_lt => saida_lt(2),
42          in_eq => saida_eq(2),
43          a => eA(1),
44          b => eB(1),
45          out_eq => saida_eq(1),
46          out_gt => saida_gt(1),
47          out_lt => saida_lt(1));
48
49    Comp4:Comparador port map(
50          in_gt => saida_gt(1),
51          in_lt => saida_lt(1),
52          in_eq => saida_eq(1),
53          a => eA(0),
54          b => eB(0),
55          out_eq => saida_eq(0),
56          out_gt => saida_gt(0),
57          out_lt => saida_lt(0));
58
59    AeqB <= saida_eq(0);
60    AltB <= saida_lt(0);
61    AgtB <= saida_gt(0);
62  end ckt;
63
64
65
```