```
1   library ieee ;
2   use ieee.std_logic_1164.all;
3
4   entity projeto02 is
5      port ( clock_27,SW1,SW0,KEY3: in std_logic ;
6             LEDR1,LEDR0: out std_logic;
7             P02HEX5,P02HEX4, P02HEX3, P02HEX2, P02HEX1, P02HEX0: out std_logic_vector(6
    downto 0);
8             est_maq_fifo: out std_logic_vector(2 downto 0));
9   end projeto02;
10
11  architecture ckt of projeto02 is
12     -- Divisor de Clock
13     component divisorClock is
14        port (clk_in : in std_logic ;
15              clk_out : out std_logic );
16     end component;
17
18     -- ROM
19     component romFIFO is
20        PORT (address: IN STD_LOGIC_VECTOR (5 DOWNTO 0);
21              clock: IN STD_LOGIC  := '1';
22              q: OUT STD_LOGIC_VECTOR (12 DOWNTO 0));
23     end component;
24
25     --FIFO
26     component fifo is
27        port (CLK_fifo, WR, RD, reset: in std_logic;
28              W_data: in std_logic_vector(12 downto 0);
29              em,fu: out std_logic;
30              R_data: out std_logic_vector(12 downto 0);
31              Estados_maquina: out std_logic_vector(2 downto 0));
32     end component;
33
34     --Contador
35     component contador6Bits is
36       port ( clk_c6B,ld_c6B,clr_c6B: in std_logic;
37              out_c6B: out std_logic_vector(5 downto 0));
38     end component;
39
40     --BINBCDtoD7SEG
41     component bitToBcd13bitsToD7Seg is
42       port (SW_in: in std_logic_vector(12 downto 0);
43             HEX0,HEX1,HEX2,HEX3: out std_logic_vector(6 downto 0));
44     end component;
45
46     signal CLK_1, led_full, led_empty, clr_reverso: std_logic;
47     signal saida_rom, saida_fifo: std_logic_vector(12 downto 0);
48     signal saida_contador: std_logic_vector(5 downto 0);
49     signal lixo1,lixo0, hx00,hx01,hx02,hx03,hx04,hx05: std_logic_vector(6 downto 0);
50     signal estados: std_logic_vector(2 downto 0);
51
52     begin
53
54        clr_reverso <= not KEY3;
55
56        DClock: divisorClock port map(
57           clk_in => clock_27,
58           clk_out => CLK_1);
59
60        FIFO16x13: fifo port map(
61           CLK_fifo => CLK_1,
62           WR => SW1,
63           RD => SW0,
64           reset => clr_reverso,
65           W_data => saida_rom,
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```
66            em => led_empty,
67            fu => led_full,
68            R_data => saida_fifo,
69            Estados_maquina => estados);
70
71         ROM: romFIFO port map(
72            address => saida_contador,
73            clock => CLK_1,
74            q => saida_rom);
75
76         Contador: contador6Bits port map(
77            clk_c6B => CLK_1,
78            ld_c6B => SW1,
79            clr_c6B => clr_reverso,
80            out_c6B => saida_contador);
81
82         DisplayRead: bitToBcd13bitsToD7Seg port map(
83            SW_in => saida_fifo,
84            HEX0 => hx00,
85            HEX1 => hx01,
86            HEX2 => hx02,
87            HEX3 => hx03);
88
89         DisplayContador: bitToBcd13bitsToD7Seg port map(
90            SW_in(12 downto 6) =>"0000000",
91            SW_in(5 downto 0) => saida_contador,
92            HEX0 => hx04,
93            HEX1 => hx05,
94            HEX2 => lixo0,
95            HEX3 => lixo1);
96
97         -- HEX
98         P02HEX0 <= hx00;
99         P02HEX1 <= hx01;
100        P02HEX2 <= hx02;
101        P02HEX3 <= hx03;
102        P02HEX4 <= hx04;
103        P02HEX5 <= hx05;
104
105        -- Estados da Maquina FIFO
106        est_maq_fifo <= estados;
107
108        -- Luzes de aviso
109        LEDR0 <= led_full;
110        LEDR1 <= led_empty;
111  end ckt;
```