```
1   library ieee;
2   use ieee.std_logic_1164.all;
3
4   entity SUM_4Bits is
5     port (A4_in,B4_in: in std_logic_vector(3 downto 0);
6           C4_in: in std_logic;
7           S4_out: out std_logic_vector(3 downto 0);
8           C4_out: out std_logic);
9   end SUM_4Bits;
10
11  architecture ckt of SUM_4Bits is
12    component SUM_2Bits is
13      port (A2_in,B2_in: in std_logic_vector(1 downto 0);
14            C2_in: in std_logic;
15            S2_out: out std_logic_vector(1 downto 0);
16            C2_out: out std_logic);
17    end component;
18
19    signal Sum_01_out : std_logic;
20
21    begin
22      SUM01: SUM_2Bits port map(
23            A2_in => A4_in(1 downto 0),
24            B2_in => B4_in(1 downto 0),
25            C2_in => C4_in,
26            S2_out => S4_out(1 downto 0),
27            C2_out => Sum_01_out);
28
29      SUM02: SUM_2Bits port map(
30            A2_in => A4_in(3 downto 2),
31            B2_in => B4_in(3 downto 2),
32            C2_in => Sum_01_out,
33            S2_out => S4_out(3 downto 2),
34            C2_out => C4_out);
35
36  end ckt;
```

```
1   library ieee;
2   use ieee.std_logic_1164.all;
3
4   entity SUM_2Bits is
5     port (A2_in,B2_in: in std_logic_vector(1 downto 0);
6           C2_in: in std_logic;
7           S2_out: out std_logic_vector(1 downto 0);
8           C2_out: out std_logic);
9   end SUM_2Bits;
10
11  architecture ckt of SUM_2Bits is
12    component SUM_1Bit is
13      port (A_in,B_in,C_in: in std_logic;
14            S_out, C_out: out std_logic);
15    end component;
16
17    signal Sum_01_out : std_logic;
18
19    begin
20      SUM01: SUM_1Bit port map(
21            A_in => A2_in(0),
22            B_in => B2_in(0),
23            C_in => C2_in,
24            S_out => S2_out(0),
25            C_out => Sum_01_out);
26
27      SUM02: SUM_1Bit port map(
28            A_in => A2_in(1),
29            B_in => B2_in(1),
30            C_in => Sum_01_out,
31            S_out => S2_out(1),
32            C_out => C2_out);
33
34  end ckt;
```

```
1   library ieee;
2   use ieee.std_logic_1164.all;
3
4   entity SUM_1Bit is
5     port (A_in,B_in,C_in: in std_logic;
6           S_out, C_out: out std_logic);
7   end SUM_1Bit;
8
9   Architecture ckt of SUM_1Bit is
10
11  Begin
12    S_out <= ((B_in and ((C_in nor A_in) or (C_in and A_in))) or ((not B_in) and (((not C_in
    ) and A_in) or (C_in and (not A_in)))));
13    C_out <= ((C_in and (A_in or B_in)) or (A_in and B_in));
14  end ckt;
```