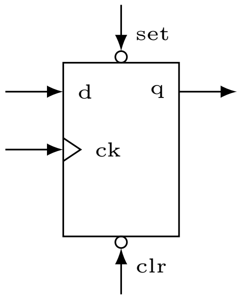
Universidade Federal do Rio Grande do Norte
Centro de Tecnologia - CT
Departamento de Engenharia Elétrica - DEE

Disciplina: ELE1717 - Sistemas Digitais
Curso: Engenharia Mecatrônica

Material de suporte - Flip-Flop D



```vhdl
library ieee;
use ieee.std_logic_1164.all;

entity ffd is
   port (ck, clr, set, d : in  std_logic;
                       q : out std_logic);
end ffd;

architecture logica of ffd is

begin
   process(ck, clr, set)
   begin
      if    (set = '0')            then q <= '1';
      elsif (clr = '0')            then q <= '0';
      elsif (ck'event and ck ='1') then q <= d;
      end if;
   end process;
end logica;
```

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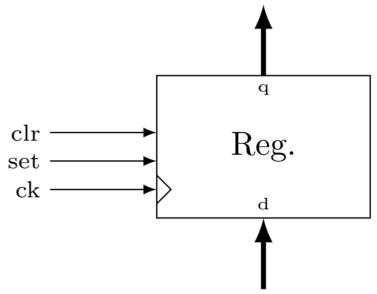
Material de suporte - Registrador de 3 bits com entradas síncronas



```
library ieee;
use ieee.std_logic_1164.all;

entity reg3bs is
  port (ck, clr, set : in  std_logic;
                   d : in  std_logic_vector(2 downto 0);
                   q : out std_logic_vector(2 downto 0));
end reg3bs;

architecture logica of reg3bs is

begin
  process (ck)
  begin
    if (ck’event and ck = ’1’) then        -- condicao do sinal relogio
      if    (clr = ’1’) then q <= "000";  -- teste para levar q=000
      elsif (set = ’1’) then q <= "111";  -- teste para levar q=111
      else                   q <= d;      -- armazena dado
      end if;
    end if;
  end process;
end logica;
```

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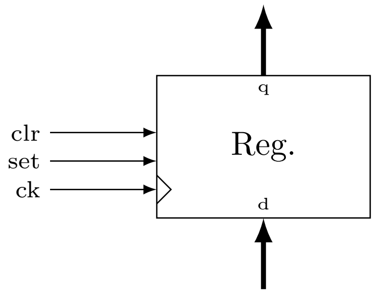
Material de suporte - Registrador de 3 bits com entradas assíncronas



```
library ieee;
use ieee.std_logic_1164.all;

entity reg3ba is
  port (ck, clr, set : in  std_logic;
                   d : in  std_logic_vector(2 downto 0);
                   q : out std_logic_vector(2 downto 0));
end reg3ba;

architecture logica of reg3ba is

begin
  process (ck, clr, set)
  begin
    if    (clr = '1')             then q <="000"; -- q=000 independente de ck
    elsif (set = '1')             then q <="111"; -- q=111 independente de ck
    elsif (ck'event and ck ='1') then q <=d;      -- condicao do sinal relogio
    end if;
  end process;
end logica;
```

Disciplina: ELE1717 - Sistemas Digitais
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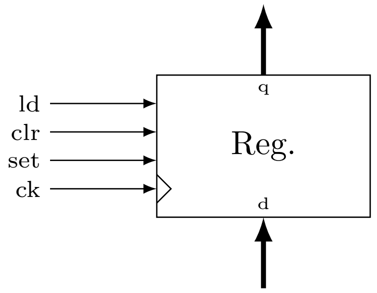
Material de suporte - Registrador de 3 bits com entradas assíncronas e habilitador



```
library ieee;
use ieee.std_logic_1164.all;

entity reg3ba_en is
  port (ck, clr, set, ld : in  std_logic;
                       d : in  std_logic_vector(2 downto 0);
                       q : out std_logic_vector(2 downto 0));
end reg3ba_en;

architecture logica of reg3ba_en is

begin
  process (ck, clr, set)
  begin
    if    (clr = ’1’) then q <= "000";    -- q=000 independente de ck
    elsif (set = ’1’) then q <= "111";    -- q=111 independente de ck
    elsif (ck’event and ck = ’1’) then    -- detecta borda de ck
      if  (ld = ’1’) then q <= d;         -- verifica habilitacao
      end if;
    end if;
  end process;
end logica;
```

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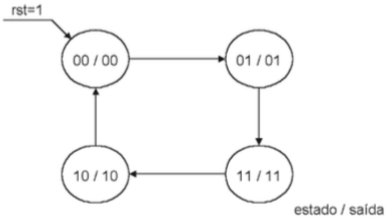
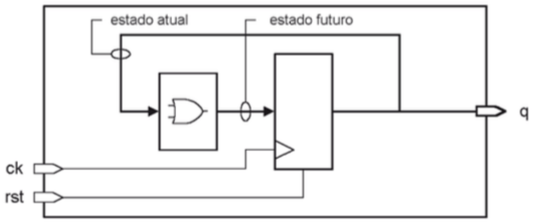
Material de suporte - MDE sequencial





```
use ieee.std_logic_1164.all;

entity mde is
   port (ck, rst : in  std_logic;
         q       : out std_logic);
end mde;

architecture logica of mde is

begin
  process (ck, rst)
  begin
    if rst = '1' then                     -- estado inicial
      q <= "00";
    elsif (ck'event and ck ='1') then     -- ciclo de estados
      case q is
        when "00" => q <= "01";
        when "01" => q <= "11";
        when "11" => q <= "10";
        when "10" => q <= "00";
       end case;
    end if;
  end process;
end logica;
```

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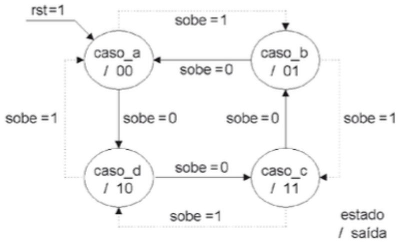
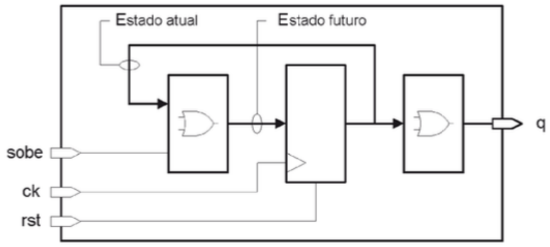
Material de suporte - MDE do tipo Moore com um processo





```
use ieee.std_logic_1164.all;

entity mde is
   port (ck, rst, sobe : in  std_logic;
                      q : out std_logic);
end mde;

architecture logica of mde is
  type st is (caso_d, caso_c, caso_b, caso_a);
  signal estado : st;

begin
  process (ck, rst)
  begin
    if rst = ’1’ then
      estado <= caso_a;
    elsif (ck’event and ck =’1’) then
      case estado is
        when caso_a =>
          if sobe = ’1’ then estado <= caso_b;
          else               estado <= caso_d;
          end if;
        when caso_b =>
          if sobe = ’1’ then estado <= caso_c;
          else               estado <= caso_a;
          end if;
        when caso_c =>
          if sobe = ’1’ then estado <= caso_d;
          else               estado <= caso_b;
          end if;
        when caso_d =>
          if sobe = ’1’ then estado <= caso_a;
          else               estado <= caso_c;
          end if;
       end case;
    end if;
  end process;

  with estado select
    q <= "00" when caso_a,
         "01" when caso_b,
         "11" when caso_c,
         "10" when caso_d;
end logica;
```

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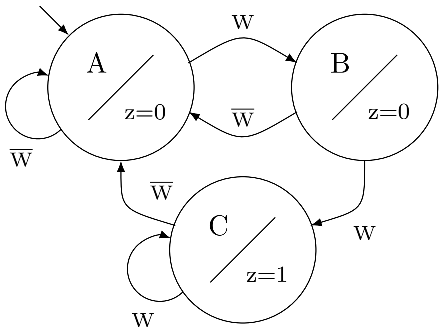
Material de suporte - MDE do tipo Moore com dois processos



```
library ieee;
use ieee.std_logic_1164.all;

entity mde_b is
   port (ck, rst, w : in  std_logic;
                  z : out std_logic);
end mde_b;

architecture logica of mde_b is
   type state_type is (a, b, c);
   signal y_present, y_next : state_type;

begin
   process (w, y_present)
   begin
      case y_present is
         when a =>
            if w = '0' then y_next <= a;
            else            y_next <= b; end if;
         when b =>
            if w = '0' then y_next <= a;
            else            y_next <= c; end if;
         when c =>
            if w = '0' then y_next <= a;
            else            y_next <= c; end if;
      end case;
   end process;

   process (ck, rst)
   begin
      if rst = '0' then
         y_present <= a;
      elsif (ck'event and ck = '1') then
         y_present <= y_next;
      end if;
   end process;

   z <= '1' when y_present = c else '0';
end logica;
```

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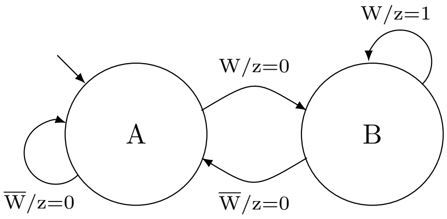
Material de suporte - MDE do tipo Mealy



```vhdl
library ieee;
use ieee.std_logic_1164.all;

entity mde_d is
    port (ck, rst, w : in std_logic;
                   z : out std_logic);
end mde_d;

architecture logica of mde_d is
  type state_type is (a, b);
  signal y : state_type;

begin
  process (rst, ck)
  begin
   if rst = '0' then
     y <= a;
   elsif (ck'event and ck = '1') then
     case y is
       when a =>
         if w = '0' then y<=a;
         else            y<=b; end if;
       when b =>
         if w = '0' then y<=a;
         else            y<=b; end if;
     end case;
   end if;
  end process;

  process (y, w)
    begin
      case y is
        when a => z <= '0';
        when b => z <= w;
      end case;
  end process;
end logica;
```

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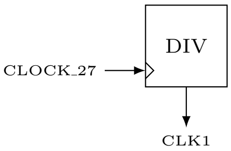
Material de suporte - Divisor de Clock



```
library ieee;
use ieee.std_logic_1164.all;

entity CLK_Div is
   port (clk_in : in  std_logic;
         clk_out: out std_logic);
end CLK_Div;

architecture logica of CLK_Div is
signal ax : std_logic;

begin
   process(clk_in)
      variable cnt: integer range 0 to 13500000 := 0;
   begin
      if (rising_edge(clk_in)) then
         if (cnt=13500000) then
            cnt:=0;
            ax <= not ax;
         else
            cnt:=cnt+1;
         end if;
      end if;
   end process;
   clk_out<=ax;
end logica;
```