```
1   library ieee ;
2   use ieee.std_logic_1164.all;
3
4   entity fifo is
5      port (CLK_fifo, WR, RD, reset: in std_logic;
6            W_data: in std_logic_vector(12 downto 0);
7            em,fu: out std_logic;
8            R_data: out std_logic_vector(12 downto 0);
9            Estados_maquina: out std_logic_vector(2 downto 0));
10  end fifo;
11
12  architecture ckt of fifo is
13
14     component blocoDeControleFIFO is
15        port (clk_ff, rst_ff, rd_ff, wr_ff: in std_logic;
16              equal_cont_wd_e_rd, equal_cont_wd_1_e_rd, equal_cont_wd_e_rd_1: in std_logic;
17              led_vazio_ff, led_cheio_ff,load_wr,load_rd,clr_ff: out std_logic;
18              saida_mv_fifo: out std_logic_vector(2 downto 0));
19     end component;
20
21     component datapathFIFO is
22       port (wr_data_dp: in std_logic_vector(12 downto 0);
23             ld_wr_dp, ld_rd_dp, clr_fifo_dp, clk_fifo_dp: in std_logic;
24             eq_comp_wr_rd,eq_comp_wr1_rd,eq_comp_wr_rd1: out std_logic;
25             rd_data_dp: out std_logic_vector(12 downto 0));
26     end component;
27
28
29     signal leitura_banco_registradores: std_logic_vector(12 downto 0);
30     signal l_vazio, l_cheio, saida_load_wr, saida_load_rd, clr_dt : std_logic;
31     signal saida_eq_cont_wr_rd, saida_eq_cont_wr1_rd, saida_eq_cont_wr_rd1: std_logic;
32     signal saida_fifo: std_logic_vector(2 downto 0);
33
34     begin
35        BlocodeControle: blocoDeControleFIFO port map(
36           clk_ff => CLK_fifo,
37           rst_ff => reset,
38           rd_ff => RD,
39           wr_ff => WR,
40           equal_cont_wd_e_rd => saida_eq_cont_wr_rd,
41           equal_cont_wd_1_e_rd => saida_eq_cont_wr1_rd,
42           equal_cont_wd_e_rd_1 => saida_eq_cont_wr_rd1,
43           led_vazio_ff => l_vazio,
44           led_cheio_ff => l_cheio,
45           load_wr => saida_load_wr,
46           load_rd => saida_load_rd,
47           clr_ff => clr_dt,
48           saida_mv_fifo => saida_fifo);
49
50        Datapath: datapathFIFO port map(
51           clk_fifo_dp => CLK_fifo,
52           wr_data_dp => W_data,
53           ld_wr_dp => saida_load_wr,
54           ld_rd_dp => saida_load_rd,
55           clr_fifo_dp => clr_dt,
56           eq_comp_wr_rd => saida_eq_cont_wr_rd,
57           eq_comp_wr1_rd => saida_eq_cont_wr1_rd,
58           eq_comp_wr_rd1 => saida_eq_cont_wr_rd1,
59           rd_data_dp => leitura_banco_registradores);
60
61
62
63        R_data <= leitura_banco_registradores;
64        em <= l_vazio;
65        fu <= l_cheio;
66        Estados_maquina <= saida_fifo;
```

```
67
68    end ckt ;
```