```
1   library ieee ;
2   use ieee.std_logic_1164.all;
3
4   entity MUX16_1_13Bits is
5     port (I15_16, I14_16, I13_16, I12_16, I11_16, I10_16, I9_16, I8_16, I7_16:
    std_logic_vector(12 downto 0);
6           I6_16, I5_16, I4_16, I3_16, I2_16, I1_16, I0_16: std_logic_vector(12 downto 0);
7           S_16: in std_logic_vector(3 downto 0);
8           ld_mux_16: in std_logic;
9           d_16: out std_logic_vector(12 downto 0));
10  end MUX16_1_13Bits;
11
12  Architecture ckt of MUX16_1_13Bits is
13    component MUX2_1_13Bits is
14      port (I_1,I_0: in std_logic_vector(12 downto 0);
15            S,ld_mux: in std_logic;
16            d: out std_logic_vector(12 downto 0));
17    end component;
18
19    signal saida_i0i1, saida_i2i3, saida_i4i5, saida_i6i7, saida_i8i9, saida_i10i11,
    saida_i12i13, saida_i14i15 : std_logic_vector(12 downto 0);
20    signal saida_S0102, saida_S0304, saida_S0506, saida_S0708 : std_logic_vector(12 downto 0
    );
21    signal saida_SS0102, saida_SS0304, saida_final : std_logic_vector(12 downto 0);
22
23    begin
24        muxI0I1: MUX2_1_13Bits port map(
25                 I_1 => I1_16,
26                 I_0 => I0_16,
27                 S => S_16(0),
28                 ld_mux => ld_mux_16,
29                 d => saida_i0i1);
30
31        muxI2I3: MUX2_1_13Bits port map(
32                 I_1 => I3_16,
33                 I_0 => I2_16,
34                 S => S_16(0),
35                 ld_mux => ld_mux_16,
36                 d => saida_i2i3);
37
38        muxI4I5: MUX2_1_13Bits port map(
39                 I_1 => I5_16,
40                 I_0 => I4_16,
41                 S => S_16(0),
42                 ld_mux => ld_mux_16,
43                 d => saida_i4i5);
44
45        muxI6I7: MUX2_1_13Bits port map(
46                 I_1 => I7_16,
47                 I_0 => I6_16,
48                 S => S_16(0),
49                 ld_mux => ld_mux_16,
50                 d => saida_i6i7);
51
52        muxI8I9: MUX2_1_13Bits port map(
53                 I_1 => I9_16,
54                 I_0 => I8_16,
55                 S => S_16(0),
56                 ld_mux => ld_mux_16,
57                 d => saida_i8i9);
58
59        muxI10I11: MUX2_1_13Bits port map(
60                 I_1 => I11_16,
61                 I_0 => I10_16,
62                 S => S_16(0),
63                 ld_mux => ld_mux_16,
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64                d => saida_i10i11);
65
66          muxI12I13: MUX2_1_13Bits port map(
67                I_1 => I13_16,
68                I_0 => I12_16,
69                S => S_16(0),
70                ld_mux => ld_mux_16,
71                d => saida_i12i13);
72
73          muxI14I15: MUX2_1_13Bits port map(
74                I_1 => I15_16,
75                I_0 => I14_16,
76                S => S_16(0),
77                ld_mux => ld_mux_16,
78                d => saida_i14i15);
79
80          muxSaida0102: MUX2_1_13Bits port map(
81                I_1 => saida_i2i3,
82                I_0 => saida_i0i1,
83                S => S_16(1),
84                ld_mux => ld_mux_16,
85                d => saida_S0102);
86
87          muxSaida0304: MUX2_1_13Bits port map(
88                I_1 => saida_i6i7,
89                I_0 => saida_i4i5,
90                S => S_16(1),
91                ld_mux => ld_mux_16,
92                d => saida_S0304);
93
94          muxSaida0506: MUX2_1_13Bits port map(
95                I_1 => saida_i10i11,
96                I_0 => saida_i8i9,
97                S => S_16(1),
98                ld_mux => ld_mux_16,
99                d => saida_S0506);
100
101         muxSaida0708: MUX2_1_13Bits port map(
102               I_1 => saida_i14i15,
103               I_0 => saida_i12i13,
104               S => S_16(1),
105               ld_mux => ld_mux_16,
106               d => saida_S0708);
107
108         muxSSaida0102: MUX2_1_13Bits port map(
109               I_1 => saida_S0304,
110               I_0 => saida_S0102,
111               S => S_16(2),
112               ld_mux => ld_mux_16,
113               d => saida_SS0102);
114
115         muxSSaida0304: MUX2_1_13Bits port map(
116               I_1 => saida_S0708,
117               I_0 => saida_S0506,
118               S => S_16(2),
119               ld_mux => ld_mux_16,
120               d => saida_SS0304);
121         muxFinal: MUX2_1_13Bits port map(
122               I_1 => saida_SS0304,
123               I_0 => saida_SS0102,
124               S => S_16(3),
125               ld_mux => ld_mux_16,
126               d => saida_final);
127
128
129         d_16 <= saida_final;
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130   end ckt;
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```
1   library ieee ;
2   use ieee.std_logic_1164.all;
3
4   entity MUX2_1_13Bits is
5     port (I_1,I_0: std_logic_vector(12 downto 0);
6           S, ld_mux: in std_logic;
7           d: out std_logic_vector(12 downto 0));
8   end MUX2_1_13Bits;
9
10  Architecture ckt of MUX2_1_13Bits is
11
12  Begin
13    d(0) <= ((((not S) and I_0(0)) or (S and I_1(0)))) and ld_mux;
14    d(1) <= ((((not S) and I_0(1)) or (S and I_1(1)))) and ld_mux;
15    d(2) <= ((((not S) and I_0(2)) or (S and I_1(2)))) and ld_mux;
16    d(3) <= ((((not S) and I_0(3)) or (S and I_1(3)))) and ld_mux;
17    d(4) <= ((((not S) and I_0(4)) or (S and I_1(4)))) and ld_mux;
18    d(5) <= ((((not S) and I_0(5)) or (S and I_1(5)))) and ld_mux;
19    d(6) <= ((((not S) and I_0(6)) or (S and I_1(6)))) and ld_mux;
20    d(7) <= ((((not S) and I_0(7)) or (S and I_1(7)))) and ld_mux;
21    d(8) <= ((((not S) and I_0(8)) or (S and I_1(8)))) and ld_mux;
22    d(9) <= ((((not S) and I_0(9)) or (S and I_1(9)))) and ld_mux;
23    d(10) <= ((((not S) and I_0(10)) or (S and I_1(10)))) and ld_mux;
24    d(11) <= ((((not S) and I_0(11)) or (S and I_1(11)))) and ld_mux;
25    d(12) <= ((((not S) and I_0(12)) or (S and I_1(12)))) and ld_mux;
26
27  end ckt;
```