```
1   library ieee;
2   use ieee.std_logic_1164.all;
3
4   entity SUM_1Bit is
5     port (A_in,B_in,C_in: in std_logic;
6           S_out, C_out: out std_logic);
7   end SUM_1Bit;
8
9   Architecture ckt of SUM_1Bit is
10
11  Begin
12    S_out <= ((B_in and ((C_in nor A_in) or (C_in and A_in))) or ((not B_in) and (((not C_in
    ) and A_in) or (C_in and (not A_in)))));
13    C_out <= ((C_in and (A_in or B_in)) or (A_in and B_in));
14  end ckt;
```