```
1   library ieee ;
2   use ieee.std_logic_1164.all;
3
4   entity bancoDeRegistrador16X13 is
5     port (wr_data: in std_logic_vector(12 downto 0);
6           cont_wr,cont_rd: in std_logic_vector(3 downto 0);
7           clk_br, ld_wr, ld_rd, clr_reg: in std_logic;
8           rd_data: out std_logic_vector(12 downto 0));
9   end bancoDeRegistrador16X13;
10
11  architecture ckt of bancoDeRegistrador16X13 is
12     component MUX16_1_13Bits is
13        port (I15_16, I14_16, I13_16, I12_16, I11_16, I10_16, I9_16, I8_16, I7_16:
    std_logic_vector(12 downto 0);
14              I6_16, I5_16, I4_16, I3_16, I2_16, I1_16, I0_16: std_logic_vector(12 downto 0);
15              S_16: in std_logic_vector(3 downto 0);
16              ld_mux_16: in std_logic;
17              d_16: out std_logic_vector(12 downto 0));
18     end component;
19
20     component decodificador1X16 is
21        port (ld_dec: in std_logic;
22              i_in: in std_logic_vector(3 downto 0);
23              d_out: out std_logic_vector(15 downto 0));
24     end component;
25
26     component reg13Bits is
27        port (clk,preSet,clr,load: in std_logic;
28              d: in std_logic_vector(12 downto 0);
29              q: out std_logic_vector(12 downto 0));
30     end component;
31
32
33     signal saida_reg_00, saida_reg_01, saida_reg_02, saida_reg_03, saida_reg_04,
    saida_reg_05, saida_reg_06, saida_reg_07: std_logic_vector(12 downto 0);
34     signal saida_reg_08, saida_reg_09, saida_reg_10, saida_reg_11, saida_reg_12,
    saida_reg_13, saida_reg_14, saida_reg_15, saida_mux: std_logic_vector(12 downto 0);
35     signal saida_decod: std_logic_vector(15 downto 0);
36
37     begin
38        Dec_wr: decodificador1X16 port map(
39           ld_dec => ld_wr,
40           i_in => cont_wr,
41           d_out => saida_decod);
42
43        Reg00: reg13Bits port map(
44           clk => clk_br,
45           preSet => '1',
46           clr => clr_reg,
47           load => saida_decod(0),
48           d => wr_data,
49           q => saida_reg_00);
50
51        Reg01: reg13Bits port map(
52           clk => clk_br,
53           preSet => '1',
54           clr => clr_reg,
55           load => saida_decod(1),
56           d => wr_data,
57           q => saida_reg_01);
58
59        Reg02: reg13Bits port map(
60           clk => clk_br,
61           preSet => '1',
62           clr => clr_reg,
63           load => saida_decod(2),
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64            d => wr_data,
65            q => saida_reg_02);
66
67         Reg03: reg13Bits port map(
68            clk => clk_br,
69            preSet => '1',
70            clr => clr_reg,
71            load => saida_decod(3),
72            d => wr_data,
73            q => saida_reg_03);
74
75         Reg04: reg13Bits port map(
76            clk => clk_br,
77            preSet => '1',
78            clr => clr_reg,
79            load => saida_decod(4),
80            d => wr_data,
81            q => saida_reg_04);
82
83         Reg05: reg13Bits port map(
84            clk => clk_br,
85            preSet => '1',
86            clr => clr_reg,
87            load => saida_decod(5),
88            d => wr_data,
89            q => saida_reg_05);
90
91         Reg06: reg13Bits port map(
92            clk => clk_br,
93            preSet => '1',
94            clr => clr_reg,
95            load => saida_decod(6),
96            d => wr_data,
97            q => saida_reg_06);
98
99         Reg07: reg13Bits port map(
100           clk => clk_br,
101           preSet => '1',
102           clr => clr_reg,
103           load => saida_decod(7),
104           d => wr_data,
105           q => saida_reg_07);
106
107        Reg08: reg13Bits port map(
108           clk => clk_br,
109           preSet => '1',
110           clr => clr_reg,
111           load => saida_decod(8),
112           d => wr_data,
113           q => saida_reg_08);
114
115        Reg09: reg13Bits port map(
116           clk => clk_br,
117           preSet => '1',
118           clr => clr_reg,
119           load => saida_decod(9),
120           d => wr_data,
121           q => saida_reg_09);
122
123        Reg10: reg13Bits port map(
124           clk => clk_br,
125           preSet => '1',
126           clr => clr_reg,
127           load => saida_decod(10),
128           d => wr_data,
129           q => saida_reg_10);
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130
131         Reg11: reg13Bits port map(
132            clk => clk_br,
133            preSet => '1',
134            clr => clr_reg,
135            load => saida_decod(11),
136            d => wr_data,
137            q => saida_reg_11);
138
139         Reg12: reg13Bits port map(
140            clk => clk_br,
141            preSet => '1',
142            clr => clr_reg,
143            load => saida_decod(12),
144            d => wr_data,
145            q => saida_reg_12);
146
147         Reg13: reg13Bits port map(
148            clk => clk_br,
149            preSet => '1',
150            clr => clr_reg,
151            load => saida_decod(13),
152            d => wr_data,
153            q => saida_reg_13);
154
155         Reg14: reg13Bits port map(
156            clk => clk_br,
157            preSet => '1',
158            clr => clr_reg,
159            load => saida_decod(14),
160            d => wr_data,
161            q => saida_reg_14);
162
163         Reg15: reg13Bits port map(
164            clk => clk_br,
165            preSet => '1',
166            clr => clr_reg,
167            load => saida_decod(15),
168            d => wr_data,
169            q => saida_reg_15);
170
171         MUX_rd: mux16_1_13Bits port map(
172            I15_16 => saida_reg_15,
173            I14_16 => saida_reg_14,
174            I13_16 => saida_reg_13,
175            I12_16 => saida_reg_12,
176            I11_16 => saida_reg_11,
177            I10_16 => saida_reg_10,
178            I9_16 => saida_reg_09,
179            I8_16 => saida_reg_08,
180            I7_16 => saida_reg_07,
181            I6_16 => saida_reg_06,
182            I5_16 => saida_reg_05,
183            I4_16 => saida_reg_04,
184            I3_16 => saida_reg_03,
185            I2_16 => saida_reg_02,
186            I1_16 => saida_reg_01,
187            I0_16 => saida_reg_00,
188            S_16 => cont_rd,
189            ld_mux_16 => ld_rd,
190            d_16 => saida_mux);
191
192         rd_data <= saida_mux;
193   end ckt;
```