```vhdl
 1    library ieee;
 2    use ieee.std_logic_1164.all;
 3
 4    entity bitToBcdToD7Seg is
 5      port (SW_in: in std_logic_vector(7 downto 0);
 6             HEX0,HEX1,HEX2: out std_logic_vector(6 downto 0));
 7    end bitToBcdToD7Seg ;
 8
 9    architecture ckt of bitToBcdToD7Seg is
10      component bitToBcd is
11        port (bit_in: in std_logic_vector(7 downto 0);
12              bcd_out: out std_logic_vector(11 downto 0));
13      end component;
14      component d7Seg is
15         port(S_in: in std_logic_vector(3 downto 0);
16              D_out: out std_logic_vector(6 downto 0));
17      end component;
18
19      signal bcd_ax_out: std_logic_vector(11 downto 0);
20      signal hex0_ax_out,hex1_ax_out,hex2_ax_out : std_logic_vector(6 downto 0);
21
22      begin
23          BtB: BitToBcd port map(
24               bit_in => SW_in,
25               bcd_out => bcd_ax_out);
26
27          D7S2: d7Seg port map(
28                S_in => bcd_ax_out(11 downto 8),
29                D_out => hex2_ax_out);
30
31          D7S1: d7Seg port map(
32                S_in => bcd_ax_out(7 downto 4),
33                D_out => hex1_ax_out);
34
35          D7S0: d7Seg port map(
36                S_in => bcd_ax_out(3 downto 0),
37                D_out => hex0_ax_out);
38          HEX0 <= hex0_ax_out;
39          HEX1 <= hex1_ax_out;
40          HEX2 <= hex2_ax_out;
41    end ckt;
```