```
1   library ieee ;
2   use ieee.std_logic_1164.all;
3
4   entity Comparador is
5     port (in_gt, in_eq, in_lt,a,b: in std_logic;
6           out_eq,out_lt,out_gt: out std_logic);
7   end Comparador;
8
9   architecture ckt of Comparador is
10    begin
11      out_gt <= in_gt OR (in_eq AND a AND (NOT b));
12      out_lt <= in_lt OR (in_eq AND (NOT a) AND b);
13      out_eq <= in_eq AND (a XNOR b);
14  end ckt;
```