```
library ieee ;
   use ieee.std logic 1164.all;
 4
   entity Comparador is
 5 port (in_gt, in_eq, in_lt,a,b: in std_logic;
 6
            out_eq,out_lt,out_gt: out std_logic);
 7 end Comparador;
8
9
   architecture ckt of Comparador is
    begin
10
11
     out_gt <= in_gt OR (in_eq AND a AND (NOT b));</pre>
12
       out lt <= in lt OR (in eq AND (NOT a) AND b);
     out_eq <= in_eq AND (a XNOR b);</pre>
13
14 end ckt;
```