```
1   library ieee ;
2   use ieee.std_logic_1164.all;
3
4   entity reg13Bits is
5      port (clk,preSet,clr,load: in std_logic;
6      d: in std_logic_vector(12 downto 0);
7      q : out std_logic_vector(12 downto 0));
8   end reg13Bits;
9   architecture ckt of reg13Bits is
10
11     signal qs: std_logic_vector(12 downto 0);
12
13     begin
14        process (clk ,preSet,clr)
15        begin
16           if preSet = '0' then qs <= "1111111111111";
17           elsif clr = '0' then qs <= "0000000000000";
18           elsif clk ='1' and clk ' event then
19              if load = '1' then
20                 qs <= d;
21              end if;
22           end if;
23        end process ;
24        q <= qs;
25  end ckt;
```