```
1   library ieee;
2   use ieee.std_logic_1164.all;
3
4   entity ciBitToBcd is
5     port (BtB_in: in bit_vector(3 downto 0);
6           BtB_out: out bit_vector(3 downto 0));
7   end ciBitToBcd;
8
9   architecture ckt of ciBitToBcd is
10  begin
11    BtB_out(3) <= (BtB_in(3) or (BtB_in(2) and (BtB_in(1) or BtB_in(0))));
12    BtB_out(2)<= ((BtB_in(2) and (not BtB_in(1)) and (not BtB_in(0))) or (BtB_in(3) and
    BtB_in(0)));
13    BtB_out(1)<= ((BtB_in(3) and (not BtB_in(0))) or (BtB_in(1) and ((not BtB_in(2)) or
    BtB_in(0))));
14    BtB_out(0)<= (((not BtB_in(3)) and (not BtB_in(2)) and BtB_in(0)) or ((not BtB_in(0))
    and (BtB_in(3) or (BtB_in(2) and BtB_in(1)))));
15  end ckt;
16
```