```
 1  library ieee;
 2  use ieee.std_logic_1164.all;
 3
 4  entity bitToBcd is
 5    port (bit_in: in std_logic_vector(7 downto 0);
 6          bcd_out: out std_logic_vector(11 downto 0));
 7  end bitToBcd ;
 8
 9  architecture ckt of bitToBcd is
10    component ciBitToBcd is
11      port (BtB_in: in std_logic_vector(3 downto 0);
12            BtB_out: out std_logic_vector(3 downto 0));
13    end component;
14
15    signal ciBtB_01_out, ciBtB_02_out, ciBtB_03_out, ciBtB_04_out, ciBtB_05_out,
    ciBtB_06_out, ciBtB_07_out: std_logic_vector(3 downto 0);
16
17    begin
18        ciBtB01: ciBitToBcd port map(
19             BtB_in(3) => '0',
20             BtB_in(2 downto 0) => bit_in(7 downto 5),
21             BtB_out => ciBtB_01_out);
22
23        ciBtB02: ciBitToBcd port map(
24             BtB_in(3 downto 1) => ciBtB_01_out(2 downto 0),
25             BtB_in(0) => bit_in(4),
26             BtB_out => ciBtB_02_out);
27
28        ciBtB03: ciBitToBcd port map(
29             BtB_in(3 downto 1) => ciBtB_02_out(2 downto 0),
30             BtB_in(0) => bit_in(3),
31             BtB_out => ciBtB_03_out);
32
33        ciBtB04: ciBitToBcd port map(
34             BtB_in(3) => '0',
35             BtB_in(2) => ciBtB_01_out(3),
36             BtB_in(1) => ciBtB_02_out(3),
37             BtB_in(0) => ciBtB_03_out(3),
38             BtB_out => ciBtB_04_out);
39
40        ciBtB05: ciBitToBcd port map(
41             BtB_in(3 downto 1)=> ciBtB_03_out(2 downto 0),
42             BtB_in(0) => bit_in(2),
43             BtB_out => ciBtB_05_out);
44
45        ciBtB06: ciBitToBcd port map(
46             BtB_in(3 downto 1)=> ciBtB_04_out(2 downto 0),
47             BtB_in(0) => ciBtB_05_out(3),
48             BtB_out => ciBtB_06_out);
49
50        ciBtB07: ciBitToBcd port map(
51             BtB_in(3 downto 1)=> ciBtB_05_out(2 downto 0),
52             BtB_in(0) => bit_in(1),
53             BtB_out => ciBtB_07_out);
54
55        bcd_out(11) <= '0';
56        bcd_out(10) <= '0';
57        bcd_out(9) <= ciBtB_04_out(3);
58        bcd_out(8 downto 5) <= ciBtB_06_out;
59        bcd_out(4 downto 1) <= ciBtB_07_out;
60        bcd_out(0) <= bit_in(0);
61
62  end ckt;
```