```
1
     library ieee;
     use ieee.std logic 1164.all;
 3
 4
     entity SUM 4Bits is
 5
      port (A4 in, B4 in: in std logic vector(3 downto 0);
 6
              C4 in: in std logic;
 7
               S4_out: out std_logic_vector(3 downto 0);
              C4_out: out std_logic);
8
9
     end SUM_4Bits;
10
11
     architecture ckt of SUM_4Bits is
12
       component SUM 2Bits is
13
         port (A2 in, B2 in: in std logic vector(1 downto 0);
14
                 C2 in: in std logic;
15
                 S2_out: out std_logic_vector(1 downto 0);
16
                 C2 out: out std logic);
17
        end component;
18
19
        signal Sum_01_out : std_logic;
20
21
       begin
22
          SUM01: SUM_2Bits port map(
23
                A2 in \Rightarrow A4 in(1 downto 0),
24
                 B2_{in} \Rightarrow B4_{in}(1 \text{ downto } 0),
                C2_in => C4_in,
25
26
                 S2 out \Rightarrow S4 out(1 downto 0),
27
                 C2 out => Sum 01 out);
28
29
          SUM02: SUM_2Bits port map(
30
                A2_{in} \Rightarrow A4_{in}(3 \text{ downto } 2),
                 B2 in \Rightarrow B4_in(3 downto 2),
31
32
                C2_in => Sum_01_out,
33
                 S2_out => S4_out(3 downto 2),
34
                 C2 \text{ out } => C4 \text{ out)};
35
36
     end ckt;
```