```
1   library ieee ;
2   use ieee.std_logic_1164.all;
3
4   entity projeto01_MV is
5      port (clock_27, KEY2, KEY3: in std_logic;
6            SW: in std_logic_vector(7 downto 0);
7            LEDR0,LEDR1: out std_logic;
8            LHEX2,LHEX1,LHEX0,LHEX5,LHEX4: out std_logic_vector(6 downto 0));
9   end projeto01_MV;
10
11  architecture ckt of projeto01_MV is
12     component maquinaVendas is
13        port (CLK_mv, C, reset: in std_logic;
14              S, A: in std_logic_vector(7 downto 0);
15              D: out std_logic;
16              saida_mv: out std_logic_vector(1 downto 0);
17              Tot_mv: out std_logic_vector(7 downto 0));
18     end component;
19     component romMV IS
20        PORT(address: IN STD_LOGIC_VECTOR (5 DOWNTO 0);
21             clock: IN STD_LOGIC  := '1';
22             q: OUT STD_LOGIC_VECTOR (7 DOWNTO 0));
23     END component;
24     component divisorClock is
25        port ( clk_in : in std_logic ;
26               clk_out : out std_logic );
27     end component ;
28     component contador6Bits is
29        port ( clk_c6B,ld_c6B,clr_c6B: in std_logic;
30               out_c6B: out std_logic_vector(5 downto 0));
31     end component;
32     component botaoSincrono is
33        port (clk, b_in: in std_logic ;
34              b_out: out std_logic );
35     end component;
36     component bitToBcdToD7Seg is
37        port (SW_in: in std_logic_vector(7 downto 0);
38              HEX0,HEX1,HEX2: out std_logic_vector(6 downto 0));
39     end component;
40
41     signal CLK_1, saida_botao, saida_MV, ld_reverso, clr_reverso: std_logic;
42     signal saida_SS: std_logic_vector(1 downto 0);
43     signal saida_contador: std_logic_vector(5 downto 0);
44     signal entrada_A_mv, total_sum_mv: std_logic_vector(7 downto 0);
45     signal saida_hex2, saida_hex1, saida_hex0, saida_hex5, saida_hex4,lixo:
   std_logic_vector(6 downto 0);
46
47     begin
48
49        ld_reverso <= not KEY2;
50        clr_reverso <= not KEY3;
51
52        DivClock: divisorClock port map(
53           clk_in => clock_27,
54           clk_out => CLK_1);
55
56        BS: botaoSincrono port map(
57           clk => CLK_1,
58           b_in => ld_reverso,
59           b_out => saida_botao);
60
61        ROM: romMV port map (
62           clock => CLK_1,
63           address => saida_contador,
64           q => entrada_A_mv);
65
```

```
66          Cont: contador6Bits port map(
67             clk_c6B => CLK_1,
68             ld_c6B => saida_botao,
69             clr_c6B => clr_reverso,
70             out_c6B => saida_contador);
71
72          MV: maquinaVendas port map(
73             CLK_mv => CLK_1,
74             C => saida_botao,
75             reset => clr_reverso,
76             S => SW,
77             A => entrada_A_mv,
78             D => saida_MV,
79             saida_mv => saida_SS,
80             Tot_mv => total_sum_mv);
81
82          LedTotalMV: bitToBcdToD7Seg port map(
83             SW_in => total_sum_mv,
84             HEX0 => saida_hex0,
85             HEX1 => saida_hex1,
86             HEX2 => saida_hex2);
87
88          LedROM: bitToBcdToD7Seg port map(
89             SW_in => entrada_A_mv,
90             HEX0 => saida_hex4,
91             HEX1 => saida_hex5,
92             HEX2 => lixo);
93
94          LEDR0 <= saida_MV;
95          LEDR1 <= saida_botao;
96          LHEX2 <= saida_hex2;
97          LHEX1 <= saida_hex1;
98          LHEX0 <= saida_hex0;
99          LHEX4 <= saida_hex4;
100         LHEX5 <= saida_hex5;
101   end ckt ;
```