```
1   library ieee;
2   use ieee.std_logic_1164.all;
3
4   entity SUM_8Bits is
5     port (A8_in,B8_in: in std_logic_vector(7 downto 0);
6           C8_in: in std_logic;
7           S8_out: out std_logic_vector(7 downto 0);
8           C8_out: out std_logic);
9   end SUM_8Bits;
10
11  architecture ckt of SUM_8Bits is
12    component SUM_4Bits is
13      port (A4_in,B4_in: in std_logic_vector(3 downto 0);
14            C4_in: in std_logic;
15            S4_out: out std_logic_vector(3 downto 0);
16            C4_out: out std_logic);
17    end component;
18
19    signal Sum_01_out : std_logic;
20
21    begin
22      SUM01: SUM_4Bits port map(
23            A4_in => A8_in(3 downto 0),
24            B4_in => B8_in(3 downto 0),
25            C4_in => C8_in,
26            S4_out => S8_out(3 downto 0),
27            C4_out => Sum_01_out);
28
29      SUM02: SUM_4Bits port map(
30            A4_in => A8_in(7 downto 4),
31            B4_in => B8_in(7 downto 4),
32            C4_in => Sum_01_out,
33            S4_out => S8_out(7 downto 4),
34            C4_out => C8_out);
35
36  end ckt;
```