```
library ieee ;
 1
     use ieee.std logic 1164.all;
 2
 3
 4
     entity REGx3 OUT is
 5
        port (clk REGx3 OUT: in std logic;
 6
              dec F s: in std logic vector(1 downto 0);
 7
              regBR in: in std logic vector(7 downto 0);
 8
              regA_out, regB_out, regC_out: out std_logic_vector(7 downto 0));
 9
     end REGx3 OUT;
10
11
    architecture ckt of REGx3_OUT is
12
13
        component reg8Bits is
14
           port (clk reg8bits, clr reg8bits, ld reg8bits: in std logic;
15
                 d in reg8bits: in std logic vector(7 downto 0);
16
                  q out reg8bits : out std logic vector(7 downto 0));
17
        end component;
18
19
        component decodificador1X3 is
20
           port (i in: in std logic vector(1 downto 0);
21
                 d_out: out std_logic_vector(2 downto 0));
22
        end component;
23
24
        signal dec out: std logic vector(2 downto 0);
25
        signal ld_A, ld_B, ld_C: std_logic;
26
        signal a_out, b_out, c_out: std_logic_vector(7 downto 0);
27
28
        begin
29
           deconder:decodificador1X3 port map(
30
              i_i =  dec_F_s,
31
              d out => dec out);
32
33
           1d A \le dec out(0);
34
           ld B <= dec_out(1);</pre>
35
           1d C \le dec out(2);
36
37
           REGISTRADOR A: reg8Bits port map(
38
              clk reg8bits => clk REGx3 OUT,
39
              clr reg8bits => '0',
40
              ld_reg8bits => ld_A,
41
              d in reg8bits => regBR in,
42
              q out reg8bits => a out);
43
44
           REGISTRADOR B: reg8Bits port map(
45
              clk reg8bits => clk REGx3 OUT,
46
              clr reg8bits => '0',
47
              ld reg8bits => ld B,
48
              d in reg8bits => regBR in,
49
              q_out_reg8bits => b_out);
50
51
           REGISTRADOR_C: reg8Bits port map(
52
              clk reg8bits => clk REGx3 OUT,
              clr reg8bits => '0',
53
54
              ld reg8bits => ld C,
55
              d in reg8bits => regBR in,
56
              q out reg8bits => c out);
57
58
           regA_out <= a_out;</pre>
59
           regB out <= b out;</pre>
60
           regC_out <= c_out;</pre>
61
     end ckt;
```