Arm Cortex-M1 DesignStart FPGA-Xilinx edition

**User Guide Addendum**

# Chapter 2

## Downloading QSPI memory models

### Shell models for users who do not require full simulation

The package supports users who may not wish to perform simulation or may not wish to perform simulation with the QSPI models. In this instance the user will not need to download the QSPI memory models from the vendor websites. However, the user will still experience the warnings associated with opening the project when these files have not been downloaded.

To remove these warnings the package contains empty shell files which can be extracted to the correct locations, such that when opening the project, the warnings are no longer present. In addition, these shell files will compile correctly under simulation, such that the user will not get simulation warnings when including them. However, the user should be aware that these files are empty shell files with no functionality. If the user does require correct simulation of the QSPI devices used by the example design, they do need to download the correct files from the respective websites.

### Installing the shell files

1. Navigate to v:/hardware/m1\_for\_arty\_a7/testbench
2. Extract the file testbench\_shell\_files.zip to the current directory, (not to a further directory). This should result in the following file structure

V:/m1\_for\_arty\_a7

|- hardware

|- sfdp.vmf

|- testbench

|- Micron\_N25Q128A13E

| |- code

| |- N25Qxxx.v

|- S25fl128s

|- model

|- s25fl128s.v

### Installing memory models having extracted shell files

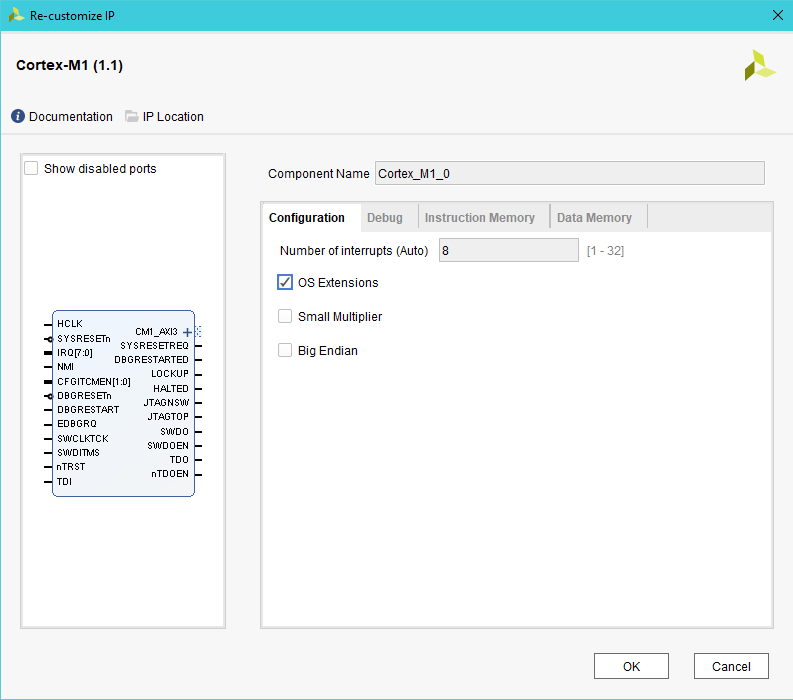
Subsequent to extracting the shell memory models, If the user requires to then install the correct QSPI memory models from the respective vendor websites, then before installing these files, they should delete the file structure above, including the three files, and all associated directories.

# Chapter 3

## Cortex-M1 processor IP configuration

### Configuration Tab

The ability to select the number of interrupts using the configuration tab has been removed. The number of interrupts port will automatically size to match the size of the vector connected to the IRQ input.

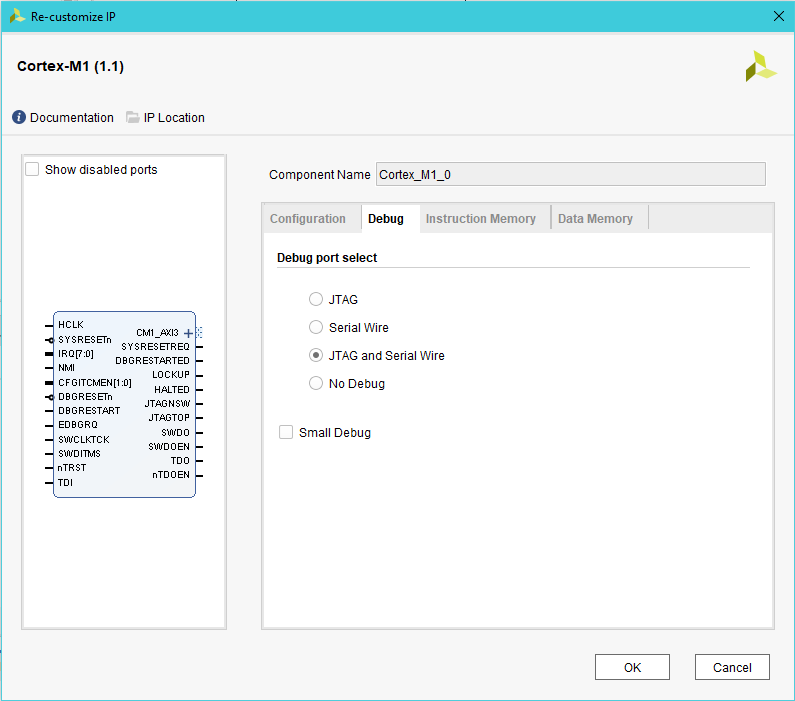


Note that valid values for the number of interrupts are 1,8,16 and 32. If the vector connected to the IRQ pin has a width different from one of the valid values, the IRQ port is set to the next highest valid value.

When editing the IPI block diagram, in order to modify the width of the IRQ port, firstly update the vector connected to the IRQ pin to the new desired width. Then run Validate Design on the block diagram. The IRQ port will then be updated to match the width of the input vector.

### Debug Tab

The debug tab has a new option, No Debug



When No Debug is selected the debug port will be removed from the Cortex-M1 core. This allows a resource optimised build to be created of the Cortex-M1 core.

Note : When No Debug is enabled, the following needs to be considered;

* The Small Debug option is disabled.
* All debug pins are removed from the Cortex-M1 instance, (JTAG, Serial Wire, and debug resets).
* The ability to drag and drop new code using the V2C-DAPLink board is no longer possible, (section 5.7). Note however that if the V2C-DAPLink J2 jumper, (Cfg), is fitted, existing code will still be run from the V2C-DAPLink QSPI device.
* The ability to debug the Cortex-M1 core is removed, (section 5.8)
* The ability to download software projects through the V2C-DAPLink board is no longer possible (section 5.9).

### Data Memory tab

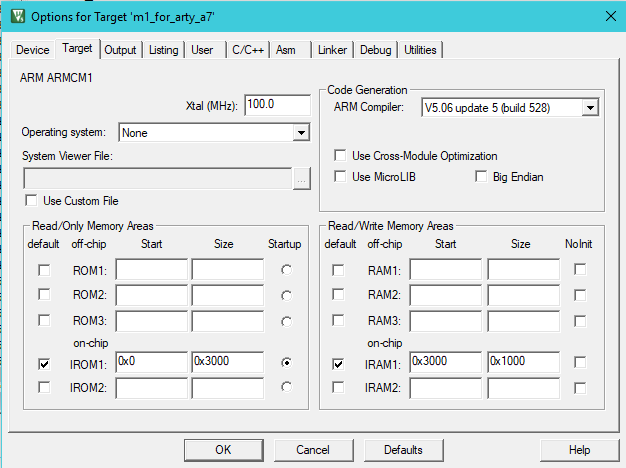
The data memory tab has an increased range of sizes for DTCM size. These now range from 2kB to 1MB. In addition, there is a new option of No DTCM, (0KB).

When selecting the smaller sizes of DTCM users need to ensure that their software project is correctly configured to match the size of DTCM available. As the DTCM is often un-initialised, then it is possible to configure a software project with a larger data memory allocation than that available in the hardware. This will lead to runtime failures.

#### No DTCM

Caution : The No DTCM configuration option should only be selected for designs that are memory resource limited. Removing the DTCM may have a small effect on performance. <end caution/>

With the No DTCM configuration the software must be compiled to divide the ITCM memory between instruction and data areas. An example Keil project configuration is shown below



The above configuration is for ITCM of 16kB, (0x4000 address range), with the first 12kB, (0x3000), allocated to instruction memory, (IROM), and the top 4kB, (0x1000), allocated to data memory, (IRAM). The data memory area starts at 0x3000 which is the top quarter of the instruction memory, and within the memory region of the ITCM. By default, if the DTCM is included, then data memory, (IRAM), should start at 0x2000\_0000. See Section 4.3 for the memory map.