集成电路原理与设计

6.电流镜与基准

宋爽

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Course Arrangements

课数	内容	课数	内容
1	导论	9	差分运算放大器
2	器件模型一	10	折叠共源共栅放大器
3	器件模型二	11	逻辑门
4	工艺流程	12	组合逻辑
5	模拟基本单元	13	时序逻辑
6	电流镜与基准	14	加法器/乘法器
7	单级运放	15	集成电路专题讲座一
8	课堂测验	16	集成电路专题讲座二

Recall the last Chapter

- MOS Switch & Charge Feedthrough

  Working in linear region

- MOS Diode/Active Resistor

  Working in saturation region

  Small signal resistance $1/g_m//r_o$ ~= $1/g_m$

- Current Sinks and Sources

  Cascode -> $r_o = (g_{m1} * r_{o1})\, g_{m2}$

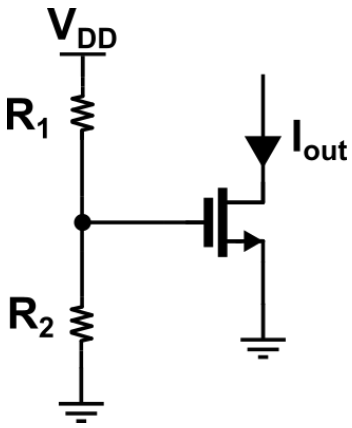
Outline

- Current Mirror
- Voltage Reference

Outline

- **Current Mirror**
- **Reference**

How to bias a MOSFET (1)



- V_{GS} is a function of V_{DD}

  M1 is in saturation:

$$I_{out} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(\frac{R_2}{R_1+R_2}V_{DD} - V_{TH}\right)^2$$

- **ΔV_{TH} : 50~100mV**
- μ_n and V_{TH}: temperature dependence

  when V_{OV} =0.2V, ΔV_{TH} = 50mV => $\Delta I_{out}/I_{out}$ = 44%

Process*, *(Supply) Voltage*, *Temperature

Corners	Nominal	C0_block	C1_block	C2_block	C3_block	C4_block
Temperature		-10 20 80	-10 20 80	-10 20 80	-10 20 80	-10 20 80
Design Variables						
vdd		2.0 3.3	2.0 3.3	2.0 3.3	2.0 3.3	2.0 3.3
vddl		1.08 1.2 1.32	1.08 1.2 1.32	1.08 1.2 1.32	1.08 1.2 1.32	1.08 1.2 1.32
Click to add						
Parameters						
Click to add						
Model Files						
Click to add						
Model Group(s)	FSTT	TTTT	SSTT	FFTT	SFTT	FSTT
Click to add						
Tests						
TRAN						
Number of Corners	1	18	18	18	18	18

How to bias a MOSFET (2)

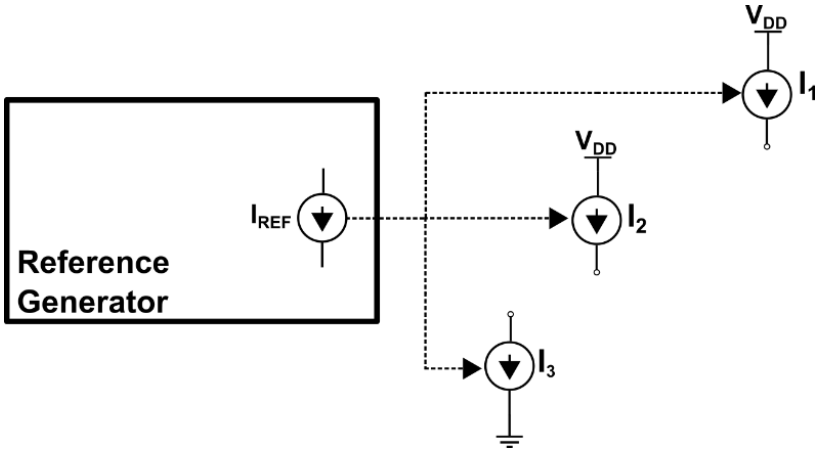
- Design of current sources

  should always base on ***copying currents from a reference*** !

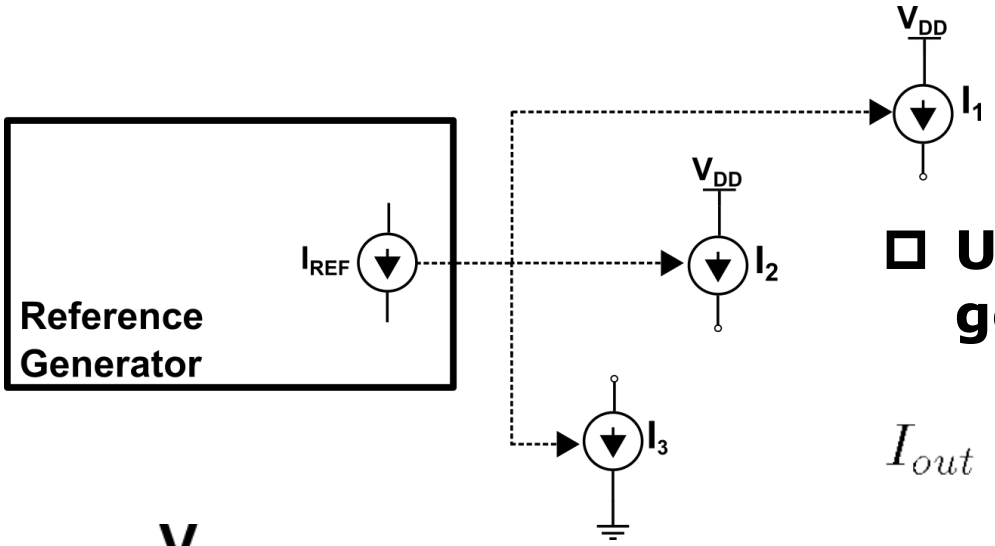
  by using ***diode connected*** transistors

Assume: one precisely-defined current source is already available ⇒ **Bandgap reference**

use of a reference to generate various currents ⇒ **Current mirrors**

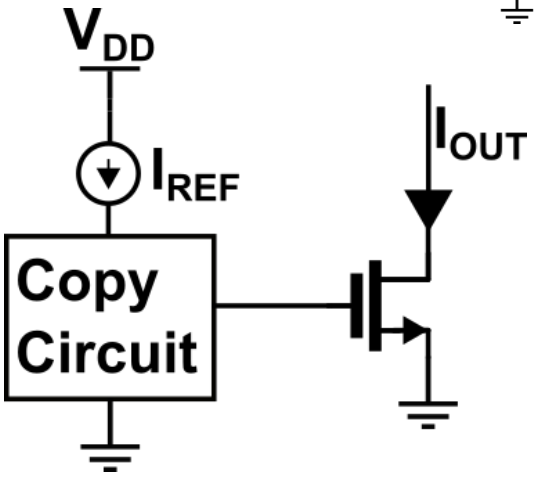


Basic Current Mirror



- Use a reference to generate various currents

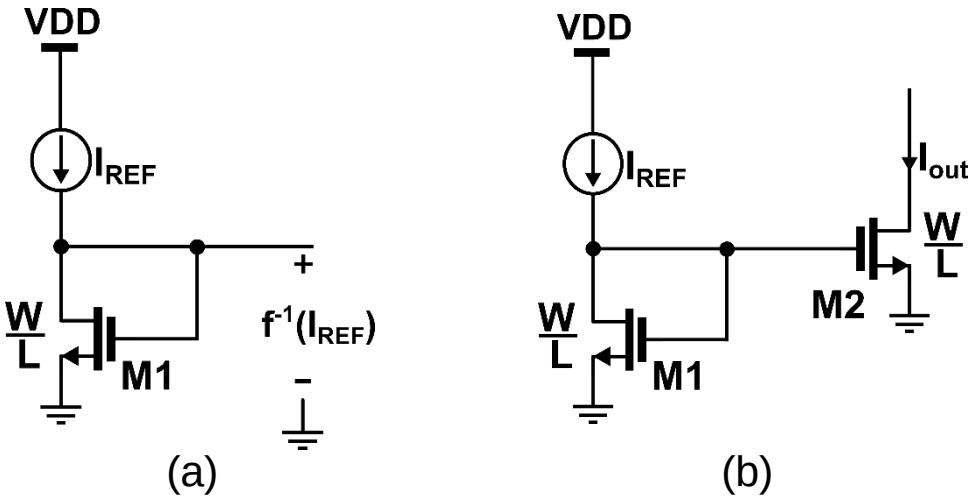
$$I_{out} = f[f^{-1}(I_{REF})] = I_{REF}$$



- Assume that one precisely-defined current source is already available
- Copy a current

$$I_{out} = I_{REF}$$

Basic Current Mirror



(a) Diode-connected device **providing inverse function** (b) basic current mirror

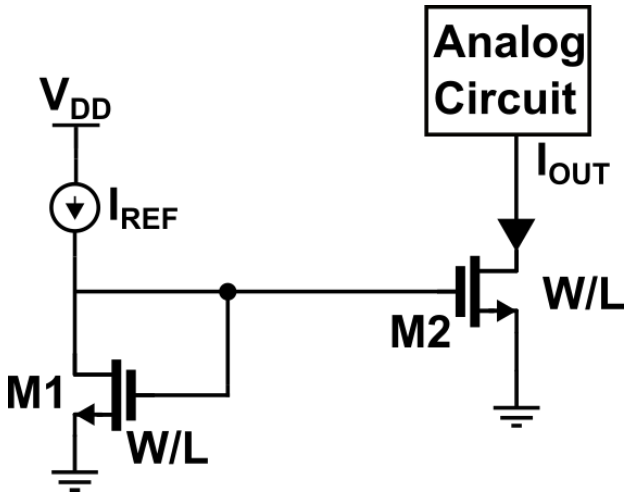
$$I_{REF} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{GS} - V_{TH})^2$$

$$I_{out} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{GS} - V_{TH})^2$$

$$\Rightarrow \quad I_{out} = \frac{(W/L)_2}{(W/L)_1} I_{REF}$$

Principle of Basic Current Mirror

- Two **identical MOS** devices that have **equal gate-source voltages** and operate in **saturation** carry equal currents



$$I_{REF} = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_1 \left(V_{GS} - V_{TH}\right)^2 \left(1 + \lambda V_{DS1}\right)$$

$$I_{out} = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_2 \left(V_{GS} - V_{TH}\right)^2 \left(1 + \lambda V_{DS2}\right)$$

$$\because\ V_{DS1} = V_{GS1} = V_{GS2}$$

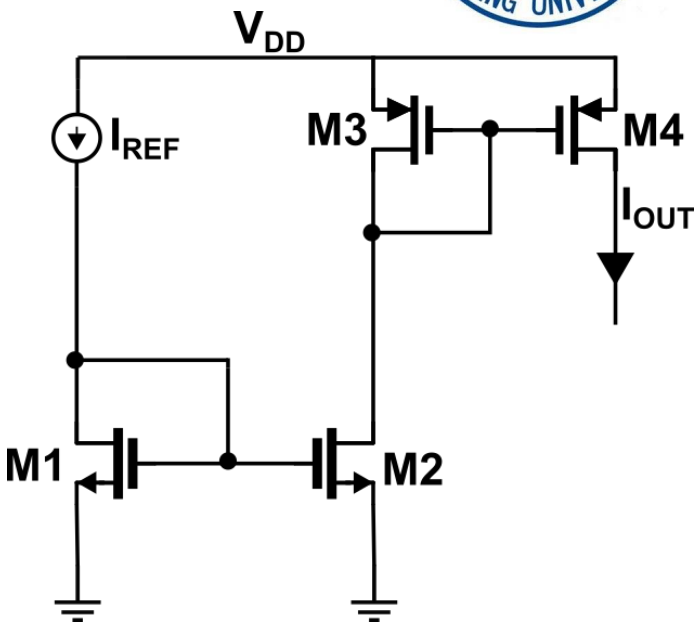
$$\therefore\ I_{out} = I_{REF}\frac{\left(W/L\right)_2\left(1 + \lambda V_{DS2}\right)}{\left(W/L\right)_1\left(1 + \lambda V_{DS1}\right)}$$

$$\lambda = 0 \Rightarrow I_{out} \approx \frac{\left(W/L\right)_2}{\left(W/L\right)_1} I_{REF} \qquad \left(W/L\right)_2 = \left(W/L\right)_1 \Rightarrow I_{out} \approx I_{REF}$$

- Allows precise copying of the current with **no dependence on process and temperature**
- $I_{out} \sim I_{REF}$ involves the **ratio of device dimensions**, that could be controlled with reasonable accuracy <1%.

Example

Find the drain current of M4 if all of the transistors are in saturation



Solution:

Ignoring the channel length modulation

$$I_{D2} = I_{REF}[(W/L)_2/(W/L)_1]$$
$$|I_{D3}| = |I_{D2}|$$
$$I_{D4} = I_{D3}[(W/L)_4/(W/L)_3]$$

$$|I_{D4}| = \alpha\beta I_{REF}$$

$$\alpha = (W/L)_2/(W/L)_1 \qquad \beta = (W/L)_4/(W/L)_3$$

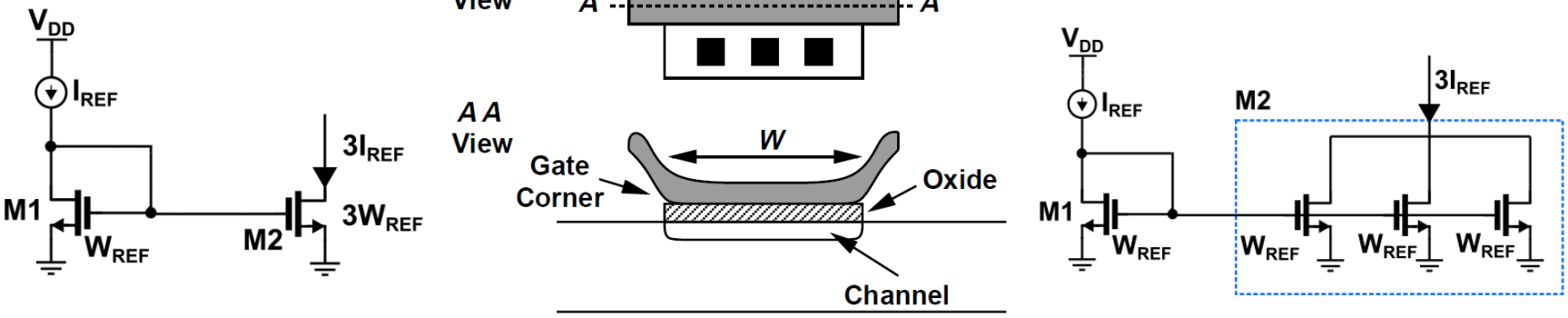
Properly choose of and establish ratios between I_{D4} and I_{REF}

$\alpha = \beta = 5$ magnification factor of 25

$\alpha = \beta = 0.2$ generate a small, well-defined current.

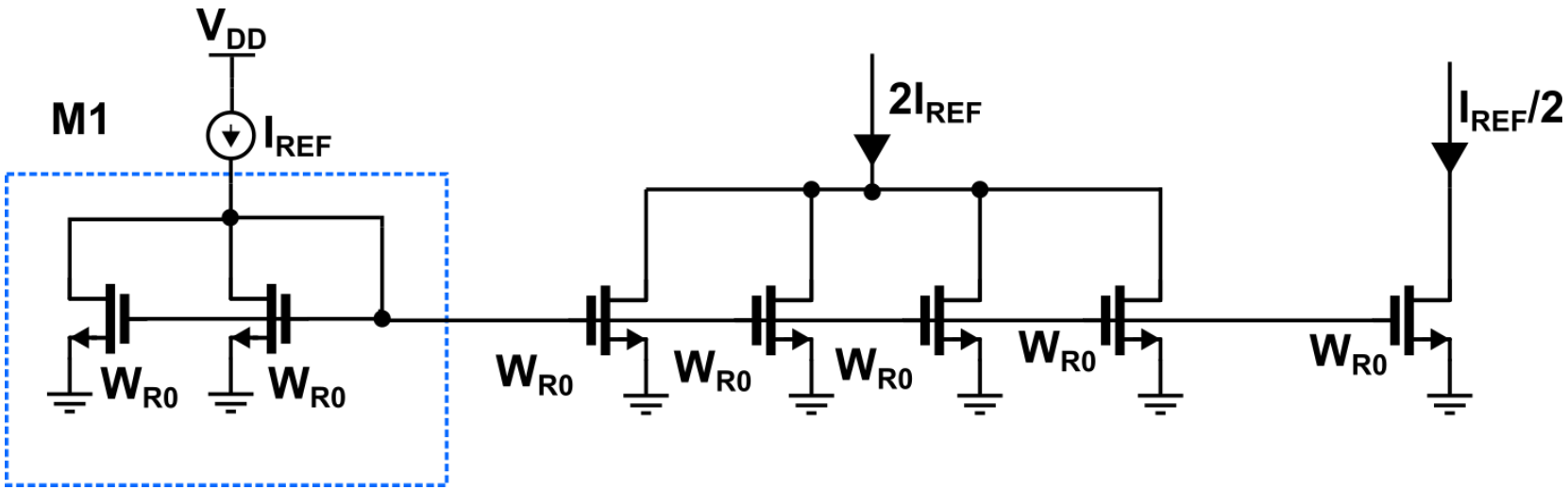
Do not use extreme values !!

Sizing Issues



- Employ the ***same length*** for all of the transistors.
- Only scaling the **width** of transistors
- Employ a **"unit" transistor** and create **copies** by repeating such a device

How to generate a current equal to IREF /2 from IREF ?



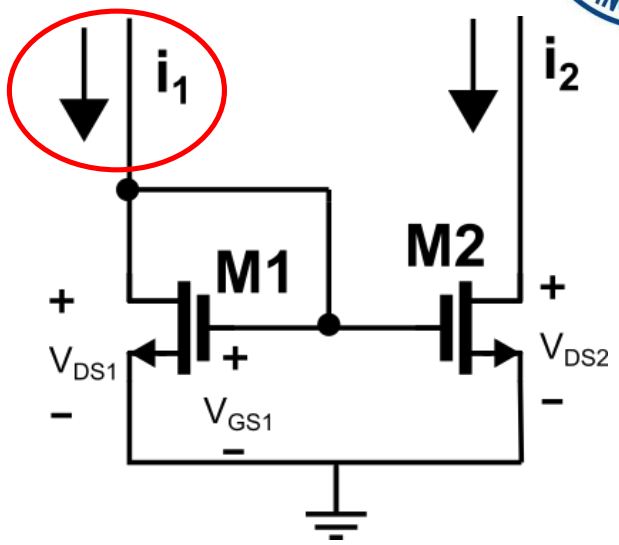
- Use Double Size of MOS to share the current which divides input current to half

Mismatches in the Current Mirror

$$\frac{i_O}{i_1} = \frac{(W_2/L_2)}{(W_1/L_1)}$$

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS})$$

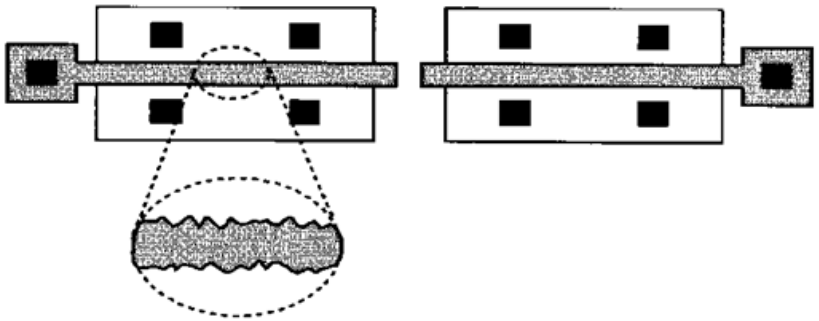
$$\frac{i_O}{i_1} = \frac{(W_2/L_2)}{(W_1/L_1)}\left(\frac{K_2'}{K_1'}\right)\left(\frac{V_{GS} - V_{T2}}{V_{GS} - V_{T1}}\right)^2\left[\frac{1+\lambda v_{DS2}}{1+\lambda v_{DS2}}\right]$$



Following cause the current mirror to be different from the ideal situation

- **Channel length modulation** $V_{DS1} \neq V_{DS2}$
- Threshold offset between the two transistors and the mismatching of transconductance gain *K'* **M1 and M2 are not matched**
- Imperfect geometrical matching **Layout Effect**

Imperfect Geometrical Matching



Random mismatches due to microscopic variations in device dimensions

For two nominally-identical transistors, mismatches between μ , C_{ox}, W, L and V_{TH}

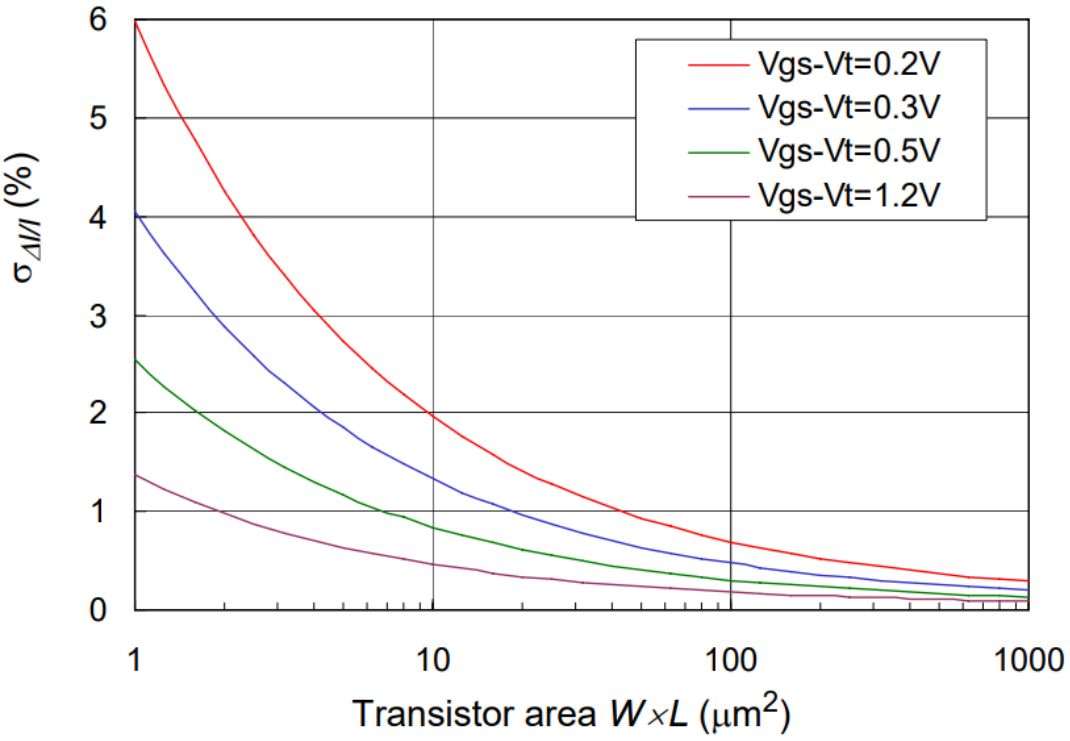
$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)\left(V_{GS}-V_{TH}\right)^2\left(1+\lambda V_{DS}\right)$$

mismatches between I_D (for a given V_{GS}) or V_{GS} (for a given I_D)

- With the **increase of W and L**, the relative mismatch will be respectively reduced (**Larger devices show smaller mismatch**).
- **With the increase of transistors' area**, all the mismatch will be reduced.

Devices matching

- The matching depends on the area

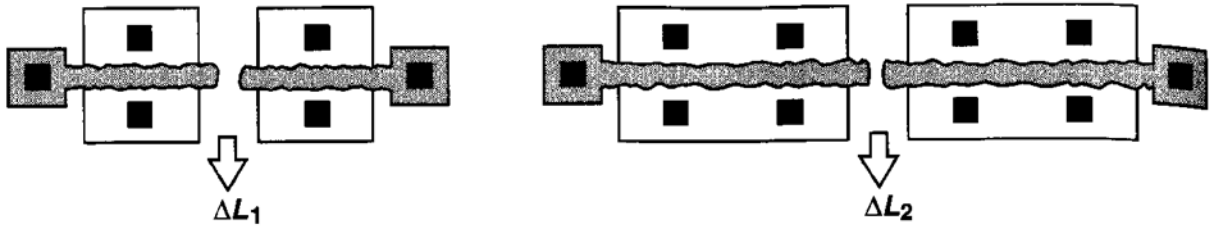


$$\sigma_{\Delta V_T} = \frac{A_{V_T}}{\sqrt{W_e \times L_e}} + B_{V_T}$$

$$\sigma_{\Delta\beta/\beta} = \frac{A_\beta}{\sqrt{W_e \times L_e}} + B_\beta$$

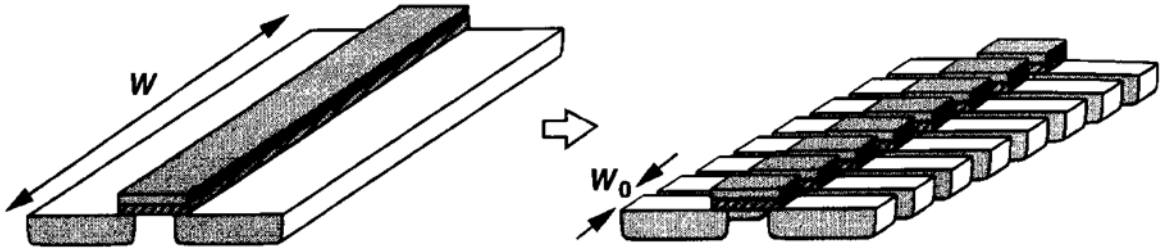
$$\sigma_{\Delta I/I} = \sqrt{\frac{4\sigma^2_{\Delta V_T}}{(V_{GS} - V_T)^2} + \sigma^2_{\Delta\beta/\beta}}$$

Mismatch



(a) $\Delta L_1 > \Delta L_2$ (b)

Reduction of length mismatch as a result of increasing the width



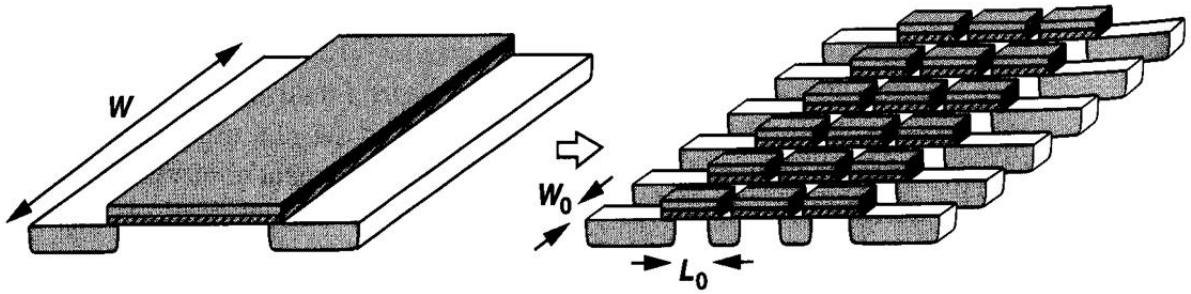
Wide MOSFET viewed as a parallel combination of narrow devices

$$Leq \approx \left(L_1 + L_2 + ... + L_n\right)/n$$

$$\Delta Leq \approx \sqrt{\left(\Delta L_1^2 + \Delta L_2^2 + \cdots + \Delta L_n^2\right)}/n = \frac{\sqrt{n\Delta L_0^2}}{n} = \frac{\Delta L_0}{\sqrt{n}}$$

Where $\Delta L_0$is the statistical variation of the length for transistor with width W_0.

Mismatch



Large MOSFET viewed as a combination of small devices

For given W_0 and L_0, as the number of unit transistors increased $(\mu C_{ox})_j$ and V_{THj} experience greater averaging, leading to smaller mismatch between two large transistor.

$$\Delta V_{TH} = \frac{A_{VTH}}{\sqrt{WL}} \qquad \Delta\left(\mu C_{OX}\frac{W}{L}\right) = \frac{A_K}{\sqrt{WL}}$$

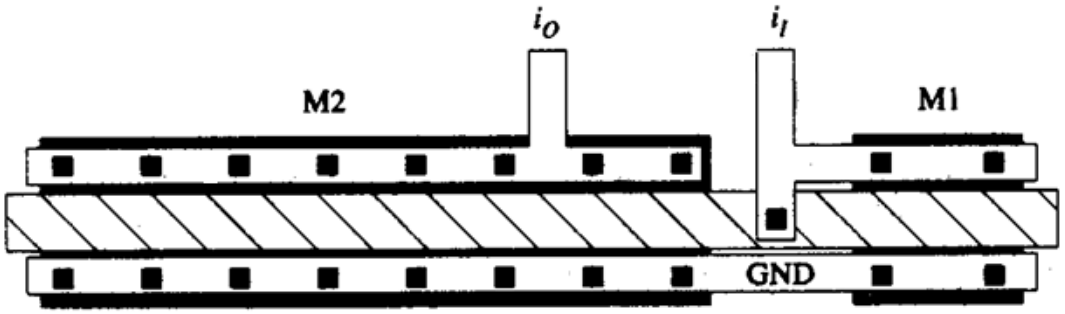
A_{VTH} is scaled down with the gate oxide thickness.

- M. J. Pelgrom, A. C. Duinmaijer, A. P. Welbers, et al., "Matching properties of mos transistors," IEEE Journal of solid-state circuits, vol. 24, no. 5, pp. 1433–1439, 1989.

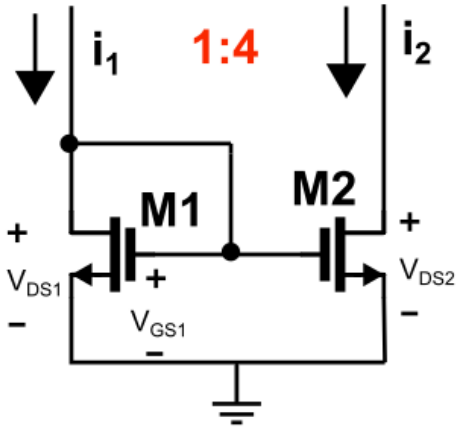
Example

Aspect ratio errors in current amplifiers

$L_1=L_2$ W1=5±0.05μm W2=20±0.05μm (***edge***)



Layout of current mirror without ΔW correction



$$\frac{i_O}{i_1}=\frac{W_2}{W_1}=\frac{20\pm0.05}{5\pm0.05}=4\times\left(\frac{1\pm\frac{0.05}{20}}{1\pm\frac{0.05}{5}}\right)\approx 4\times\left(1\pm\frac{0.05}{20}\right)\left(1-\frac{\pm0.05}{5}\right)$$

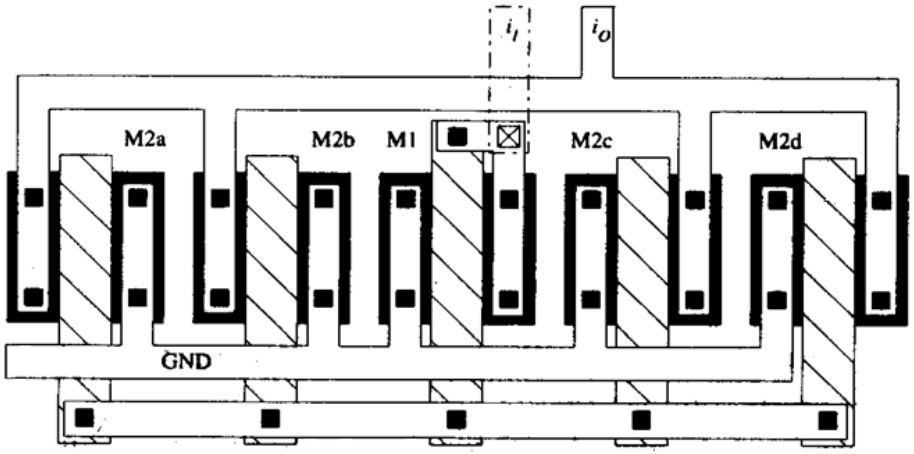
$$\approx 4\times\left(1\pm\frac{0.05}{20}-\frac{\mp0.05}{5}\right)=4\left(1-\frac{\mp0.15}{20}\right)$$

NOTE: The error above would be valid if every other aspect of the transistor were matched perfectly. Assume that the variations would both have the same sign (correlated)

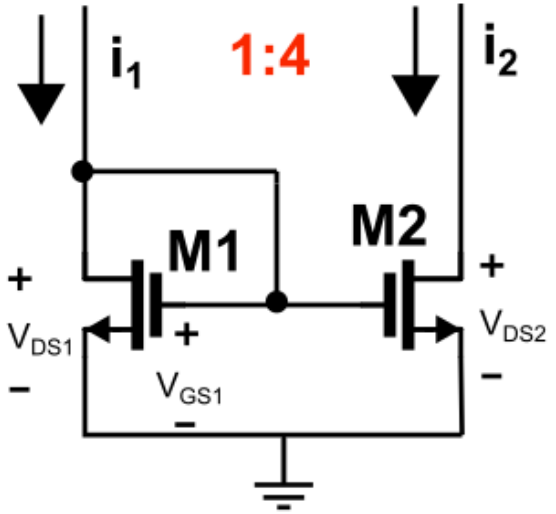
Example

Reduction of the aspect ratio error in current amplifiers.

$L_1=L_2$ $W_1=5\pm0.05\mu m$ $W_2=4(5\pm0.05)\ \mu m$



Layout of current mirror with ΔW correction as well as common-centroid layout techniques



Unit transistor
Common-centroid !!!!

$$\frac{i_O}{i_1}=\frac{W_2}{W_1}=\frac{4\left(5\pm0.05\right)}{5\pm0.05}=4$$

Matching equation is for two identical devices !!!!

NOTE: Assume that ΔW should be the same for all transistors.

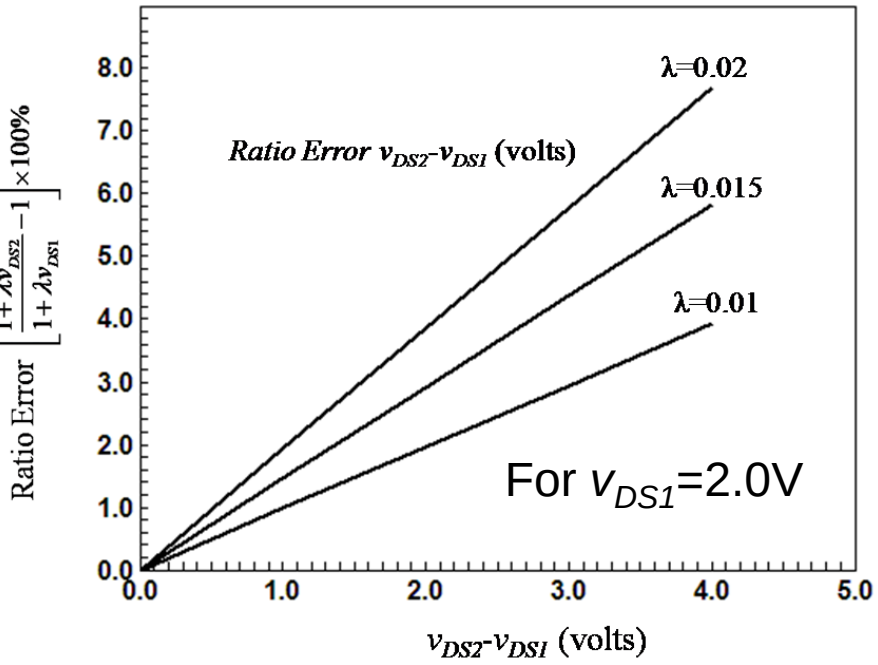
Channel Length Modulation

$$I_{D1} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{GS} - V_{TH})^2 (1 + \lambda V_{DS1})$$

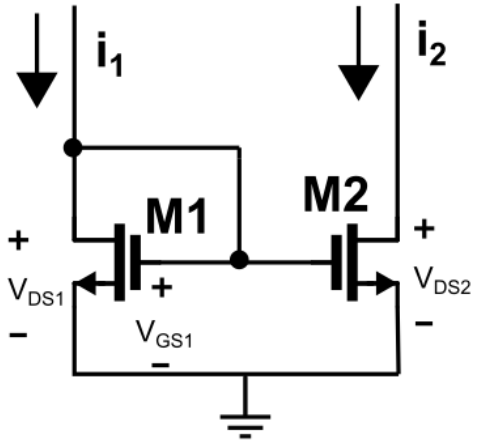
$$I_{D2} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{GS} - V_{TH})^2 (1 + \lambda V_{DS2})$$

$$\Rightarrow \quad \frac{I_{D2}}{I_{D1}} = \frac{(W/L)_2}{(W/L)_1} \cdot \frac{1 + \lambda V_{DS2}}{1 + \lambda V_{DS1}}$$

Assuming all other aspects of the transistor are ideal and the aspect ratios of the two transistors are both unity



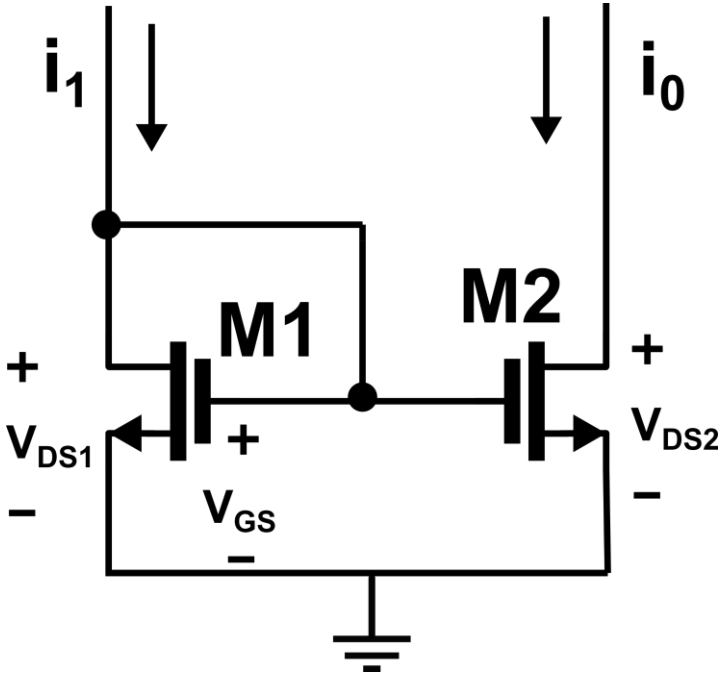
$$\frac{i_O}{i_1} = \frac{1 + \lambda v_{DS2}}{1 + \lambda v_{DS1}}$$



- **Identical drain-source voltage**
- **High output resistance**

Note: one could use this effect to measure λ.

Output resistance and output voltage



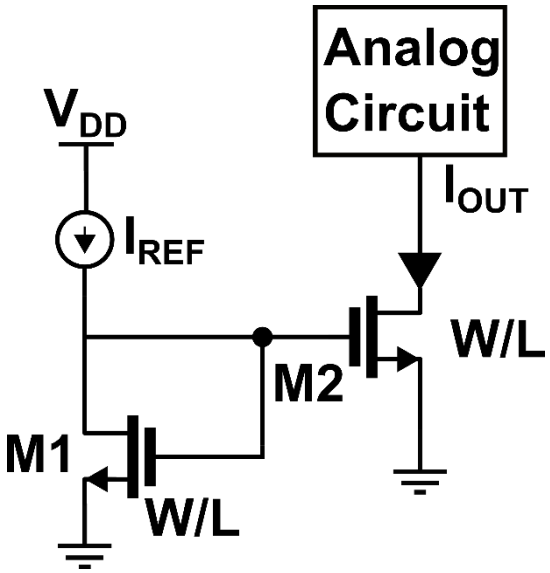
- Output Resistance r_{out}

$$r_{out} = \frac{1}{g_{ds}} \cong \frac{1}{\lambda I_O}$$

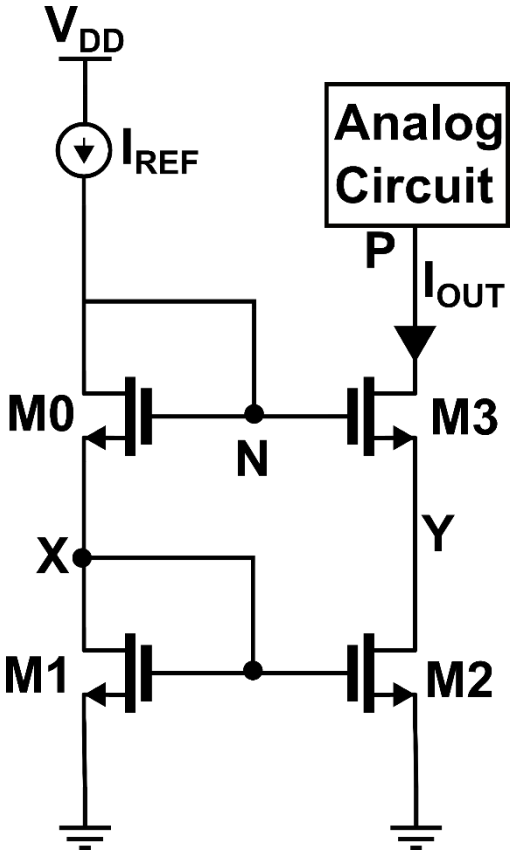
- Output voltage

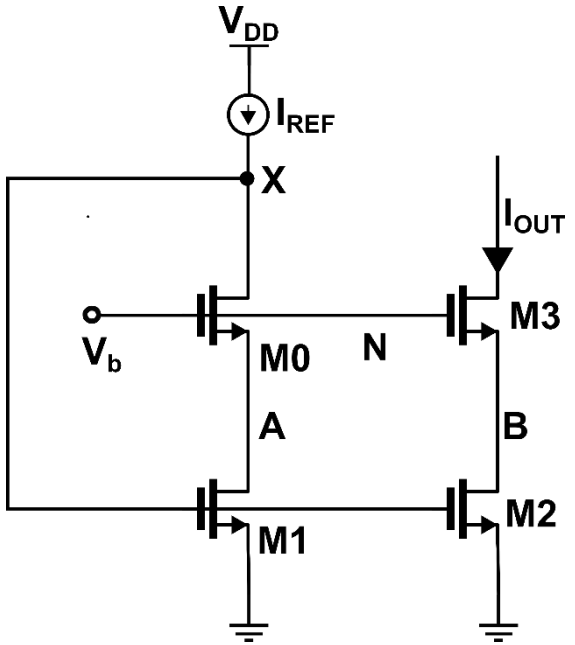
$$V_{\min} = V_{DS,SAT} = V_{GS} - V_{THN}$$

Cascode mirrors



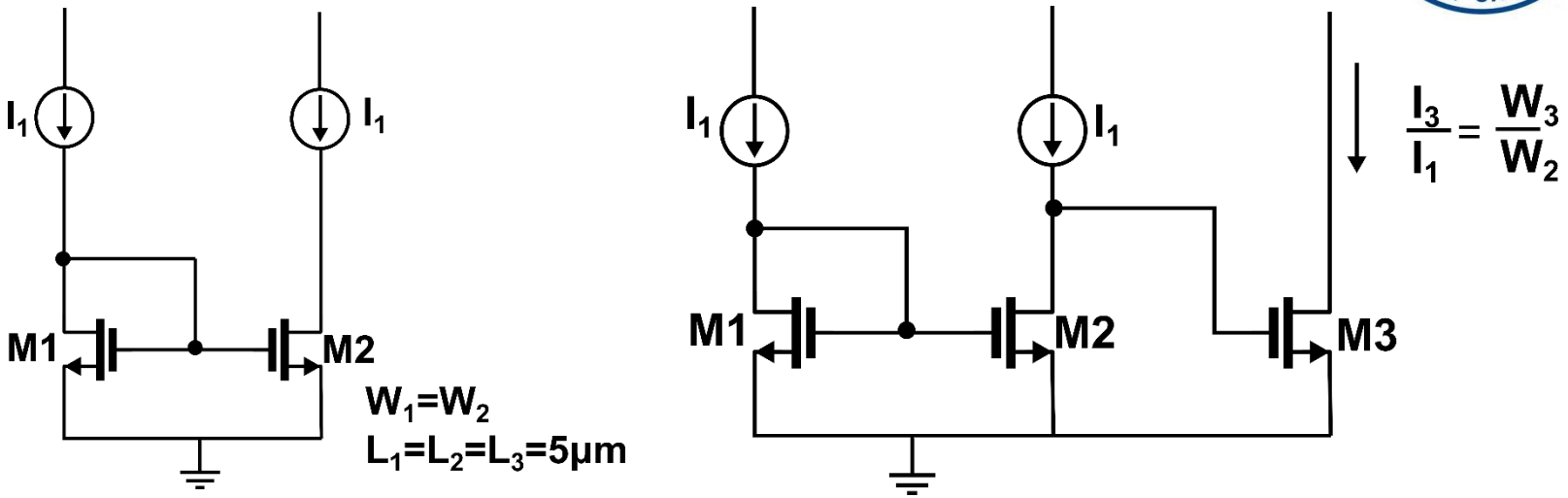
$$r_{out} \cong r_{ds2}$$





$$r_{out} \cong \left(g_{m3} r_{ds3}\right) r_{ds2}$$

Example



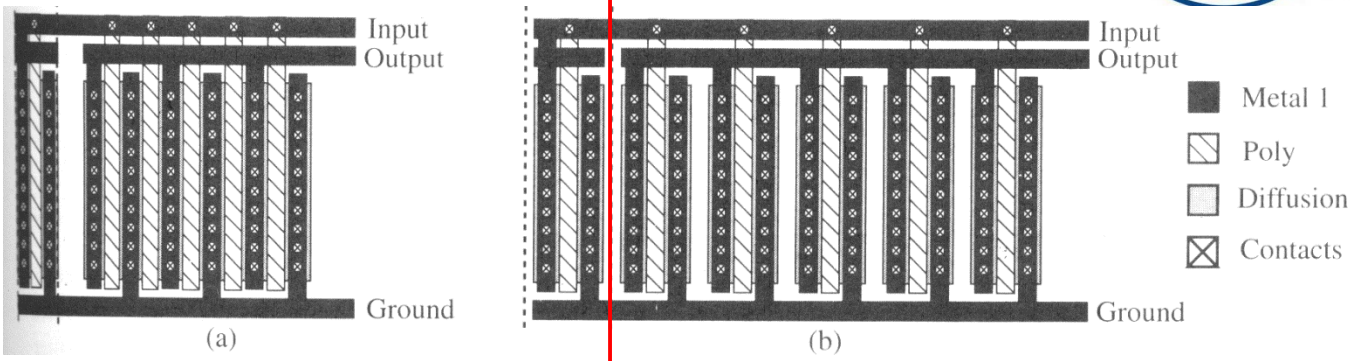
(a) (b)

(a) **The drain of M2 is at the same potential as the gate of M1 or M2** and (b) using this to bias M3. For biasing purposes, we treat M3 as if its gate were tied to the gates of M1 and M2.

$$V_{GS1} = V_{GS2} = V_{DS1} = V_{DS2} \Rightarrow V_{GS3} = V_{GS1} = V_{GS2}$$

Layout: 5:1 ratio

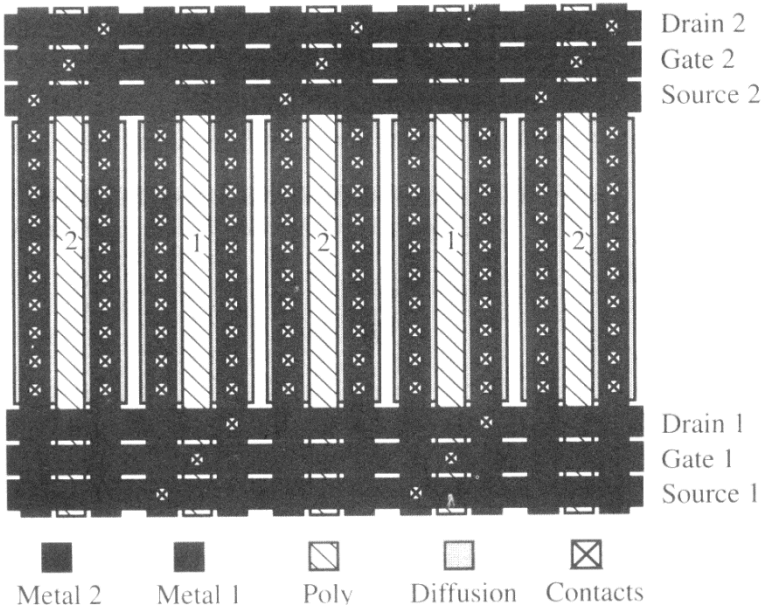
The layout of 5-to1 current mirror



minimizes

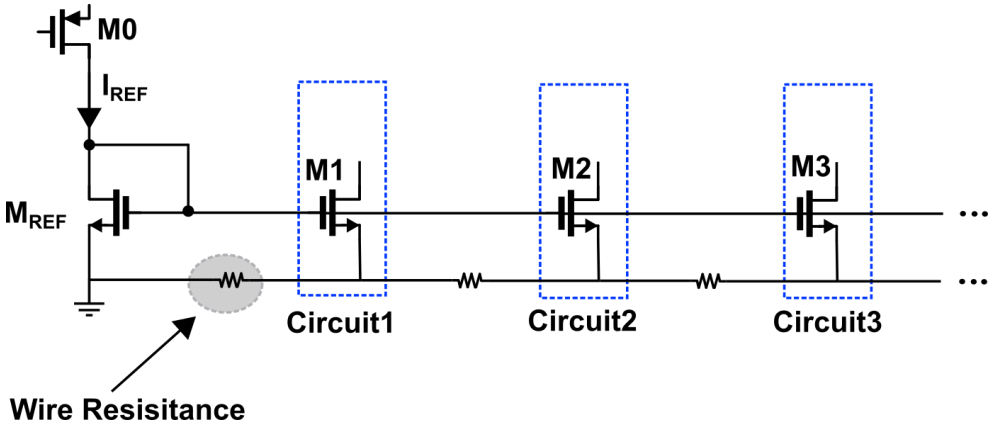
optimizes matching

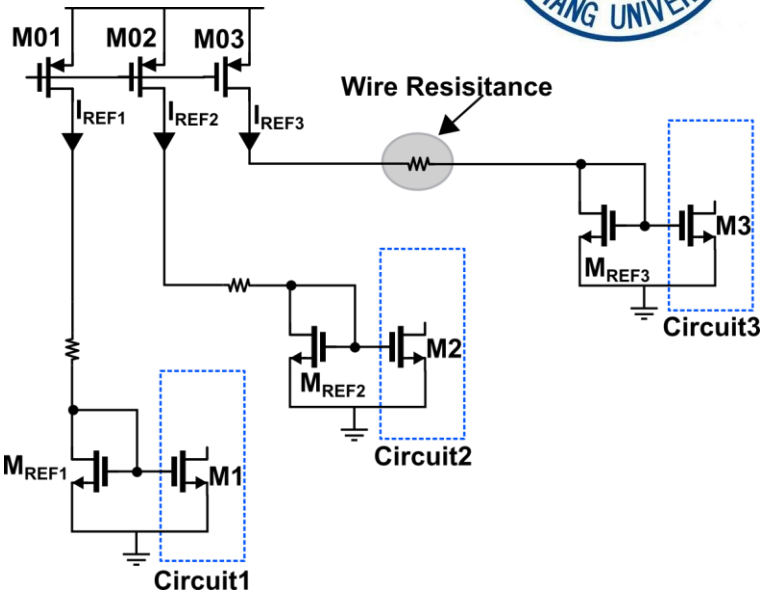
The layout of two transistors with 1.5-to-1 matching



Using centroid geometry to improve matching

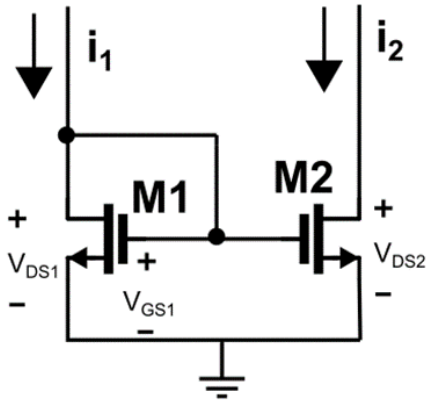
Reference Distribution

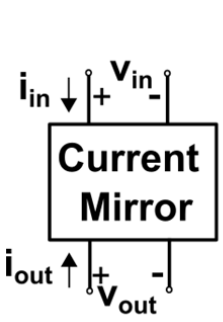


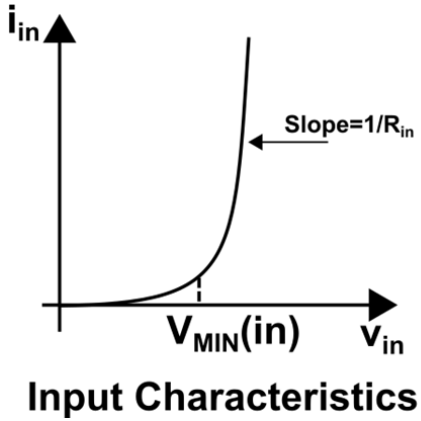


- If the matching is critical, then the voltage drop **along the ground line** must be taken into account.
- **To remedy, the reference can be distributed in the current domain rather than in the voltage domain. (again Vgs vs Vds)**
- Local current mirror pair, or even local bandgap reference is necessary.
- Particular orientation must be paid attention to.

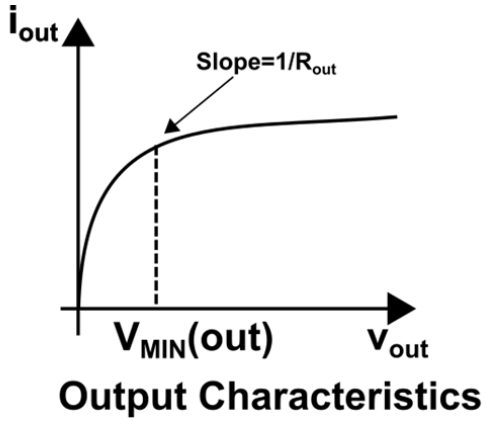
Characterization of Current Mirrors



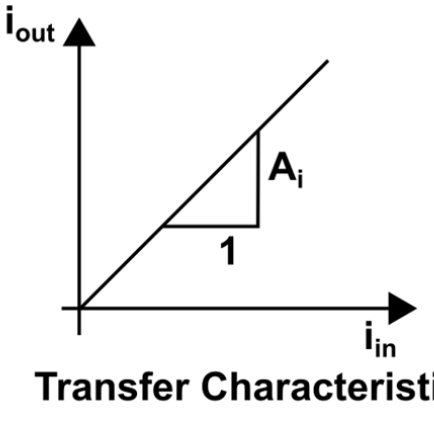




Input Characteristics



Output Characteristics



Transfer Characteristics

Characterization of Current Mirrors

A current mirror is basically nothing more than a current amplifier.

- $i_{out}=A_i i_{in}$ R_{in}->0 R_{out}->∞

- V_{MIN}(in): the range of *v*in over which R_{in} is not small
  which Equation should be used ? (square law)

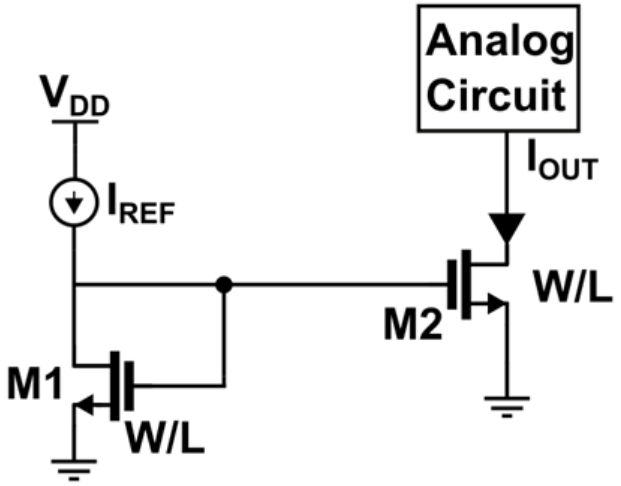
- V_{MIN}(out): the range of *v*out over which R_{out} is not large
  - *a measure of the "flatness" of the current sink/source (its independence of voltage) => large output resistance*
  - *the min. across the sink/source for which the current is no longer constant => large working voltage range*
    which Equation should be used ?
    (channel length modulation and cascode)

Outline

- Current Mirror
- Reference

General Considerations

- Use of bias currents and current mirrors implicitly assumes a "golden" reference current is available
- If I_{REF} does not Change with V_{DD}, and channel-length modulation of M_1 and M_2 is neglected, then I_{out} remain independent of the supply voltage
- However where is the I_{REF}?



General Considerations

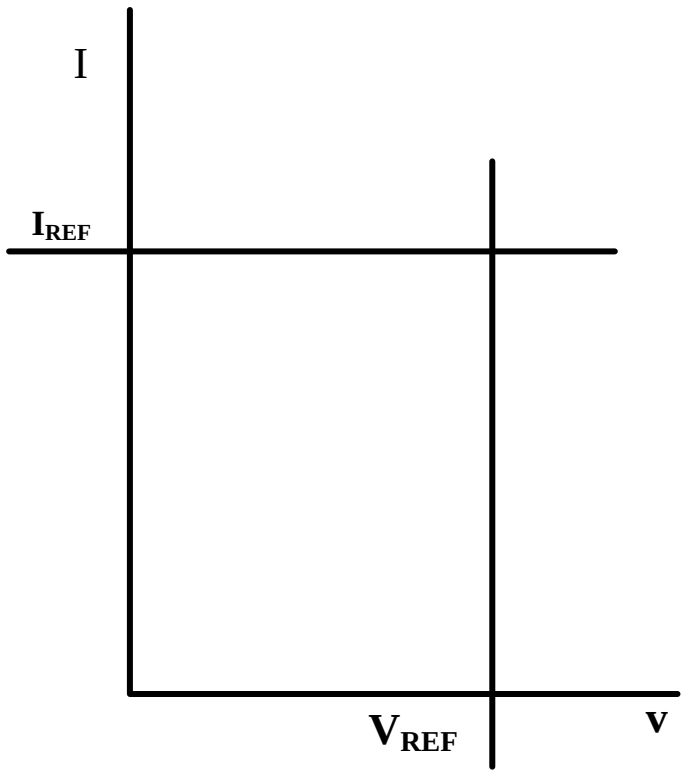
- **I-V characteristics of ideal current and voltage references**
- **Two design problems:**
  - Supply-independent biasing
  - Definition of temperature variation

$$S_{VDD}^{V_{ref}} = \frac{\partial V_{ref} / V_{ref}}{\partial VDD / VDD} = \frac{VDD}{V_{ref}} \cdot \frac{\partial V_{ref}}{\partial VDD}$$

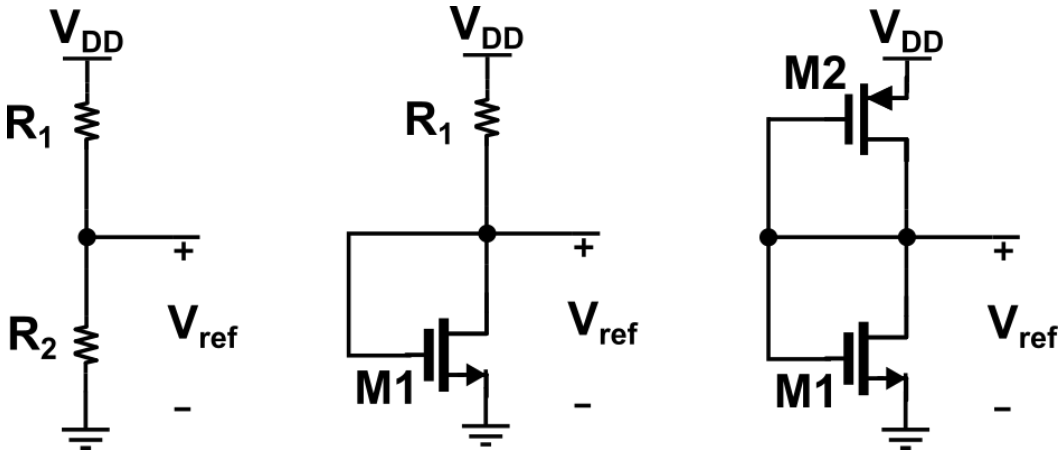
Supply Rejection

$$TC(V_{ref}) = \frac{1}{V_{ref}} \cdot \frac{\partial V_{ref}}{\partial T}$$

Temperature Coefficient



Voltage Biasing



Implementation of voltage dividers in CMOS

1.Resistor Divider

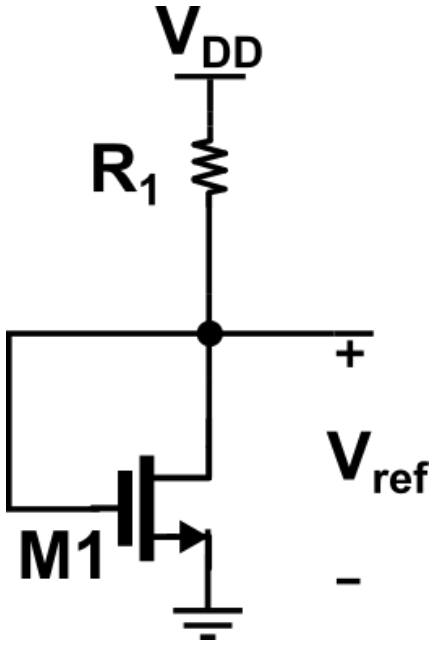
Advantage:

- Simplicity
- Temperature insensitivity
- Process insensitivity

Problems:

- Power dissipation vs. Area
- Power supply sensitivity (Supply Rejection =1)

The Resistor-MOSFET Divider



$$I_D = \frac{VDD - V_{ref}}{R} = \frac{\beta_1}{2}(V_{ref} - V_{THN})^2$$

$$V_{ref} = V_{THN} + \sqrt{\frac{2I_D}{\beta_1}} = V_{THN} + \sqrt{\frac{2(VDD - V_{ref})}{R \cdot \beta_1}}$$

or $$V_{ref} = V_{THN} - \frac{1}{\beta_1 R} + \sqrt{\frac{2(VDD - V_{THN})}{\beta_1 R} + \frac{1}{\beta_1^2 R^2}}$$

The MOSFET-only Voltage Divider

$I_{D1}=I_{D2}$,

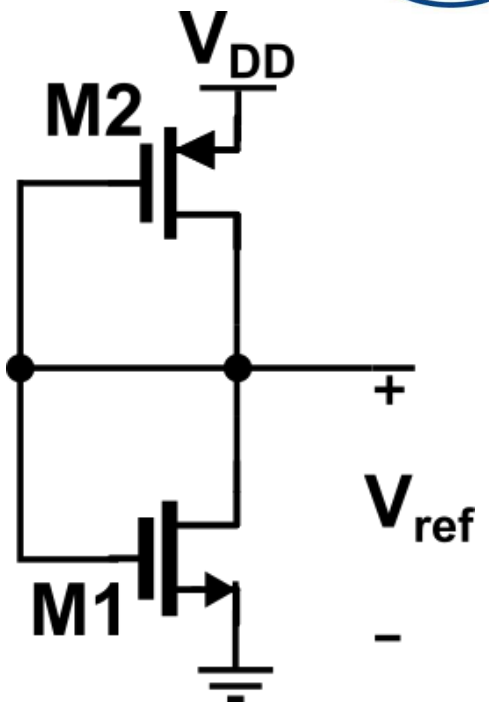
$$\frac{\beta_1}{2}\left(V_{ref}-VSS-V_{THN}\right)^2=\frac{\beta_2}{2}\left(VDD-V_{ref}-V_{THP}\right)^2$$

the reference voltage:

$$V_{ref}==\frac{VDD-V_{THP}+\sqrt{\beta_1/\beta_2}\,(VSS+V_{THN})}{\sqrt{\beta_1/\beta_2}+1}$$

or knowing the reference voltage and the power supply voltages gives

$$\frac{\beta_1}{\beta_2}=\left[\frac{VDD-V_{ref}-V_{THP}}{V_{ref}-VSS-V_{THN}}\right]^2$$



Design:

(1) determine the reference voltages needed;

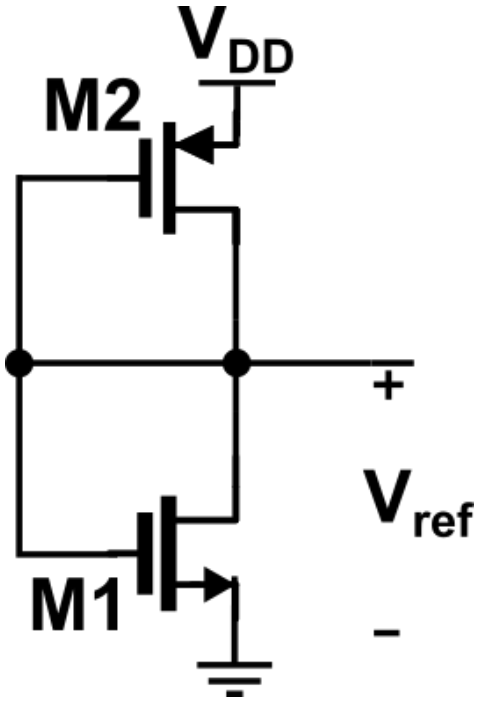
(2) select a drain current through the MOSFETs;

(3) solve for the size of the devices.

The MOSFET-only Voltage Divider

The sensitivity of V_{ref} to VDD

$$S_{VDD}^{V_{ref}} == \frac{VDD}{VDD - V_{THP} + \sqrt{\frac{\beta_1}{\beta_2}}(VSS + V_{THN})}$$



The temperature coefficient

assuming the temperature of the ratio of the transconductance parameters, β_1/β_2, is negligible,

$$TC(V_{ref}) = \frac{1}{V_{ref}} \cdot \frac{\partial V_{ref}}{\partial T}$$

$$= \frac{1}{V_{ref}} \cdot \frac{1}{\sqrt{\frac{\beta_1}{\beta_2}} + 1} \cdot \left[\frac{\partial(-V_{THP})}{\partial T} + \sqrt{\frac{\beta_1}{\beta_2}} \frac{\partial V_{THN}}{\partial T} \right]$$

Example

Design a 3V reference using the MOSFET-only voltage divider assuming VDD=+5V and VSS=0V. Determine the temperature coefficient of the reference and the power dissipation when $L_1=L_2=5\mu m$.

Solution: Assume $V_{THN}=0.8V$ and $V_{THP}=0.9V$

$$KP_n = 50\,\mu A/V^2,\ KP_p = 17\,\mu A/V^2$$

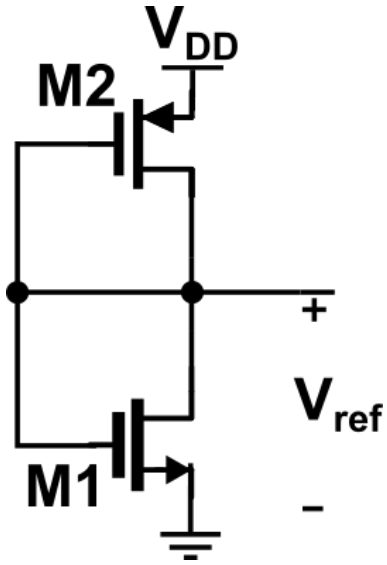
$$\frac{\beta_1}{2}\left(V_{ref}-VSS-V_{THN}\right)^2=\frac{\beta_2}{2}\left(VDD-V_{ref}-V_{THP}\right)^2$$

$$V_{ref}==\frac{VDD-V_{THP}+\sqrt{\beta_1/\beta_2}\,(VSS+V_{THN})}{\sqrt{\beta_1/\beta_2}+1} \quad\Rightarrow\quad \frac{\beta_1}{\beta_2}=\left[\frac{VDD-V_{ref}-V_{THP}}{V_{ref}-VSS-V_{THN}}\right]^2$$

determine the ratio of β_1 to β_2: $\frac{\beta_1}{\beta_2}=\left[\frac{5-3-0.9}{3-0-0.8}\right]^2=0.25$

Setting $L_1=L_2=W_1=5\mu m$ gives

$$\frac{KP_nW_1L_2}{KP_pW_2L_1}=\frac{(50\times10^{-6}\frac{A}{V^2})5\mu 5\mu}{(17\times10^{-6}\frac{A}{V^2})W_2 5\mu}=0.25 \quad\Rightarrow\quad W_2=60\mu m$$

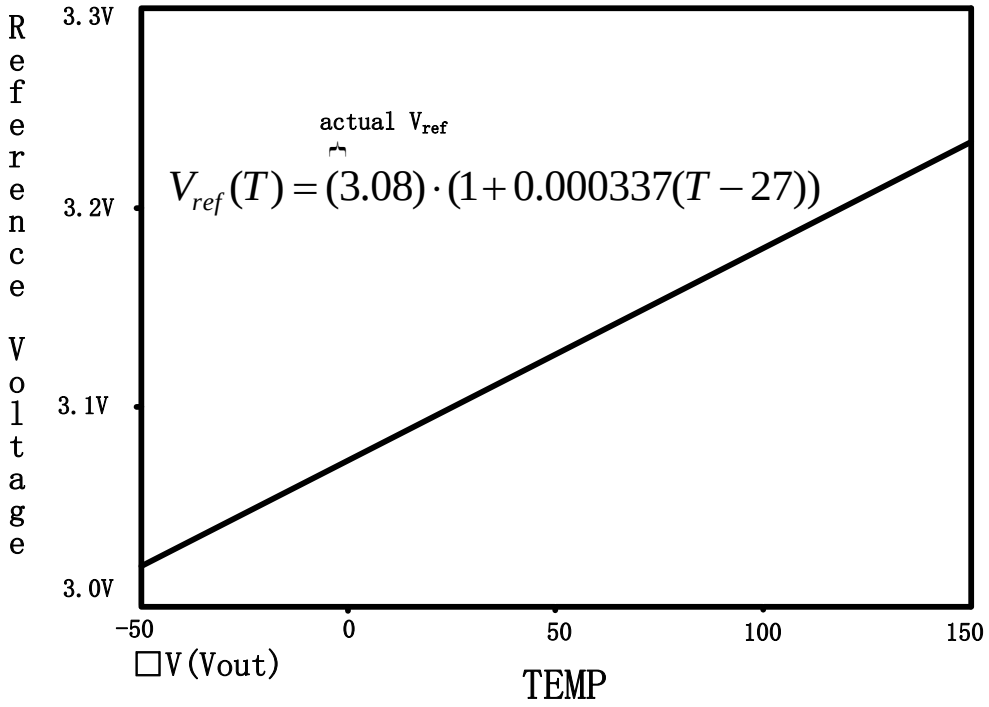


The temperature coefficient is given by

$$TC(V_{ref})=\frac{1}{3}\cdot\frac{1}{\sqrt{\frac{50\times5}{17\times60}}+1}\cdot\left[.0027+\sqrt{\frac{50\cdot5}{17\cdot60}}(-0.0024)\right]=337\,ppm/^\circ C$$

How many mV per degree ?

The MOSFET-only Voltage Divider



Trade-OFF!

- L=5μm →I_D=125μA ⟶ Power Dissipation 600μW
- L=50μm →I_D=12.5μA ⟶ Power Dissipation 60μW
- Devices larger→ ***Power*** Dissipation↓ → ***Area*** Bigger

Example

Design a 2V and a 3.5V voltage reference using the three-MOSFET voltage divider Assume that VDD=+5V, VSS=0V, the drain current of the MOSFETs is 10μA, and that $L_1=L_2=L_3=20\mu m$

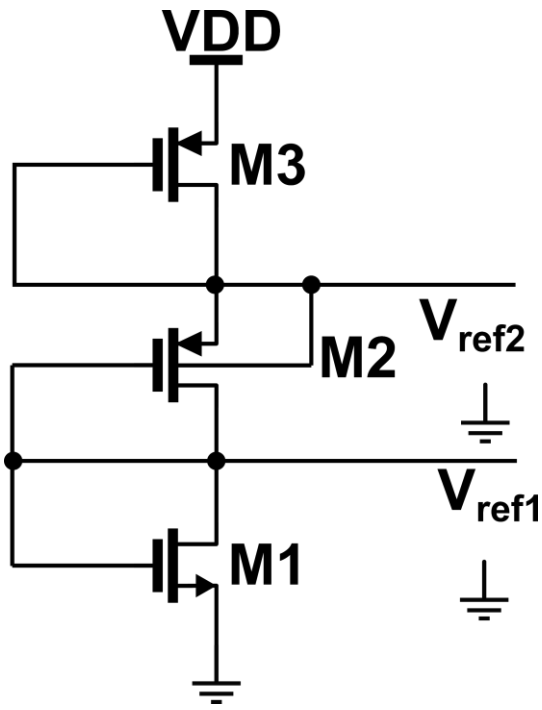
$KP_n = 50\,\mu A/V^2, KP_p = 17\,\mu A/V^2$

Solution:

Since V_{GS1}=2V, $10\mu A = \frac{KP_n}{2}\frac{W_1}{20\mu m}(2-0.8)^2 \Rightarrow W_1 \approx 5\mu m$

since V_{SG2}=1.5V, $10\mu A = \frac{KP_p}{2}\frac{W_2}{20\mu m}(1.5-0.9)^2 \Rightarrow W_2 \approx 65\mu m$

The width of M3, with V_{SG3}=1.5V, is also 65μm.



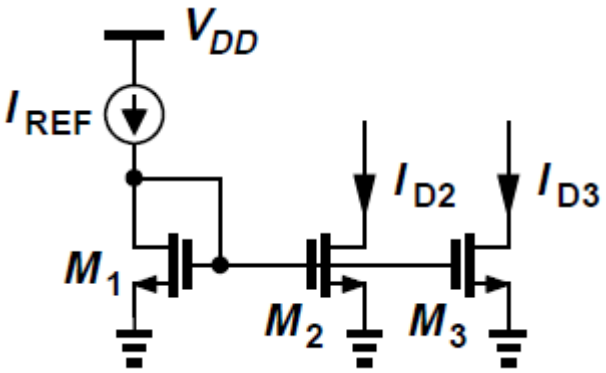
the area of the reference designed in Example (in Page. 36) (using the case when L=50μm and drain current is 12.5μA)

$$A_{Ex(P9)} = L_1W_1 + L_2W_2 = 3250\mu m^2$$

While the area needed in this example is 2700μm².

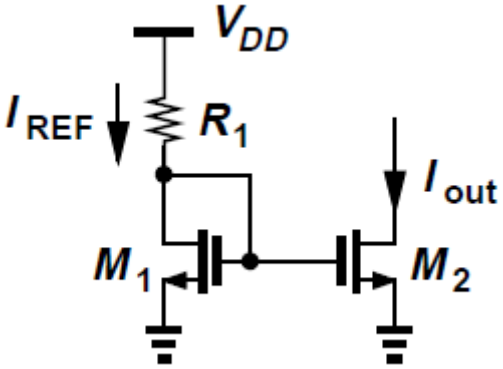
In addition, the power dissipation is slightly lower, 50μW, **when we use a second MOSFET.**

Bias Current Generation



- Ideal I_{REF} : be independent of V_{DD}
- Neglecting the channel-length modulation,
- I_{D2} and I_{D3}: independent of V_{DD}

How to generate I_{REF}?



$$\Delta I_{out} = \frac{\Delta V_{DD}}{R_1 + 1/g_m} \frac{(W/L)_2}{(W/L)_1}$$

Sensitive!

To arrive at a less sensitive solution, the circuit must bias itself, i.e., I_{REF} must somehow be derived from $I_{out.}$

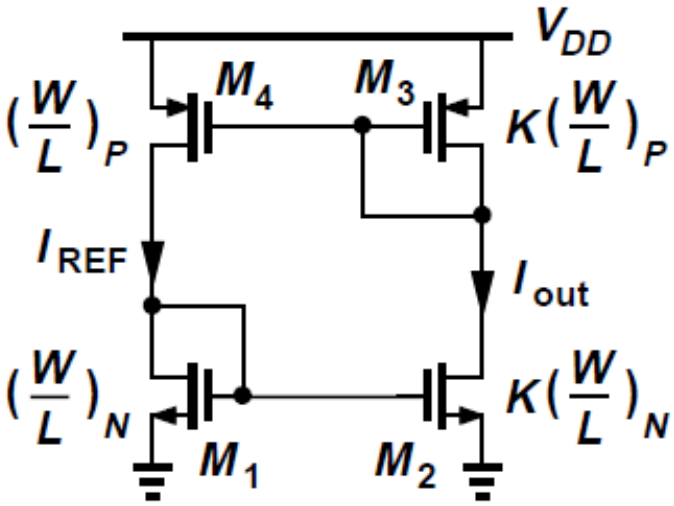
How to improve?

Self-Biasing

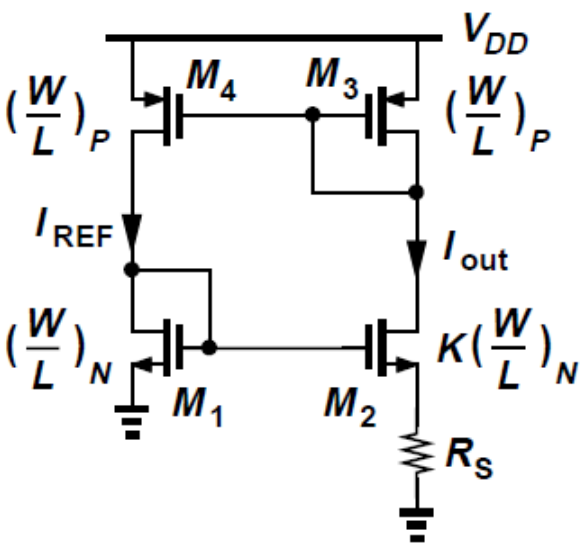
- If I_{out} is independent of V_{DD}, I_{REF} can be a replica of I_{out}
- M_3 and M_4 copy I_{out}, thus defining I_{REF}
- I_{REF} is "bootstrapped" to I_{out}
- Since each diode-connected device feeds from a current source, I_{out} and I_{REF} are relatively independent of V_{DD}

$$I_{out} = KI_{REF}$$

It can support any current level !



Self-Biasing



$$V_{GS1} = V_{GS2} + I_{D2}R_S$$

$$\sqrt{\frac{2I_{out}}{\mu_n C_{OX}(W/L)_N}} + V_{TH1} = \sqrt{\frac{2I_{out}}{\mu_n C_{OX} K (W/L)_N}} + V_{TH2} + I_{out}R_S$$

Neglecting body effect $V_{TH1} \approx V_{TH2}$ $(\gamma = 0)$

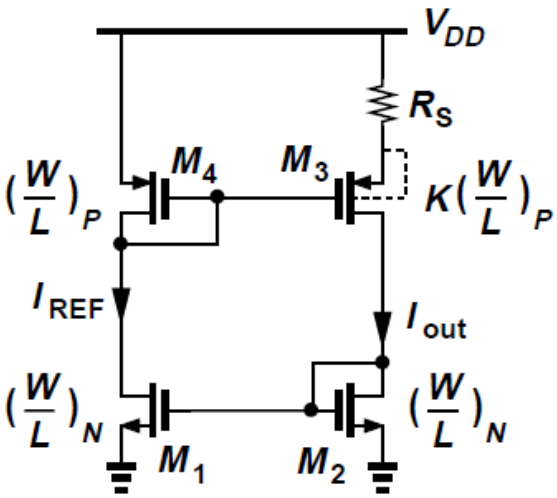
$$\sqrt{\frac{2I_{out}}{\mu_n C_{OX}(W/L)_N}}\left(1 - \frac{1}{\sqrt{K}}\right) = I_{out}R_S$$

$$I_{out} = \frac{2}{\mu_n C_{OX}(W/L)_N}\frac{1}{R_S^2}\left(1 - \frac{1}{\sqrt{K}}\right)^2$$

- **be independent of the V_{DD}**
- be dependent of R_S

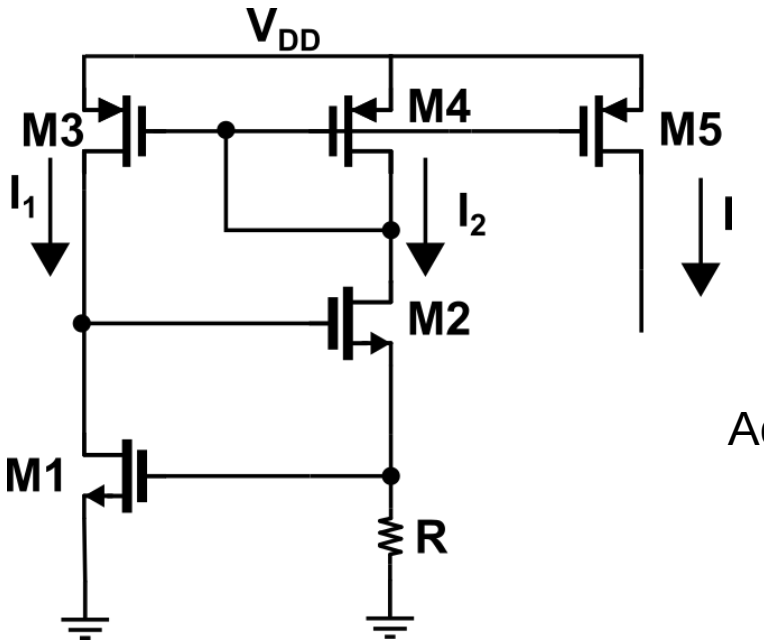
(but still a function of process and temperature)

- -- In fact, $V_{TH1} \neq V_{TH2}$ (**the body effect**)



N-Well, P-Sub
Eliminating Body Effect

Threshold Voltage Referenced Self-Biasing



Threshold reference self-biasing circuit

$$I_2 R = V_{GS1} = V_{THN} + \sqrt{\frac{2I_1}{\beta_1}}$$

$$= V_{THN} + \left(\frac{2I_1 L_1}{K'_N W_1}\right)^{1/2} \approx V_{THN}$$

$$I_O = I_2 \approx \frac{V_{THN}}{R}$$

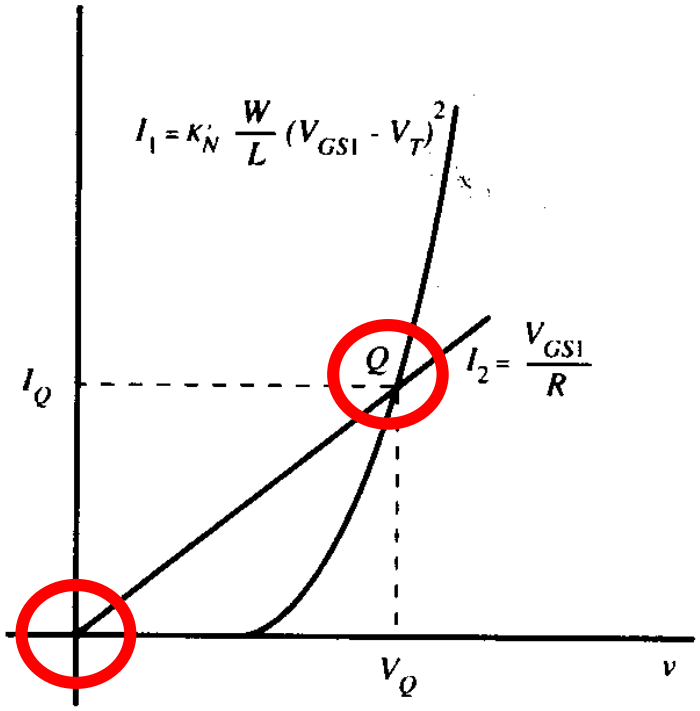
Accurate solution

$$I_2 R = V_{THN} + \left(\frac{2I_1 L_1}{K'_N W_1}\right)^{1/2}$$

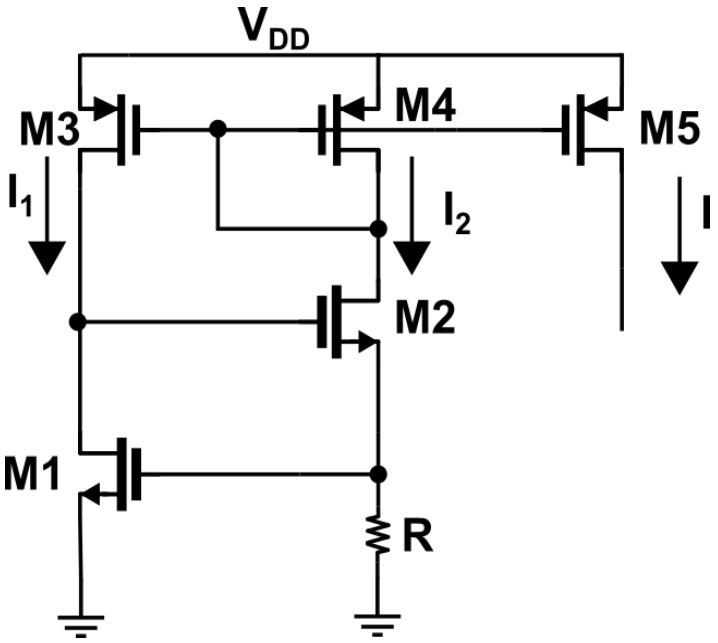
$$I_O = I_2 = \frac{V_{THN}}{R} + \frac{1}{\beta_1 R^2} + \frac{1}{R}\sqrt{\frac{2V_{THN}}{\beta_1 R} + \frac{1}{\beta_1^2 R^2}}$$

Independence of the power supply voltages

Startup Circuit

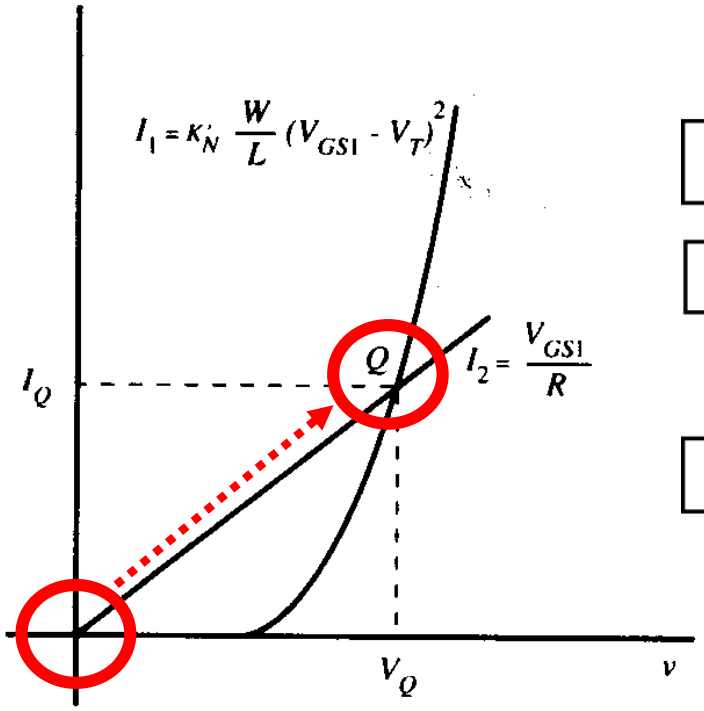


(a)

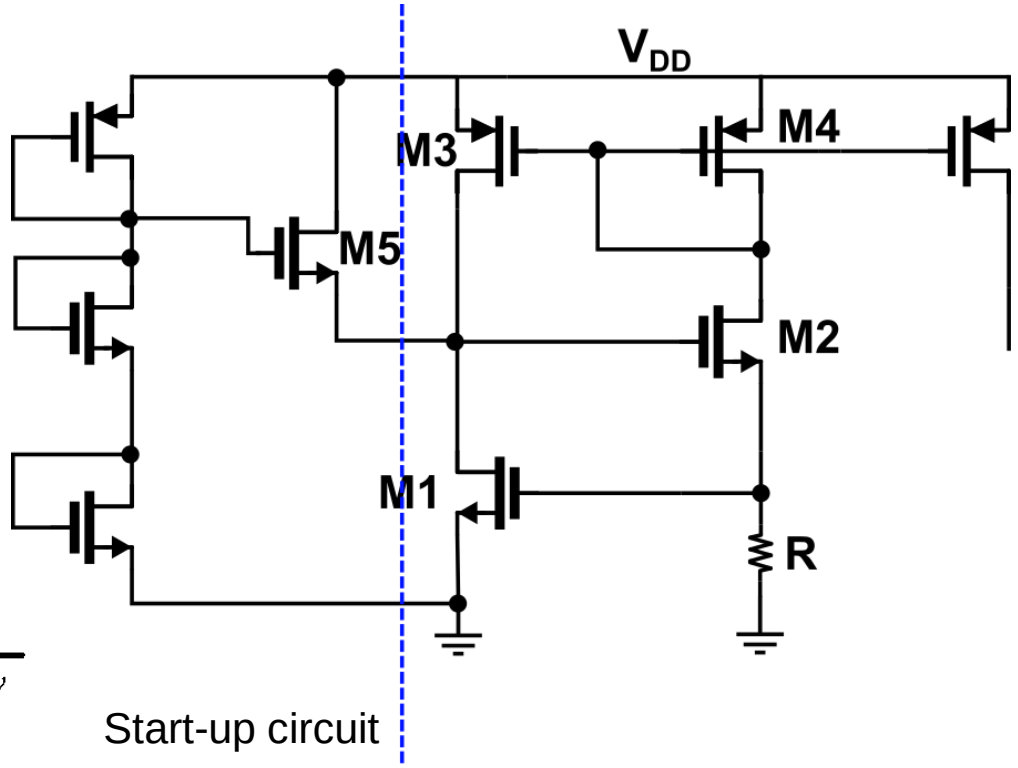


- Two possible operating points of self-biased circuit

Startup Circuit



(a)

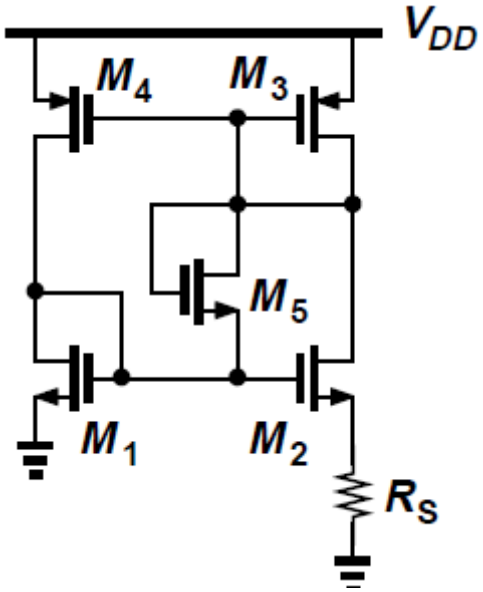


Start-up circuit

- Two possible operating points of self-biased circuit

Startup Circuit

- **Adding a circuit to drive the circuit out of degenerate bias point when supply is turned on**
- a current path: V_{DD} - M_3 - M_5 - M_1
- M_3 and M_1, and hence M_2 and M_4, cannot remain off
- After M_2 和 M_3 turn on, $V_{GS5} < V_{TH5}$, M_5 remains off after start-up



Temperature Independent Reference

- In IC technology, almost everything have temperature dependence (TC)
- If two voltages having opposite temperature coefficients (TCs) are added with proper weighting, the result displays a ZERO TC
- V_1 and V_2 that vary in opposite directions with temperature, we choose α_1 and α_2 such that $\alpha_1 \partial V_1/\partial T + \alpha_2 \partial V_2/\partial T = 0$, obtaining a reference voltage, $V_{REF} = \alpha_1 V_1 + \alpha_2 V_2$, with zero TC
- Characteristics of bipolar transistors have proven the most reproducible and well-defined quantities that can provide positive and negative TCs

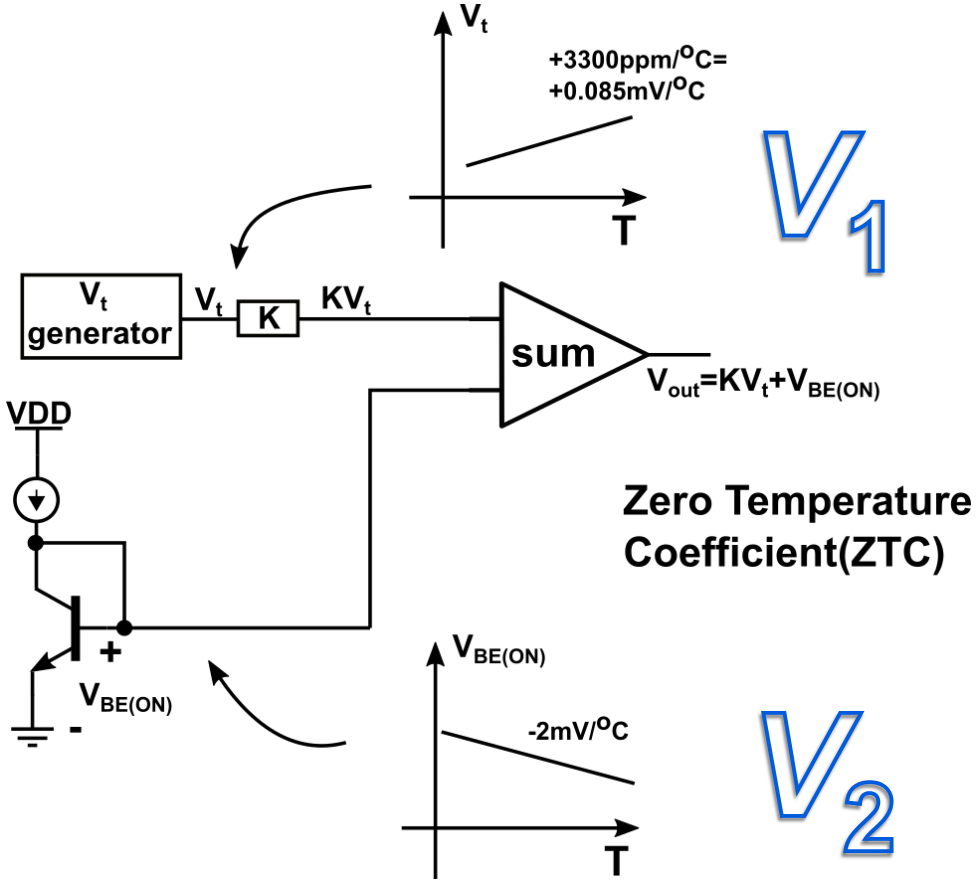
Temperature Independent Reference

- If two quantities having **opposite** **temperature coefficients (TCs)** are **added** with proper weighting, the result displays **a zero TC**

$$\alpha_1 \frac{\partial V_1}{\partial T} + \alpha_2 \frac{\partial V_2}{\partial T} = 0$$

>0 <0

$$V_{REF} = \alpha_1 V_1 + \alpha_2 V_2$$



Negative-TC Voltage

Forwards voltage of a diode

$$I_C = I_S \exp\left(V_{BE}/V_t\right) \qquad \text{or} \qquad V_{BE} = V_t \ln\left(I_C/I_S\right)$$

where $V_t = kT/q$

$$I_S \propto \mu k T n_i^{\,2}$$

$$\mu \propto \mu_0 T^m, \quad m \approx -3/2$$

$$n_i^{\,2} \propto T^3 \exp\left[-E_g/(kT)\right], \; E_g \approx 1.12eV$$

$$I_S = bT^{4+m} \exp\frac{-E_g}{kT}$$

Negative-TC Voltage

$$V_{BE} = V_t \ln\left(I_C / I_S\right) \Rightarrow \frac{\partial V_{BE}}{\partial T} = \frac{\partial V_t}{\partial T}\ln\frac{I_C}{I_S} - \frac{V_t}{I_S}\frac{\partial I_S}{\partial T}$$

$$I_S = bT^{4+m}\exp\frac{-E_g}{kT} \qquad \frac{\partial I_S}{\partial T} = b(4+m)T^{3+m}\exp\frac{-E_g}{kT} + bT^{4+m}\exp\left(\frac{-E_g}{kT}\right)\left(\frac{-E_g}{kT^2}\right)$$

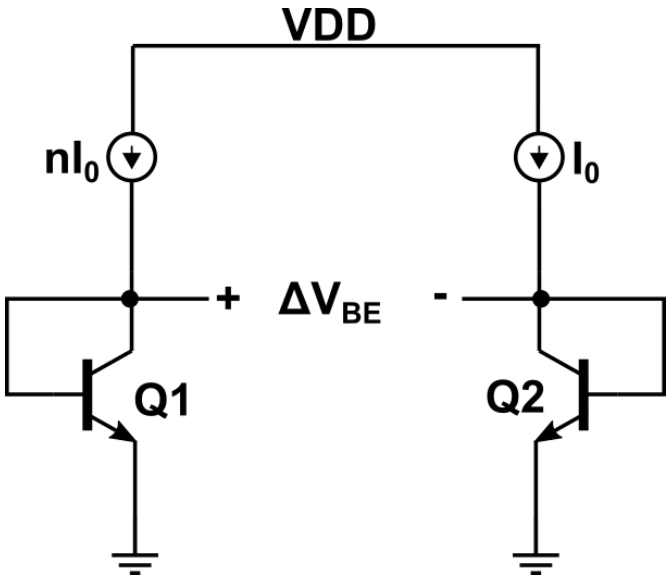
$$\Rightarrow \frac{V_t}{I_S}\frac{\partial I_S}{\partial T} = (4+m)\frac{V_t}{T} + \frac{E_g}{kT^2}V_t$$

$$\frac{\partial V_t}{\partial T} = \frac{k}{q} = \frac{V_t}{T}$$

$$\frac{\partial V_{BE}}{\partial T} = \frac{V_t}{T}\ln\frac{I_C}{I_S} - (4+m)\frac{V_t}{T} - \frac{E_g}{kT^2}V_t = \frac{V_{BE} - (4+m)V_t - E_g/q}{T}$$

$$T = 300K \quad V_{BE} = 600mV \quad \frac{\partial V_{BE}}{\partial T} \approx -2\,mV/K$$

Positive-TC Voltage



Generation of PTAT voltage

$$\Delta V_{BE} = V_{BE1} - V_{BE2}$$

$$= V_t \ln \frac{nI_0}{I_{S1}} - V_t \ln \frac{I_0}{I_{S2}}$$

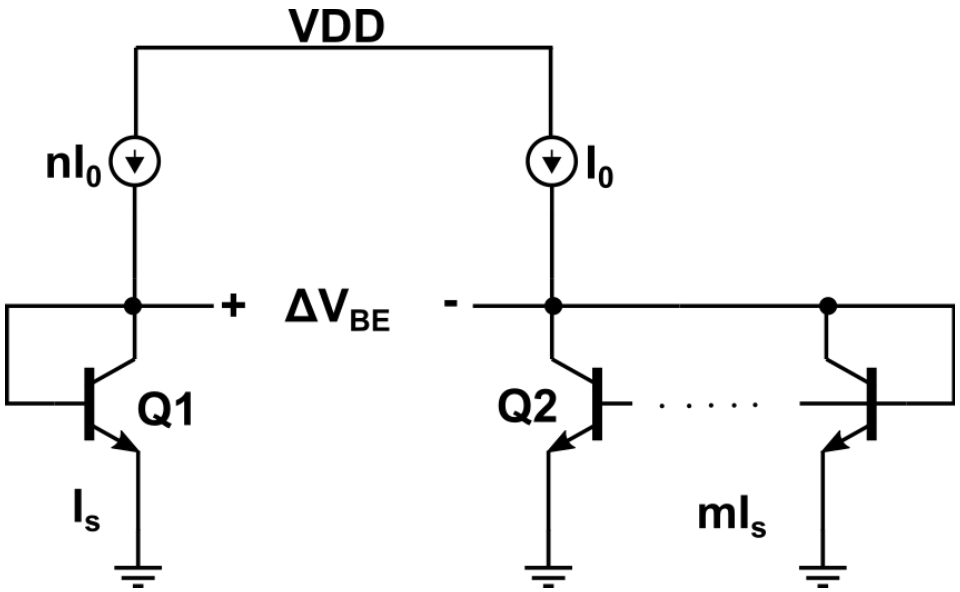
$$= V_t \ln n$$

$$\frac{\partial \Delta V_{BE}}{\partial T} = \frac{k}{q} \ln n$$

If two bipolar transistors work under different current density, their base-emitter junction voltage difference is

Proportional To the Absolute Temperature (PTAT)

Positive-TC Voltage



$$\Delta V_{BE} = V_{BE1} - V_{BE2}$$

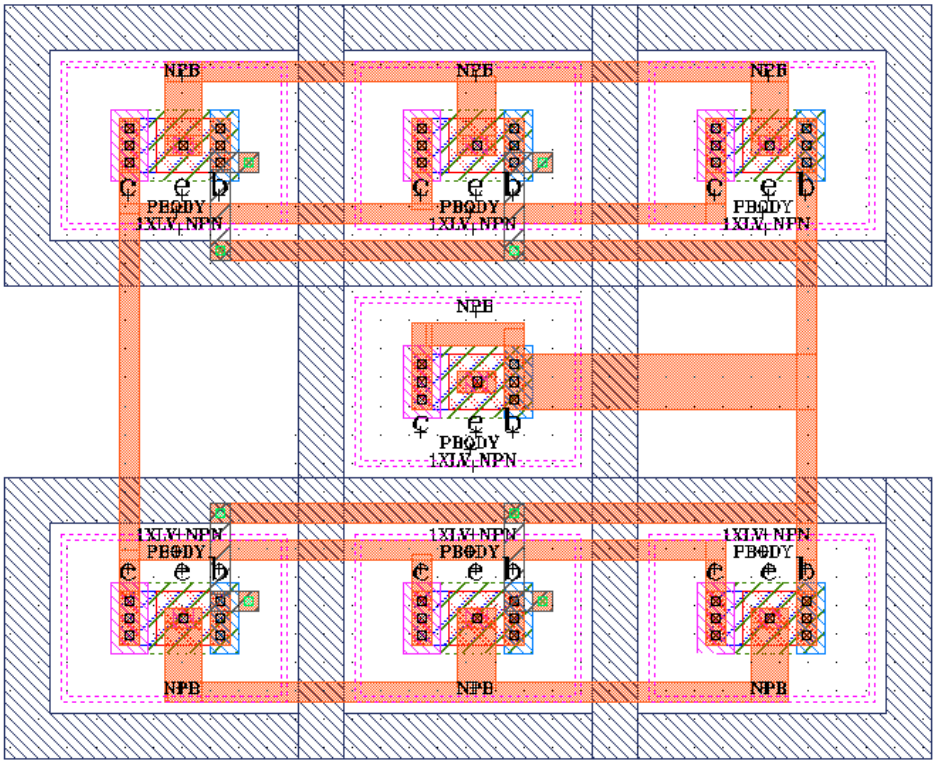
$$= V_t \ln \frac{nI_0}{I_{S1}} - V_t \ln \frac{I_0}{mI_{S2}}$$

$$= V_t \ln (nm)$$

$$\frac{\partial \Delta V_{BE}}{\partial T} = \frac{k}{q} \ln nm$$

Layout

1:6 Bipolar Layout

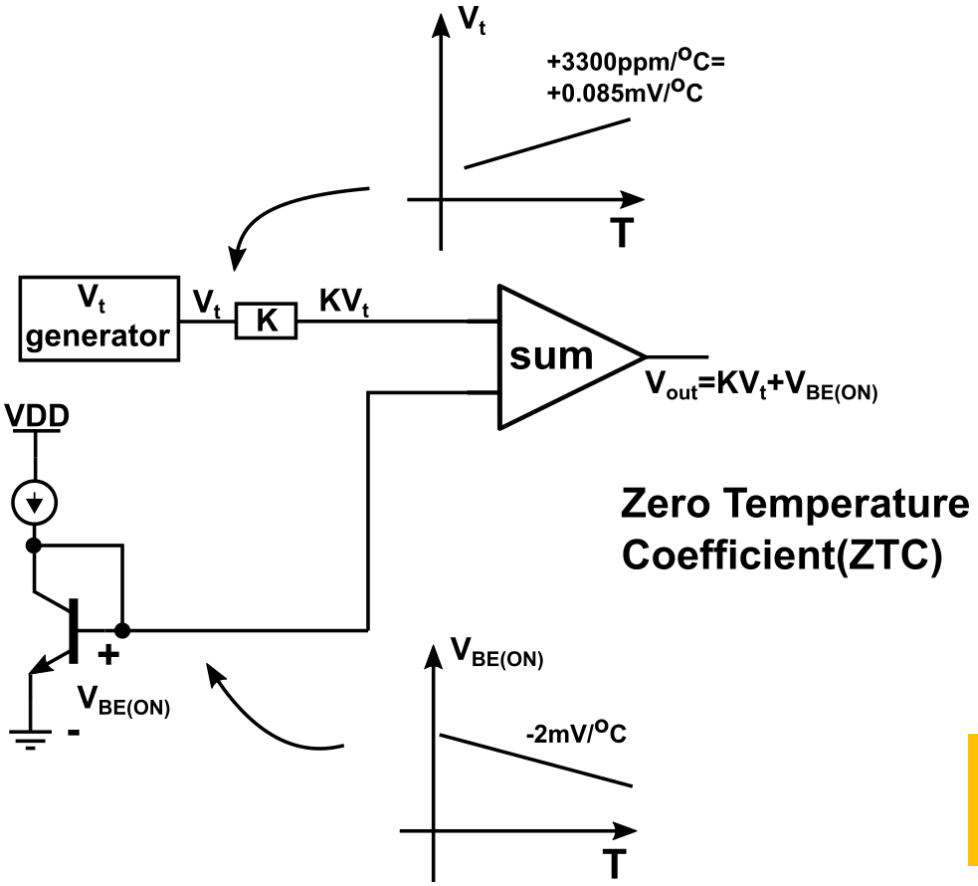


Symmetry !

Symmetry !

Symmetry !

Bandgap Reference (BGR)



Zero Temperature Coefficient(ZTC)

$$V_{REF} = V_{BE} + KV_t$$

$$\frac{\partial V_{BE}}{\partial T} \approx -2\,mV/K$$

$$\frac{\partial V_t}{\partial T} = \frac{k}{q} = 0.085mV/^\circ C$$

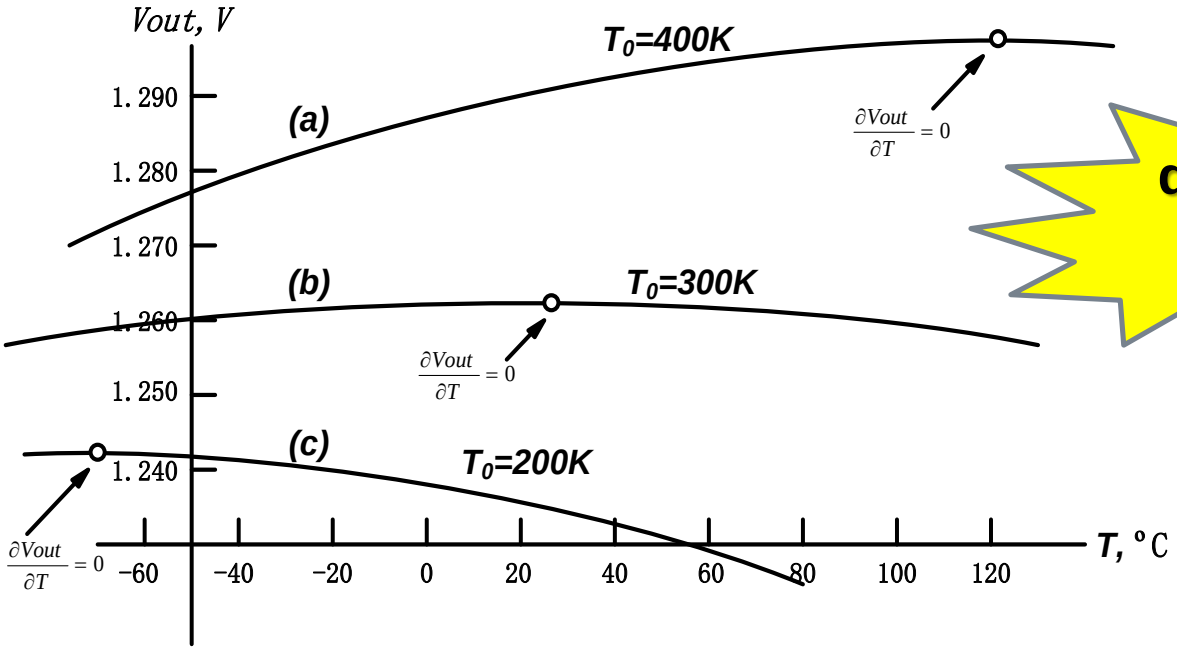
$$K \cdot \left(0.085mV/^\circ C\right) = 2\,mV/^\circ C$$

$$\therefore \quad K = 23.5$$

$$V_{REF} = V_{BE} + 23.5V_t \approx 1.2V$$

Curvature

- Bandgap voltages exhibit a finite “curvature”:
  - the TC is zero at one temperature and positive or negative at others
  - Curvature arises from temperature variation of base-emitter voltages, collector currents, offset voltages

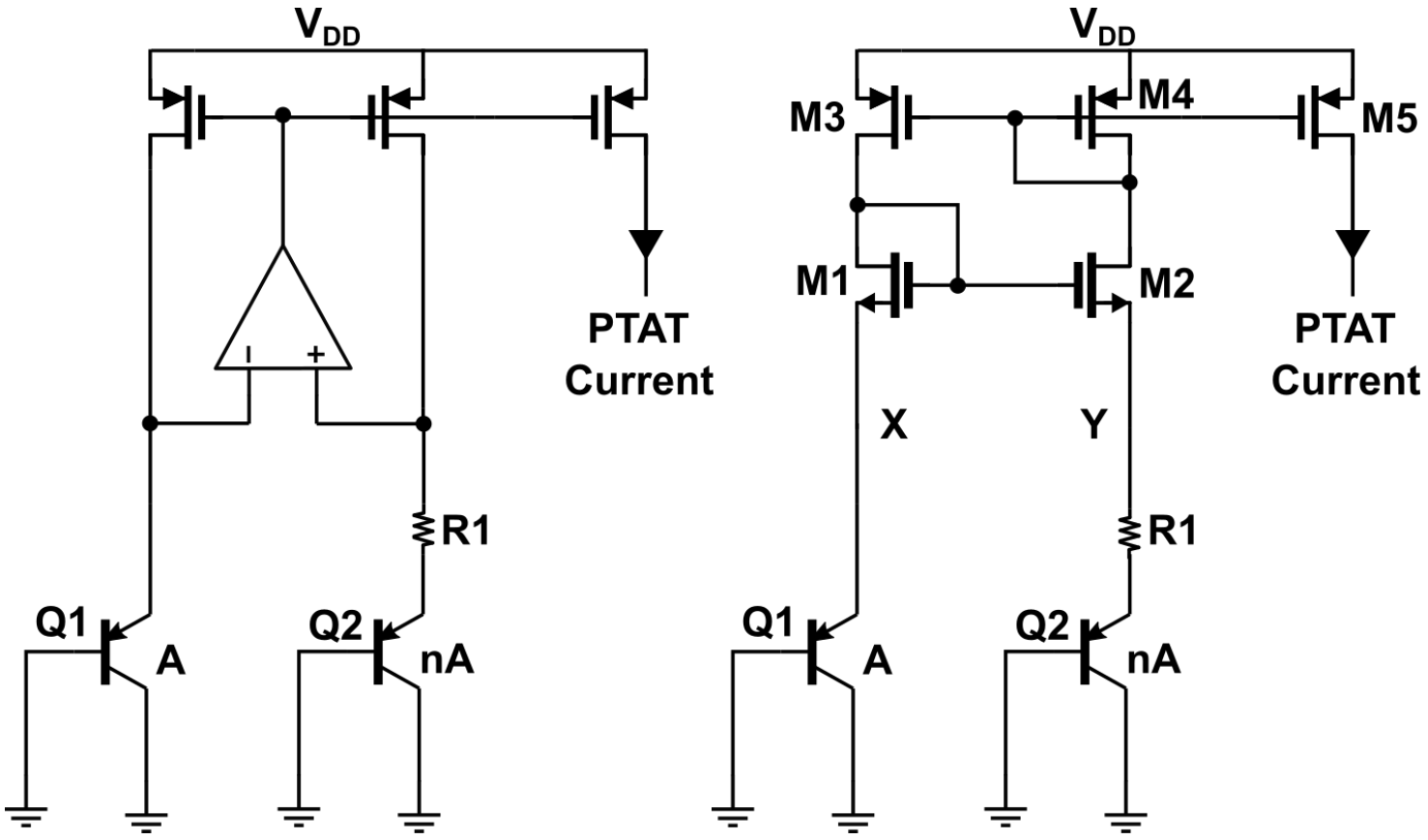


dozens of ppm/℃

Variation of band-gap reference output voltage with temperature

PTAT Current Generation

- Proportional To Absolute Temperature



PTAT Current Generation

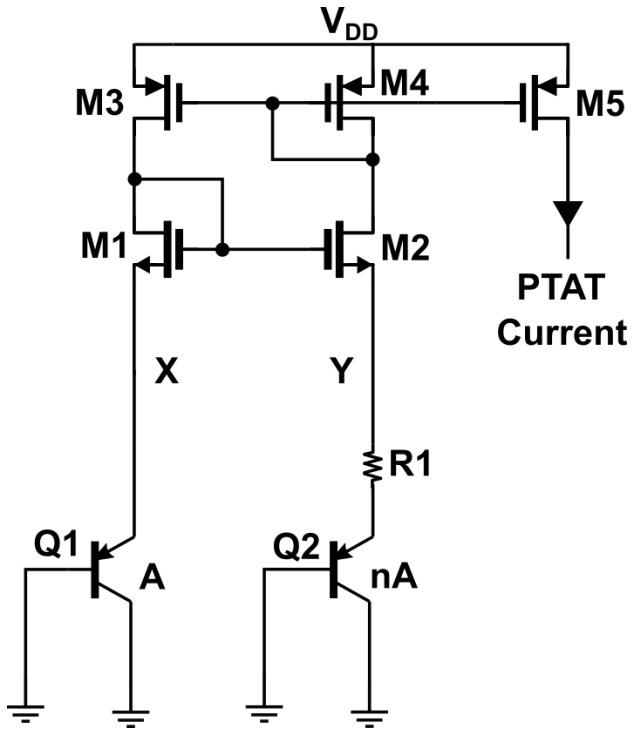
$$\Delta V_{BE} = V_{BE1} - V_{BE2} = V_t \ln\left(\frac{I_1}{I_{S1}}\right) - V_t \ln\left(\frac{I_2}{I_{S2}}\right)$$

$$\frac{A_{E2}}{A_{E1}} = n \qquad \frac{I_{S2}}{I_{S1}} = n$$

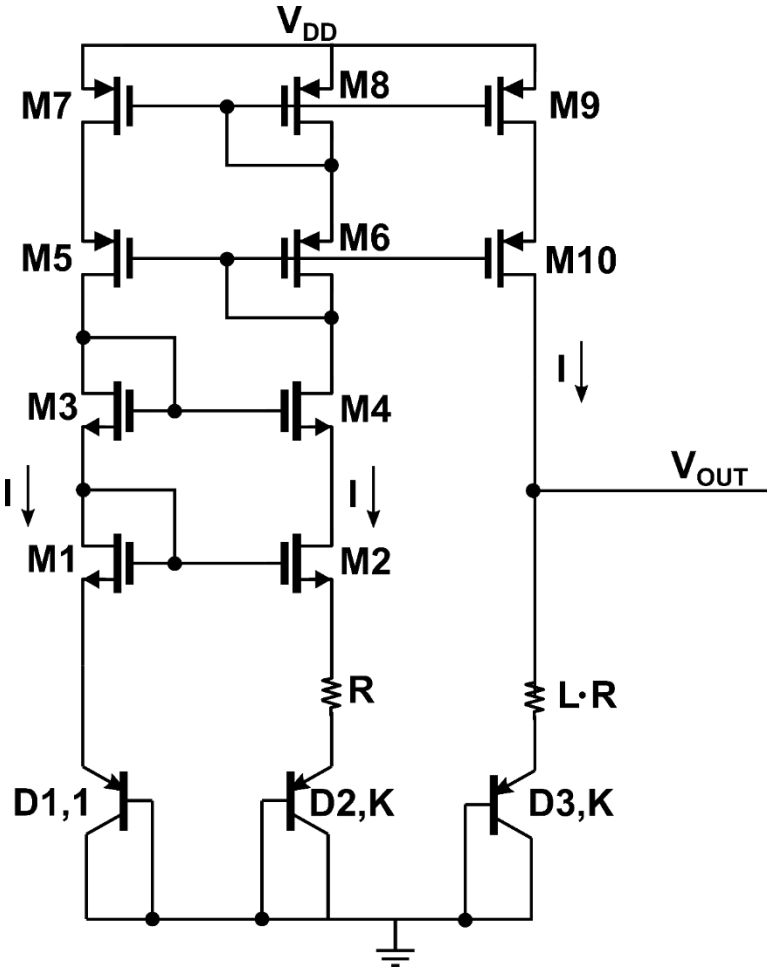
$$V_R = \Delta V_{BE} = V_t \ln\left(\frac{I_1}{I_{S1}} \cdot \frac{I_{S2}}{I_2}\right)$$

$$= V_t \ln\left(\frac{I_{S2}}{I_{S1}}\right) = V_t \ln\left(\frac{A_{E2}}{A_{E1}}\right) = V_t \ln n$$

$$I_O = I_2 = \frac{\Delta V_{BE}}{R} = \frac{V_t}{R} \ln n$$



Example



Requires startup circuit

A bandgap voltage reference

$$V_{ref} = V_{EB3} + I \times LR$$

$$= V_{EB3} + \frac{V_t \ln K}{R} \times LR$$

$$= V_{EB3} + LV_t \ln K$$

ZTC?

Example

The TC of the bandgap voltage reference is zero when

$$\frac{\partial V_{ref}}{\partial T} = L \cdot \ln K \cdot \underbrace{\frac{\partial V_t}{\partial T}}_{0.085mV/^\circ C} + \underbrace{\frac{\partial V_{EB3}}{\partial T}}_{-2mV/^\circ C} = 0$$

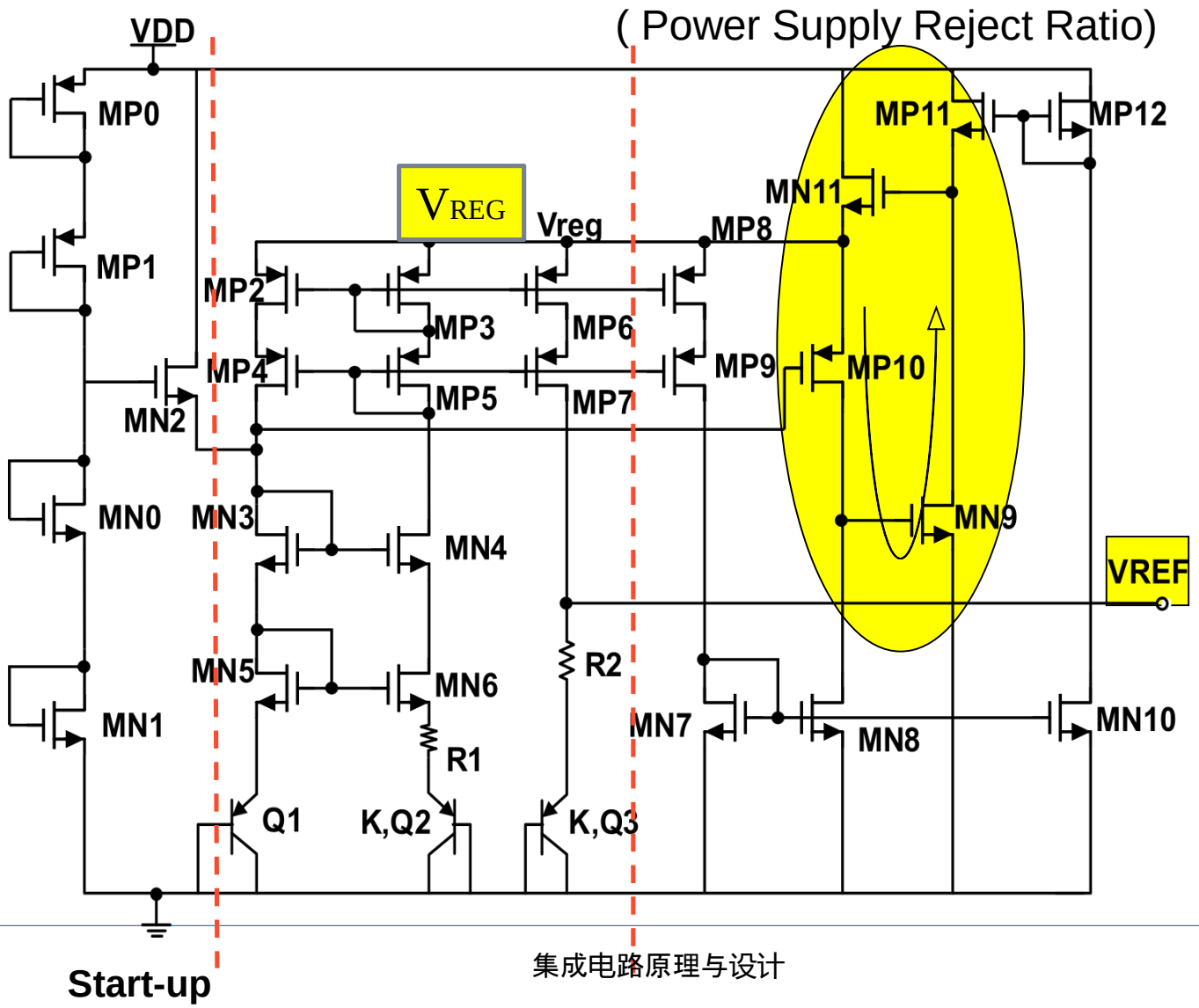
This is true when $L \cdot \ln K = \frac{2}{0.085} = 23.5$

For K=8, the factor L is 11.3 for a zero TC. We will round L up to 12 for the design here. The reference voltage, with respect to VSS, may also be written as

$$V_{ref} = \left(L \cdot \ln K\right) \cdot V_t + V_t \cdot \ln \frac{I}{K \cdot I_s}$$

The reference voltage at 300ºK for I=10uA, Is=10e-15A, K=8,and L=12 is 1.25V (i.e., Vref=1.25 if VSS=0 and VDD=5V).

Case Study


VDD
(Power Supply Reject Ratio)
MP0
MP1
MP2
MP3
MP4
MP5
MP6
MP7
MP8
MP9
MP10
MP11
MP12
MN0
MN1
MN2
MN3
MN4
MN5
MN6
MN7
MN8
MN9
MN10
VREG
Vreg
R1
R2
Q1
K,Q2
K,Q3
VREF
Start-up

Principles

$$V_{REG} = V_{BE1} + V_{GSN5} + V_{GSN3} + V_{GSP10}$$

- $VDD \uparrow \rightarrow V_{REG} \uparrow$

  $\rightarrow V_{SMP10} \uparrow \rightarrow V_{DMP10} \uparrow \rightarrow V_{GMN9} \uparrow$

  $\rightarrow V_{DMN9} \downarrow \rightarrow V_{GMN11} \downarrow$

  $\rightarrow V_{REG} \downarrow$

  The *PSRR* of the output reference voltage is improved correspondingly.

- Internal amplifier mainly consists of *MP10*, *MN9* and *MN11*, are used to amplify while *MN11* is mainly used as buffer and isolation to ensure the stability of current supply.
- Cascode current mirror:
  - Prevent the bottom transistor from the impact of the load thus decrease the mismatch caused by the channel length modulation effect.

集成电路原理与设计
6.电流镜与基准

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