集成电路原理与设计

11. 导线

Wire

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Syllabus

课数	内容	课数	内容
1	导论	9	差分放大器
2	器件模型	10	运算放大器
3	电容特性，小信号模型	11	导线
4	工艺流程	12	反相器
5	模拟基本单元	13	组合逻辑
6	电流镜与基准	14	时序逻辑
7	单级放大器	15	集成电路专题讲座一
8	课堂测验	16	集成电路专题讲座二

Goals

- Understanding the design metrics that govern digital design is crucial
- Determining and quantifying interconnect parameters
- Introducing circuit models for interconnect wires
- Technology scaling and its impact on interconnect

Design metrics of the gate

- ***Cost:*** *complexity, area*
- ***Integrity and robustness:*** *static (or steady-state) behavior*
- ***Performance:*** *dynamic (or transient) response*
- ***Energy efficiency:*** *energy and power consumption*

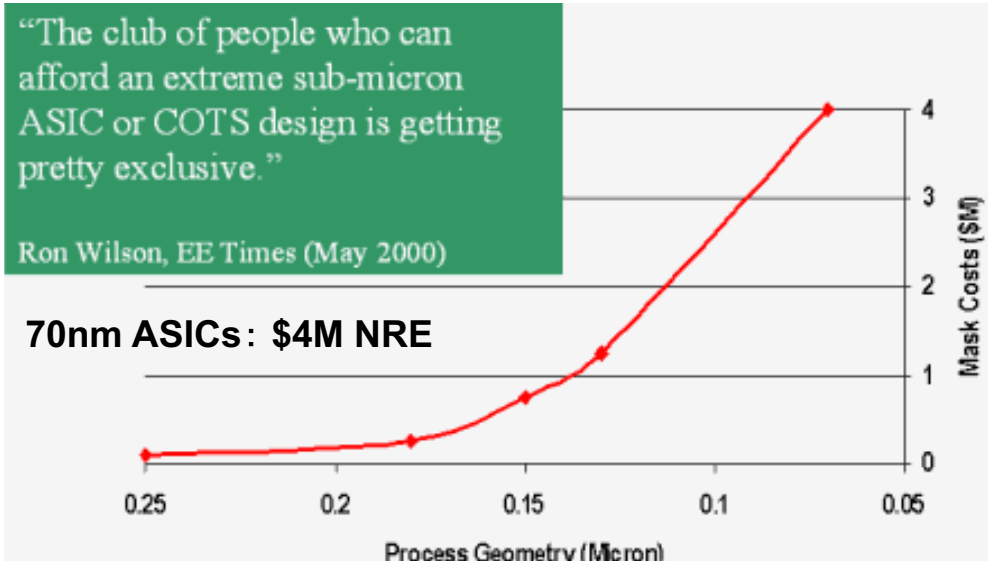
Outline

- Review: Quantity Metrics of Digital Design
- Wire: A First Glance
- Interconnect Parameters: R, C, L
- Electrical Wire Models

Cost

- NRE (non-recurrent engineering) cost or *fixed cost*
  - Design Time and Effort, Mask Generation
  - One-time Cost Factor
- Recurrent cost or *variable cost*
  - Silicon Processing, Packaging, Test
  - Proportional to Volume
  - Proportional to Chip Area

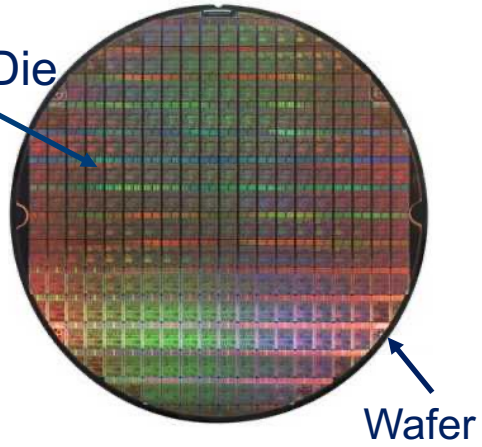
Cost per IC = variable cost per IC + fixed cost/volume



-- Yield（良率，成品率）

up to 12″ (30cm)

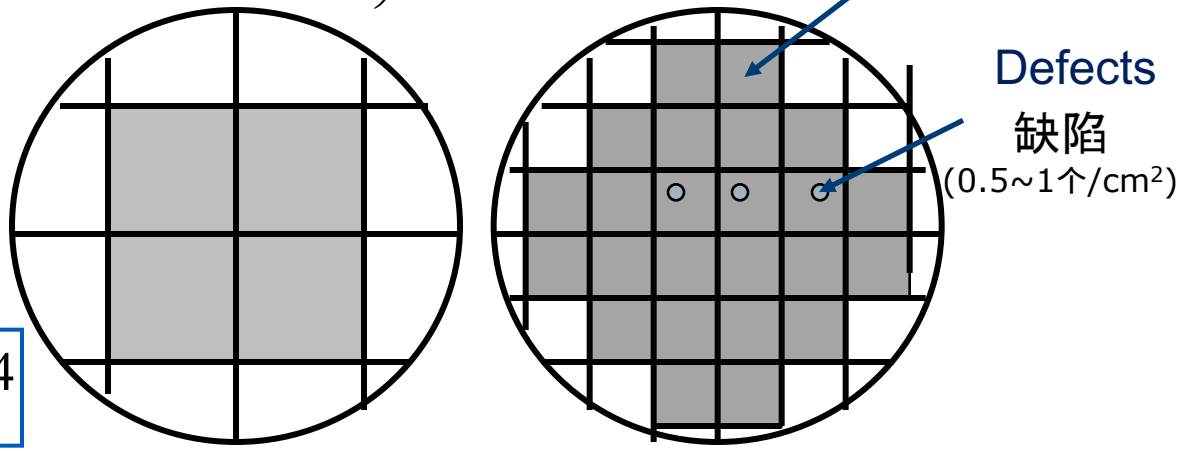
Yield: $Y = \frac{\text{No. of good chips per wafer}}{\text{Total number of chips per wafer}} \times 100\%$



$$\text{Die cost} = \frac{\text{Wafer cost}}{\text{Dies per wafer} \times \text{Die yield}}$$

$$\text{Dies per wafer} = \frac{\pi \times (\text{wafer diameter}/2)^2}{\text{die area}} - \frac{\pi \times \text{wafer diameter}}{\sqrt{2 \times \text{die area}}}$$

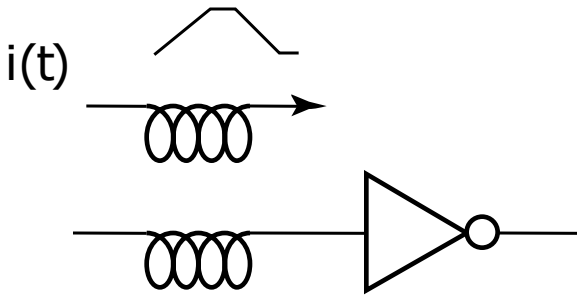
$$\text{die yield} = \left(1 + \frac{\text{defects per unit area} \times \text{die area}}{\alpha}\right)^{-\alpha} \quad (\alpha \approx 3)$$



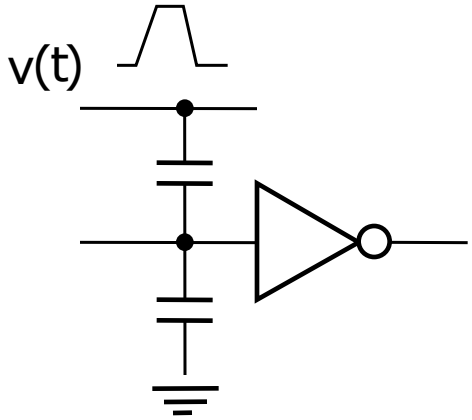
$$\text{die cost} = f(\text{die area})^4$$

Reliability – Noise

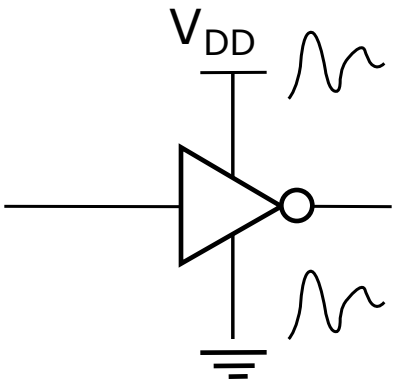
Noise*: unwanted variation* of voltages and currents at the logic node.



Inductive coupling



Capacitive coupling

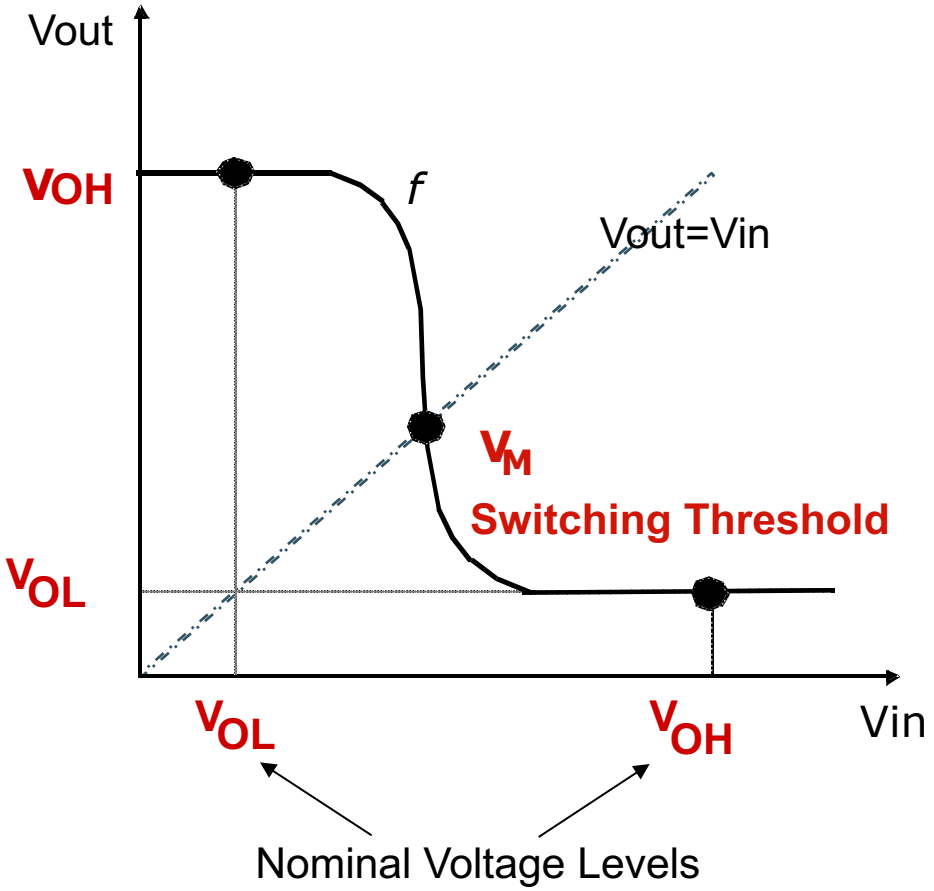


Power and GND

How to cope with all these disturbances is one of the main challenges in the design of high-performance digital circuits.

-- Voltage Transfer Characteristic (VTC)

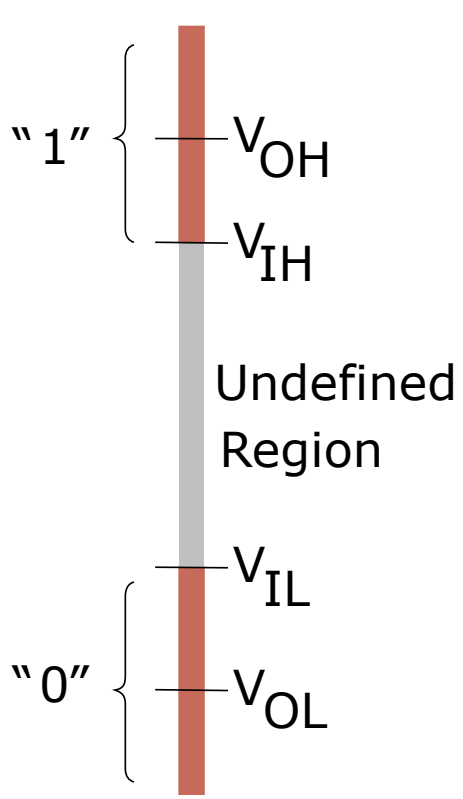
- VTC or DC operation for an inverting gate

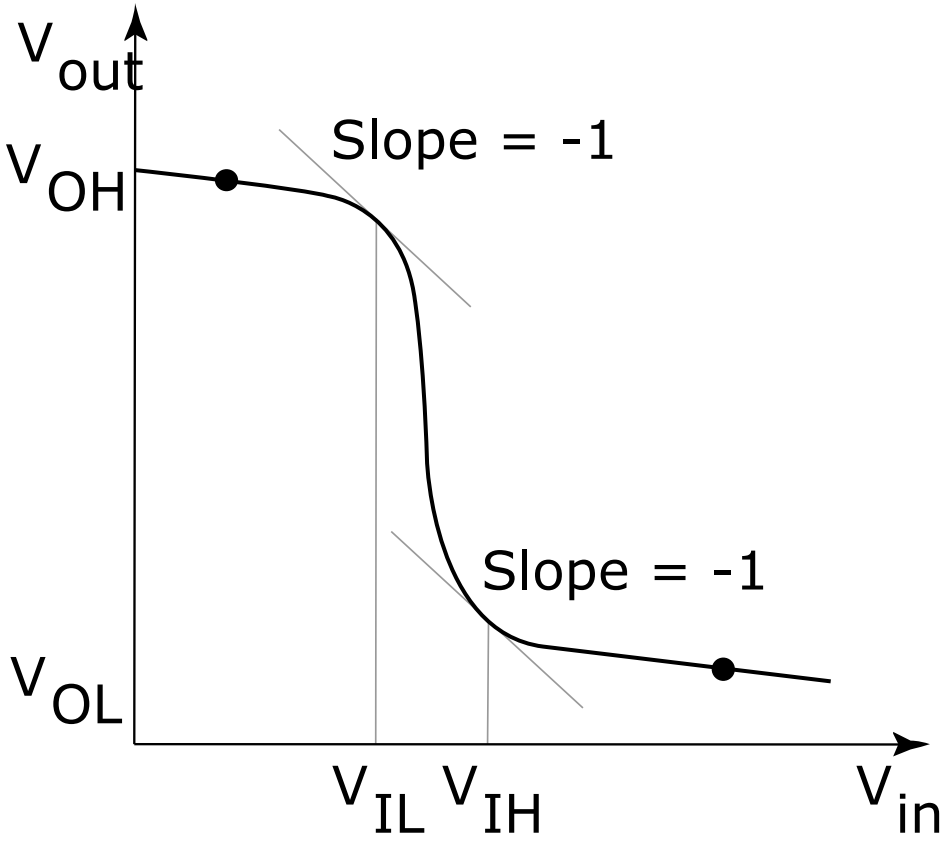


$$V_{OH} = f(V_{OL})$$
$$V_{OL} = f(V_{OH})$$
$$V_M = f(V_M)$$

Relationship between voltage and logic levels

- A range of acceptable voltages

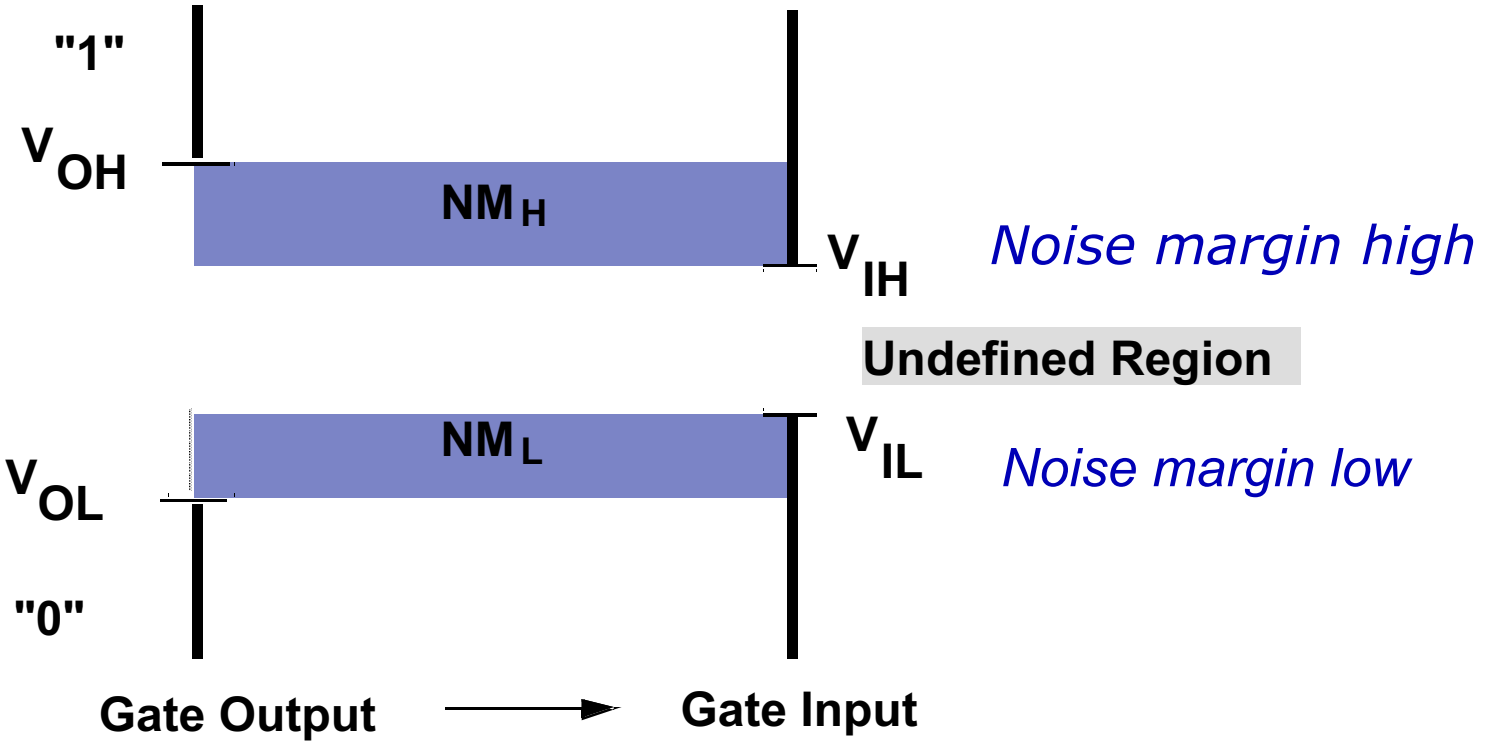




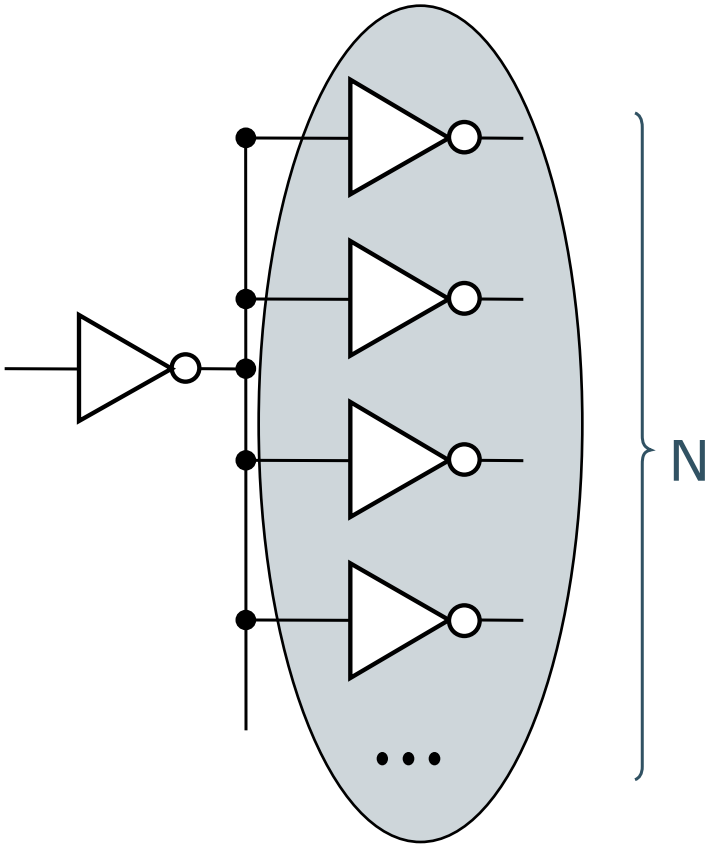
Undefined region (Transition width, TW)

-- Noise Margin

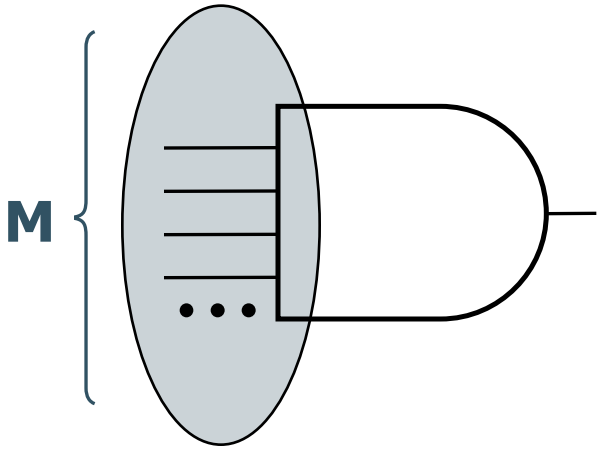
- “0” and “1” intervals be as large as possible => robust and intensive to noise disturbances
- Noise margin: the levels of noise that can be sustained when gates are cascaded.



-- Fan-in and Fan-out

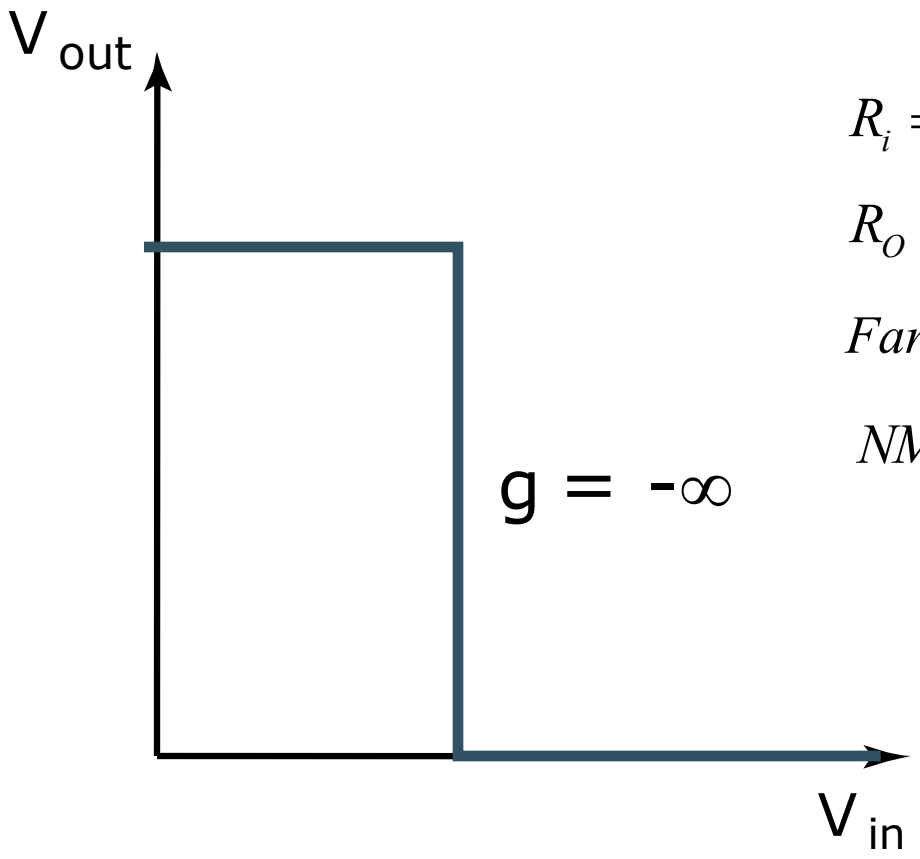


Fan-out N



Fan-in M

-- Ideal Gate



$$R_i = \infty$$

$$R_O = 0$$

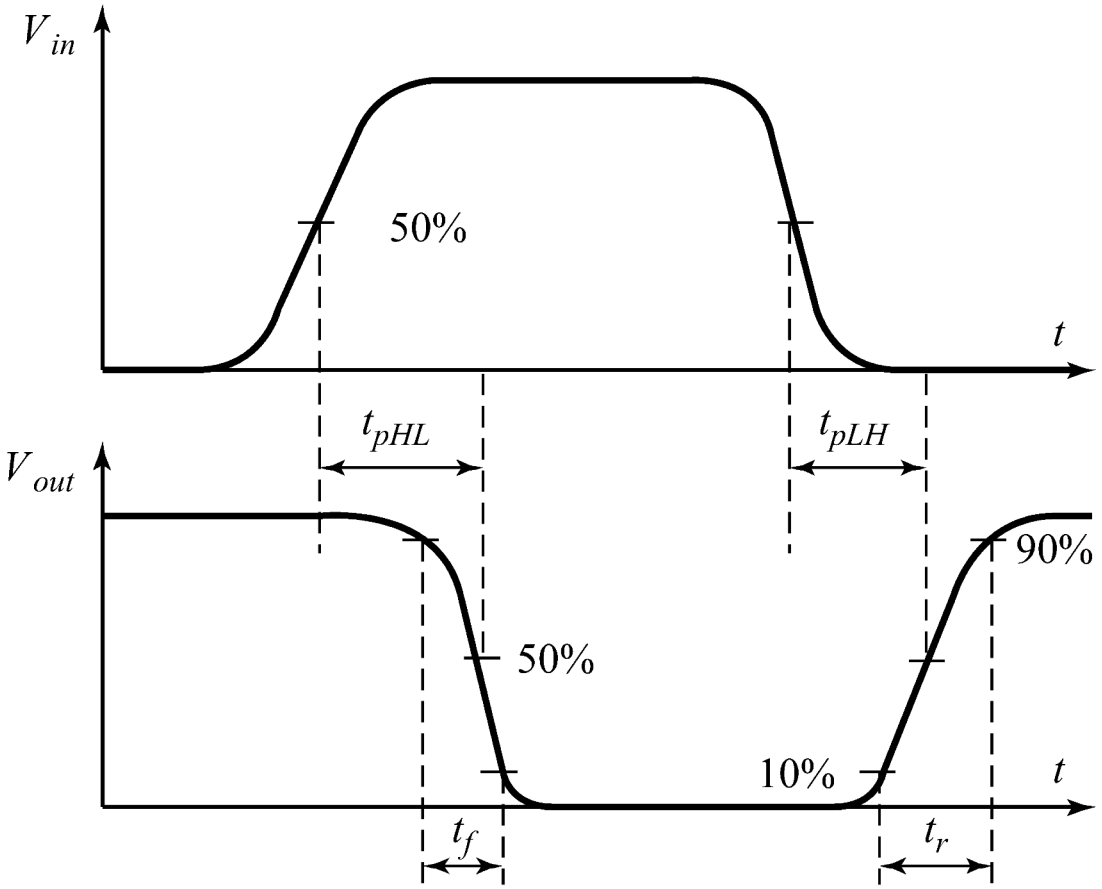
$$Fanout = \infty$$

$$NM_H = NM_L = V_{DD}/2$$

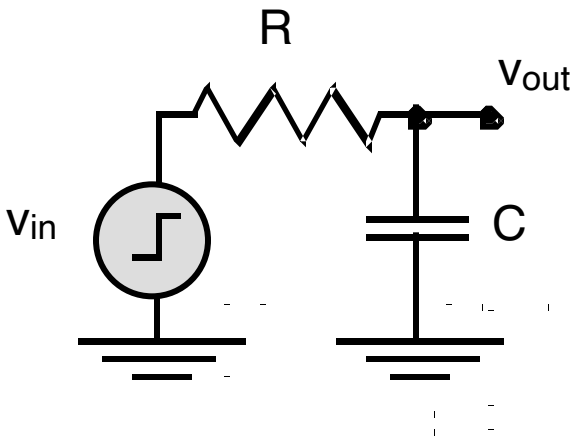
Speed: Delay Definition

- Propagation delay $t_p = \frac{t_{pLH} + t_{pHL}}{2}$

- t_f t_r



Example: *First-order RC network*



$$v_{out}(t) = (1 - e^{-t/\tau})\ V$$

$$t_p = \ln(2)\ t = 0.69\ RC$$

$$t_{0.1\text{-}0.9} = \ln(9)\ t = 2.2\ RC$$

Power Dissipation

- Instantaneous power:

$$p(t) = v(t)i(t) = V_{supply}i(t)$$

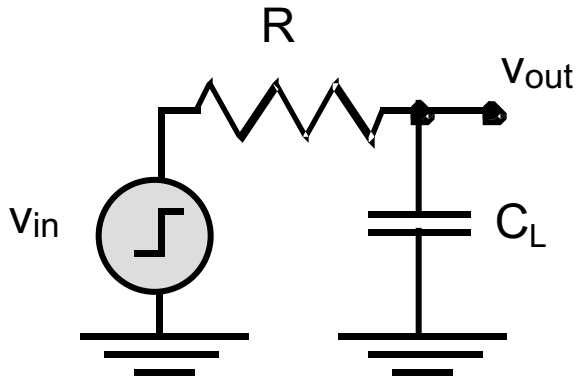
- Peak power:

$$P_{peak} = V_{supply}i_{peak}$$

- Average power:

$$P_{ave} = \frac{1}{T}\int_{t}^{t+T} p(t)dt = \frac{V_{supply}}{T}\int_{t}^{t+T} i_{supply}(t)dt$$

Example: *First-order RC network*



$$E_{0\to 1} = \int_0^T P(t)dt = V_{dd}\int_0^T i_{supply}(t)dt = V_{dd}\int_0^{Vdd} C_L dV_{out} = C_L \bullet V_{dd}^2$$

$$E_{cap} = \int_0^T P_{cap}(t)dt = \int_0^T V_{out} i_{cap}(t)dt = \int_0^{Vdd} C_L V_{out} dV_{out} = \frac{1}{2} C_L \bullet V_{dd}^2$$

- The other half is dissipated as heat in the R

Interconnect

电子系统中的互连线

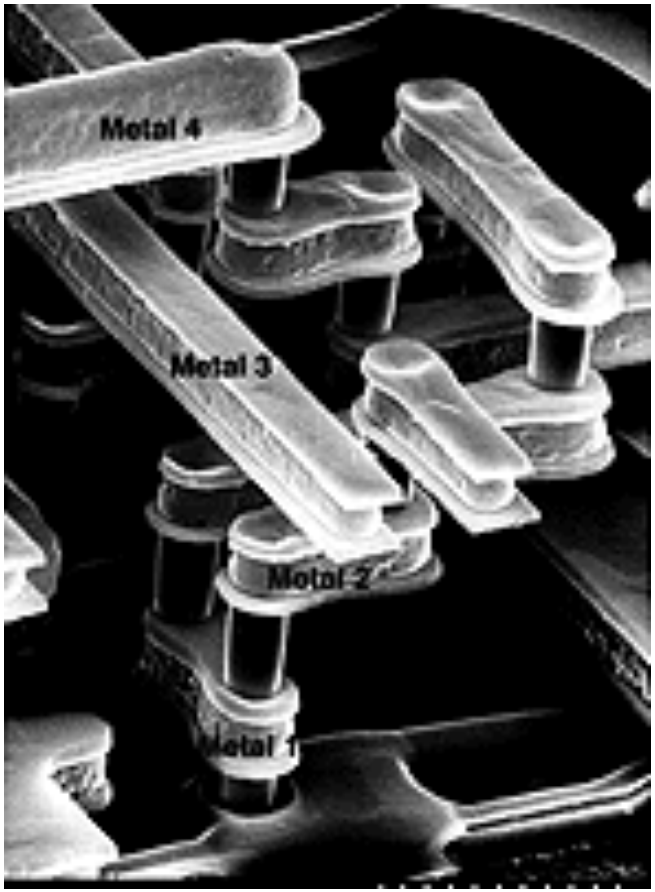
同轴电缆　三层平带线　微带线　导线在接地平面上

$$CL = \varepsilon\mu$$

C：电容，*L*：电感

	W	R	C	L
芯片上互连线	0.6μm	150kΩ/m	200pf/m	600nH/m
PC板上互连线	150μm	5Ω/m	100pf/m	300nH/m
美国标准双股线	511μm	0.08Ω/m	40pf/m	400nH/m

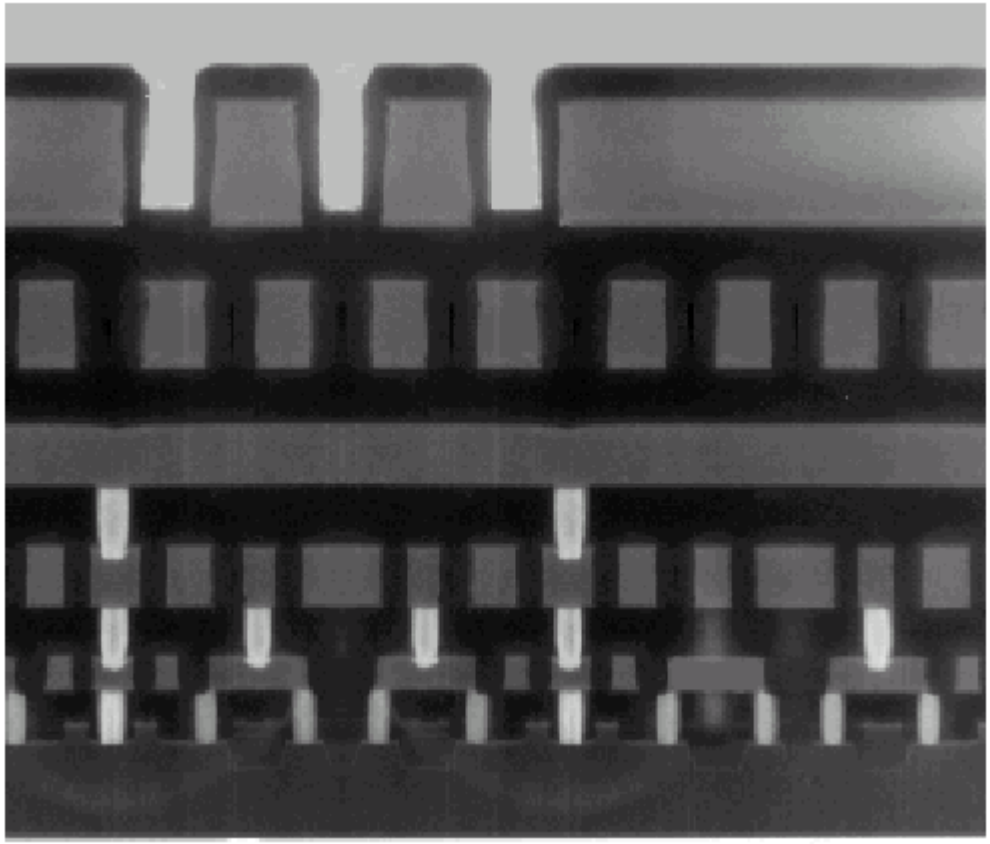
Modern Interconnect



Layer Stack

- **AMI 0.6 μm process: 3 metal layers**
  - *M1: within-cell routing*
  - *M2: vertical routing between cells*
  - *M3: horizontal routing between cells*
- **Modern processes:6-10+ metal layers**
  - *M1: thin, narrow (< 3λ)*
    (High density cells)
  - *Mid layers: thicker and wider*
    (density vs. speed)
  - *Top layers: thickest*
    (For V_{DD}, GND, clk)

Intel 0.25μm Process

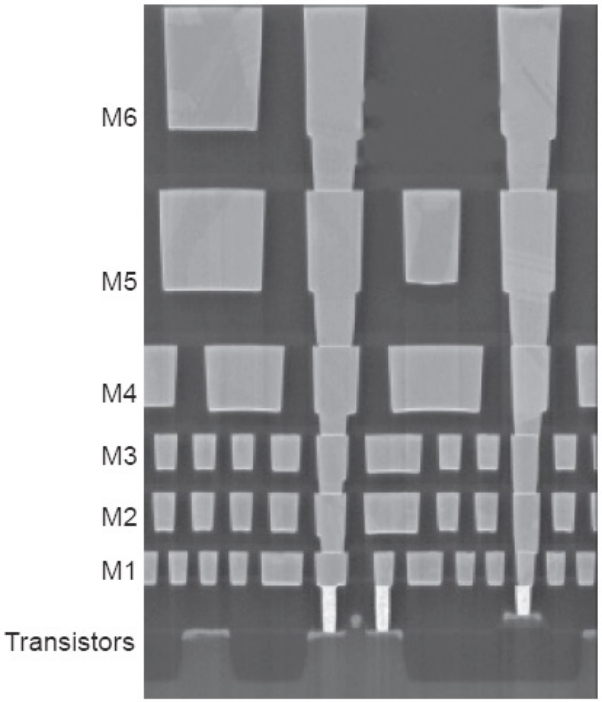


5 metal layers
Ti/Al - Cu/Ti/TiN
Polysilicon dielectric

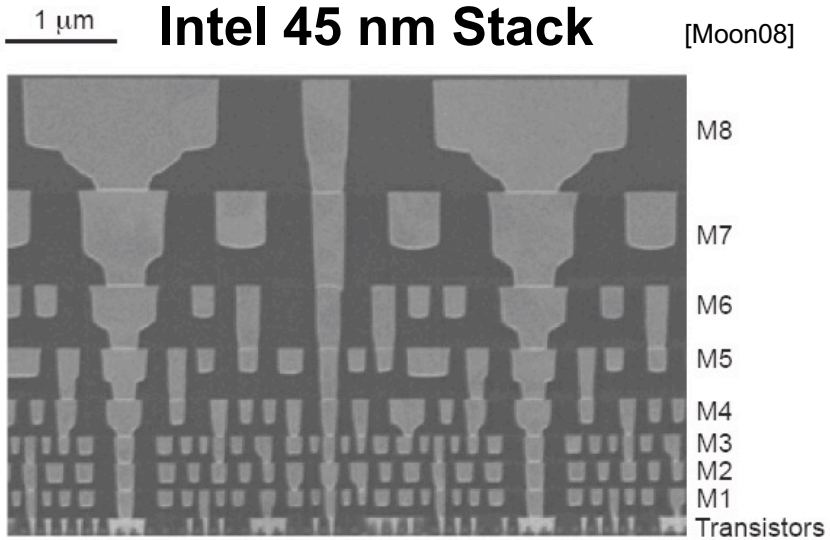
LAYER	PITCH	THICK	A.R.
Isolation	0.67	0.40	-
Polysilicon	0.64	0.25	-
Metal 1	0.64	0.48	1.5
Metal 2	0.93	0.90	1.9
Metal 3	0.93	0.90	1.9
Metal 4	1.60	1.33	1.7
Metal 5	2.56	1.90	1.5
	μm	μm	

Layer pitch, thickness and aspect ratio

More Examples



Intel 90 nm Stack [Thompson02]



Intel 45 nm Stack [Moon08]

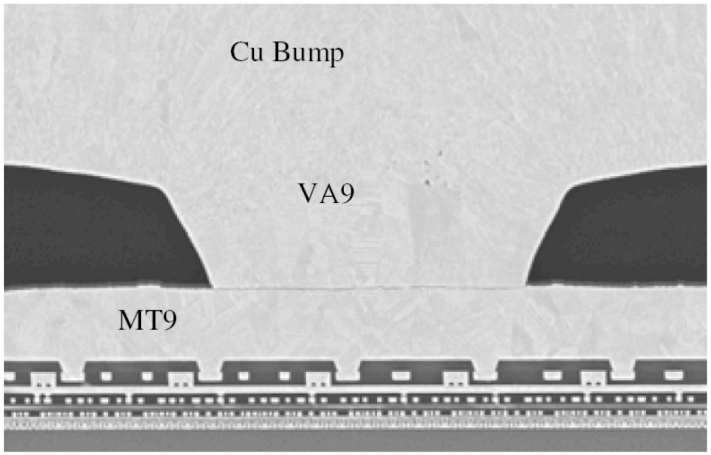


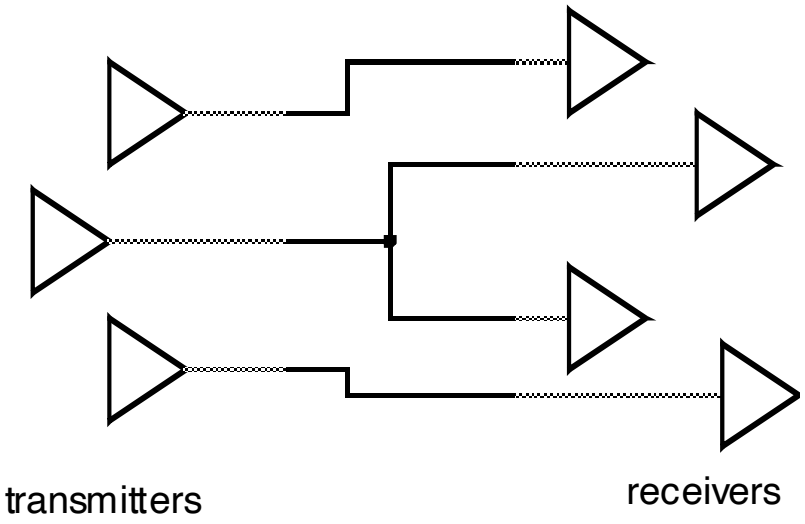
FIGURE 6.3 SEM image of complete cross-section of Intel's 45 nm process including M9 and I/O bump (From [Moon08] with permission of Intel Corporation.)

Wire Model

Parasitics: capacitance, resistance, inductance

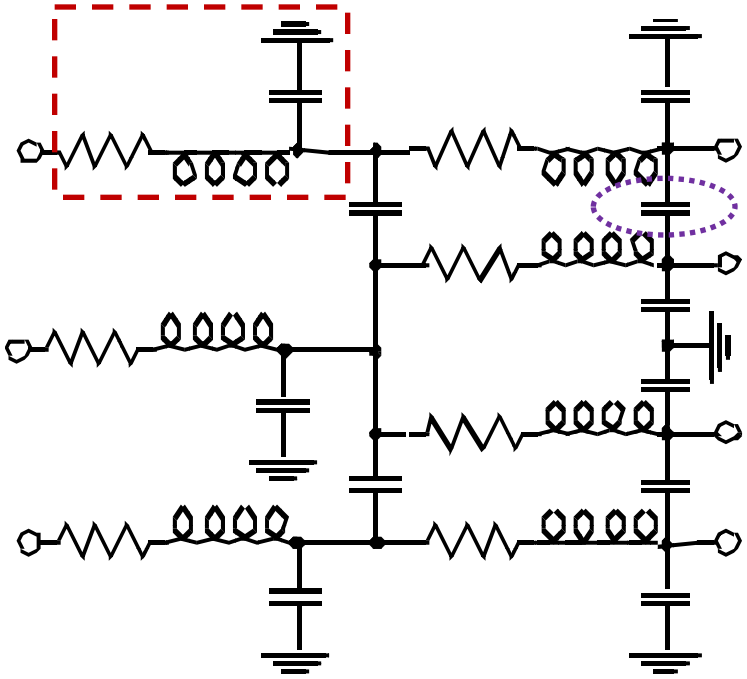
- increase in propagation delay, or drop in performance
- an impact on power consumption
- an introduction of extra noise sources -> reliability

Schematics

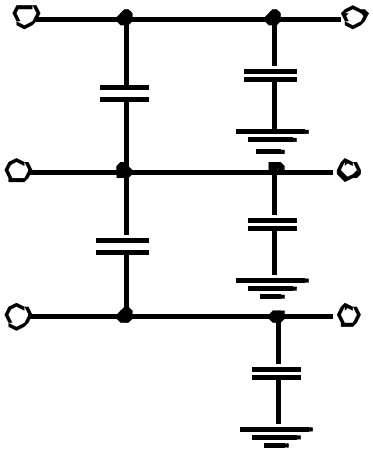


Physical

Wire: Models



All-inclusive model



Capacitance-only model

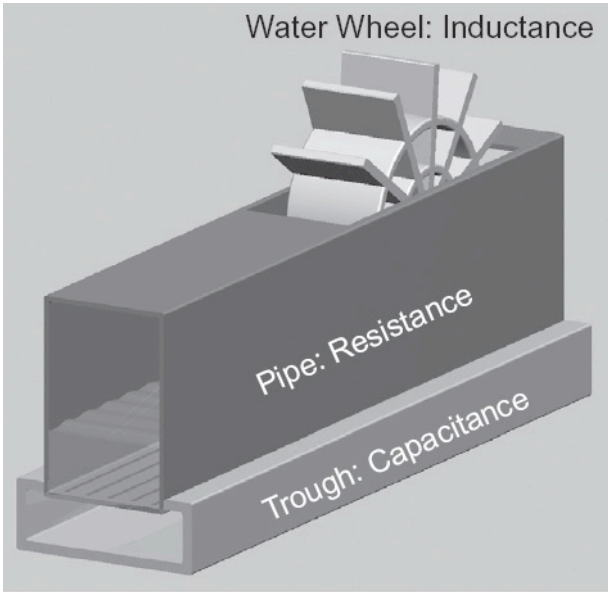
Wire: Parasitic Simplifications

- Inductive effects can be ignored
  - if the resistance of the wire is substantial enough (as is the case for long Al wires with small cross-section)
  - If the rise and fall times of the applied signals are **slow enough**
- Capacitance only model can be used
  - When the wire is short, or the cross-section is large,
  - The interconnect material has low resistivity,
- Interwire capacitance can be ignored, and all the parasitic capacitance can be modeled as capacitance to ground
  - when the separation between neighboring wires is large
  - when the wires run together for only a short distance

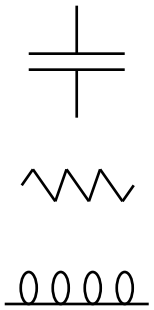
Interconnect Modeling

- Current in a wire is analogous to current in a pipe
  - -- **Resistance:** narrow size impedes flow
  - -- **Capacitance:** trough under the leaky pipe must fill first
  - -- **Inductance:** paddle wheel inertia opposes changes in flow rate

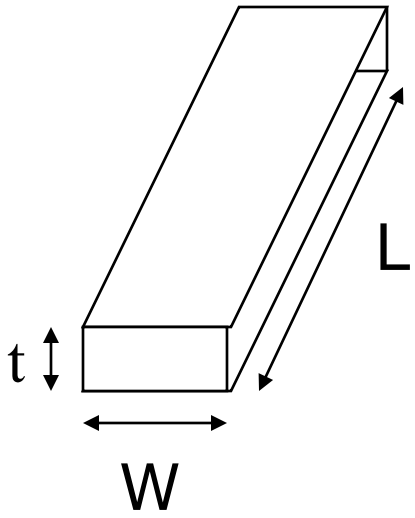
  (Negligible for most wires)



- Classes of parasitics
  - **-- Capacitive**
  - **-- Resistive**
  - **-- Inductive**



Wire Resistance



$$R = \frac{\rho L}{A} = \frac{\rho}{t}\frac{L}{W} = R_{\square}\frac{L}{W}$$

方块电阻

$R_{\square}$: Sheet Resistance

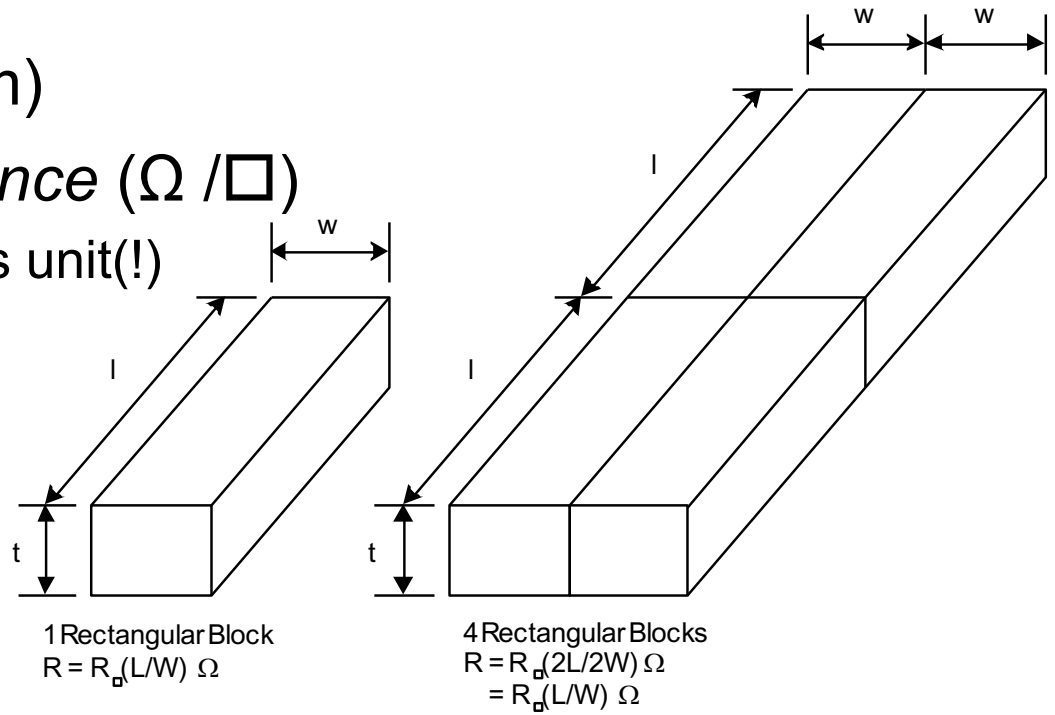
Material	ρ(Ω-m)
Silver (Ag)	1.6 x 10^{-8}
Copper (Cu)	*1.7 x 10^{-8}*
Gold (Au)	2.2 x 10^{-8}
Aluminum (Al)	*2.7 x 10^{-8}*
Tungsten (W)	5.5 x 10^{-8}

Material	$R_{\square}$ (Ω/□)
n, p well diffusion	1000 to 1500
n+, p+ diffusion	50 to 150
n+, p+ diffusion with silicide	3 to 5
polysilicon	150 to 200
polysilicon with silicide	4 to 5
Aluminum	0.05 to 0.1

Wire Resistance: ρ vs. $R_{\square}$

- ρ: *resistivity* (Ω*m)
- $R_{\square}$: *sheet resistance* (Ω /□)
  - □ is a dimensionless unit(!)

$$R = \frac{\rho L}{A} = R_{\square}\frac{L}{W}$$



Example

The Al wire is 10cm long and 1μm wide and is routed on the first Al layer:

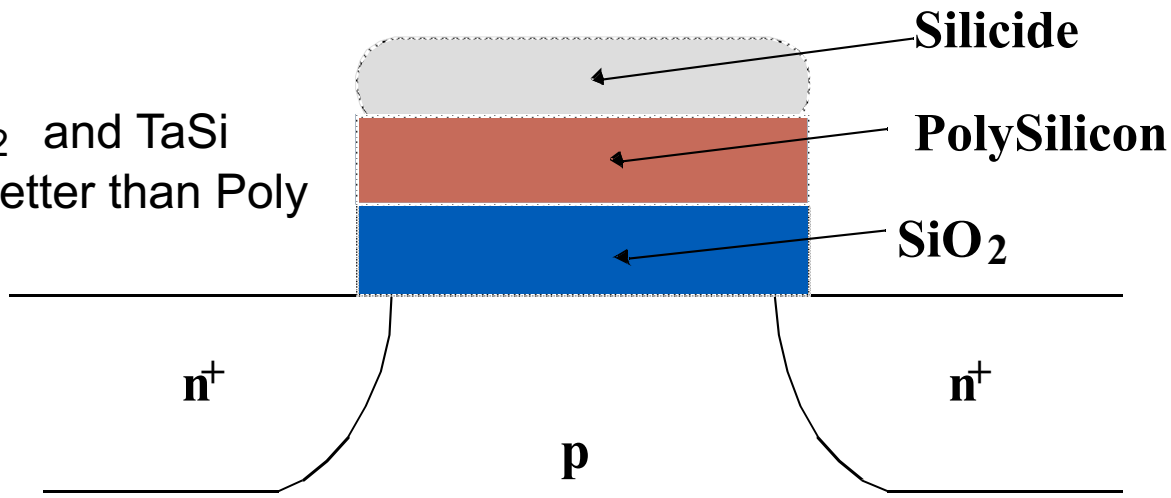
$$R_{wire} = 0.075\Omega/\square \times \left(0.1\times 10^{6}\,\mu m\right)/1\mu m = 7.5k\Omega$$

Poly(175Ω/□) ： 17.5MΩ； Silicided Polysilicon(4Ω/□) ： 400kΩ

Dealing with Resistance

- Use better interconnect materials
  - reduce average wire-length
  - e.g. copper, silicides
- More interconnect layers
  - reduce average wire-length

Silicides: WSi_2, $TiSi_2$, $PtSi_2$ and TaSi
Conductivity: 8-10 times better than Poly



Choice of Metals

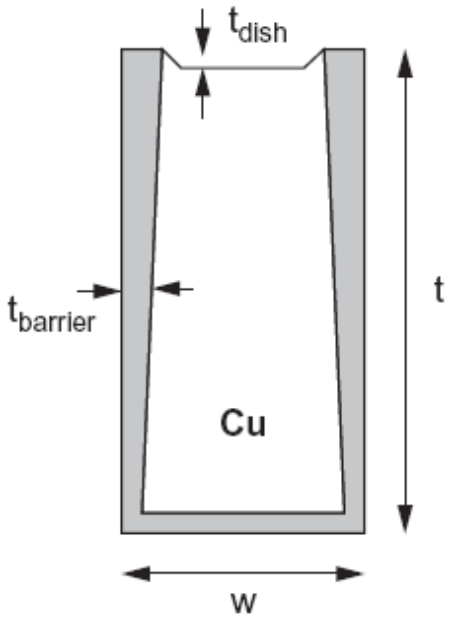
- Until 180 nm generation, most wires were aluminum
- Contemporary processes normally use copper
  - Cu atoms diffuse into silicon and damage FETs
  - Must be surrounded by a diffusion barrier

Metal	Bulk resistivity ($\mu\Omega \cdot cm$)
Silver (Ag)	1.6
Copper (Cu)	**1.7**
Gold (Au)	2.2
Aluminum (Al)	2.8
Tungsten (W)	5.3
Titanium (Ti)	43.0

Appendix：Copper Issues

- Copper wires diffusion barrier has high resistance
- Copper is also prone to *dishing* during polishing
- Effective resistance is higher

$$R = \frac{\rho}{(t - t_{\text{dish}} - t_{\text{barrier}})} \frac{l}{(w - 2t_{\text{barrier}})}$$



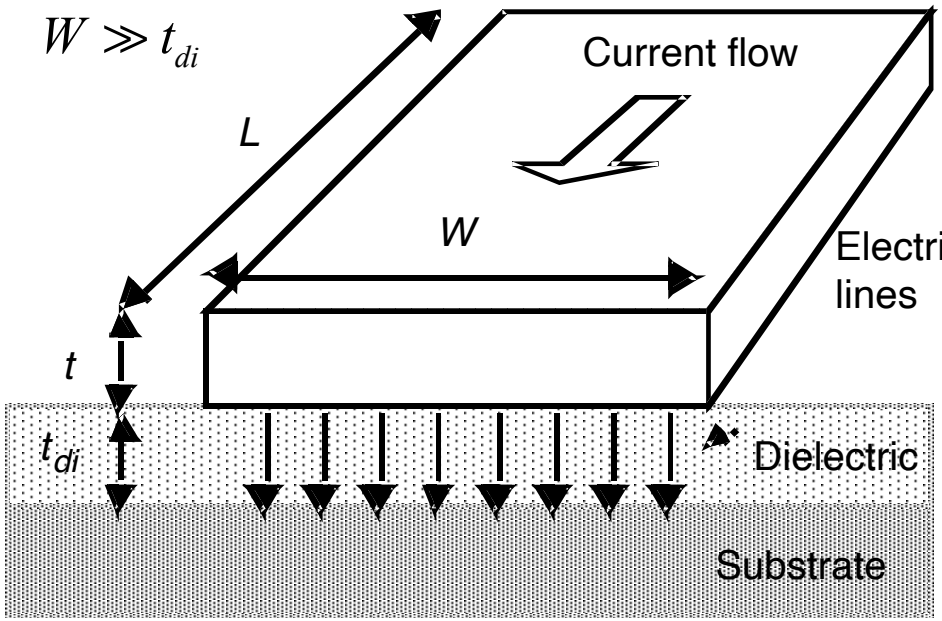
Contacts Resistance

- Contacts Resistance: transitions between routing layers add extra resistance to a wire
  - Contacts: **5-20Ω** vias: **1-5 Ω**
  - **Preferred routing strategy: keep signal wire on a single layer**
- Use many contacts for lower R
  - Many small contacts for current crowding around periphery

Outline

- Review: Quantity Metrics of Digital Design
- Wire: A First Glance
- Interconnect Parameters: R, C, L
  - Resistance
  - Capacitor
  - Inductance
- Electrical Wire Models
- Perspective

Capacitance: Parallel-Plate Model



$$c_{int} = \frac{\varepsilon_{di}}{t_{di}} WL$$

Permittivity Constant

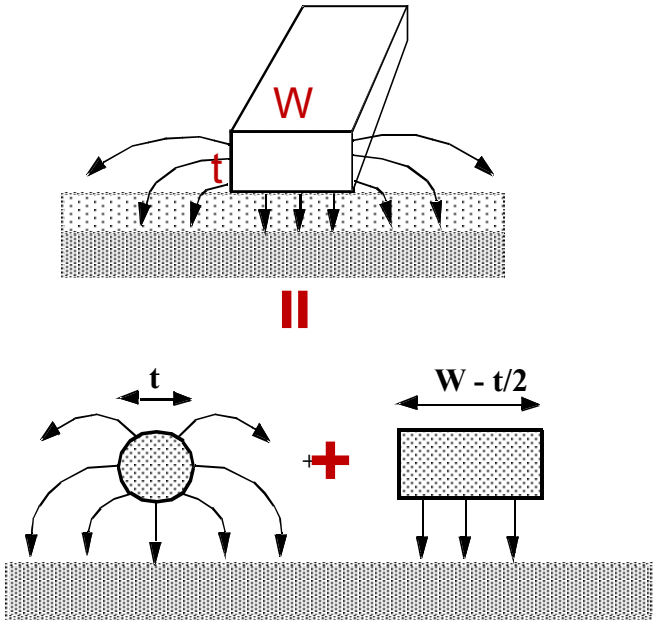
Material	ε_r
Free space	1
Aerogels	~1.5
Polyimides (organic)	3-4
Silicon dioxide	3.9
Glass-epoxy (PC board)	5
Silicon Nitride (Si_3N_4)	7.5
Alumina (package)	9.5
Silicon	11.7

$$\varepsilon_0 = 8.854 \times 10^{-12}\ F/m$$

Capacitance Trends

- Parallel-plate equation: $C = \varepsilon_{ox} A / t_{di}$
  - Wires are not parallel plates, but obey trends
  - Increasing area (W, L) increases capacitance
  - Increasing distance (t_{di}) decreases capacitance
- Dielectric constant
  - $\varepsilon_{ox} = k\varepsilon_0$
    - ε_0 = 8.85 x 10^{-14} F/cm
    - k = 3.9 for SiO_2 (ideal oxide, 4.1 with phosphorous)
- Processes are starting to use low-k dielectrics
  - k ≈ 3 (or less) as dielectrics use air pockets

Fringing Capacitance边缘电容



$$c_{wire} = c_{pp} + c_{fringe} = \frac{w\varepsilon_{di}}{t_{di}} + \frac{2\pi\varepsilon_{di}}{\log(\frac{2t_{di}}{t} + 1)}$$

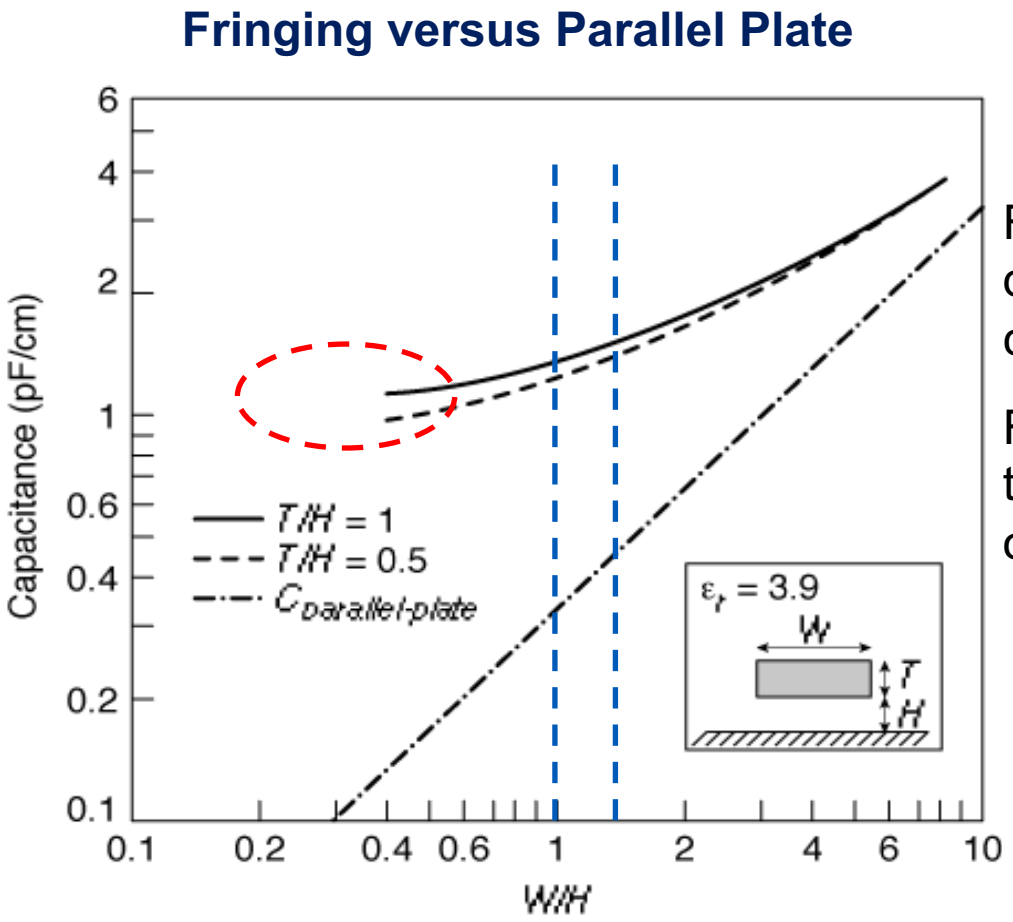
w=W-t/2

- Capacitance of a line without neighbors is approximated as

$$C_{tot} = \varepsilon_{ox} l \left[\frac{w}{h} + 0.77 + 1.06 \left(\frac{w}{h} \right)^{0.25} + 1.06 \left(\frac{t}{h} \right)^{0.5} \right]$$

--the empirical formula is accurate to 6% for AR < 3.3

Capacitance: Fringing vs. Parallel Plate

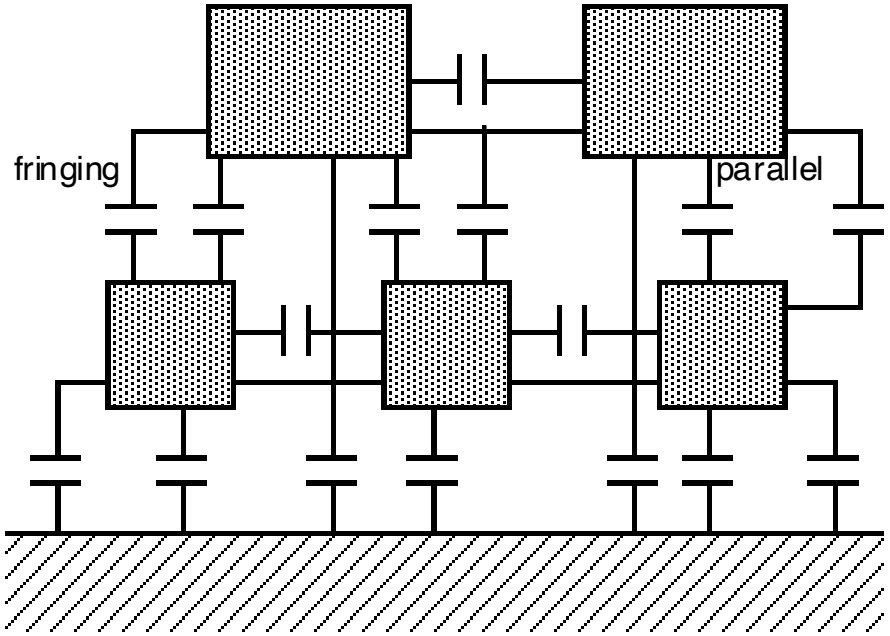


For W/H<1.5, the fringe component dominates the parallel-plate component.

Fringing capacitance can increase the overall capacitance by a factor of 10 or more.

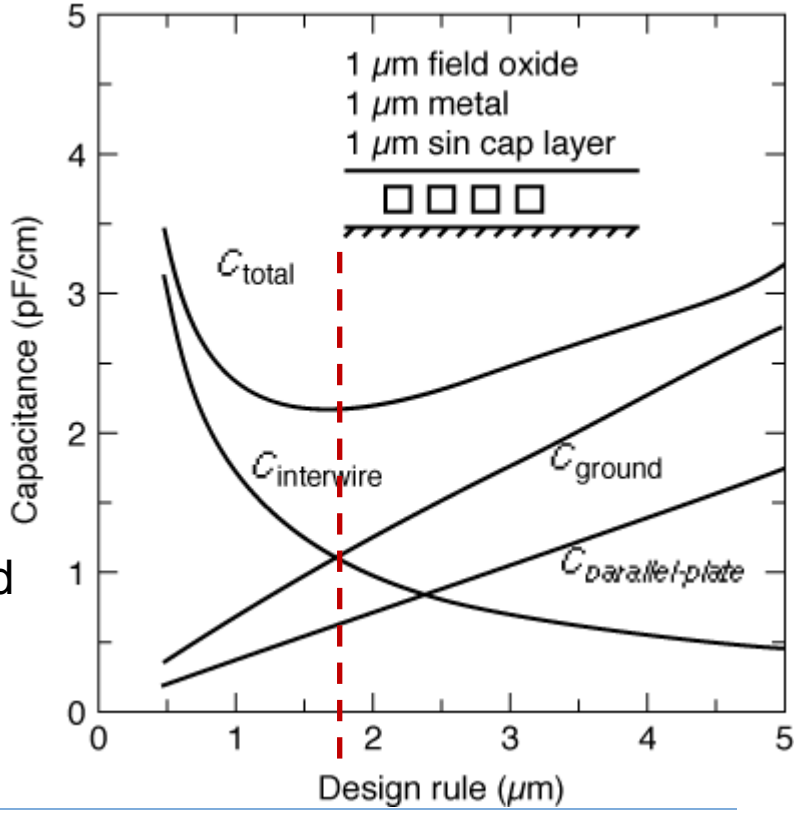
Note that the cap level levels off to a constant value of approx: 1pf/cm

Interwire Capacitance



$C_{wire} = C_{pp} + C_{fringe} + C_{interwire}$

- When W < 1.75H, interwire capacitance: dominate
- Interwire capacitance is more pronounced for wires in the higher interconnect layers (further from the substrate)



Interwire Capacitances: 0.25μm CMOS

	Field	Active	Poly	Al1	Al2	Al3	Al4
Poly	88				*pp: in aF/μm^2*		
	54				*fringe: in aF/μm*		
Al1	30	41	57				
	40	47	54				
Al2	13	15	17	36			
	25	27	29	45			
Al3	8.9	9.4	10	15	41		
	18	19	20	27	49		
Al4	6.5	6.8	7	8.9	15	35	
	14	15	15	18	27	45	
Al5	5.2	5.4	5.4	6.6	9.1	14	38
	12	12	12	14	19	27	52

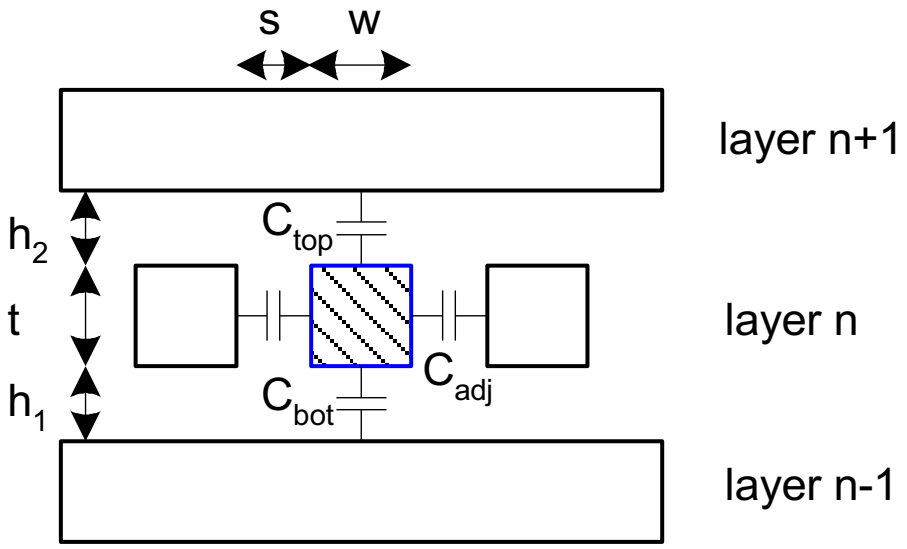
同一层	Poly	Al1	Al2	Al3	Al4	Al5
Interwire Cap	40	95	85	85	85	115

aF/μm

单位长度的线间电容

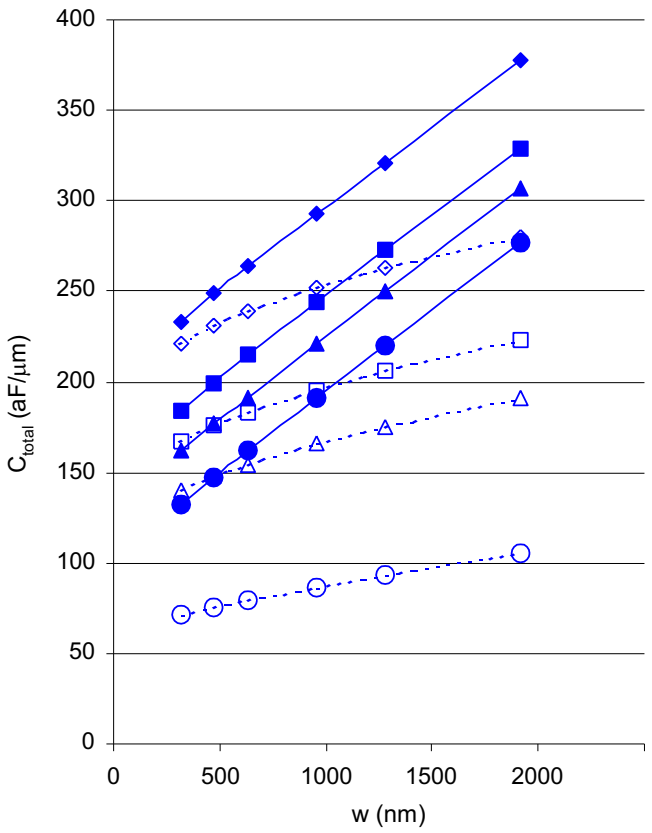
Multilayer Wire Capacitance

- Wire has capacitance per unit length
  - To neighbors
  - To layers above and below
- $C_{total} = C_{top} + C_{bot} + 2C_{adj}$



Example: M2 Capacitance Data

- Typical dense wires have ~ 0.2 fF/mm
  - Compare to 1-2 fF/mm for gate capacitance



A metal2 wire in a 180 nm process with wire and oxide thicknesses of 0.7mm.

- For an isolated wire above the substrate, the capacitance is strongly influenced by spacing between conductors
- For a wire sandwiched between metal1 and metal3 planes, the capacitance is higher and is more sensitive to the width but less sensitive to spacing

Diffusion & Polysilicon

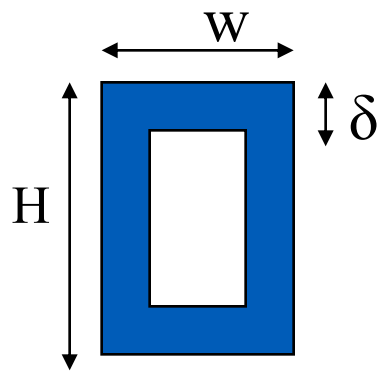
- Rules of thumb
  - Use poly only for short runs
  - Shorter wires – lower R and C
  - Thinner wires – lower C but higher R

Insights

- Diffusion capacitance is very high (1-2 fF/mm)
  - Comparable to gate capacitance
  - Diffusion also has high resistance
  - Avoid using diffusion *runners* for wires!
- Polysilicon has lower C but high R
  - Use for transistor gates
  - Occasionally for very short wires between gates

Skin Effect(趋肤效应)

At high frequency, currents tend to flow primarily on the surface of a conductor with the current density falling off exponentially with depth into the wire



Skin depth:

$$\delta = \sqrt{\frac{\rho}{\pi f \mu}}$$

permeability: $\mu = 4\pi \times 10^{-7}$ H/m

δ= 2.6 μm for Al at 1 GHz

⇨ the overall cross section is ~ $2(w+t)\delta$

$$r(f) = \frac{\sqrt{\pi f \mu \rho}}{\pi \mu \left(\max(W,H)\right)^2}$$

- The onset of skin effect is at f_s - where the skin depth is equal to half the largest dimension of the wire

$$f_s = \frac{4\rho}{\pi\mu(\max(W,H))^2}$$

An issue for **wide (tall) wires** in high frequency: **i.e., clocks!**

Inductance

- On-chip inductance: ringing and overshoot effects, reflections of signal due to impendence mismatch, inductive coupling between lines, and switching noise due to *L*d*i*/d*t* voltage

$$\Delta V = L\frac{di}{dt}$$

- The capacitor c and the inductance l (per unit length) of a wire:

$$cl = \varepsilon\mu \qquad v = \frac{1}{\sqrt{cl}} = \frac{1}{\sqrt{\varepsilon\mu}} = \frac{c_0}{\sqrt{\varepsilon_r \mu_r}}$$

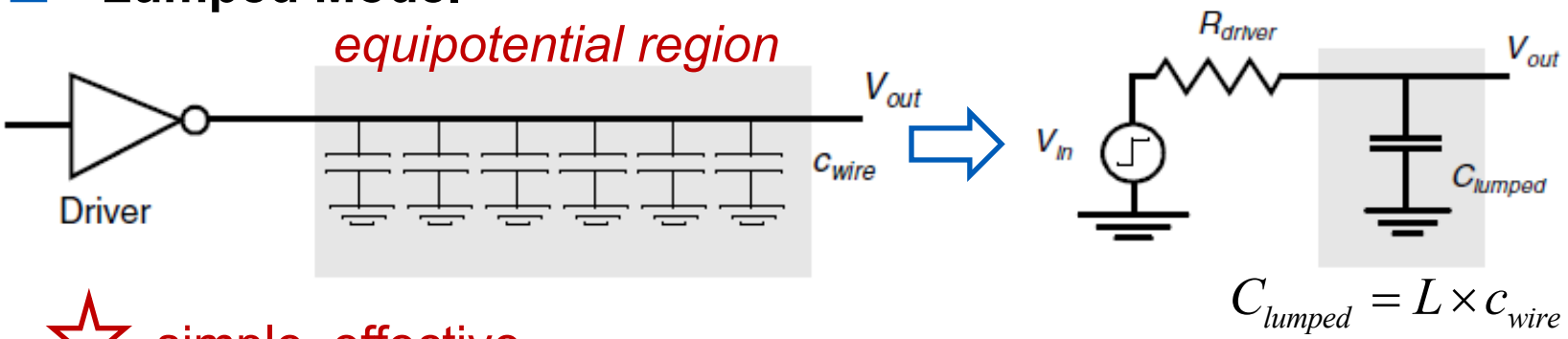
Dielectric	ε_r	Propagation speed (cm/nsec)
Vacuum	1	30
SiO_2	3.9	15
PC board (epoxy glass)	5.0	13
Alumina (ceramic package)	9.5	10

Wire Delay Model: Ideal Wire

- Ideal wire simplistic
  - The same voltage is present at every segment of the wire at every point in time: *equipotential region*
  - early phases of the design process
  - only holds for *very short* wires, i.e., interconnects between *very* nearest neighbor gates

Lumped Model

Lumped Model



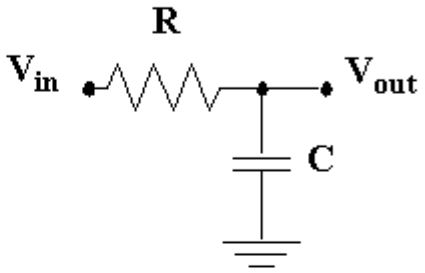
$$C_{lumped} = L \times c_{wire}$$

simple, effective

an ordinary differential equation

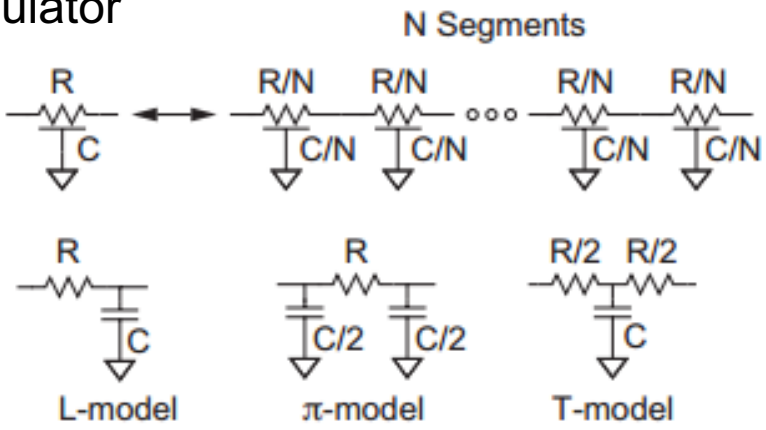
Lumped RC model

- total wire resistance is lumped into a single R and total capacitance into a single C
- good for short wires
- pessimistic and inaccurate for long wires



Distributed RC Model

- A wire is a distributed circuit with a resistance and capacitance per unit length. Its behavior can be approximated with a number of lumped elements.
- Three standard approximations:
  - **L-model**: a large number of segments are required for accurate results => poor choice
  - **π-model**: three segments are sufficient to give results accurate to 3% [Sakurai83].
  - **T-model**: produces a circuit with one more node that is slower to solve by hand or with a circuit simulator

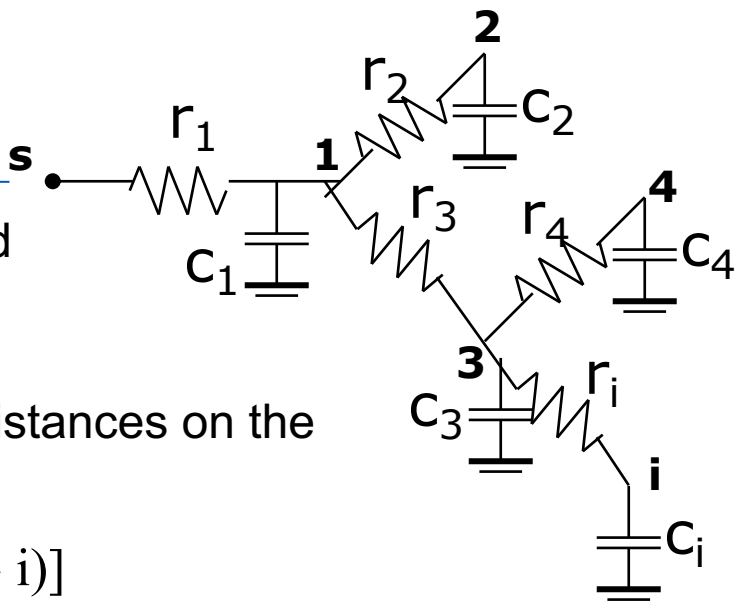


- Common practice to model long wires for simulation:

  3–5 segment π-model

-- RC Tree Definitions

- A unique resistive path exists between the source node and any node of the network
  - Single input (source) node： s
  - All capacitors are between a node and GND
  - No resistive loops



- **Path resistance** 路径电阻 (sum of the resistances on the path from the input node ***s*** to node ***i***)

$$R_{ii} = \sum_{j=1}^{i} r_j \Rightarrow (r_j \in [\text{path}(s \rightarrow i)]$$

- **Shared path resistance**共享路径电阻 (resistance shared along the paths from the input node ***s*** to nodes ***i*** and ***k***)

$$R_{ik} = \sum_{j=1}^{N} r_j \Rightarrow (r_j \in [\text{path}(s \rightarrow i) \cap \text{path}(s \rightarrow k)])$$

- **Elmore Delay**

$$\tau_{Di} = \sum_{k=1}^{N} C_k R_{ik} \Rightarrow \tau_{Di} = R_1C_1 + R_1C_2 + (R_1 + R_3)C_3 + (R_1 + R_3)C_4 + (R_1 + R_3 + R_i)C_i$$

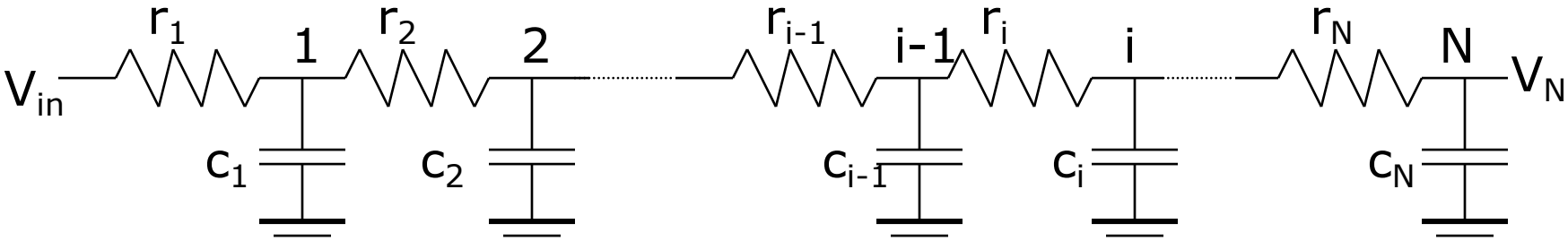
-- Chain Network Elmore Delay

- **Elmore delay equation**

$$\tau_{Di} = \sum_{k=1}^{N} C_k R_{ik} \Rightarrow \tau_{DN} = \sum_{i=1}^{N} C_i \sum_{j=1}^{N} R_j = \sum_{i=1}^{N} C_i R_{ii}$$

$\tau_{D1}=c_1r_1$

$\tau_{D2}=c_1r_1 + c_2(r_1+r_2)$



$\tau_{Di}=c_1r_1+ c_2(r_1+r_2)+\ldots+c_i(r_1+r_2+\ldots+r_i)$

$\tau_{Di}=c_1r_{eq}+ 2c_2r_{eq}+ 3c_3r_{eq}+\ldots+ ic_ir_{eq}$

-- Distributed RC Model for Simple Wires

- A length *L* wire can be modeled by *N* segments of length *L*/*N*
  - The resistance and capacitance of each segment are given by *r L*/*N* and *c L*/*N*

$$\tau_{DN} = (\frac{L}{N})^2 (rc + 2rc + ... + Nrc) = (rcL^2) \frac{N(N+1)}{2N^2} = RC \frac{N+1}{2N}$$

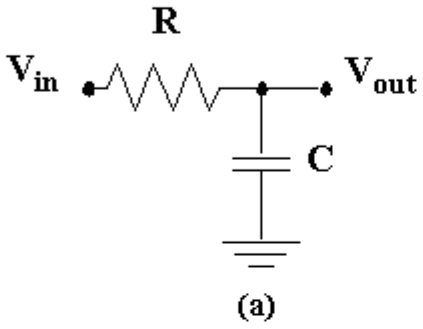
$$N \to \infty \qquad \tau_{DN} = \frac{RC}{2} = \frac{rcL^2}{2}$$

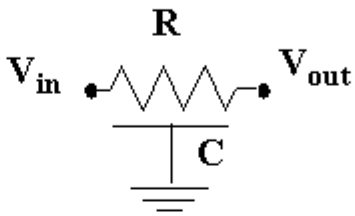
  - For large N

-- Delay of a wire is a quadratic function of its length, *L*

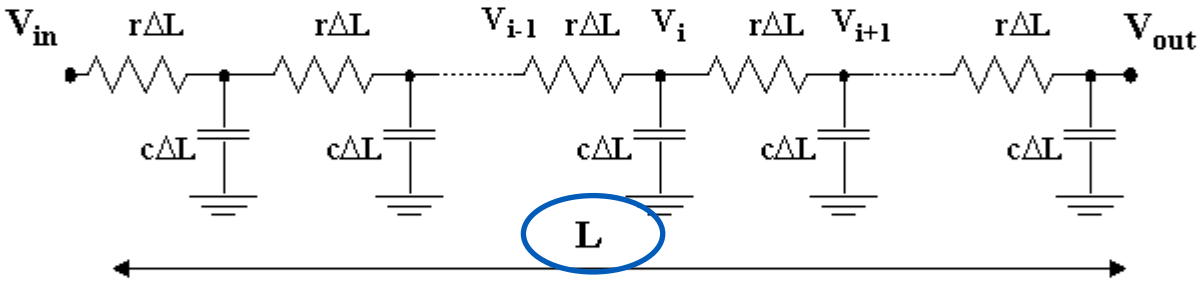
-- The delay is 1/2 of that predicted by the lumped model

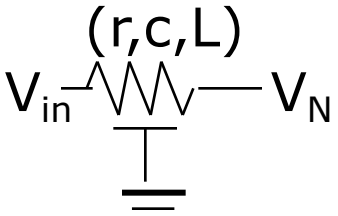
Distributed *rc* line





--SPICE Model



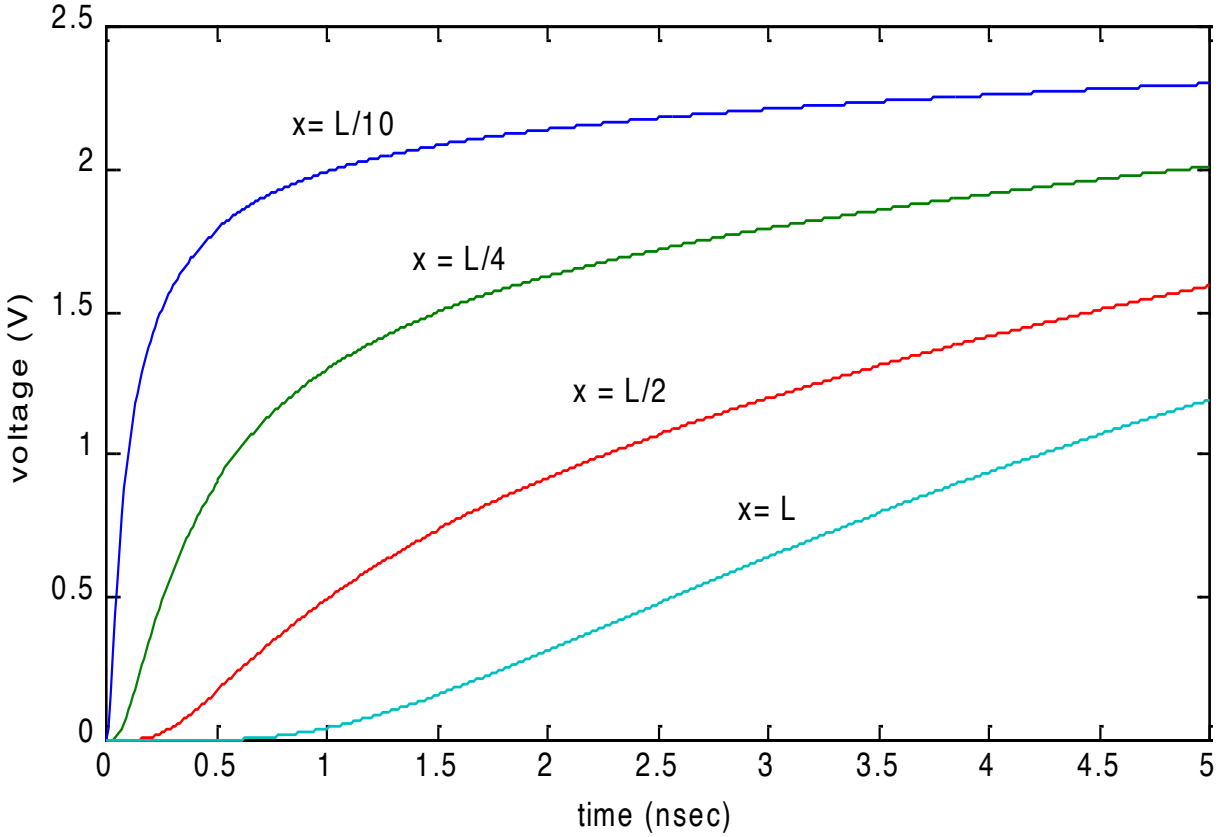


Partial differential equation: $c\Delta L\frac{\partial V_i}{\partial t} = \frac{(V_{i+1}-V_i)+(V_{i-1}-V_i)}{r\Delta L}$

$\Delta L \to 0$

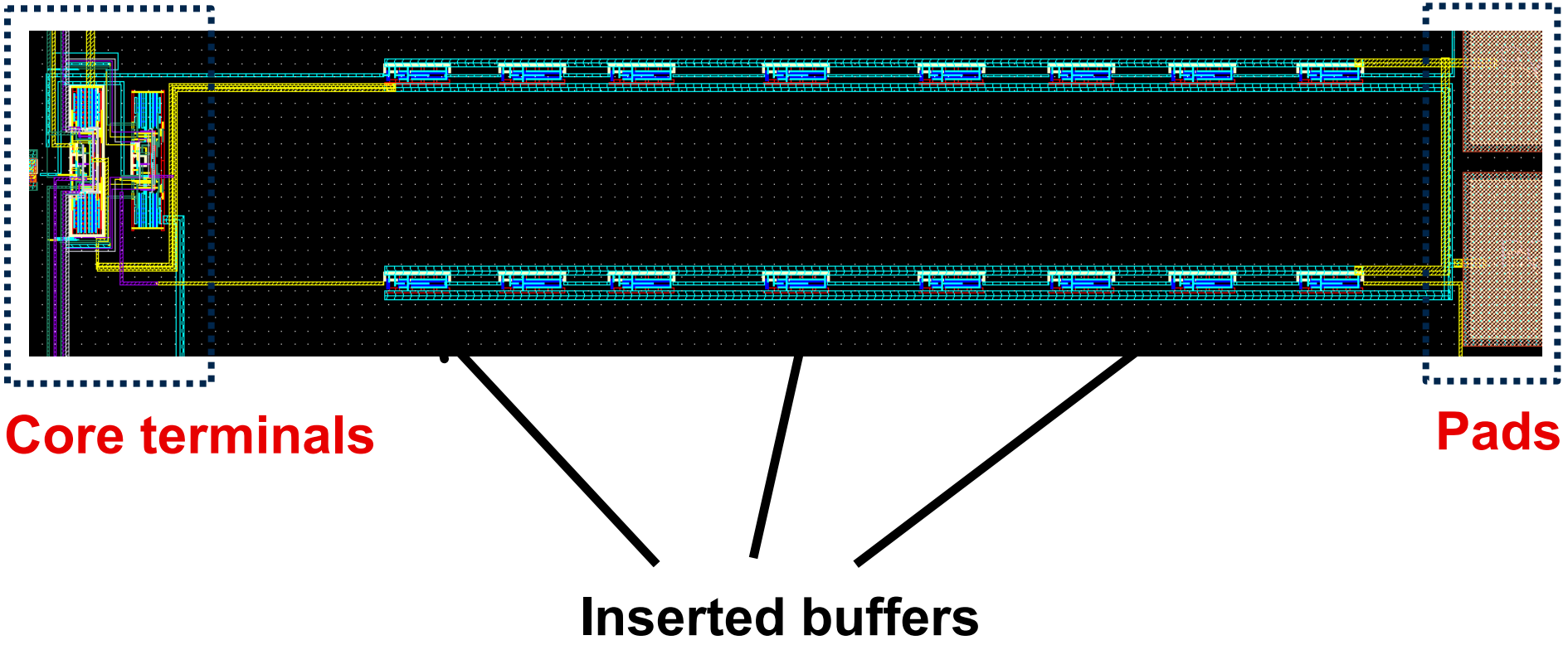
Diffusion equation: $rc\frac{\partial V}{\partial t} = \frac{\partial^2 v}{\partial x^2}$ $\qquad \tau(V_{out}) = \frac{rcL^2}{2}$

Step-response of *rc* line



Driving these *rc* lines and minimizing the delay and signal degradation is one of the trickiest problems in IC design.

Layout example of buffers insertion



Step Response Points

Voltage Range	Lumped RC	Distributed RC
$0 \rightarrow 50\%$ (t_p)	0.69 RC	0.38 RC
$0 \rightarrow 63\%$ (τ)	RC	0.5 RC
$10\% \rightarrow 90\%$ (t_r)	2.2 RC	0.9 RC

Time to reach the 50% point: $t = \ln(2)\tau = 0.69\tau$

Time 10%- 90% point: $t = \ln(9)\tau = 2.2\tau$

- **Example** Consider a Al1 wire: 10 cm long and 1 μm wide
  - Using a lumped C only model with a source resistance (R_{Driver}) of 10 kΩ and a total lumped capacitance (C_{lumped}) of 11 pF

    $t_{50\%}$ = 0.69 x 10 kΩ x 11pF = 76 ns

    $t_{90\%}$ = 2.2 x 10 kΩ x 11pF = 242 ns
  - Using a distributed RC model with c = 110 aF/μm and r = 0.075 Ω/μm

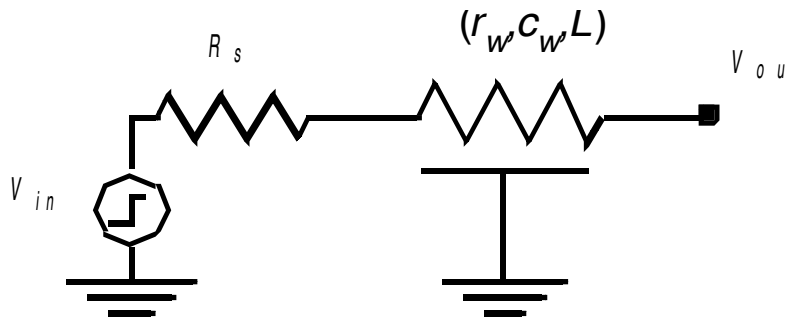
    $t_{50\%}$ = 0.38 x (0.075 Ω/μm) x (110 aF/μm) x $(10^5$ μm$)^2$ = 31.4 ns

    $t_{90\%}$ = 0.9 x (0.075 Ω/μm) x (110 aF/μm) x $(10^5$ μm$)^2$ = 74.25 ns

    Poly: $t_{50\%}$ = 0.38 x (150 Ω/μm) x (88+2×54 aF/μm) x $(10^5$ μm$)^2$ = 112 μs

    Al5: $t_{50\%}$ = 0.38 x (0.0375 Ω/μm) x (5.2+2×12 aF/μm) x $(10^5$ μm$)^2$ = 4.2 ns

Driving an *rc* line



$$\tau_D = R_s C_w + \frac{R_w C_w}{2} = R_s C_w + 0.5 r_w c_w L^2$$

$$t_p = 0.69 R_s C_w + 0.38 R_w C_w$$

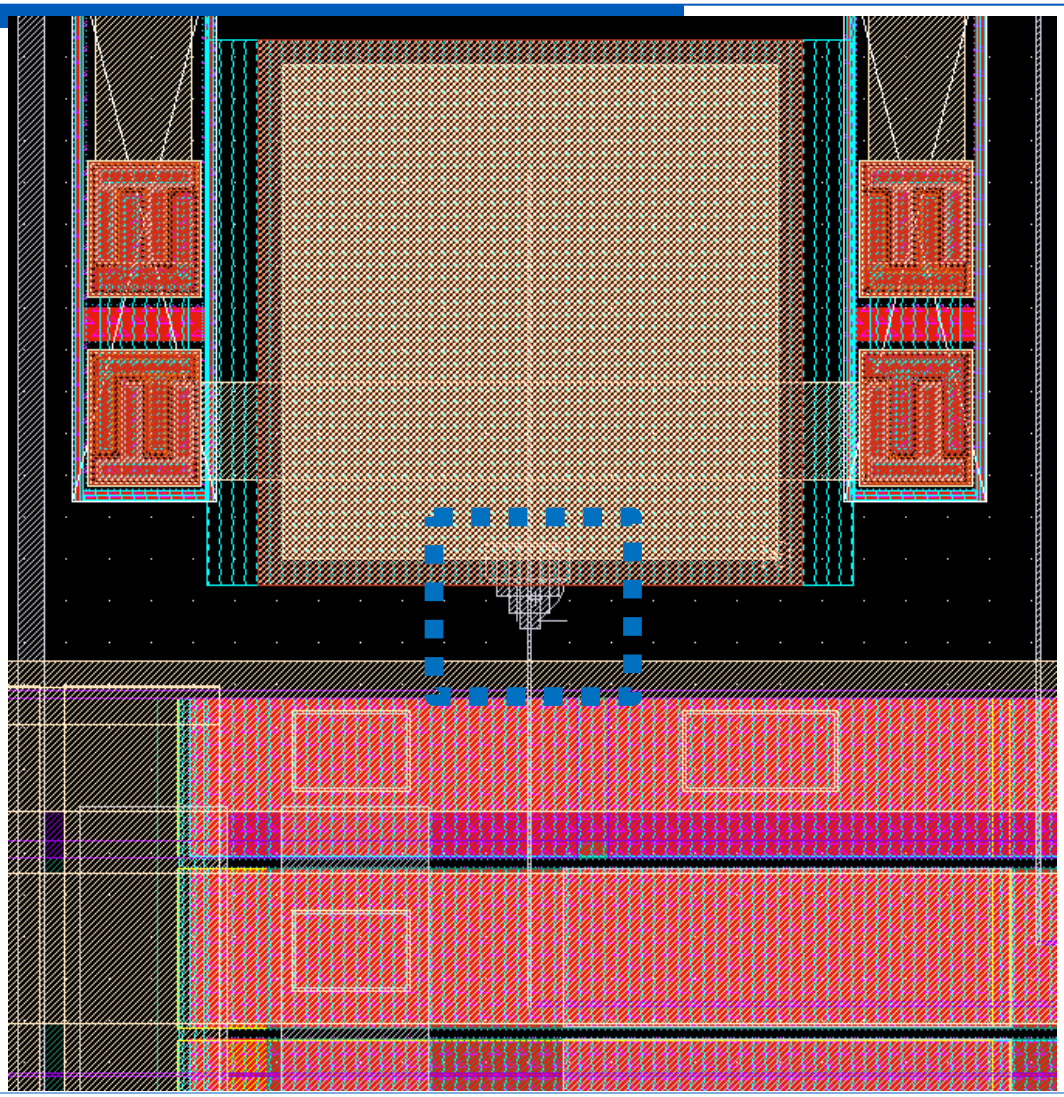
The delay introduced by the wire resistance becomes dominant when $R_w C_w/2 \geq R_s C_w$, or $L \geq 2Rs/r$

Wire Sizing

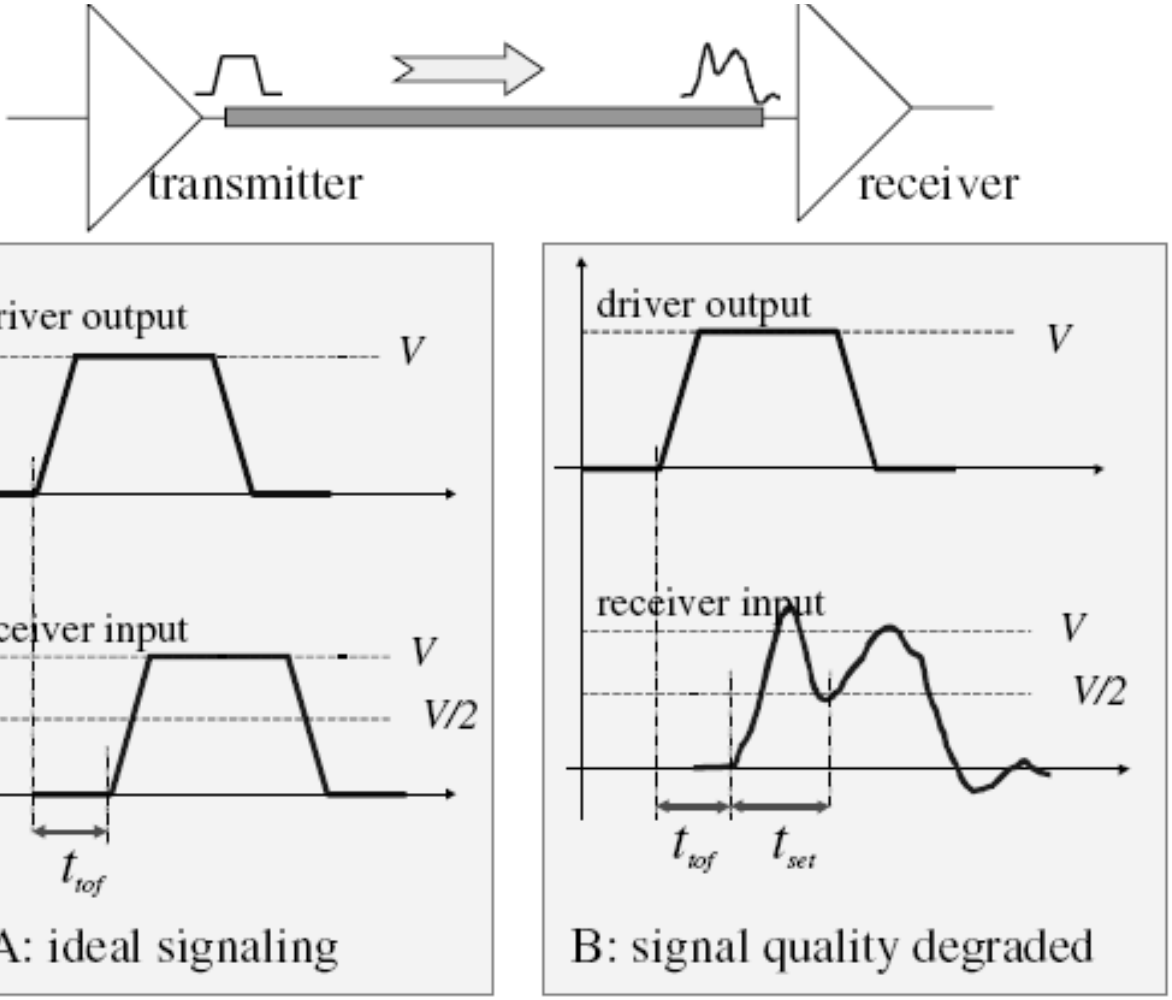
- Wire **length** is determined by layout architecture, but we can choose wire **width** to minimize delay.
- Wire width can vary with distance from driver to adjust the resistance which drives downstream capacitance.
- Wire with minimum delay has an **exponential taper**.
- Optimal tapering improves delay by about 8%.

Approximate tapering with a few rectangular segments

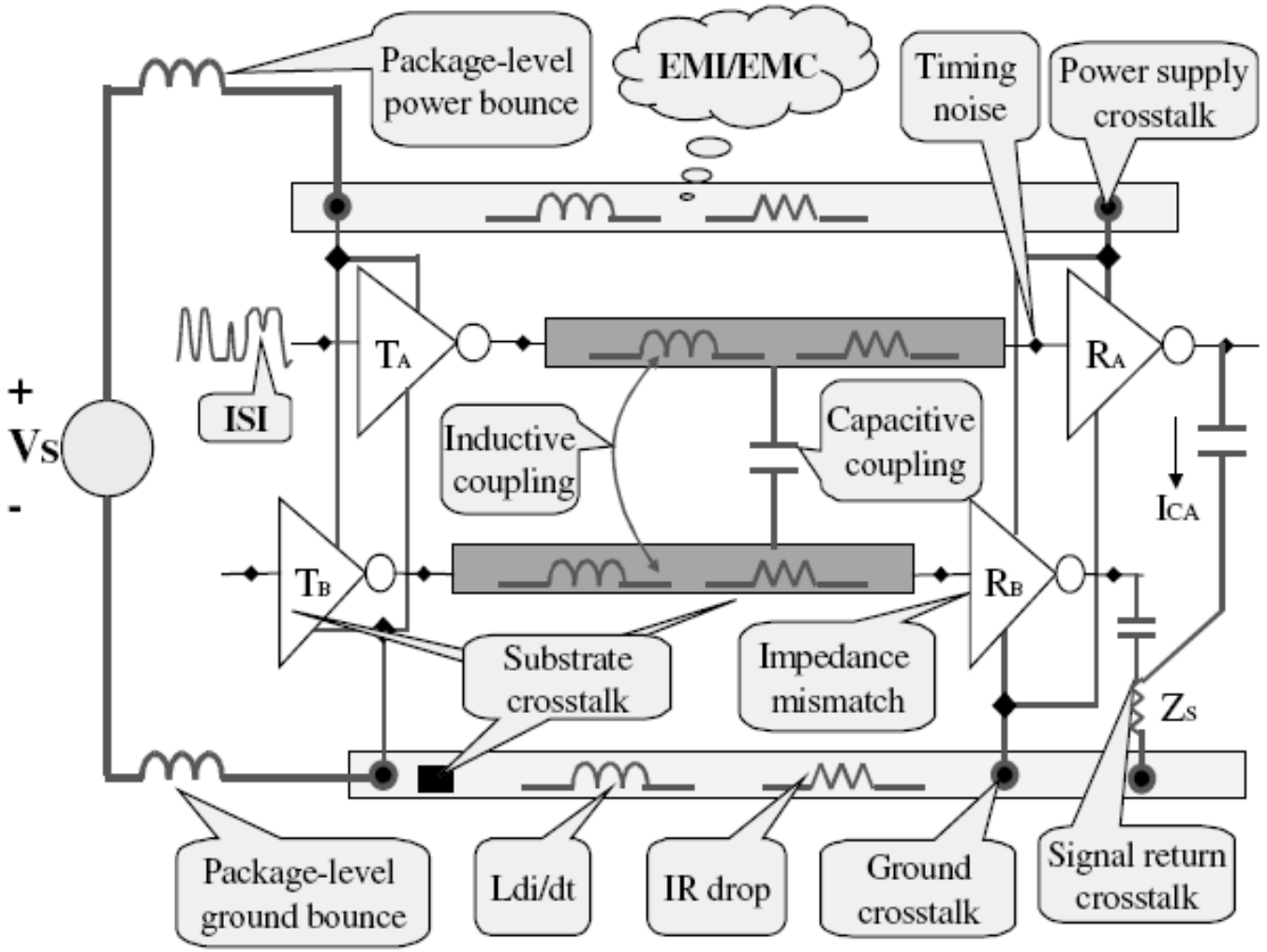
Example of Approximate tapering



Signal Integrity(信号完整性)

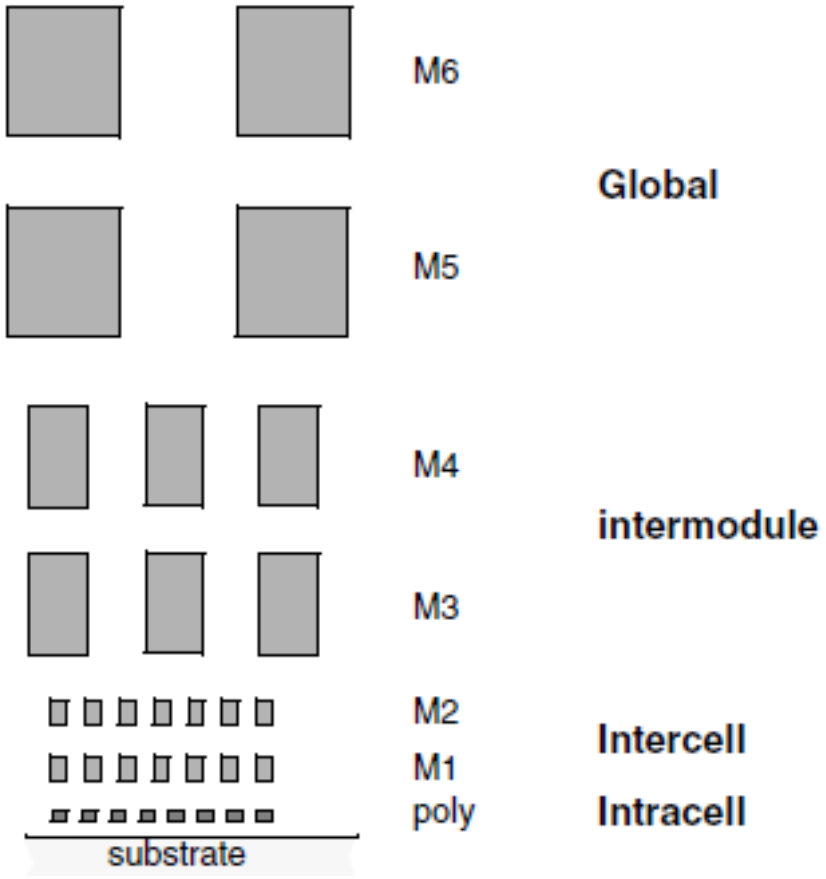


Noise


Package-level power bounce
EMI/EMC
Timing noise
Power supply crosstalk
ISI
TA
RA
Inductive coupling
Capacitive coupling
ICA
+
Vs
-
TB
RB
Substrate crosstalk
Impedance mismatch
ZS
Package-level ground bounce
Ldi/dt
IR drop
Ground crosstalk
Signal return crosstalk

Perspective

- Better interconnect (Cu) and insulation material (polymers and air)
- Differentiate between wires
  - Local: density, low-cap
  - Global: low-resistance



集成电路原理与设计

11. 导线

Wire

谭志超

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