集成电路原理与设计
10.运算放大器

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Assignment 2

2-1 The circuit shown in Fig.2.1 illustrates a single-channel MOS resistor with a W/L of 2μm/2μm. Using Table.2.1 model parameters calculate the small-signal on-resistance of the MOS transistor at various values for VS and fill in the table below. (Note that the transistor **was in linear region**, VB=0, I_{DS}=0)

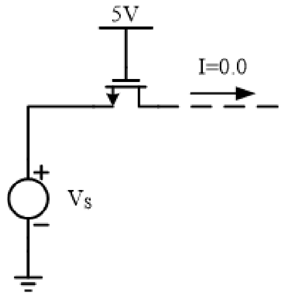


Fig.2.1

Vs(V)	R(Ω)
0.0	
1.0	
2.0	
3.0	
4.0	
5.0	

Answer

The equation for threshold voltage is represented with absolute values so that it can be applied to n-channel or p-channel transistors without confusion.

$$|V_T| = |V_{T0}| + \gamma[\sqrt{2|\Phi_F| + |V_{SB}|} - \sqrt{2|\Phi_F|}]$$

$$r_{on} = \frac{1}{\partial I_D/\partial V_{DS}} = \frac{L}{KW(|V_{GS}| - |V_T| - |V_{DS}|)}$$

For n-channel device

$V_{T0} = 0.7$ $\gamma = 0.45$ $2|\Phi_F| = 0.9$ $K = 134$

(1) When $V_S = 0, V_{GS} = 5$ and $V_{SB} = 0$

$$|V_T| = |V_{T0}| + \gamma[\sqrt{2|\Phi_F| + |V_{SB}|} - \sqrt{2|\Phi_F|}] = 0.7$$

$$r_{on} = \frac{1}{\partial I_D/\partial V_{DS}} = \frac{L}{KW(|V_{GS}| - |V_T| - |V_{DS}|)} = 1.736K\Omega$$

(2) When $V_S = 1, V_{GS} = 4$ and $V_{SB} = 1$

$$|V_T| = |V_{T0}| + \gamma[\sqrt{2|\Phi_F| + |V_{SB}|} - \sqrt{2|\Phi_F|}] = 0.893$$

$$r_{on} = \frac{1}{\partial I_D/\partial V_{DS}} = \frac{L}{KW(|V_{GS}| - |V_T| - |V_{DS}|)} = 2.402K\Omega$$

(3) When $V_S = 2, V_{GS} = 3$ and $V_{SB} = 2$

$$|V_T| = |V_{T0}| + \gamma[\sqrt{2|\Phi_F| + |V_{SB}|} - \sqrt{2|\Phi_F|}] = 1.039$$

$$r_{on} = \frac{1}{\partial I_D/\partial V_{DS}} = \frac{L}{KW(|V_{GS}| - |V_T| - |V_{DS}|)} = 3.806K\Omega$$

(4) When $V_S = 3, V_{GS} = 2$ and $V_{SB} = 3$

$$|V_T| = |V_{T0}| + \gamma[\sqrt{2|\Phi_F| + |V_{SB}|} - \sqrt{2|\Phi_F|}] = 1.162$$

$$r_{on} = \frac{1}{\partial I_D/\partial V_{DS}} = \frac{L}{KW(|V_{GS}| - |V_T| - |V_{DS}|)} = 8.905K\Omega$$

(5) When $V_S = 4, V_{GS} = 1$ and $V_{SB} = 4$

$$|V_T| = |V_{T0}| + \gamma[\sqrt{2|\Phi_F| + |V_{SB}|} - \sqrt{2|\Phi_F|}] = 1.269$$

$V_{GS} < V_T$ The device is cutoff, so r_{on} = infinity

(6) When $V_S = 5, V_{GS} = 0$ and $V_{SB} = 5$

The device is cutoff, so r_{on} = infinity

Vs(V)	R(Ω)
0.0	1.736K
1.0	2.402K
2.0	3.806K
3.0	8.905K
4.0	infinity
5.0	infinity

Assignment 2

3-2 An NMOS with W=50μm and L=0.5μm operates in the saturated region and its layout is folded shown as Fig3.2. Calculate the all capacitances by using the parameters in Table3.2 and C_{ox}=3.8×10^{-3} F/m, V_R=0.6V. Assume that the minimum size (lateral) of S/D region is 1.5μm

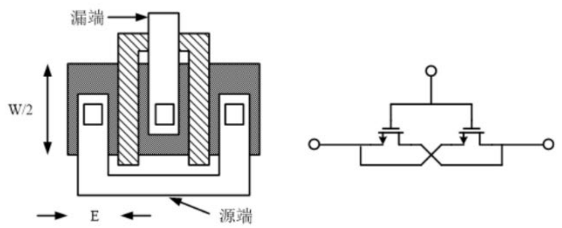


Fig.3.2

Answer:

$$C_{j0} = 0.56 \times \frac{10^{-3}F}{m^2}, C_{jsw0} = 0.35 \times \frac{10^{-11}F}{m}, m_j = 0.45, m_{jsw} = 0.2$$

$$C_{ov} = 0.4 \times \frac{10^{-9}F}{m}, W = 50\mu m, L = 0.5\mu m, L_D = 0.08\mu m, E = 1.5\mu m$$

$$V_R = 0.6V, 2\Phi_F = 0.9V, C_{ox} = 3.8 \times 10^{-3}F/m^2, P_{SUB} = 9 \times 10^8 m^{-3}$$

$$\varepsilon_{si} = 11.7 \times 8.85 \times 10^{-12}F/m, q = 1.6 \times 10^{-19}C$$

$$C_j = \frac{C_{j0}}{(1 + V_R/2\Phi_F)^{m_j}} = 0.445\ fF/\mu m^2 \quad C_{jsw} = \frac{C_{jsw0}}{(1 + V_R/2\Phi_F)^{m_{jsw}}} = 3.16 \times \frac{10^{-3}fF}{\mu m}$$

$$L_{eff} = L - 2L_D = 0.34\ \mu m \qquad C_d = WL_{eff}\sqrt{q\varepsilon_{si}P_{SUB}/4\Phi_F} = 1.55 \times 10^{-6}fF$$

$$C_{DB} = \frac{W}{2}EC_j + 2(\frac{W}{2} + E)C_{jsw} = 16.85fF$$

$$C_{SB} = 2(\frac{W}{2}EC_j + 2(\frac{W}{2} + E)C_{jsw}) = 33.71fF$$

$$C_{GD} = 2(\frac{W}{2}C_{ov}) = 20.0fF$$

$$C_{GS} = \frac{2}{3}WL_{eff}C_{ox} + WC_{ov} = 63fF$$

$$C_{GB} = \frac{WL_{eff}C_{ox}C_d}{(WL_{eff}C_{ox} + C_d)} = 1.55 \times 10^{-6}fF$$

Table.3.1

Typical Parameter Value

Parameter Symbol	Parameter Description	n-Channel	p-Channel	Units
V_{T0}	Threshold voltage(V_{BS}=0)	0.7	-0.8	V
K	Transconductance parameter(in saturation)	134	50	μA/V^2
γ	Bulk threshold parameter	0.45	0.4	V$^{1/2}$
λ	Channel length modulation parameter	0.1	0.2	V^{-1}
2|ϕ_F|	Surface potential at strong inversion	0.9	0.8	V

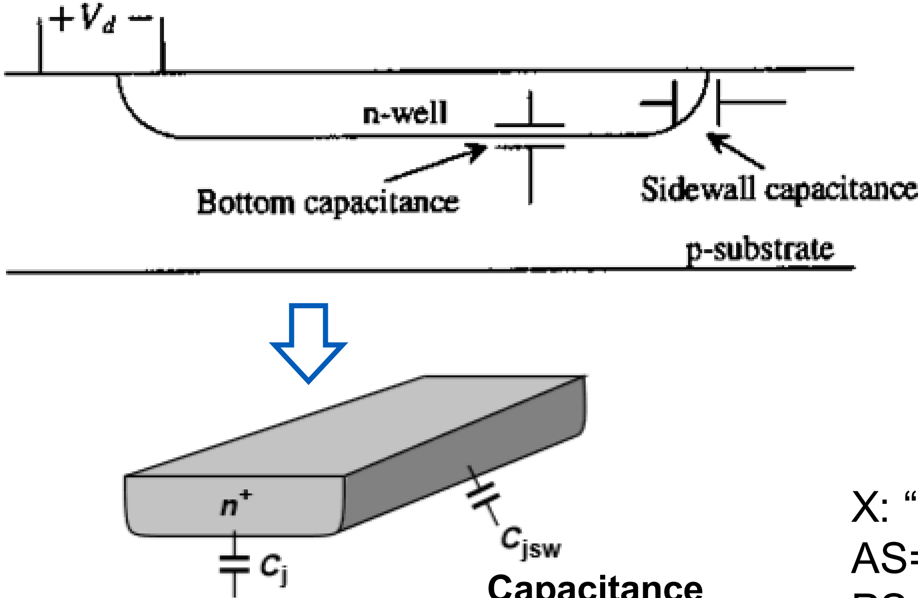
Table.3.2

NMOS Model			
LEVEL=1	VTO=0.7	GAMMA=0.45	PHI=0.9
PSUB=9e+14	LD=0.08e-6	UO=350	LAMBDA=0.1
TOX=9e-9	PB=0.9	CJ=0.56e-3	CJSW=0.35e-11
MJ=0.45	MJSW=0.2	CGDO=0.4e-9	JS=1.0e-8
PMOS Model			
LEVEL=1	VTO=-0.8	GAMMA=0.4	PHI=0.8
PSUB=5e+14	LD=0.09e-6	UO=100	LAMBDA=0.2
TOX=9e-9	PB=0.9	CJ=0.94e-3	CJSW=0.32e-11
MJ=0.5	MJSW=0.3	CGDO=0.3e-9	JS=0.5e-8

上表给出的是 0.5μm 工艺 level 1 MOS SPICE 模型参数的典型值，其中的参数定义如下：

VTO:	VSB=0 时的阈值电压	（单位：V）
GAMMA:	体效应系数	（单位：V$^{1/2}$）
PHI:	2Φ_F	（单位：V）
TOX:	栅氧厚度	（单位：m）
NSUB:	衬底掺杂浓度	（单位：cm^{-3}）
LD:	源/漏侧扩散长度	（单位：m）
UO:	沟道迁移率	（单位：cm2/(v/s)）
LAMBDA:	沟道长度调制系数	（单位：V^{-1}）
CJ:	单位面积的源/漏结电容	（单位：F/m^2）
CJSW:	单位长度的源/漏侧壁结电容	（单位：F/m）
PB:	源/漏结内建电势	（单位：V）
MJ:	CJ 公式中的幂指数	（无单位）
MJSW:	CJSW 等式中的幂指数	（无单位）
CGDO:	单位宽度的栅/漏交叠电容	（单位：F/m）
CGSO:	单位宽度的栅/源交叠电容	（单位：F/m）
JS:	源/漏结单位面积的漏电流	（单位：A/m^2）

MOS Device Capacitance: Depletion Cap



Capacitance per area：F/m²

Capacitance per perimeter：F/m

$$C_{BX} = \frac{(CJ)(AS)}{\left[1-\left(\frac{v_{BX}}{PB}\right)\right]^{MJ}} + \frac{(CJSW)(PS)}{\left[1-\left(\frac{v_{BX}}{PB}\right)\right]^{MJSW}}$$

Bottom-plate Capacitance ***(per area)***

Side-wall capacitance ***(per perimeter)***

X: “S” or “D”
AS=area of the source
PS=perimeter of the source
CJSW=zero bias, bulk-source sidewall capacitance
MJSW=bulk-source sidewall grading coefficient

Assignment 2

2-3 There is an N-type current source, I_D is 0.5mA, and the drain-source voltage V_{DS} must more than 0.4V when it works as a current source. If the minimum output resistance is 20 KΩ, determine the length and width of the device by using the parameters in Table.2.2.

Answer:

$$\begin{cases} r_o = \dfrac{1}{\lambda I_D} = 20K\Omega \\ I_D = 0.5mA \end{cases} \Rightarrow \quad \lambda = 0.1$$

From the table3.2, L can be determined as L=0.5um.(

$$L_{eff} = L - 2L_D = 0.5\mu m - 2\times 0.08\mu m = 0.34\mu m$$

Calculating W

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L_{eff}}(V_{GS}-V_{TH})^2, \quad V_{GS}-V_{TH}=V_{DSAT}=0.4V$$

$$\frac{W}{L_{eff}} = \frac{I_D}{\frac{1}{2}\mu_n C_{ox}(V_{GS}-V_{TH})^2} = \frac{0.5\times 10^{-3}}{\frac{1}{2}\times 134\times 10^{-6}\times 0.4^2} = 46.64$$

$$\therefore \quad W = 46.64L_{eff} = 15.86\mu m$$

Assignment 2

2-4 A "ring" MOS structure is shown in Fig.2.3. Explain how the device operations and estimate its equivalent aspect ratio. Calculate the drain junction capacitance of the structure. (use Cj and Cjsw)

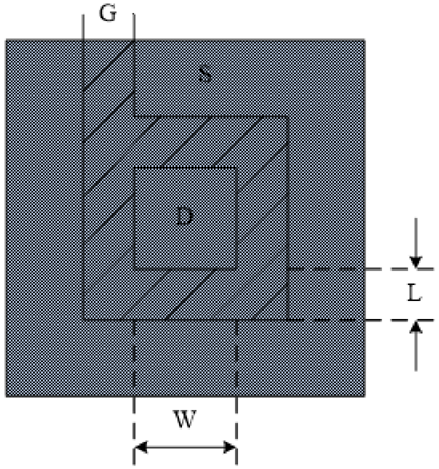


Fig.2. 3

Answer:

- Width/length ratio is 4W/L

- $$C_{DB} = W^2 C_j + 4WC_{jsw}$$

Assignment 2

2-5 Find the small-signal model (g_m, g_{mb}, g_{ds}) for an n-channel transistor with the drain at 4 V, gate at 4 V, source at 2 V, and the bulk at 0 V. Assume the model parameters from Table.2.1, and W/L = 10 µm/1 µm.

Answer:

$$V_T = V_{T0} + \gamma\left[\sqrt{2|\Phi_F| + v_{SB}} - \sqrt{2|\Phi_F|}\right]$$

$$V_T = 0.7 + 0.45\left[\sqrt{0.9 + 2.0} - \sqrt{0.9}\right] = 1.04\ \ V$$

$$I_D = \frac{KW}{L}(v_{GS} - v_T)^2(1 + \lambda v_{DS})$$

$$I_D = 134 \times 10^{-6} \times 10 \times (2 - 1.04)^2(1 + 0.1 \times 2) = 1482 \times 10^{-6}\ \ \mathrm{A}$$

$$g_m = \sqrt{4\frac{KW}{L}I_D}$$

$$g_m = \sqrt{4 \times 134 \times 10^{-6} \times 10 \times 1482 \times 10^{-6}} = 2.818 \times 10^{-3}\ \ \mathrm{S}$$

$$g_{mb} = g_m \frac{\gamma}{2(2|\Phi_F| + V_{SB})^{\frac{1}{2}}}$$

$$g_{mb} = 2.818 \times 10^{-3}\frac{0.45}{2(0.9 + 2.0)^{\frac{1}{2}}} = 372.3 \times 10^{-6}\ \ \mathrm{S}$$

$$g_{ds} = \frac{\lambda I_D}{1 + \lambda V_{DS}}$$

$$g_{ds} = 1482 \times 10^{-6} \times 0.1 \div 1.2 = 123.5 \times 10^{-6}\ \ \mathrm{S}$$

Course Arrangements

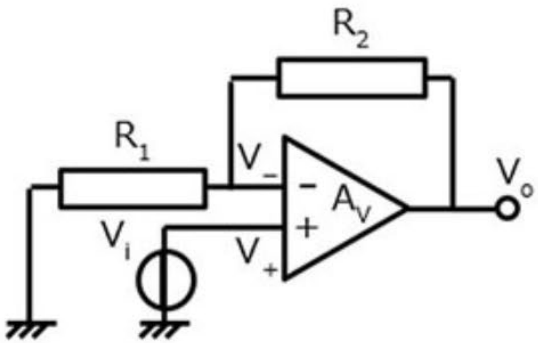
课数	内容	课数	内容
1	导论	9	差分放大器
2	工艺流程	10	运算放大器
3	器件模型一	11	逻辑门
4	器件模型二	12	组合逻辑
5	模拟基本单元	13	时序逻辑
6	电流镜与基准	14	加法器/乘法器
7	单级放大器	15	集成电路专题讲座一
8	课堂测验	16	集成电路专题讲座二

Outline

- General Consideration
- One-Stage Op Amps
- Two-Stage Op Amps
- Compensation of 2-Stage Op Amps
- Other Issues of Op Amps

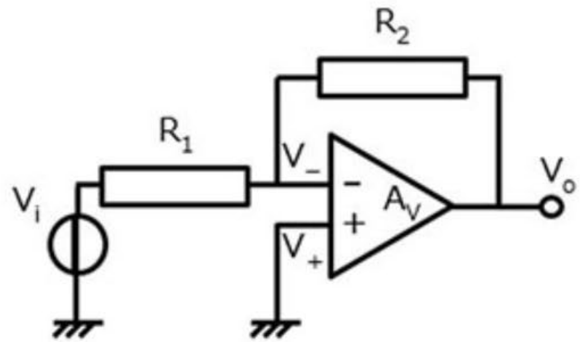
Why it is called Op. Amp

For different operations based on feedbacks



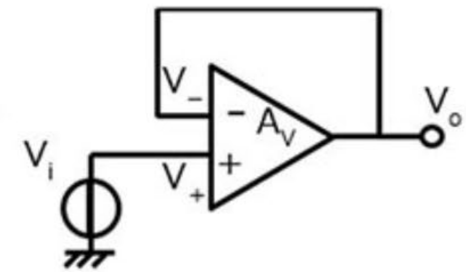
Noninverting amplifier

$G_V^* = (R_1 + R_2) / R_1$



Inverting amplifier

$G_V^* = R_2 / R_1$

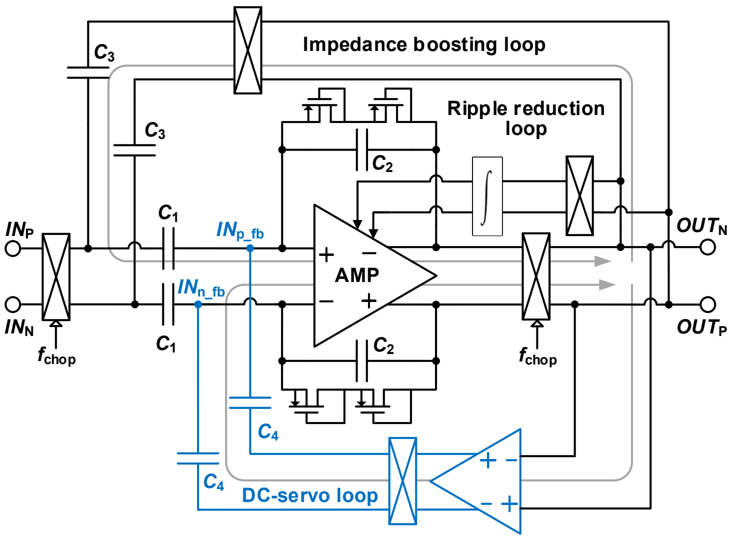


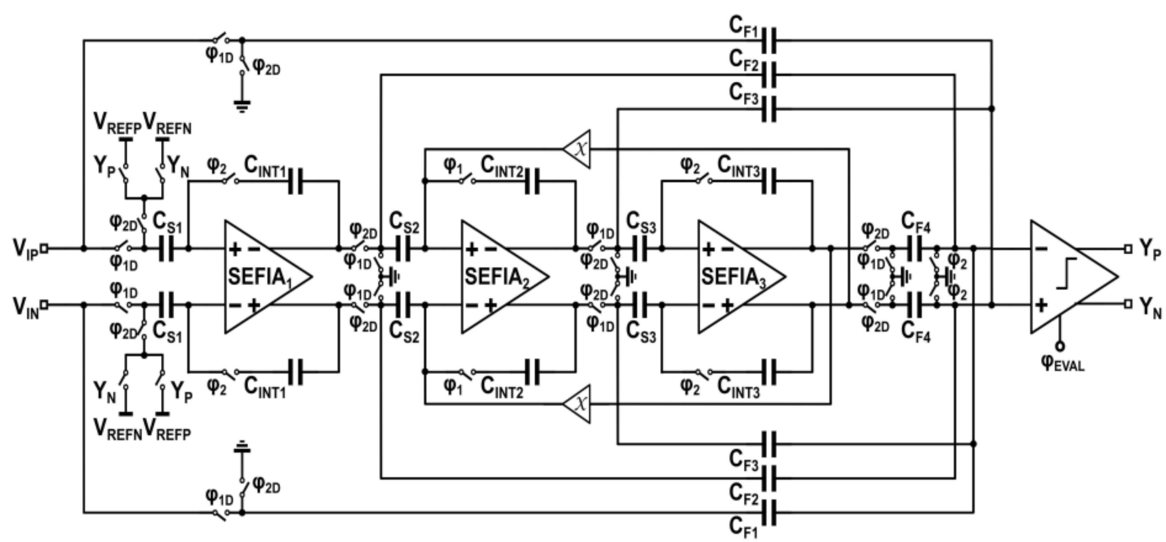
Voltage follower

$G_V^* = 1$

Why it is so important

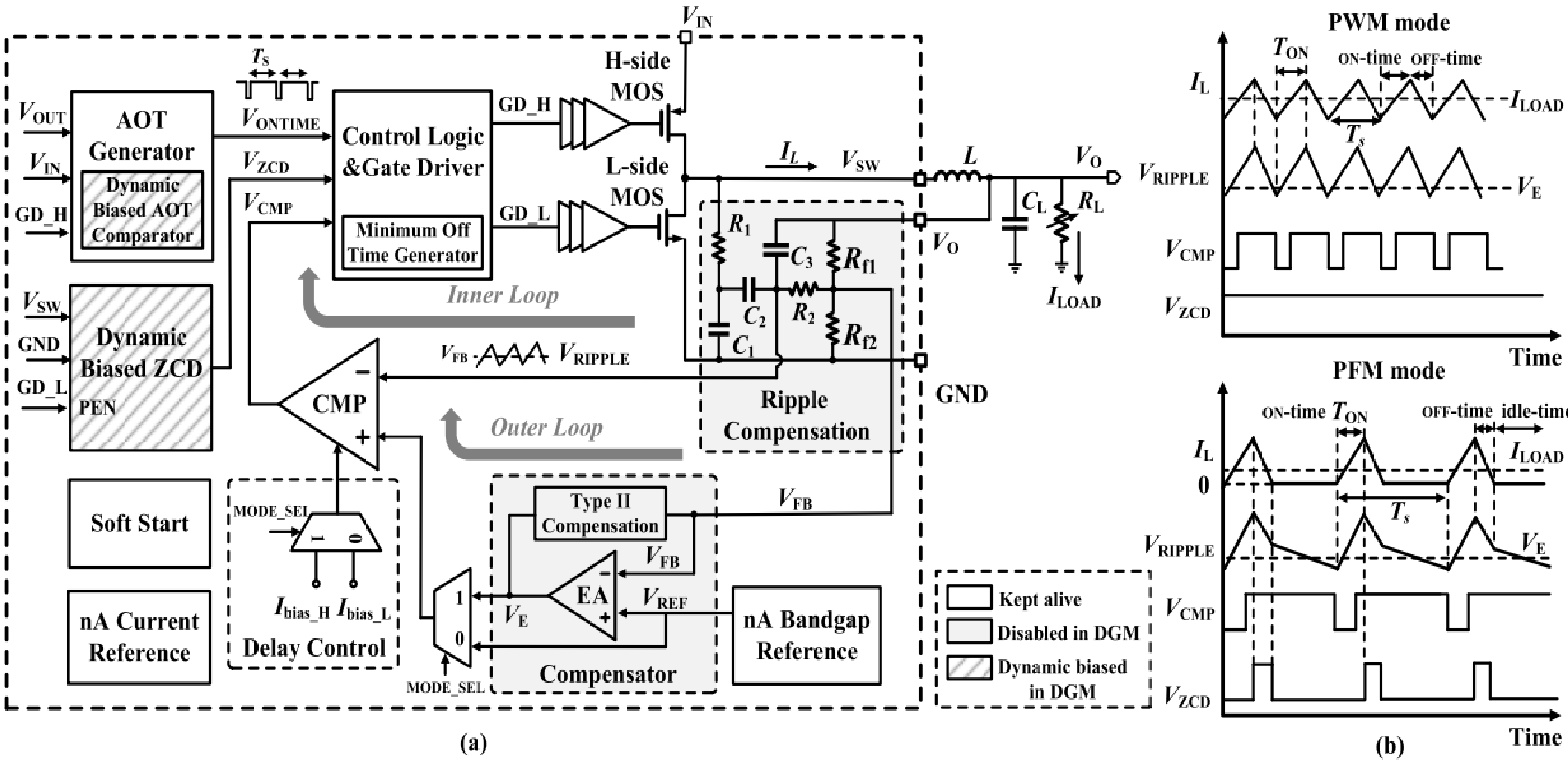
In signal chain applications: （IA+ADC）





Why it is so important

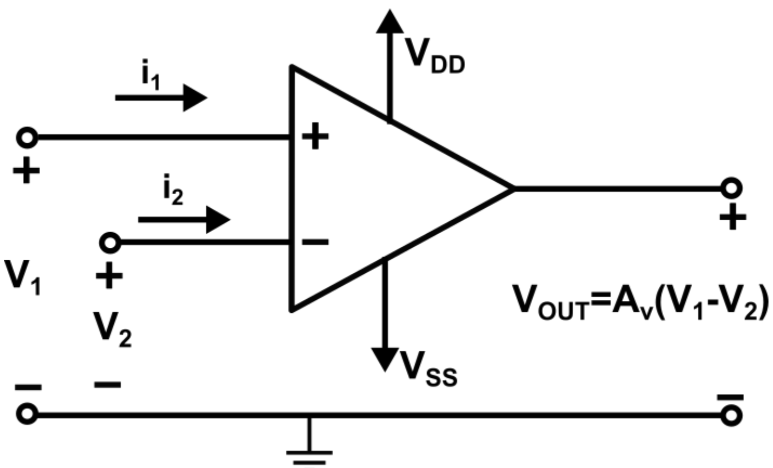
In power management applications:



Basic Concept of Op Amp

A high-gain differential amplifier

- **Ideal op amp**
  - Voltage controlled voltage source
  - **Infinite** gain
  - Infinite **input impedance**
  - Zero **output impedance**
  - Infinite CMRR and PSRR



- **Application**
  - DC generation
  - Amplification
  - Integration/Differentiation
  - Filtering (HP/LP/BP)

If the infinite differential gain, then

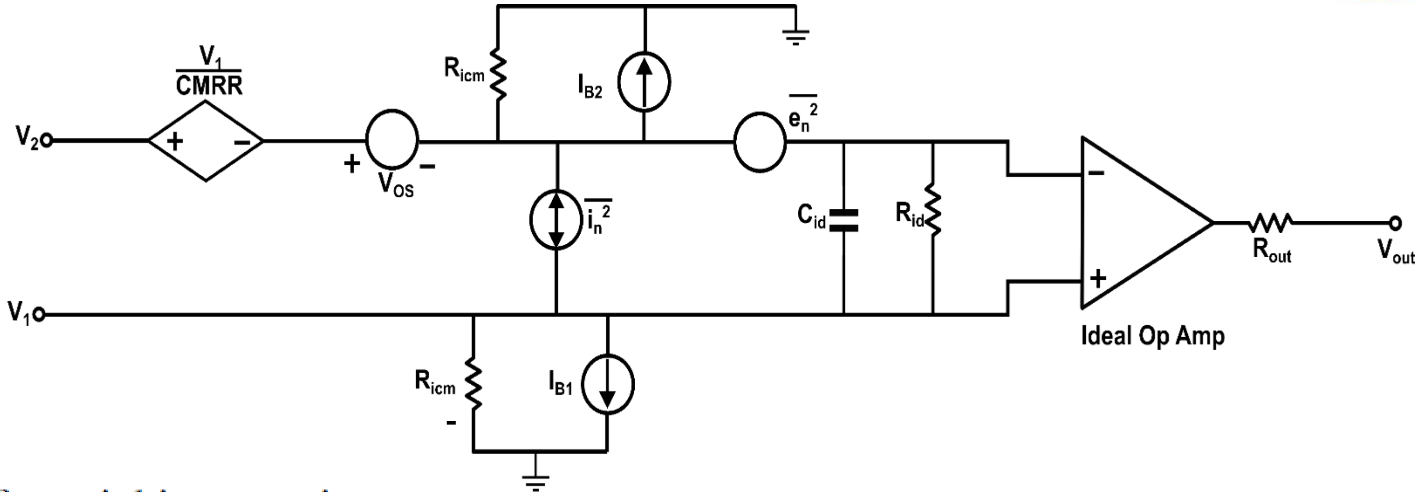
$$v_1 - v_2 = v_i = 0$$

$$i_1 = 0 \text{ and } i_2 = 0$$

The differential input voltage is zero and no current flow into or out of the differential input

Feedback

Nonideal model of Op amp



where

R_{id} = differential input resistance

C_{id} = differential input capacitance

R_{icm} = common mode input resistance

V_{OS} = input-offset voltage

I_{B1} and I_{B2} = differential input-bias currents

I_{OS} = input-offset current ($I_{OS} = I_{B1}$-I_{B2})

$CMRR$ = common-mode rejection ratio

e_n^2 = voltage-noise spectral density (mean-square volts/Hertz)

i_n^2 = current-noise spectral density (mean-square amps/Hertz)

Performance Parameters

□ Gain

- Open-loop gain: DC条件下，在输入加一小信号，得到输出电压

  $A_d = 10 \sim 10^5$ (20dB~100dB)

  High gain: $A_d \sim$ 80dB - 100dB

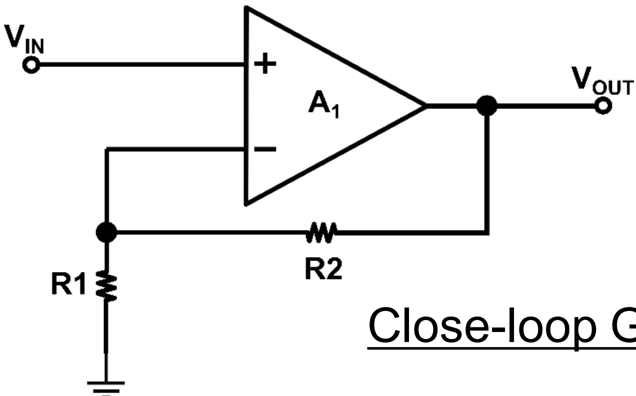
- Common-mode Gain: 在输入加共模小信号，得到输出电压

  $A_{CM} \sim$ 20dB - 40dB

- CMRR(Common-mode Rejection Ratio)

  CMRR ~ 40dB - 80dB

Example Non-inverting Voltage Amplifier.



- Input and output swing: rail-to-rail
- Amplifier buffer
- **High open-gain could suppress nonlinearity**

Close-loop Gain: $$\left(V_{in} - \frac{R_2}{R_1 + R_2} V_{out}\right) A_1 = V_{out}$$

$$\frac{V_{out}}{V_{in}} = \frac{A_1}{1 + \frac{R_2}{R_1 + R_2} A_1} = \frac{R_1 + R_2}{R_2} \frac{A_1}{1 + \frac{R_1 + R_2}{R_2} A_1} \approx \left(1 + \frac{R_1}{R_2}\right)\left(1 - \frac{R_1 + R_2}{R_2} \frac{1}{A_1}\right)$$

$$= \frac{1}{\beta}\left(1 - \frac{1}{\beta A_1}\right) \xrightarrow{\beta A \to \infty} \frac{1}{\beta}$$

Feedback coefficient: $\beta = \frac{R_2}{R_1 + R_2}$

Loop gain: βA_1

Relative gain error: $\frac{1}{\beta A_1}$

The circuit has a nominal gain of 10. i.e., $1+R_1/R_2=10$
If a gain error **<1%** => $\boldsymbol{A_1>1000}$

Higher open gain ➔ smaller gain error

Small-signal behavior of frequency response

- Differential and common-mode frequency response

$$V_{out}(s) = A_d(s)\left[V_1(s) - V_2(s)\right] \pm A_C(s)\left(\frac{V_1(s) + V_2(s)}{2}\right)$$

- Differential-frequency response:

$$A_d(s) = \frac{A_{d0}}{\left(\frac{s}{p_1} - 1\right)\left(\frac{s}{p_2} - 1\right)\left(\frac{s}{p_3} - 1\right)\cdots} = \frac{A_{d0}p_1p_2p_3\cdots}{\left(s - p_1\right)\left(s - p_2\right)\left(s - p_3\right)\cdots}$$

where p_1, p_2, p_3, … are the poles of the differential-frequency response (ignoring zeros)

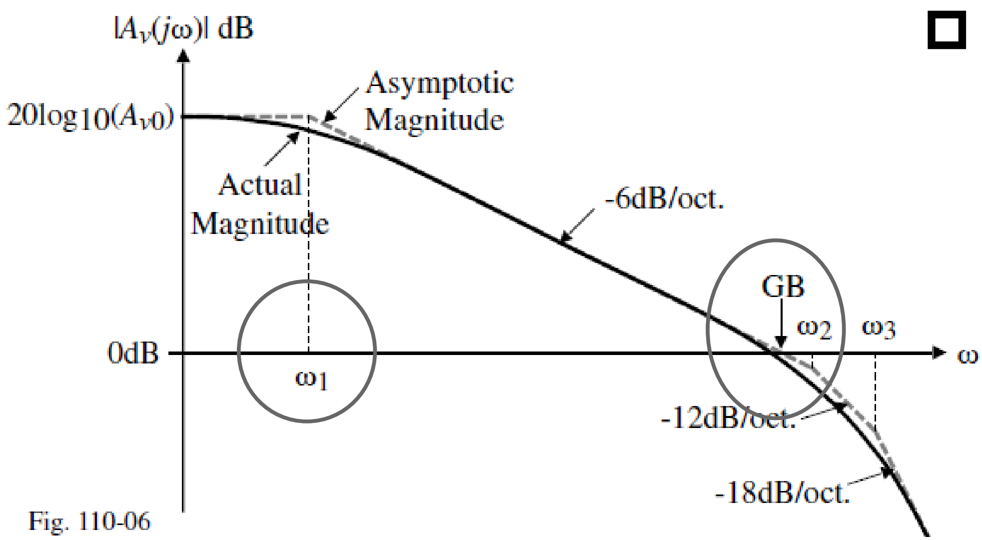


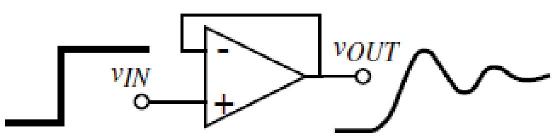
Fig. 110-06

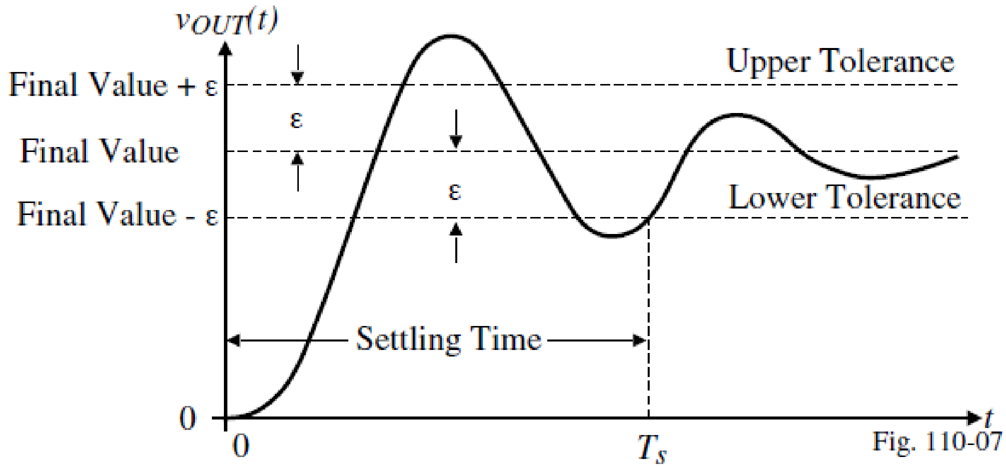
- **Bandwidth: BW**
  - **Unity-Gain frequency: GB** $f_u \rightarrow w_u$
  - **-3dB frequency:** $f_{-3dB} \rightarrow w_1$

Large-signal behavior of frequency response

在瞬态输入**大信号**工作时，表征运放的速度：

- 转换速率 SR (Slew Rate)
  - SR= output voltage rate limit of the op amp
- 建立时间 T_S (Settling time, usually <1%)

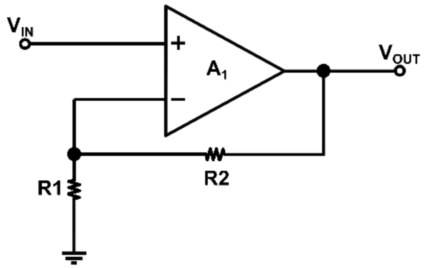


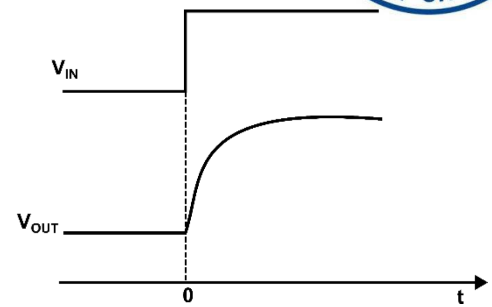


Example

Assume the op amp is a single-pole voltage amplifier and V_{in} is a small step input. Calculate the time for V_{out} to reach within 1% and the unity-gain bandwidth if $1+R_1/R_2=10$ and the settling time <5ns.

Solution: *Speed vs. Bandwidth*





For a single-pole amp:

$$A(s) = \frac{A_0}{(1 + s/\omega_0)}$$

$$\frac{V_{out}}{V_{in}}(s) = \frac{A(s)}{1 + \frac{R_2}{R_1 + R_2} A(s)} = \frac{A_0/(1 + A_0\beta)}{1 + \frac{s}{(1 + A_0\beta)\omega_0}}$$

Bandwidth expanding

$$\tau = \frac{1}{(1 + A_0\beta)\omega_0} \approx \left(1 + \frac{R_1}{R_2}\right)\frac{1}{A_0\omega_0}$$

$$V_{in} = au(t) \Rightarrow V_{out} = a\left(\frac{A_0}{1 + \beta A_0}\right)\left(1 - \exp\frac{-t}{\tau}\right)u(t)$$

For 1% settling: $V_{out} = 0.99V_F$ $\quad 1-\exp\frac{-t_{1\%}}{\tau} = 0.99 \Rightarrow t_{1\%} = \tau \ln 100 = 4.6\tau < 5ns$

$$\tau \approx 1.09ns$$

$$A_0\omega_0 \approx (1 + R_1/R_2)/\tau = 9.21\,Grad/s \qquad (1.47GHz)$$

For 0.1% settling: $t_{0.1\%} = \tau \ln 1000 = 6.9\tau$

Performance Parameters

- **Output Swing**: output voltage range without distortion
- **ICMR:** (Input Common Mode Range)
  - ICMR= the voltage range over which the input common-mode signal can vary without influence the differential performance
- **Linearity:** input-pair exhibit a nonlinear relation between its differential drain current and its input voltage
- **PSRR:** (Power Supply Rejection Ration)

$$PSRR = \frac{\Delta V_{DD}}{\Delta V_{OUT}} A_V(s) = \frac{V_O / V_{in} \left(V_{dd} = 0\right)}{V_O / V_{dd} \left(V_{in} = 0\right)}$$

- **Offset:** the minimum signal level that can be processed with reasonable quality
- **Noise**

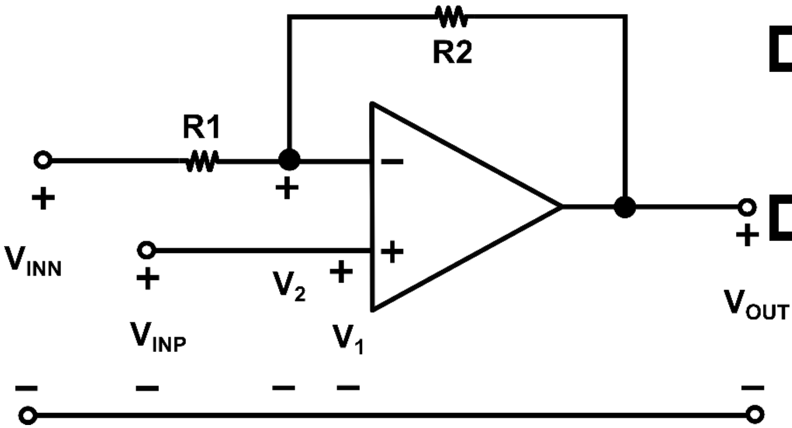
Specifications for a typical unbuffered CMOS Op Amp

Boundary Conditions	Requirement
Process Specification	See Tables 3.1-1 and 3.1-2
Supply Voltage	±2.5 V ±10%
Supply Current	100 μA
Temperature Range	0 to 70°C

Specifications	Value
Gain	≥ 70 dB
Gainbandwidth	≥ 5 MHz
Settling Time	≤ 1 μsec
Slew Rate	≥ 5 V/μsec
Input *CMR*	≥ ±1.5 V
CMRR	≥ 60 dB
PSRR	≥ 60 dB
Output Swing	≥ ±1.5 V
Output Resistance	N/A, capacitive load only
Offset	≤ ±10 mV
Noise	≤ 100nV/$\sqrt{\text{Hz}}$ at 1KHz
Layout Area	≤ 10,000 min. channel length^2

AMP and OTA

Inverting Voltage Amplifier $V_{inp} = 0$



- Input common mode: a fixed voltage
- Input range could be small, but the output range could be rail-to-rail

$$A \to \infty \quad A_V = \frac{V_{out}}{V_{in}} = -\frac{R_2}{R_1}$$

Operational Transconductance Amplifiers (OTAs)

- Driving capacitive load

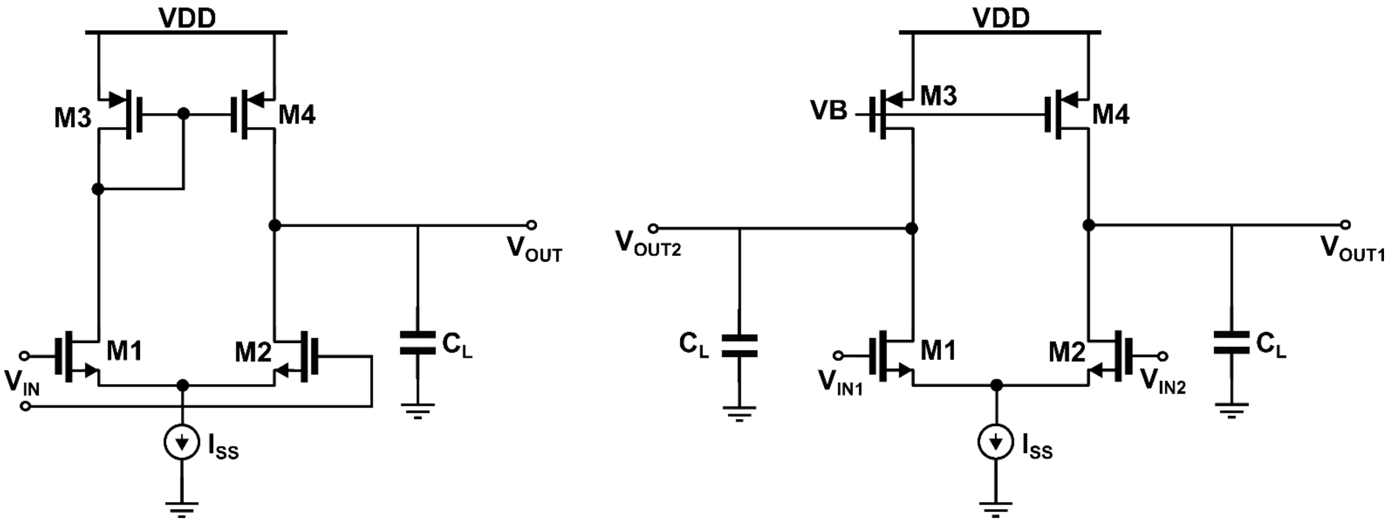
G_m stage

- High gain : **high output resistance**
- Generally be used in switched-capacitor (SC) circuits

Outline

- General Consideration
- One-Stage Op Amps（First Stage of Opamps）
- Two-Stage Op Amps
- Compensation of 2-Stage Op Amps
- Other Issues of Op Amps

Basic Topologies

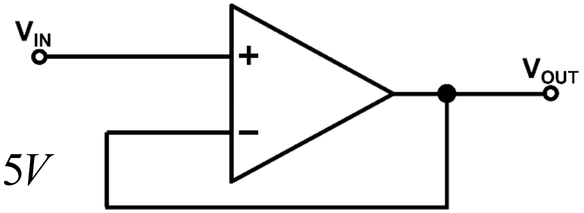


- **Low-frequency gain**: $A_O = g_{mN} r_{out} = g_{mN}\left(r_{ON} // r_{OP}\right) < g_{mN} r_O$
- **Bandwidth**: $\omega_1 = \dfrac{1}{C_L R_{out}} = \dfrac{1}{\left(r_{O2} // r_{O4}\right) C_L} \quad \omega_u = \dfrac{g_{mN}}{C_L}$
- **Output Swing** (single-side): V_{DD} -3V_{OV}
- **Mirror pole** in single ended

Example

Calculate the input common-mode voltage range and the closed-loop output impedance of **the unity-gain buffer**.

Input common-mode voltage range

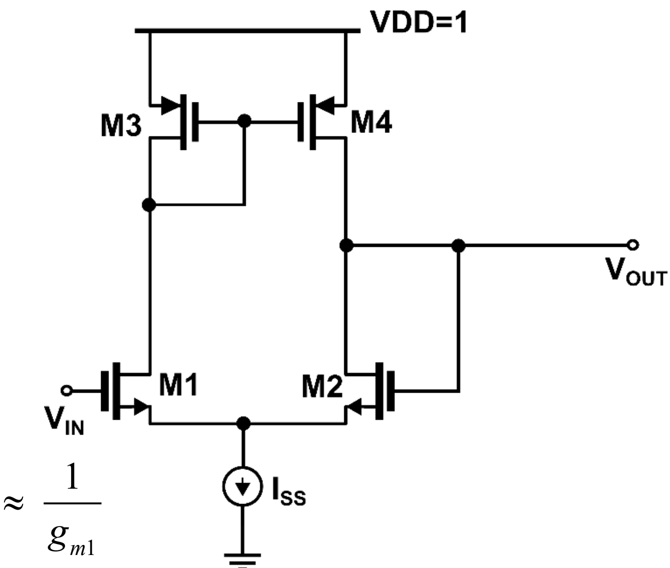


All transistors operate saturation region

$$V_{in,\min} = V_{ISS} + V_{GS1} = V_{ISSds,sat} + V_{th1} + V_{ds,sat1} = 0.1 + 0.3 + 0.1 = 0.5V$$

$$V_{in,\max} = V_{DD} - \left(\left| V_{GS3} \right| + V_{th1} \right) = 1 - (0.1 + 0.3) = 0.9V$$

$$V_{in,\max} - V_{in,\min} = V_{DD} - \left| V_{th3} \right| - 3V_{ds,sat} = 0.4V$$



Output resistance

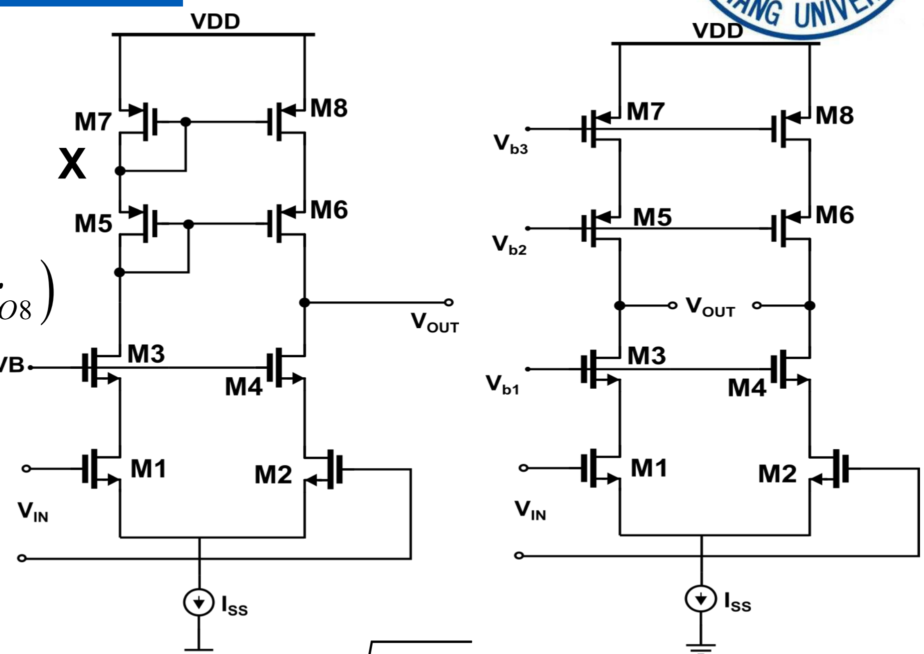
- The open-loop output impedance: $r_{O2} // r_{O4}$
- Loop gain: $g_{m1} \left(r_{O2} // r_{O4} \right)$
- The closed-loop output impedance : $\dfrac{r_{O2} // r_{O4}}{1 + g_{m1} \left(r_{O2} // r_{O4} \right)} \approx \dfrac{1}{g_{m1}}$

Voltage feedback at output

The closed-loop pole is independent of open-loop output impedance.

Telescopic Cascode Op Amps

High gain!!! ***×20~40***
Small output swing!!!



- **Low-frequency gain:**

$$A_O = g_{m2}R_{out} = g_{m2}\left(g_{m4}r_{O2}r_{O4}//g_{m6}r_{O6}r_{O8}\right)$$

$$\approx g_{mN}\left(g_{mN}r_{ON}^2//g_{mP}r_{OP}^2\right)$$

- **Output Swing (single-side):**

  V_{DD} -5V_{OV}

- **Speed:**
  - Dominant pole $\omega_1 = \dfrac{1}{C_L R_{out}}$ $\quad \omega_u = \dfrac{g_m}{C_L} = \dfrac{\sqrt{2\beta I_O}}{C_L} = \dfrac{\beta V_{eff}}{C_L}$
  - Additional poles X in high frequency
  - Mirror pole in single-ended
- **Be difficult to short telescopic OPAMP output to input (why)**

Telescopic Cascode Op Amps

Input common-mode voltage range

All transistors operate saturation region

$$V_{in,\min} = V_{ds,sat,ISS} + V_{GS2} = V_{ds,sat,ISS} + V_{th2} + V_{ds,sat2}$$

$$V_{in,\max} = V_{b1} - |V_{GS3}| + V_{th2}$$

$$V_{in,\max} - V_{in,\min} = V_{b1} - V_{th4} - 3V_{ds,sat}$$

$$V_{b1} > V_{th4} + 3V_{ds,sat}$$

Output common-mode voltage range

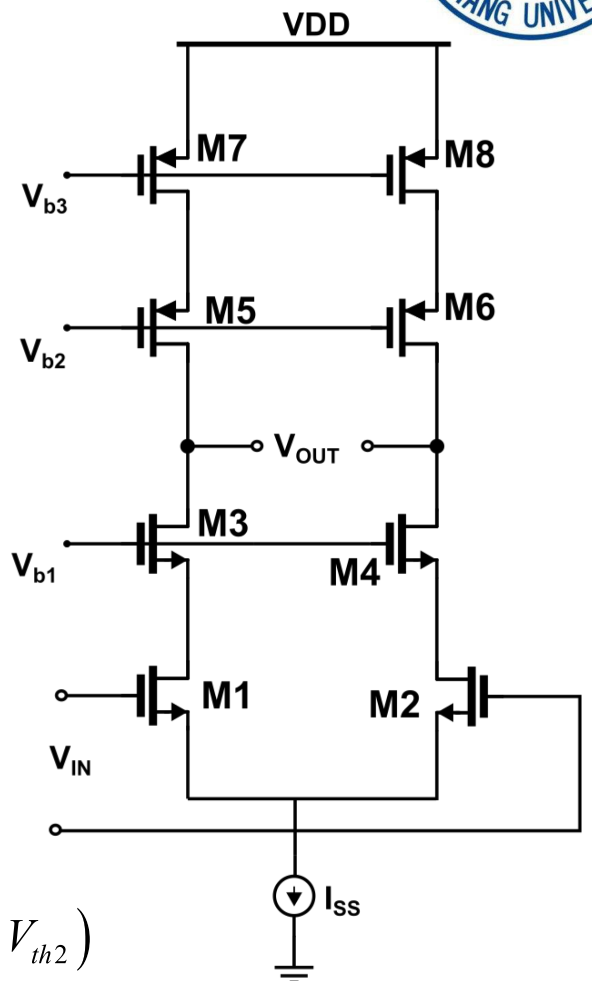
All transistors operate saturation region

$$V_{out,\min} = V_{b1} - V_{th4}$$

$$V_{out,\max} = V_{b2} + |V_{th6}|$$

Output swings: $2\left(V_{out,\max} - V_{out,\min}\right) = 2\left(V_{b2} + |V_{th6}| - V_{b1} + V_{th2}\right)$

$$V_{b2} \uparrow,\ V_{b1} \downarrow \ \Rightarrow \ \text{output range} \uparrow$$



极限值 $\rightarrow 2\left(V_{DD} - V_{ds8,sat} - V_{ds6,sat} - V_{ds4,sat} - V_{ds2,sat} - V_{ISS,ds,sat}\right) = 2\left(V_{DD} - 5V_{ds,sat}\right)$

Output common-mode voltage range of unity-gain buffer

All transistors operate saturation region

M2:

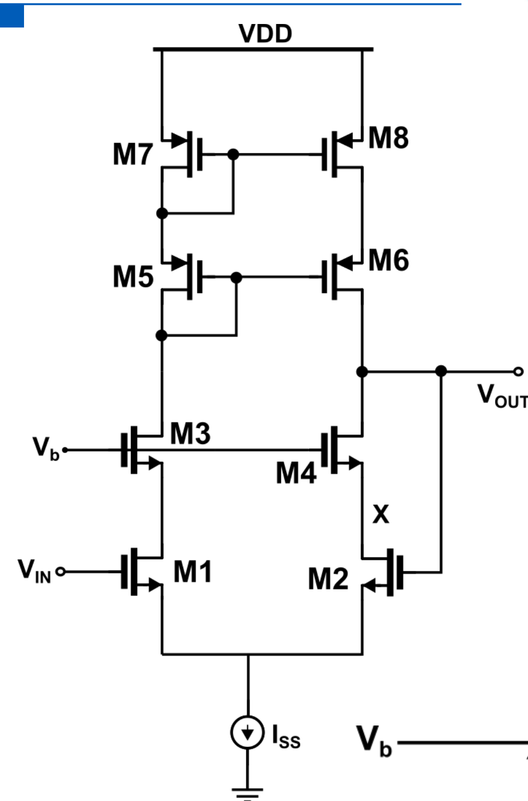
$$V_{out,\max} = V_x + V_{th2} = V_b - V_{GS4} + V_{th2}$$

M4:

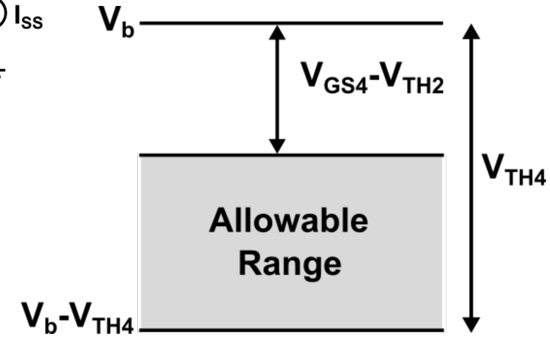
$$V_{out,\min} = V_b - V_{ds4,sat}$$

$$V_b - V_{th4} \le V_{out} \le V_b - V_{GS4} + V_{th2}$$

$$V_{out,\max} - V_{out,\min} = V_{th4} - \left(V_{GS4} - V_{th2}\right) = V_{th2} - V_{ds4,sat}$$



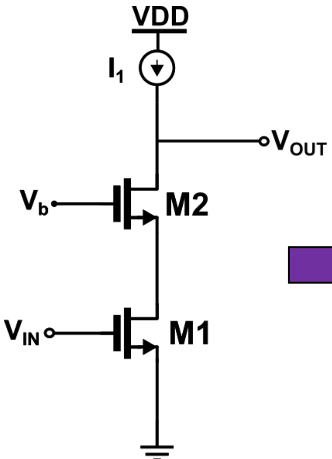
Difficult to short telescopic op amp output to input !!!

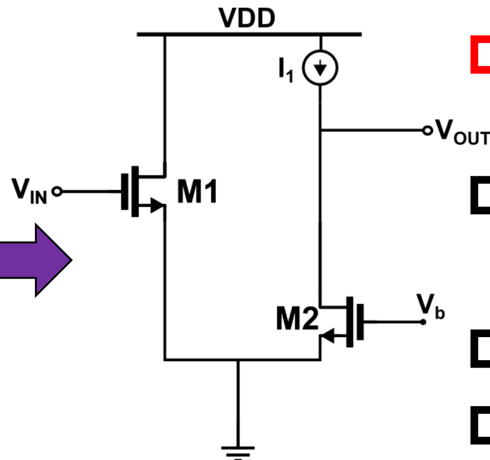


High gain, small output swing √

Unity-gain Buffer ✗

Folded Cascode Op Amps

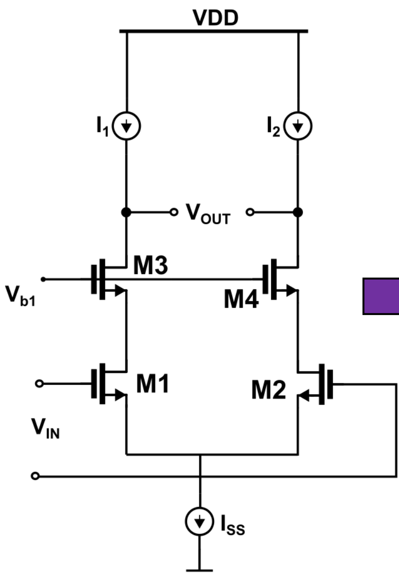


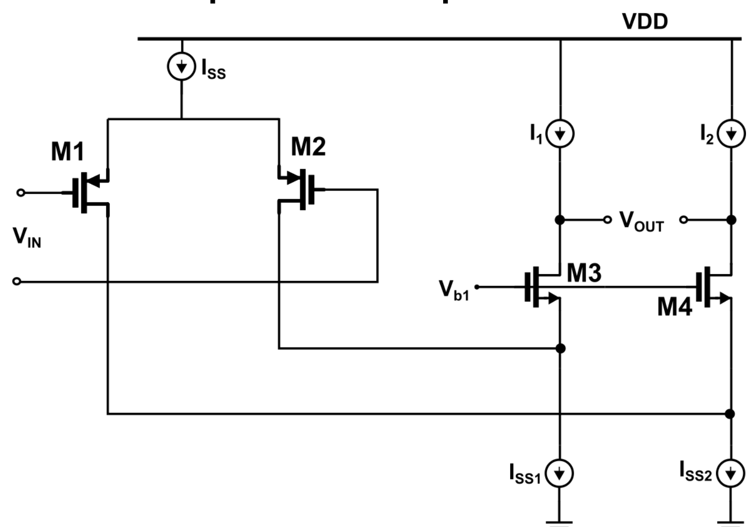


- **Not "stack" the cascode transistor on the input device**
- Consume higher power

$$P = V_{DD} \times \left(I_{SS} + I_{SS1} + I_{SS2}\right) > V_{DD} \times I_{SS}$$

- Output Voltage Swing: V_{DD} -4V_{OV}
- Output and input could short together





Folded Cascode Op Amps

- **Voltage Gain**

$$|A_V| = G_m R_{out}$$

$$|A_V| \approx g_{m1}\left[\left(g_{m3}+g_{mb3}\right) r_{O3}\left(r_{O1}//r_{O5}\right)\right] // \left[\left(g_{m7}+g_{mb7}\right) r_{O7} r_{O9}\right]$$

  - 2~3 times lower than a telescopic topology

- **Input Voltage Range: P-diff pair**

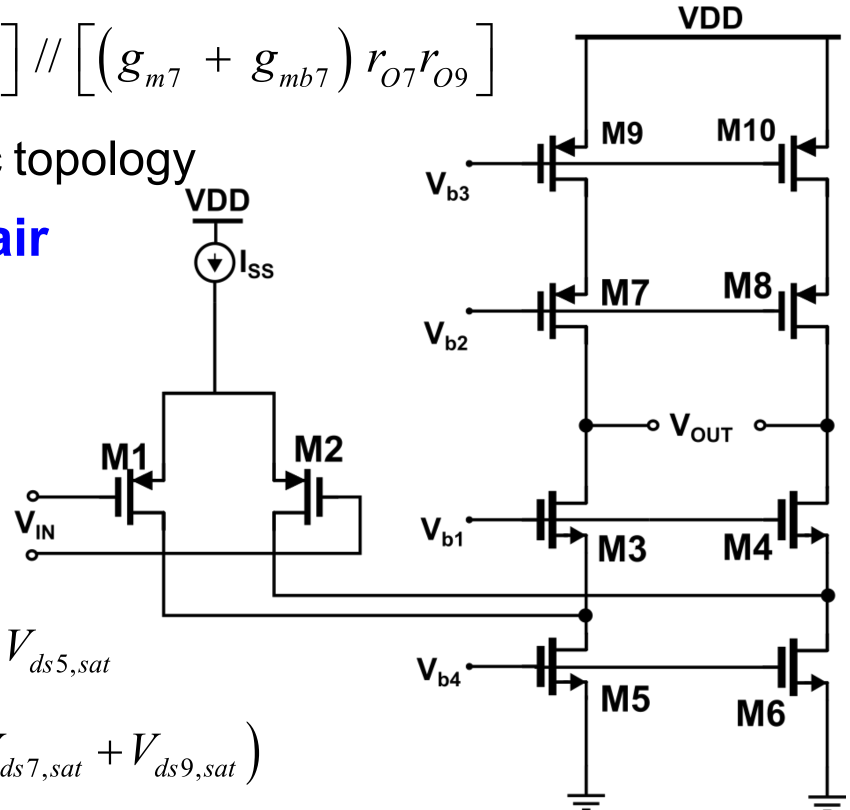
$$V_{in,\min} = 0 \quad \surd$$

$$V_{in,\max} = V_{DD} - V_{ds,sat,ISS} - V_{GS1}$$

- **Output Voltage Range**

$$V_{out,\min} = V_{b1} - V_{th3} \qquad V_{out,\min} > V_{ds3,sat} + V_{ds5,sat}$$

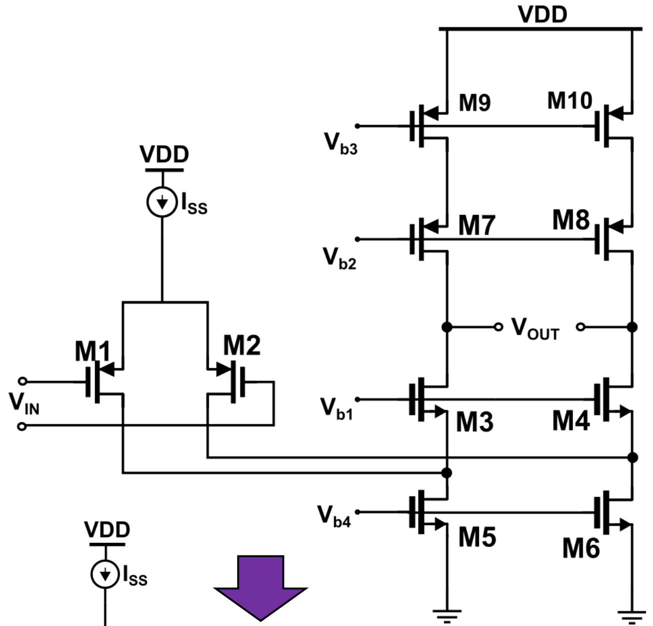
$$V_{out,\max} = V_{b2} + |V_{th7}| \qquad V_{out,\max} < V_{DD} - \left(V_{ds7,sat} + V_{ds9,sat}\right)$$



Folded Cascode Op Amps

Effect Capacitance on Non-dominant Pole

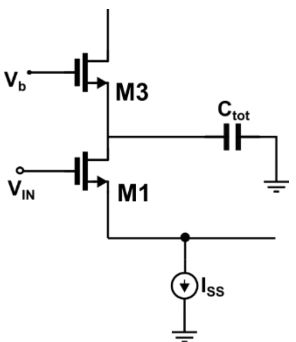
At “folding point”, a large capacitance due to a large current device M5 would be added to the total capacitance.



$$\omega_p = \frac{1}{RC}$$

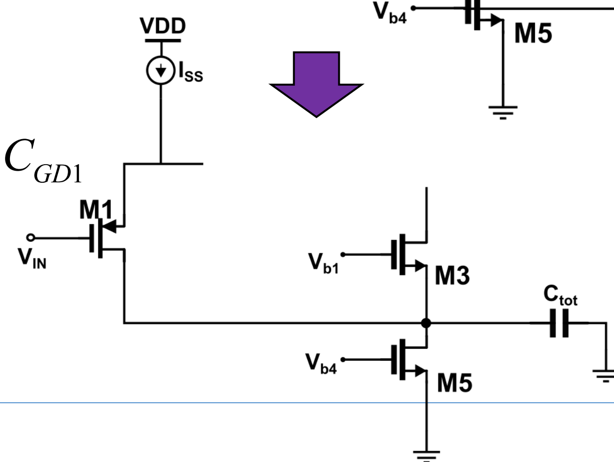
$$R = \frac{1}{g_{m3} + g_{mb3}}$$

$$C_{tot} = C_{GS3} + C_{SB3} + C_{DB1} + C_{GD1} + C_{DB5} + C_{GD5}$$



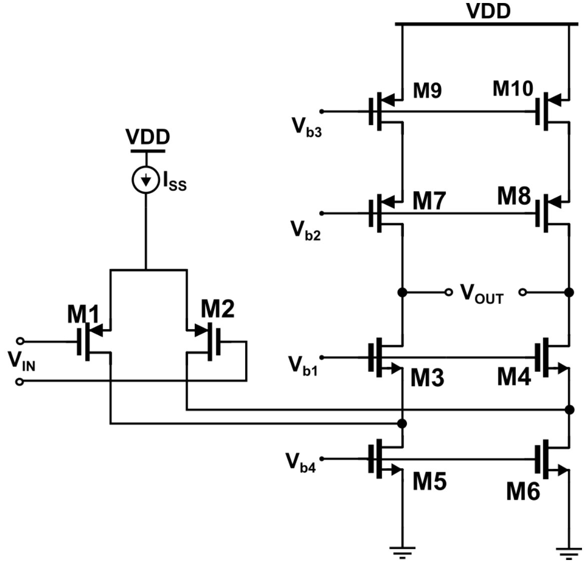
Telescopic

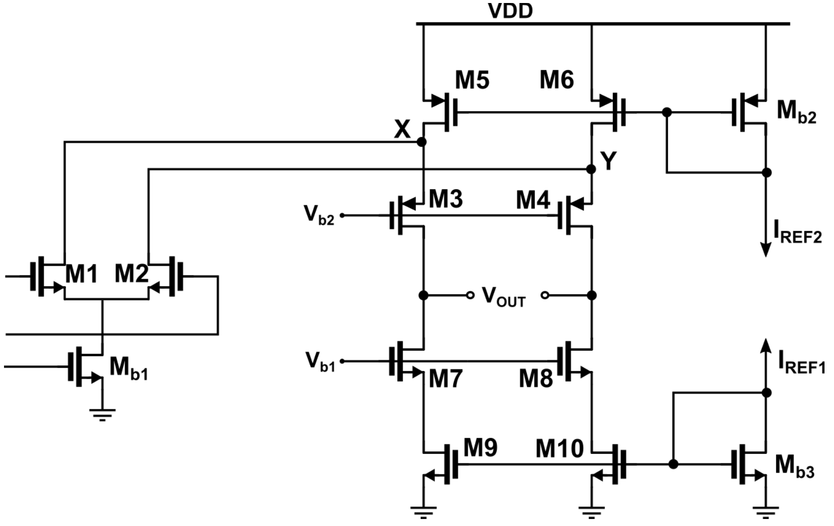
$$C_{tot} = C_{GS3} + C_{SB3} + C_{DB1} + C_{GD1}$$



Input Arrangments

NMOS vs. PMOS Input





Other Properties of Folded Cascode

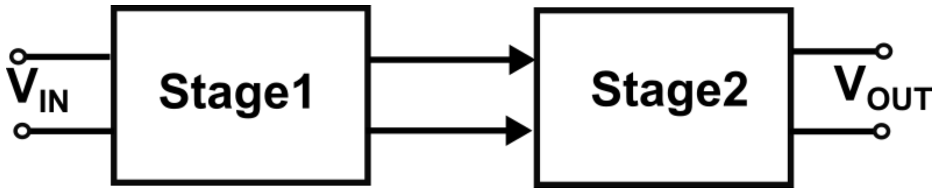
- Slighter **Higher Output Swing** than Telescopic
- Higher power dissipation, similar voltage gain, similar pole frequency
- Input and output can be shorted: 2 overdrive from bound
- A better input CM range

Outline

- General Consideration
- One-Stage Op Amps
- Two-Stage Op Amps
- Compensation of 2-Stage Op Amps
- Other Issues of Op Amps

Two-Stage Op Amps

- Design limitation: low supply voltage, high gain and large output swing



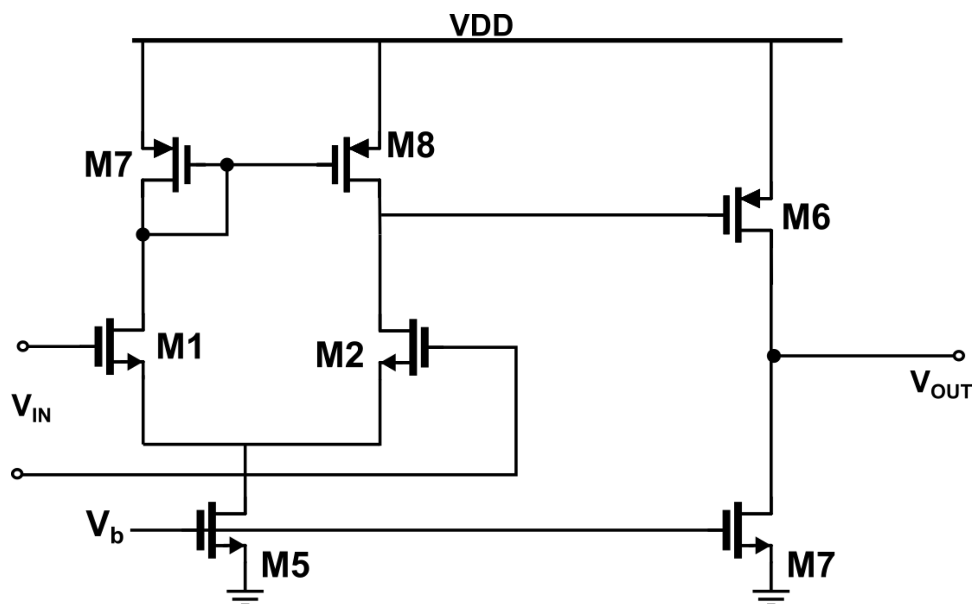
$$A_V = A_{V1} \times A_{V2}$$

Stage 1: High Gain

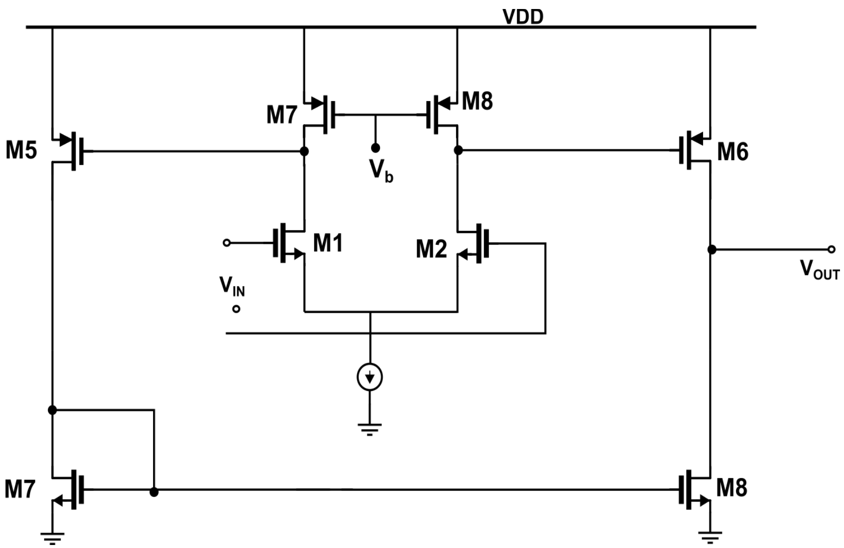
- Output swing could be small
- OTA

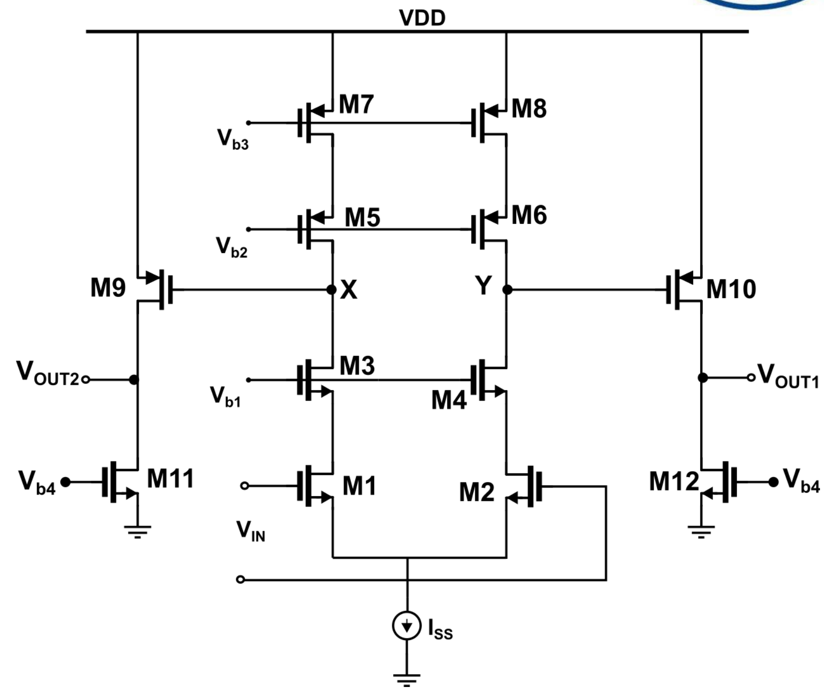
Stage 2: High Swing

- **Can we have more stages?**
  Feedback stability limits！



Two-Stage Op Amps





$$A_V = A_{V1} \times A_{V2}$$

$$A_V = g_{m1,2}\left(r_{O1,2} // r_{O3,4}\right) g_{m5,6}\left(r_{O5,6} // r_{O7,8}\right)$$

$$A_V = g_{m1}\left(g_{m3} r_{O3} r_{O1} // g_{m5} r_{O5} r_{O7}\right) g_{m9}\left(r_{O9} // r_{O11}\right)$$

$$V_{out,\min} = V_{ds7,sat}$$

$$V_{out,\max} = V_{DD} - V_{ds5,sat}$$

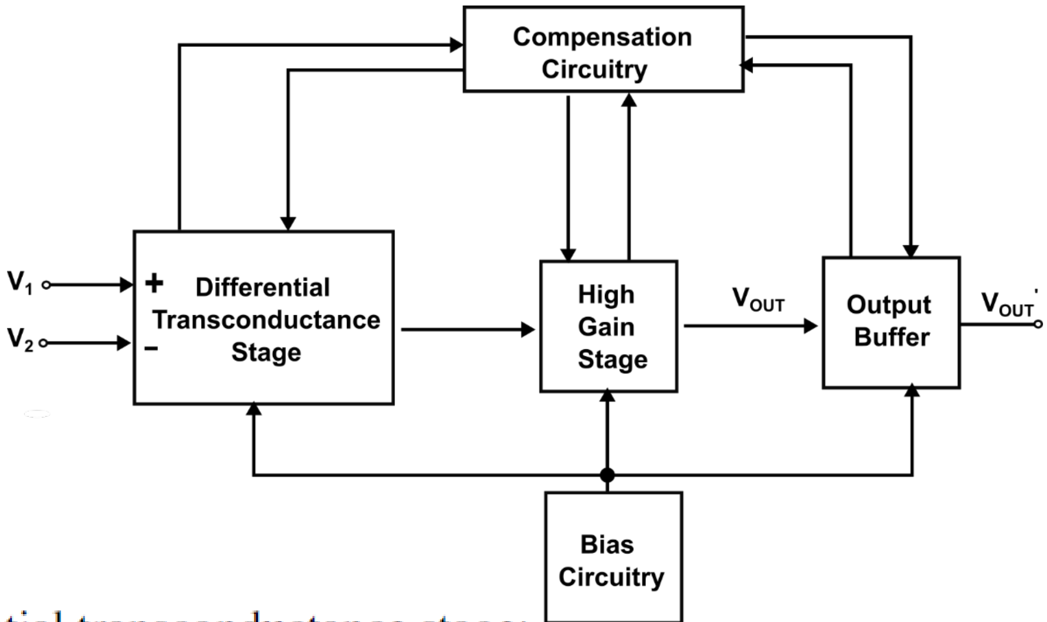
$$V_{out,\min} = V_{ds11,sat}$$

$$V_{out,\max} = V_{DD} - V_{ds9,sat}$$

Outline

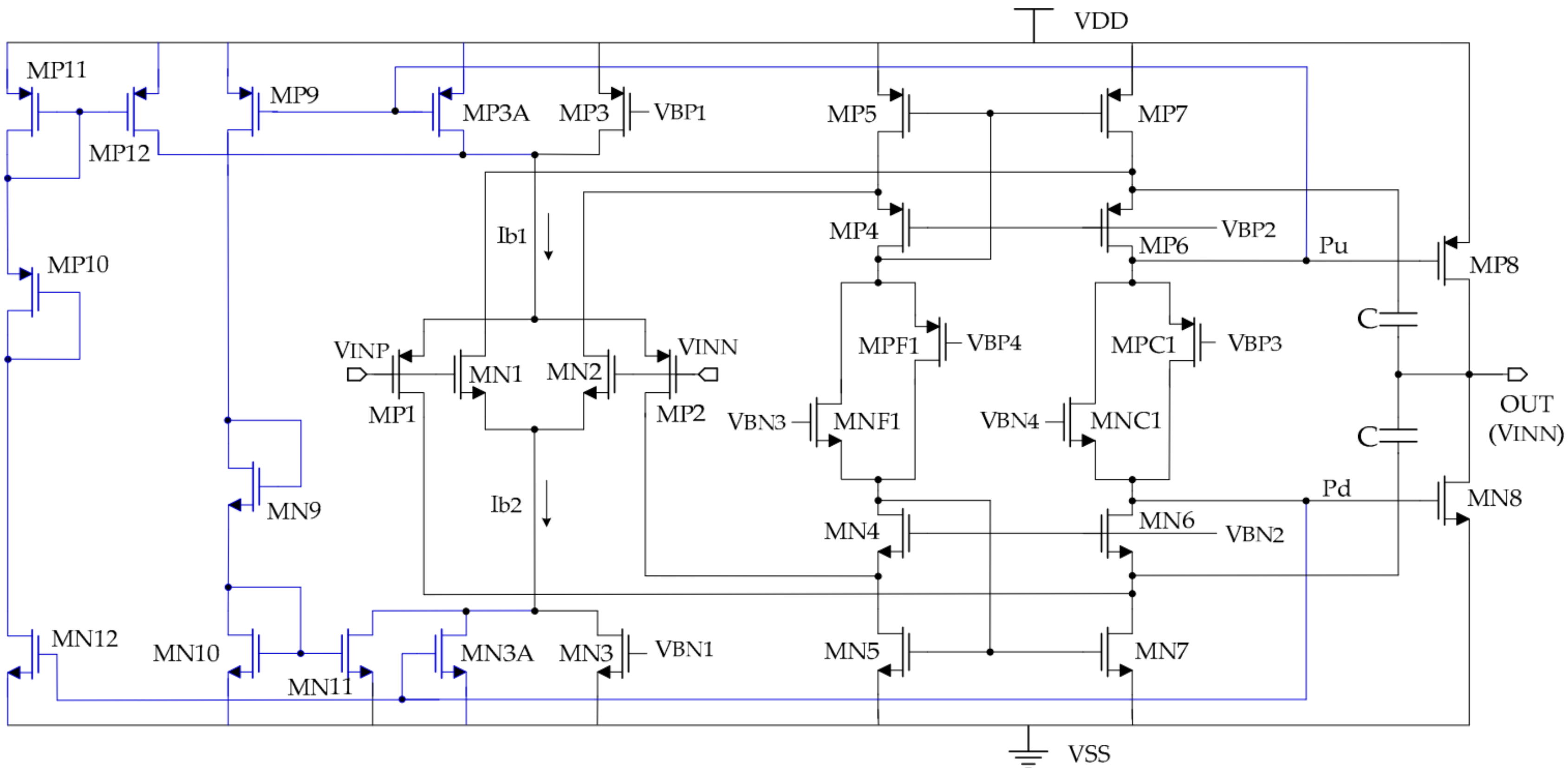
- General Consideration
- One-Stage Op Amps
- Two-Stage Op Amps
- Compensation of 2-Stage Op Amps
  - -> Control Theory
  - -> Miller compensation
- Other Issues of Op Amps

Block diagram of two-stage op-amp



- Differential transconductance stage:
  Forms the input and sometimes provides the differential-to-single ended conversion.
- High gain stage:
  Provides the voltage gain required by the op amp together with the input stage.
- Output buffer:
  Used if the op amp must drive a low resistance.
- Compensation:
  Necessary to keep the op amp stable when resistive negative feedback is applied.

Rail to rail Folded Cascode

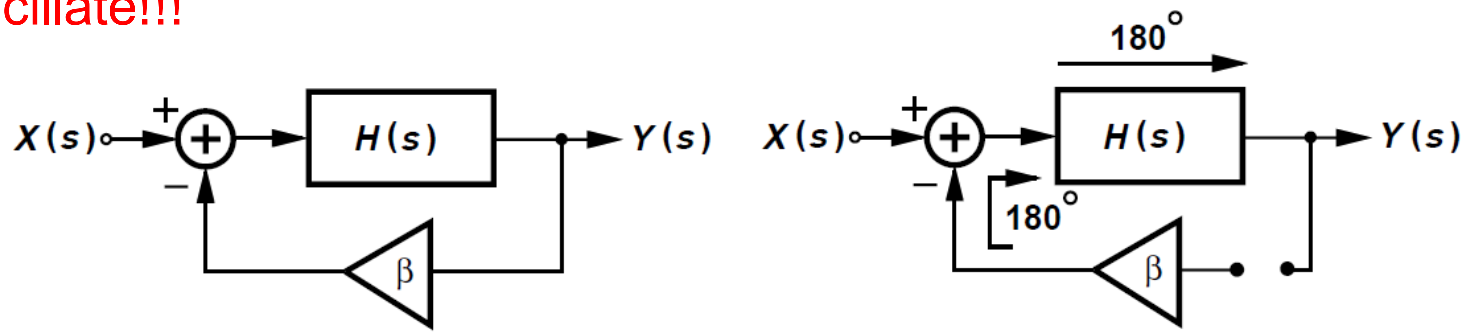


- Input Stage, Gain Stage, Output Stage

\+ Bias Circuit, Frequency Compensation

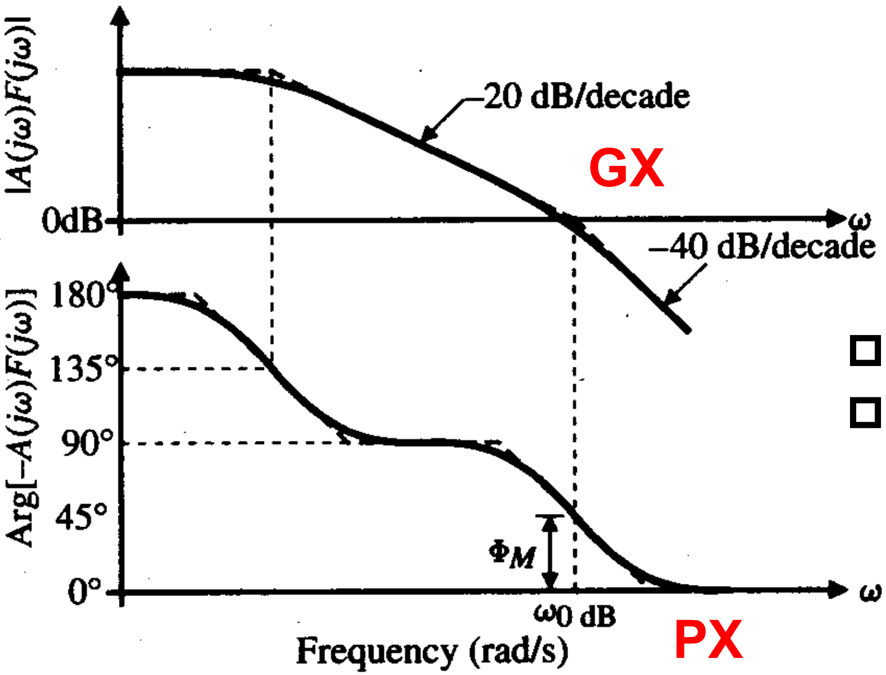
General Considerations of Stability

- Feedback systems suffer from potential instability and they may oscillate!!!



- Closed-loop transfer function: $\dfrac{Y(s)}{X(s)} = \dfrac{H(s)}{1+\beta H(s)}$
- When $\beta H(s) = -1$, the closed-loop "gain" goes to infinity -> oscillate
- **Barkhausen's Criteria**: $$\left|\beta H(j\omega_1)\right| = 1$$ $$\angle \beta H(j\omega_1) = -180^\circ$$
- **Negative feedback itself provides 180 phase shift**
- Loop transmission determines the stability issue

Review: Bode approximation

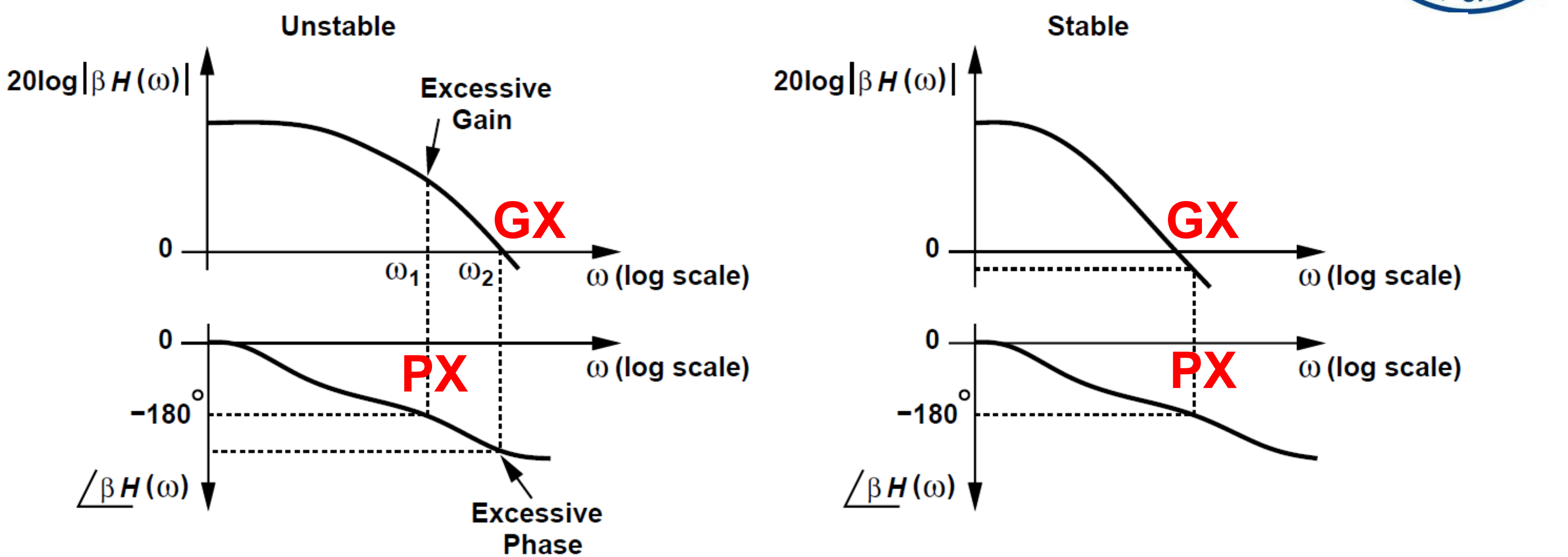


- GX (Gain Crossover Point): |gain|=1
- PX (Phase Crossover Point): phase= –180 °

- The slope of the magnitude at zero frequency: +20dB/dec

  at pole frequency: -20dB/dec.
- Zero 0.1ω: begin to change, ω: +45° , 10ω: +90°
- Pole 0.1ω: begin to change, ω: -45° , 10ω: -90°
- **The key point is that phase changes faster than magnitude.**
- The phase is much more significantly affected by high-frequency poles and zeros than the magnitude is .

System with bode plots of loop transmission: unstable vs. stable



- Phase shift changes the negative feedback to positive

  Oscillate: when phase=– 180° , gain>1

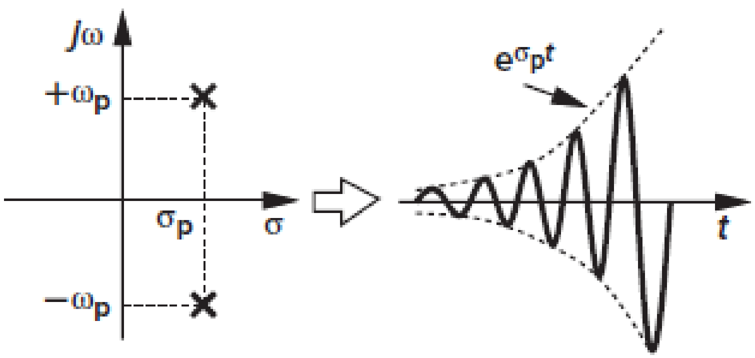
  Stable: when gain=1, phase<– 180°

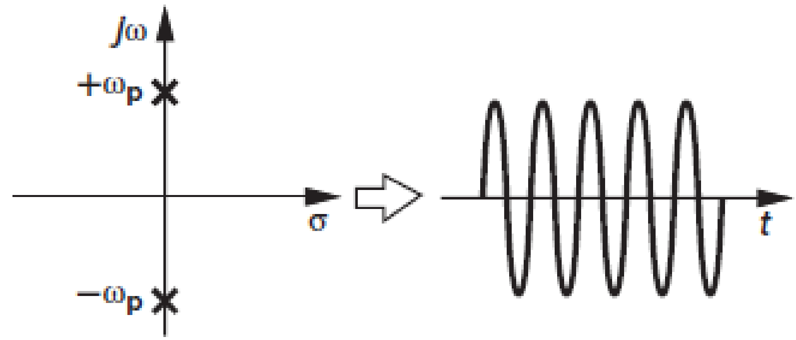
- In a stable system, PX must be behind GX **(GX<PX),** and GX is equal to unity-gain bandwidth in the open-loop system

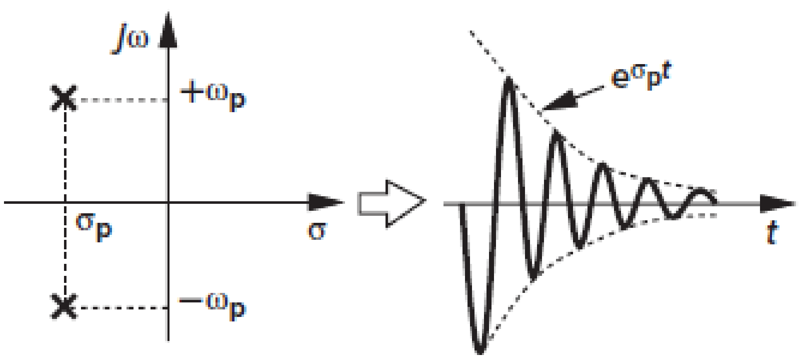
Phase Margin

$$\boxed{PM = 180^\circ + \angle \beta H\left(\omega = \omega_2\right)}$$

Location of the poles on a complex plane: Root Locus





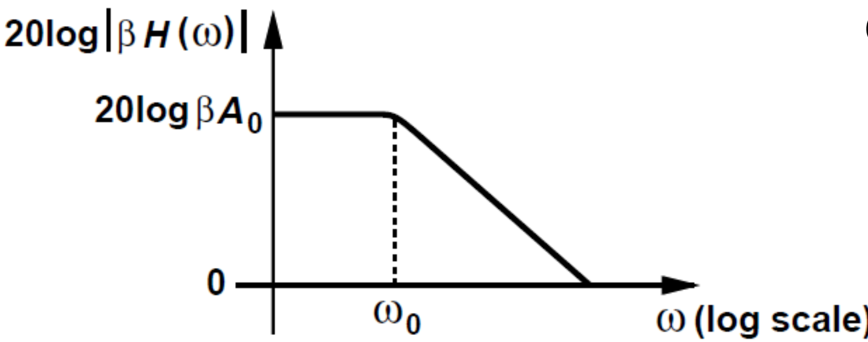


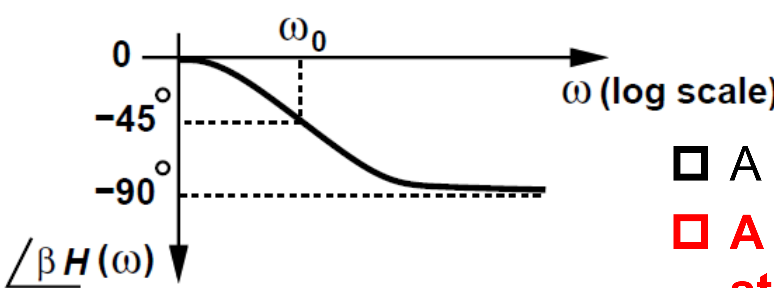
$$\beta H = \frac{1}{as^2 + bs + c},\ s = \sigma_p + j\omega_p$$

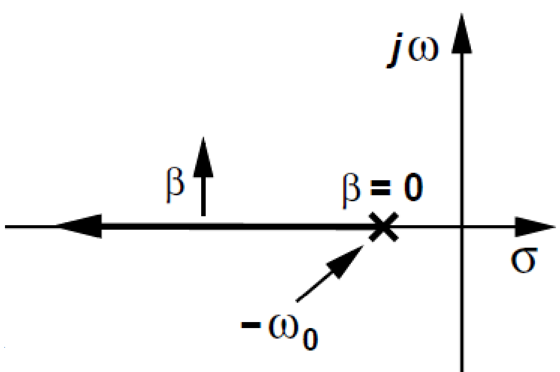
a term of impulse response:

$$\exp\left(\sigma_p + j\omega_p\right)$$

One-Pole System







Open loop: $H(s) = \dfrac{A_0}{1 + s/\omega_0}$

Close loop: $$\frac{Y(s)}{X(s)} = \frac{\dfrac{A_0}{1+\beta A_0}}{1 + \dfrac{s}{\omega_0(1+\beta A_0)}}$$

- A phase shift less than 90 °
- **A one-pole system is unconditionally stable**

- A real-valued pole in the **left half plane**
- Pole moves away from the origin as the loop gain β increases

Two-pole Systems

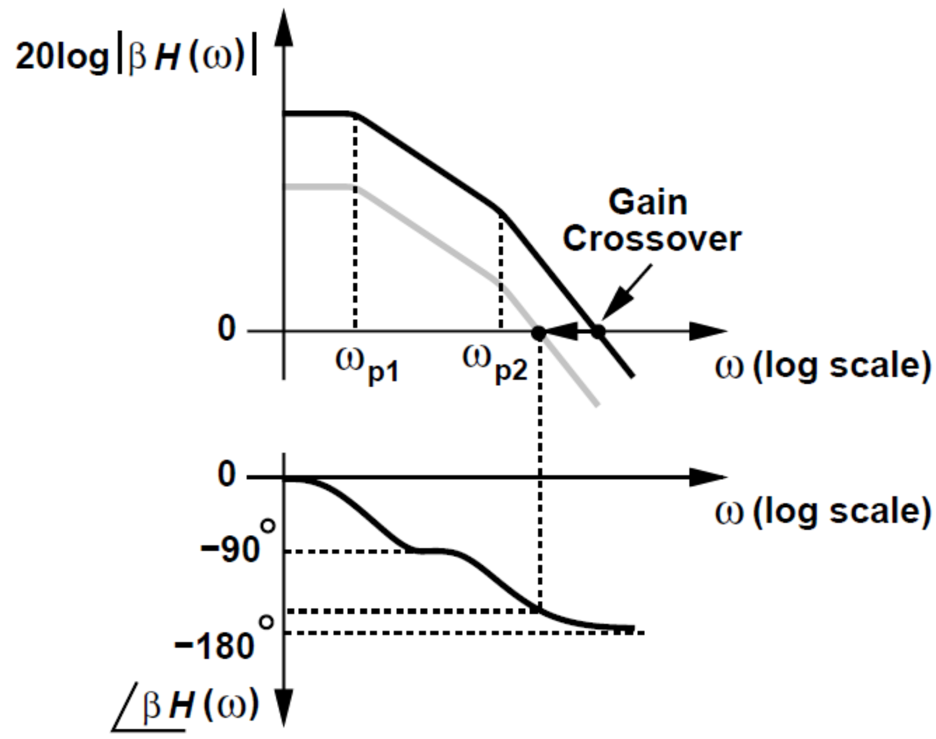
$$\omega = \omega_{p1}, \angle\beta H = -45^\circ$$

$$\omega = 10\omega_{p1}, \angle\beta H \Rightarrow -90^\circ$$

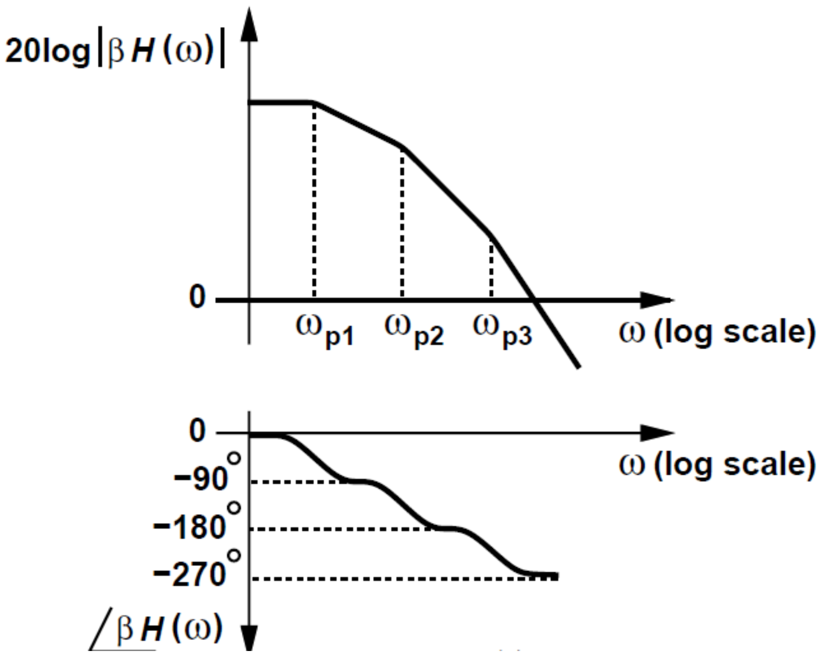
$$\omega = \omega_{p2}, \angle\beta H = - - 135^\circ$$

$$\omega = 10\omega_{p2}, \angle\beta H \Rightarrow -180^\circ$$

- Stable: PX> -180 ° @GX



Three-Pole Systems



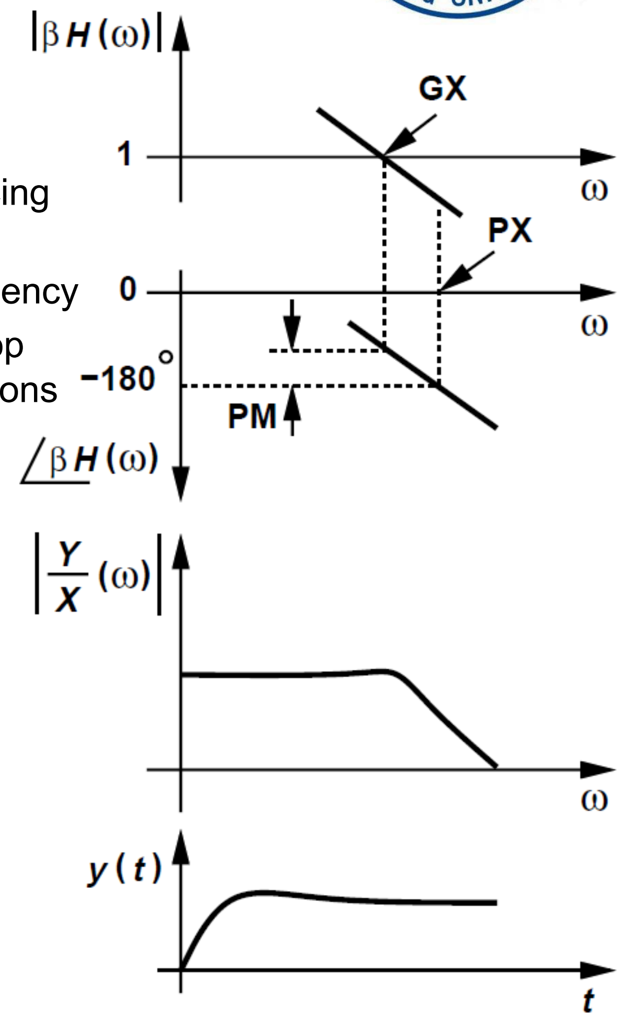
- ω_{p3}: additional phase shift
  decreases the magnitude of the loop gain at a greater rate
  => GX does not move as much as PX
  => additional poles/zeros affect the phase gristlier than they do the magnitude

Phase margin (PM)

◻ How far should PX be from GX?

$$PM = 180^\circ + \angle \beta H\left(\omega = \omega_1 @GX\right)$$

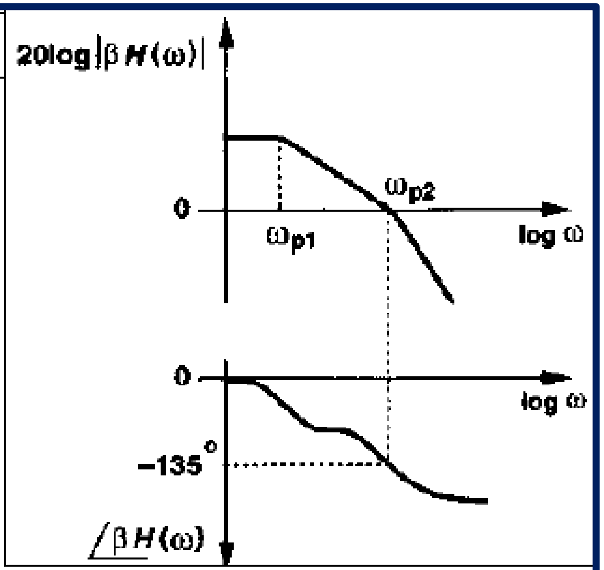
- ◻ A “well-behaved” closed-loop response concludes a greater spacing between GX and PX
- ◻ The **unity-gain bandwidth** cannot exceed the second pole frequency
- ◻ For large-signal application, time-domain simulation of closed-loop system **more relevant** and useful than small-signal as computations



For 2-pole system

$$\left|\beta H\left(\omega_{p2}\right)\right| = 1$$

$$PM = ?$$



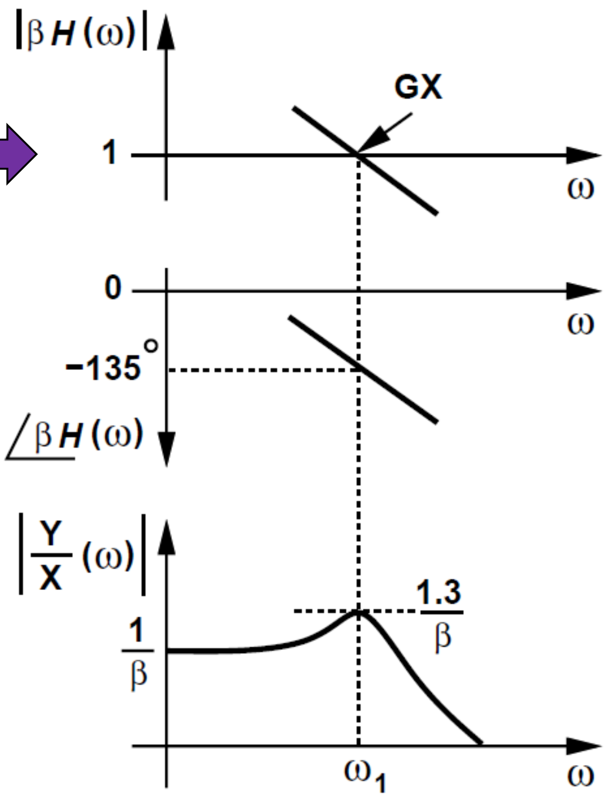
Phase Margin and step response of closed loop

PM=45°

$$\frac{Y}{X}(j\omega_1)=\frac{H(j\omega_1)}{1+1\times\exp(-135^\circ)}=\frac{H(j\omega_1)}{0.29-0.71j}=\frac{1.3}{\beta}$$

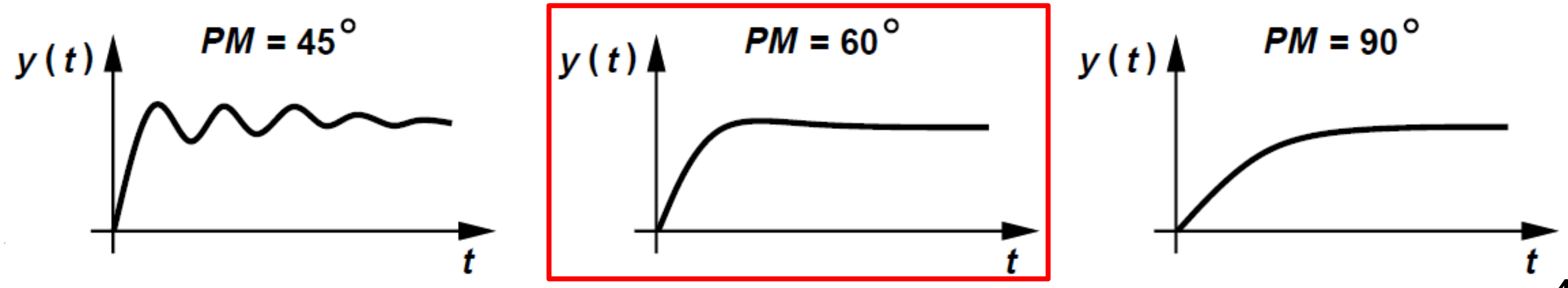
$$\left|\frac{Y}{X}\right|(\omega=\omega_1)=\frac{1}{\beta}\frac{1}{|0.29-0.71j|}=\frac{1.3}{\beta}$$

-- The frequency response of the feedback system suffers from a 30% peak at $\omega=\omega_1$



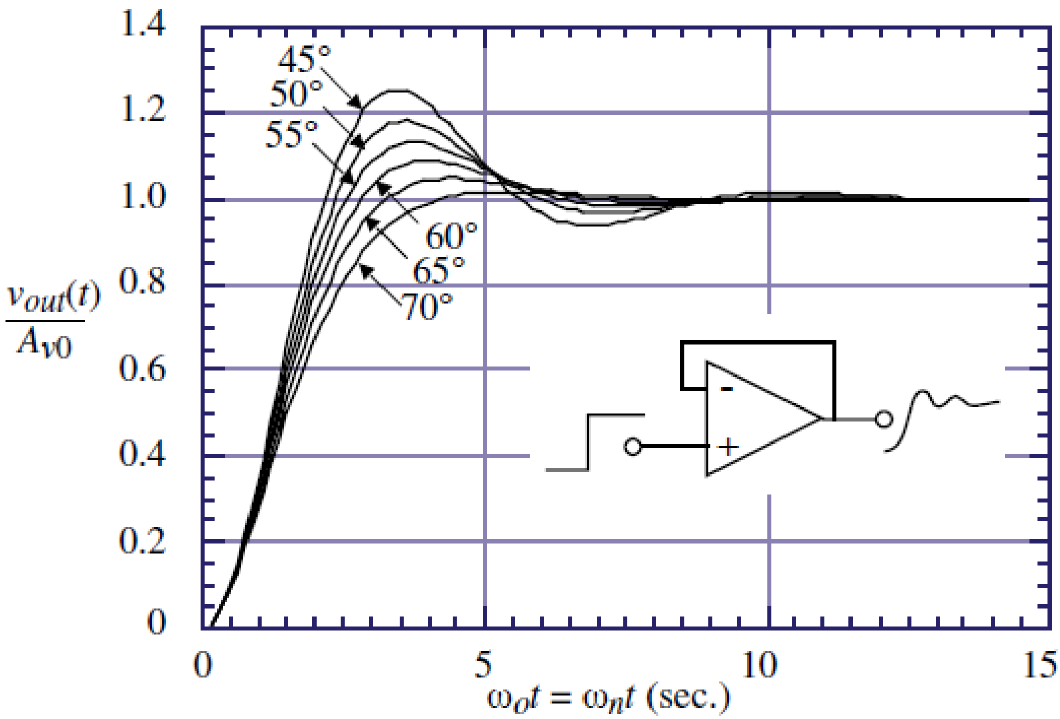
PM=60° $\left|\frac{Y}{X}\right|=\frac{1}{\beta}$

Trade-off



Phase Margin and step response of closed loop

- For less PM, exhibits more ringing
- For greater PM, the system is more stable, **but the time response slows down**
- Generally, PM>45 ° and the optimum value: PM=60 °



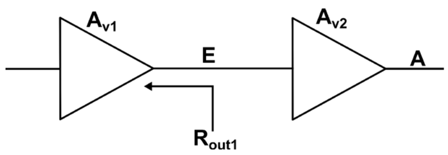
Trade off

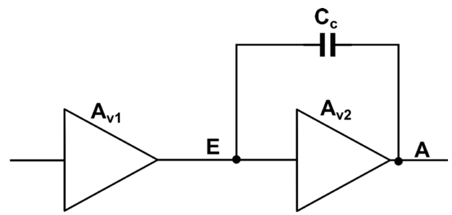
Outline

- General Consideration
- One-Stage Op Amps
- Two-Stage Op Amps
- Compensation of 2-Stage Op Amps
  - -> Control Theory
  - -> Miller compensation
- Other Issues of Op Amps

Compensation of 2-stage Op Amps

-- Miller Compensation





Stage 1: High output impedance

Stage 2: A moderate gain

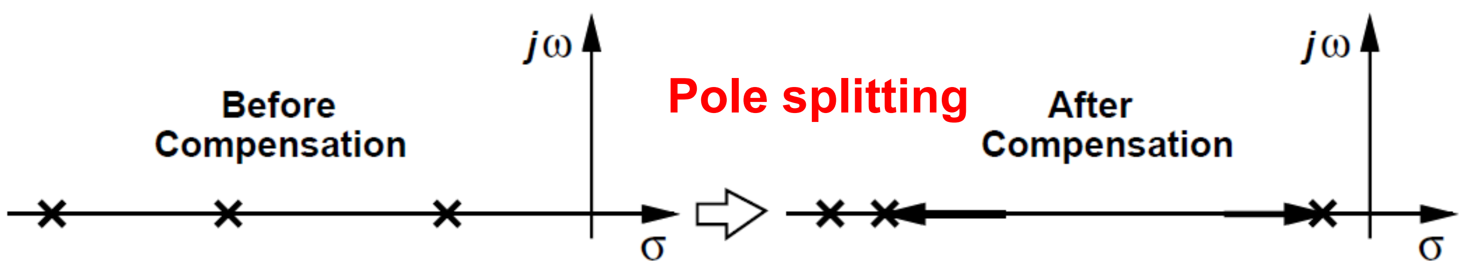
- **dominating pole: a large C at node E** $C_{eq} = C_E + \left(1 + A_{v2}\right) C_C$

$\Rightarrow$ a low frequency pole with a moderate capacitor

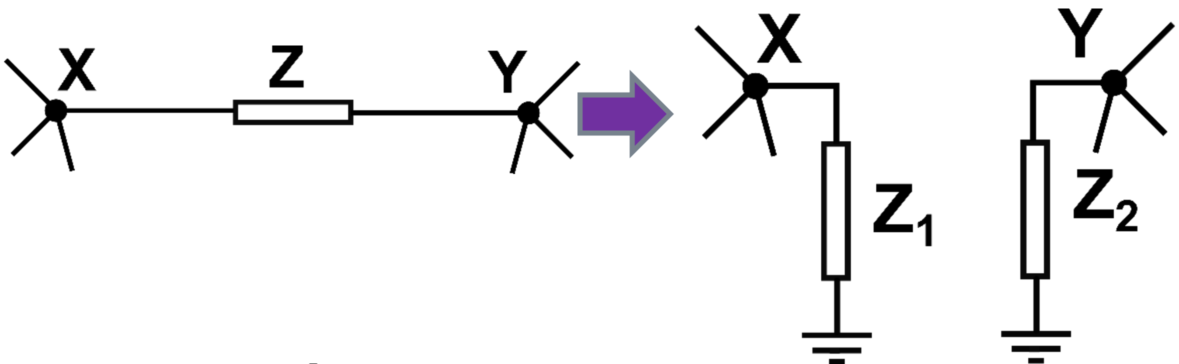
Miller Compensation !

$$f_{pE} = \frac{1}{2\pi R_{out1}\left[C_E + \left(1 + A_{v2}\right) C_C\right]} \approx \frac{1}{2\pi R_{out1} A_{v2} C_C}$$

$\Rightarrow$ move the output pole away from the origin

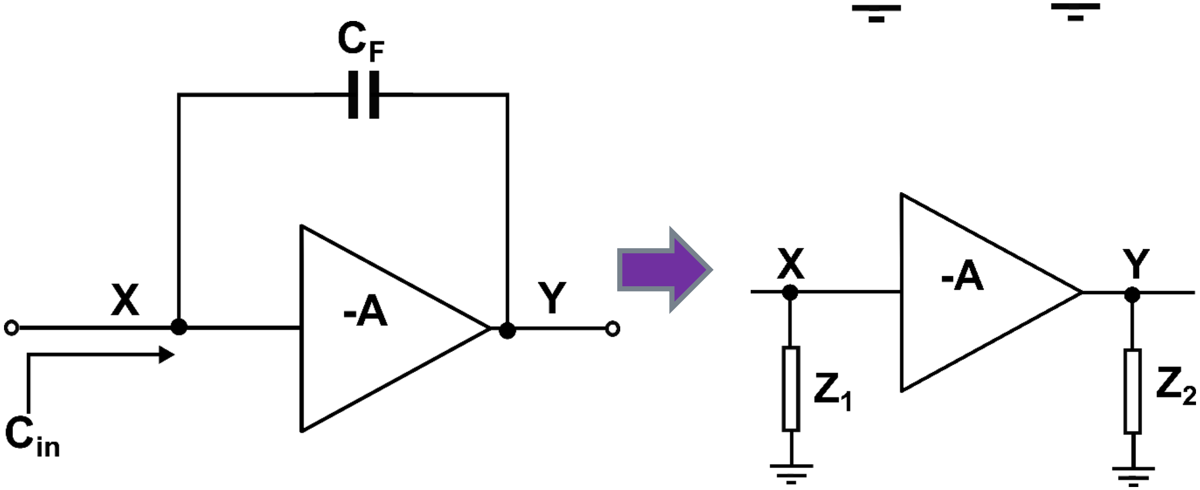


Miller Theorem



$$Z_1 = \frac{Z}{1 - \frac{V_Y}{V_X}} = \frac{Z}{1 - A_v}$$

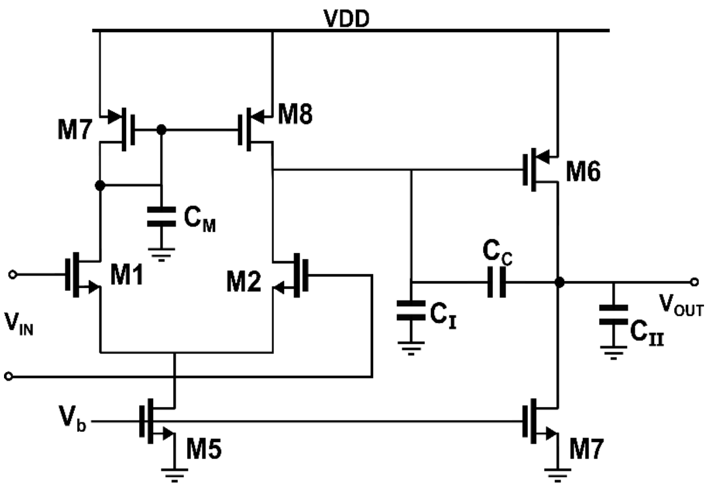
$$Z_2 = \frac{Z}{1 - \frac{V_Y}{V_X}} = \frac{Z}{1 - \left(A_v\right)^{-1}}$$

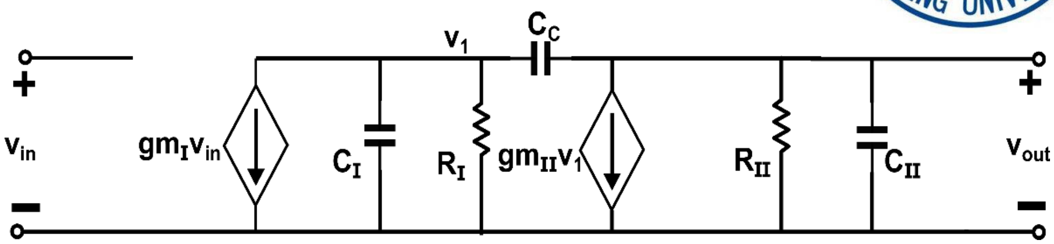


$$C_{in} = C_F\left(1 + A\right)$$

$$C_{out} = C_F\left(1 + A^{-1}\right)$$

2-stage Op Amps with Cc





$g_{mI} = g_{m1} = g_{m2}$, $R_I = r_{ds2} || r_{ds4}$, $C_I = C_1$

$g_{mII} = g_{m6}$, $R_{II} = r_{ds6} || r_{ds7}$, $C_{II} = C_2 = C_L$

C_c = accomplishes the Miller compensation

C_M = capacitance associated with the first-stage mirror (mirror pole)

C_I = output capacitance to ground of the first-stage

C_{II} = output capacitance to ground of the second-stage

$$-g_{mI}V_{in} = [G_I + s(C_I + C_c)]V_2 - [sC_c]V_{out}$$

$$0 = [g_{mII} - sC_c]V_2 + [G_{II} + sC_{II} + sC_c]V_{out}$$

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{g_{mI}(g_{mII} - sC_c)}{G_IG_{II} + s\,[G_{II}(C_I+C_{II}) + G_I(C_{II}+C_c) + g_{mII}C_c] + s^2[C_IC_{II} + C_cC_I + C_cC_{II}]}$$

$$= \frac{A_o[1 - s\,(C_c/g_{mII})]}{1 + s\,[R_I(C_I+C_{II}) + R_{II}(C_2+C_c) + g_{mII}R_IR_{II}C_c] + s^2[R_IR_{II}(C_IC_{II} + C_cC_I + C_cC_{II})]}$$

where, $A_o = g_{mI}g_{mII}R_IR_{II}$

2-stage Op Amps with Cc

In general, $D(s) = \left(1 - \frac{s}{p_1}\right)\left(1 - \frac{s}{p_2}\right) = 1 - s\left(\frac{1}{p_1} + \frac{1}{p_2}\right) + \frac{s^2}{p_1 p_2} \rightarrow D(s) \approx 1 - \frac{s}{p_1} + \frac{s^2}{p_1 p_2}$, if $|p_2| >> |p_1|$

$$\boxed{p_1 = \frac{-1}{R_I(C_I + C_{II}) + R_{II}(C_{II} + C_c) + g_{mII} R_I R_{II} C_c} \approx \frac{-1}{g_{mII} R_I R_{II} C_c}}$$

--Dominant left-half pole (the Miller pole)

--This root accomplishes the desired compensation

$$\boxed{p_2 = \frac{-[R_I(C_I + C_{II}) + R_{II}(C_{II} + C_c) + g_{mII} R_I R_{II} C_c]}{R_I R_{II}(C_I C_{II} + C_c C_I + C_c C_{II})} \approx \frac{-g_{mII} C_c}{C_I C_{II} + C_c C_I + C_c C_{II}} \approx \frac{-g_{mII}}{C_{II}}}$$

--Left-half plane output pole

--This pole must be ≥ unity-gain-bandwidth or PM will not be satisfied

$$\boxed{z = \frac{g_{mII}}{C_c}} \qquad (C_{II} > C_C >> C_I)$$

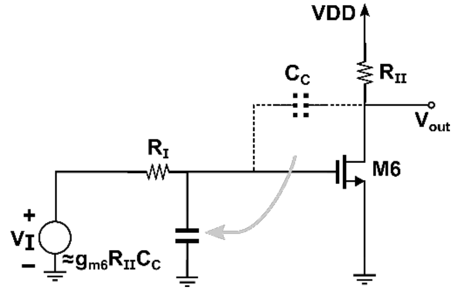
-- Right-half plane zero

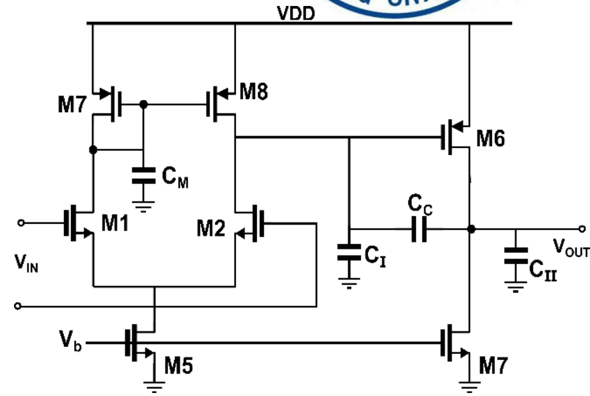
-- This root is very undesirable: it boosts the magnitude while decreasing the phase

Conceptually, where do these roots come from?

1) The Miller pole

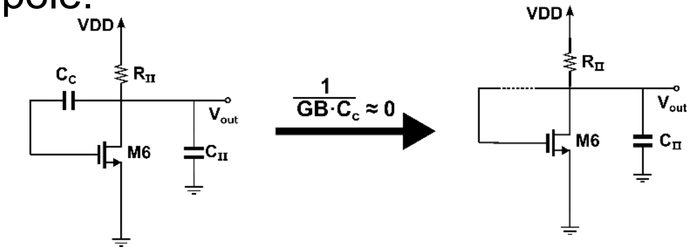
$$|p_1| \approx \frac{1}{R_{\mathrm{I}}\,(g_{m6} R_{\mathrm{II}} C_c)}$$





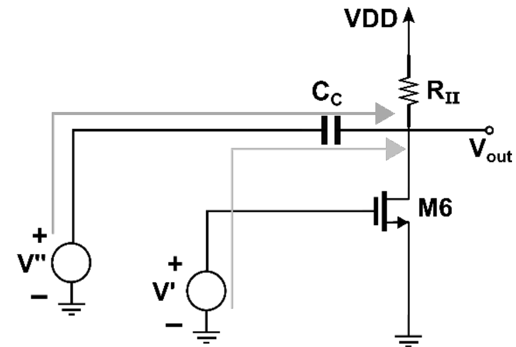
2) The left-half plane output pole:

$$|p_2| \approx \frac{g_{m6}}{C_{\mathrm{II}}}$$



3) Right-half plane zero (One source of zeros is from multiple paths from the input to output):

$$v_{out} = \left(\frac{-g_{m6} R_{\mathrm{II}} \left(\frac{1}{sC_C}\right)}{R_{\mathrm{II}} + \frac{1}{sC_C}}\right) \mathrm{V}' + \left(\frac{R_{\mathrm{II}}}{R_{\mathrm{II}} + \frac{1}{sC_C}}\right) \mathrm{V}'' = \frac{-R_{\mathrm{II}} \left(\frac{g_{m6}}{sC_C} - 1\right)}{R_{\mathrm{II}} + \frac{1}{sC_C}} \mathrm{V}$$



4) Mirror pole-zero $p_3 = -\left(\frac{g_{m3}}{C_3}\right)$ $z_3 = -\left(\frac{2g_{m3}}{C_3}\right)$

Outline

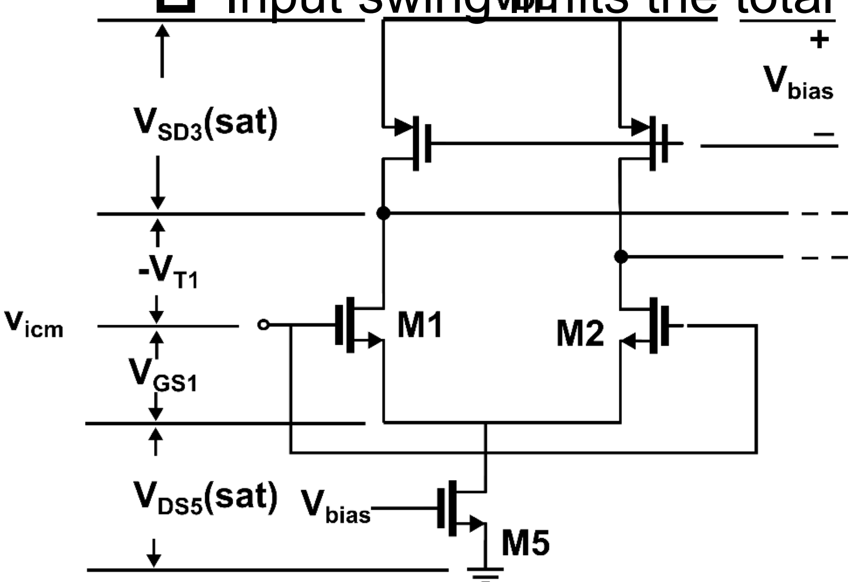
- General Consideration
- One-Stage Op Amps
- Two-Stage Op Amps
- Compensation of 2-Stage Op Amps
- Other Issues of Op Amps

Input Range Limitations

- **Input common-mode level** may need to vary over a wide range,

  e.g. ADC input comparator.

- Input swing limits the total range sometimes.



Assume V_{GS}≈0.9V, V_{DSsat}≈0.2V, VDD=1.5V

- Input common-mode range ICMR=0.9V

$$V_{icm}(upper) = V_{DD} - V_{SD3}(sat) + V_{T1} \qquad 2.0\text{V}$$

$$V_{icm}(lower) = V_{DS5}(sat) + V_{GS1} \qquad 1.1\text{V}$$

- Minimum power supply (*ICMR*=0)

$$V_{DD}(\min)$$

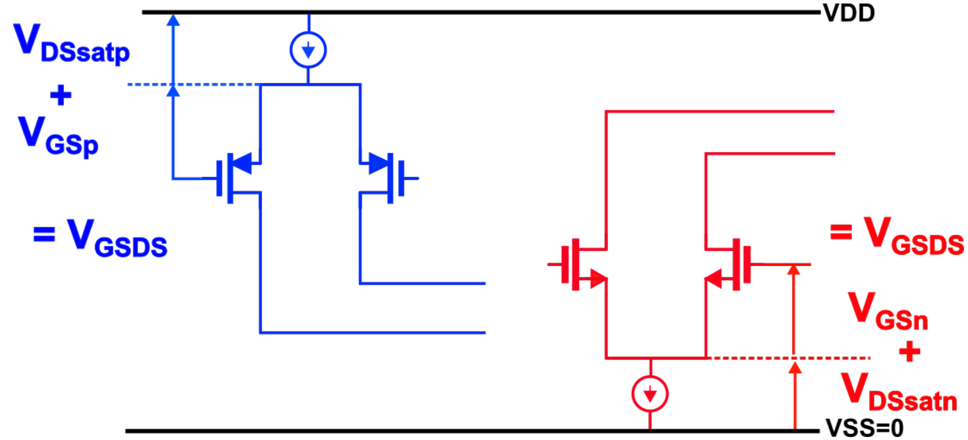
$$= V_{SD3}(sat) - V_{T1} + V_{GS1} + V_{DS5}(sat)$$

$$= V_{SD3}(sat) + V_{DS1}(sat) + V_{DS5}(sat) \qquad 0.6\text{V}$$

? Input pair: PMOS

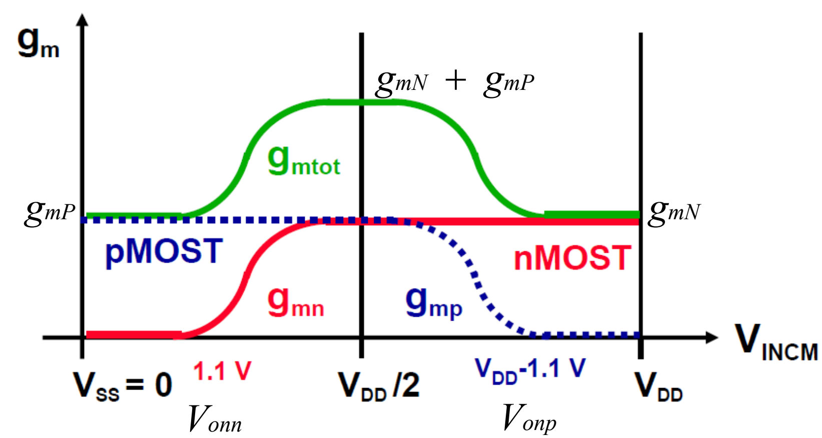
Input Range Limitations

- N-MOSTs differential pair
- P-MOSTs differential pair

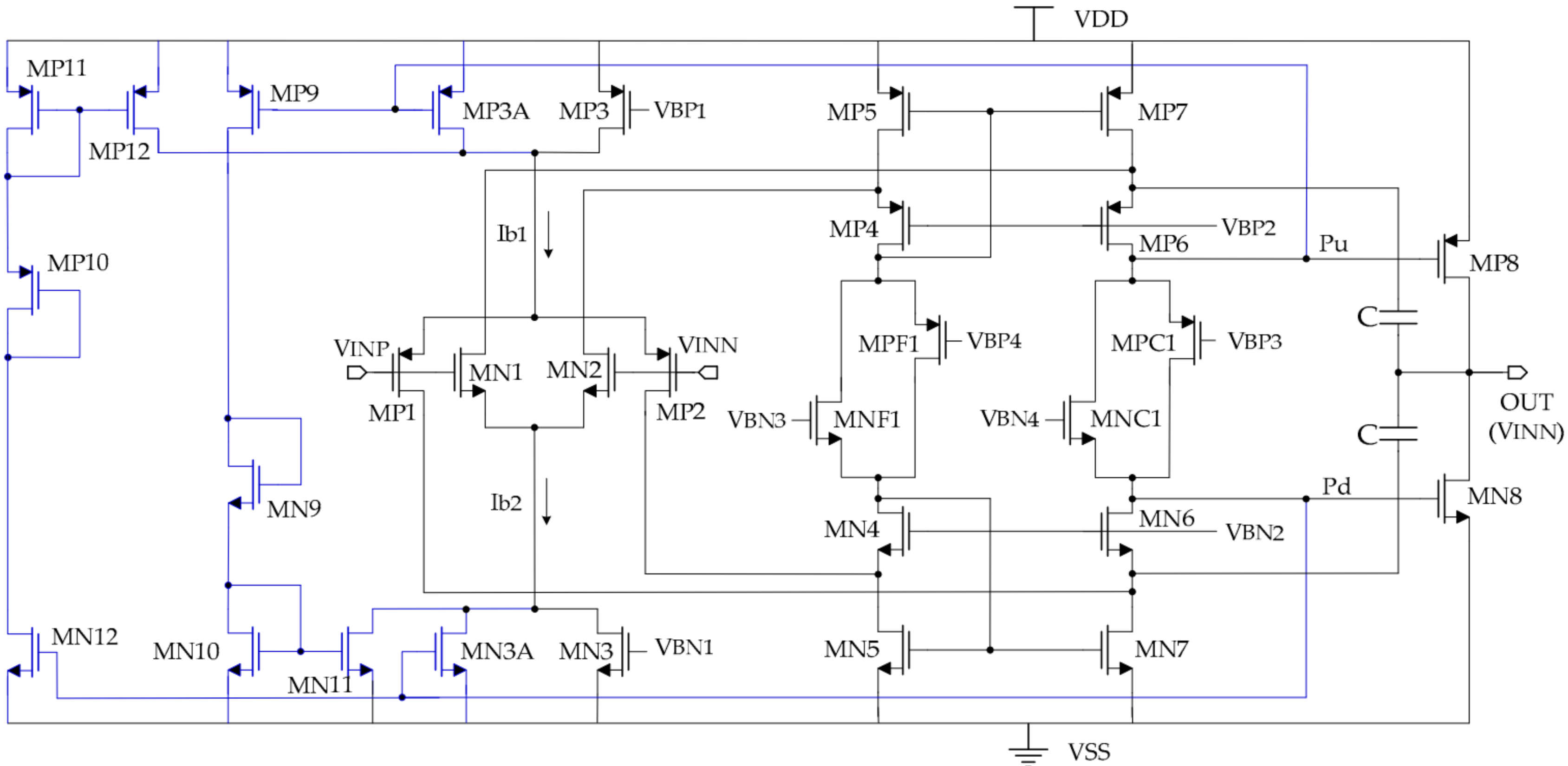


- ***How to extending the input CM range?***

-- Parallel Input Stage



Rail to rail Folded Cascode



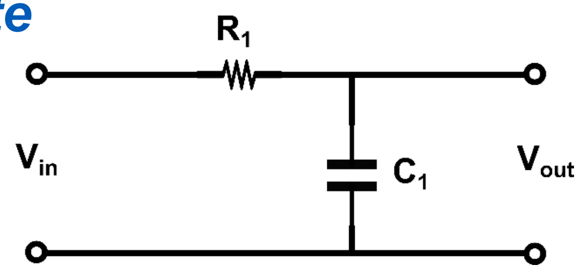
- Input Stage, Gain Stage, Output Stage

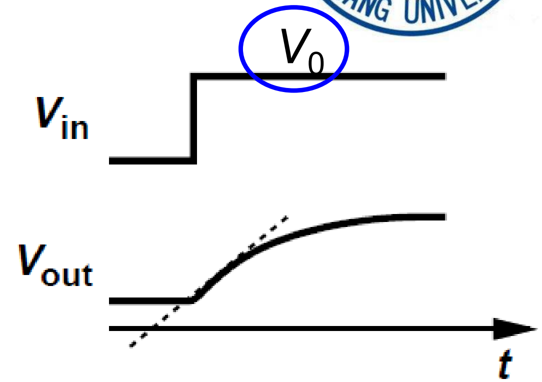
\+ Bias Circuit, Frequency Compensation

Slew Rate

Concept of Slew Rate

Linear circuit





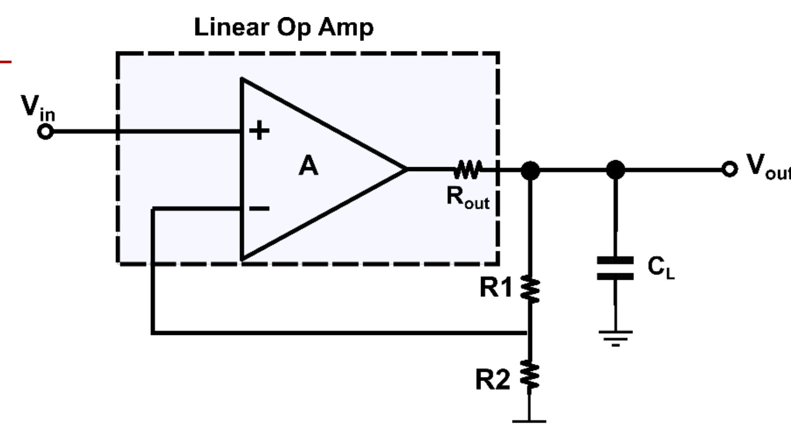
$$\frac{V_{out}}{V_{in}} = \frac{1/sC}{R + 1/sC} = \frac{1}{1 + sRC}$$

for an input step

$$V_{out} = V_0\left[1 - \exp\left((-t)/\tau\right)\right] \qquad \frac{dV_{out}}{dt} = \frac{V_0}{\tau}\exp\left(\frac{-t}{\tau}\right)$$

- the slope of the step response is proportional to the final output value V_0

Linear feedback system with op amp



$$\beta = \frac{R_2}{R_1 + R_2}$$

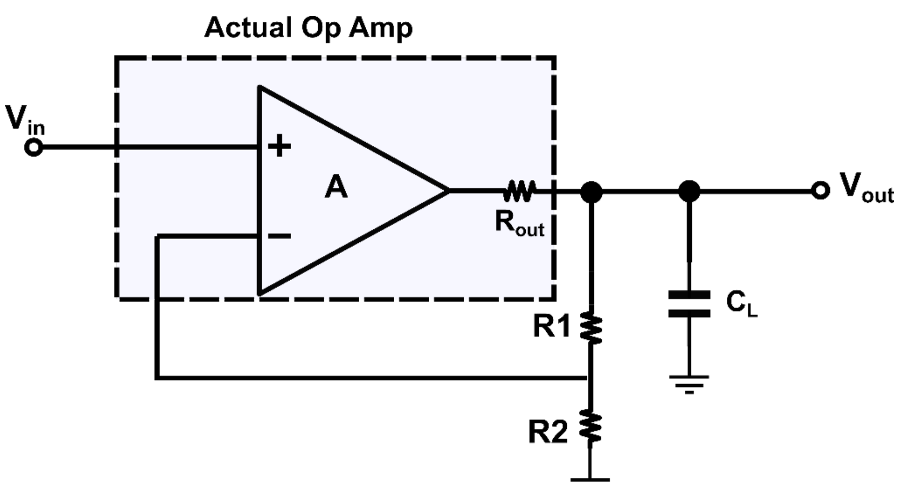
$$V_{out} = \frac{AV_0}{1 + A\beta}\left[1 - \exp\frac{-t}{C_L R_{out}/(1 + A\beta)}\right]u(t)$$

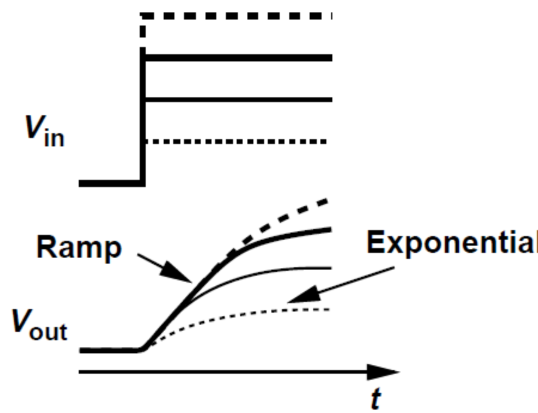
Linear feedback system with real op amp

- With large input steps, the output displays a linear ramp having a constant slope. The slope of ramp is the "**slew rate**".
- It seems that **the maximum current to charge** the load capacitance is limited.
- Nonlinear behaviors **reduce speed** and increase distortion.
- Increase SR would consume power and wider device

Trade off

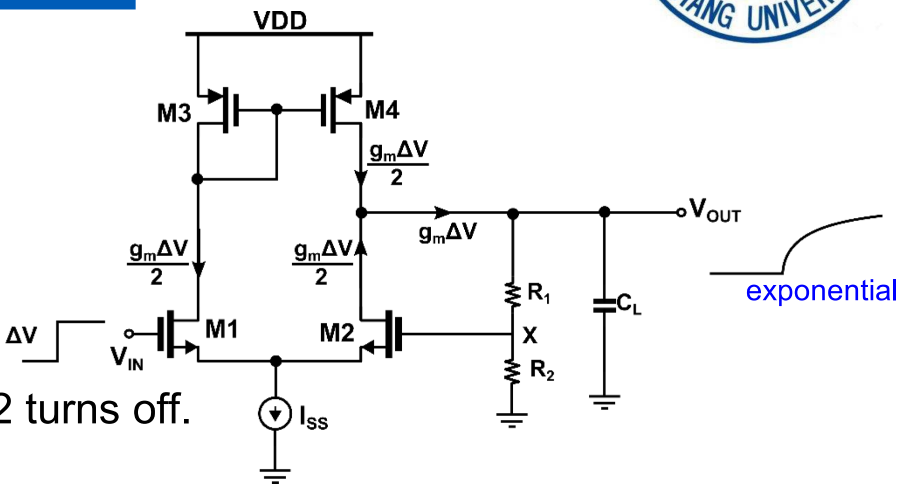
$$I = C_L \frac{dV_{out}}{dt} = \frac{AV_0}{R_{out}} \exp\left[\frac{-\left(1 + A\beta\right)t}{R_{out}C_L}\right]$$





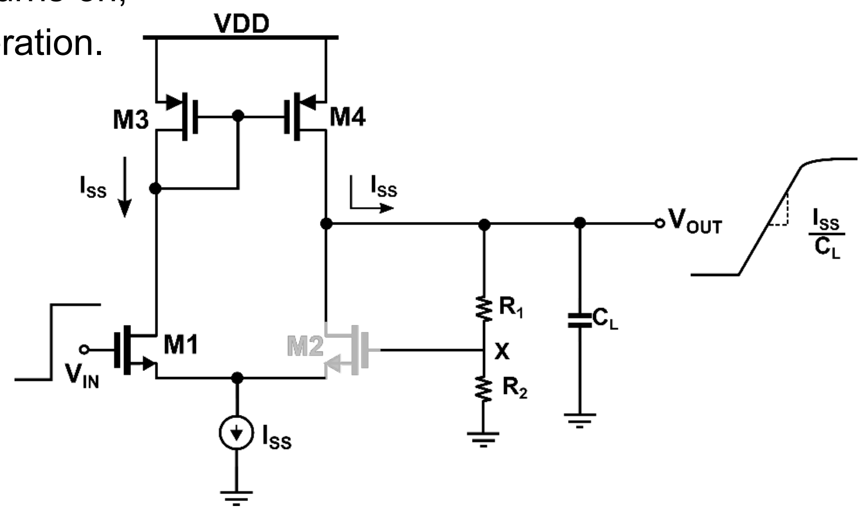
Slewing in op amp

- V_{in} : $\uparrow \Delta V$,
  - $V_{G1}\uparrow$: $I_{D1}\uparrow$ $g_m\Delta V/2$
  - $V_{G2}\downarrow$: $I_{D2}\downarrow$ $g_m\Delta V/2$
  - => the charging current to C_L:
  - $I = g_m\Delta V$



- When M1 experiences a large step, M2 turns off.
  - C_L: a constant current I $I_{SS} = g_m\Delta V$
  - Feedback is broken but after M2 turns on,
  - the circuit returns to a linear operation.
  - Slew rate:

$$\boxed{I_{SS}/C_L}$$

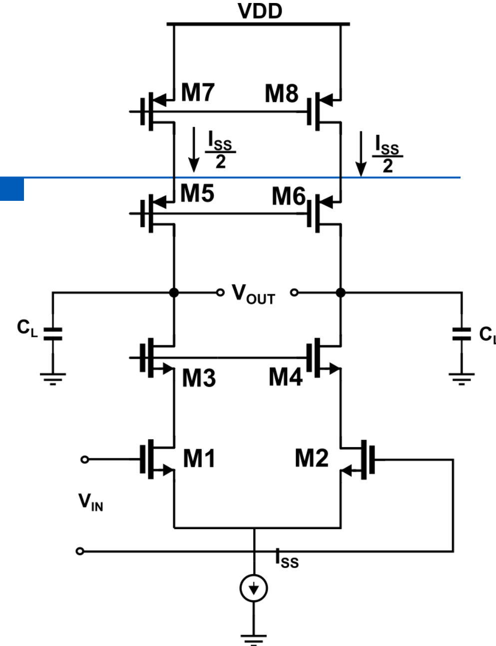


be independent of the input !!!

- $V_{in}\downarrow \Delta V$

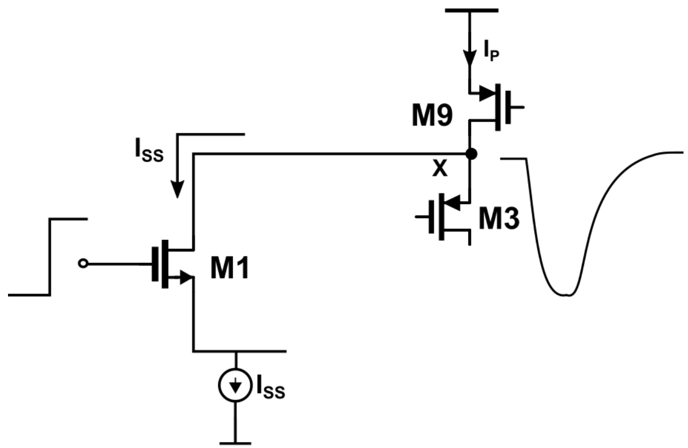
-- Slew rate: $\boxed{I_{SS}/C_L}$

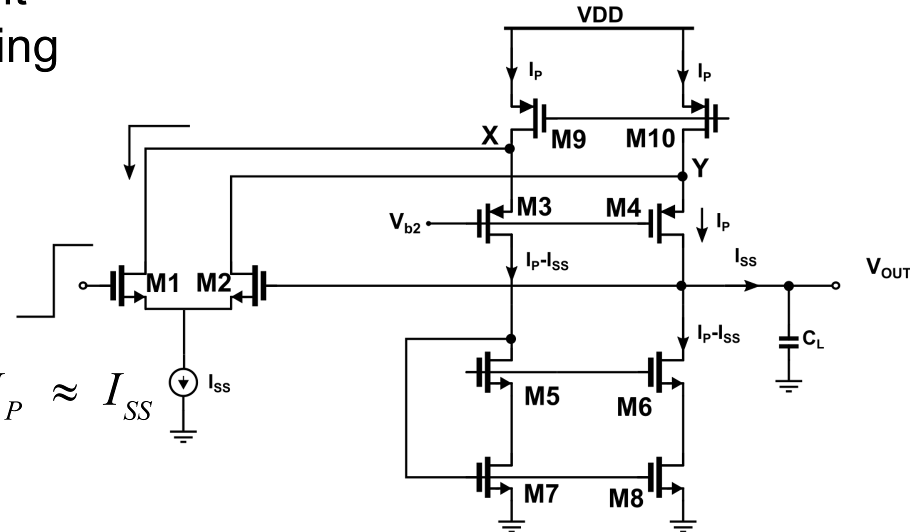
Slew Rate of Telescopic and Folded op amp



- **Telescopic op amp**
  - -- The ramp slope in each side: $\pm I_{SS}/(2C_L)$
  - -- The slew rate for $V_{out1} - V_{out2}$: I_{SS}/C_L

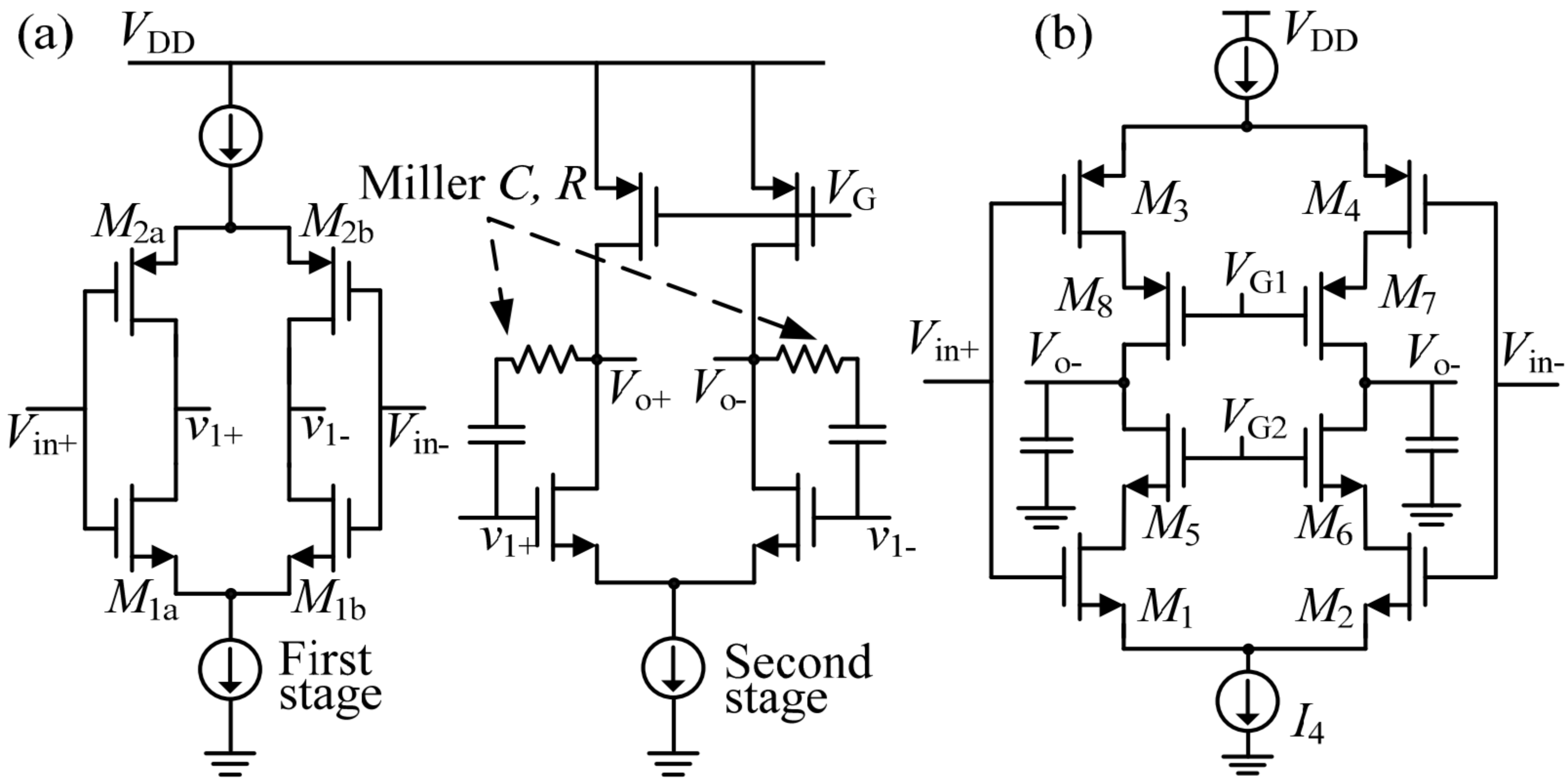
- **Folded op amp**
  - --if $I_P \geq I_{SS}$, slew rate: I_{SS}/C_L
  - --if $I_{SS} > I_P$, M3 turns off and tail current source enters the triode region. The settling time increases.





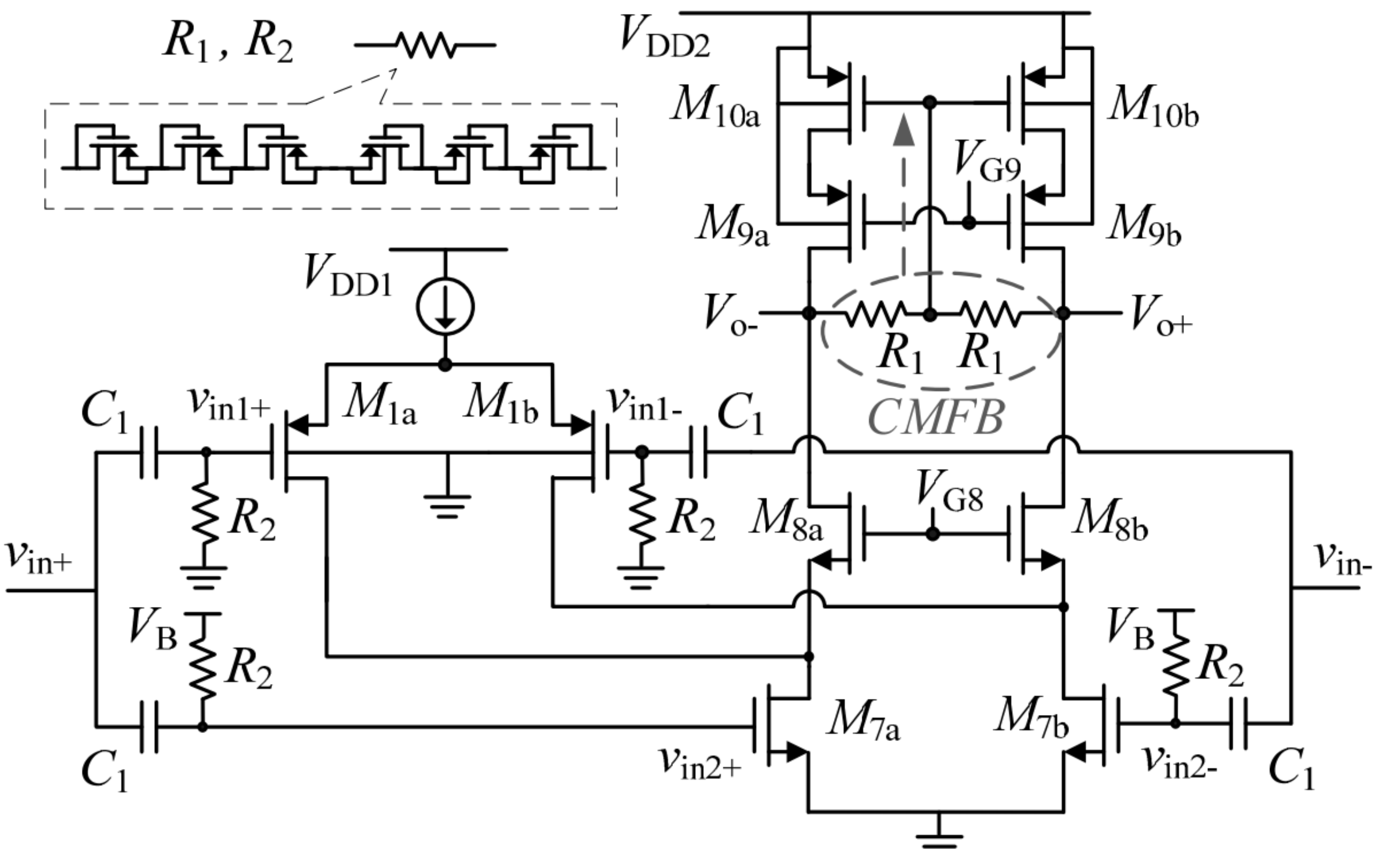
$I_P \approx I_{SS}$

Other examples (1)



- Current reuse: two stage and telescoppic

Other examples (2)



- Current reuse: folded cascode

Summary

- Ideal Opamp
- DC gain and dominant pole of single stage, telescopic and folded-cascade amplifier
- DC gain and two poles of two stage amplifier, after miller compensation
- Input and output range

  (everyone in saturation)
- Speed and Slew rate

  (small signal and large signal behavior)

集成电路原理与设计

10.运算放大器

宋爽

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