Exercise 8

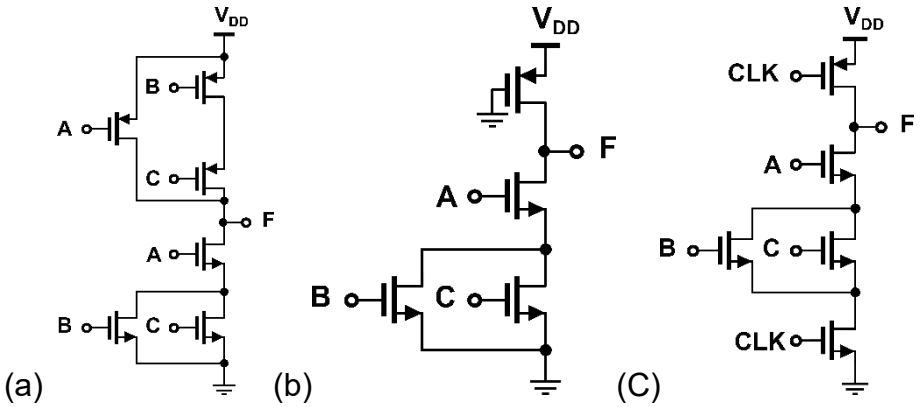
8-1 Sketch 3-input gates $F = (A \cdot (B + C))'$ using each of the following circuit techniques:

(a) Static CMOS.

(b) Pseudo-nMOS.

(c) Dynamic Gates.

Answer:



8-2 Consider the circuit of Fig 8.1.

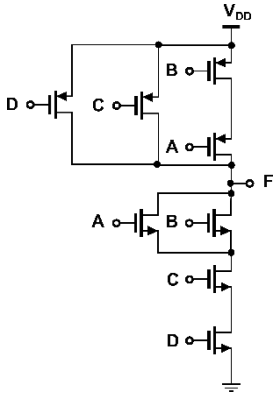


Fig.8.1

(a) What is the logic function implemented by the CMOS transistor network?

(b) What are the input patterns that give the worst case tpHL and tpLH. State clearly what are the initial input patterns and which input(s) has to make a transition in order to achieve this maximum propagation delay. Consider the effect of the capacitances at the internal nodes.

Answer:

(a) The logic function is : $F = \overline{(A + B)CD}$.

8-3 Implement the function $S = ABC + AB'C' + A'B'C + A'BC'$, which gives the sum of two inputs with a carry bit, using NMOS pass transistor logic.

Answer: