1.Moore's Law refers to Gordon Moore's perception that the number of _____ on a microchip ___ Every 18-24 month, though the cost of computers is halved. (B)

A. gates, triples B. transistors, doubles C. registers, doubles

2.With the development of CMOS IC technology, the feature size of MOS transistor becomes ___ and its intrinsic gain $g_m r_o$ becomes _____ (C)

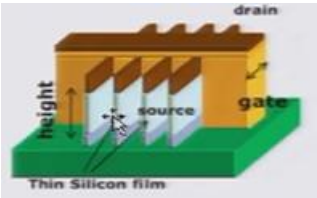
A. increasing, increasing B. unchanging, increasing C. decreasing, decreasing

3._____ IC design is mostly done at an abstracted level with HDL (Hardware Description Language), while _____ IC design generally involves more personalized focus into each transistor, determining the sizing of each. (C)

A. Analog, digital B. Analog, mixed signal C. Digital, analog

4.The type of transistors in the following figure is _____, which is invented for advanced technology node like 14nm CMOS. (C)

A. GAA B. Planar MOS C. FinFET



5._____ transfers the circuit layout information to the wafer. (A)

A. Photolithography B. Oxidation C.Etching

6.With "self-aligned" structure, the fabrication sequence of PMOS is _____ (A)

A. n-well, gate oxide and polysilicon, source/drain junctions;

B. n-well, source/drain junctions, gate oxide and polysilicon;

C. source/drain junctions, gate oxide and polysilicon, n-well.

7.Which is improper for the CMOS processing? (A)

A. Ion implantation does not damages the silicon lattice extensively and the operation of annealing is not needed;

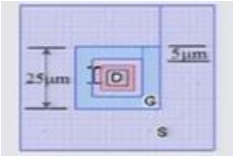
B. A self-aligned structure makes the source/drain regions the implanted at precisely the edges of the gate area;

C. Two types of photoresists are used in processing, as negative and positive.

8.Silicon dioxide can act as _____ in many steps of fabrication. Which one is not proper? (B)

A. the gate-oxide layer　B. photoresist　C. the field oxide(FOX)

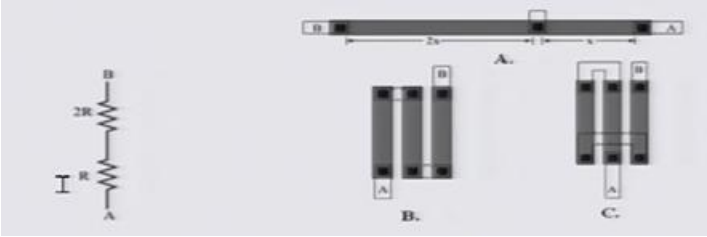
9.What is the W/L ratio of two NMOS transistors shown in the figure? (C)



A.　20/25　B. 15/5　C.60/5

10.A resistor divider in figure shows 3 different layouts. Which one is best for matching (C)

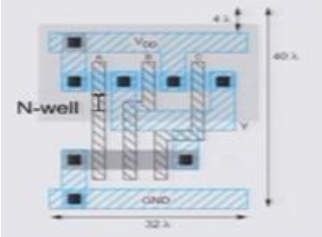
Give your reason: 1.单位管　2.对称性　（个人答案，仅供参考）



11.In the CMOS process of p-sub and N-well, all N-MOSFETs share the same substrate which is tied to _____? (B)

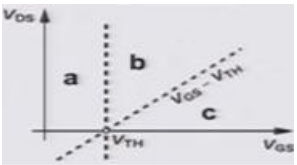
A. the most positive supply　B. ground　C. arbitrary potential

12.A layout of a logic gate is shown in the following figure. What logic does it represent? (B)



A.　Y=ABC　B. $Y=\overline{ABC}$　C. $\overline{A+B+C}$　画出来是上面 3 个 P 管并，下面 3 个 N 管串

13.In the following figure, the region “b” represents _____ regions. (B)



A. cut off　B. saturation　C.triode

So, for a MOSFET, the necessary condition to turn the MOSFET on is __Vds 大于等于 Vgs-Vth__. And the definition of the threshold voltage or its physical meaning is __书上原话反型层载流子浓度那句__.

14.Considering the channel length modulation effect, as Vds of a NMOS rising, the drain current of the transistor will _____, which means the drain current is not only controlled by the gate voltage, but also affected by the drain voltage. (A)

A. increase B. decrease C. fluctuate

Then the square law equations should be modified as __考虑沟道调制效应的那个平方公式（实际考试要把公式写出来，我这只是不想打公式了）_____.

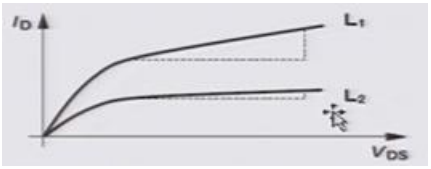
15.Assuming that a NMOS is in saturation region, which kind of expression cannot describe its transconductance g_m? (A)

A. 修改系数少了 2 B 和 C 都是原式。跨导公式背清楚即可

16. For NMOS, the threshold voltage will _____ when the bulk voltage drops. (B)

A. decrease B. increase C. remain constant

17.The figure shows the real I-V characteristics of two enhancement N-MOSFETs by real line respectively. Compare the corresponding channel length L_1 and L_2, which one is longer? (B)



A.L_1 B. L_2 C. L_1=L_2

18.Which is improper in the following statement? (B)

A. The analog design octagon presents the trade-off of the performance of the circuit;

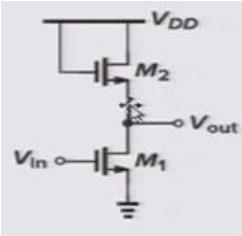
B. Mobility is not dependent on the temperature;

C. With the scaling of the channel length of MOS, it may result in the velocity saturation of carriers if the bias voltage is very high.

19.Please give the expression of Cgs and Cgd in the saturation region of a NMOS;

Cgs _____; and Cgd _____.(书上有对应公式)

20.(a)The main configuration of the following figure is _____(B)



A. common gate B. common source C. common drain

(b) Which is improper for schematic shown in Fig? (C)

A. M2, a diode-connected device, is always in saturation region;

B. If the body effect is neglected, the input-output characteristic is relatively linear;

C. With the increase of $(W/L)_1$ or $(W/L)_2$, the voltage gain would increase.

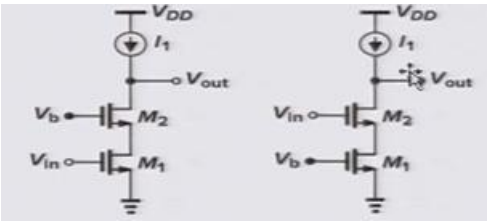
21. What is the characteristic of the source follower? (A)

A. voltage buffer B. high output resistance C. low input resistance

22.In application requiring a large voltage gain in a single stage amplifier, we can choose load. (C)

A. resistive B. diode-connected C. current-source

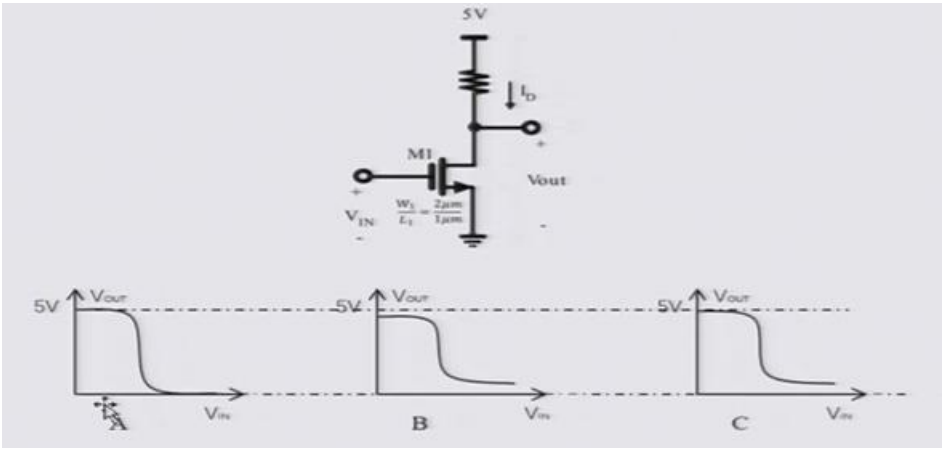
23.Compare the output resistance of the following figures, which one is larger? (C)



A. the left B. the right C. the same

24.Which one curve can sketch voltage transfer characteristic of the following figure. (C)

Give your reason:____书上对应知识点理解_____.


5V
I_D
M1
Vout
V_{IN}
$\frac{W_1}{L_1} = \frac{2\mu m}{1\mu m}$
5V
V_{OUT}
V_{in}
A
B
C