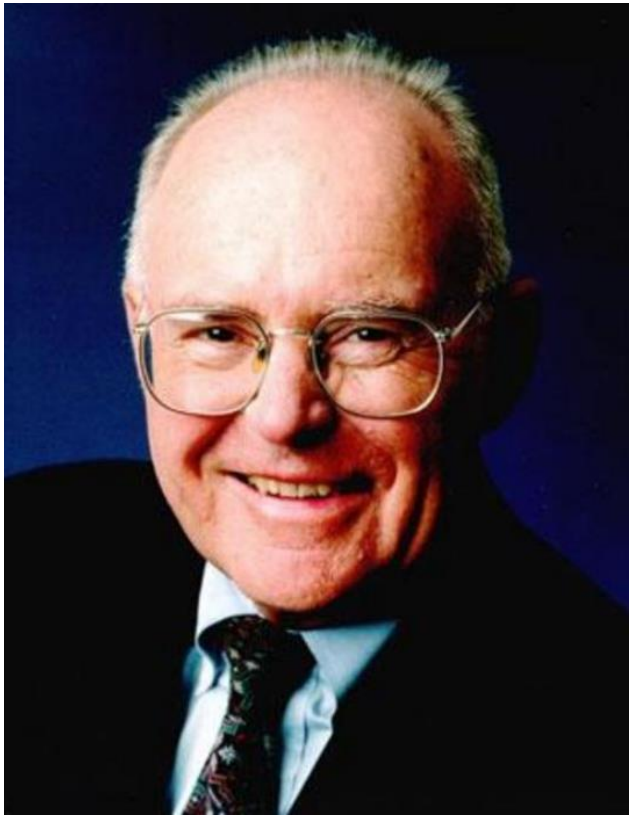
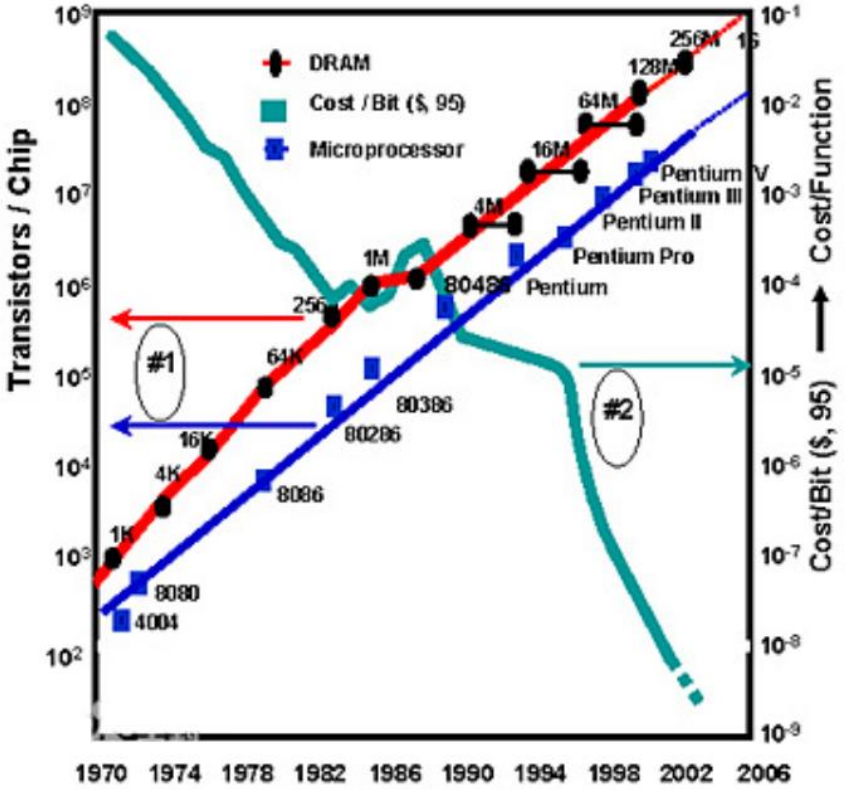
集成电路原理与设计
5.模拟基本单元

宋爽
shuangsonghz@zju.edu.cn

Commemorating Goldon Moore





1929.1.3~2023.3.24

Syllabus

课数	内容	课数	内容
1	导论	9	差分放大器
2	器件模型一	10	运算放大器
3	器件模型二	11	逻辑门
4	工艺流程	12	组合逻辑
5	模拟基本单元	13	时序逻辑
6	电流镜与基准	14	加法器/乘法器
7	单级放大器	15	集成电路专题讲座一
8	课堂测验	16	集成电路专题讲座二

Outline

- MOS Switch
- MOS Diode/Active Resistor
- Current Sinks and Sources

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- MOS Diode/Active Resistor
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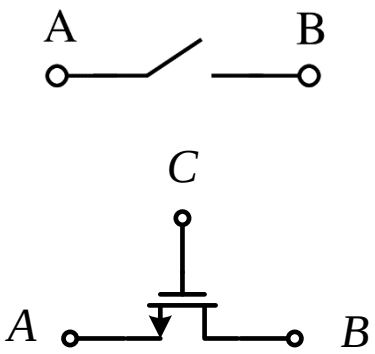
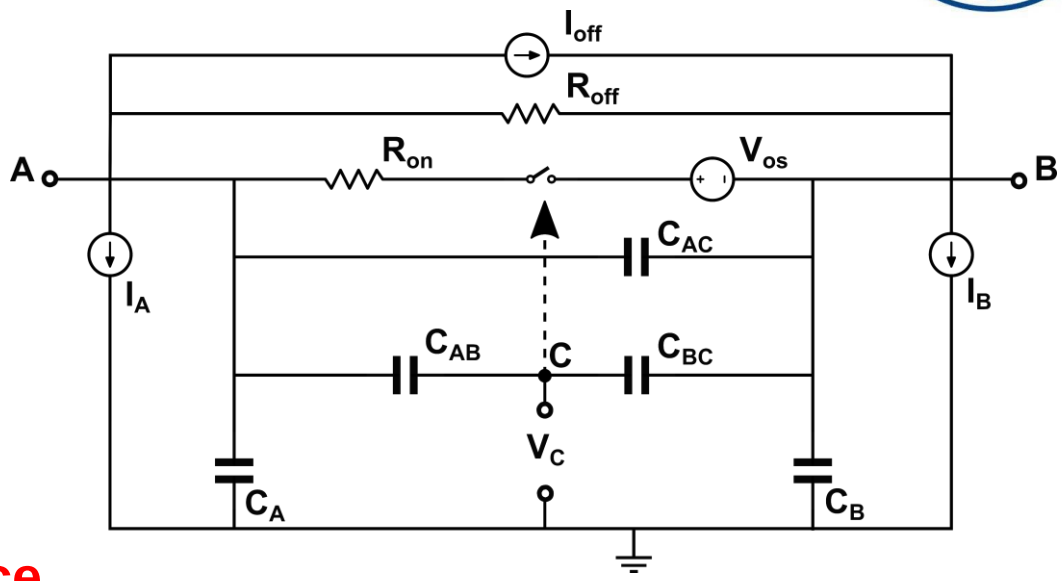
MOS Devices used as SWITCH





- r_{ON} **ON resistance**
- r_{OFF} **OFF resistance**
- V_{OS} Voltage offset
- I_{OFF} Leakage current
- I_A I_B Leakage current
- Parasitic capacitors …

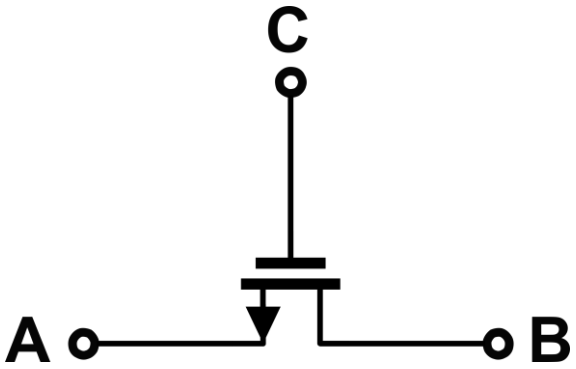
Some English:

Open vs. Closed
Switch off vs. Switched on

An N-Channel Transistor

ON State：

$$0 < V_{DS} \le V_{GS} - V_{TH}$$

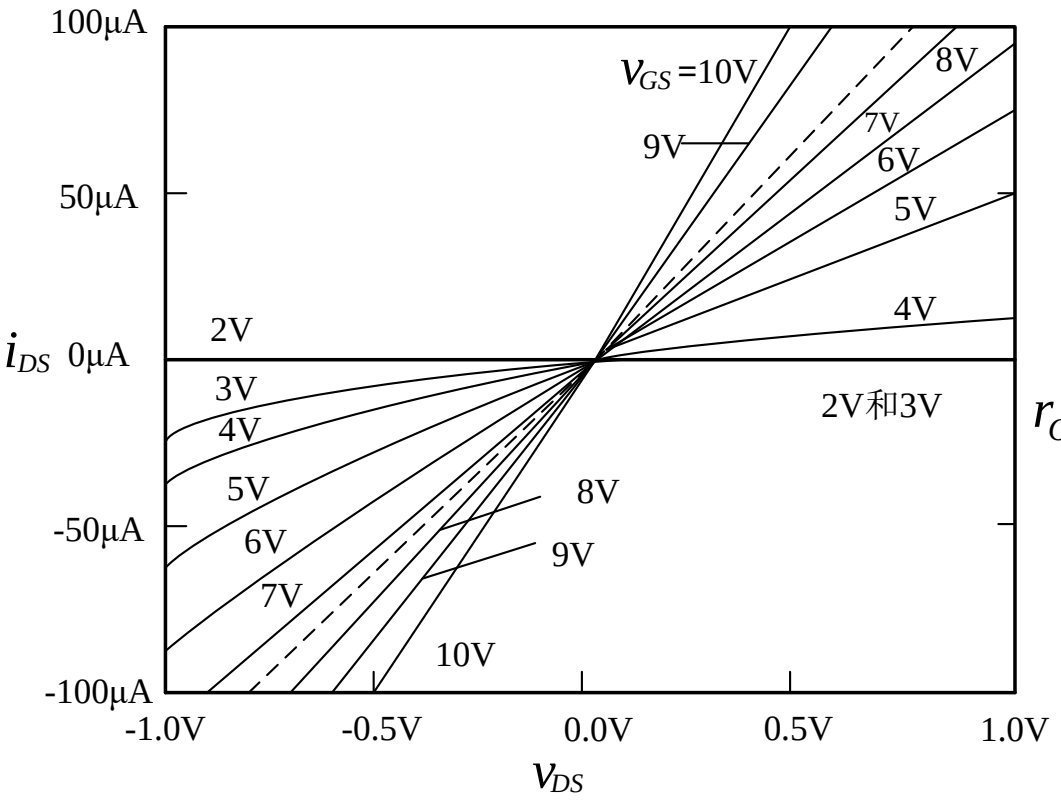


$$i_D = \frac{K'W}{L}\left[(v_{GS} - V_{TH})v_{DS} - \frac{v_{DS}^2}{2}\right]$$

$$r_{ON} = \left.\frac{1}{\partial i_D / \partial v_{DS}}\right|_Q = \frac{L}{K'W(V_{GS} - V_{TH} - V_{DS})}$$

(1) How to get r_{ON} with good linearity?
(2) How to get a smaller r_{ON}?

I-V characteristic of an NMOS operating as a switch



$$i_D = \frac{K'W}{L}\left[\left(v_{GS} - V_T\right)v_{DS} - \frac{v^2_{DS}}{2}\right]$$

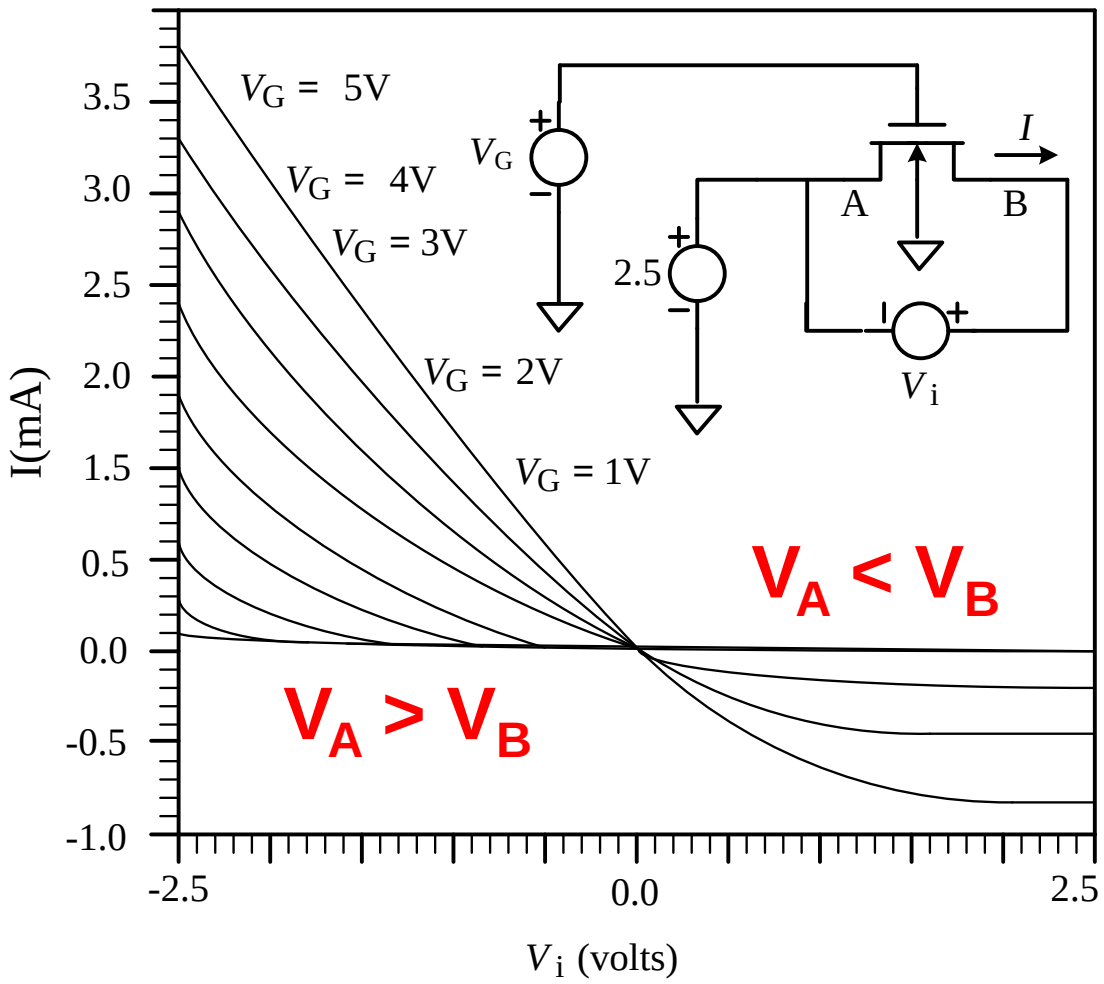
$$r_{ON} = \left.\frac{1}{\partial i_D / \partial v_{DS}}\right|_Q = \frac{L}{K'W\left(V_{GS} - V_{TH} - V_{DS}\right)}$$

$$\begin{pmatrix} v_{DS} \approx 0 \\ i_D \cong \dfrac{K'W}{L}\left(v_{GS} - V_T\right)v_{DS} \end{pmatrix}$$

↑ *V*gs

↑ *W*/*L*

I-V Characteristic of an NMOS Operating as a Switch



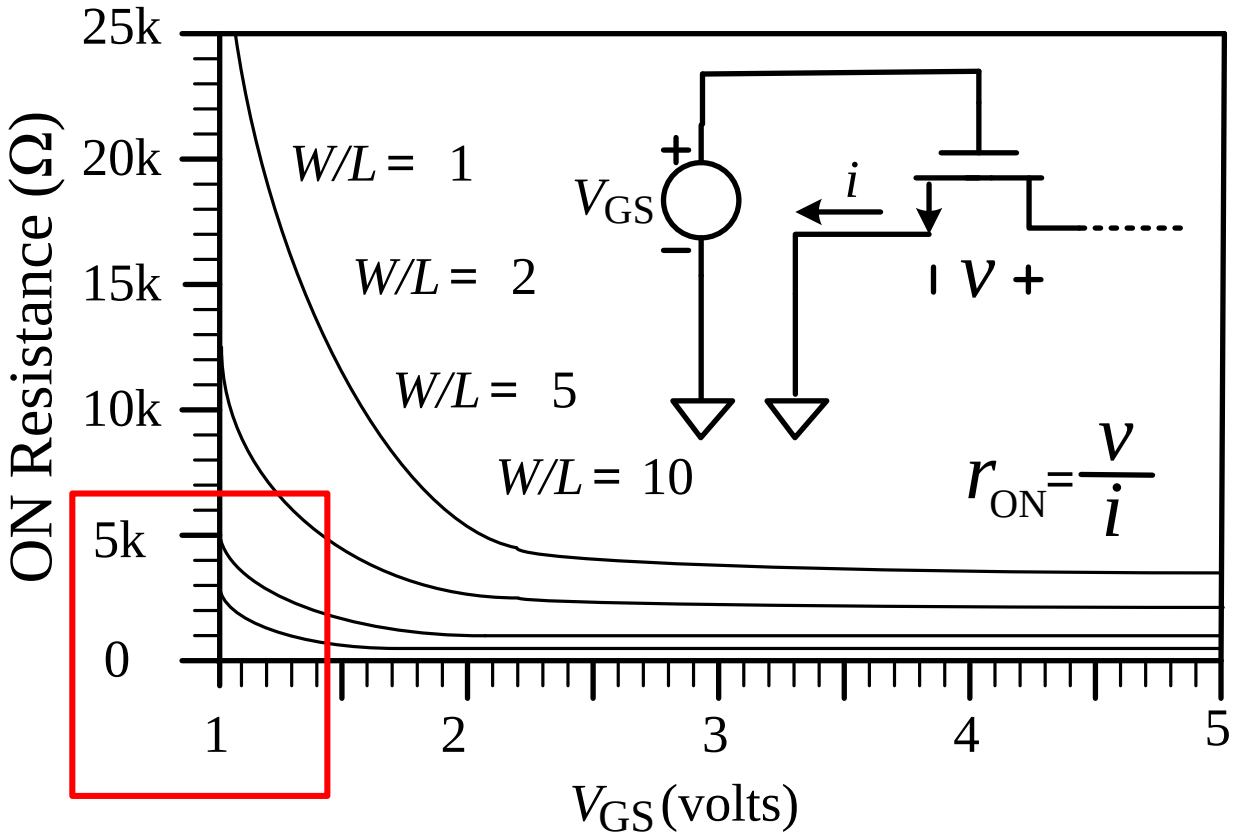
$$r_{ON} = \left.\frac{1}{\partial i_D / \partial v_{DS}}\right|_Q$$

$$= \frac{L}{K'W\left(V_{GS} - V_{TH} - V_{DS}\right)}$$

Source is A or B?

Why they are different?

ON Resistance: R_{ON}



$$r_{ON} = \left.\frac{1}{\partial i_D / \partial v_{DS}}\right|_Q$$

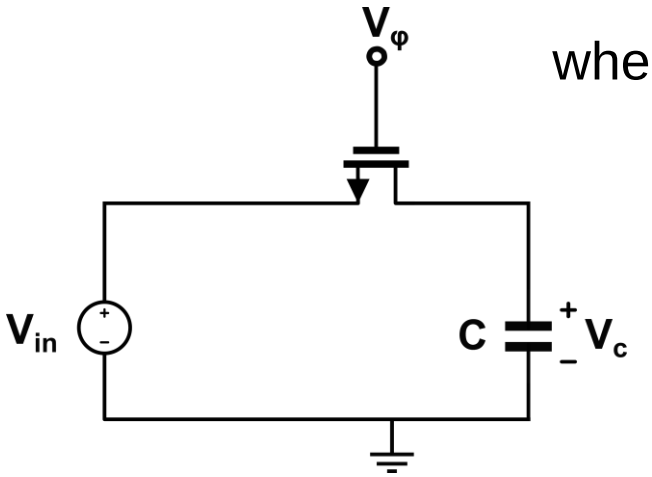
$$= \frac{L}{K'W\left(V_{GS} - V_{TH} - V_{DS}\right)}$$

$W/L\uparrow \rightarrow R_{ON}\downarrow$

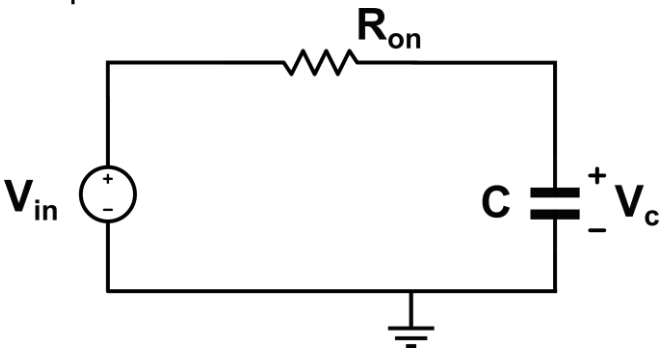
Trade-OFF!

C_{gs} vs. R_{on}

Using a Switch to Charge a Capacitor



when V_φ goes high ($V_\varphi > v_{in} + V_T$)



time constant of $r_{ON}C$

$r_{ON}C << T$

the worst-case value for r_{ON}(the highest value): when v_{DS}=0 and v_{GS}= V_φ-v_{in}

Example

The time V_φ is high is T=0.1μs and C=0.2pF, then r_{ON} must be less than 100 kΩ if sufficient charge transfer occurs in **five time constants**.

Time Constant vs. Resolution

时间	1RC	2RC	3RC	4RC	5RC	6RC
分辨率	1.89b	3.07b	4.40b	5.80b	7.22b	8.66b
%	63.21	86.47	95.02	98.17	99.33	99.75

7RC	8RC	9RC	10RC	11RC	12RC	13RC
10.10b	11.54b	12.98b	14.43b	15.87b	17.31b	18.76b
99.91	99.97	99.99	99.995	99.998	99.999	99.999

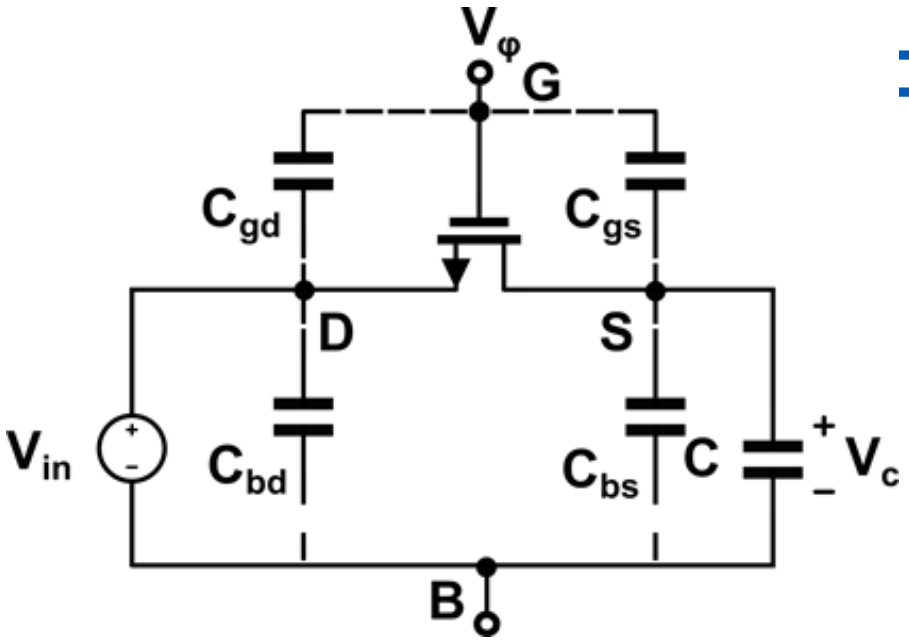
Switch width vs. SNDR

Table 10 Simulated signal to total distortion ratio of the sampled signal for different switch sizes at sampling frequency of 2kHz

Size \ f_{signal}	62.5Hz	250Hz	1kHz
2μm/0.2μm	119.1dB (19.5bit)	109.7dB (17.9bit)	97.5dB (15.9bit)
4μm/0.2μm	116.8dB (19.1bit)	113.8dB (18.6bit)	103.3dB (16.9bit)
8μm/0.2μm	110.9 dB (18.1bit)	110.3dB (18.0bit)	105.8dB (17.3bit)
16μm/0.2μm	104.2 dB (17.0bit)	103.6dB (16.9bit)	100.8dB (16.4bit)

- Use wider switches for fast signals

Clock Feedthrough

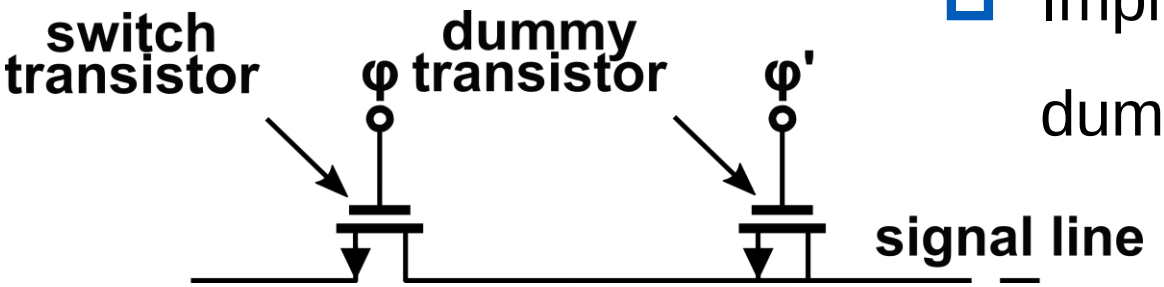


- Clock feedthrough:
  - Negative feedthrough: (sampling)

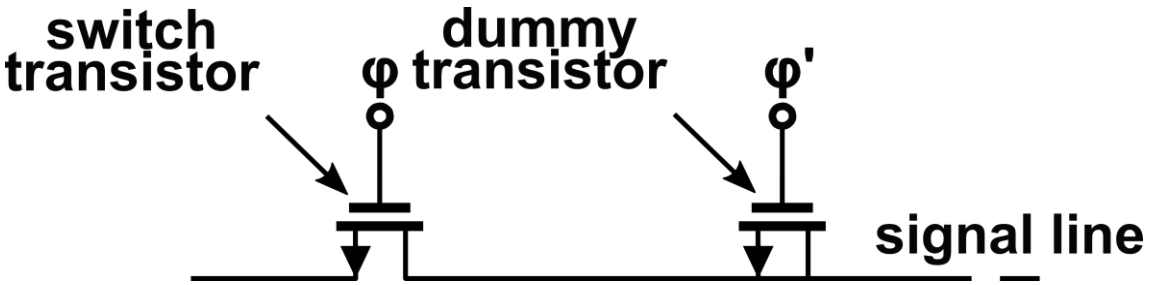
the change of V_{C1} during Φ_1 decreased from $V_{in}+V_T$ to zero.

$$\Delta V_{C_1} = \left(\frac{C_{gs}}{C_1 + C_{gs}} \right) (V_{in} + V_T)$$

- Improving method: using dummy transistor.



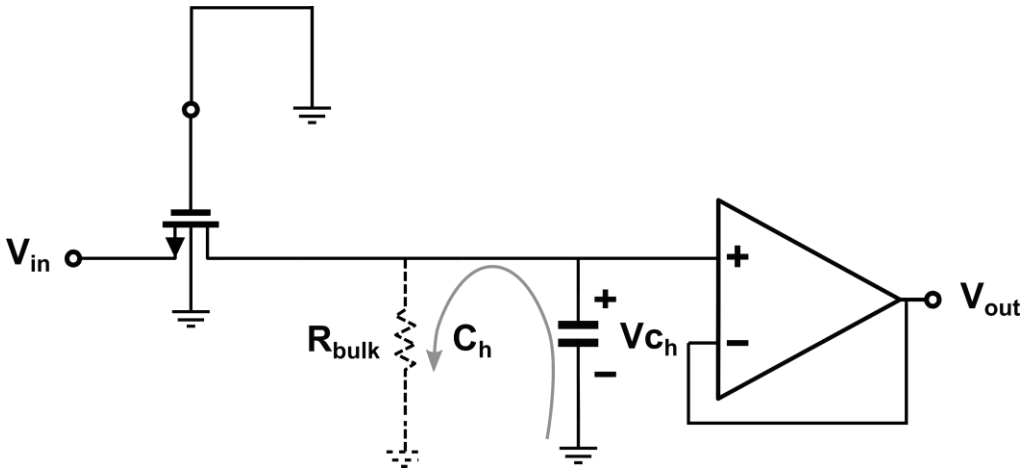
Clock Feedthrough



- **Using "dummy transistor" can alleviate the clock feedthrough. (different clock rising/falling time)**
- **Meanwhile, "dummy transistor" also alleviates the effect of "channel charge".**
- When Φ is high, the channel of MOS transistor is negatively charged; when Φ is low, the negative charge will be transferred to C1, which changes V_{C1}.

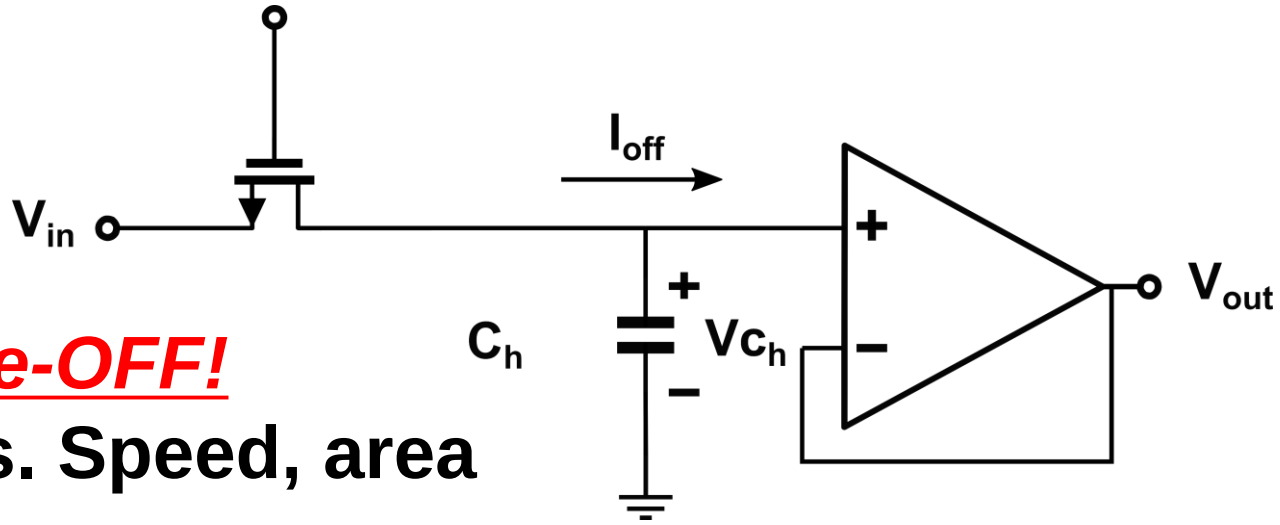
OFF-State

- $V_{GS} \leq V_{TH}$ r_{OFF}
  - Drain-bulk current
  - Source-bulk current (light/temp. sensitive!)
    - Leakage current of PN junction



Applications of a MOS Switch

The influence of I_{OFF} in a sample-and-hold circuit



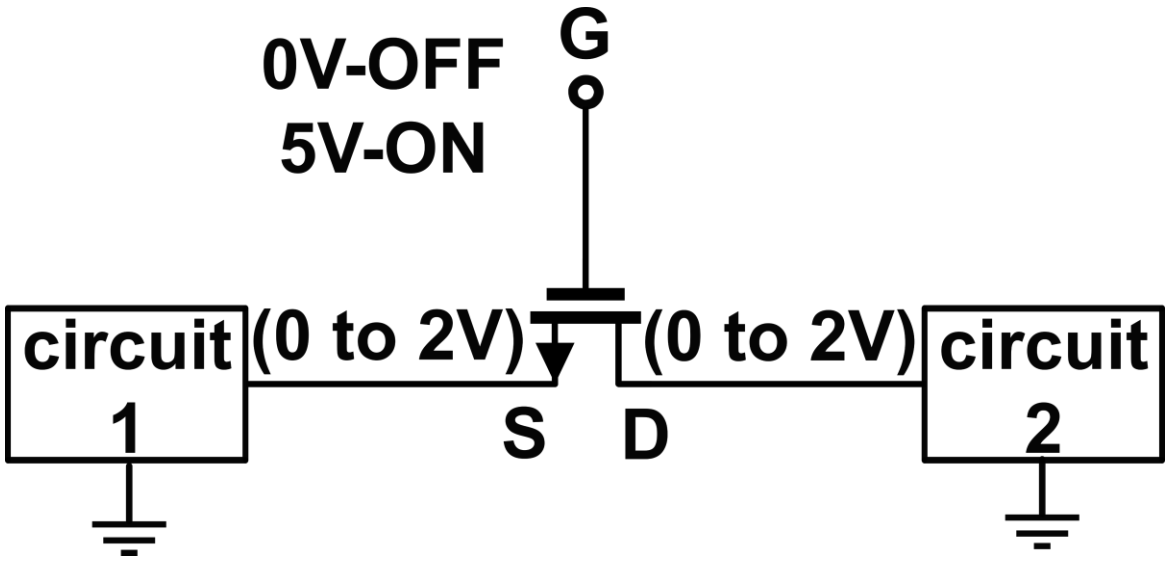
Trade-OFF!

C_h vs. Speed, area

If C_H is not large enough, then in the hold mode where the MOS switch is OFF the **leakage current** can **charge or discharge** C_H a **significant amount**.

Range of Voltages on the MOS Switch Terminals

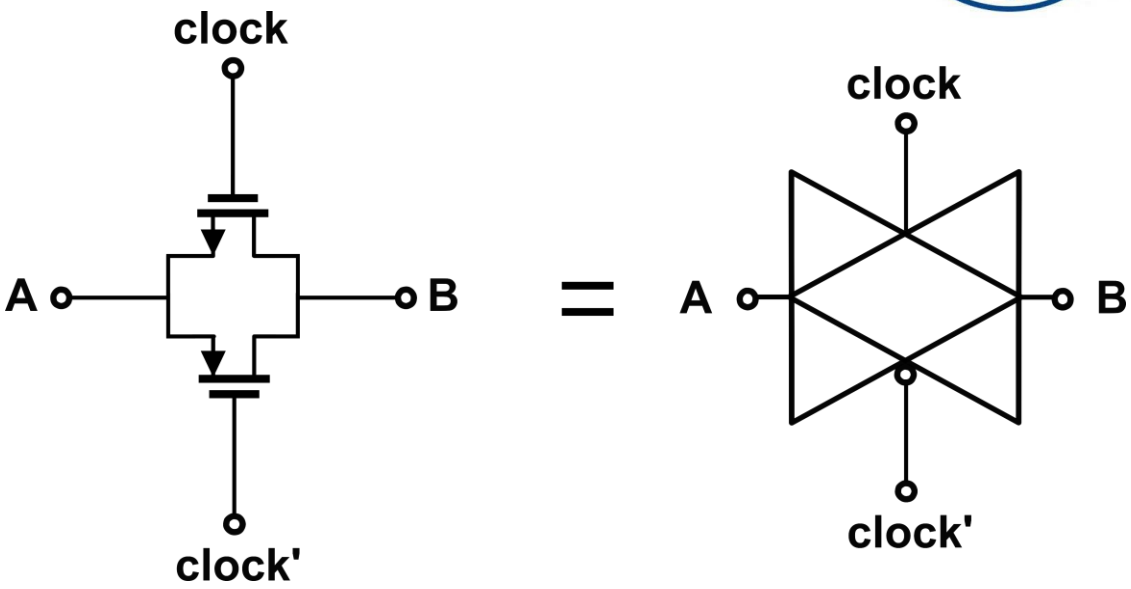
- N-MOS: V_G must be larger than V_D *or* V_S
- P-MOS: V_G must be less than V_D *or* V_S



Application of an n-channel transistor as a switch with typical terminal voltages indicated

CMOS Switch

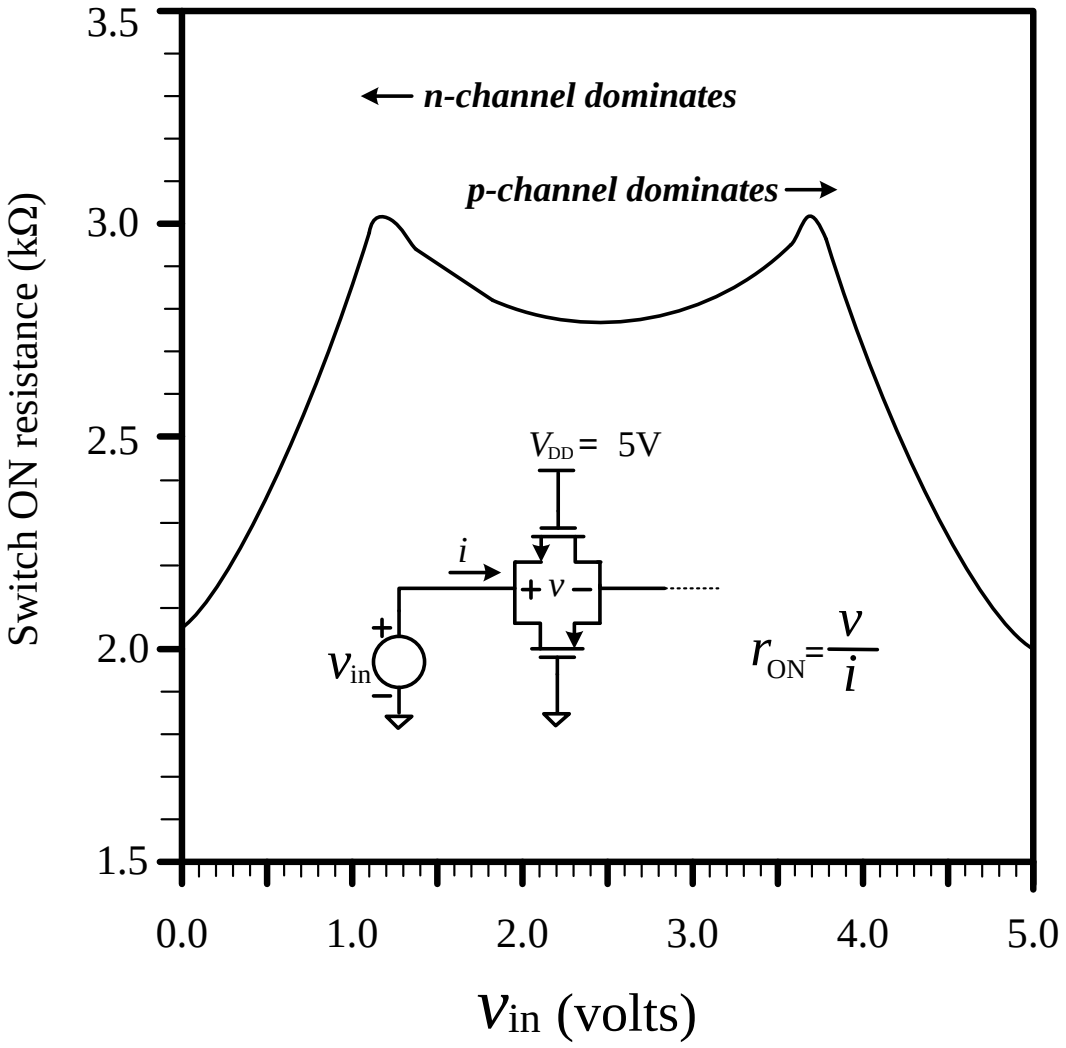
Transmission Gate



- Advantages:
  - Feedthrough somewhat diminished
  - Larger dynamic range
  - Lower ON resistance
- Disadvantages:
  - Requires a **complementary clock**
  - Requires more area

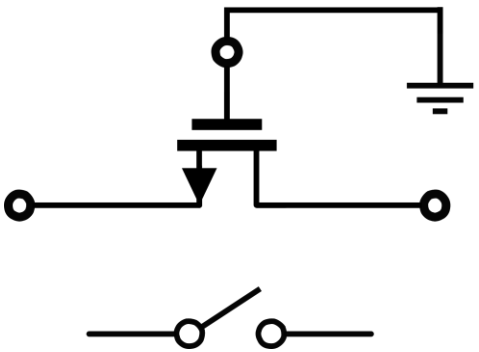
Trade-OFF!

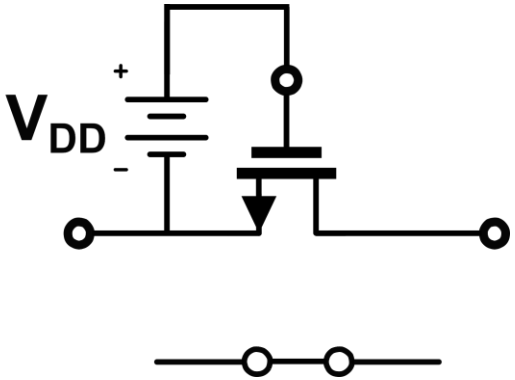
CMOS Switch

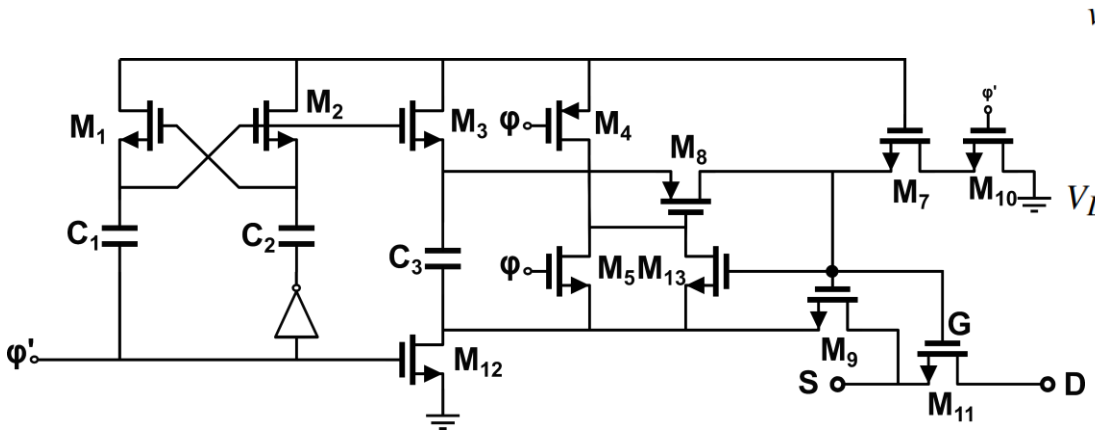

n-channel dominates
p-channel dominates
Switch ON resistance (kΩ)
3.5
3.0
2.5
2.0
1.5
0.0
1.0
2.0
3.0
4.0
5.0
V_{in} (volts)
V_{DD} = 5V
i
v
v_{in}
$r_{ON}=\frac{v}{i}$

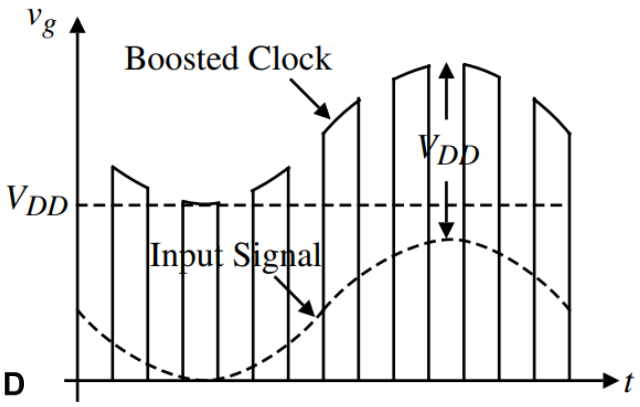
Bootstrapped Switches

- Constant Overdrive Voltage







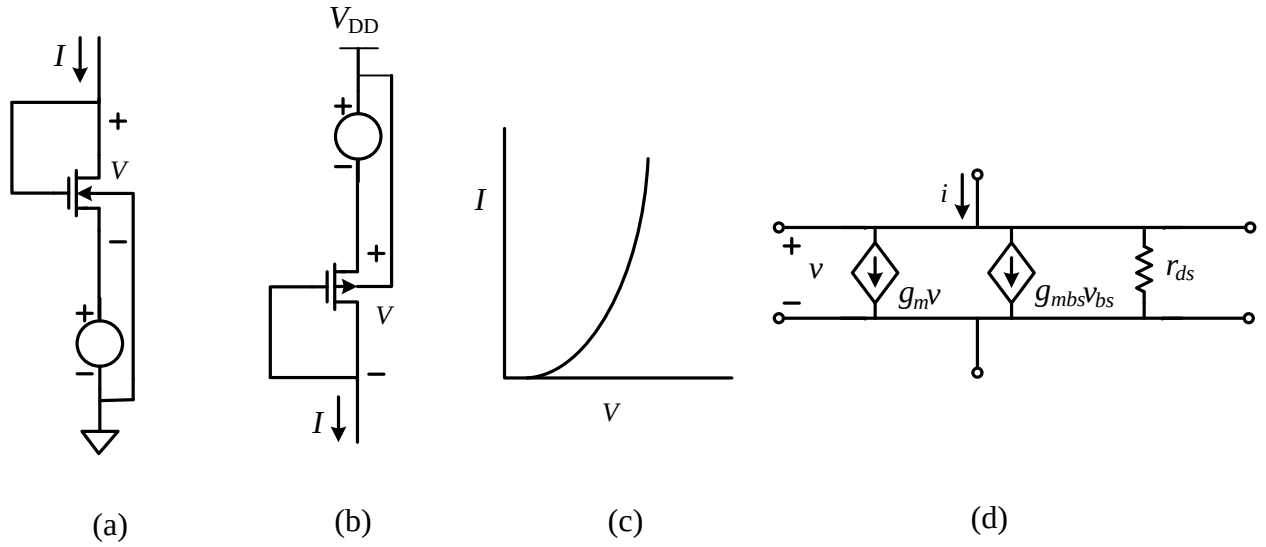


A.M. Abo and P.R. Gray, "A 1.5V, 10-bit, 14.3-MS/s CMOS Pipeline Analog-to-Digital Converter, IEEE J. of Solid-State Circuits, Vol. 34, No. 5, May 1999, pp. 599-605.

Outline

- MOS Switch
- MOS Diode/Active Resistor
- Current Sinks and Sources

MOS Diode/Active Resistor



(a) (b) (c) (d)

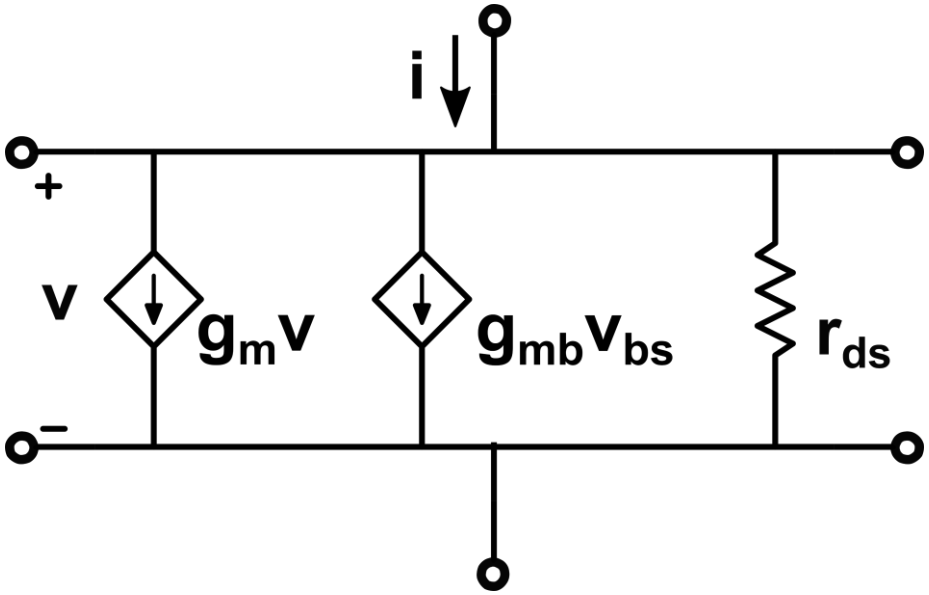
Active resistor: (a) n-Channel; (b) p-Channel; (c) I-V characteristics for n-channel case; (d) Small signal model.

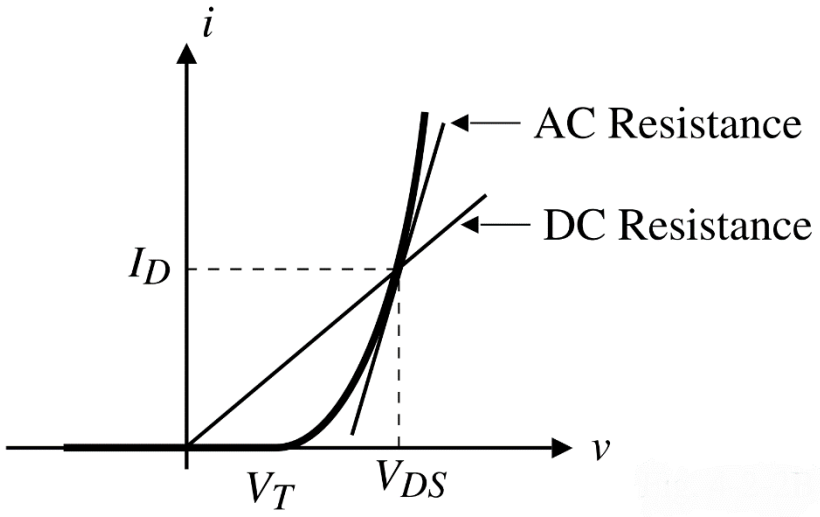
I-V characteristics

$$I = I_D = \left(\frac{K'W}{2L}\right)\left[\left(V_{GS} - V_{TH}\right)^2\right] = \frac{\beta}{2}\left(V_{GS} - V_{TH}\right)^2$$

$$V = V_{GS} = V_{DS} = V_{TH} + \sqrt{2I_D/\beta}$$

I-V Characteristics

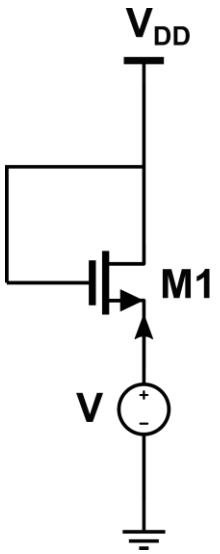


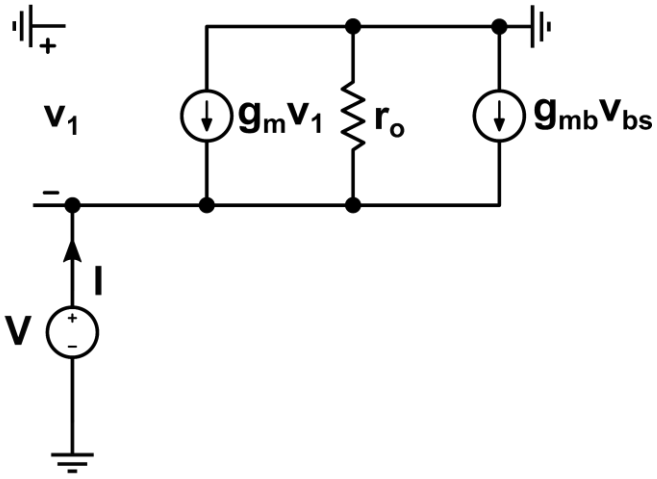


$$g = \frac{\partial I}{\partial V} = \left(\frac{2IK'W}{L} \right)^{\frac{1}{2}} = \frac{K'W}{L}\left(V - V_{TH}\right)$$

$$r_{OUT} = \frac{1}{g_m + g_{mbs} + g_{ds}} \cong \frac{1}{g_m}$$

I-V Characteristics





MOS-diode circuit and its small signal equivalent circuit when considering body effect.
(a) MOS diode when considering body effect;
(b) Small signal equivalent circuit of (a)

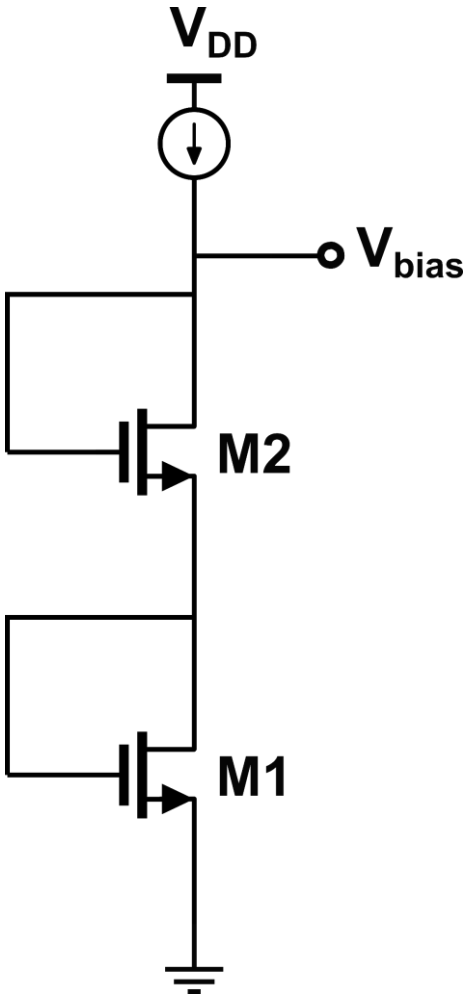
$$V_1 = -V$$

$$V_{bs} = -V$$

$$\left(g_m + g_{mb}\right)V + \frac{V}{r_0} = I$$

$$\frac{V}{I} = \frac{1}{g_m + g_{mb} + 1/r_0} = \frac{1}{g_m + g_{mb}} // r_0$$

Voltage Division using Active Resistors



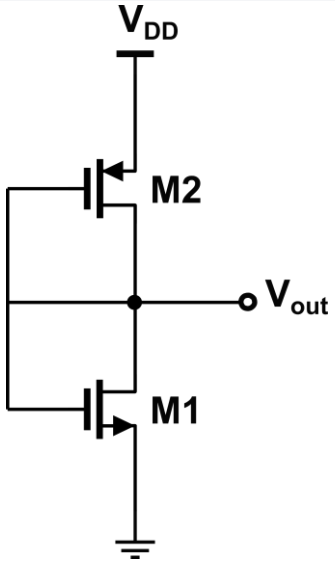
$$V_{DS} = \sqrt{2I_D/\beta} + V_{TH} = V_{ON} + V_{TH}$$

$$V_{BIAS} = V_{DS1} + V_{DS2} = 2V_{ON} + 2V_{TH}$$

Example 5.1

If Vdd ＝5V, Vss =-5V , Vout=0V , I=8uA , calculate the W/L of M1 and M2. (Using the model parameter values in TABLE 3.1)

Designing voltage division using active resistors



From TABLE 3.1 we get

$$K'_N = 17.0 \pm 10\% \mu A/V^2$$

$$K'_P = 8.0 \pm 10\% \mu A/V^2$$

$$V_{TN0} = 1 \pm 0.2V, V_{TP0} = -1 \pm 0.2V$$

then $$I = I_D = \left(\frac{K'W}{2L}\right)\left[\left(V_{GS} - V_{TH}\right)^2\right] = \frac{\beta}{2}\left(V_{GS} - V_{TH}\right)^2$$

$$8 \times 10^{-6} = \frac{1}{2} K' \frac{W}{L} (5-1)^2$$

NMOS is better !

so $$K = K'\frac{W}{L} = 1\mu A/V^2$$

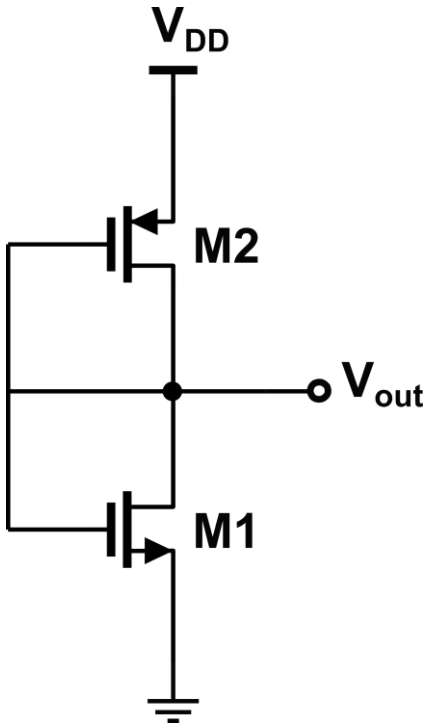
(W/L)1=1/17，(W/L)2=1/8.

TABLE 5.1

符号	模型参数	典型的模型参数值		单位
		NMOS	PMOS	
V_{T0}	V_{BS}=0时的阈值电压	1±0.2	−1±0.2	V
K' (饱和)	跨导参数（在饱和区）	17.0±10%	8.0±10%	μA/V^2
K' (非饱和)	跨导参数（在非饱和区）	25.0±10%	10.0±10%	μA/V^2
γ	体效应因子	1.3	0.6	(V)$^{1/2}$
λ	沟道长度调制系数	0.01 (L=10μm) 0.004(L=20μm)	0.02 (L=10μm) 0.008(L=20μm)	(V)$^{-1}$
$2\|\Phi_F\|$	强反型时表面势	0.7	0.6	(V)

Area Issue

Active resistors are always limited by area:
Example 3.1. W1/L1=1/17, if we choose W1 as the unit length, then L1 is 17 units long, and the active area is 17 units. For M2, choose W2 as the unit length, then L2 is 8 units long, and the active area is 8 units.



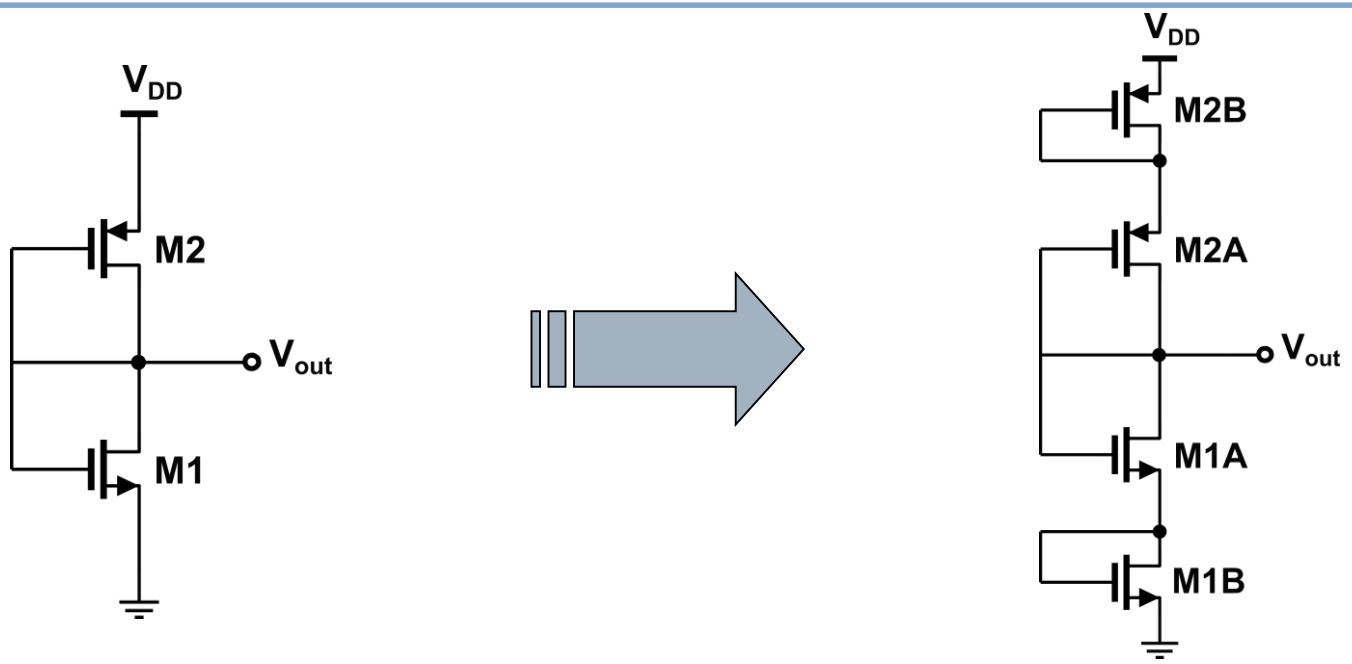
M1: W1/L1=1/17

M2: W2/L2=1/8

Example 5.2

Reducing the area of active resistors

M1A=M1B, M2B=M2A, ignore the body effect of M1A and M2A, calculate the W/L of M1 and M2 and the consumed area with the same condition of example 3.1.



A practical circuit with the same function but consuming smaller area

Example 5.2

Reducing the area of active resistors

The supply voltage is divided equally by M1 and M2, the gate source voltage of both are 2.5V. Therefore，β1＝β2＝64/9uA/V². So W1/L1 is 64/153 and W2/L2 is 8/9.

$$\frac{K_1}{2}(5-1)^2 = \frac{K_{1_{NEW}}}{2}(2.5-1)^2$$

$$\frac{K_1}{2}\cdot 16 = \frac{K_{1_{NEW}}}{2}\cdot 2.25 \Rightarrow \frac{K_{1_{NEW}}}{K_1} = \frac{64}{9}$$

$$K_1 = 1\mu A/V^2, K_{1_{NEW}} = 64/9\,\mu A/V^2$$

$$K'_1\frac{W_1}{L_1}\bigg|_{NEW} = \frac{64}{9}, \frac{W_1}{L_1}\bigg|_{NEW} = \frac{64}{9}\frac{1}{17} = \frac{64}{153}$$

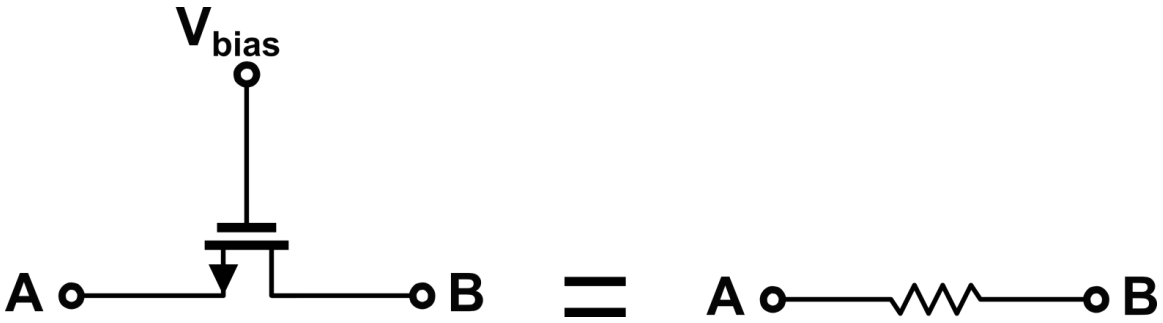
$$K'_2\frac{W_2}{L_2}\bigg|_{NEW} = \frac{64}{9}, \frac{W_2}{L_2}\bigg|_{NEW} = \frac{64}{9}\frac{1}{8} = \frac{8}{9}$$

Choose W1 as the unit length, then L1 is 153/64, and the active area of M1A and M1B is 2×(153/64)＝4.781 units square.

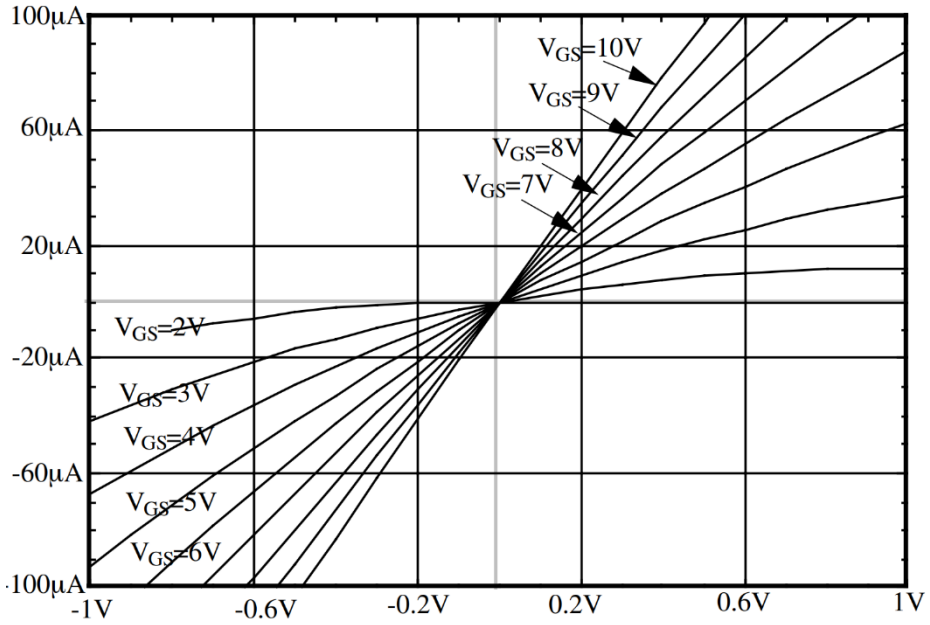
Similarly, the active area of M2A and M2B is 2×(9/8)＝2.25 units square.

The total area consumed by the four devices is only 7.03 units square.

Floating Active Resistor using a Single MOS



Floating active resistor using a single MOS transistor.



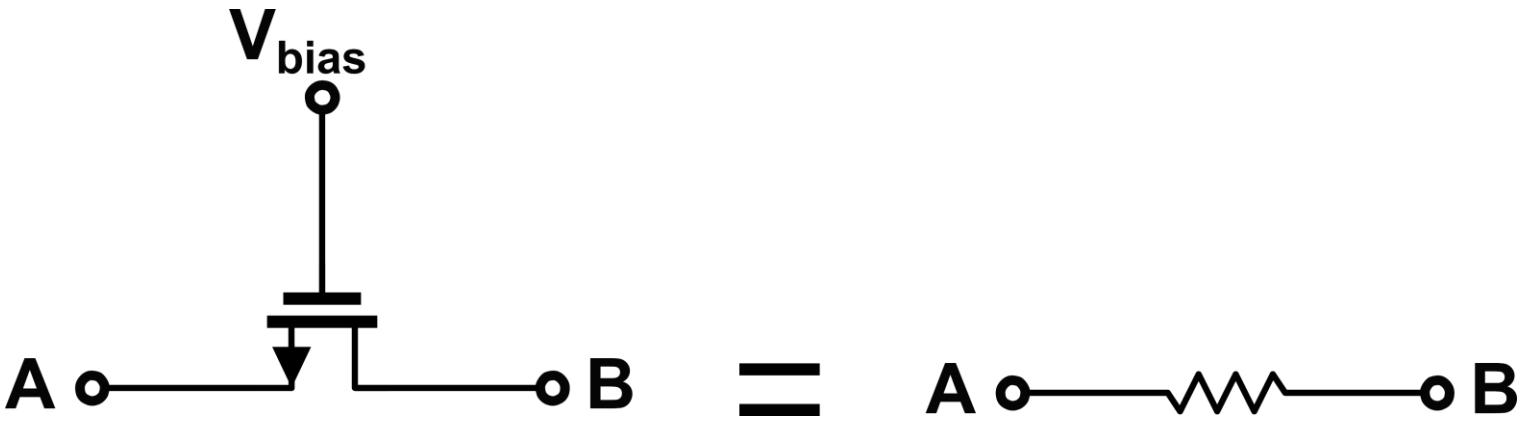
Non-saturation region:

$$r_{ds} = \frac{L}{K'W\left(V_{GS} - V_T\right)}$$

Example 5.3

Calculation of the resistance of an active resistor

The floating active resistor is to be used to design a 1kΩ resistance. The dc value of $V_{A,B}$=2V. Use the device parameters in TABLE 3.2 and assume the active resistor is an n-channel transistor with the gate voltage at 5 V. Assume that V_{DS}=0.0. Calculate the required *W/L* to achieve 1kΩ resistance. The bulk terminal is 0.0V.



Floating active resistor using a single MOS transistor.

Example 5.3

Calculation of the resistance of an active resistor

The floating active resistor is to be used to design a 1kΩ resistance. The dc value of $V_{A,B}$=2V. Use the device parameters in TABLE 3.2 and assume the active resistor is an n-channel transistor with the gate voltage at 5 V. Assume that $\boldsymbol{V_{DS}=0.0}$. Calculate the required *W/L* to achieve 1kΩ resistance. The bulk terminal is 0.0V.

Solution:

Before applying Eq. (2), it is necessary to calculate the **new threshold voltage**, V_T, due to V_{BS} not being zero (VBS｜=2V). From Eq. (1) the new V_T is found to be 1.022V. Equating Eq. (2) to 1000Ω gives a W/L of 4.597≈4.6

$$V_T = V_{T0} + \gamma\left(\sqrt{2|\phi_F| + v_{SB}} - \sqrt{2|\phi_F|}\right) \qquad (1)$$

$$r_{ds} = \frac{L}{K'W\left(V_{GS} - V_T\right)} \qquad (2)$$

Example 5.3

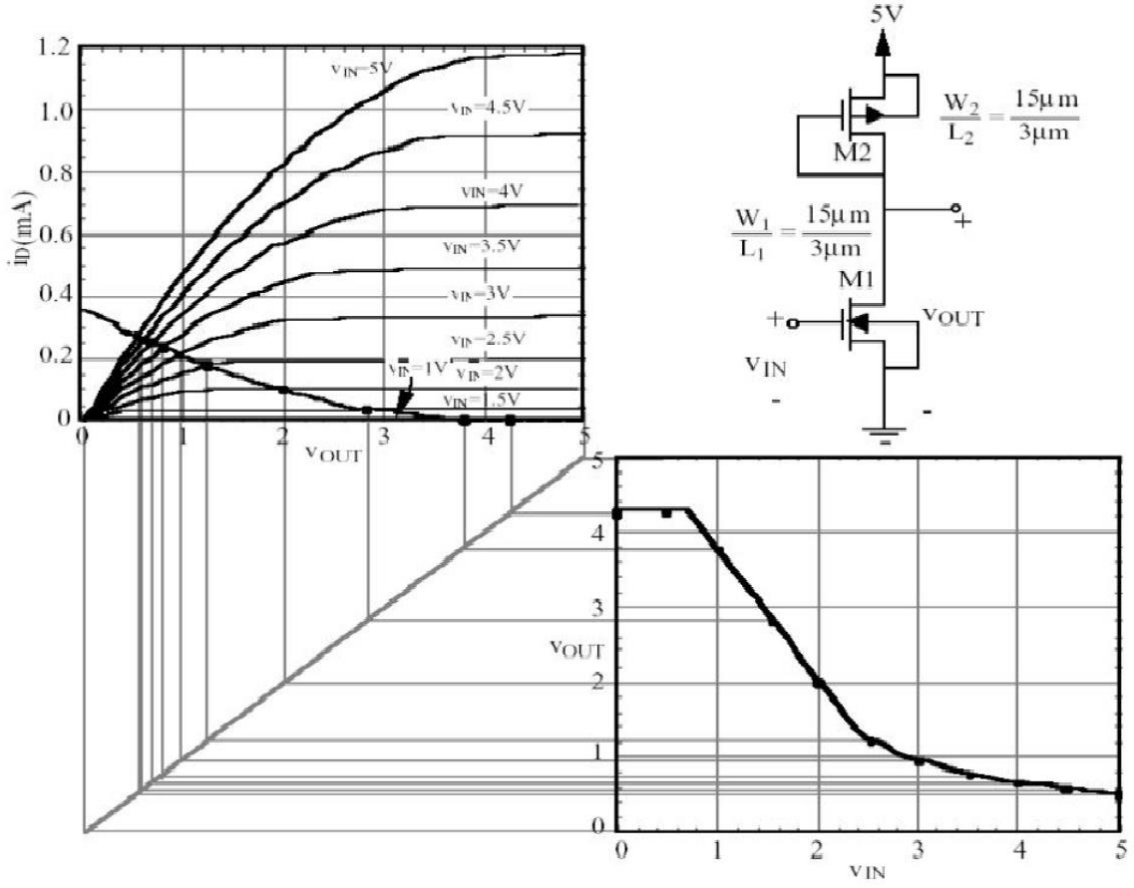
Calculation of the resistance of an active resistor

TABLE 3.2 Model Parameters for a Typical COMS Bulk Process Suitable for Hand Calculations Using the Simple Model with Values Based on a 0.8μm Silicon-Gate Bulk CMOS n- Well Process

Parameter Symbol	Parameter Description	Typical Parameter Value		Units
		n-Channel	p-Channel	
V_{T0}	Threshold voltage (V_{BS} =0)	0.7±0.15	−0.7±0.15	V
K'	Transconductance parameter (in saturation)	110.0±10%	50.0±10%	$\mu A/V^2$
γ	Bulk threshold parameter	0.4	0.57	$V^{1/2}$
λ	Channel length modulation parameter	0.04 (L=1μm) 0.01 (L=2μm)	0.05 (L=1μm) 0.01 (L=2μm)	V^{-1}
$2\|\Phi_F\|$	Surface potential at strong inversion	0.7	0.8	V

Application of diode resistor (1)

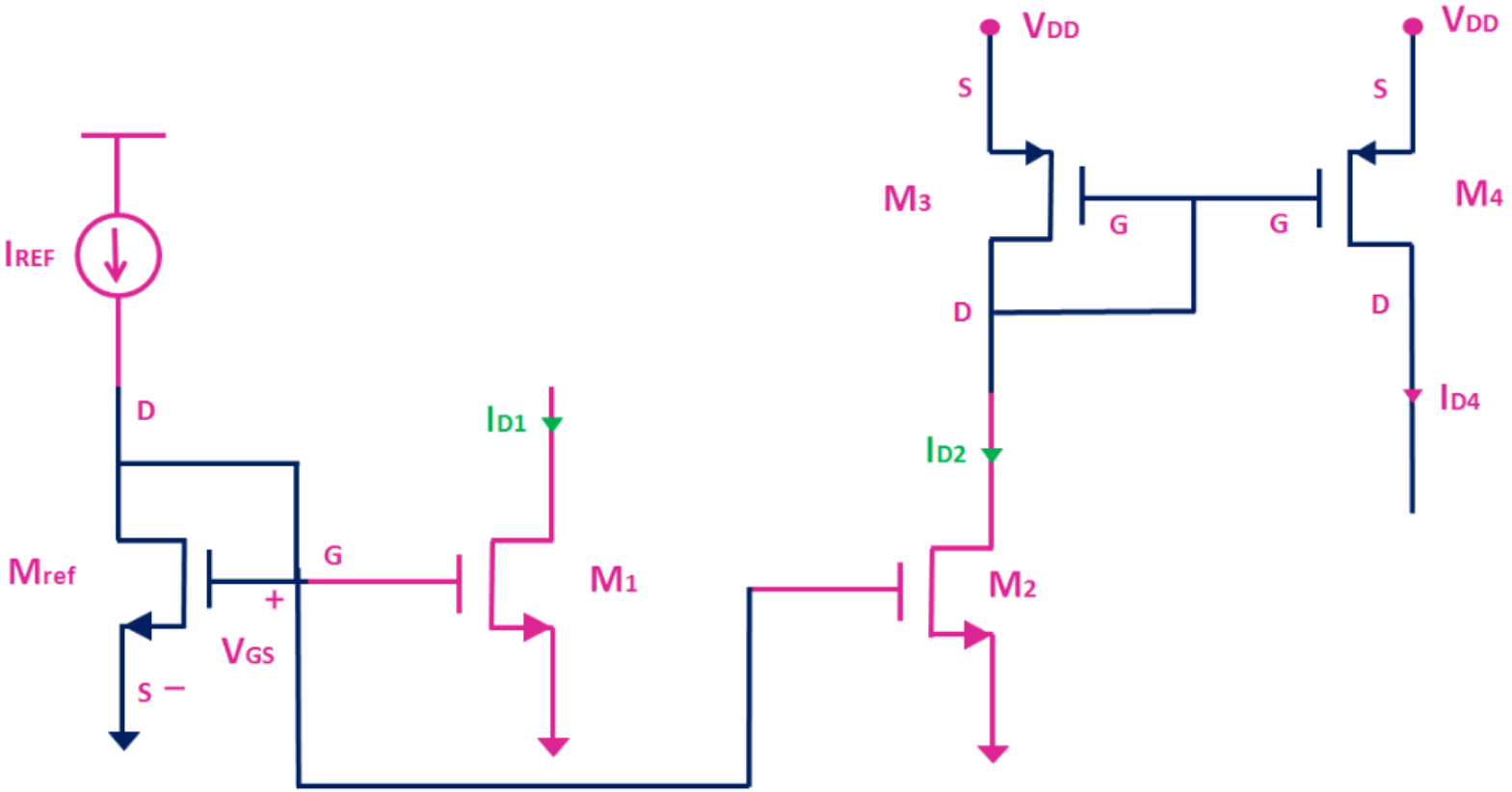
- Low gain amplifier



$Gain = G_{m1} / G_{m2}$

Application of diode resistor (2)

- Current mirror



Voltage bias vs. current bias

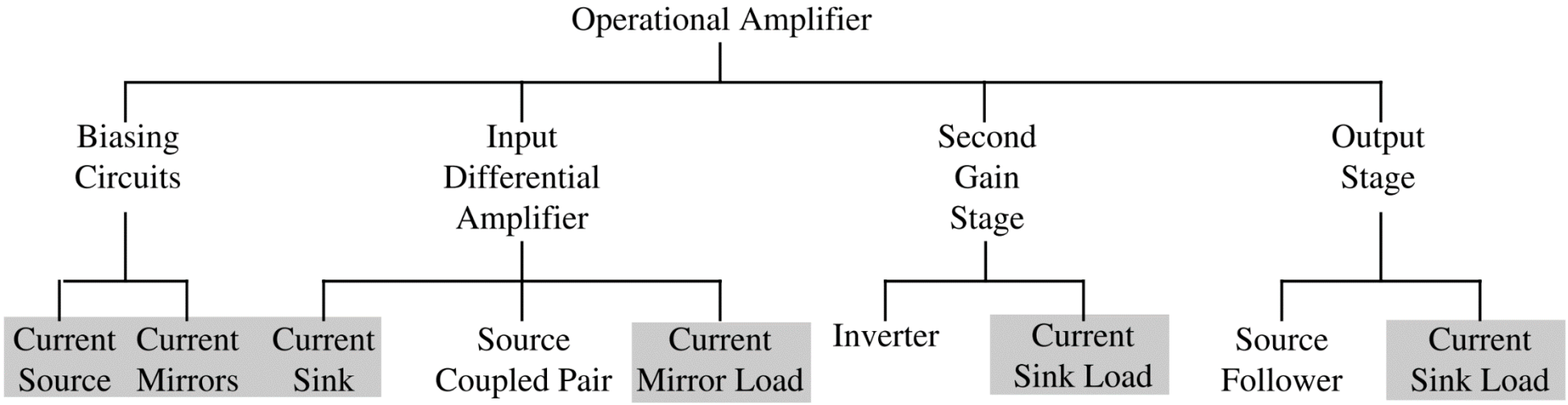
Difference between Sw. & Diode

- **MOS Switch**
  - *linear region resistor*
  - *work dynamically -> charge feedthrough etc.*
- **MOS Diode/Active Resistor**
  - *saturation region resistor*
  - *work continuously -> Gain/Bandwidth etc.*

Outline

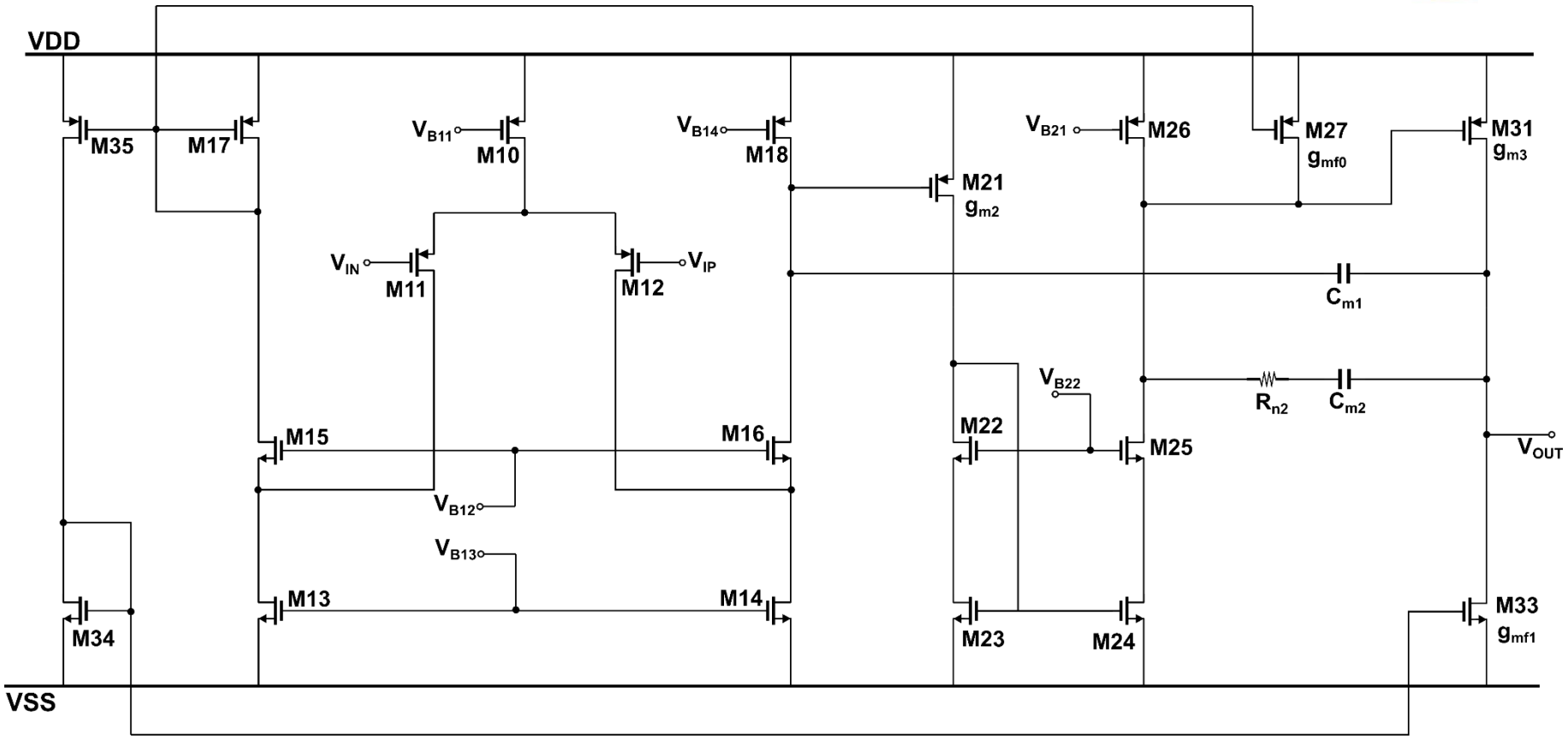
- MOS Switch
- MOS Diode/Active Resistor
- Current Sinks and Sources

Op-AMP: Hierarchy



The Basic Block of all Complicate Systems

Op-AMP:Example



Noise **Bandwidth** **Driving**

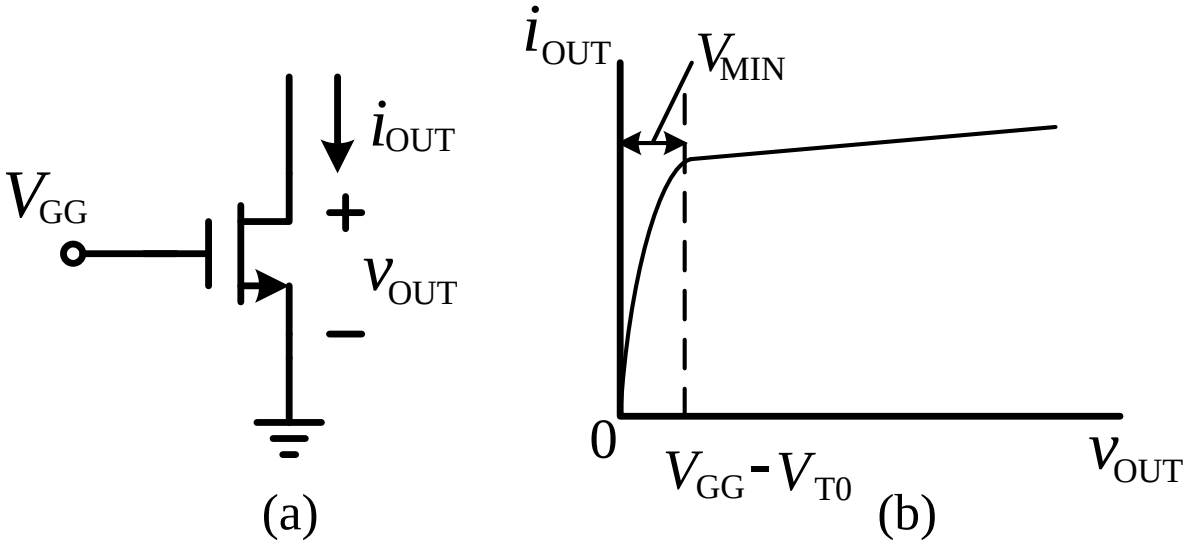
Current Sinks and Sources

- Two terminal components
- Ideal current sink and current source:
  - Current - constant
  - Independent of the voltage

    -> **high output resistance**

*why aforementioned **MOS Switch** and **MOS Diode/Active Resistor** cannot be current source?*

Current Sinks

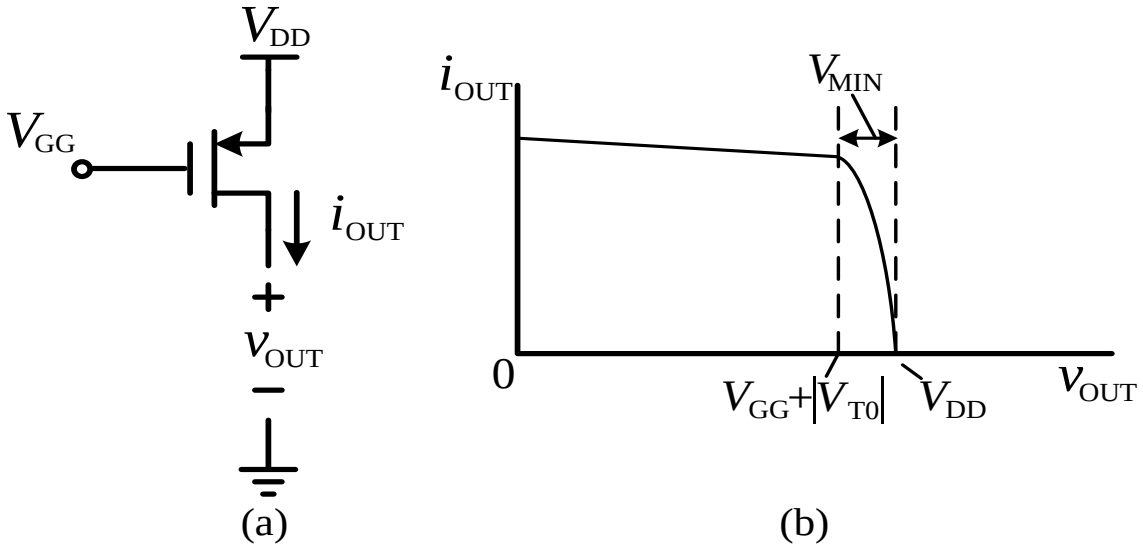


(a) Current sink ; (b) Current-voltage characteristics of (a)

$$v_{OUT} \geq V_{GG} - V_{T0}$$

$$r_{out} = \frac{1+\lambda V_{DS}}{\lambda I_D} \cong \frac{1}{\lambda I_D}$$

Current Sources



(a) Current source; (b) Current-voltage characteristics of (a)

$$v_{OUT} \le V_{GG} + |V_{T0}| \qquad r_{out} = \frac{1+\lambda V_{DS}}{\lambda I_D} \cong \frac{1}{\lambda I_D}$$

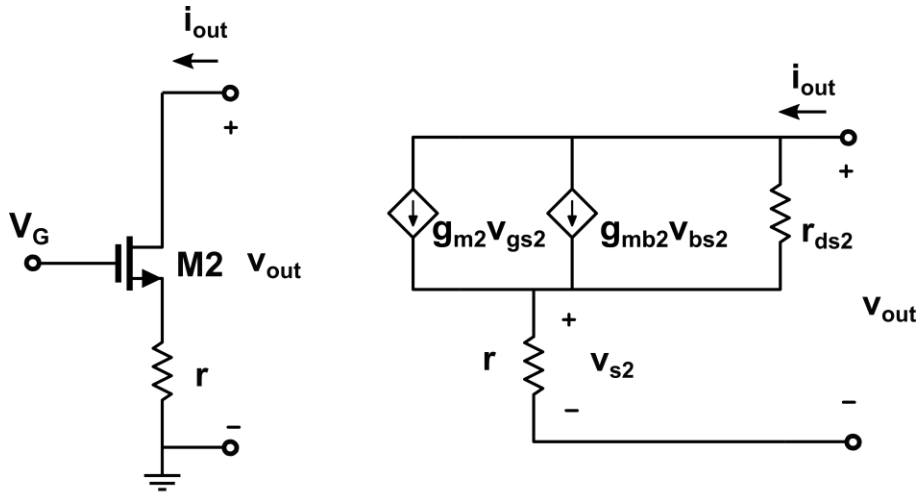
Improvement of Current Sink and Source

- Increase the small-signal **output resistance**
  - more constant current over the range of v_{OUT}
- Reduce the value of V_{MIN}
  - a large range of v_{OUT} over which the current sink/source works

√ **Device structure**

√ **Circuit structure**

Increasing the Output Resistance of a Resistor R



Use control loop to derive the output resistance !

(a) Technique for increasing the output resistance of a resistor r. (b) Small. signal model for the circuit in (a).

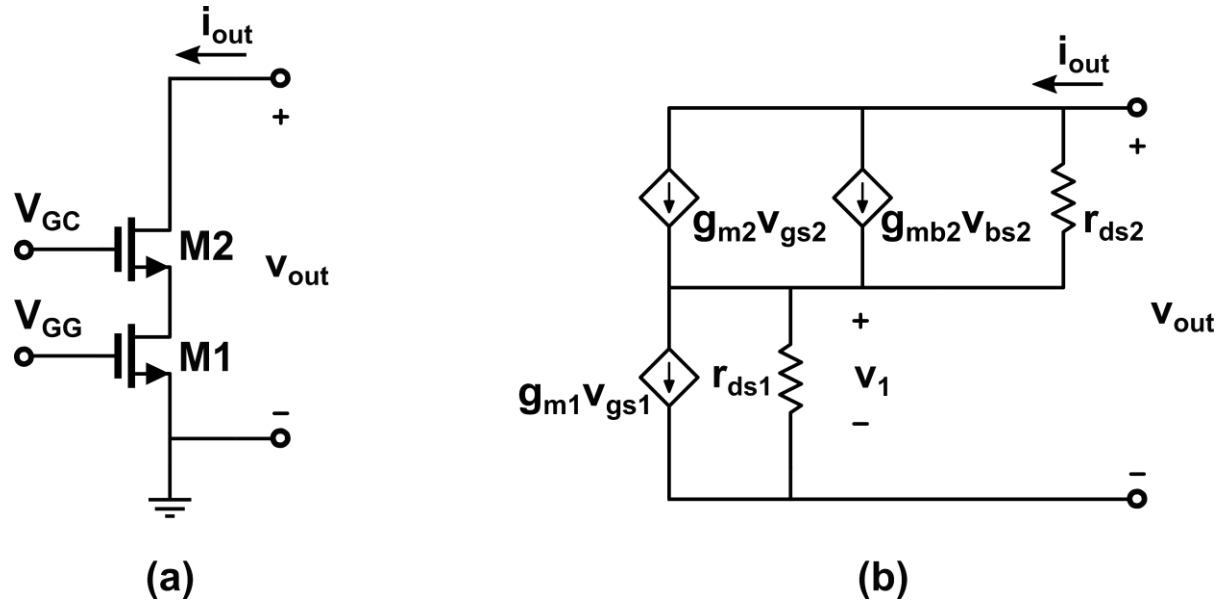
$$v_{out} = i_{out}r + i_{out}r_{ds2} + i_{out}r_{ds2}\left(g_{m2} + g_{mbs2}\right)r$$

$$v_{gs2} = -v_{s2}$$
$$v_{bs2} = -v_{s2}$$

$$r_{out} = \frac{v_{out}}{i_{out}} = r + r_{ds2} + \left[\left(g_{m2} + g_{mbs2}\right)r_{ds2}\right]r \cong \left(g_{m2} \cdot r_{ds2}\right)r$$

where $g_{m2}r_{ds2} >> 1$ and $g_{m2} > g_{mbs2}$

Circuit for increasing Rout of a Current Sink



$$v_1 = i_{out} r_{ds1}$$

$$v_{gs2} = -v_1$$

$$v_{gs1} = 0$$

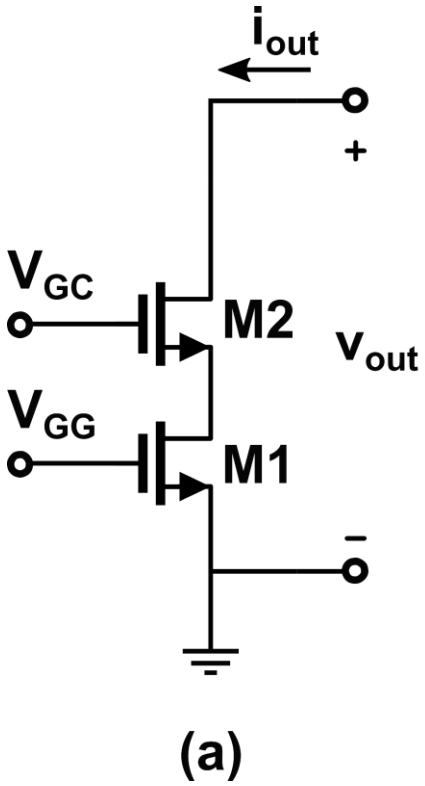
(a) Circuit for increasing rout of a current sink. (b) Small-signal model for the circuit in (a).

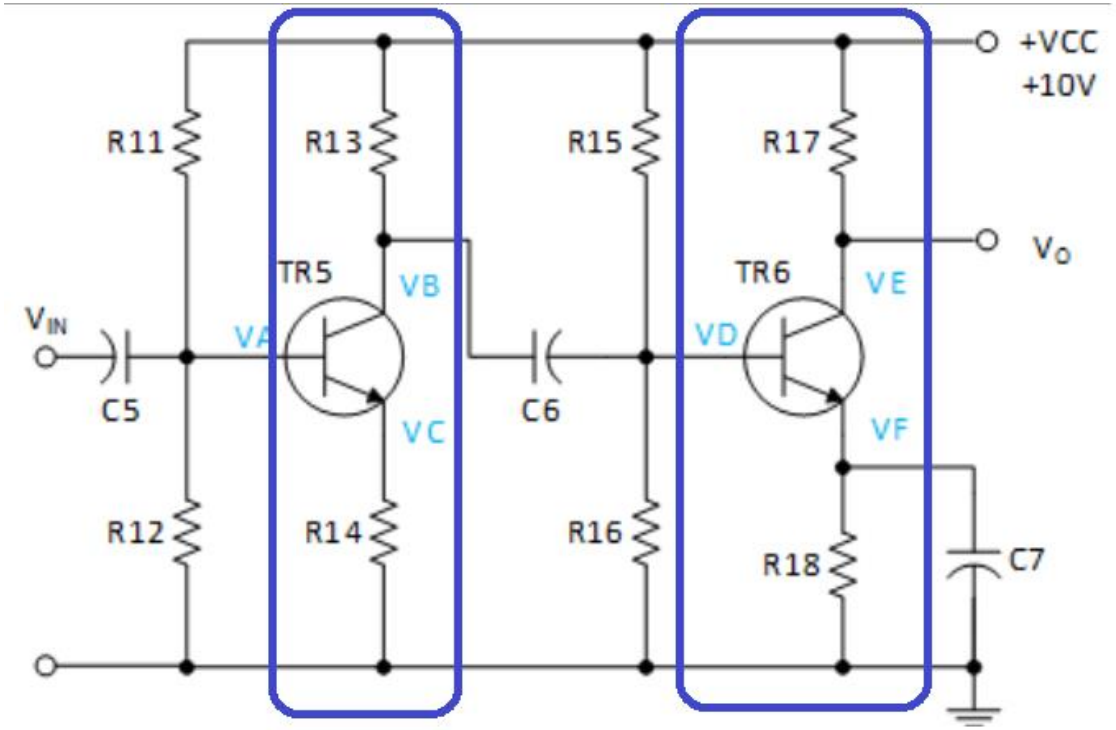
$$i_{out} + g_{m2}v_1 + g_{mbs2}v_1 = g_{ds2}\left(v_{out} - v_1\right)$$

$$r_{out} = \frac{v_{out}}{i_{out}} = r_{ds2}\left(1 + g_{m2}r_{ds1} + g_{mbs2}r_{ds1} + g_{ds2}r_{ds1}\right) = r_{ds1} + r_{ds2} + g_{m2}r_{ds1}r_{ds2}\left(1 + \eta_2\right)$$

$$r_{out} \cong \left(g_{m2} \cdot r_{ds2}\right) r_{ds1}$$

Cascode vs Cascade

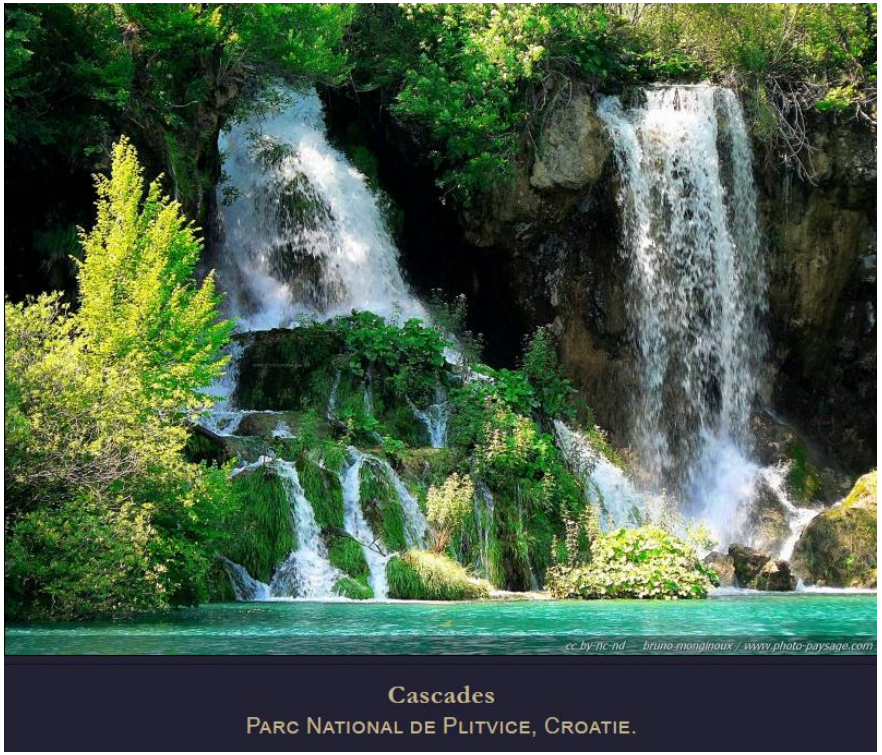


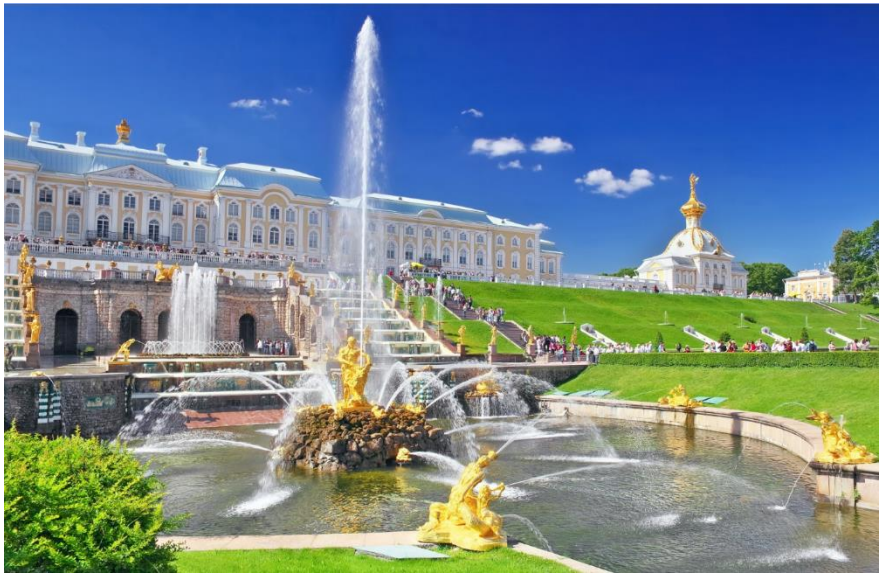


共源共栅级 Cascode

级联型 Cascaded Amplifier

A Cascade from sightseeing…

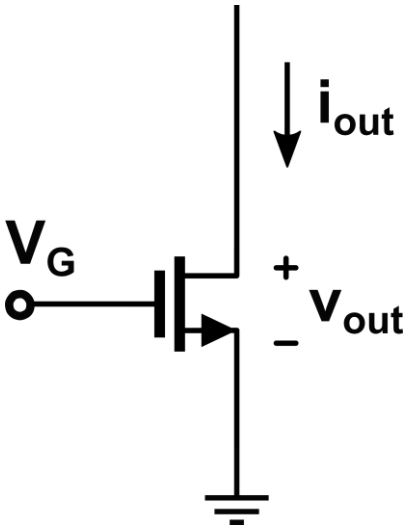


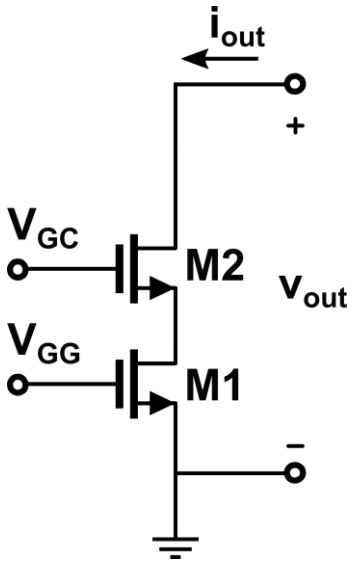


The Grand Cascade
St Petersburg, Russia

Example 5.4

Calculation of output resistance for a current sink





Use the model parameters of Table to calculate:

(a) the small-signal output resistance for the simple current sink of Fig.(left) if I_{OUT}=100μA;

(b) the small-signal output resistance if the simple current sink of Fig.(left) is inserted into the cascode current-sink configuration of Fig.(right). Assume that $W1/L1=W2/L2=1$.

Example 5.4

Calculation of output resistance for a current sink

Table 5.1-2

Parameter Symbol	Parameter Description	Typical Parameter Value		Units
		n-Channel	p-Channel	
V_{T0}	Threshold voltage (V_{BS} =0)	0.7±0.15	−0.7±0.15	V
K'	Transconductance parameter (in saturation)	110.0±10%	50.0±10%	μA/V^2
γ	Bulk threshold parameter	0.4	0.57	V$^{1/2}$
λ	Channel length modulation parameter	0.04 (L=1μm) 0.01 (L=2μm)	0.05 (L=1μm) 0.01 (L=2μm)	V^{-1}
$2\|\Phi_F\|$	Surface potential at strong inversion	0.7	0.8	V

Solution:

(a) Using λ=0.04 and I_{OUT}=100μA gives a small-signal output resistance of **250kΩ**.

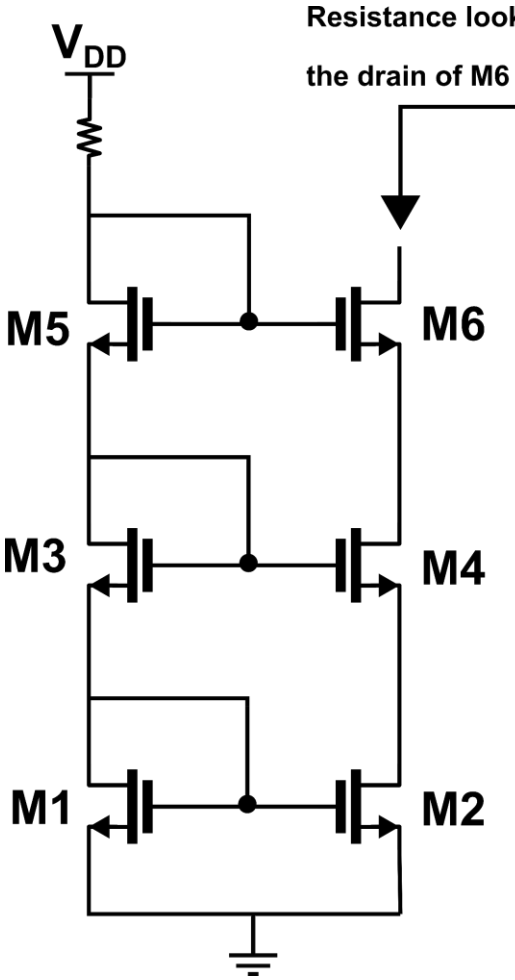
$$r_{out} \cong 1/\lambda I_D$$

(b) The body-effect term, g_{mbs2}, can be ignored with little error in the result. Eq. (1) gives g_{m1}= g_{m2}=148μA/V. Substituting these values into Eq.(2), gives the small-signal output resistance of the cascode current sink as **9.25 MΩ.**

$$g_m = \frac{\partial i_D}{\partial v_{GS}} = \sqrt{(2K'W/L)|I_D|(1+\lambda V_{DS})} \cong \sqrt{2K'W/L|I_D|} \qquad (1)$$

$$r_{out} \cong (g_{m2} r_{ds2}) r_{ds1} \qquad (2)$$

Three-stage Cascode Current Source



The triple cascode current source

$$r_{out} = r_{ds6}\left\{1+g_{m6}\left[r_{ds4}\left(1+g_{m4}r_{ds2}\right)+r_{ds2}\right]\right\}$$
$$+r_{ds4}\left(1+g_{m4}r_{ds2}\right)+r_{ds2}$$
$$\approx g_{m6}g_{m4}r_0^3$$

assume:

$$r_{ds2} = r_{ds4} = r_{ds6} = r_0$$

Reduce the Value of V_{MIN}

$$V_{GS} = V_{ON} + V_{TH} \Rightarrow i_D = \frac{K'W}{2L}(V_{ON})^2$$

the minimum value of v_{DS} when the device remain in saturation:

$$v_{DS}(sat) = V_{GS} - V_{TH} = V_{ON}$$

- If currents are equal (in series):

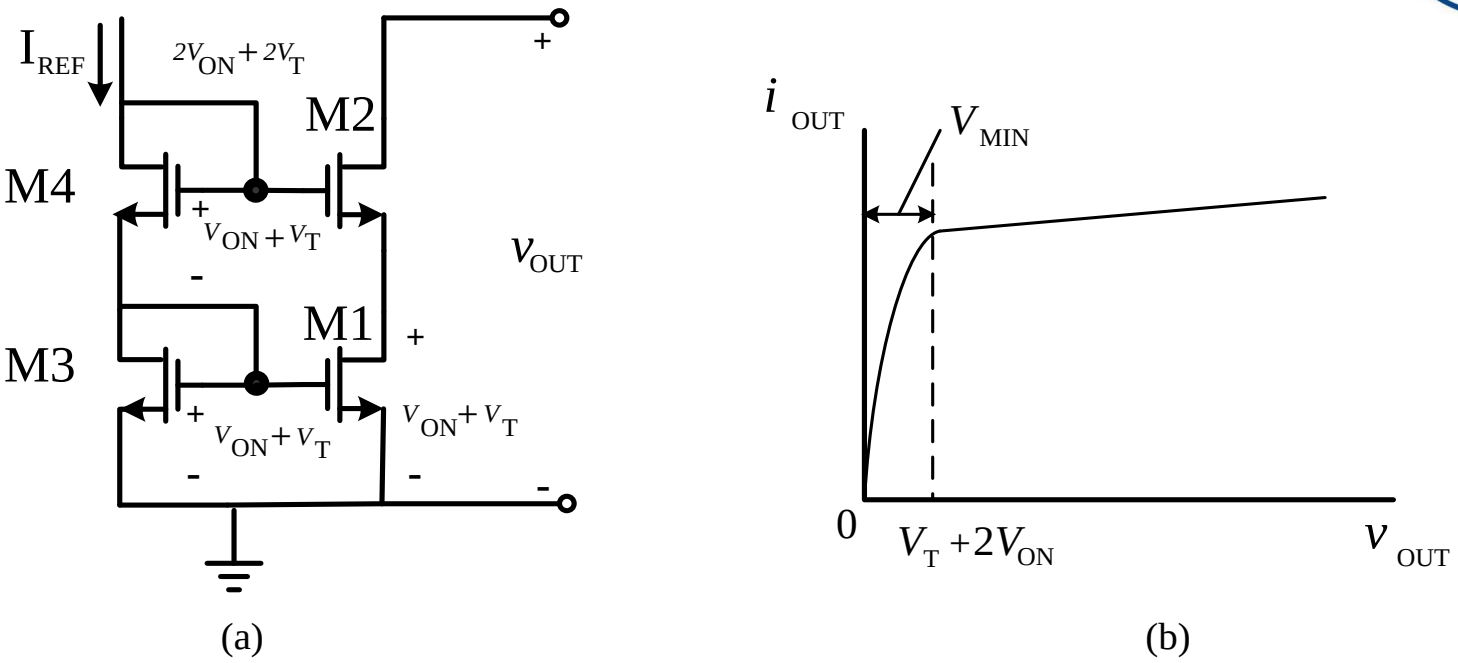
$$\frac{K_1'W_1}{2L_1}(V_{ON1})^2 = \frac{K_2'W_2}{2L_2}(V_{ON2})^2$$

$$\Rightarrow \frac{W_1}{L_1}(V_{ON1})^2 = \frac{W_2}{L_2}(V_{ON2})^2 \quad \text{or} \quad \frac{(W_1/L_1)}{(W_2/L_2)} = \frac{(V_{ON2})^2}{(V_{ON1})^2}$$

- If V_{GS} are equal

$$i_{D1}\left(\frac{W_2}{L_2}\right) = i_{D2}\left(\frac{W_1}{L_1}\right) \quad \text{or} \quad \frac{i_{D1}}{i_{D2}} = \frac{(W_1/L_1)}{(W_2/L_2)}$$

Standard Cascode Current Sink

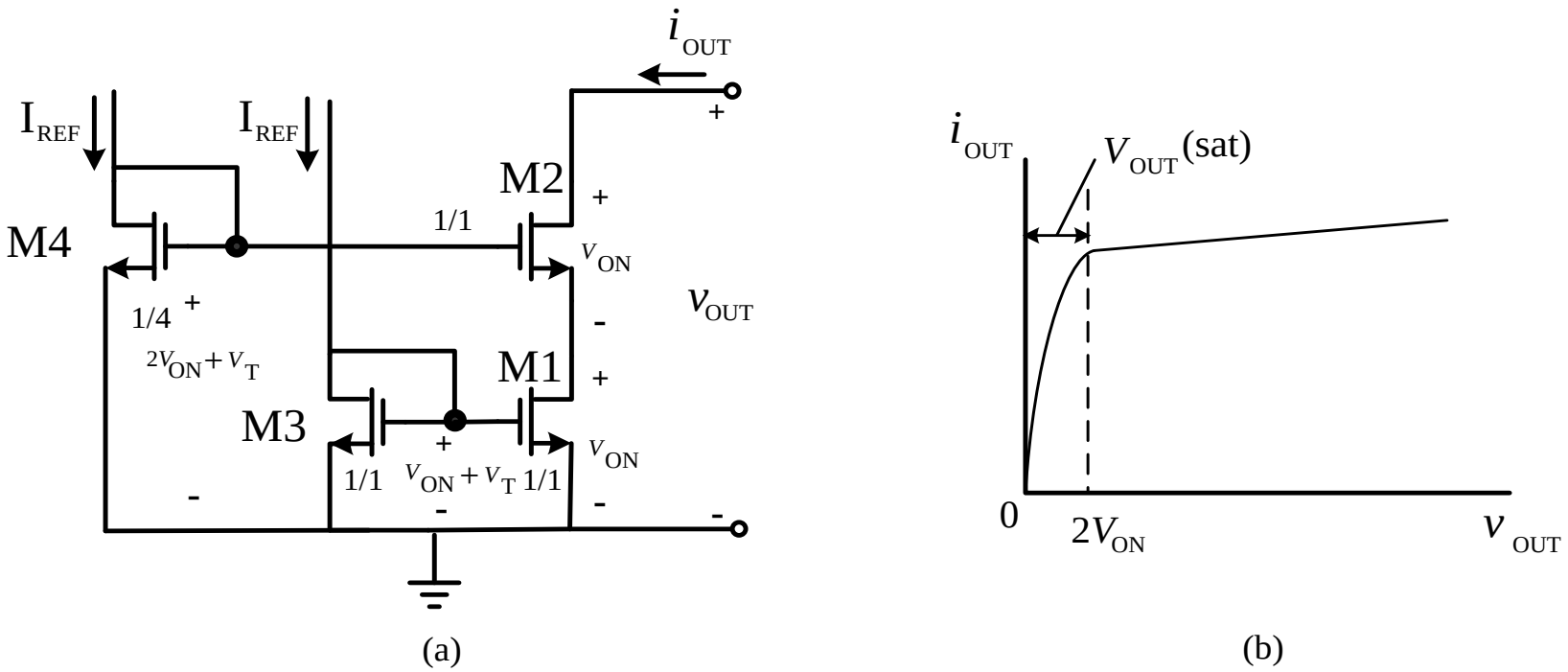


(a) standard cascode current sink; (b) output characteristics of circuit in (a)

$$v_D \geq V_G - V_T$$

$$V_{D2}(\min) = V_{MIN} = V_T + 2V_{ON}$$

High-Swing Cascode



(a) High-swing cascode; (b) Output characteristics of circuit in (a)

High-Swing Cascode

$$I_{REF} = i_{D3} = i_{D4}$$

$$\frac{W_1}{L_1} = \frac{W_3}{L_3} \Rightarrow i_{D1} = i_{D3}$$

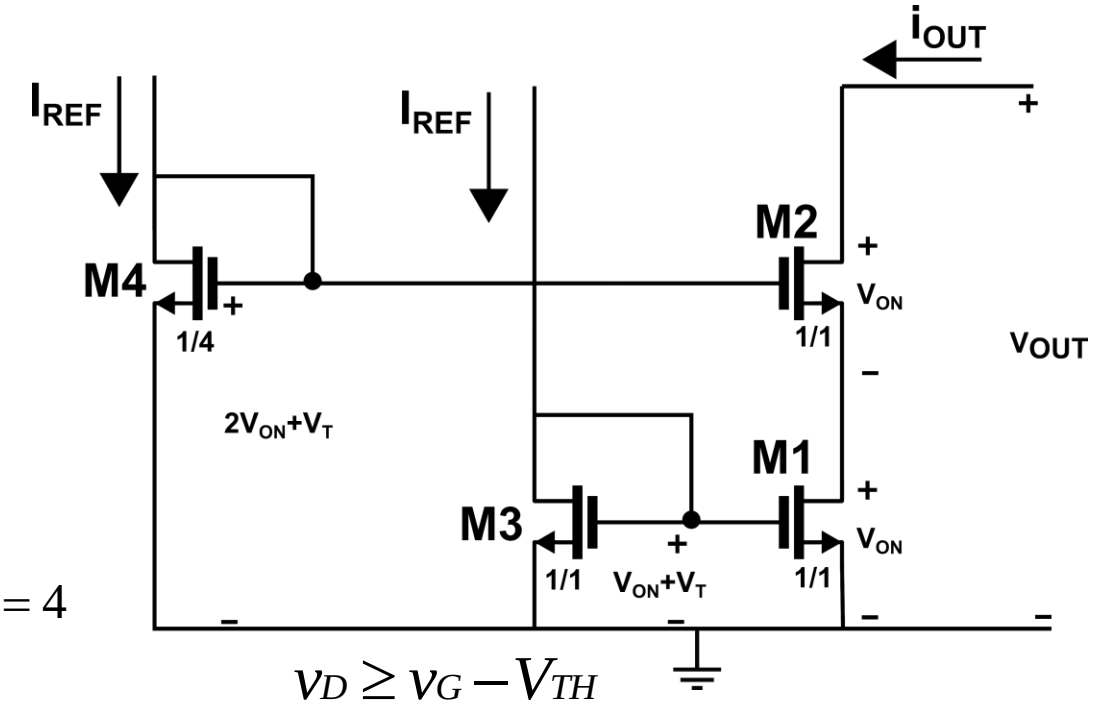
$$\therefore i_{D1} = i_{D4}$$

$$\frac{W_1}{L_1}(V_{ON1})^2 = \frac{W_4}{L_4}(V_{ON4})^2$$

$$\frac{\left(\frac{W_1}{L_1}\right)}{\left(\frac{W_4}{L_4}\right)} = \frac{(V_{ON4})^2}{(V_{ON1})^2} \qquad \frac{\left(\frac{W_1}{L_1}\right)}{\left(\frac{W_4}{L_4}\right)} = 4$$

$$V_{ON4} = 2V_{ON1}$$

$$V_{G4} = V_{TH} + V_{ON4} = V_{TH} + 2V_{ON1}$$



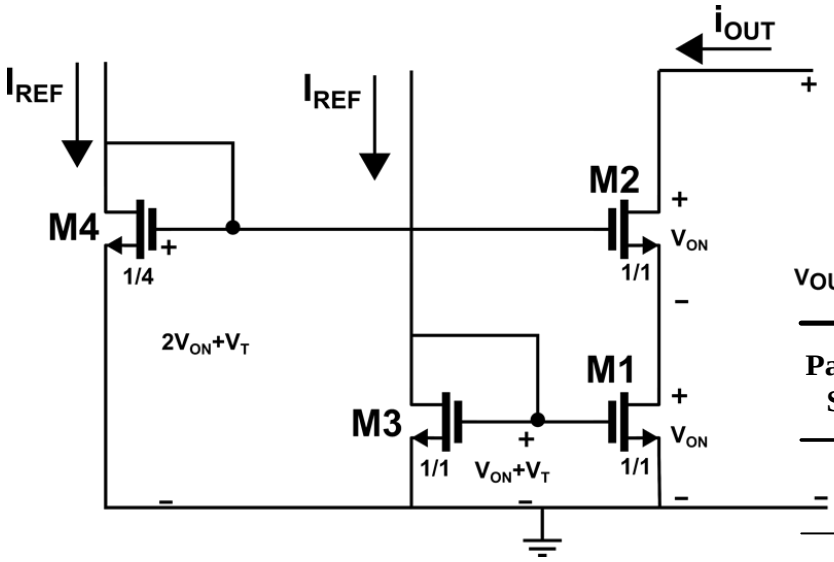
$$v_D \geq v_G - V_{TH}$$

$$V_{D2}(\min) = V_{G2} - V_{TH}$$

$$V_{D2}(\min) = V_{MIN} = 2V_{ON}$$

Example 5.5

Designing the cascode current sink for a given V_{MIN}

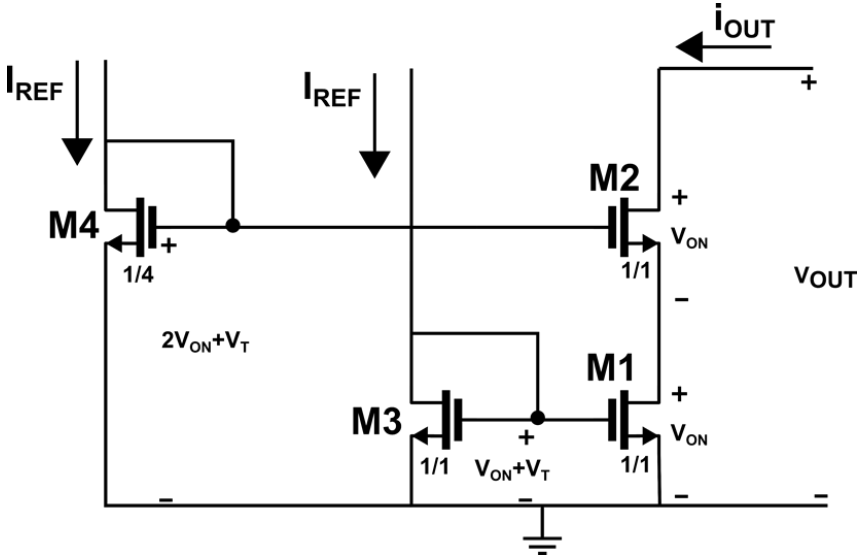


Use the cascode current-sink configuration to design a current sink of 100μA and a V_{MIN} of 1V.

$$K' = (110.0 \pm 10\%)\mu A/V^2$$

Parameter Symbol	Parameter Description	Typical Parameter Value		Units
		n-Channel	p-Channel	
V_{T0}	Threshold voltage ($V_{BS}=0$)	0.7 ± 0.15	-0.7 ± 0.15	V
K'	Transconductance parameter (in saturation)	$110.0 \pm 10\%$	$50.0 \pm 10\%$	$\mu A/V^2$
γ	Bulk threshold parameter	0.4	0.57	$V^{1/2}$
λ	Channel length modulation parameter	0.04 (L=1μm) 0.01 (L=2μm)	0.05 (L=1μm) 0.01 (L=2μm)	V^{-1}
$2\lvert\Phi_F\rvert$	Surface potential at strong inversion	0.7	0.8	V

Solution:



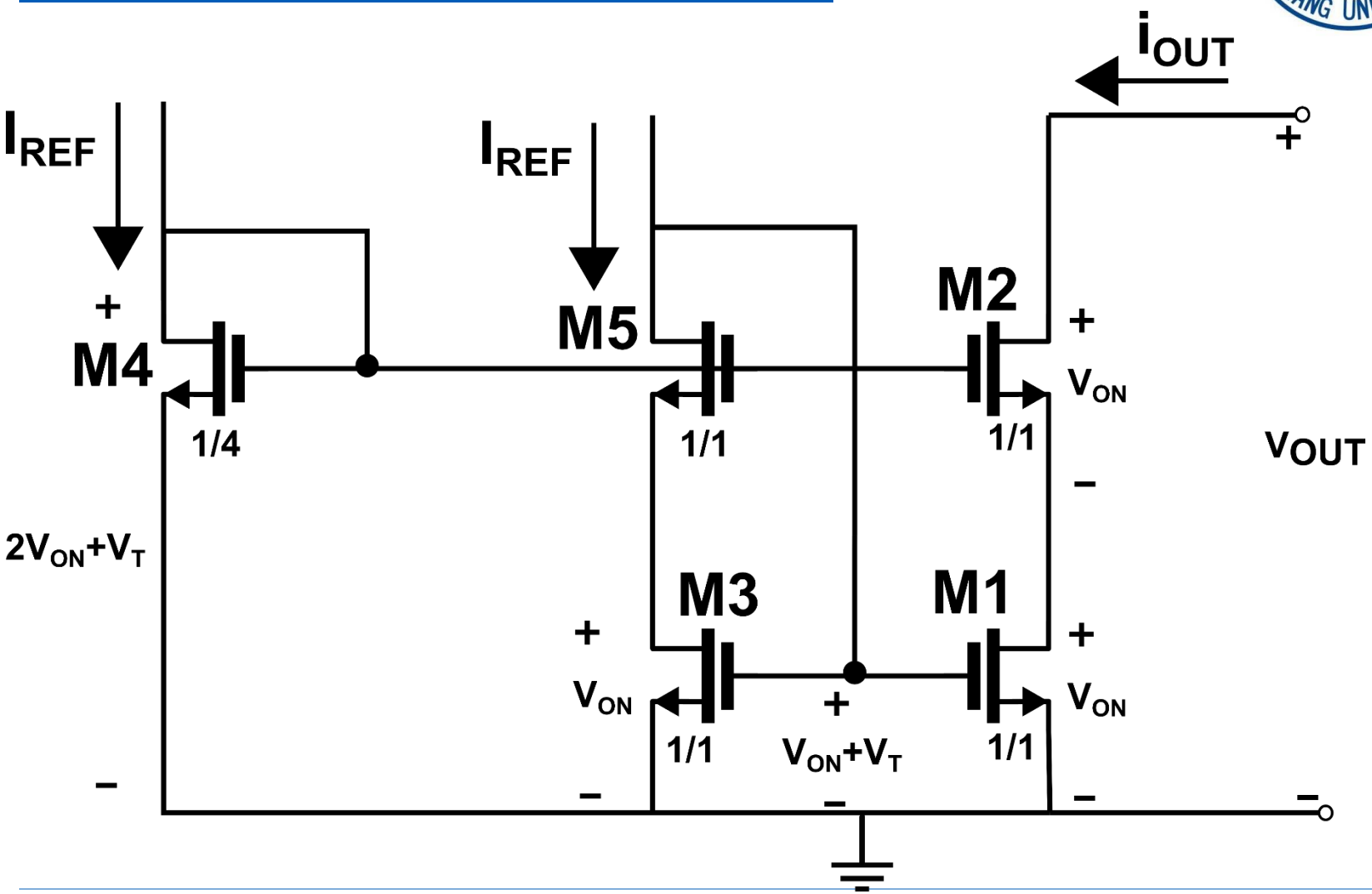
Use the cascode current-sink configuration to design a current sink of 100μA and a V_{MIN} of 1V.

- With V_{MIN} of 1V, choose V_{ON}=0.5V. Using the saturation model, the *W/L* ratio of M1 through M3 can be found from

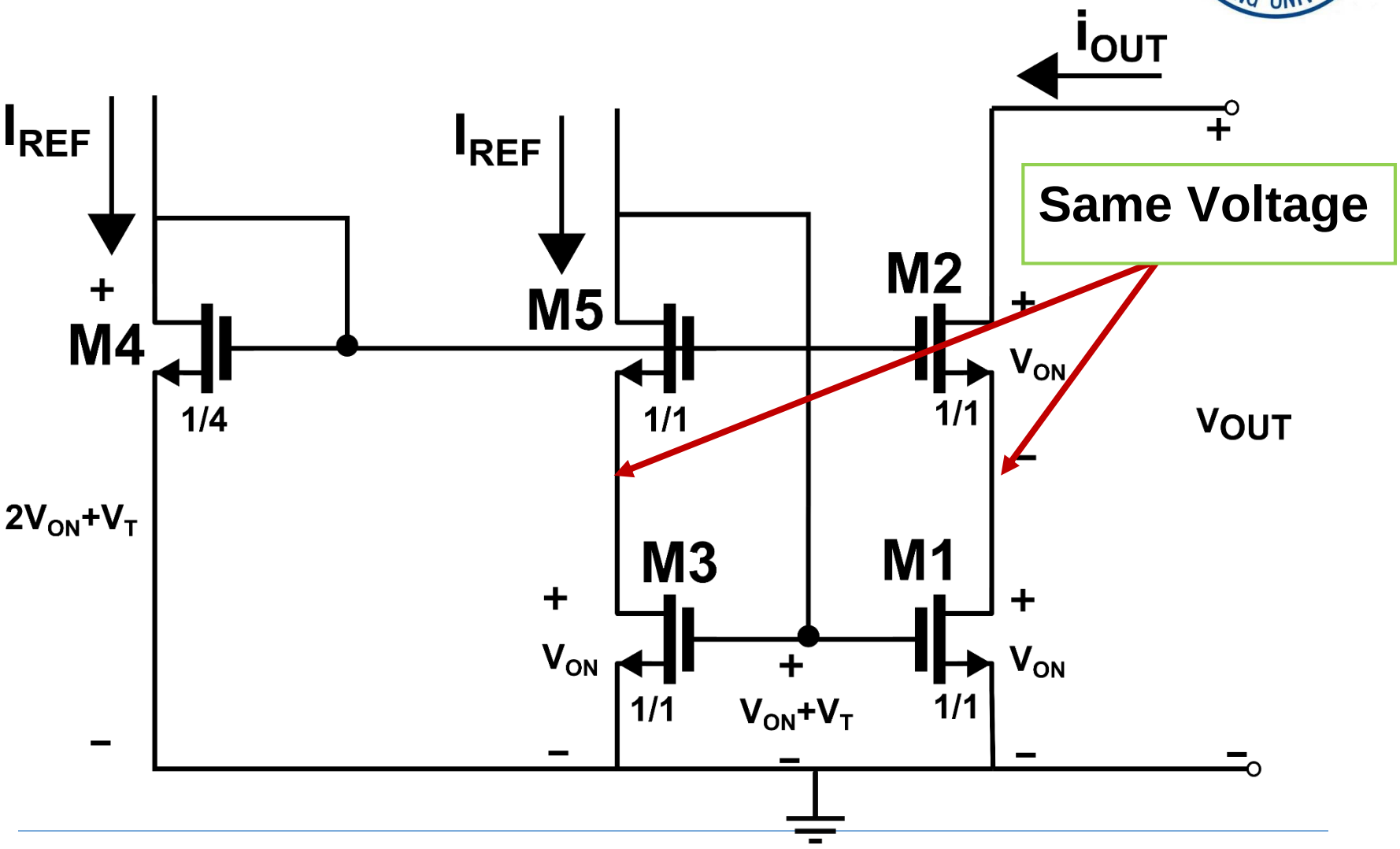
$$\frac{W}{L}=\frac{2i_{OUT}}{K'V^2_{ON}}=\frac{2\times100\times10^{-6}}{110\times10^{-6}\times0.25}=7.27$$

- The *W/L* ratio of M4 will be one-quarter this value or 1.82.

Improved High-swing Cascode



Improved High-swing Cascode



Improved High-swing Cascode

$$I_1 = \frac{K'}{2}\frac{W}{L}(V_{GS1} - V_{TH})^2 = \frac{K'}{2}\frac{W}{L}V_{ON}{}^2$$

$$\because I_1 = I_5 \quad \frac{K'}{2}\left(\frac{1}{4}\frac{W}{L}\right)(V_{ON5})^2 = \frac{K'}{2}\frac{W}{L}(V_{ON1})^2$$

$$\frac{1}{4}(V_{ON5})^2 = (V_{ON1})^2$$

$$V_{ON5} = 2V_{ON1} = 2V_{ON}$$

so $V_{GS5} = V_{TH} + 2V_{ON} = V_{G3}$

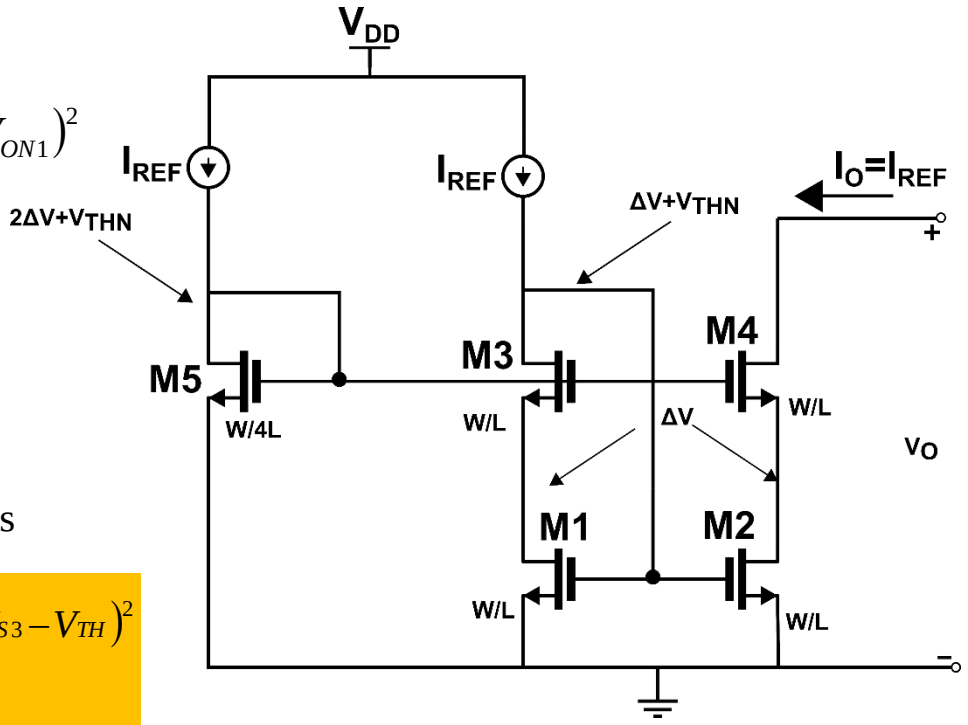
$\because I_1 = I_3$ and M1, M3 have the same sizes

$$I_3 = \frac{1}{2}K'\frac{W}{L}(V_{GS3} - V_{TH})^2 = \frac{1}{2}K'\frac{W}{L}(V_{G3} - V_{S3} - V_{TH})^2$$

$$= \frac{1}{2}K'\frac{W}{L}(V_{TH} + 2V_{ON} - V_{S3} - V_{TH})^2$$

$$= \frac{1}{2}K'\frac{W}{L}(2V_{ON} - V_{S3})^2$$

$$= I_1 = \frac{1}{2}K'\frac{W}{L}V_{ON}{}^2$$



That means $2V_{ON} - V_{S3} = V_{ON}$

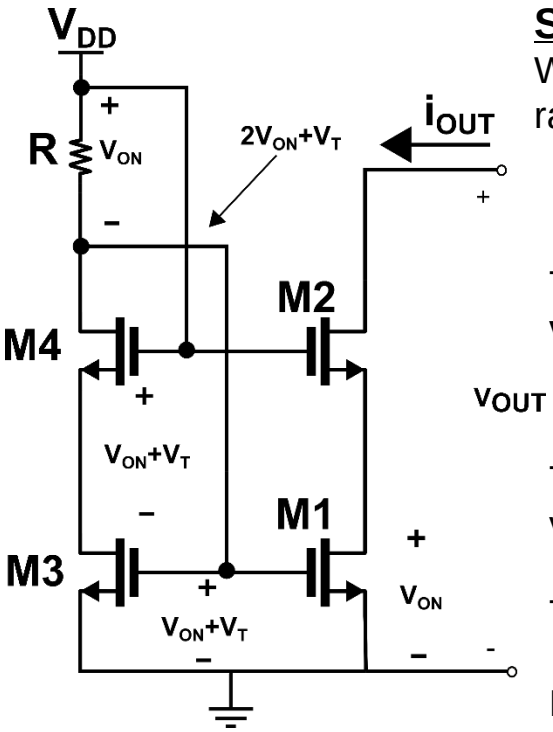
$\therefore V_{S3} = V_{ON}$

and also $V_{S4} = V_{ON}$

Example 5.6

Designing the self-biased high-swing cascode current sink for a given V_{MIN}

Design a current sink of 250μA and a V_{MIN} of 0.5 V. (what? W/L and R)
Assume the device parameters of Table 5.1-2.



Self-biased
high-swing cascode current

Solution:

With V_{MIN} of 0.5 V, choose V_{ON}=0.25V. Using the saturation model, the ***W/L*** ratio of M1 and M3 can be found from

$$\frac{W}{L}=\frac{2i_{OUT}}{K'V^2_{ON}}=\frac{2\times250\times10^{-6}}{110\times10^{-6}\times0.0626}=72.73$$

The back-gate bias on M2 and M4 is -0.25 V. Therefore, the **threshold voltage** for M2 and M4 is calculated to be

$$V_{TH}=0.7+0.4\left(\sqrt{0.25+0.7}-\sqrt{0.7}\right)=0.755$$

Taking into account the increased value of the threshold voltage, the gate voltage of M4 and M2 is

$$V_{G4}=0.755+0.25+0.25=1.255$$

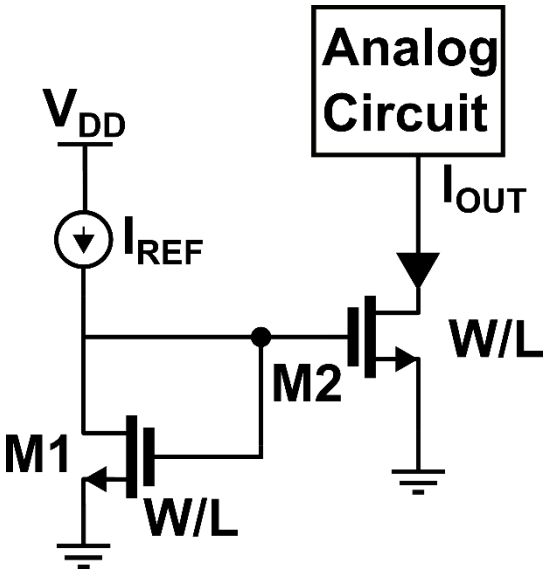
The gate voltage of M1 and. M3 is

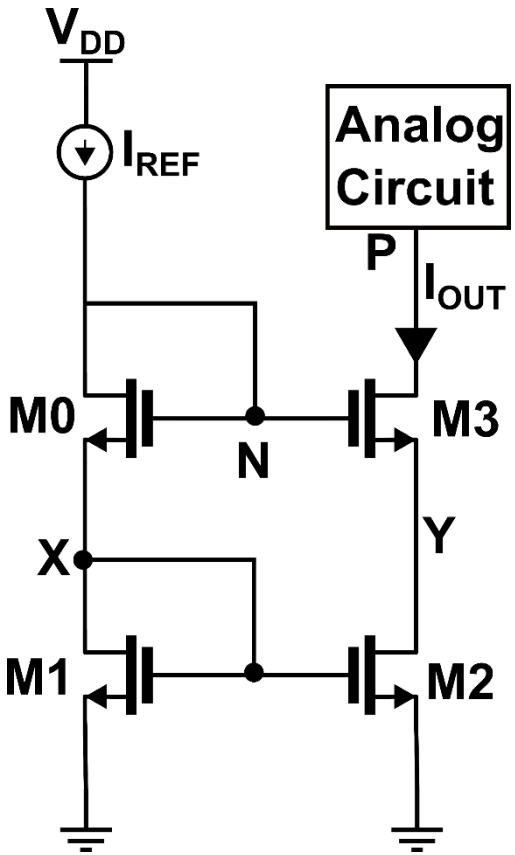
$$V_{G1}=0.70+0.25=0.95$$

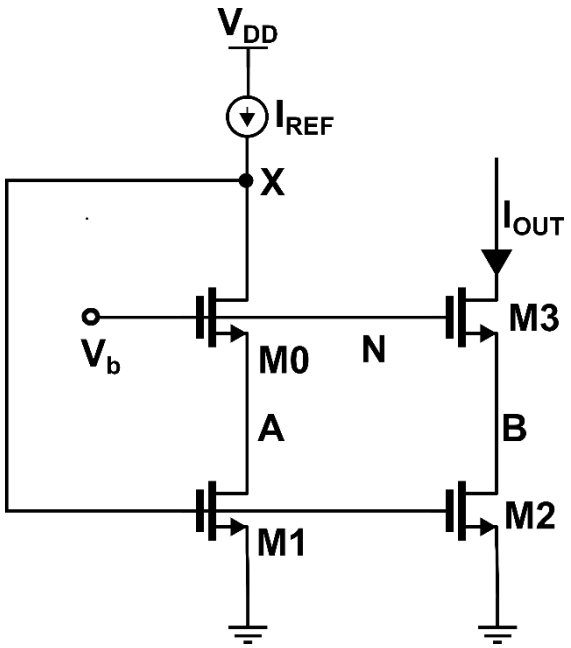
Both terminals of the resistor are now defined so that **the required resistance value** is easily calculated to be

$$R=\frac{V_{G4}-V_{G1}}{250\times10^{-6}}=\frac{1.255-0.95}{250\times10^{-6}}=1220\Omega$$

Summary


Analog
Circuit
V_{DD}
I_{REF}
I_{OUT}
W/L
M2
M1
W/L


V_{DD}
I_{REF}
Analog
Circuit
P
I_{OUT}
M0
N
M3
Y
X
M1
M2


V_{DD}
I_{REF}
X
I_{OUT}
V_b
M0
N
M3
A
B
M1
M2

Today's Summary

- MOS Switch & Charge Feedthrough
- MOS Diode/Active Resistor

  Gain = gm * rop//ron
- Current Sinks and Sources

  Cascode -> ro = (gm1 * ron1) ro2

集成电路原理与设计

5.模拟基本单元

宋爽

shuangsonghz@zju.edu.cn