Exercise 2

2-1. Consider the circuit of Fig.2.1.

a) Using the simple model with $V_{Don} = 0.7V$, solve for I_D;

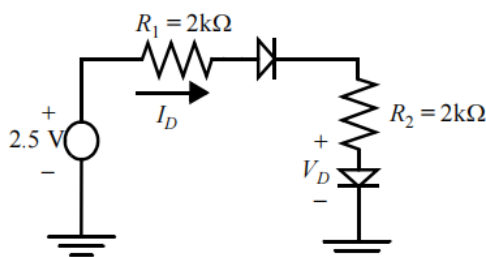b) Find I_D and V_D using the ideal diode equation. Use $I_S = 10^{-14}$ A and T=300 K.

Fig.2.1

Answer:

a. $I_D = \frac{V_{in} - 2*V_{Don}}{R_1 + R_2} = \frac{2.5 - 2*0.7}{4K\Omega} = 275uA$

b. $I_S = 10^{-14}A, T = 300K, V_{Don} = 0.7V. I_D = I_S \times (e^{\frac{V_D q}{KT}} - 1)$ where $\frac{KT}{q} = 26mV@300K$

$I_D = \frac{V_{in} - 2 \cdot V_{Don}}{R_1 + R_2} = I_S \times (e^{\frac{V_D q}{KT}} - 1)$ iterating on this expression we can obtain $\frac{V_D}{I_D} = \frac{0.628V}{311uA}$

2-2. For the circuit in Fig.2.2, V_s=3.3 V. Assume $A_D = 12$ μm^2, $\varphi_0 = 0.65$ V, and m= 0.5, $N_A = 2.5 \times 10^{16}$ and $N_D = 5 \times 10^{15}$.

a) Is the diode forward- or reverse-biased?

b) Find I_D and V_D;

c) Find the depletion region width, W_j, of the diode;

d) Use the parallel-plate model to find the junction capacitance, C_j;

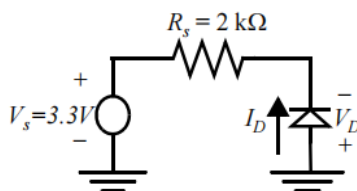e) Set $V_s = 1.5$ V. Again using the parallel-plate model, explain qualitatively why C_j increases.

Fig.2.2

Answer:

a. Reverse biased

b. $I_D = I_{REV} = -I_S \approx 0, V_D = -V_S = -3.3V$

c. $W_j = \sqrt{\frac{2 \cdot \varepsilon_{si}}{q} \times \frac{N_A + N_D}{N_A N_D} \times (\varphi_0 - V_D)}, q = 1.6 \times 10^{-19} C, V_D = -V_S = -3.3V,$

$\varepsilon_{si} = 11.7\varepsilon_0 = 1.035 \times 10^{-10} F/m, N_A = 2.5 \times \frac{10^{16}}{cm^3}, N_D = 5 \times \frac{10^{15}}{cm^3}.$

$W_j = 1.107 \times 10^{-4} cm.$

d. $C_j = \frac{\varepsilon_{si} \cdot A_D}{W_j}, A_D = 12 \times 10^{-8} cm^2, C_j = 1.12 \times 10^{-15} F.$

e. $V_{SNEW} = 1.5V < V_{SOLD} = 3.3V$. The new voltage reduces the reverse bias of the PN junction, hence the width of the depletion region, W_j, decreases. As you bring the plates of capacitor together, the capacitance increases.

2-3. Fig.2.3 shows NMOS and PMOS devices with drains, source, and gate ports annotated. Determine the operation region (saturation, linear, or cut-off) and the drain current I_D for each of the biasing configurations given in table. Assume the model parameters from Table.2.1, $V_{BS}=0$ and $W/L = 1$, $L=1um$, fill the table
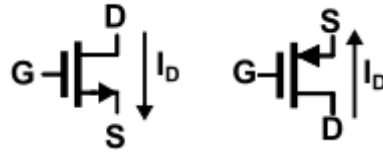

Fig.2.3

Answer:

	V_{GS}(V)	V_{DS}(V)	Operation region	I_D
NMOS	2.5	2.5	saturation	392.04uA
	3.3	2.2	linear	726uA
	0.6	0.1	cut-off	0
PMOS	-0.5	-1.25	cut-off	0
	-2.5	-1.8	saturation	176.58uA
	-2.5	-0.7	linear	101.5uA

NMOS :1. Saturation $I_D = k'_n \frac{W}{L}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS}) = 392.04uA;$

2. linear $I_D = 2 \times k'_n \frac{W}{L}\left((V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}\right) = 726uA;$

3. cut-off $I_D = 0,$

PMOS : 1. cut-off $I_D = 0,$

2. Saturation $I_D = k'_p \frac{W}{L}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS}) = 176.58uA$

3. linear $I_D = 2 \times k'_p \frac{W}{L}\left((V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}\right) = 101.5uA$

2-4. An NMOS device is plugged into the test configuration shown below in Fig .2.4 The input V_{in} is 2V. The current source draws a constant current of 50 µA. R is a variable resistor between 10kΩ and 30 kΩ. Transistor M1 has following transistor parameters: $k' = 110\mu$ V/A^2, $V_T = 0.7$V, and $V_{DSAT} = 0.6$V, and has a $W/L = 2.5\mu m/0.25$um. For simplicity, the body effect and channel length modulation can be neglected, i.e $\lambda=0$, $\gamma=0$.

a) When $R = 10$kΩ find the operation region, V_D and V_S.

b) For the case of $R = 10$kΩ, would V_S increase or decrease if $\lambda \neq 0$. Explain qualitatively.

Fig.2.4

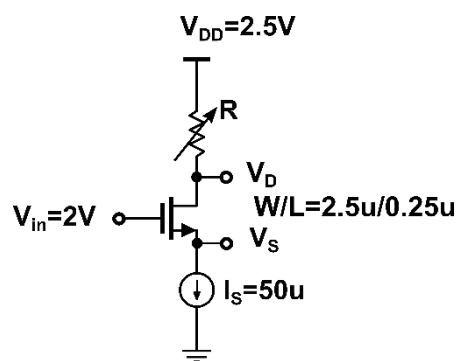**Answer:**

a. When $R = 10K$, $V_D = V_{DD} - IR = 2.5 - 50 \times 10^{-6} \times 10^4 = 2.5 - 0.5 = 2V$. Assume the device is in

saturation $I_D = k'_n \dfrac{W}{L}(V_{GS} - V_{TH})^2 = 50uA$ find $V_{GS} - V_{TH} = 0.213V$, so $V_{GS} = 0.213 +$

$0.7V = 0.913V$,

$V_S = 1.087V$. $V_{GS}=0.913V$, $V_{DS}=1.087V$ device in the saturation.

b. Increase. V_D is fixed due to constant current. $1 + \lambda V_{DS}$ form would try to increase the current more then 50uA, thus V_{GS} needs to reduce by increase V_S.

2-5. Find the small-signal model (g_m, g_{mb}, g_{ds}) for an n-channel transistor with the drain at 4 V, gate at 4 V, source at 2 V, and the bulk at 0 V. Assume the model parameters from Table.2.1, and $W/L = 10$ µm/1 µm.

Answer:

$$V_T = V_{T0} + \gamma \left[\sqrt{2|\Phi_F| + v_{SB}} - \sqrt{2|\Phi_F|} \right]$$

$$V_T = 0.7 + 0.4\left[\sqrt{0.7 + 2.0} - \sqrt{0.7}\right] = 1.02$$

$$I_D = \frac{K'W}{L}(v_{GS} - v_T)^2(1 + \lambda v_{DS})$$

$$I_D = 110 \times 10^{-6} \times 10 \times (2 - 1.02)^2(1 + 0.04 \times 2) = 1140 \times 10^{-6}$$

$$g_m = \sqrt{4\frac{K'W}{L}I_D}$$

$$g_m = \sqrt{4 \times 110 \times 10^{-6} \times 10 \times 1140 \times 10^{-6}} = 2.24 \times 10^{-3}$$

$$g_{mb} = g_m \frac{\gamma}{2(2|\Phi_F| + V_{SB})^{\frac{1}{2}}}$$

$$g_{mb} = 2.24 \times 10^{-3} \frac{0.4}{2(0.7 + 2.0)^{\frac{1}{2}}} = 273 \times 10^{-6}$$

$$g_{ds} = \frac{\lambda I_D}{1 + \lambda V_{DS}}$$

$$g_{ds} = 1140 \times 10^{-6} \times 0.04 \div 1.08 = 42.22 \times 10^{-6}$$

Thinking Questions(optional)

2-6. Show that two MOS transistors connected in parallel with channel widths of W_1 and W_2 and identical channel lengths of L can be modeled as one equivalent MOS transistor whose width is $W_1 + W_2$ and whose length is L, as shown in Fig.2.6 Assume the transistors are identical except for their channel widths.
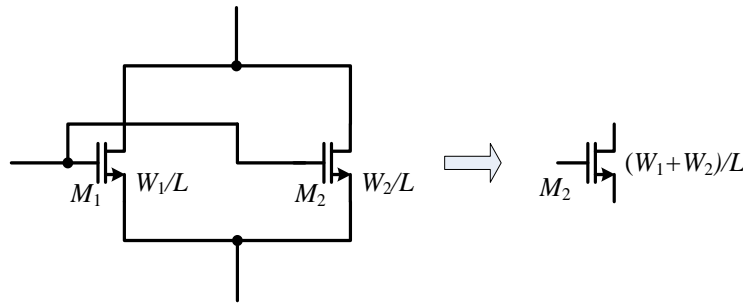

Fig.2.6

Answer:

For $V_{DS} \leq V_{GS} - V_{TH}$

$$I_{D1} = \mu C_{OX} \frac{W_1}{L} [(V_{GS} - V_{TH})V_{DS} - \frac{1}{2} V_{DS}^2]$$

$$I_{D2} = \mu C_{OX} \frac{W_2}{L} [(V_{GS} - V_{TH})V_{DS} - \frac{1}{2} V_{DS}^2]$$

......

$$I_{Dn} = \mu C_{OX} \frac{W_n}{L} [(V_{GS} - V_{TH})V_{DS} - \frac{1}{2} V_{DS}^2]$$

$$\therefore I_D = I_{D1} + I_{D2} + \ldots + I_{Dn} = \mu C_{OX} \frac{W_1 + W_2 + \ldots + W_n}{L} [(V_{GS} - V_{TH})V_{DS} - \frac{1}{2} V_{DS}^2]$$

For $V_{DS} \geq V_{GS} - V_{TH}$

$$I_D = I_{D1} + I_{D2} + \ldots + I_{Dn} = \frac{1}{2} \mu C_{OX} \frac{W_1 + W_2 + \ldots + W_n}{L} (V_{GS} - V_{TH})^2$$

Thus the equivalent length = L and the equivalent width = $W_1 + W_2 + \ldots + W_n$.

2-7. Show that two MOS transistors connected in series with channel lengths of L_1 and L_2 and identical channel widths of W can be modeled as one equivalent MOS transistor whose width is W and whose length is L_1+L_2, as shown in Fig. 2.7. Assume the transistors are identical except for their channel lengths. Ignore the body effect and channel-length modulation.
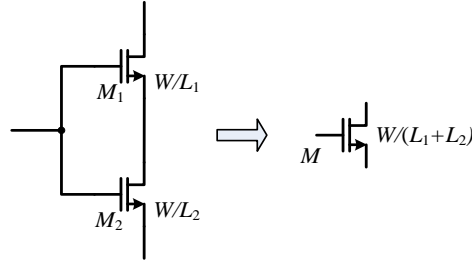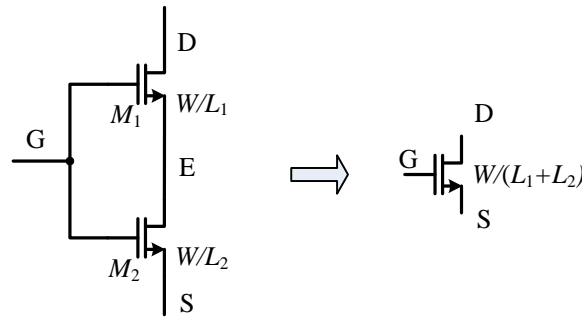

Fig.2.7

Answer:

(1) When $V_{GS}<V_{TH}$ and $V_{GE}<V_{GS}<V_{TH}$, the MOSFETs are in cut off.

(2) While M1 operates in triode ($V_{DE} < V_{GE} -V_{THN}$), that is equivalent to $V_{DE} +V_{ES} < V_{GE} + V_{ES-}$ V_{THN}, i.e. $V_{DS} < V_{GS} -V_{THN}$.

Thus M2 operates in triode, too.

Thus

$$I_{D1} = \mu_n C_{OX} \frac{W}{L_1}[(V_{GE} -V_{TH})V_{DE} -\frac{1}{2}V_{DE}^2] \quad (1)$$

$$I_{D2} = \mu_n C_{OX} \frac{W}{L_2}[(V_{GS} -V_{TH})V_{ES} -\frac{1}{2}V_{ES}^2] \quad (2)$$

Since

$$V_{DS} = V_{DE} +V_{ES} \quad (3)$$

$$V_{GE} = V_{GS} -V_{ES} \quad (4)$$

$$I_{D1} = I_{D2} = I_D \quad (5)$$

It can be derived from equations (1), (2), (3), (4) and (5) that

$$(V_{GS} - V_{TH})V_{ES} - \frac{1}{2}V_{ES}{}^2 = \frac{L_2}{L_1}[(V_{GS} - V_{TH} - V_{ES})(V_{DS} - V_{ES}) - \frac{1}{2}(V_{DS} - V_{ES})^2]$$

$$= \frac{L_1}{L_1 + L_2}[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}{}^2]$$

So we can get $I_D = \mu_n C_{OX} \dfrac{W}{L_1 + L_2}[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}{}^2]$

(3) While M1 operates in saturation ($V_{DE} > V_{GE} - V_{THN}$). It means $V_{DE} + V_{ES} > V_{GE} + V_{ES} - V_{THN}$, i.e. $V_{DS} > V_{GS} - V_{THN}$.

$V_E = V_G - V_{GE} < V_G - V_{THN}$, it means $V_{ES} < V_{GS} - V_{THN}$. M2 operates in triode.

So

$$I_{D1} = \frac{1}{2}\mu_n C_{OX} \frac{W}{L_1}(V_{GE} - V_{TH})^2 \quad (1)$$

$$I_{D2} = \frac{1}{2}\mu_n C_{OX} \frac{W}{L_2}[2(V_{GS} - V_{TH})V_{ES} - V_{ES}{}^2] \quad (2)$$

$$V_{DS} = V_{DE} + V_{ES} \quad (3)$$

$$V_{GE} = V_{GS} - V_{ES} \quad (4)$$

$$I_{D1} = I_{D2} = I_D \quad (5)$$

It can be derived from equations (1), (2), (3), (4) and (5) that

$$I_D = \frac{1}{2}\mu_n C_{OX} \frac{W}{L_1 + L_2}(V_{GS} - V_{TH})^2$$

That just like a MOSFET operating in saturation, which has a length of $L_1 + L_2$ and a width of W. It can be deducted similarly that n MOSFETs in series acts as a MOSFET with an aspect ratio of $W/(L_1 + L_2 + \dots L_n)$.

Table.2.1

Parameter Symbol	Parameter Description	Typical Parameter Value		Units
		n-Channel	p-Channel	
V_{TO}	Threshold voltage ($V_{BS}=0$)	0.7	-0.7	V
K'	Transconductance parameter (in saturation)	110.0	50.0	$\mu A/V^2$
γ	Bulk threshold parameter	0.4	0.57	$V^{1/2}$
λ	Channel length modulation parameter	0.04 (L=1µm) 0.01 (L=2µm)	0.05 (L=1µm) 0.01 (L=2µm)	V^{-1}
$2|\Phi_F|$	Surface potential at strong inversion	0.7	0.8	V

$$*K' = \frac{1}{2}\mu C_{ox}$$