习 题 2

2-1. An N-type current source folded as in Fig. 2.1 must operate with drain-source voltage V_{DS} as low as 0.4V. I_D is 0.5mA. Assume that L=0.5μm and E=3μm.
(a)If the minimum required output resistance is 20 KΩ, determine the width of the device.
(b)With the width in (a), calculate the gate-source, gate-drain, and drain-substrate capacitance. Use the parameters in Table 2.1 and C_{ox}=3.8×10^{-3} F/m^2, V_R=0.6V.

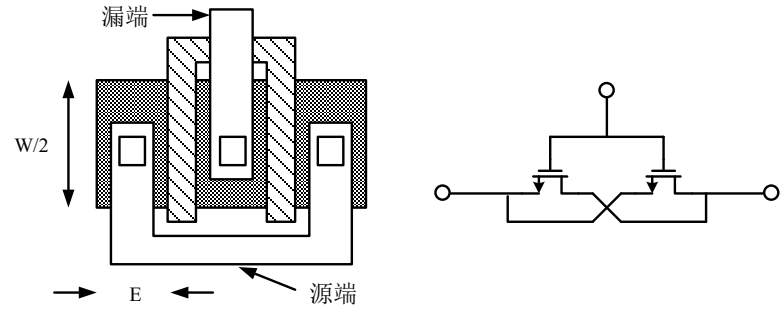


Figure 2-1

Answer:

(a)

$$\begin{cases} r_o = \dfrac{1}{\lambda I_D} = 20K\Omega \\ I_D = 0.5mA \end{cases} \quad \Rightarrow \quad \lambda=0.1$$

From the table2.1,

$$L_{eff} = L - 2L_D = 0.5\mu m - 2\times 0.08\mu m = 0.34\mu m$$

Calculating W

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L_{eff}}(V_{GS}-V_{TH})^2, \quad V_{GS}\text{-}V_{TH}=V_{DSAT}=0.4V$$

$$\frac{W}{L_{eff}} = \frac{I_D}{\frac{1}{2}\mu_n C_{ox}(V_{GS}-V_{TH})^2} = \frac{0.5\times 10^{-3}}{\frac{1}{2}\times 350\times 10^{-4}\times 3.8\times 10^{-3}\times 0.4^2} = 47$$

$$\therefore\ W = 47L_{eff} = 16\mu m$$

(b)

$$C_{j0} = 0.56\times 10^{-3}\ F/m^2, C_{jsw0} = 0.35\times 10^{-11}\ F/m, m_j = 0.45, m_{jsw} = 0.2,$$
$$C_{ov} = 0.4\times 10^{-9}\ F/m, W = 16\mu m, L = 0.5\mu m, L_D = 0.08\mu m, E = 3\mu m,$$
$$V_R = 0.6V, 2\Phi_F = 0.9V, C_{ox} = 3.8\times 10^{-3}\ F/m^2, P_{SUB} = 9\times 10^8 m^{-3},$$

$$\varepsilon_{si} = 11.9 \times 8.85 \times \frac{10^{-12}F}{m}, q = 1.6 \times 10^{-19}C$$

$$C_j = \frac{C_{j0}}{(1 + V_R/2\Phi_F)^{m_j}} = 4.45\times10^{-4}\frac{F}{m^2}, C_{jsw} = \frac{C_{jsw0}}{(1 + V_R/2\Phi_F)^{m_{jsw}}} = 3.16\times10^{-12}\ F/m$$

$$L_{eff} = L - 2L_D \qquad C_d = WL_{eff}\sqrt{\frac{q\varepsilon_{si}P_{SUB}}{4\Phi_F}}$$

$$C_{DB} = \frac{W}{2}EC_j + 2\left(\frac{W}{2} + E\right)C_{jsw} = 10.7fF$$

$$C_{SB} = 2\left(\frac{W}{2}EC_j + 2\left(\frac{W}{2} + E\right)C_{jsw}\right) = 21.5fF$$

$$C_{GD} = 2\left(\frac{W}{2}C_{ov}\right) = 6.4fF$$

$$C_{GS} = \frac{2}{3}WL_{eff}C_{ox} + WC_{ov} = 20.2fF$$

C_{GB}：栅-衬底电容在三极管区和饱和区通常被忽略，因为反型层在栅和衬底之间起了“屏蔽”的作用。换句话说，如果栅电压发生变化，电荷是由源和漏提供，而不是由衬底提供。

2-2. The layout of an n-channel MOSFET is shown in Fig.2.2. What is this device's channel width and length?

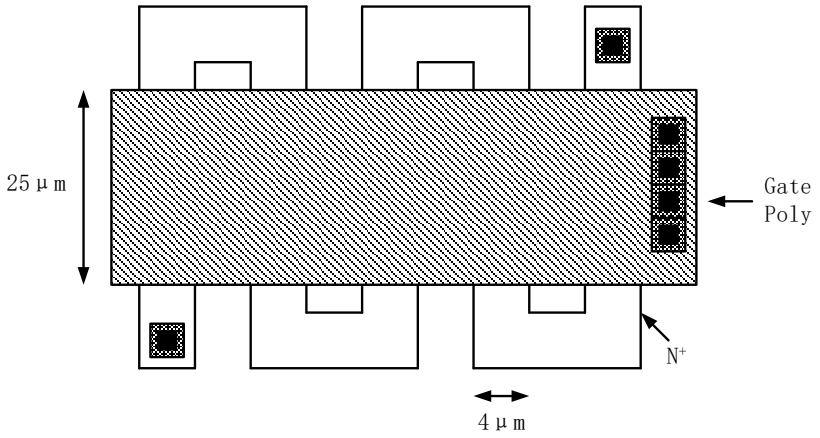


Figure 2.3

Answer:

$$Length = 5\times25\mu m = 125\mu m$$

$$Width = 4\mu m$$

2-3. A “ring” MOS structure is shown in Fig. 2.3. Explain how the device operations and estimate its equivalent aspect ratio. Calculate the drain junction capacitance of the structure (using C_j and C_{jsw})

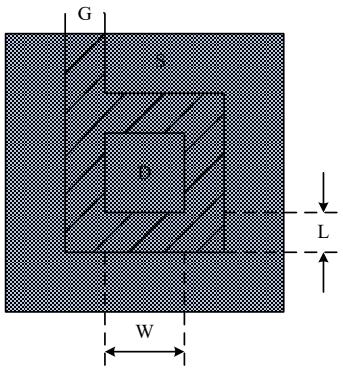


Figure 2.4

Answer:

Width/length ratio is 4W/L

$$C_{DB} = W^2 C_j + 4WC_{jsw}$$

2-4. An NMOS device operating in the subthreshold region has a ζ of 1.5. What variation in V_{GS} results in a tenfold change in I_D? If I_D = 10 μA, what is g_m?

Answer:

$$I_D = I_0 \exp\frac{V_{GS}}{\xi V_T}$$

$$\frac{I_{D2}}{I_{D1}} = \exp\frac{V_{GS2}-V_{GS1}}{\xi V_T}, \quad \frac{I_{D2}}{I_{D1}} = 10 \Rightarrow \Delta V_{GS} - \xi V_T \ln 10$$

$$\Delta V_{GS} = 1.5 \times \ln 10 \times 26\text{mV} = 89.8\text{mV}$$

$$g_m = \frac{I_D}{\xi V_T} = \frac{10\mu A}{1.5\times 26^{mV}} = 0.26\text{mA/V}$$

2-5. Consider an NMOS device with V_G = 1.5 V and V_S = 0. Explain what happens if we continually decrease V_D below zero or increase V_{sub} above zero.

Answer:

a) If we decrease V_D below zero, Source and drain exchange their roles and device operates in the triode region.

b) If we increase V_B, V_{TH} decreases, because $\Delta V_{TH} = \gamma\left(\sqrt{2\Phi_F - V_B} - \sqrt{2\Phi_F}\right)$ is negative. Therefore, I_D increases.

2-6. The layout of a circuit fabricated in n-well technology is shown as Fig.2.6. Give the corresponding schematic and mark the W/L sizes of each transistor. Then give the output expression of the schematic (use A, B and C). Assume L=2λ, λ=0.4μm.

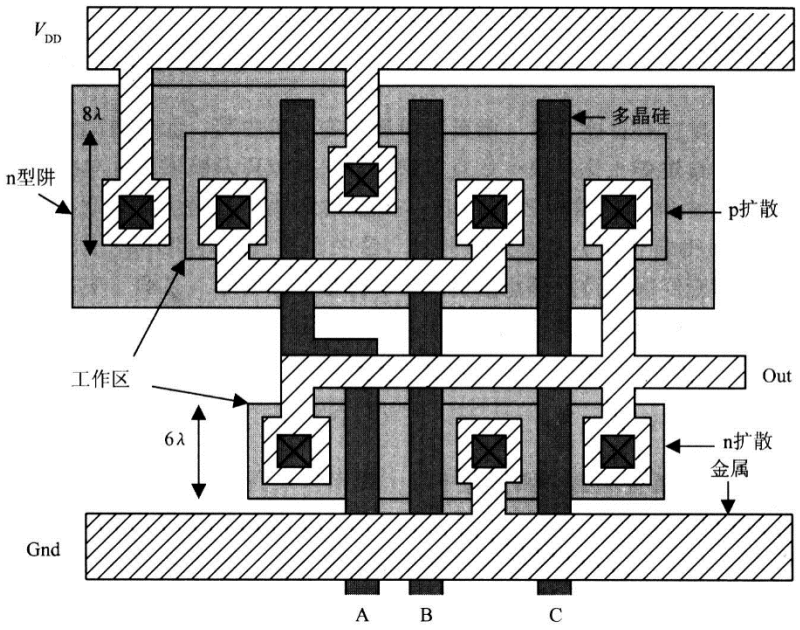
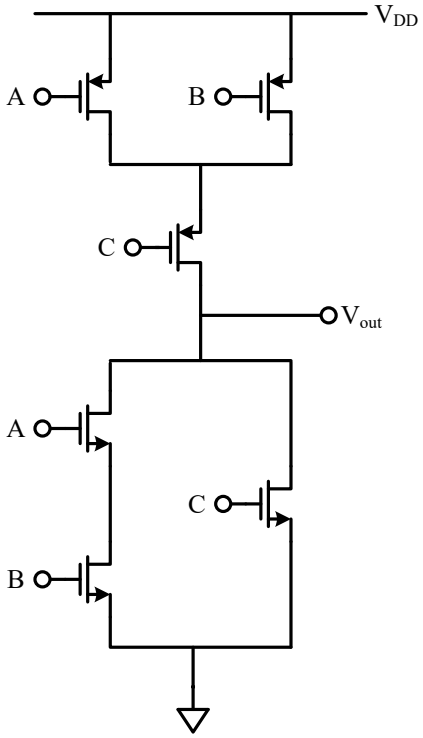


Figure 2.5

Answer:

Schematic



$$Out=\overline{AB+C}$$

W/L of N-MOSFET:

$$\frac{6\lambda}{2\lambda}=\frac{6\times 0.4}{2\times 0.4}=\frac{2.4}{0.8}$$

W/L of P-MOSFET:

$$\frac{8\lambda}{2\lambda}=\frac{8\times 0.4}{2\times 0.4}=\frac{3.2}{0.8}$$

Table 2.1

NMOS Model			
LEVEL=1	VTO=0.7	GAMMA=0.45	PHI=0.9
PSUB=9e+14	LD=0.08e-6	UO=350	LAMBDA=0.1
TOX=9e-9	PB=0.9	CJ=0.56e-3	CJSW=0.35e-11
MJ=0.45	MJSW=0.2	CGDO=0.4e-9	JS=1.0e-8
PMOS Model			
LEVEL=1	VTO=-0.8	GAMMA=0.4	PHI=0.8
PSUB=5e+14	LD=0.09e-6	UO=100	LAMBDA=0.2
TOX=9e-9	PB=0.9	CJ=0.94e-3	CJSW=0.32e-11
MJ=0.5	MJSW=0.3	CGDO=0.3e-9	JS=0.5e-8

上表给出的是 0.5μm 工艺 level 1 MOS SPICE 模型参数的典型值，其中的参数定义如下：

VTO:	VSB=0 时的阈值电压	（单位：V）
GAMMA:	体效应系数	（单位：$V^{1/2}$）
PHI:	$2\Phi_F$	（单位：V）
TOX:	栅氧厚度	（单位：m）
NSUB:	衬底掺杂浓度	（单位：cm^{-3}）
LD:	源/漏侧扩散长度	（单位：m）
UO:	沟道迁移率	（单位：cm2/(v/s)）
LAMBDA:	沟道长度调制系数	（单位：V^{-1}）
CJ:	单位面积的源/漏结电容	（单位：F/m^2）
CJSW:	单位长度的源/漏侧壁结电容	（单位：F/m）
PB:	源/漏结内建电势	（单位：V）
MJ:	CJ 公式中的幂指数	（无单位）
MJSW:	CJSW 等式中的幂指数	（无单位）
CGDO:	单位宽度的栅/漏交叠电容	（单位：F/m）
CGSO:	单位宽度的栅/源交叠电容	（单位：F/m）
JS:	源/漏结单位面积的漏电流	（单位：A/m^2）