集成电路原理与设计

3.器件模型二

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Syllabus

课数	内容	课数	内容
1	导论	9	差分放大器
2	器件模型一	10	运算放大器
3	器件模型二	11	逻辑门
4	工艺流程	12	组合逻辑
5	模拟基本单元	13	时序逻辑
6	电流镜与基准	14	加法器/乘法器
7	单级放大器	15	集成电路专题讲座一
8	课堂测验	16	集成电路专题讲座二

Recall the last chapter (1)

- **Diode and its application for ESD devices**
- **I/V curve and operation region of MOSFET**

Linear: $$I_D = \mu_n C_{OX} \frac{W}{L}\left[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

Saturation: $$I_D = \frac{1}{2}\mu_n C_{OX} \frac{W}{L}(V_{GS} - V_{TH})^2$$

- **Body Effect**

$$V_{TH} = V_{TH0} + \gamma\left(\sqrt{|2\Phi_F + V_{SB}|} - \sqrt{|2\Phi_F|}\right)$$

Recall the last chapter (2)

- **Channel Length Modulation**

$$I_D \approx \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{GS}-V_{TH}\right)^2\left(1+\lambda V_{DS}\right)$$

- **Weak inversion for low power circuits**

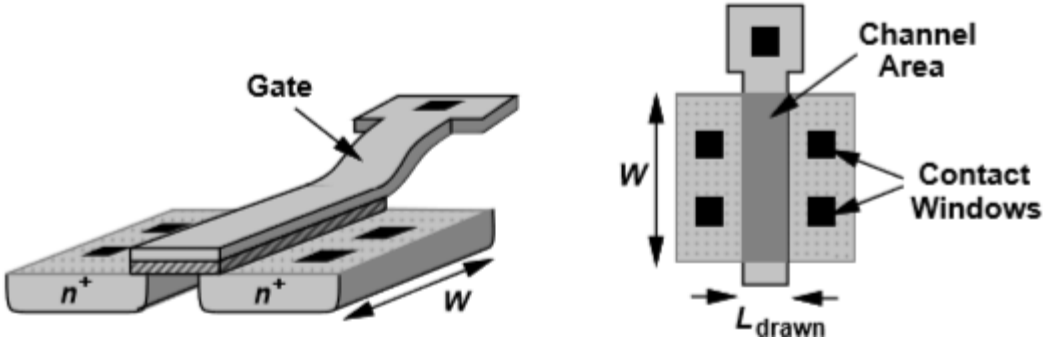
$$I_D = I_0 \exp\frac{V_{GS}}{\varsigma V_T}$$

Derive Gm in linear, saturation and weak inversion

Outline

- Review：Diodes
- MOS I/V Characteristics
- MOS Device Models
  - MOS Device Capacitances
  - MOS Small-Signal Model
- MOS Short-Channel Effect
- MOS SPICE Models

Parasitic Resistance and Capacitance



- The gate polysilicon, S/D terminals must be tied to metal (aluminum) wires that serve as interconnects **with low resistance and capacitance**.
- Parasitic resistance and capacitance

  They are small: several ohms resistance

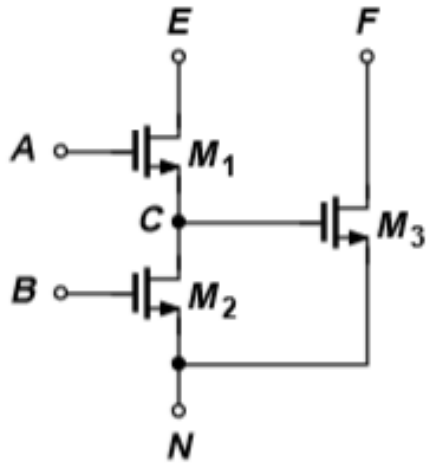
  and several famtofarad capacitance (fF)

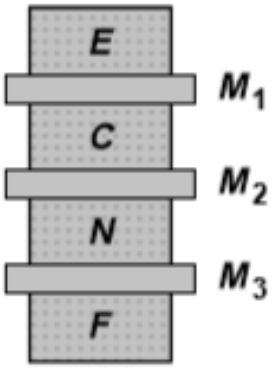
  They are important: - speed for digital/analog

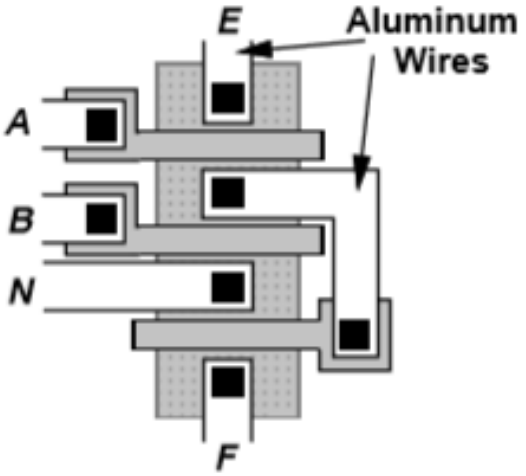
  - stability for digital/analog

MOS Device Layout

- To minimize the capacitance of the source and drain, the **total area of each junction** must be minimized.

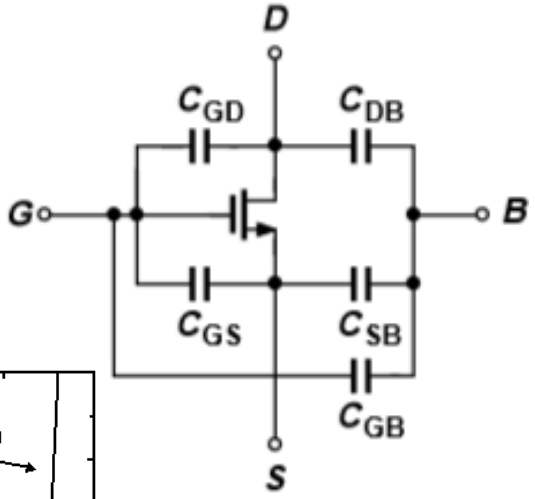


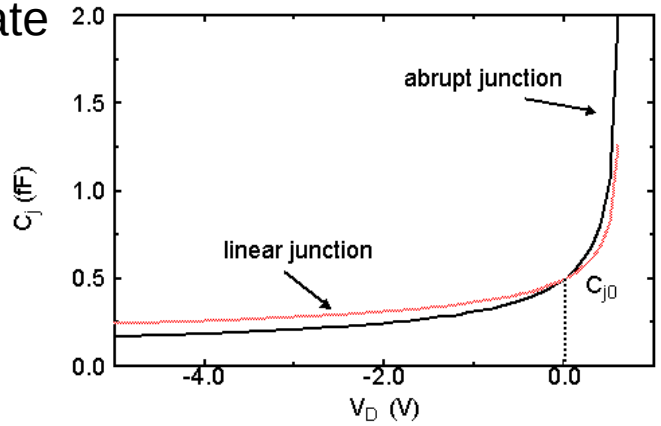




MOS Device Capacitance: C_{BX}

- ***To predict high-frequency behavior***
- C_{BD} and C_{BS} (diode cap) associate with the **back-biased depletion region** between the drain and substrate and the source and substrate

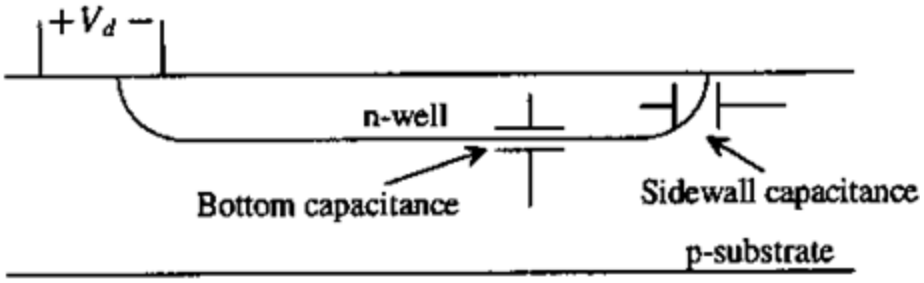


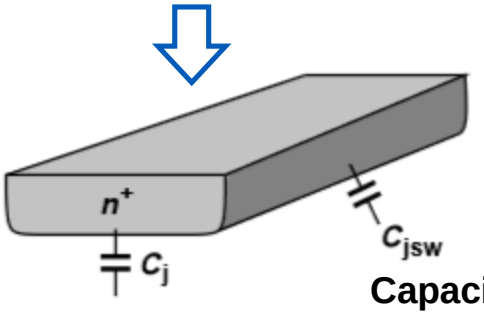


$$C_j = \frac{C_{j0}}{\left[1-\left(\frac{V_d}{\varphi_0}\right)\right]^m} \qquad C_{j0} = \sqrt{\frac{q\varepsilon_{si}\left(N_A+N_D\right)}{2\varphi_0}} \qquad \varphi_0 = \frac{kT}{q}\cdot\ln\left(\frac{N_A N_D}{n_i^2}\right) \qquad m=0.3\sim0.5$$

- Capacitance per area

MOS Device Capacitance: Depletion Cap





Capacitance per area: F/m²

Capacitance per perimeter: F/m

$$C_{BX} = \frac{(CJ)(AS)}{\left[1-\left(\frac{v_{BX}}{PB}\right)\right]^{MJ}} + \frac{(CJSW)(PS)}{\left[1-\left(\frac{v_{BX}}{PB}\right)\right]^{MJSW}}$$

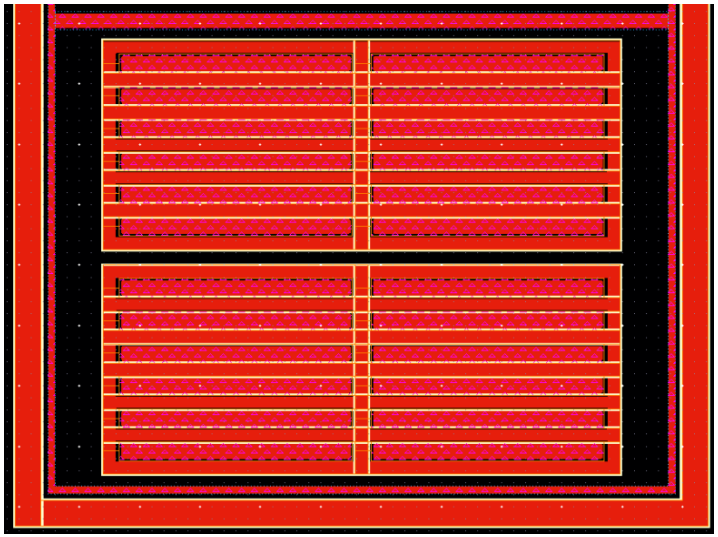
Bottom-plate Capacitance ***(per area)***

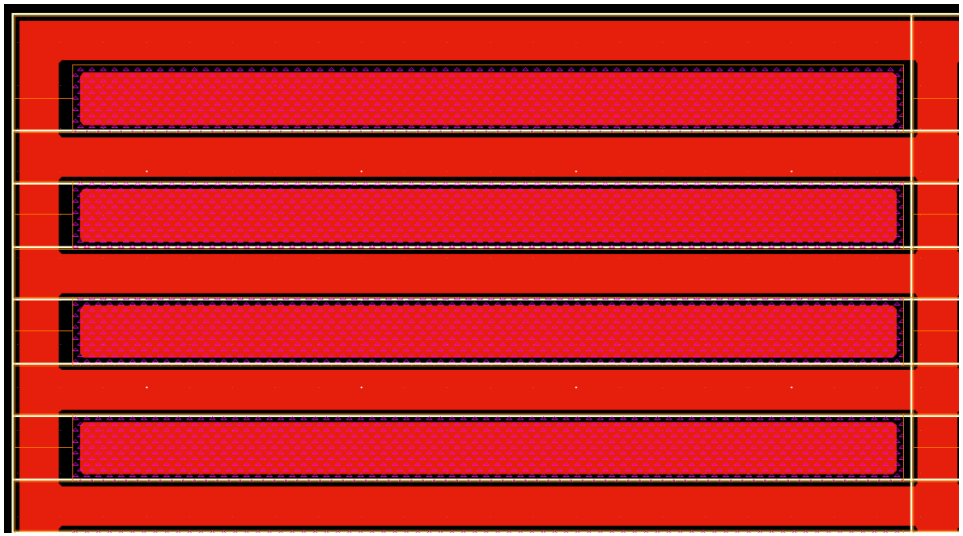
Side-wall capacitance ***(per perimeter)***

X: “S” or “D”
AS=area of the source
PS=perimeter of the source
CJSW=zero bias, bulk-source sidewall capacitance
MJSW=bulk-source sidewall grading coefficient

An ESD device based on sidewalls

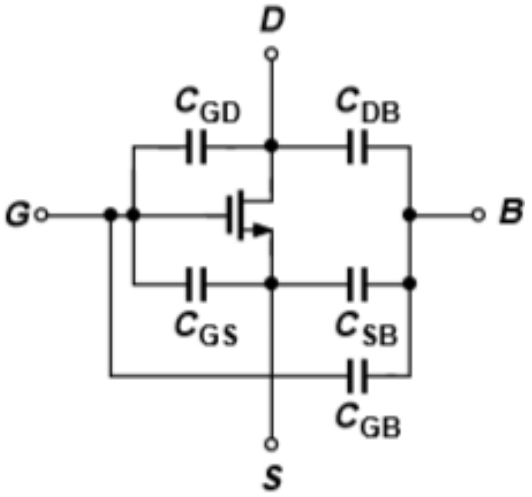
- Cjsw >> Cj

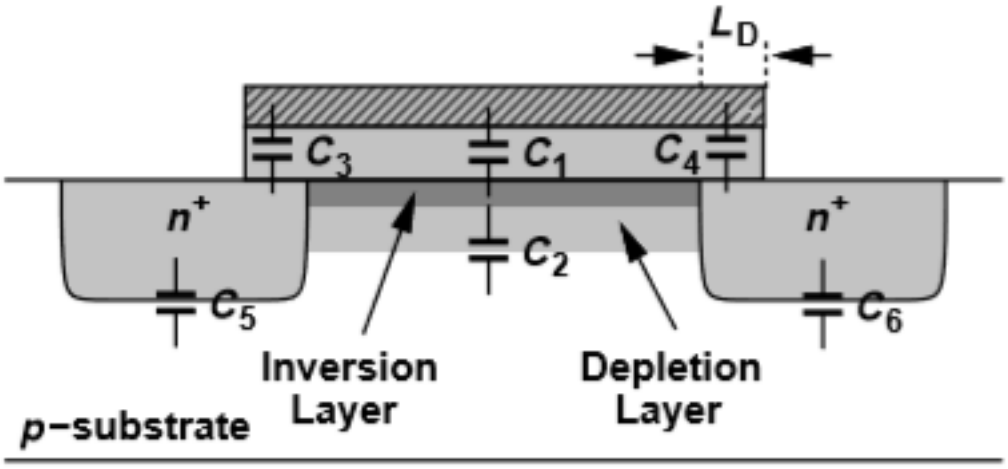




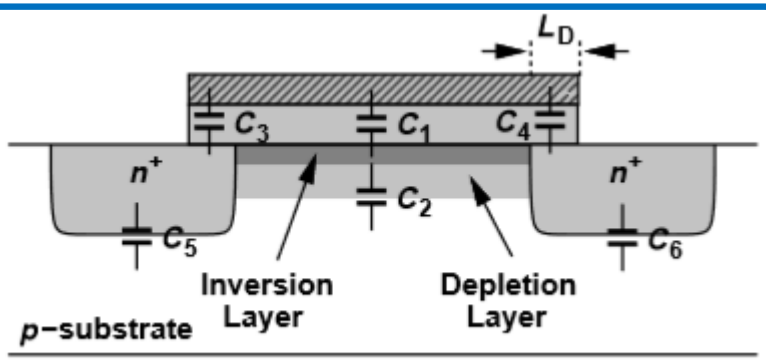
MOS Device Capacitance: $C_{GD/GS/GB}$

- C_{GD}, C_{GS} and C_{GB}
  are all common to the gate and **are dependent on the operating condition of the transistor**

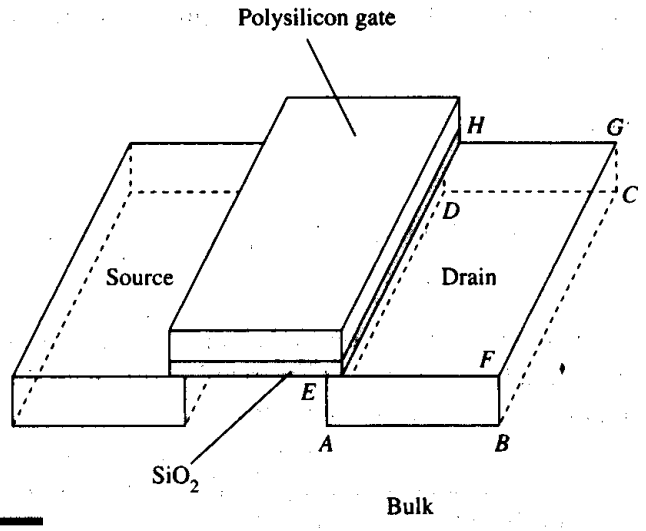




MOS Device Capacitance: Depletion Cap



C_5、C_6: the junction capacitance between S/D areas and the substrate



Type	p-Channel	n-Channel	Units
CGSO	220×10^{-12}	220×10^{-12}	F/m
CGDO	220×10^{-12}	220×10^{-12}	F/m
CGBO	700×10^{-12}	700×10^{-12}	F/m
CJ	560×10^{-6}	770×10^{-6}	F/m^2
CJSW	350×10^{-12}	380×10^{-12}	F/m
MJ	0.5	0.5	
MJSW	0.35	0.38	

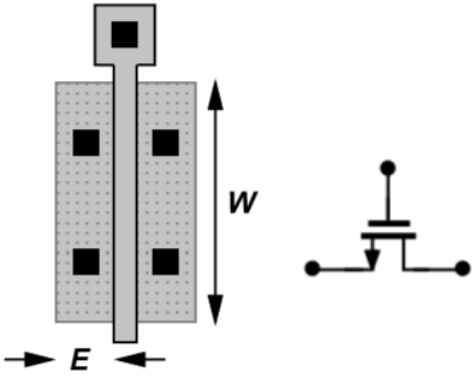
Bottom: ABCD=EFGH
Sidewall: ABFE+BCGF+ DCGH+ADHE
=> perimeter: EF+FG+GH+HE

A typical S/D: 1.8μm × 5μm
C_{BX} of N-Channel: 12.1fF
C_{BX} of P-Channel: 9.8fF.

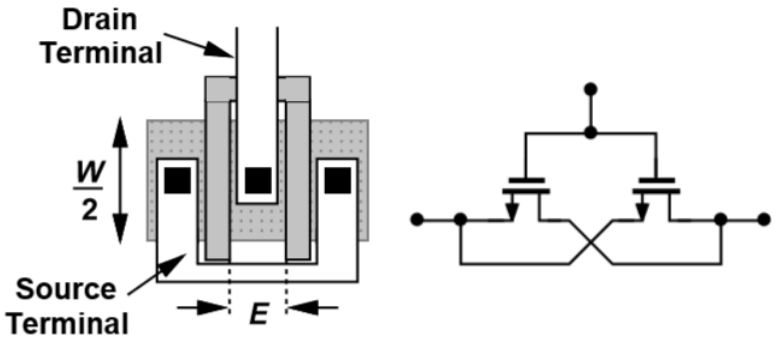
C_2: the channel-to-bulk capacitance $C_{2,j0} = \sqrt{\frac{q\varepsilon_{si}N_{sub}}{4\varphi_F}} \times WL$

MOS Device Capacitance: Depletion Cap

Example Calculate the source and drain junction capacitance of the transistor



$$C_{DB} = C_{SB} = WEC_j + 2(W+E)C_{jsw}$$



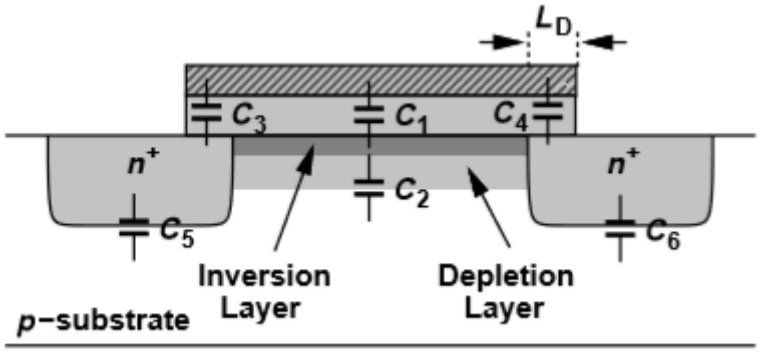
$$C_{DB} = \frac{W}{2}EC_j + 2\left(\frac{W}{2}+E\right)C_{jsw}$$

$$C_{SB} = 2\left[\frac{W}{2}EC_j + 2\left(\frac{W}{2}+E\right)C_{jsw}\right]$$

$$= WEC_j + 2(W+2E)C_{jsw}$$

- *How to reduce the drain junction capacitor of MOS ?*

MOS Device Capacitance: Charge-storage Cap



C_1: gate-to-channel capacitance

$C_1 = W_{eff}(L-2L_D)C_{ox} = W_{eff}L_{eff}C_{ox}$

C_3/C_4: overlap capacitances between G and S/D

$C_3 = C_4 \approx (L_D)(W_{eff})\ C_{ox} = (CGXO)W_{eff}$

$= C_{OV}W$ X: "S" or "D"

Type	p-Channel	n-Channel	Units
CGSO	220×10^{-12}	220×10^{-12}	F/m
CGDO	220×10^{-12}	220×10^{-12}	F/m
CGBO	700×10^{-12}	700×10^{-12}	F/m
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MJ	0.5	0.5	
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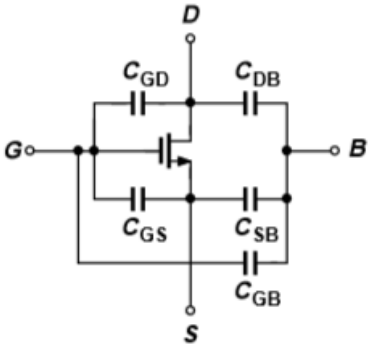
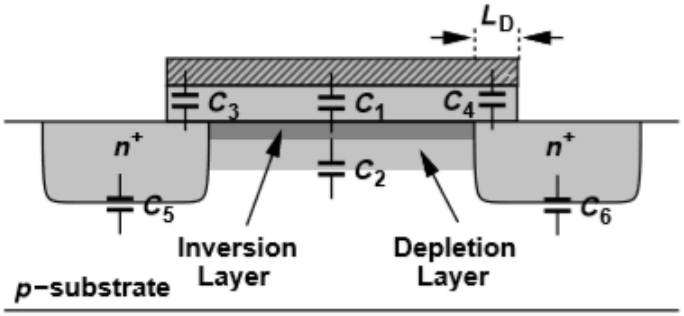
MOS Device Capacitance: C_{GS}, C_{GD}, C_{GB}





Cutoff region

$C_{GS}=C_3$

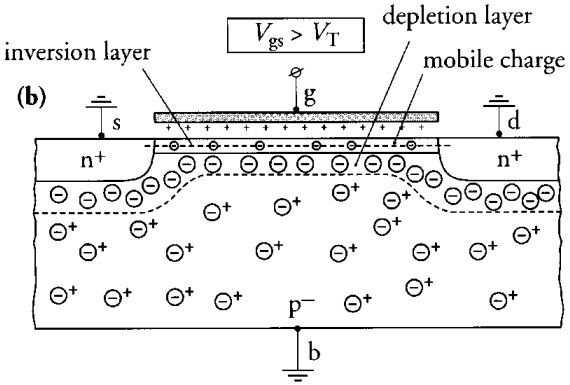
$C_{GD}=C_4$

$C_{GB}=C_1//C_2$

Triode region

$C_{GS}=C_3+1/2 \cdot C_1$

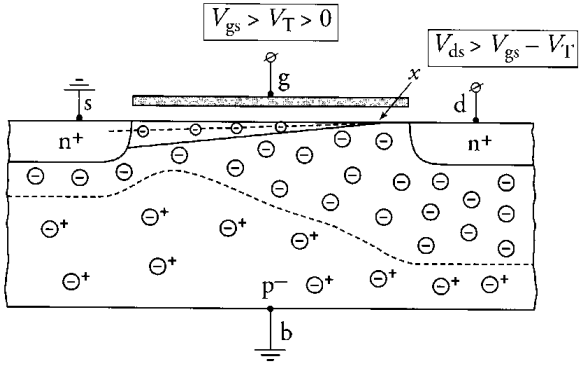
$C_{GD}=C_4+1/2 \cdot C_1$



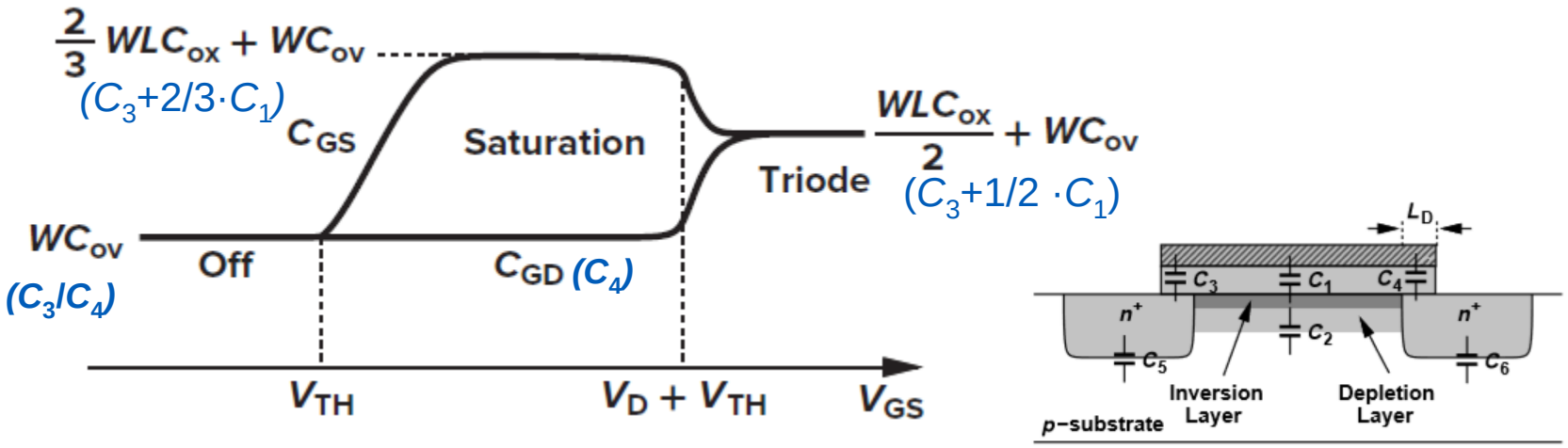
Saturation region

$C_{GS}=C_3+2/3 \cdot C_1$

$C_{GD}=C_4$



MOS Device Capacitance: C_{GS}, C_{GD}, C_{GB}



- C_{SB} and C_{DB} are a **function of the source and drain voltages** with respect to the substrate.
- C_{GB} is usually **neglected** in triode and saturation regions because the **inversion layer acts as a "shield"** between the gate and the bulk, so if V_G varies, the charge is supplied by S/D rather than the bulk.

Outline

- Review: Diodes
- MOS I/V Characteristics
- MOS Device Models
  - MOS Device Capacitances
  - MOS Small-signal Models
- MOS Short-Channel Effect
- MOS SPICE Models

MOS Small-Signal Model

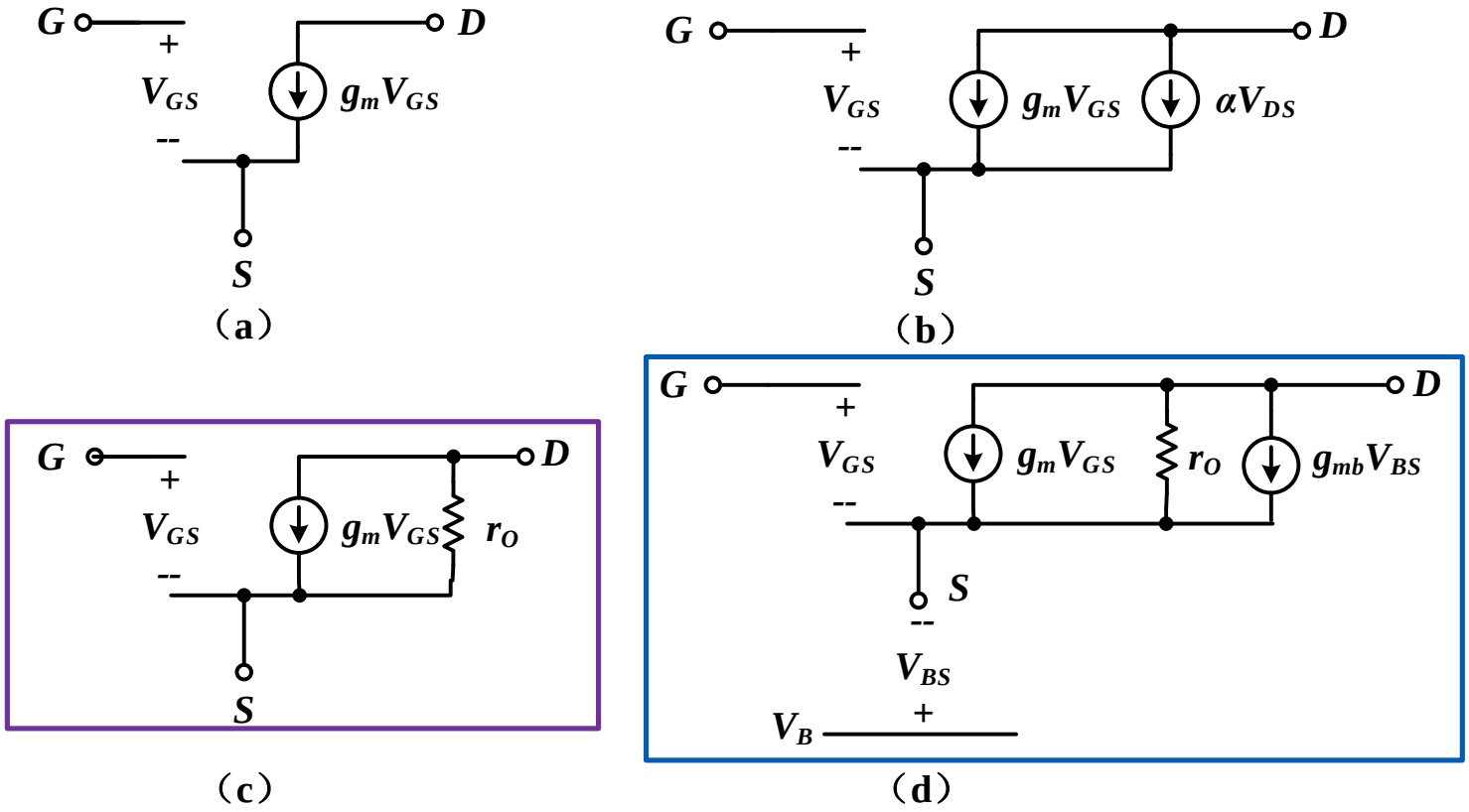


Fig. (a) Basic MOS small-signal model, (b) channel-length modulation represented by a dependent current source, (c) Channel-length modulation represented by a resistor, (d) Body effect represented by a dependent current source.

MOS Small-Signal Model: Parameters

- Transconducance跨导 g_m

$$g_m = \frac{\partial I_D}{\partial V_{GS}}\bigg|_{V_{DS},const} = \mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH}) = \sqrt{2\mu_n C_{ox}\frac{W}{L}I_D} = \frac{2I_D}{V_{GS}-V_{TH}} \qquad V_{ON} = V_{GS}-V_{TH}$$

- 衬底跨导 g_{mb}

$$g_{mb} = \frac{\partial I_D}{\partial V_{BS}} = \mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})\left(-\frac{\partial V_{TH}}{\partial V_{BS}}\right)$$

g_{mb}和g_m的作用是一致的。

$$\because \frac{\partial V_{TH}}{\partial V_{BS}} = -\frac{\partial V_{TH}}{\partial V_{SB}} = -\frac{\gamma}{2}(2\Phi_F + V_{SB})^{-1/2} \qquad \therefore \quad g_{mb} = g_m\frac{\gamma}{2\sqrt{2\Phi_F + V_{SB}}} = \eta g_m$$

$$V_{TH} = V_{TH0} + \gamma\left(\sqrt{|2\Phi_F + V_{SB}|} - \sqrt{|2\Phi_F|}\right)$$

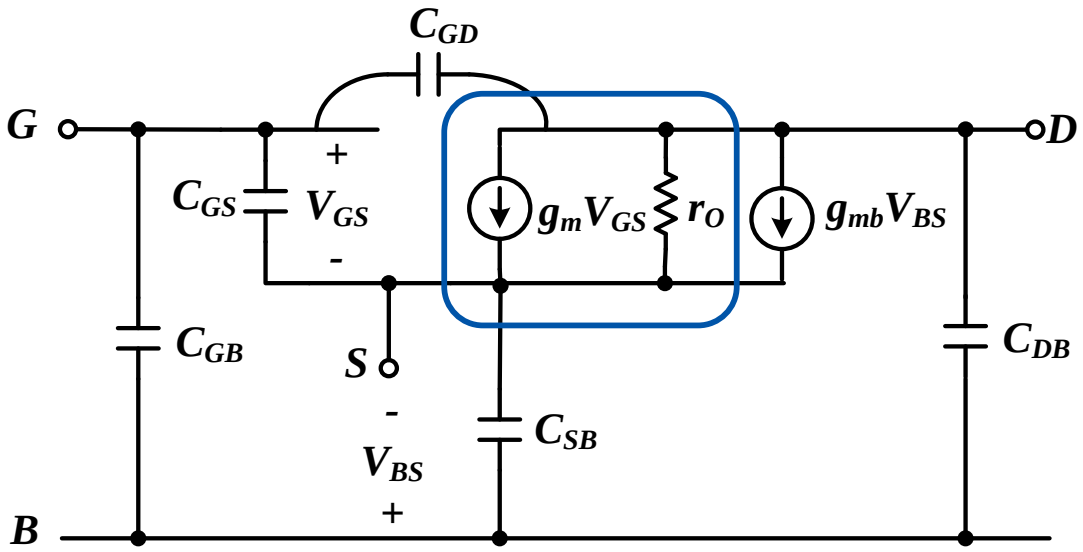
$$\eta = g_{mb}/g_m \qquad \eta\uparrow \Rightarrow g_{mb}\uparrow,$$

$$\eta = g_{mb}/g_m \sim 0.1-0.2$$

- **Output resistance r_o in saturation region**

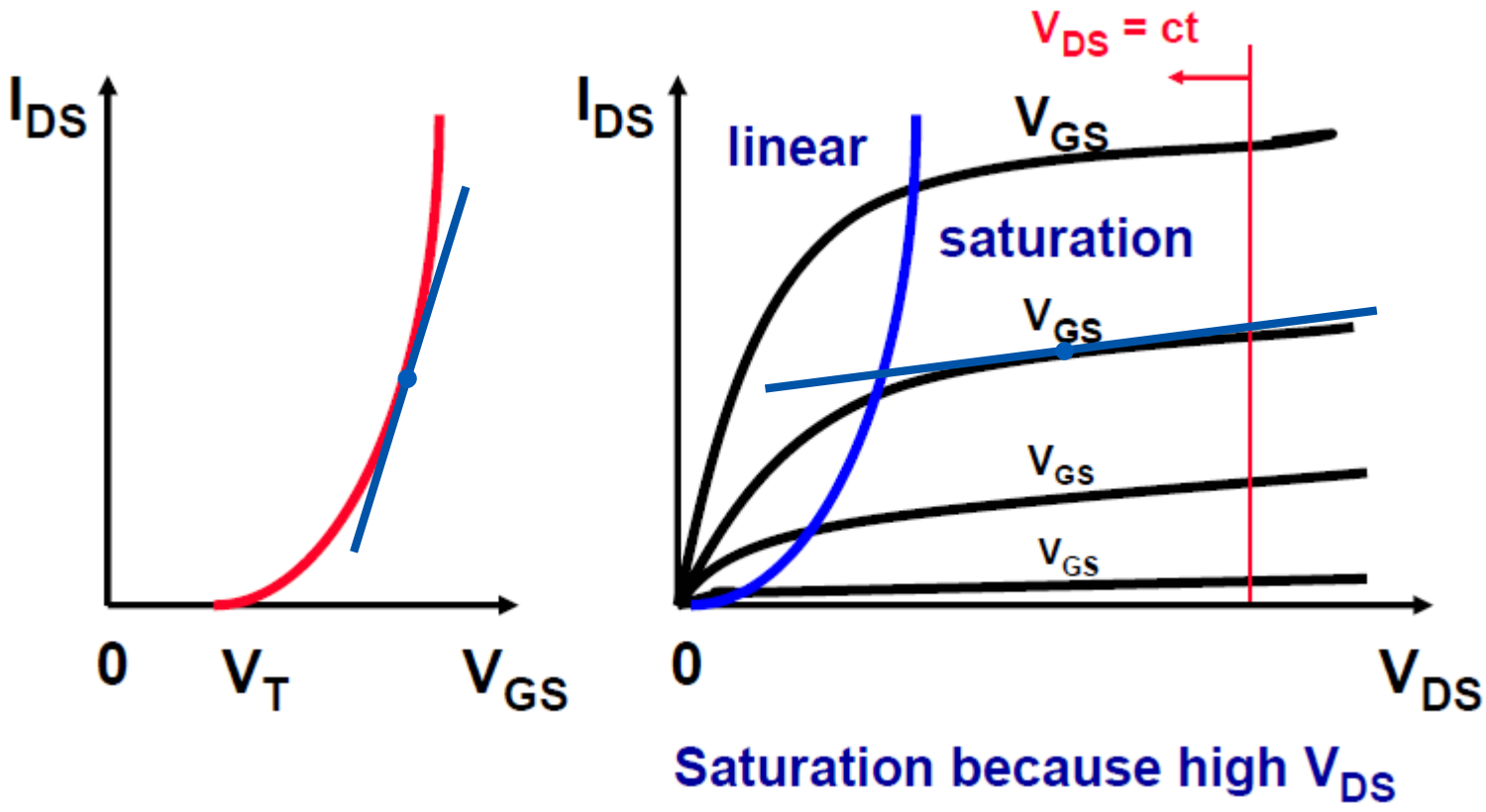
$$ro = \frac{\partial V_{DS}}{\partial I_D} = \frac{1}{\partial I_D/\partial V_{DS}} = \frac{1}{\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2\cdot\lambda} \approx \frac{1}{\lambda I_D} \qquad r_O = \frac{V_E L}{I_{DS}}$$

MOS Small-Signal Model



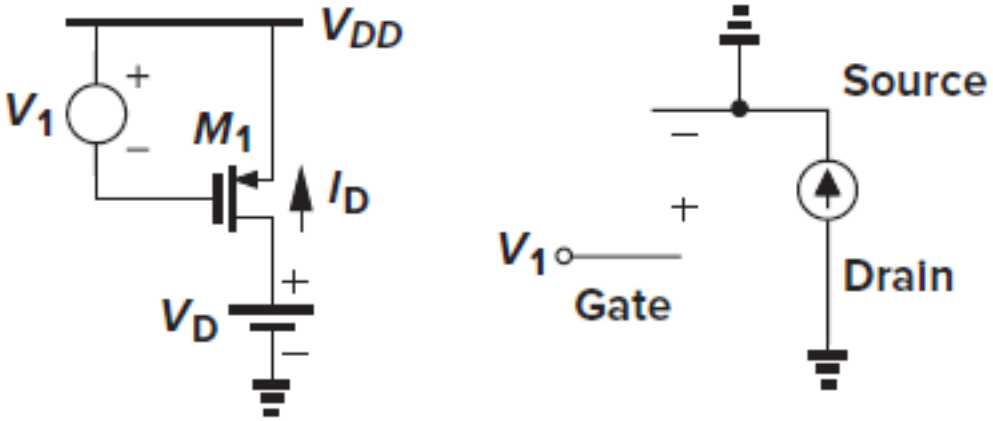
- How to use the model in analyzing a complex circuit **intuitively**?
- Determine the **simplest device model** with reasonable accuracy to represent the role of each transistor!

Gm and ro in I/V curve



G_m r_o

NMOS vs. PMOS



The current in PMOS model is opposite of that in NMOS model

- PMOS devices are quite **inferior** (remember the substrate is p-type) to NMOS in most CMOS technology.
  - Lower mobility of holes ($\mu_p C_{ox} \approx 1/2 \sim 1/3\ \mu_n C_{ox}$) yield lower current drive and conductance.
- NMOS exhibit **higher output resistance**, providing more ideal current sources and higher gain in amplifiers.
- As such is it preferred to incorporate NMOS rather than PMOS wherever possible.

MOS SPICE Models – Level 1

Table Level 1 SPICE Models for NMOS and PMOS Devices.

NMOS Model			
LEVEL = 1	VTO = 0.7	GAMMA = 0.45	PHI = 0.9
NSUB = 9e+14	LD = 0.08e-6	UO = 350	LAMBDA = 0.1
TOX = 9e-9	PB = 0.9	CJ = 0.56e-3	CJSW = 0.35e-11
MJ = 0.45	MJSW = 0.2	CGDO = 0.3e-9	JS = 1.0e-8
PMOS Model			
LEVEL = 1	VTO = -0.8	GAMMA = 0.4	PHI = 0.8
NSUB = 5e+14	LD = 0.09e-6	UO = 100	LAMBDA = 0.2
TOX = 9e-9	PB = 0.9	CJ = 0.94e-3	CJSW = 0.32e-11
MJ = 0.5	MJSW = 0.3	CGDO = 0.3e-9	JS = 0.5e-8

VTO: threshold voltage with zero V_{SB} (unit: V); **GAMMA**: body effect coefficient (unit: $V^{1/2}$)
PHI: $2\Phi_F$ (unit: V); **TOX**: gate oxide thickness (unit: m)
NSUB: substrate doping (unit: cm^{-3}) **LD:** source/drain side diffusion (unit: m)
UO: channel mobility (unit: $cm^2/V/s$) **LAMBDA:** channel-length modulation coefficient (unit: V^{-1})
CJ: source/drain bottom-plate junction capacitance per unit area (unit: F/m^2)
CJSW: source/drain sidewall junction capacitance per unit length (unit: F/m)
PB: source/drain junction built-in potential (unit: V)
MJ: exponent in CJ equation (unitless) **MJSW:** exponent in CJSW equation (unitless)
CGDO: gate-drain overlap capacitance per unit width (unit: F/m)
CGSO: gate-source overlap capacitance per unit width (unit: F/m)
JS: source/drain leakage current per unit area (unit: A/m^2)

Some useful values

- Vth: 400~600mV
- Vgs: 400~800mV
- Vds: minimum 100~200mV
- Gm/I_D : 0.1 ~ 25
  （>20 subthreshold region）
- Ro: $1/(0.1\sim10*I_D)$
- Gm* Ro: ~100
  (single-stage amplifier)
- Cgs, Cgd: $1\sim3fF/um^2$

Real values based on simulations

- *R*o at different W/L and Vds/Ids

PMOS

W/L(um) Id / Vds	1/0.1	10/0.1	1/1	10/1	10/10	100/1	100/10
1uA 0.2V	326.2k	319k	732.4k	898.5k	1.14M	1.36M	1.49M
10uA 0.5V	66.2k	48.6k	273.6k	269.4k	837k	165.3k	874.8k

NMOS

W/L(um) Id / Vds	1/0.1	10/0.1	1/1	10/1	10/10	100/1	100/10
1uA 0.2V	499.5k	429.6k	765.7k	1.654M	913.3k	1.42M	2.94M
10uA 0.5V	111k	48.2k	146.6k	609.7k	139.6k	394.3k	1.89M

Outline

- Review: Diodes
- MOS I/V Characteristics
- MOS Device Models
- MOS Short-Channel Effect
  - Scaling Theory
  - Short-channel Effects: Carrier Mobility Degradation, Hot-Carrier Effect
- MOS SPICE Models

Reference:
Chapter 17, <Design of Analog CMOS Integrated Circuits>Razavi著

Scaling-down按比例缩小（1）

- The square-law characteristics for MOSFETs provide moderate accuracies for devices with minimum channel lengths of greater than **several microns（μm）.**
- As device dimensions continue to scale down, higher order effects necessitate more complex models.

The two principal reasons for the dominance of **CMOS technology** in today's semiconductor industry:

1) the **zero static power** dissipation of CMOS logic;
2) the **scalability** of MOSFETs.

Scaling-down按比例缩小（2）

Scaling theory (Robert Dennard, IBM Reseacher)

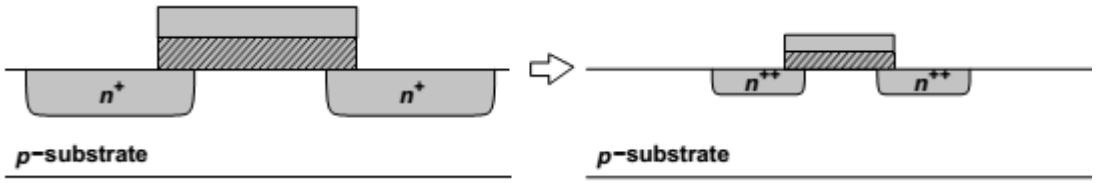
(1) reduce all lateral and vertical dimensions by α (>1) W, L, t_{ox}, x_j, …… density↑α^2

(2) reduce the threshold voltage and the supply voltage by α V_{DD}, V_{TH}

(3) increase all of the doping levels by α n^+, p^+

⇨ ***Constant-field scaling***

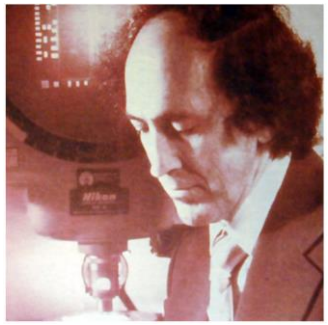
I_D/α, $C_{channel}/\alpha$ =>speed ↑α P/α^3,



g_m不变, $g_m r_O$不变

V_{DD}/α => DR/α, P/α^2,
(no the same DR)

⇨ ***Constant-voltage scaling***



Dennard, Robert H., *Gaensslen, Fritz H., Yu, Hwa-Nien, Rideout, V. Leo, Bassous, Ernest, & LeBlanc, Andre R. "Design of ion-implanted MOSFET's with Very Small Physical Dimensions,"* ***IEEE Journal of Solid-State Circuits****, Vol. 9 (October 1974) pp. 256-268.*

Short-Channel Effect

Reasons:

- The **electric fields** increase ⇦ supply voltage has not scaled proportionally.
- The **built-in potential** Φ_B is neither scalable nor negligible.
- The **depth of S/D junctions** cannot be reduced easily.
- The **mobility decreases** as the substrate doping increases.
- The subthreshold slope (described below) is not scalable.

Short-Channel Effect:

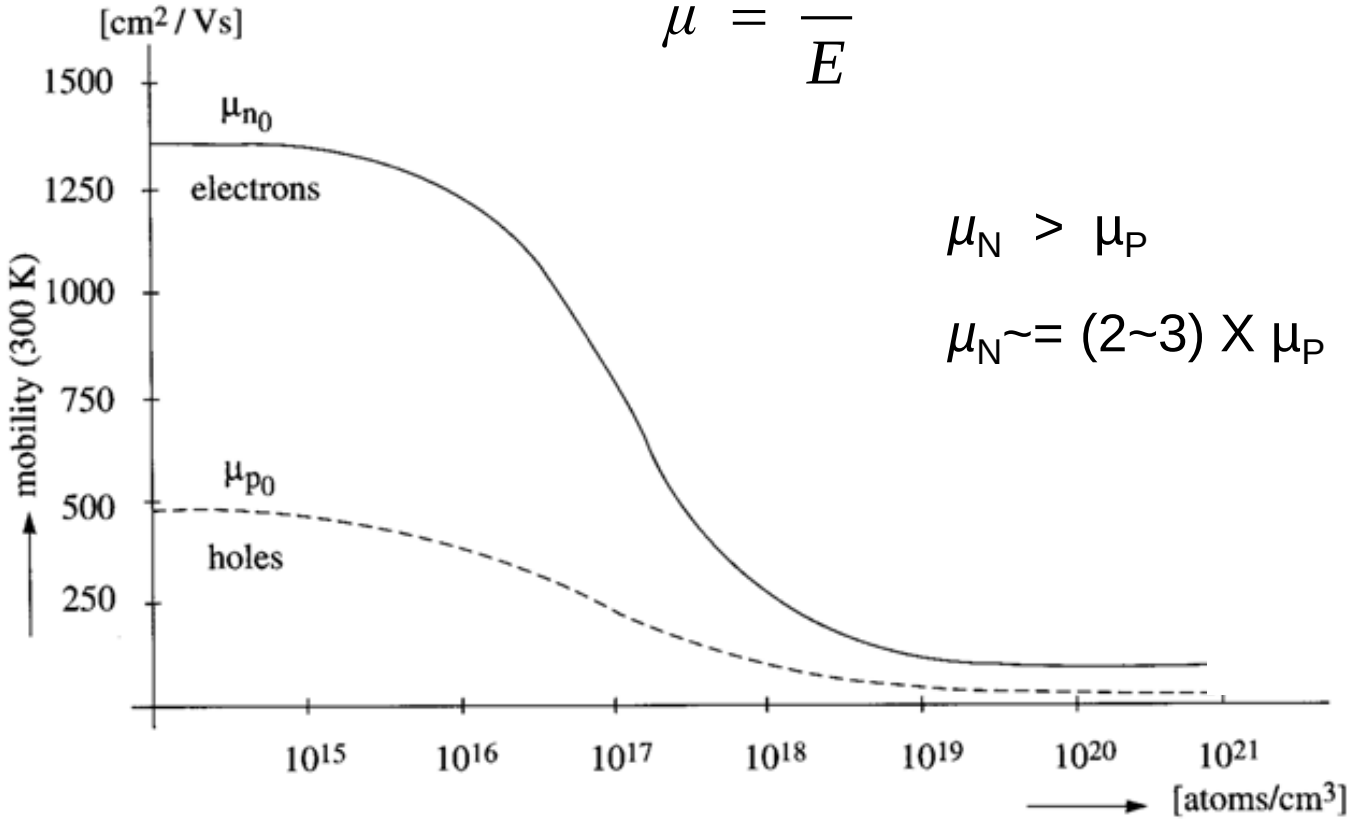
- Threshold voltage variation
  - Effect of channel length on threshold: Short channel -> **Reduction of V_{TH}**
  - Drain-induced barrier lowering (DIBL): High V_{DS} -> **Reduction of V_{TH}**
- Output impedance variation with V_{DS}
  - How to simulate this? DC OP at the maximum signal amplitude

- **Mobility degradation and velocity saturation**
- **Hot carrier effect**
- **Aging model**

Carrier Mobility Degradation

- **Zero Field Mobility**

$$\mu = \frac{v}{E}$$



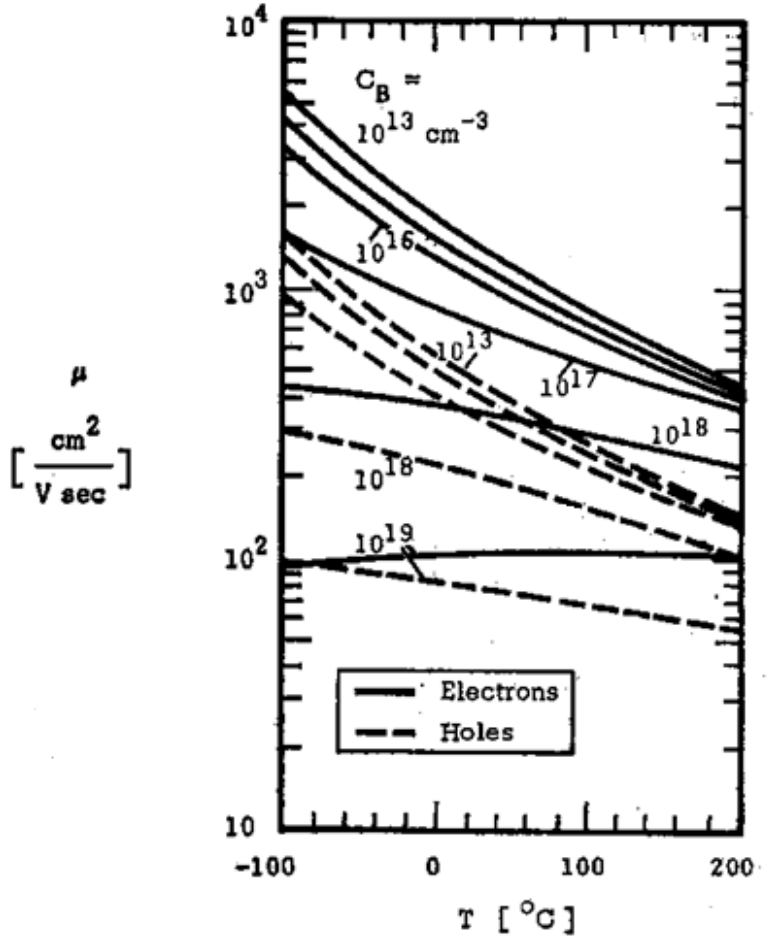
$\mu_N > \mu_P$

$\mu_N \sim= (2\sim3) \times \mu_P$

Carrier mobility as a function of **doping concentration** in silicon at room temperature

Carrier Mobility Degradation- Temp dependence

- **Temperature-Dependence Carrier Mobility Degradation**



$$\mu(T) = \mu_0(T_0) \cdot \left(\frac{T}{T_0}\right)^{-m}$$

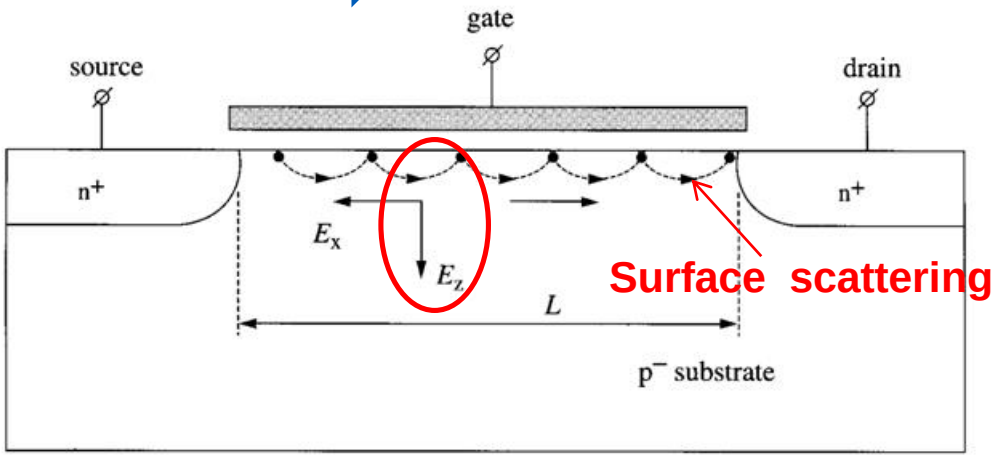
$$m = 1.2 \sim 1.6 \quad \mathbf{1.5}$$

$$K'(T) = K'(298K) \cdot \left(\frac{298K}{T}\right)^{3/2}$$

$$\frac{\partial(V_{TH})}{\partial T} \approx -2 \sim 3mV/^{\circ}C$$

Carrier Mobility Degradation- Vertical Field

- At large V_{GS}, the high electric field between the gate and the channel confines the charge carries to a narrow region below the oxide-silicon interface ⇨ **more carrier scattering and lower mobility**



$$\mu_{eff} = \frac{\mu_0}{1 + \theta(V_{GS} - V_{TH})}$$

where θ is constants.

lowering I_D and g_m

$$I_D = \frac{1}{2}\frac{\mu_0 C_{ox}}{1 + \theta(V_{GS} - V_{TH})}\frac{W}{L}(V_{GS} - V_{TH})^2$$

$$\theta(V_{GS} - V_{TH}) \ll 1 \quad I_D \approx \frac{1}{2}\mu_0 C_{ox}\frac{W}{L}[1 - \theta(V_{GS} - V_{TH})](V_{GS} - V_{TH})^2$$

$$\approx \frac{1}{2}\mu_0 C_{ox}\frac{W}{L}[(V_{GS} - V_{TH})^2 - \theta(V_{GS} - V_{TH})^3].$$

the existence of higher harmonics in the drain current.

Carrier Mobility Degradation- Velocity saturation

Lateral Field $E = \dfrac{\mu_n}{2v_{sat}L}$

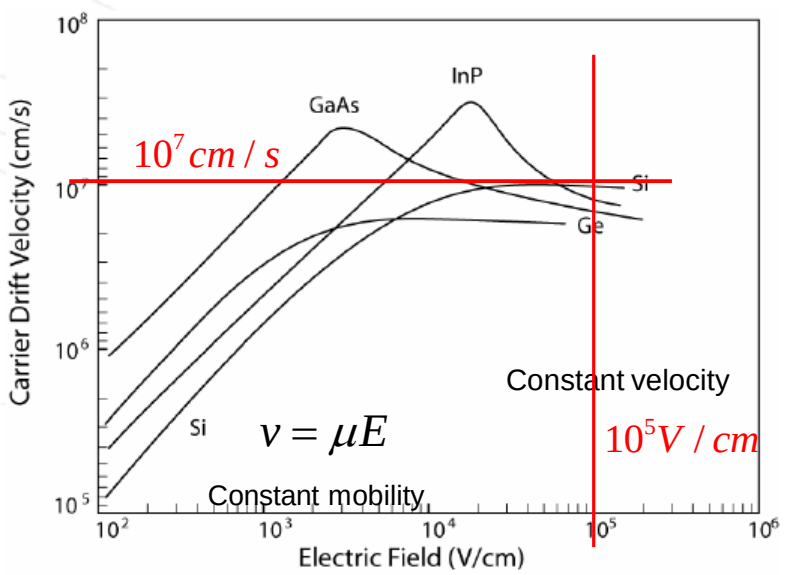
E_X=1V/μm v_{sat}=10^7cm/s

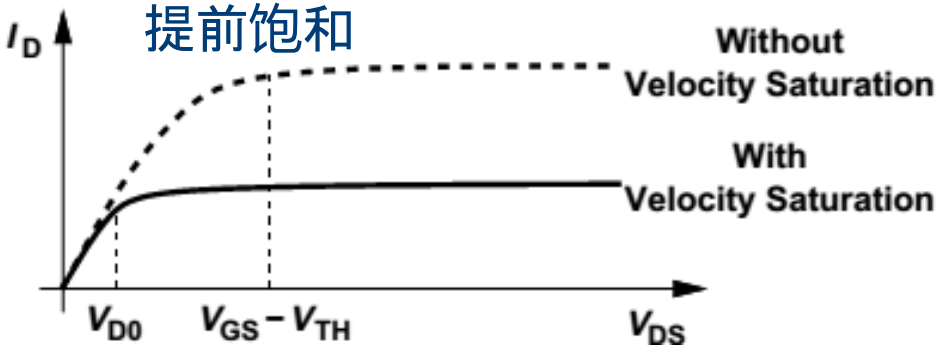
$$I_D = v_{sat}Q_d = v_{sat}WC_{OX}\left(V_{GS} - V_{TH}\right)$$

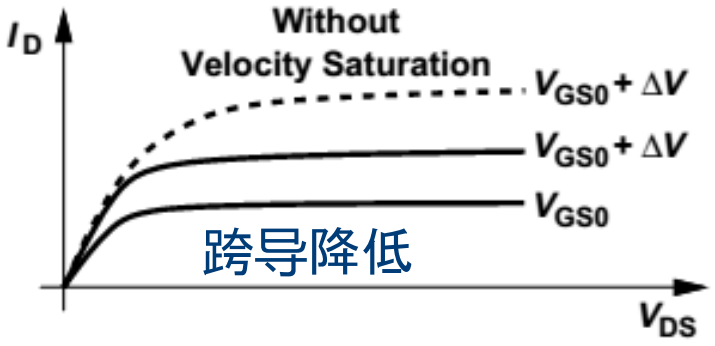
线性！与L无关！

$g_m = v_{sat}WC_{OX}$ **恒定！**

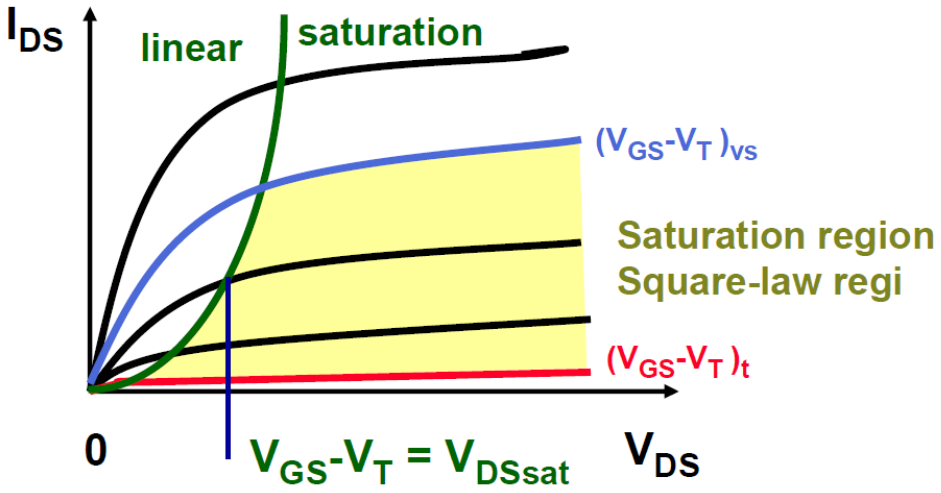
!!! Never enter the high-current or velocity saturation region

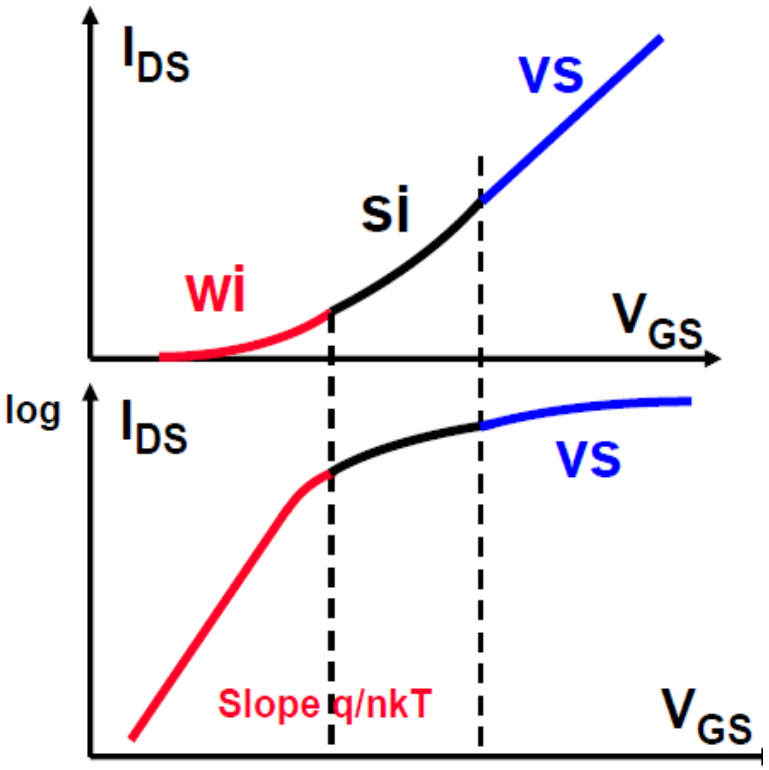






Saturation region vs. velocity saturation





Velocity Saturation

$$I_{DS} = v_{sat} W C_{ox} \left(V_{GS} - V_{TH}\right)$$

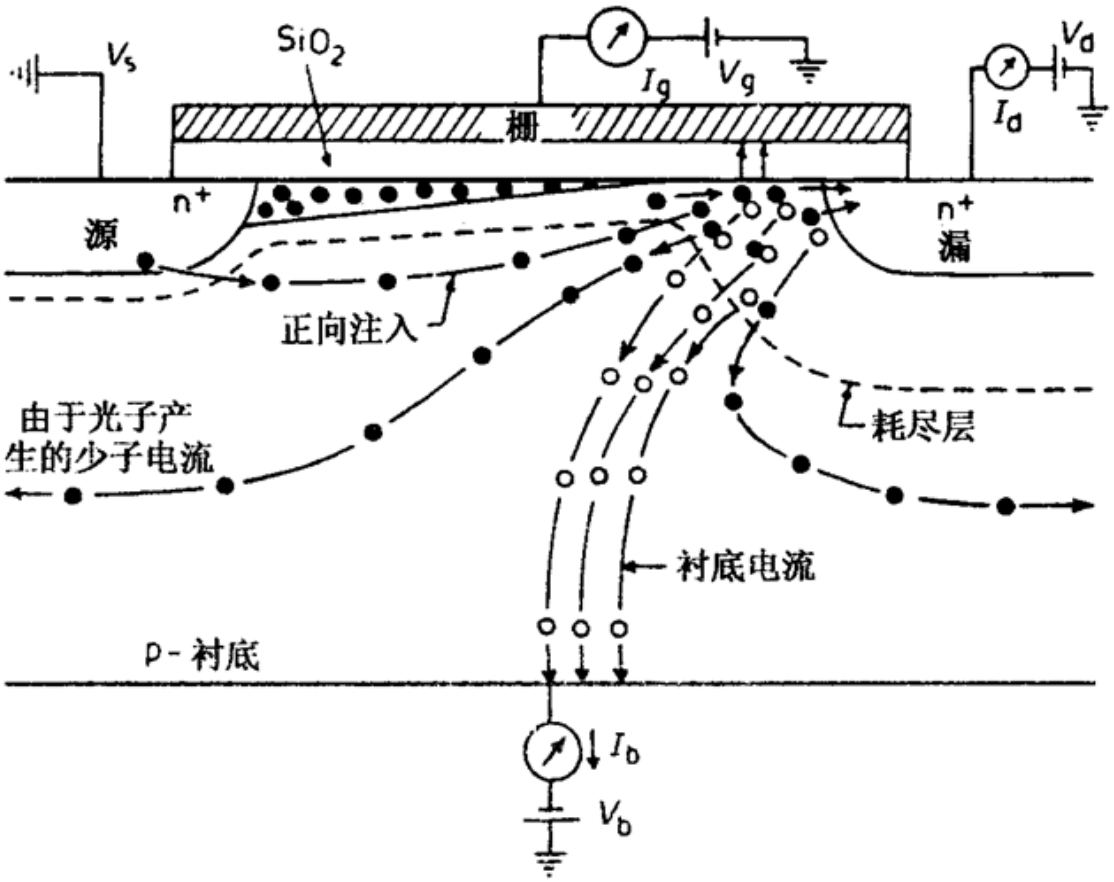
Strong Inversion

$$I_{DS} = \frac{1}{2}\mu_n C_{OX} \frac{W}{L}\left(V_{GS} - V_{TH}\right)^2$$

Weak Inversion

$$I_{DS} = I_0 \exp \frac{V_{GS}}{nkT/q}$$

Hot-Carrier Effect



- Velocity saturation lead to more gate and bulk leakage current.
- The leakage current of memory becomes the majority of power consumption
- Balance between dynamic power and static power

How to mitigate

- Threshold voltage variation
  - Effect of channel length on threshold: Short channel -> **Reduction of V_{TH}**

    Use long channels
  - Drain-induced barrier lowering (DIBL): High V_{DS} -> **Reduction of V_{TH}**

    Reduce the V_{DD}
- Output impedance variation with V_{DS}
  - How to simulate this? DC OP at the maximum signal amplitude

  Use long channels and Reduce the V_{DD}
- Mobility degradation and velocity saturation

  Use lower Vgs (large W/L) and lower Vds

  Use long channels
- Hot carrier effect

  Use lower Vgs (large W/L) and lower Vds

  Use long channels

  Use thick oxide transistors

  Use bulk-source connection

< ~180nm node is good for digital but usually more challenge for analog

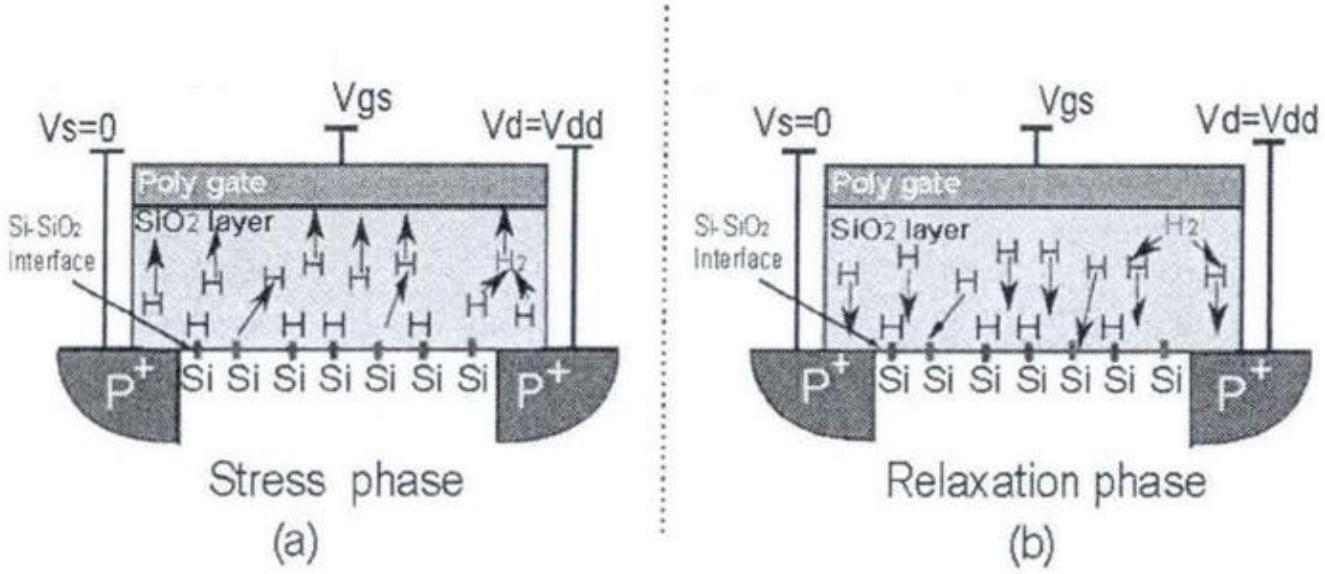
Aging model

- High reliability for Industrial and Auto Grade ICs
  Consumer Grade: -10 ~ 85 ºC, >1 years
  Industrial Grade: -40 -125 ºC, > 3 years
  Auto Grade: -40 150 ºC, > 10 years
  Takes years to get qualified: **AEC-Q100**

- The aging model is the real competitiveness of a foundry

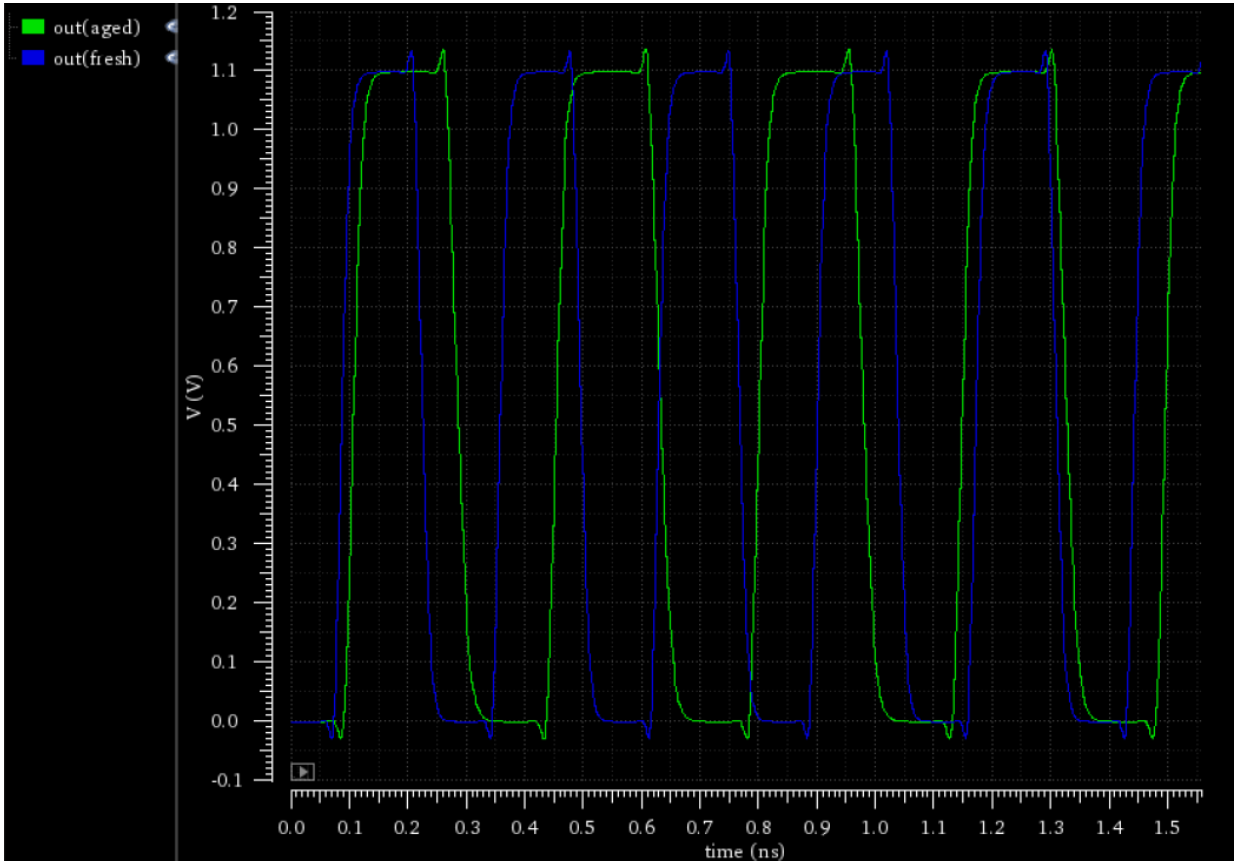
- The aging model includes:
  - Hot carrier effect
  - Positive Bias Temperature Instability
  - Negative Bias Temperature Instability

PBTI induced V_{TH} increase



- High temperature and high Vgs leads to Si-H Bond breaking:
  - Increase of V_{TH}
  - Decrease of channel current
  - Decrease of device speed

An example of Aged inverter



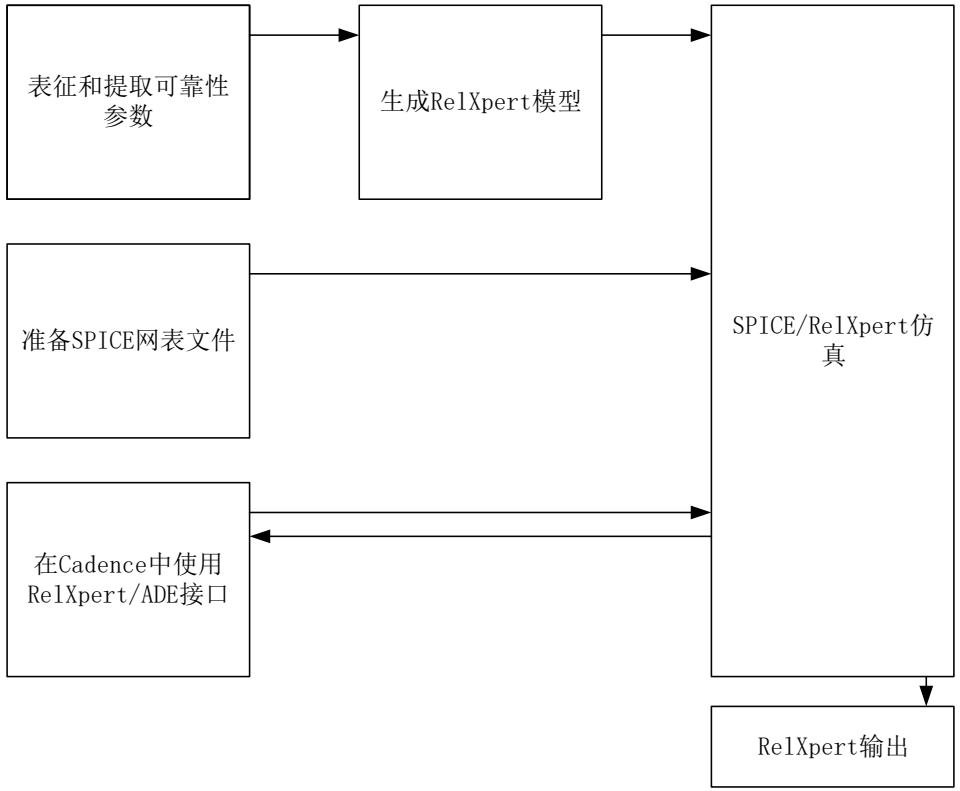
Tool for Aging Simulation

- RelXpert: Reliability Expert

cadence

Virtuoso® RelXpert Reliability Simulator User Guide

Product Version 7.2
December 2009



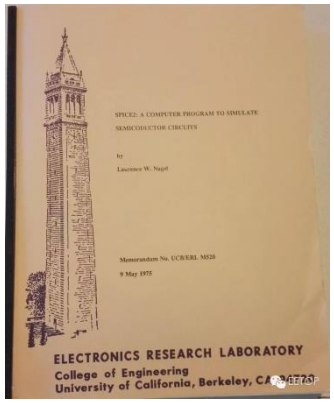
Outline

- Review: Diodes
- MOS I/V Characteristics
- MOS Device Models
- MOS Short-Channel Effect
- MOS SPICE Models

SPICE and Models

- **Simulation Program with Integrated Circuit Emphasis**

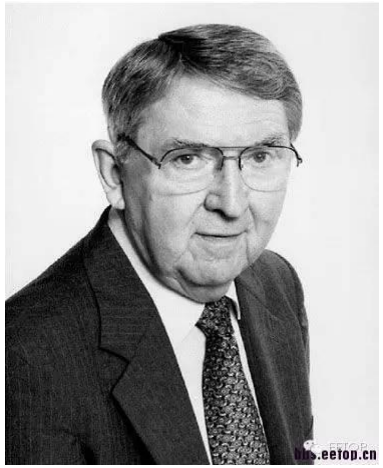
  <= CANCER (**Computer Analysis of Nonlinear Circuits, Excluding Radiation**)



- Prof. Rohrer Nagel, Prof. Peterson (Department head)
- SPICE 2: Nagel

  SPICE2G6: Ellis, Nagel的室友

  SPICE3: Quarles, 增加了用户图像界面
- 开源代码的先驱
- 求解含有非线性器件的电路方程
  - ✓ 改进的节点分析法
  - ✓ 稀疏矩阵求解
  - ✓ 牛顿-拉夫逊迭代
  - ✓ 隐形数值积分
  - ✓ 。。。。。。



SPICE Simulator

- HSPICE: Meta-software -> Avant!(1996) -> Synopsys (2001)
- PSPICE (PC SPICE): MicroSim -> OrCAD (1998) -> Cadence(2000)
- Spectre/Spectre-RF: Cadence
- Smart-Spice: Silvaco
- APLS: 华大九天

Types of Simulator

- SPICE级仿真工具
  - **aps** (Cadence)，Hspice(Synopsys)，finesim spice(Synopsys)，ALPS-AS(Empyrean)
  - 适合求解对精度要求高的模拟电路。
- Fast SPICE级仿真工具
  - hsim (Synopsys)，XA(Synopsys)，finesim pro(Synopsys)，XPS(Cadence)，ultrasim(Cadence)
  - 速度快、精度有损失
  - 数字电路
- 混合信号仿真工具
  - **AMS Designer** (Cadence)，ALPS-MS(Empyrean)
  - SPICE+数字仿真器（如Synopsys的VCS，Cadence的NC，Mentor的Modelsim）连在一起运行

MOS SPICE Models

- **Level 1: Shichman-Hodges Model**

$$i_D = \frac{\mu_0 C_{OX} W}{L}\left[(V_{GS} - V_{TH})V_{GS} - \frac{V_{DS}}{2}\right]V_{DS}(1+\lambda V_{DS}) \quad (0 \le V_{DS} \le V_{GS} - V_{TH})$$

$$i_D = \frac{1}{2}\frac{\mu_0 C_{OX} W}{L}(V_{GS} - V_{TH})^2(1+\lambda V_{DS}) \quad (0 \le V_{GS} - V_{TH} \le V_{DS})$$

$$i_D = 0 \quad (V_{GS} < V_{TH})$$

$$V_{TH} = V_{TH0} + \gamma\left(\sqrt{2|\phi_F| + v_{SB}} - \sqrt{2|\phi_F|}\right) \qquad L_{eff} = L - 2L_D$$

- NOTE:
  - The model does not include subthreshold conduction or any short-channel effects.
  - C_{GS} abruptly changes from (2/3)*WLC*ox + *WC*ov in saturation to (1/2)*WLC*ox + *Wc*ov in the triode region most computation algorithms experience convergence difficulties here

MOS SPICE Models – Level 1

Table Level 1 SPICE Models for NMOS and PMOS Devices.

NMOS Model			
LEVEL = 1	VTO = 0.7	GAMMA = 0.45	PHI = 0.9
NSUB = 9e+14	LD = 0.08e-6	UO = 350	LAMBDA = 0.1
TOX = 9e-9	PB = 0.9	CJ = 0.56e-3	CJSW = 0.35e-11
MJ = 0.45	MJSW = 0.2	CGDO = 0.3e-9	JS = 1.0e-8
PMOS Model			
LEVEL = 1	VTO = -0.8	GAMMA = 0.4	PHI = 0.8
NSUB = 5e+14	LD = 0.09e-6	UO = 100	LAMBDA = 0.2
TOX = 9e-9	PB = 0.9	CJ = 0.94e-3	CJSW = 0.32e-11
MJ = 0.5	MJSW = 0.3	CGDO = 0.3e-9	JS = 0.5e-8

VTO: threshold voltage with zero V_{SB} (unit: V); **GAMMA**: body effect coefficient (unit: $V^{1/2}$)
PHI: $2\Phi_F$ (unit: V); **TOX**: gate oxide thickness (unit: m)
NSUB: substrate doping (unit: cm^{-3}) **LD:** source/drain side diffusion (unit: m)
UO: channel mobility (unit: $cm^2/V/s$) **LAMBDA:** channel-length modulation coefficient (unit: V^{-1})
CJ: source/drain bottom-plate junction capacitance per unit area (unit: F/m^2)
CJSW: source/drain sidewall junction capacitance per unit length (unit: F/m)
PB: source/drain junction built-in potential (unit: V)
MJ: exponent in CJ equation (unitless) **MJSW:** exponent in CJSW equation (unitless)
CGDO: gate-drain overlap capacitance per unit width (unit: F/m)
CGSO: gate-source overlap capacitance per unit width (unit: F/m)
JS: source/drain leakage current per unit area (unit: A/m^2)

MOS SPICE Models – Level 2, 3, …

- Level 2: Physics model
  - Include serval short channel effect
- Level 3: Semi-theoretical & Semi-empirical model
  - Simplified Level 2 model（accuracy vs. computational complexity）

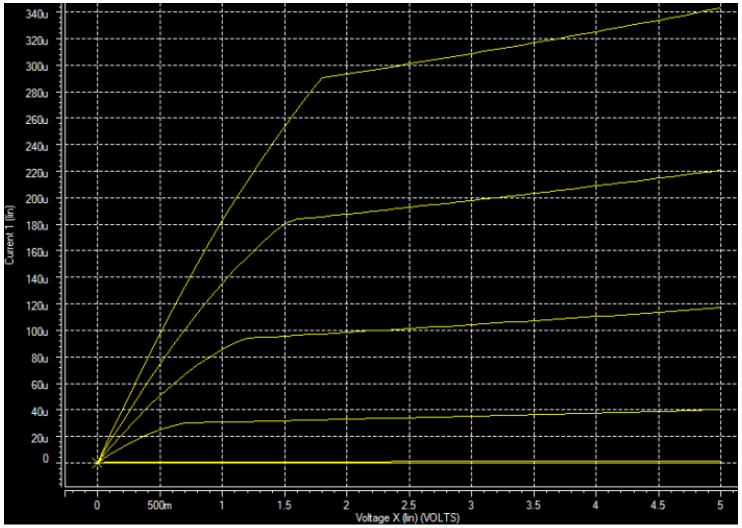


Fig. 2. Variation of Id as a function of gate voltage in LEVEL 1 model

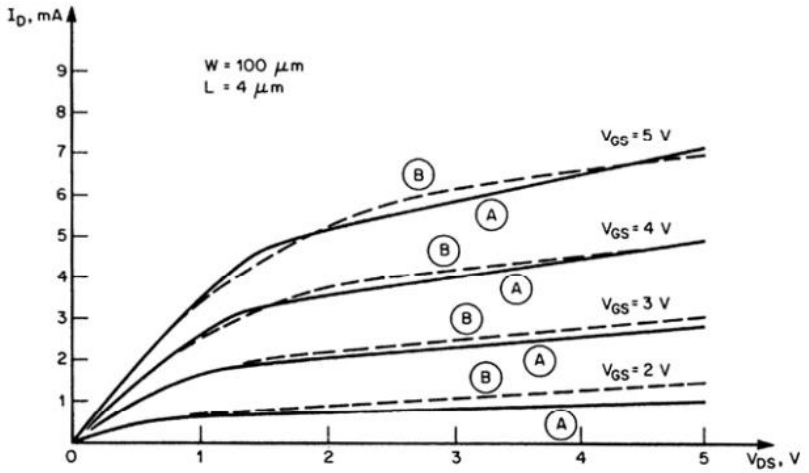


Fig. 7. Id-Vds characteristics of NMOS for LEVEL 2 (A) and LEVEL 3 (B) model.

MOS BSIM model

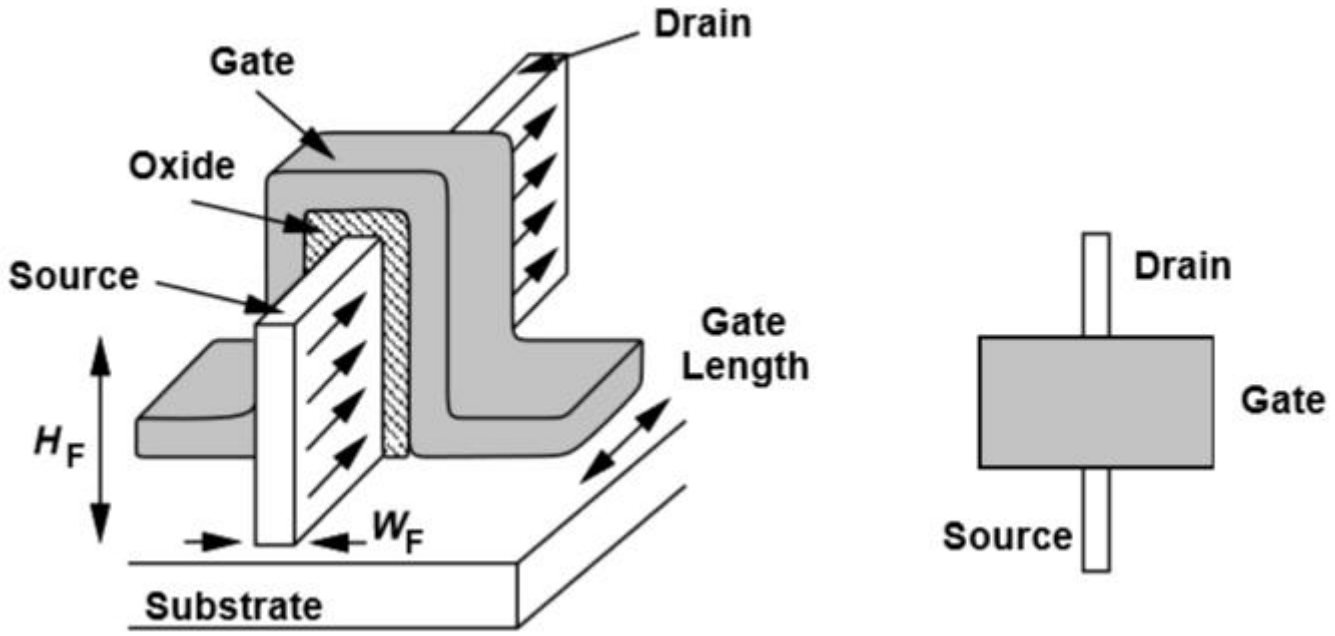
- BSIM (*Berkeley Short Channel IGFET Model*)
  - 胡正明教授(Prof. Chenmin Hu)
  - numerous **empirical parameters**: simplify the equations, but at the cost of **losing touch with** the actual device operation.
  - a simple equation to represent the geometry dependence of many of the device parameters.

$$P = P_0 + \frac{\alpha_P}{L_{eff}} + \frac{\beta_P}{W_{eff}}$$

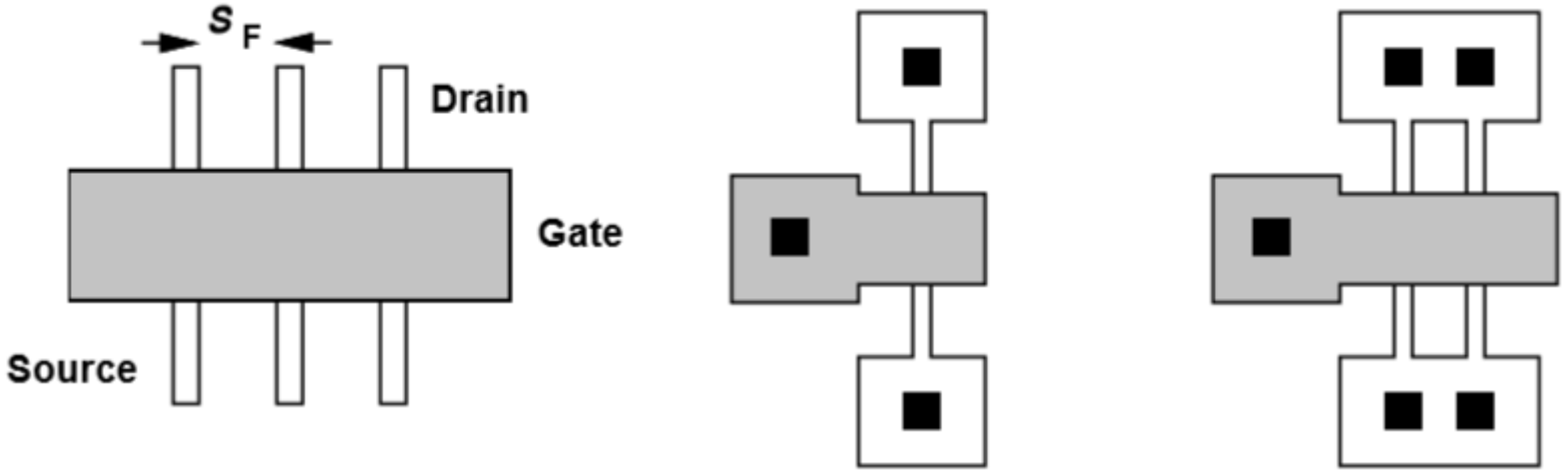
  - http://www-device.eecs.berkeley.edu

  - **FinFET**

Appendix: FinFETs



- FinFETs have three-dimensional geometry and exhibit superior performance as channel lengths fall **below ~20 nm**.
- Here, $\mathbf{W = W_F + 2H_F}$, but since H_F is not under the circuit designer's control and W_F, impacts device imperfections, there are only discrete values for transistor width.



- Spacing between fins, S_F, also plays a significant role in performance and is typically fixed.
- Due to small dimensions of the intrinsic FinFET, the gate and S/D contacts must be placed away from the core of the device.

Compare of MOS Models

Performance Comparison of Models (from Cheng and Hu, *MOSFET Modeling & BSIM3 Users Guide*)

Model	Minimum L (μm)	Minimum Tox (nm)	Model Continuity	i_D Accuracy in Strong Inversion	i_D Accuracy in Subthreshold	Small signal parameter	Scalability
MOS1	5	50	Poor	Poor	Not Modeled	Poor	Poor
MOS2	2	25	Poor	Poor	Poor	Poor	Fair
MOS3	1	20	Poor	Fair	Poor	Poor	Poor
BSIM1	0.8	15	Fair	Good	Fair	Poor	Fair
BSIM2	0.35	7.5	Fair	Good	Good	Fair	Fair
BSIM3v2	0.25	5	Fair	Good	Good	Good	Good
BSIM3v3	0.15	4	Good	Good	Good	Good	Good

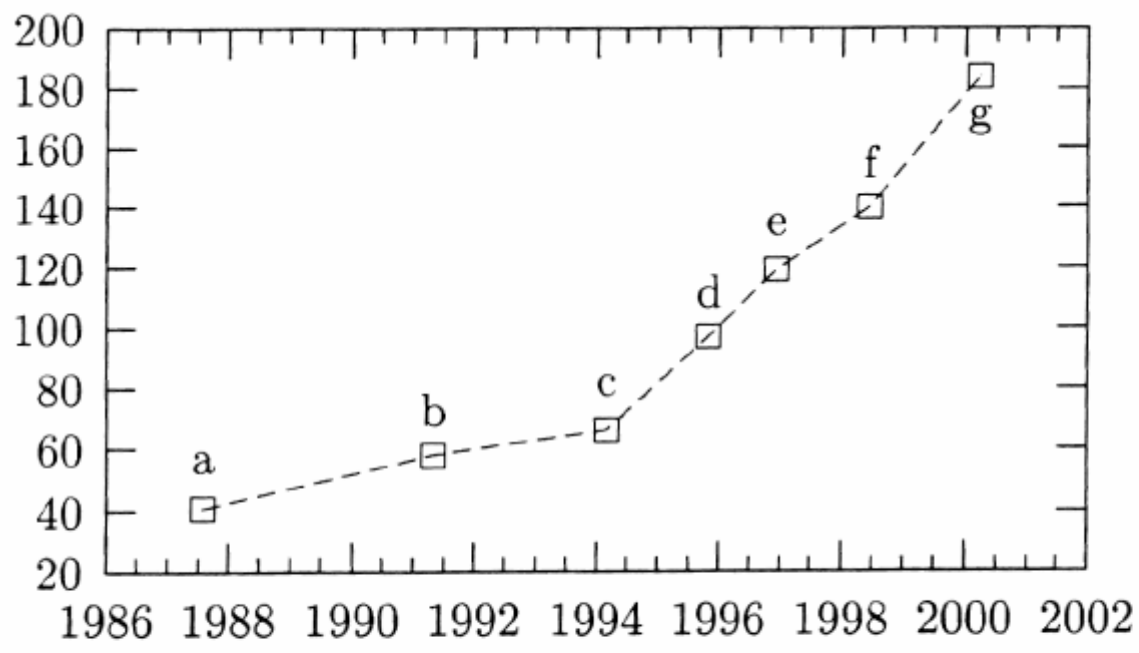
Example of BSIM (NMOS)

```
.MODEL CMOSN NMOS (                                LEVEL   = 49
+VERSION = 3.1          TNOM    = 27            TOX     = 7.7E-9
+XJ      = 1E-7         NCH     = 2.2E17        VTH0    = 0.5121595
+K1      = 0.5552701    K2      = 0.0186698     K3      = 0.0538742
+K3B     = -10          W0      = 1.205177E-5   NLX     = 1.908819E-7
+DVT0W   = 0            DVT1W   = 0             DVT2W   = 0
+DVT0    = 3.9538405    DVT1    = 0.8598993     DVT2    = -0.1996874
+U0      = 432.4300555  UA      = -2.98252E-12  UB      = 1.600316E-18
+UC      = 4.087018E-11 VSAT    = 1.926227E5    A0      = 1.2168698
+AGS     = 0.1792583    B0      = 1.066995E-6   B1      = 5E-6
+KETA    = 5.364714E-3  A1      = 0             A2      = 0.3684583
+RDSW    = 812.3404098  PRWG    = 0.0657941     PRWB    = -0.0936282
+WR      = 1            WINT    = 6.735212E-8   LINT    = 0
+XL      = -2E-8        XW      = 0             DWG     = -6.735256E-9
+DWB     = 3.548415E-9  VOFF    = -0.078735     NFACTOR = 1.2829312
+CIT     = 0            CDSC    = 2.4E-4        CDSCD   = 0
+CDSCB   = 0            ETA0    = 1             ETAB    = 6.277321E-3
+DSUB    = 0.7952596    PCLM    = 1.4453347     PDIBLC1 = 5.21245E-4
+PDIBLC2 = 4.731652E-3  PDIBLCB = 0.0785725     DROUT   = 0.0413584
+PSCBE1  = 5.072986E8   PSCBE2  = 1.787904E-5   PVAG    = 0
+DELTA   = 0.01         RSH     = 3.2           MOBMOD  = 1
+PRT     = 0            UTE     = -1.5          KT1     = -0.11
+KT1L    = 0            KT2     = 0.022         UA1     = 4.31E-9
+UB1     = -7.61E-18    UC1     = -5.6E-11      AT      = 3.3E4
+WL      = 0            WLN     = 1             WW      = 0
+WWN     = 1            WWL     = 0             LL      = 0
+LLN     = 1            LW      = 0             LWN     = 1
+LWL     = 0            CAPMOD  = 2             XPART   = 0.5
+CGDO    = 2.78E-10     CGSO    = 2.78E-10      CGBO    = 1E-12
```

Example of BSIM (PMOS)

```
.MODEL CMOSP PMOS (
+VERSION = 3.1            TNOM    = 27            LEVEL   = 49
+XJ      = 1E-7           NCH     = 8.52E16       TOX     = 7.7E-9
+K1      = 0.4594954      K2      = -0.0165827    K3      = 88.8977872
+K3B     = -5             W0      = 7.515625E-6   NLX     = 2.511816E-7
+DVT0W   = 0              DVT1W   = 0             DVT2W   = 0
+DVT0    = 1.4472839      DVT1    = 0.4769835     DVT2    = -0.0167159
+U0      = 157.2254632    UA      = 1E-10         UB      = 2.103088E-18
+UC      = -1.49211E-11   VSAT    = 2E5           A0      = 1.0641153
+AGS     = 0.3707576      B0      = 2.412043E-6   B1      = 5E-6
+KETA    = -7.666067E-3   A1      = 0             A2      = 0.3
+RDSW    = 3.484979E3     PRWG    = -0.1230866    PRWB    = 0.0388117
+WR      = 1              WINT    = 7.093263E-8   LINT    = 0
+XL      = -2E-8          XW      = 0             DWG     = -1.8394E-8
+DWB     = 1.055952E-8    VOFF    = -0.1190324    NFACTOR = 2
+CIT     = 0              CDSC    = 2.4E-4        CDSCD   = 0
+CDSCB   = 0              ETA0    = 0.1127394     ETAB    = 0.0173484
+DSUB    = 0.7008224      PCLM    = 4.0197889     PDIBLC1 = 9.251931E-3
+PDIBLC2 = 2.748506E-3     PDIBLCB = 0.0131404     DROUT   = 0.0594943
+PSCBE1  = 8E10           PSCBE2  = 5.024895E-10   PVAG    = 3.459432
+DELTA   = 0.01           RSH     = 2.5           MOBMOD  = 1
+PRT     = 0              UTE     = -1.5          KT1     = -0.11
+KT1L    = 0              KT2     = 0.022         UA1     = 4.31E-9
+UB1     = -7.61E-18      UC1     = -5.6E-11      AT      = 3.3E4
+WL      = 0              WLN     = 1             WW      = 0
+WWN     = 1              WWL     = 0             LL      = 0
+LLN     = 1              LW      = 0             LWN     = 1
+LWL     = 0              CAPMOD  = 2             XPART   = 0.5
+CGDO    = 2.96E-10       CGSO    = 2.96E-10      CGBO    = 1E-12
```

Growing number of parmeters



a: BSIM1
b: BSIM2
c: BSIM3 version 2.0
d: BSIM3 version 3.0
e: BSIM3 version 3.1
f: BSIM3 version 3.2.2
g: BSIM4.0.0

BSIM4 : http://www-device.eecs.berkeley.edu/bsim/bsim_ent.html
Model 11 : http://www.semiconductors.philips.com/Philips_Models/mos_models/model11/index.html
EKV : http://legwww.epfl.ch/ekv/model.html

EKV Model

- **SPICE**

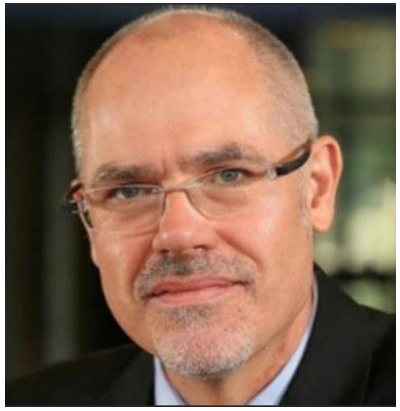
  Simulation Program with Integrated Circuit Emphasis

- **BSIM**

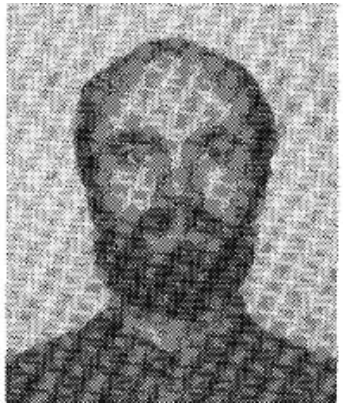
  Berkeley Short Channel IGFET Model

- **EKV**

  Christian C. Enz, Francois Krummenacher, Eric Vittoz



1957 ~



1955 ~

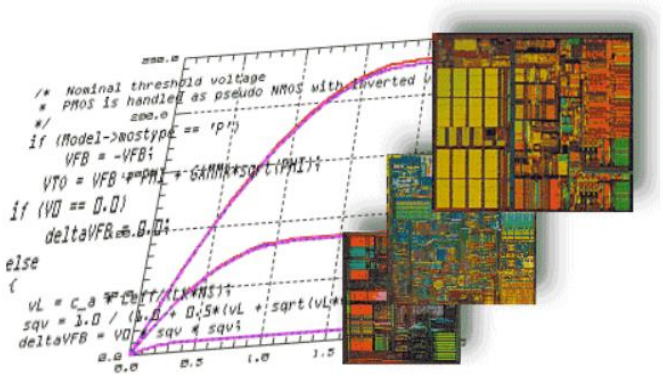
1938 ~

EKV Model: for weak inversion

- **EKV**

  Based on voltage of the bulk

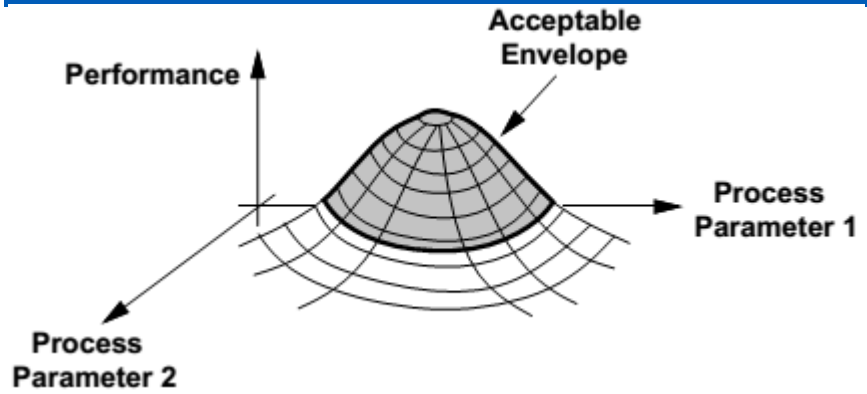
  I_{ds} equation for weak and strong inversion



BSIM and **EKV** groups have agreed to collaborate on the long-term development and support of BSIM6 as a world-class open-source MOSFET SPICE model for the international community for years to come. This is an exciting opportunity to leverage the long experience and widespread adoption of the BSIM model with the long experience and active role of EKV in furthering charge-based compact model.

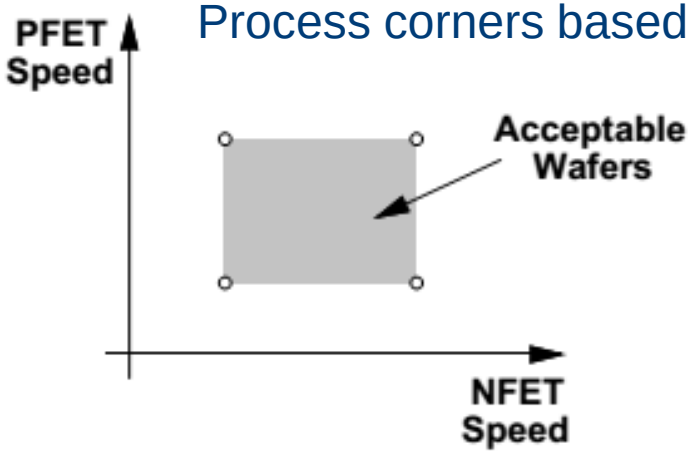
Prof. C.Hu and Prof. C. Enz at MOS-AK/GSA in Helsinki

Process Corner(工艺角)



- Process engineers guarantee a performance envelope for the devices.
- The idea is to constrain the speed envelope of the NMOS/PMOS transistors to a rectangle defined by four corners – called process corners.

Process corners based on speed of NMOS and PMOS devices



S: slow
F: fast
T: typical

TT, FF, FS, SS, SF

Examples

- Settings: P. V. T.
  Voltage: +- 10%
  Temperature: -10~80 ºC

Corners	Nominal	C0_block	C1_block	C2_block	C3_block	C4_block	C5_block	C6_block	C7_block	C8_block	...MM_block	MM_block
Temperature												
Design Variables												
temperature		-10 20 80	-10 20 80	-10 20 80	-10 20 80	-10 20 80	-10 20 80	-10 20 80	-10 20 80	-10 20 80	-10 20 80	20
vdd		1.05 1.2 1.3	1.05 1.2 1.3	1.05 1.2 1.3	1.05 1.2 1.3	1.05 1.2 1.3	1.05 1.2 1.3	1.05 1.2 1.3	1.05 1.2 1.3	1.05 1.2 1.3	1.05 1.2 1.3	1.2
Click to add												
Parameters												
Click to add												
Model Files												
Click to add												
Model Group(s)		TTTT	SSTT	FFTT	SFTT	FSTT	TTFT	TTST	SSSS	FFFF	MCMM	MMTT
Click to add												
Tests												
...:TB_NonOverl:1	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Number of Corners	1	9	9	9	9	9	9	9	9	9	9	1

Single-Page MOSFET Model

$$I_{DS} = K'_n \frac{W}{L} (V_{GS}-V_T)^2$$

$V_{GS}-V_T \approx 0.2$ V

$K'_n = \frac{1}{2}\mu_n C_{ox}$

$K'_n \approx 100\ \mu A/V^2$

$K'_p \approx 40\ \mu A/V^2$

$$g_m = 2K'_n \frac{W}{L} (V_{GS}-V_T) = 2\sqrt{K'_n \frac{W}{L} I_{DS}} = \frac{2 I_{DS}}{V_{GS}-V_T}$$

$$r_{DS} = r_o = \frac{V_E L}{I_{DS}}$$

$$r_O = \frac{1}{I_D \lambda}$$

$V_{En} \approx 5$ V/μmL $V_{Ep} \approx 8$ V/μmL

$v_{sat} = 10^7$ cm/s

$$f_T = \frac{1}{2\pi} \frac{3}{2n} \frac{\mu}{L^2} (V_{GS}-V_T) \quad \text{or now} \approx \frac{v_{sat}}{2\pi L}$$

$$f_T = \frac{g_m}{2\pi C_{GS}}$$

Appendix: Single-page Bipolar Transistor Model

$$I_{CE} = I_S \exp^{\frac{V_{BE}}{kT/q}}$$

$I_S \approx 10^{-15}$ A kT/q = 26 mV at 300 K

$$g_m = \frac{I_{CE}}{kT/q} \qquad r_o = \frac{V_E}{I_{CE}}$$

$V_{En} \approx 20$ V $V_{Ep} \approx 10$ V

$$f_T = \frac{1}{2\pi} \frac{1}{\tau_F + \frac{C_{je}+C_{jc}}{g_m}}$$

$$\text{or} \approx \frac{v_{sat}}{2\pi W_B}$$

Willy Sansen 10-05 0182

Appendix: SPICE Simulation of MOS Circuit

M<number> <DRAIN> <GATE> <SOURCE> <BULK>
modelname parameters

Example：M1 3 6 7 0 NCH W=100u L=1u

.MODEL <modelname> <model type> <model parameters>

convergence

ABSTOL default value 1pA

VNTOL default value 1uV

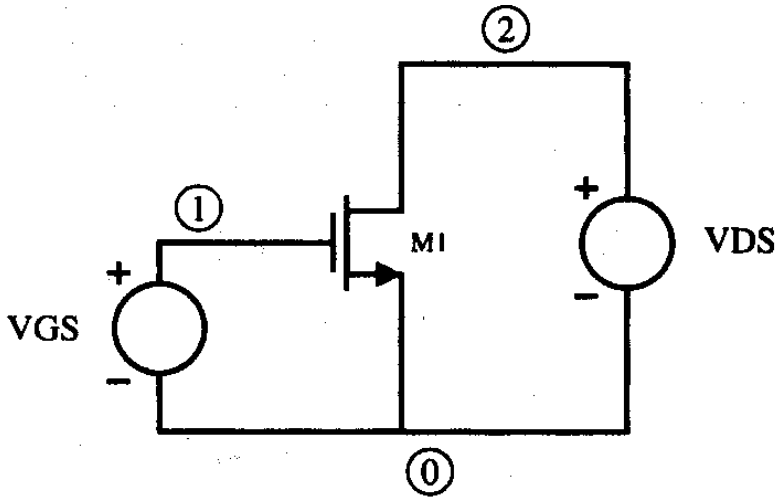
RELTOL default value 0.001(0.1%)

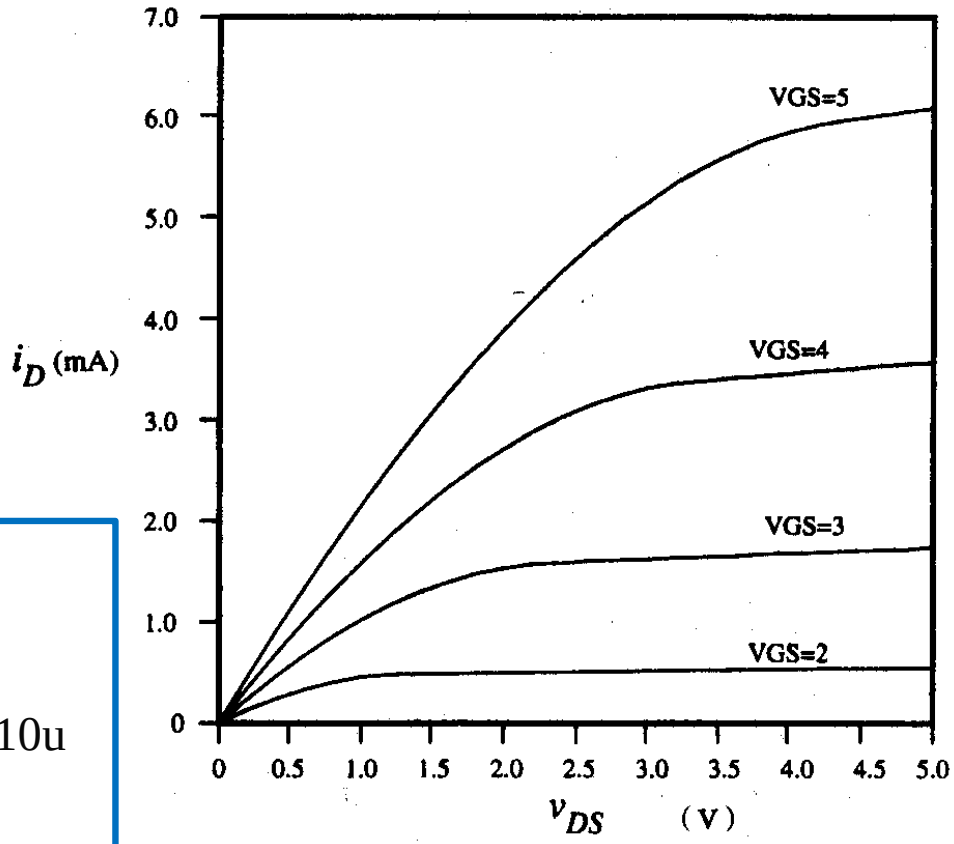
Example:
.OPTIONS ABSTOL=1uA VNTOL=1mV RELTOL=0.01

Cost: Accuracy

Example

Use of SPICE to simulate MOS output characteristics





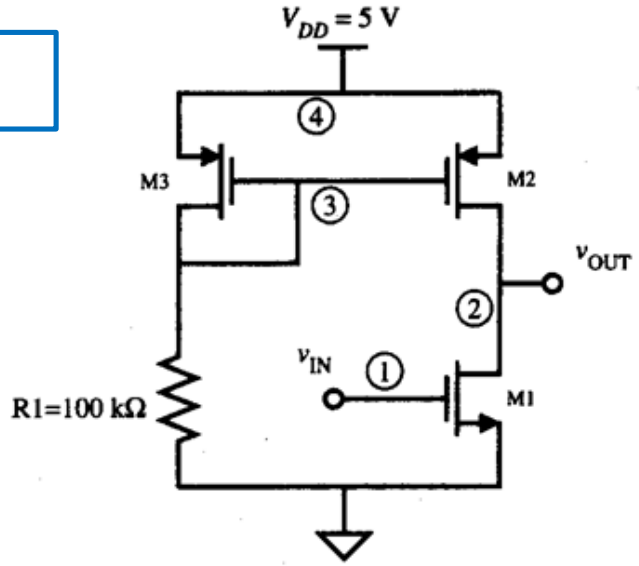

```
M1        2  1  0  0 MOS1 w=5u l=1.0u
VDS       2  0  5
VGS       1  0  1
.model    MOS1 NMOS VT0=0.7 KP=110u
GAMMA=0.4 LAMBDA=0.04 PHI=0.7
.dc VDS 0  5  0.2  VGS  1 5  1
.print DC V(2)  I(VDS)
.end
```

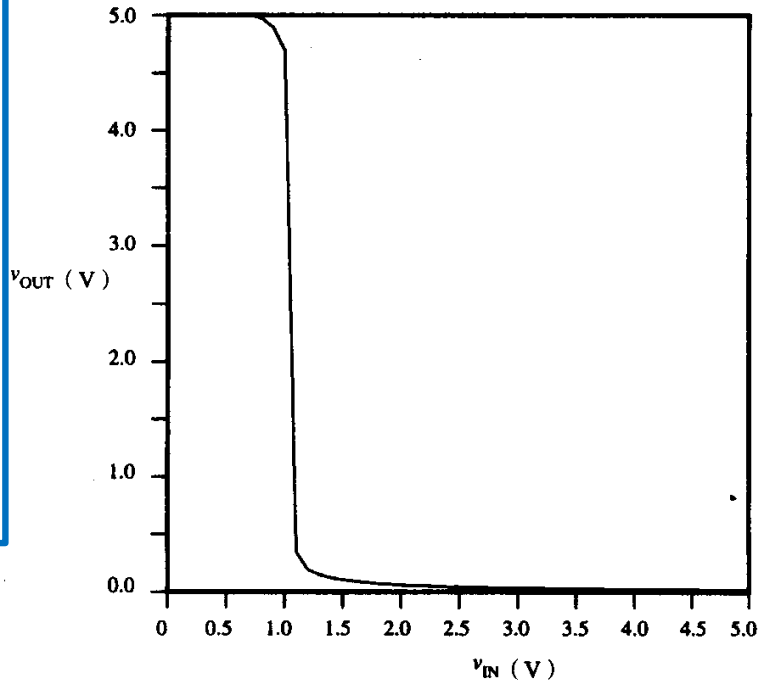
Example

DC Analysis of Fig.

EX. DC Analysis of Fig. 2.48.

```
M1      2  1  0  0 MOSN w=5u l=1.0u
M2      2  3  4  4 MOSP w=5u l=1.0u
M3      3  3  4  4 MOSP w=5u l=1.0u
R1      3  0  100k
VDD     4  0  DC  5.0
VIN     1  0 DC  5.0
.model MOSN NMOS VT0=0.7 KP=110u
GAMMA=0.4 LAMBDA=0.04 PHI=0.7
.model MOSP  PMOS VT0=-0.7 KP=50u
GAMMA=0.57 LAMBDA=0.05 PHI=0.8
.dc VIN  0  5  0.1
.print DC V(2)
.end
```





Summary

- Model philosophy for IC design
  - Use **simple models** for design and sophisticated model for verification
- Models have several parts
  - Large signal static (DC variables)
  - Small signal static (gains, input/output resistances)
  - Small signal dynamic (frequency response, noise)
  - Large signal dynamic (slew rate)
  - In addition models may include
    - Temperature
    - Noise
    - Process variations (Monte Carlo method)
- Computer models
  - Must be numerically efficient
  - Quickly derived from new technology

Analog Design “Tricks”:
Stay away from minimum channel length if possible
⇨ Larger r_o -> large gains Better agreement
Don’t use the computer models for design, rather verification of design

Outline

- Review: Diodes
- MOS I/V Characteristics
- MOS Device Models
- MOS Short-Channel Effect
- MOS SPICE Models

集成电路原理与设计

4.器件模型二

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