1. Explain the Abbreviations (English and Chinese) 3X15 = 45 pts

e.g. 例子: IC: Integrated Circuits 集成电路

(1) CMOS Complementary Metal Oxide Semiconductor 互补金属氧化物半导体

(2) DSP Digital Signal Processor 数字信号处理器

(3) FPGA Field Programmable Gate Array 现场可编程逻辑门阵列

(4) ASIC Application Specific Integrated Circuit 专用集成电路

(5) CVD Chemical Vapor Deposition 气相沉积法

(6) SOI Silicon on Insulator 绝缘体上硅

(7) DRC/LVS Design Rule Check 设计规则检测/ Layout Versus Schematics 验证版图和逻辑图

(8) C_{GS} / C_{BD}

(9) Cascode/Cascade (中文) 共源共栅/水平级联

(11) PTAT Proportional to Absolute Temperature 与绝对温度成正比

(12) ZTC Zero Temperature Coefficient 零温度系数

(13) OTA operational transconductance amplifier 跨导运算放大器

(14) SiP System In a Package 系统级封装

(15) ISSCC/JSSC IEEE International Solid-State Circuits Conference 国际固态电路会议/ IEEE Journal of Solid-State Circuits IEEE 固态电路学报

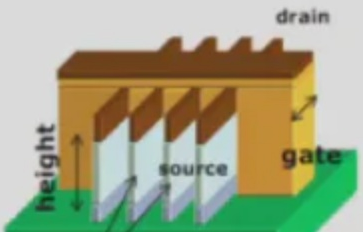
2. Short Questions 4X8 = 32 pts

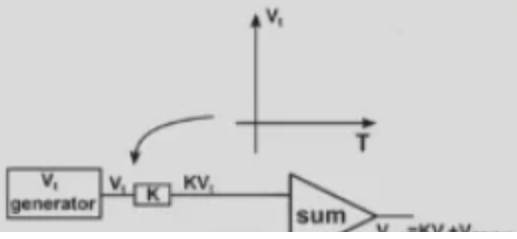
(1) Moore's Law refers to Gordon Moore's perception that the number of _transistors_ (what) on a microchip _doubles_ (change how many times) every 18-24 month, though the cost of computers is halved.

(2) _Analog_ (Analog/Digital) IC design differs greatly from digital IC design. Where _digital_ (analog/digital) IC design is mostly done at an abstracted level with HDL (Hardware Description Language), _analog_ (analog/digital) IC design generally involves more personalized focus into each transistor, determining the sizing of each.

(3) Modern CMOS technologies involve roughly the following operations: (1) Wafer Preparation: produce the proper type of substrate; (2) _ lithography _: (step name) precisely define each region by light; (3) Oxidation, deposition and _ion_ (what) implantation: add materials to the wafer; (4) Etching: remove materials from the wafer

(4) The type of transistors in the following figure.1 is _FinFET_ (Planar MOS/FinFET), which is invented for _advanced_ (conventional/advanced) technology node like 14nm CMOS.





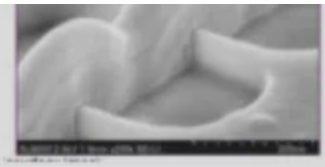


Fig. 1

Fig. 2

(5) An NMOS transistor with a _ higher _ (lower/higher) Vds tends to work in saturation region. In saturation region, it usually has a _lower_ (higher/lower) small signal resistance (r_o) compared to linear region.

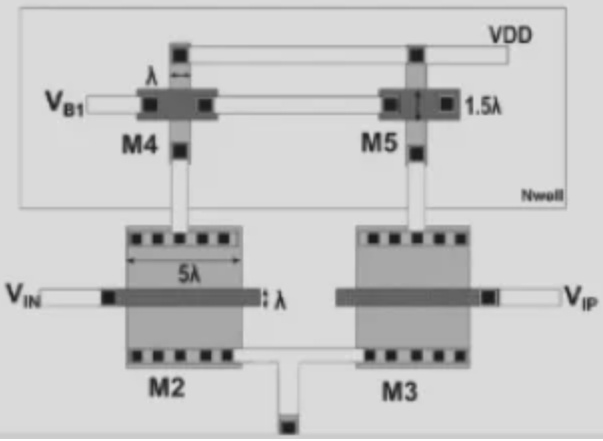
(6) An NMOS transistor (working at saturation region) at FF corner has a _lower_ (lower/higher) threshold voltage (Vth) than at TT corner. The same transistor at SS corner has a _higher_ (lower/higher) trans-conductance (gm) than at TT corner.

(7) An NMOS transistor working as a switch has _lower_ (higher/lower) resistance than a PMOS based switch. That is the reason why a transmission gate (consisting of a PMOS and an NMOS transistor) use a larger W/L ratio for _ PMOS _ (NMOS/PMOS).

(8) The Vbe is the following figure has a _negative_ (positive/negative) temperature coefficient(TC), the KVt has a _positive_ (positive/negative) TC. A bandgap reference provides a stable output voltage at both temperature and _voltage_ (what) range.

3. Calculation 5 + 8 + 10 = 23 pts

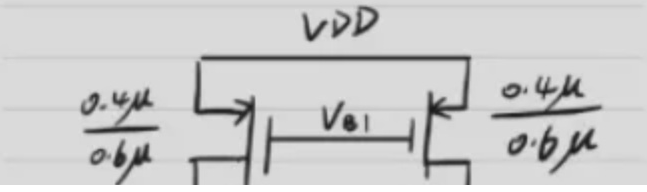
(1) The Layout of a different pair with PMOS current source loads in p-sub N-well technology is shown as the following figure. (5 pts)

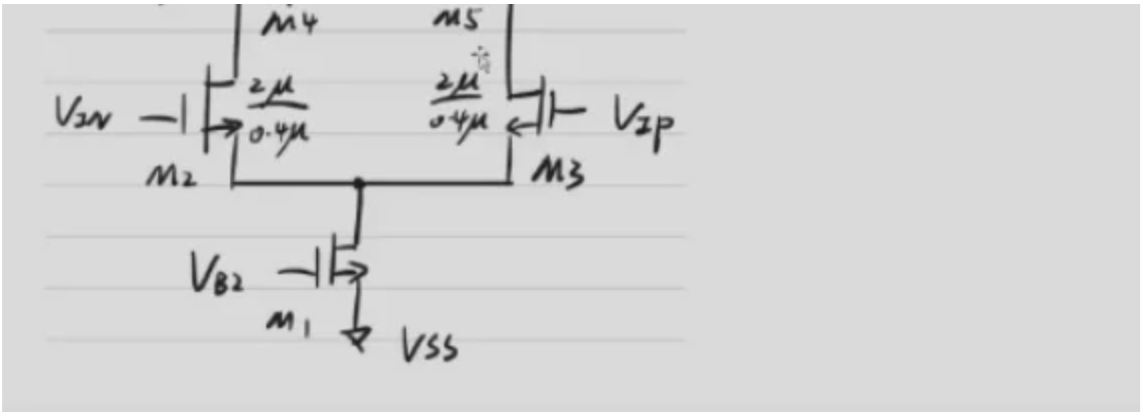


(a) Give the corresponding circuits schematics and mark the W/L sizes of each transistor. Assume λ=0.4μm.

(b) To achieve better matching of the input pair (M2 and M3), draw an alternative layout configuration. (by using multiple transistors with smaller W/L)

Answer:

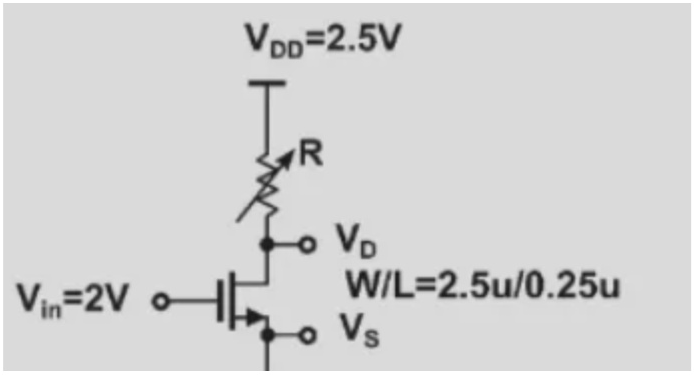




(2) An NMOS device is used within the topology shown in the following figure. The input Vin is 2 V. The current source draws a constant current of 50 μA. R is a variable resistor between 10kΩ and 30 kΩ. Transistor M1 has following transistor parameters: $k' = 110\mu A/V^2$, $V_{TH} = 0.7V$, $V_{DSSAT} = 0.6V$, and has a W/L = 2.0μ/0.4. For simplicity, the body effect and channel length modulation can be neglected, i.e λ=0, γ=0. (8 pts)

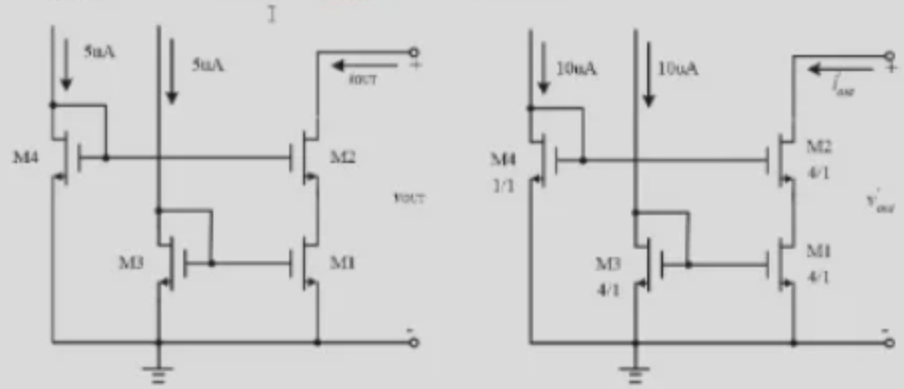
a) When R =12kΩ find the operation region, V_D and V_S.

b) For the case of R = 12kΩ, would V_S increase or decrease if λ ≠ 0 (when there is channel length effect)? and explain why.



(3) There are two cascode current mirror shown in the following figures (10 pts)

(a) Design M3 and M4 of (a) so that the output characteristics are identical to the circuit shown in Fig. (b). It is desired that IOUT is ideally 10uA.



(a) (b)