集成电路原理与设计
2. 器件模型一

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Syllabus

课数	内容	课数	内容
1	导论	9	差分放大器
2	器件模型一	10	运算放大器
3	器件模型二	11	逻辑门
4	工艺流程	12	组合逻辑
5	模拟基本单元	13	时序逻辑
6	电流镜与基准	14	加法器/乘法器
7	单级放大器	15	集成电路专题讲座一
8	课堂测验	16	集成电路专题讲座二

Recall the last chapter

- Technology scaling down (digital driven) with Moore's Law
- What is IC, CMOS, SoC, SiP, CPU and MCU?
- Analog Design Flow
- Digital Design Flow
- Analog vs. Digital with technology scaling down
- ISSCC & JSSC

Goal of this chapter

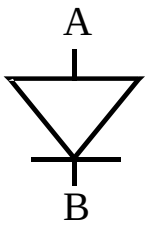
- Present **intuitive understanding** of device operation
- Introduction of **basic device equations and models** for **manual** analysis
- Analysis of **second effects**
- Introduction of models for SPICE simulation
- Future trends

Outline

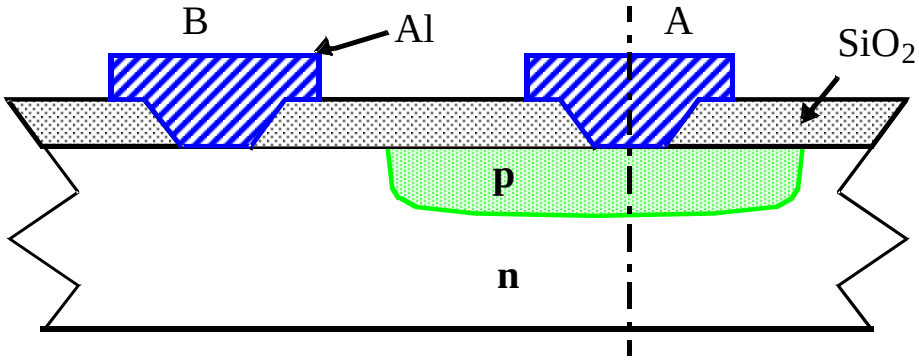
- **Review：Diodes**
- **MOS I/V Characteristics**
- **MOS Device Models**
- **MOS Short-Channel Effect**
- **MOS SPICE Models**

Reference:
Chapter 2/17, <Design of Analog CMOS Integrated Circuits>Razavi著

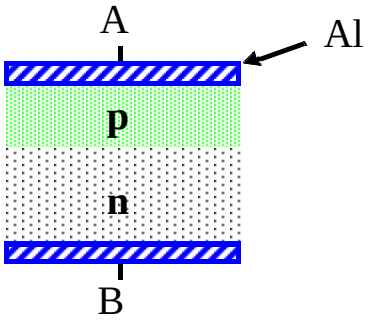
The Diode



Diode Symbol

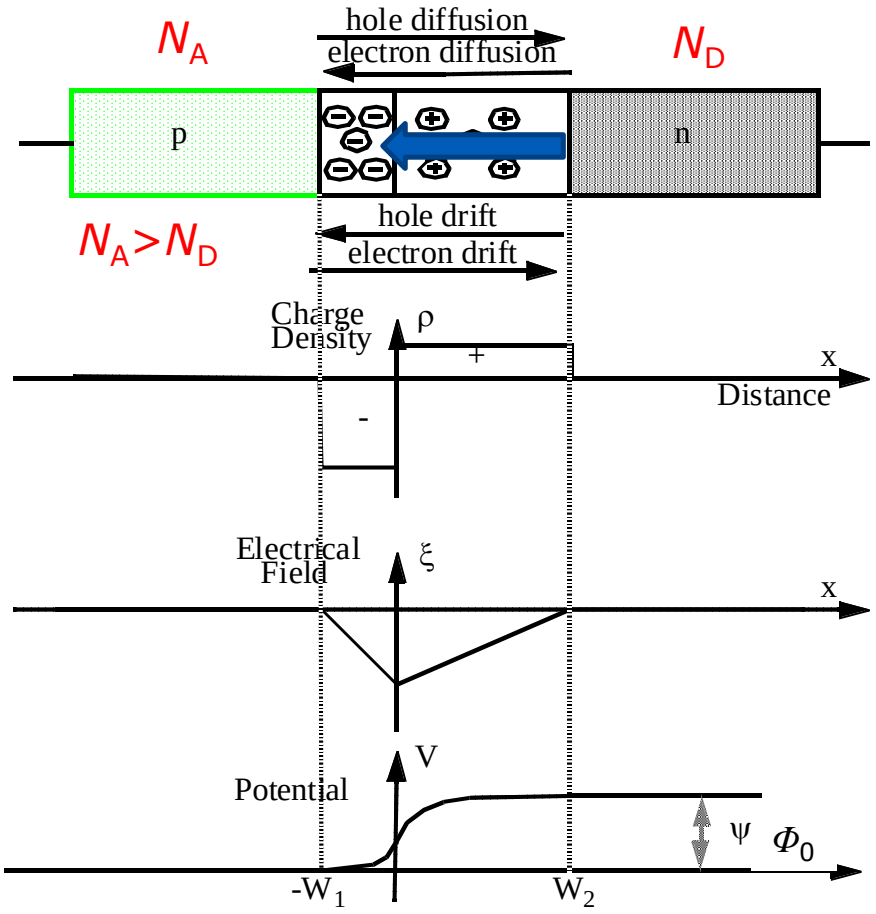


Cross-section of *pn*-junction in an IC process



One-dimensional representation

Depletion Region(耗尽区)



The abrupt *pn*-junction under equilibrium bias

耗尽区或空间电荷区

Built-in potential (内建电势):

$$\phi_0 = \phi_T \ln[\frac{N_A N_D}{n_i^2}]$$

Thermal voltage:

$$\phi_T = \frac{kT}{q} = 26mV \ (300\text{K})$$

Depletion Region

- Depletion-region charge

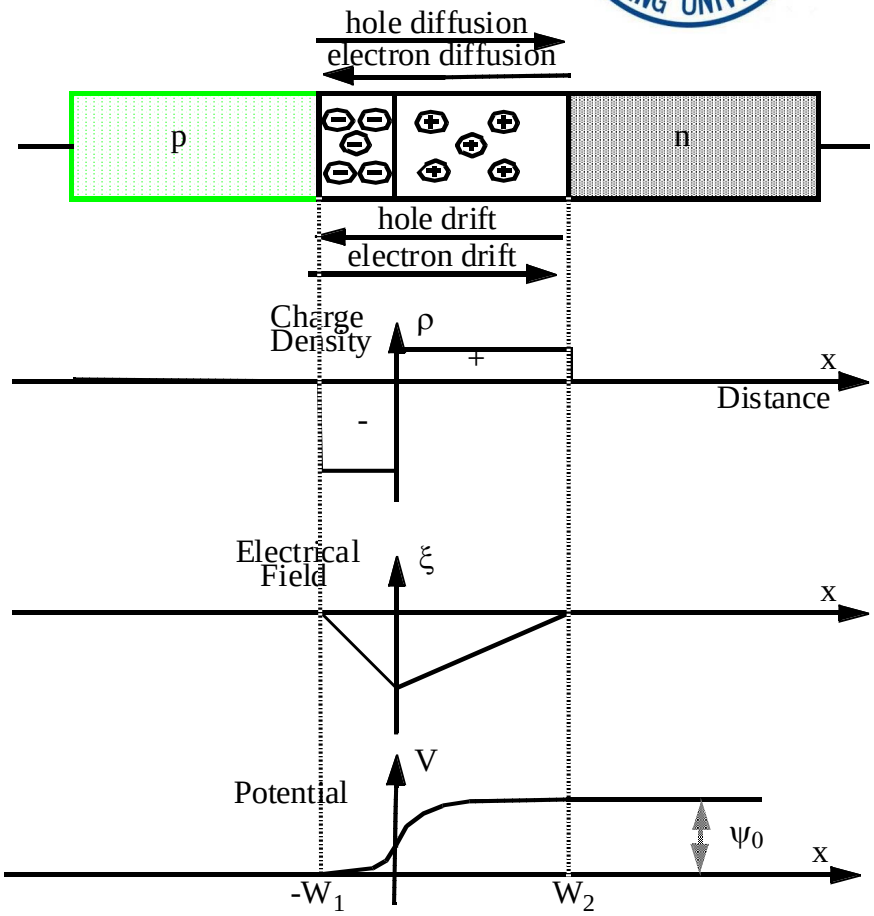
$$Q_j = A_D\sqrt{(2\varepsilon_{si}q\frac{N_A N_D}{N_A+N_D})(\phi_0 - V_D)}$$

- Depletion-region width

$$W_j = W_2 - W_1 = \sqrt{(\frac{2\varepsilon_{si}}{q}\frac{N_A+N_D}{N_A N_D})(\phi_0 - V_D)}$$

- Maximum electric field

$$E_j = \sqrt{(\frac{2q}{\varepsilon_{si}}\frac{N_A N_D}{N_A+N_D})(\phi_0 - V_D)}$$



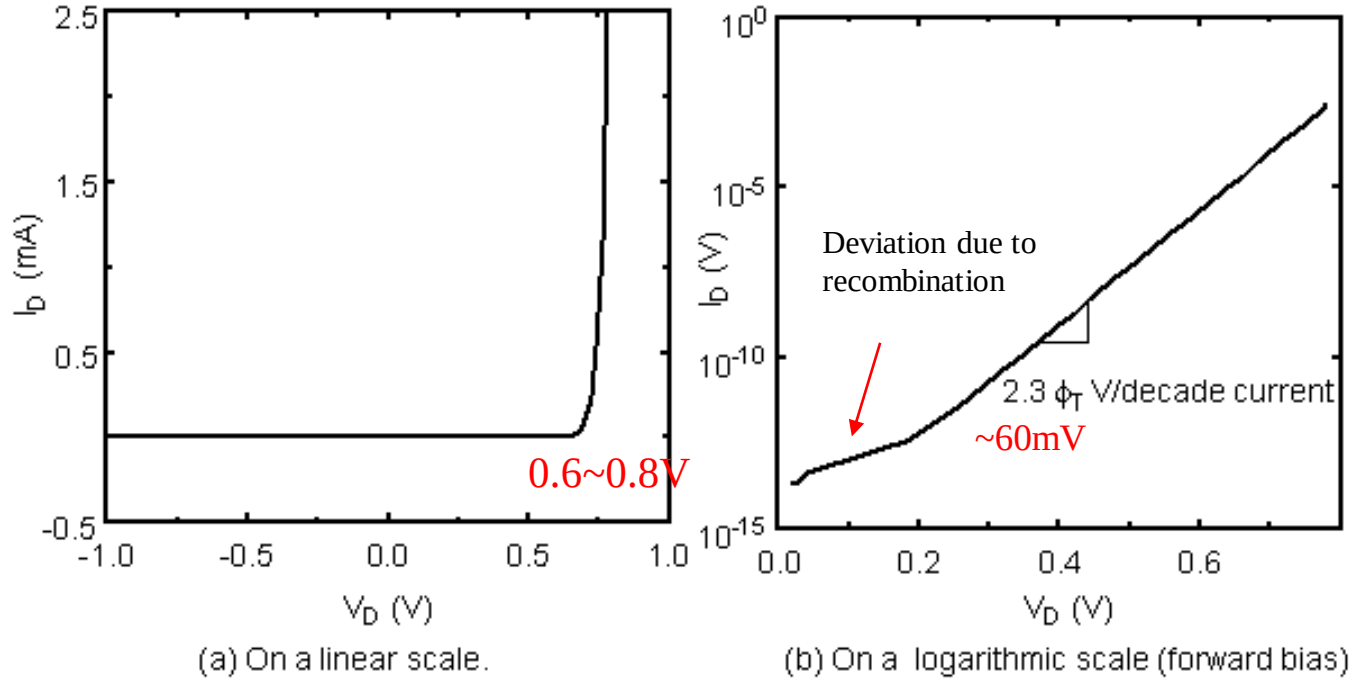
V_D（forward voltage vs. **reverse voltage）is applied to the junction?**

Diode Current

$$I_D = I_S\left(e^{V_D/\varphi_T} - 1\right)$$

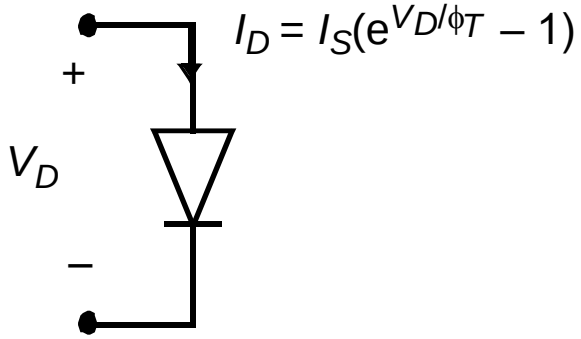
$$\phi_T = \frac{kT}{q} = 26mV \ (300\text{K})$$

- *I*s (the saturation current): a constant value ~10^{-17}A/μm^2
  - -- be proportional to **the area** of the diode
  - -- temperature-dependent double every ~5~8° C



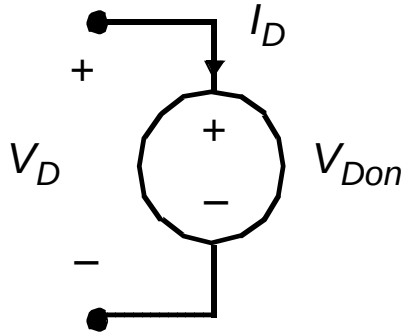
(a) On a linear scale. (b) On a logarithmic scale (forward bias)

Models for Manual Analysis



(a) Ideal diode model

strongly nonlinear



~0.7V

(b) First-order diode model

conducting diode: V_{Don}: 0.6~0.8V

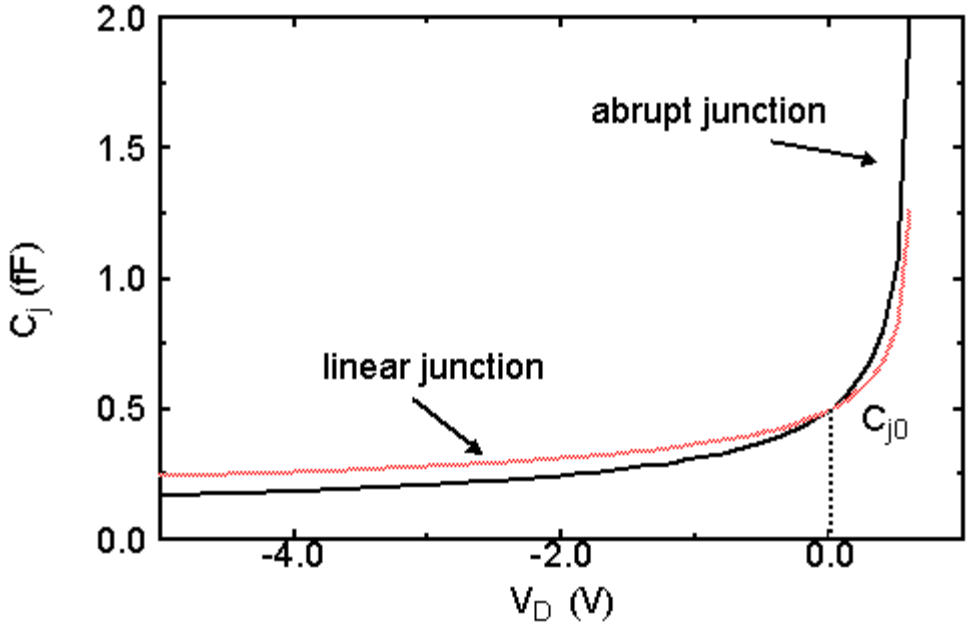
non-conducting diode: open

Depletion-layer capacitance

- *pn*-junction is an abrupt junction

$$C_j = \frac{dQ_j}{dV_D} = A_D\sqrt{(\frac{\varepsilon_{si}q}{2}\frac{N_A N_D}{N_A+N_D})(\phi_0 - V_D)^{-1}} = \frac{C_{j0}}{\sqrt{1-V_D/\phi_0}}$$

$$C_{j0} = A_D\sqrt{(\frac{\varepsilon_{si}q}{2}\frac{N_A N_D}{N_A+N_D})\phi_0^{-1}}$$ （zero-bias conditions）



$$C_j = \frac{C_{j0}}{(1 - V_D/\phi_0)^m}$$

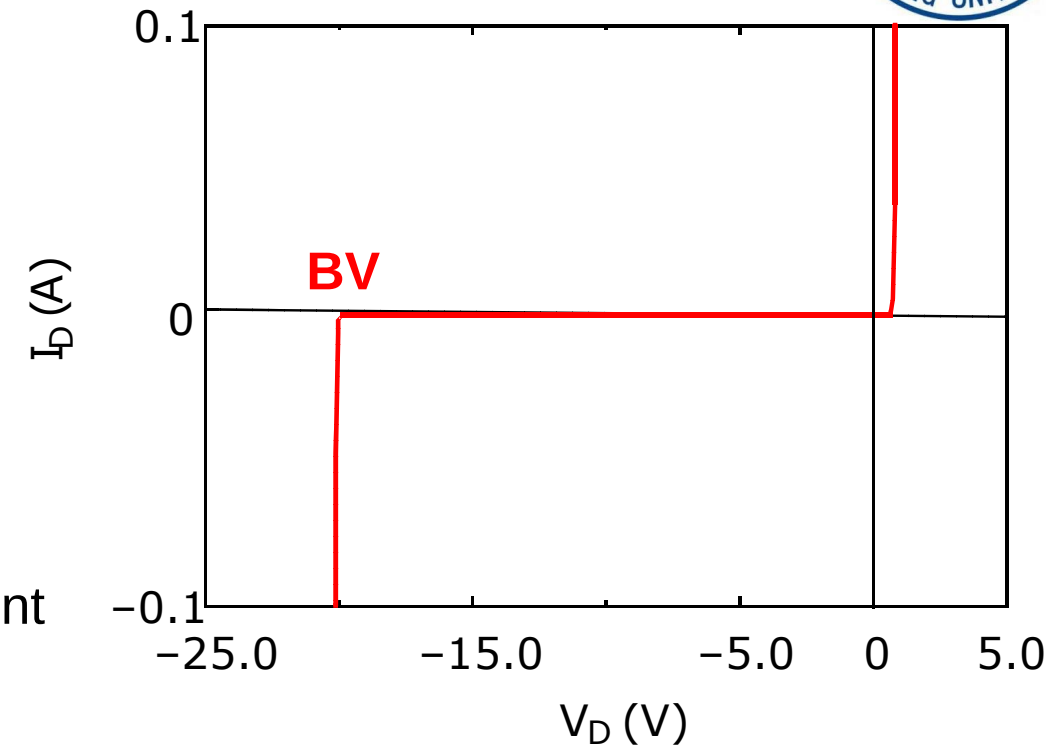
m = 0.5: abrupt junction
m = 0.33: linear junction

Secondary Effects

- Breakdown

$$E_{\max} = 3\times10^5\, V/cm$$

$$BV \cong \frac{\varepsilon_{Si}\left(N_A + N_D\right)}{2qN_AN_D}E_{\max}^2$$



- Temperature-dependent

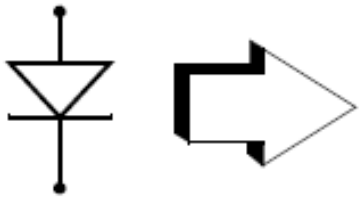
$$I_D = I_S\left(e^{V_D/\varphi_T} - 1\right)$$

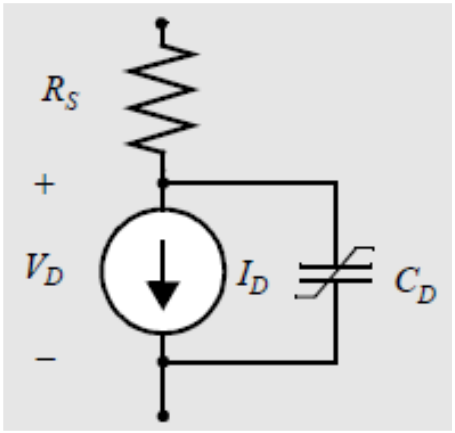
T↑ I_D ↑ power↑

I_D ↑ : +6%/℃ double/12℃

V_D ↑ : -2mV/℃

SPICE Diode Model





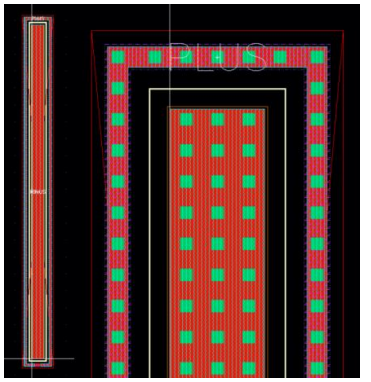
$$I_D = I_S(e^{V_D/n\phi_T} - 1)$$

$$C_D = \frac{C_{j0}}{(1 - V_D/\phi_0)^m} + \frac{\tau_T I_S}{\phi_T} e^{V_D/n\phi_T}$$

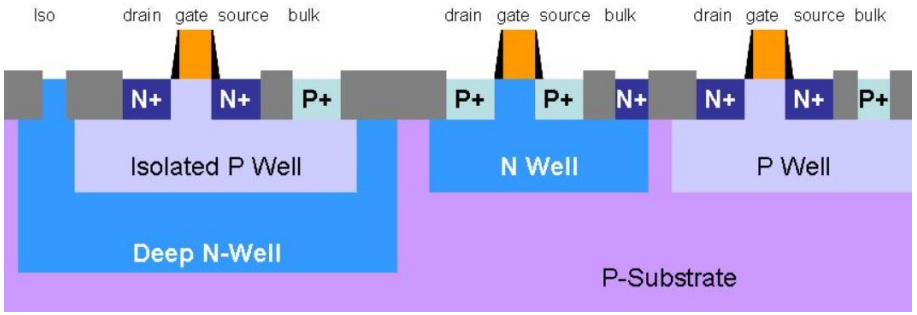
Parameter Name	Symbol	SPICE Name	Units	Default Value
Saturation current	I_S	IS	A	1.0 E–14
Emission coefficient发射系数	n	N	–	1
Series resistance	R_S	RS	Ω	0
Transit time	τ_T	TT	s	0
Zero-bias junction capacitance	C_{j0}	CJ0	F	0
Grading coefficient	m	M	–	0.5
Junction potential	ϕ_0	VJ	V	1

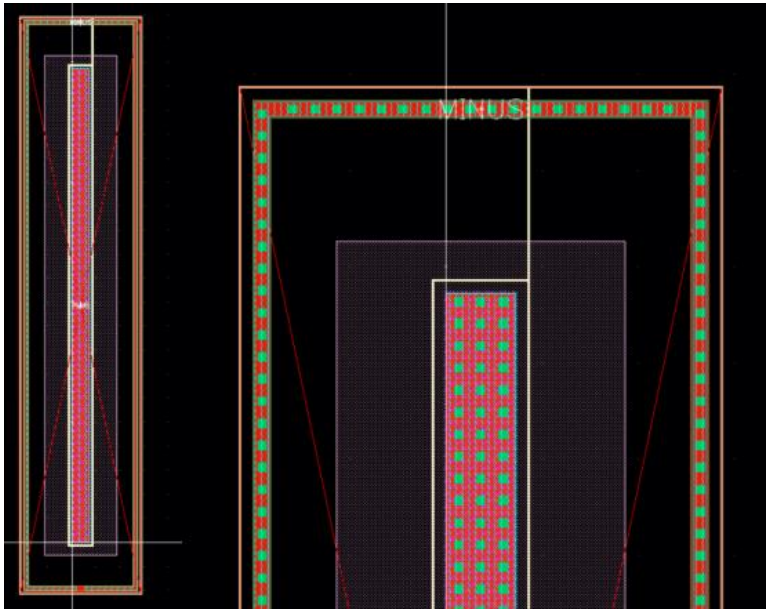
Diodes in IC Process

- P-sub surrounding Nwell



- Nwell/DNW surrounding P-sub



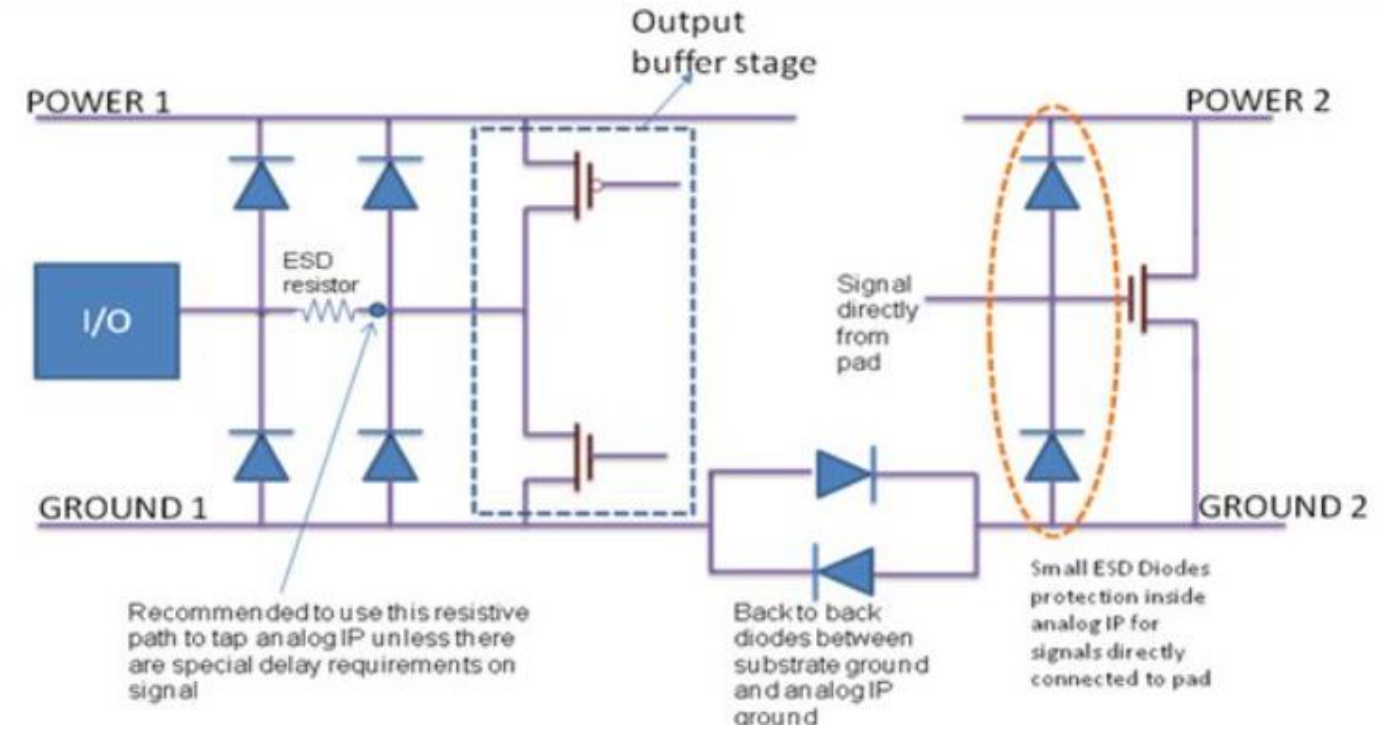


The Deepnwell-Nwell is a bow

Why the substrate is P type?

Diodes in IC Design (1)

- Mainly for ESD devices

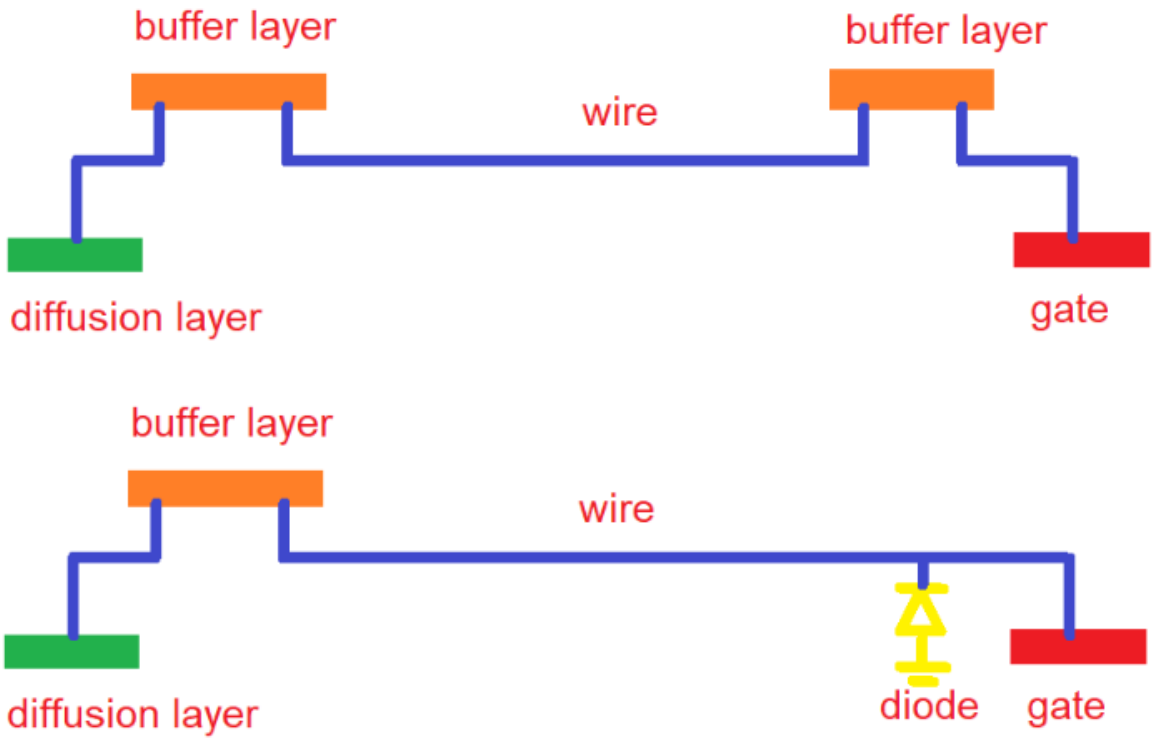


Provide a path for electrostatic charge

Direct connect to gate of a transistor ☹

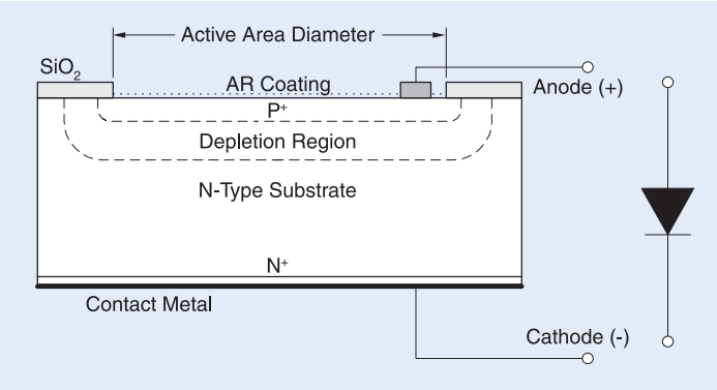
Diodes in IC Design (2)

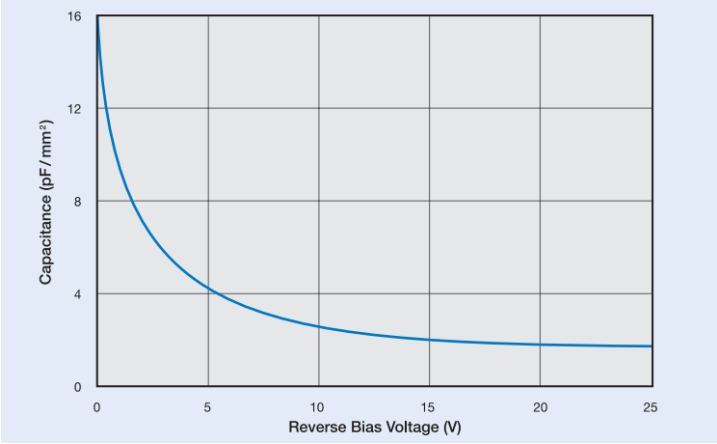
- To alleviate process antenna effect



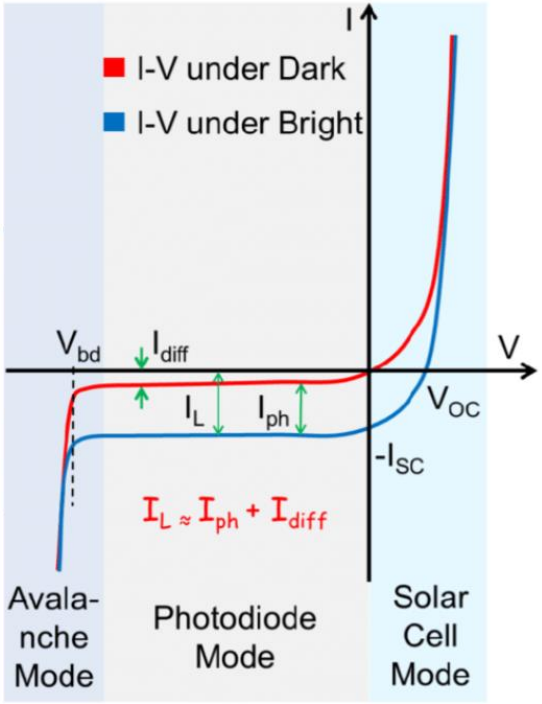
Diodes in IC Design (3)

Photodiode





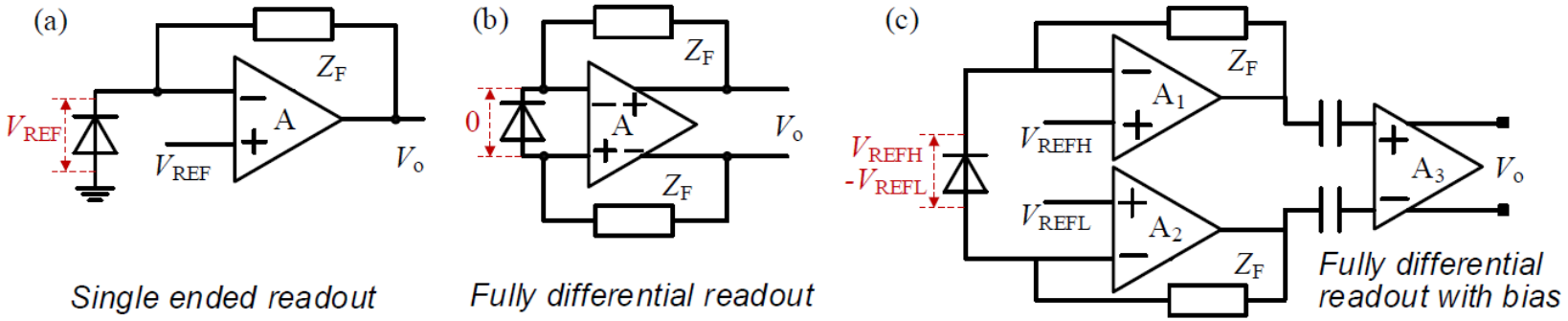
V_{OC}	Open Circuit Voltage
V_{bd}	Break Down Voltage
I_L	Total Photodiode Current
I_{ph}	Photon Current
I_{diff}	Diffusion Current



Light current is a reverse current -> from N to P

Diodes in IC Design (4)

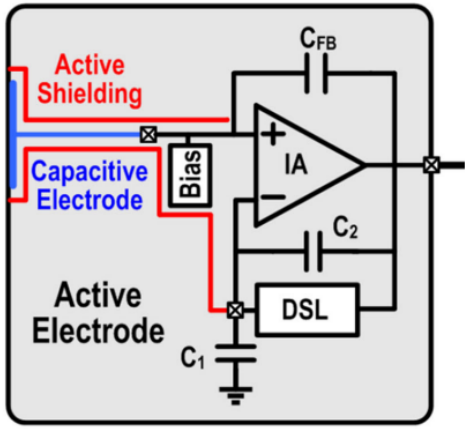
- Trans-impedance amplifier

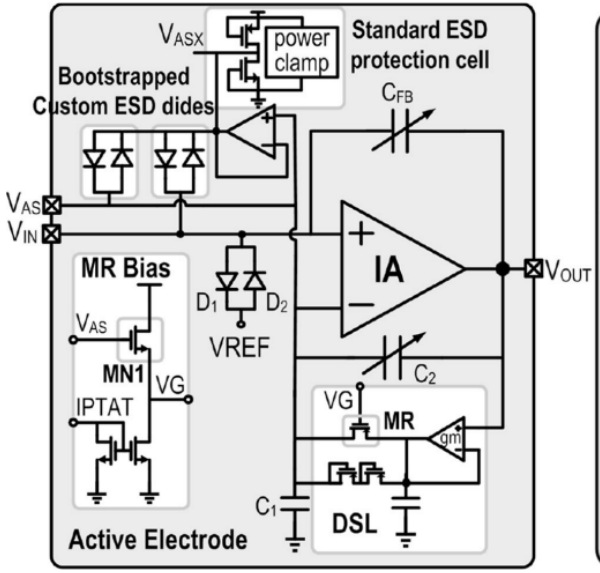


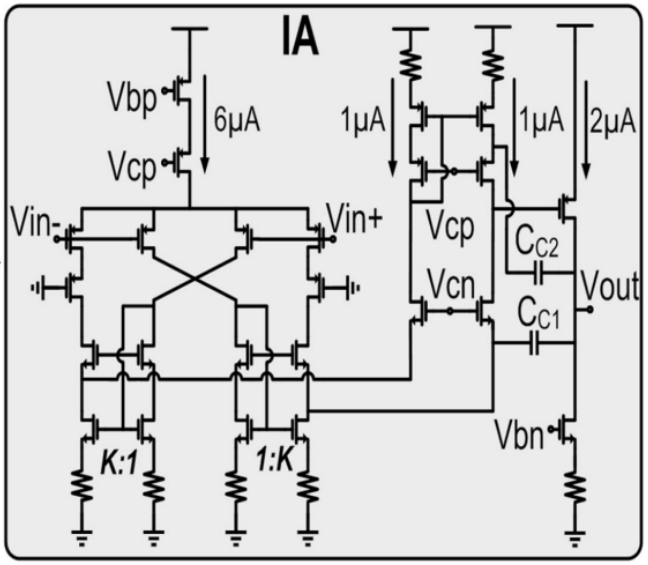
- *From current signal to voltage signal*
- *Parasitic capacitance matters !*

Diodes in IC Design (5)

- Input Impedance boosting for I/O devices







Parasitic capacitance matters !

M. Chen *et al.*, "A 400 GΩ Input-Impedance Active Electrode for Non-Contact Capacitively Coupled ECG Acquisition With Large Linear-Input-Range and High CM-Interference-Tolerance," in *IEEE Transactions on Biomedical Circuits and Systems*, vol. 13, no. 2, pp. 376-386, April 2019

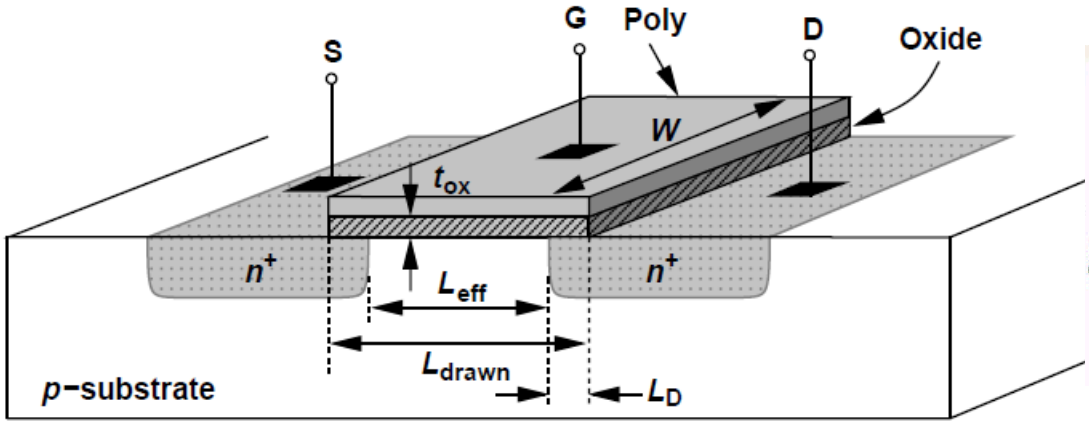
Summary

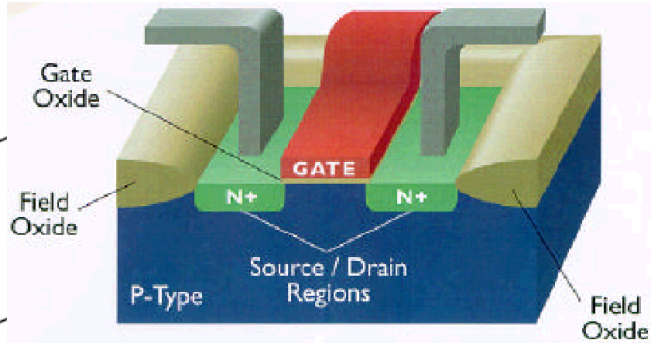
- Diode conducts when a voltage is applied
- The parasitic cap. is reversely proportional to v-n voltage
- Diodes are mainly used for electrostatic charge protection
- Diodes can be implemented by P-sub/Nwell/DeepNwell
- Any diode is a photodiode!

Outline

- Review：Diodes
- MOS I/V Characteristics
  - General Considerations
  - MOS I/V Characteristics
  - Second-Order Effects
- MOS Device Models
- MOS Short-Channel Effect
- MOS SPICE Models

MOSFET Structure





- NMOS has *n*-doped source (S) and drain (D) on *p*-type substrate ("bulk" or "body")

  S: provide charge carriers

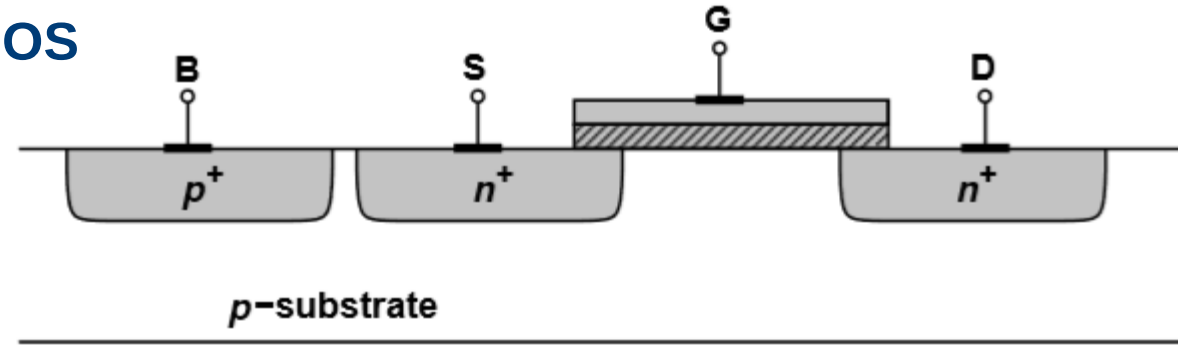
  D: collecte charge carriers
- S/D junctions "side-diffuse"(横向扩散 -> L_D)

  ⇨ the effective length $L_{eff} = L_{drawn} - 2L_D$.
- As voltages at the three terminals changes, the source and drain may exchange roles.

Drain and Source are made identical in process

MOSFET Structure：4 terminals

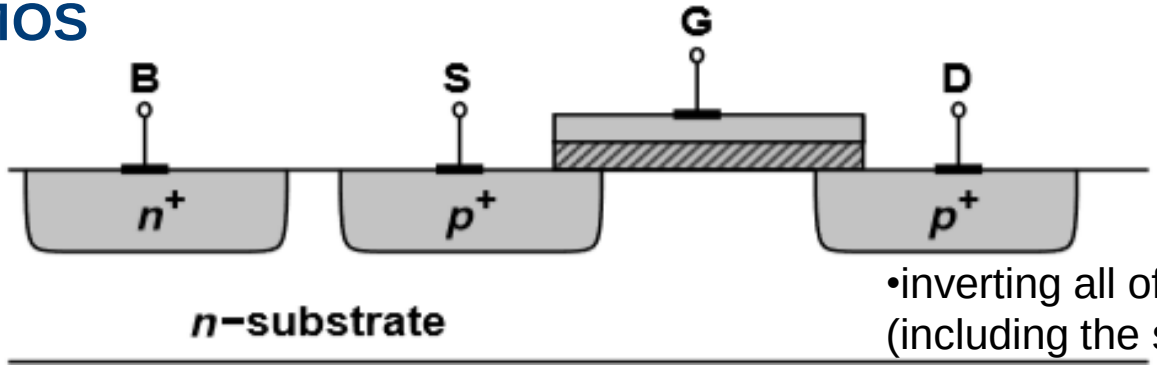
NMOS



- MOSFETs actually have **four terminals**.
- Substrate potential greatly influences device characteristics.
- Typically **S/D junction diodes are reversed-biased** and the NMOS substrate is connected to the most negative supply in the system.

GND or V_{SS}

PMOS

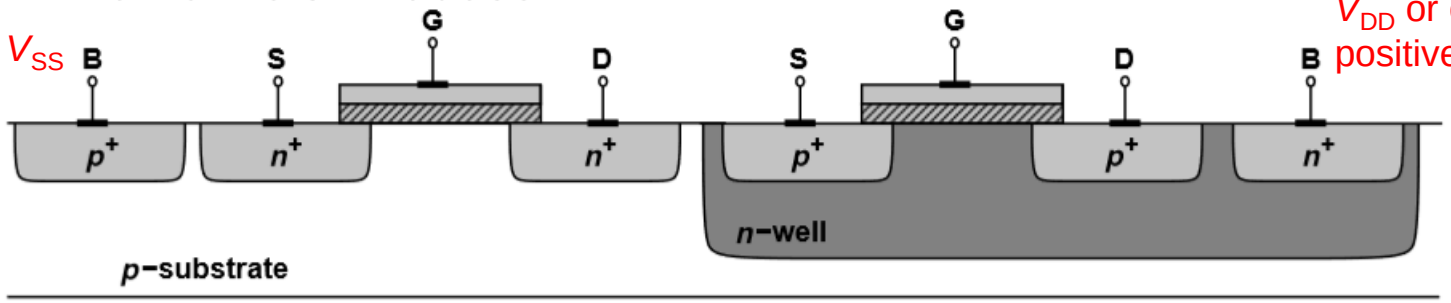


•inverting all of the doping types (including the substrate).

MOSFET Structure：N-well or dual-well

- N-Well CMOS Process

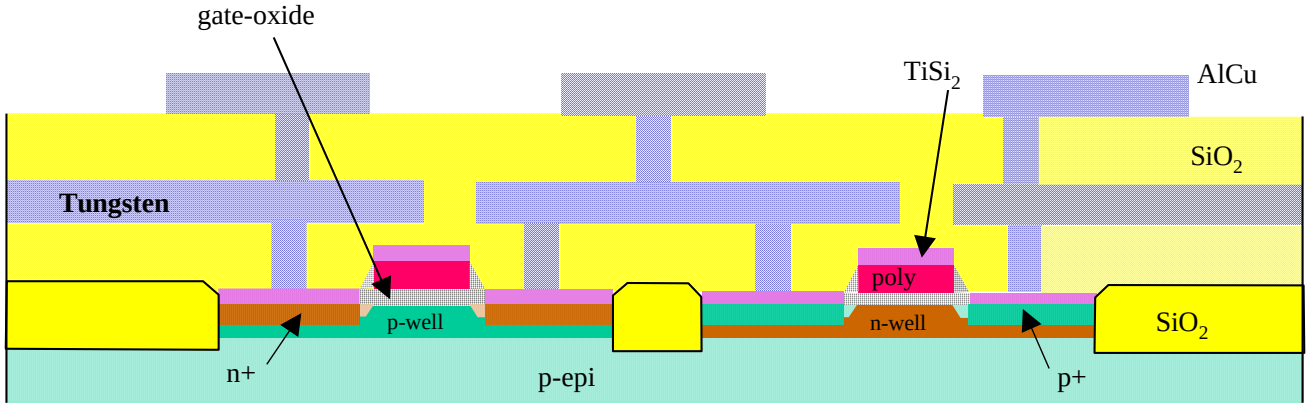
GND or V_{SS} V_{DD} or other positive potential



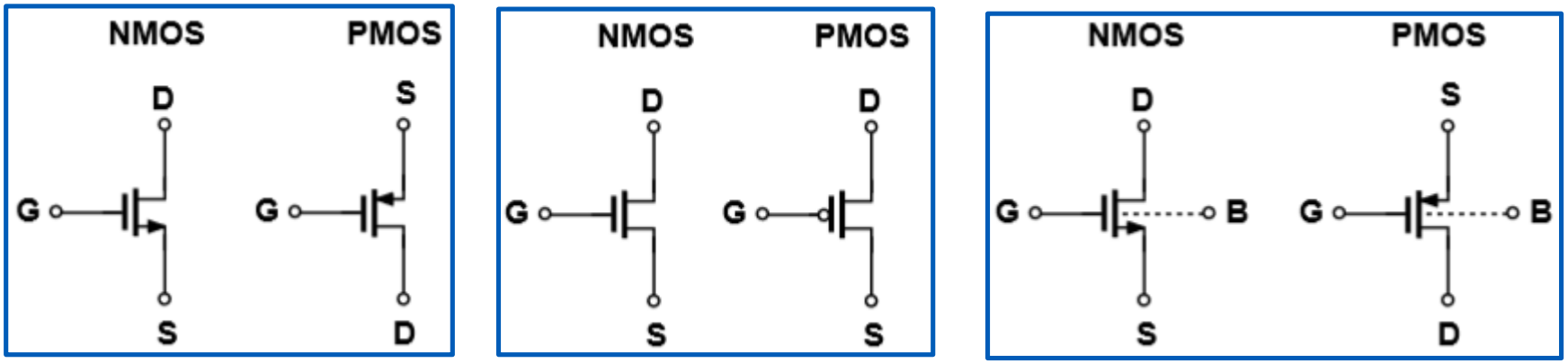
Both NMOS and PMOS are fabricated on the same wafer

- **All NMOS share the same substrate**
- **Each PMOS have an independent n-well**

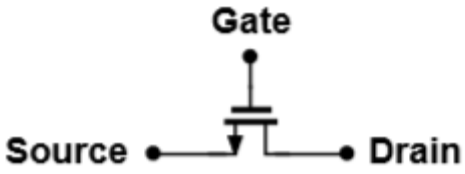
- Dual-Well Trench-Isolated CMOS Process



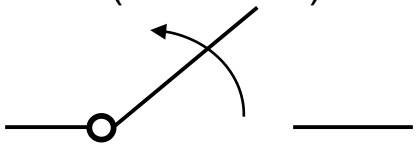
MOSFET Symbol



MOSFET as a Switch

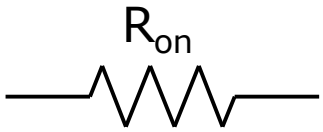


Open (off)
(Gate = '1')



$|V_{GS}| > |V_{DD} - |V_{TH}|$

Closed (on)
(Gate = '0')



$|V_{GS}| < |V_{DD} - |V_{TH}||$

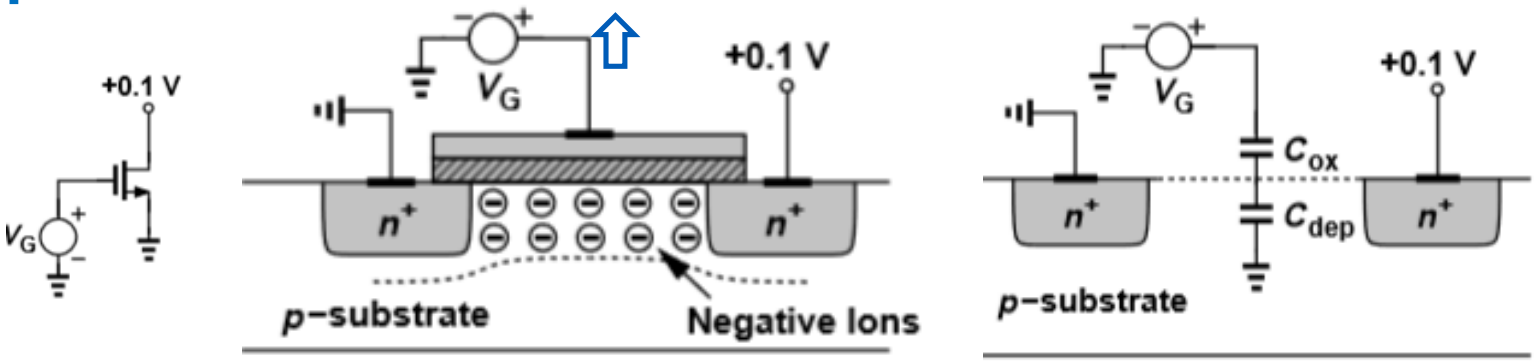
- When gate voltage is high, device is on.
- When gate voltage is low, device is off.

Outline

- Review：Diodes
- MOS I/V Characteristics
  - General Considerations
  - MOS I/V Characteristics: Threshold voltages, I/V characteristics, Transconductance
  - Second-Order Effects
- MOS Device Models
  - MOS SPICE Models
- MOS Short-Channel Effect

Threshold Voltage

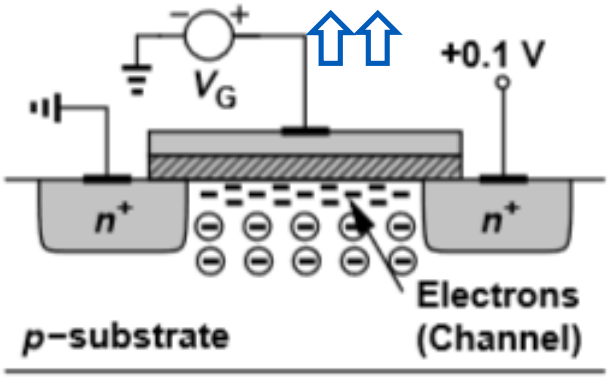
Depletion:



- The holes in p-sub are repelled from the gate area, leaving negative ions to mirror the charge on the gate
- No current flows because no charge carriers are available.
- Increasing V_G -> increasing the potential at the oxide-silicon interface
  increasing the width of the depletion region
- Voltage divider: C_{ox} and C_{dep} in series.

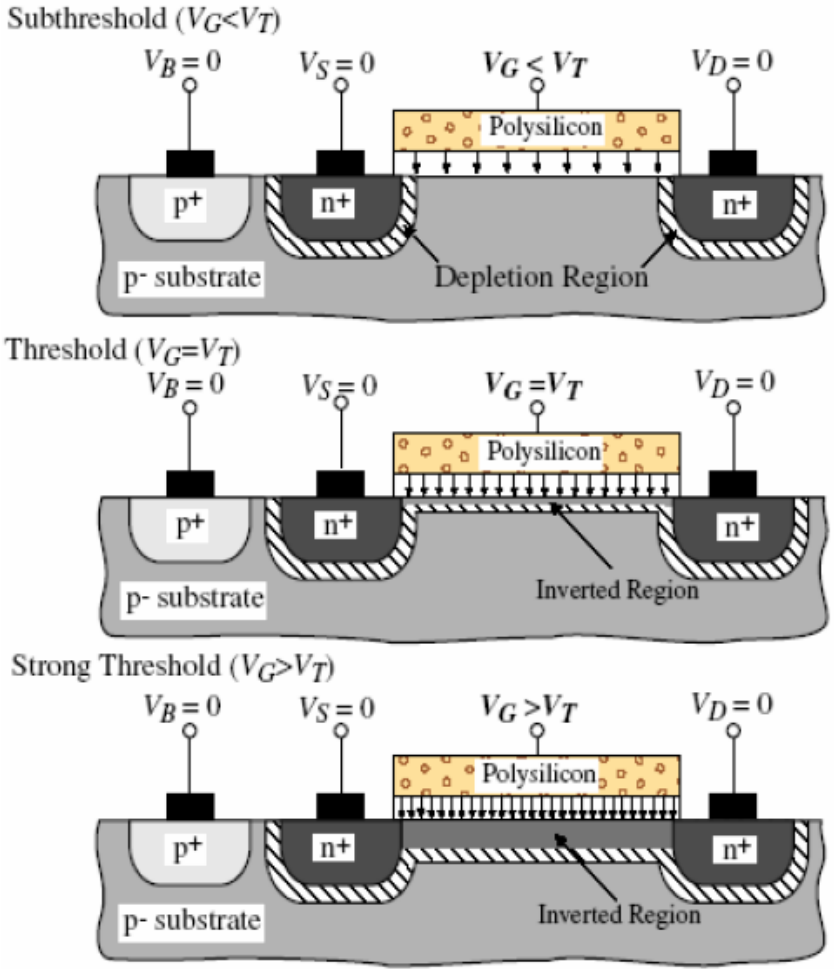
Threshold Voltage: inversion

Inversion:



- **Inversion layer**
- the charge in depletion region remains relatively constant while the channel charge density continue to increase
- When V_{DS}≠0, electrons: source -> drain
- the value of V_G at which the inversion layer occurs is **the threshold voltage (V_{TH})**.

Appendix:



- 以NMOS为例：D和S接地

① VG<0， 多子积累

空穴在硅表面积积累

② 0<VG<VTH 多子耗尽

硅表面耗尽：表面只有固定的负电荷

③ VG>VTH 少子反型

硅表面反型：自由电子吸引到硅表面

- 强反型条件：

栅极下硅表面反型层的载流子浓度 = 衬底掺杂浓度

Threshold Voltage

Strong inversion: the interface is “as much n-type as the substrate is p-type” **(electrons = holes, n=p)**

Ideal threshold voltage:

$$V_{TH} = \Phi_{MS} + 2\Phi_F + \frac{Q_{dep}}{C_{ox}}$$

$$\Phi_F = (kT/q)\ln(N_{sub}/n_i)$$

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{\varepsilon_o \varepsilon_{sio_2}}{t_{ox}}$$ (unit: F/um^2)

$$Q_{dep} = \sqrt{4q\varepsilon_{si}|\Phi_F|N_{sub}}$$

$$\varepsilon_{sio_2} = 3.9$$

$$\varepsilon_{si} = 11.9$$

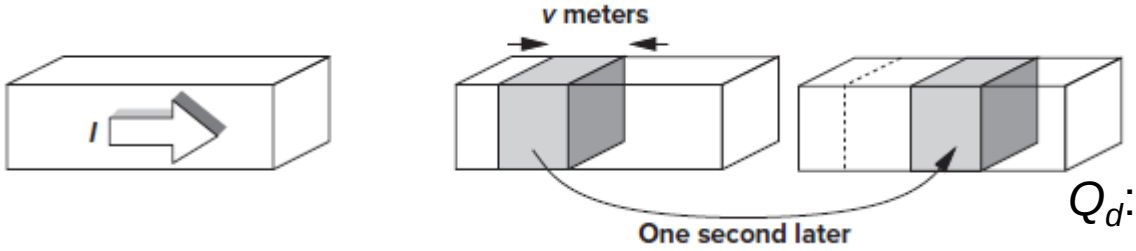
$$\Phi = \Phi_B = 2\Phi_F$$

$$x_d = \sqrt{\frac{4\varepsilon_0 \varepsilon_{si} \Phi_F}{qN_{sub}}}$$

NOTE:

- In practice, threshold voltage is adjusted by implanting dopants into the channel area. Native threshold voltage
- Turn-on phenomena in PMOS is similar to that of NMOS but with all polarities reversed.
  -- The threshold voltage of PMOS is negative.

Derivation of I/V Characteristics



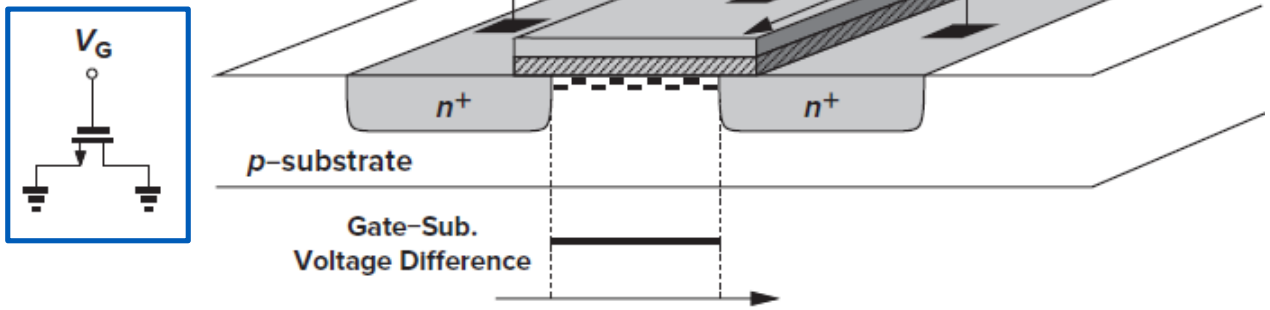
$$I = \frac{Q}{t} = \frac{Q_d l}{t} = Q_d v$$

Q_d: Charge per unit length (C/m)

V: velocity of charge (m/s)

For $V_{GS} \geq V_{TH}$

1) $V_{DS}=0$



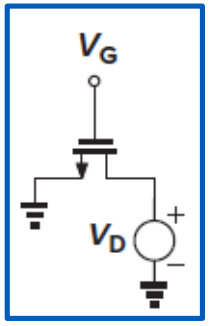
$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{\varepsilon_o \varepsilon_{sio_2}}{t_{ox}}$$

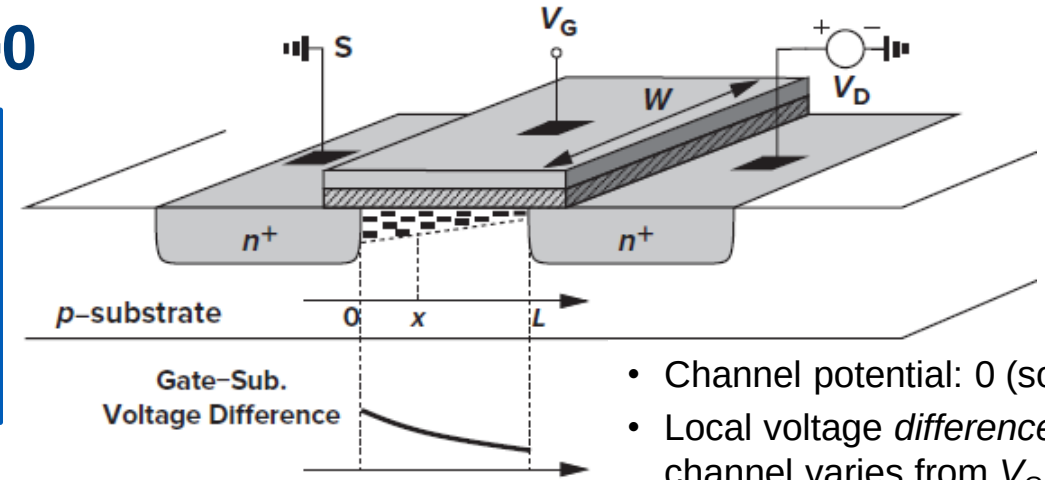
$$Q_d(x) = WC_{OX}(V_{GS} - V_{TH})$$

WC_{ox}: the total capacitance per unit length

Derivation of I/V: Triode region

2) $V_{DS}>0$





- Channel potential: 0 (source) ->V_D (drain)
- Local voltage *difference* between the gate and the channel varies from V_G to $V_G - V_D$.

$$Q_d(x) = WC_{OX}\left[V_{GS} - V(x) - V_{TH}\right]$$

V(x): the channel potential at x

$$\Rightarrow I_D = -WC_{OX}\left[V_{GS} - V(x) - V_{TH}\right]v$$

For semiconductors, *v=μE, E(x)=-dV/dx*

$$I_D = WC_{OX}\left[V_{GS} - V(x) - V_{TH}\right]\mu_n \frac{dV(x)}{dx}$$

$$\int_{x=0}^{L} I_D dx = \int_{V=0}^{V_{DS}} \mu_n WC_{OX}\left[V_{GS} - V(x) - V_{TH}\right]dV(x)$$

$$\Rightarrow \boxed{I_D = \mu_n C_{OX}\frac{W}{L}\left[\left(V_{GS} - V_{TH}\right)V_{DS} - \frac{1}{2}V_{DS}^2\right]}$$

Derivation of I/V: Triode region

$$I_D = \mu_n C_{OX} \frac{W}{L}\left[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

-- Sah Equation

- Process transconductance parameter(工艺跨导参数)

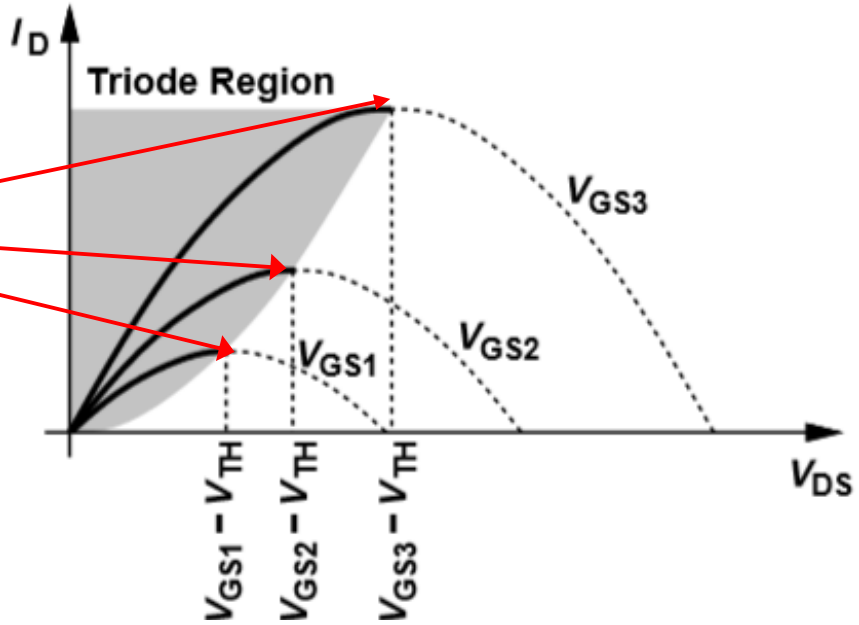
$$k_n' = \mu_n C_{ox} = \mu_n \frac{\varepsilon_{ox}}{t_{ox}}$$

跨导参数 $\beta = \mu_n C_{ox} \frac{W}{L}$

- Aspect ratio: W/L

When $V_{DS} = V_{GS} - V_{TH}$

$$I_{D,\max} = \frac{1}{2}\mu_n C_{OX} \frac{W}{L}(V_{GS} - V_{TH})^2$$



- Overdrive voltage (V_{ON} , V_{eff}, V_{OV}):

$$V_{ON} = V_{GS} - V_{TH}$$

Derivation of I/V : Triode region

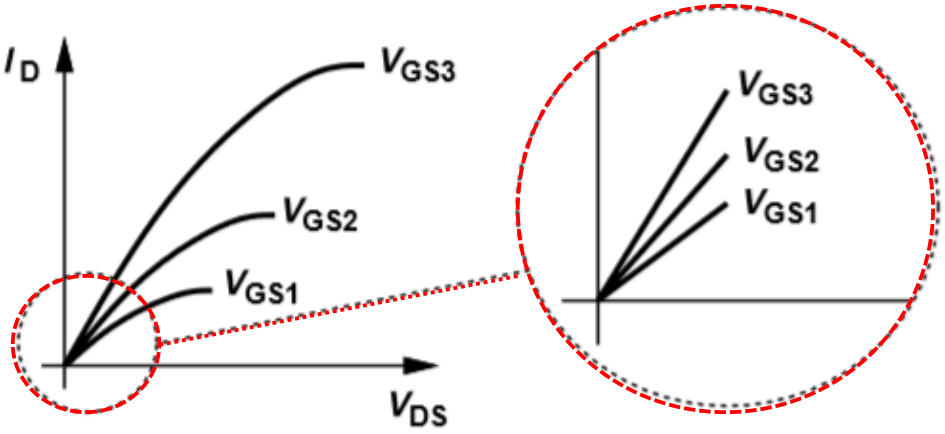
Linear region (Deep triode region)：

For small V_{DS}, there is a linear dependence between V_{DS} and I_D

If $V_{DS} << 2(V_{GS}-V_{TH})$

$$I_D = \mu_n C_{OX} \frac{W}{L}\left[(V_{GS}-V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

$$\Rightarrow \boxed{I_D \approx \mu_n C_{OX} \frac{W}{L}(V_{GS}-V_{TH})V_{DS}}$$

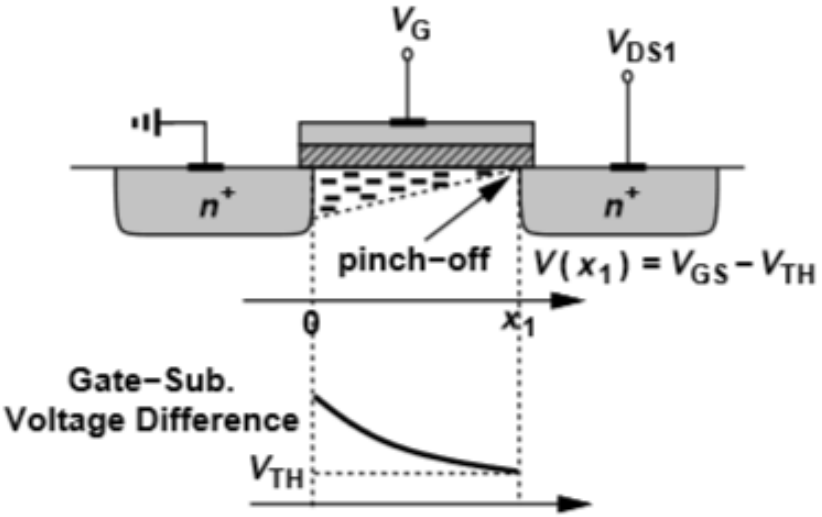


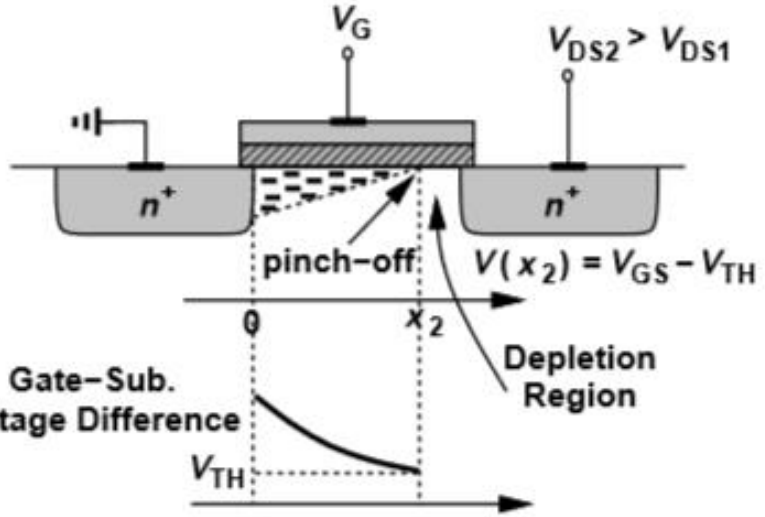
$$R_{on} = \frac{1}{\mu_n C_{OX} \frac{W}{L}(V_{GS}-V_{TH})}$$

- I_D is a linear function of V_{DS}
- Operate as a resistor controlled by (V_{GS}-V_{TH})

Derivation of I/V: Saturation region

3) $V_{DS} > V_{GS} - V_{TH}$





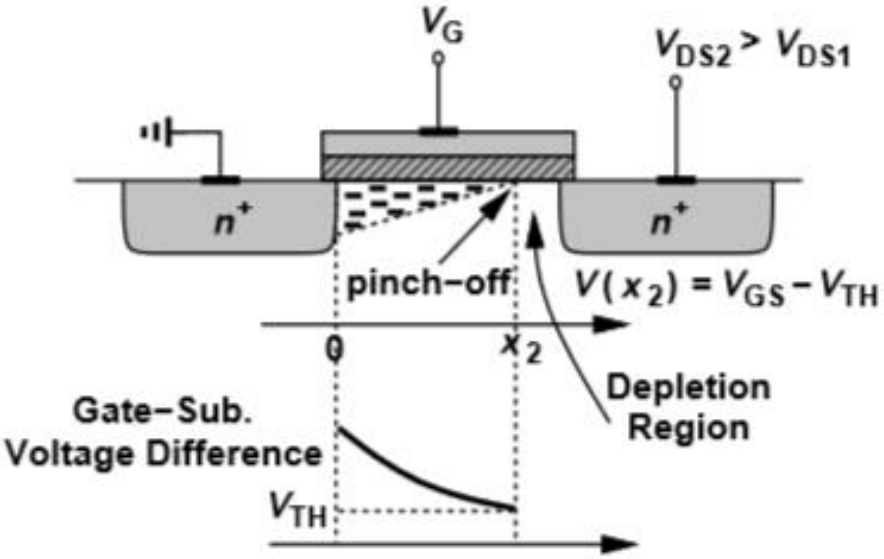
$$\int_{x=0}^{L} I_D dx = \int_{V=0}^{V_{DS}} \mu_n W C_{OX} \left[V_{GS} - V(x) - V_{TH} \right] dV(x)$$

$$I_D = \mu_n C_{OX} \frac{W}{L} \left[(V_{GS} - V_{TH}) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \Rightarrow \boxed{I_{D,\max} = \frac{1}{2} \mu_n C_{OX} \frac{W}{L} (V_{GS} - V_{TH})^2}$$

- $V_{D,sat} = V_{GS} - V_{TH}$: the minimum V_{DS} for operation in saturation
- I_D becomes relatively constant

Appendix : Pinch off（夹断点）

Electron velocity ($v=I/Q_d$) rises tremendously as they approach the pinch-off point (Q_d ->0) and shoot through the depletion region near the drain junction and arrive at the drain terminal.



$$\int_{x=0}^{x=x_2=L'} I_D dx = \int_{V=0}^{V=V_{GS}-V_{TH}} \mu_n W C_{OX} \left[V_{GS} - V(x) - V_{TH} \right] dV(x)$$

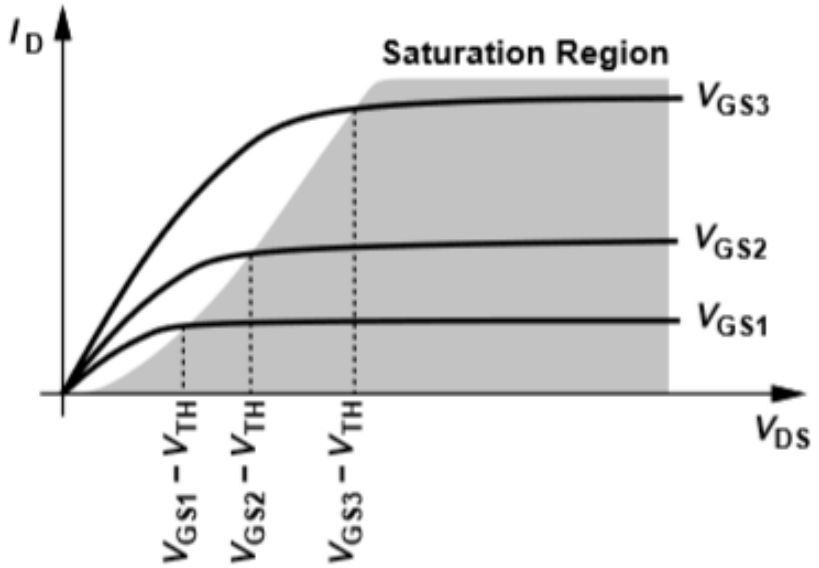
Derivation of I/V: Saturation region

- if $V_{DS} > V_{GS} - V_{TH}$, I_D becomes relatively constant

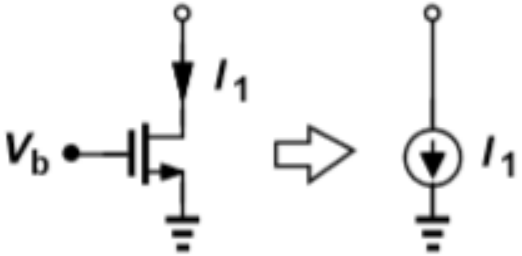
$$I_D = \frac{1}{2}\mu_n C_{OX}\frac{W}{L}(V_{GS} - V_{TH})^2$$

-- Square-law Equation

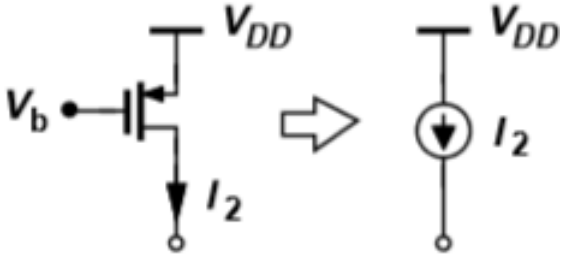
$$V_{GS} = \sqrt{\frac{2I_D}{\mu_n C_{OX}\frac{W}{L'}}} + V_{TH}$$



- Current Source



NMOS

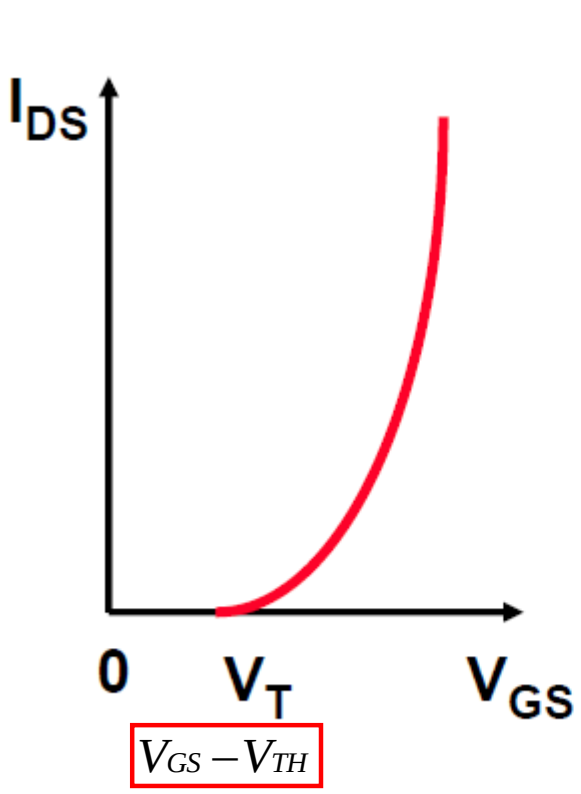


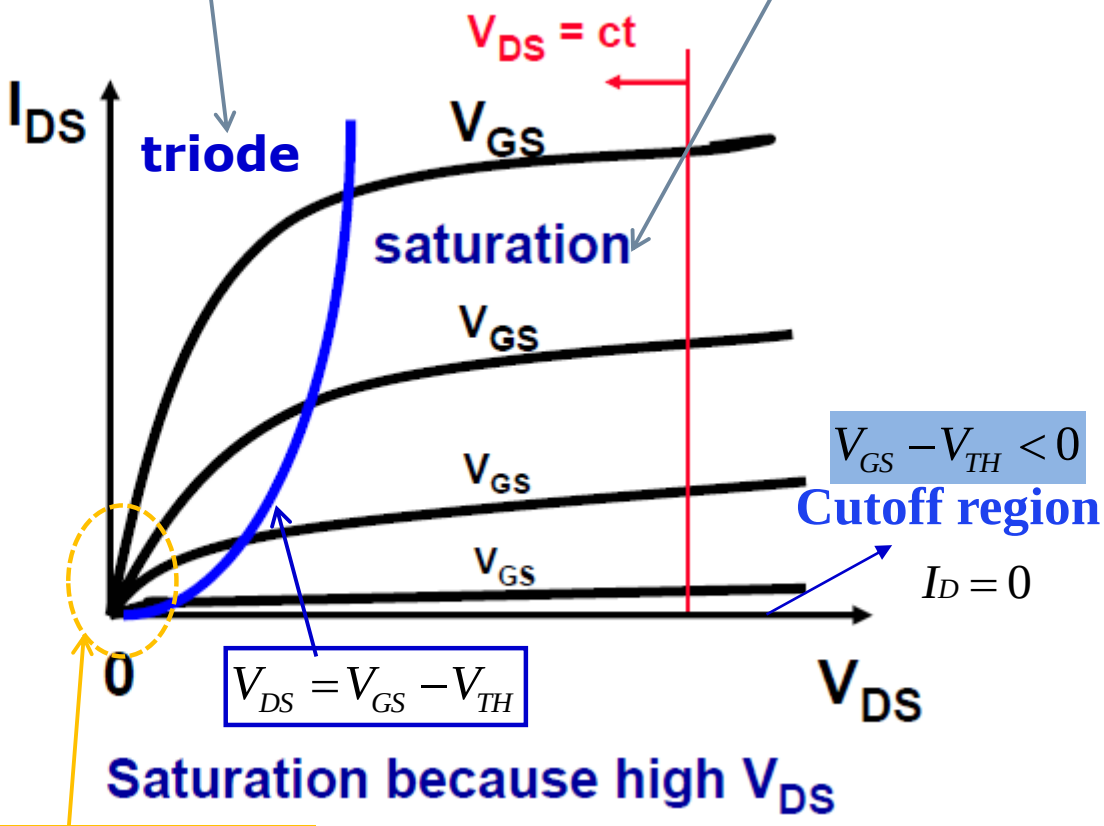
PMOS

I/V Characteristics: I_{DS} vs. V_{GS} and V_{DS}

$$I_D = \mu_n C_{OX} \frac{W}{L}\left[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

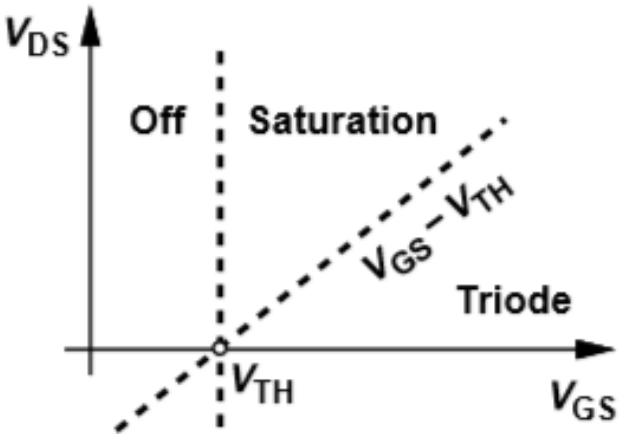
$$I_D = \frac{1}{2}\mu_n C_{OX} \frac{W}{L}(V_{GS} - V_{TH})^2$$



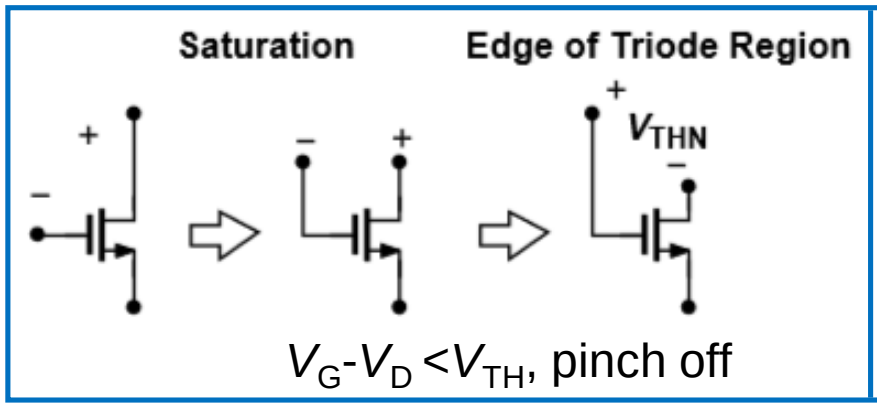


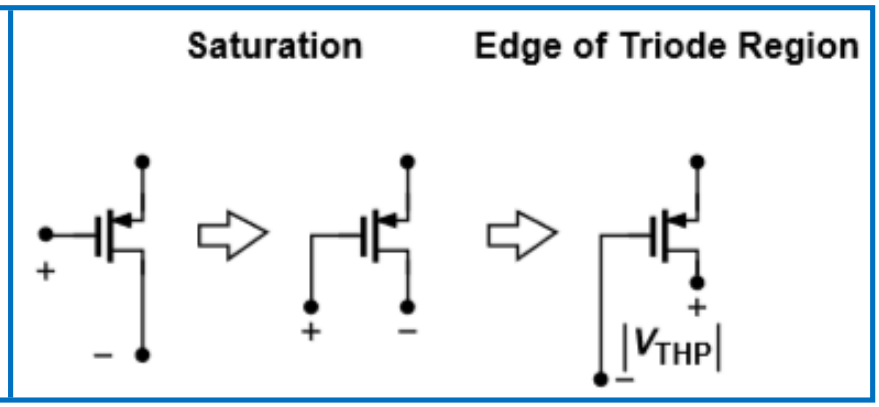
$$I_D \approx \mu_n C_{OX} \frac{W}{L}(V_{GS} - V_{TH})V_{DS}$$

I/V Characteristics: Operation Region



- $V_{GS}<V_{TH}$: off region
- $V_{DS} = V_{GS}-V_{TH} = V_{D,sat}$: saturation and triode region
- For a given V_{DS}, V_{GS} increases: off, saturation, triode





I/V Characteristics: Summary

For NMOS Device

- Triode Region $V_{DS}<V_{GS}-V_{TH}>0$ $$I_D = \mu_n C_{OX} \frac{W}{L}\left[(V_{GS}-V_{TH})V_{DS}-\frac{1}{2}V_{DS}^2\right]$$
- Saturation Region: $V_{DS}>V_{GS}-V_{TH}>0$ $$I_D = \frac{1}{2}\mu_n C_{OX}\frac{W}{L}(V_{GS}-V_{TH})^2$$

For PMOS Device

- Triode Region: $|V_{DS}|<|V_{GS}| - |V_{TH}|$ $$I_D = -\mu_p C_{ox} \frac{W}{L}\left[(V_{GS}-V_{TH})V_{DS}-\frac{1}{2}V_{DS}^2\right]$$
- Saturation Region: $|V_{DS}| > |V_{GS}| - |V_{TH}|$ $$I_D = -\frac{1}{2}\mu_p C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2$$
- NOTE:

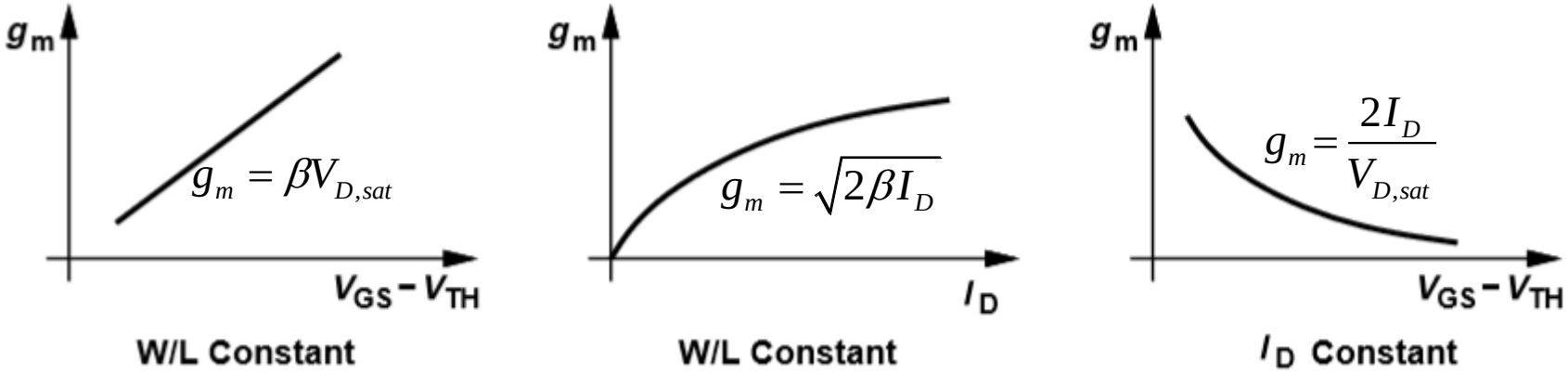
1) "-": drain current flows from drain to source, whereas holes in a PMOS flow in the reverse direction.
2) V_{GS}, V_{DS}, V_{TH}, and $V_{GS}-V_{TH}$ are negative for PMOS that is turned on.
3) $\mu_p \approx (1/3\sim1/2)\,\mu_n$ => PMOS devices: lower "current drive" capability.

Transconductance g_m

Transconductance (usually defined in the saturation region):

- how well a device converts a voltage to a current
- the sensitivity if a high value implies a small change in V_{GS} will result in a large change in I_D

$$g_m = \frac{\partial I_D}{\partial V_{GS}}\bigg|_{V_{DS},const} = \mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH}) = \sqrt{2\mu_n C_{ox}\frac{W}{L}I_D} = \frac{2I_D}{V_{GS} - V_{TH}}$$



- g_m in the saturation region is the inverse of R_{on} in the deep triode region.

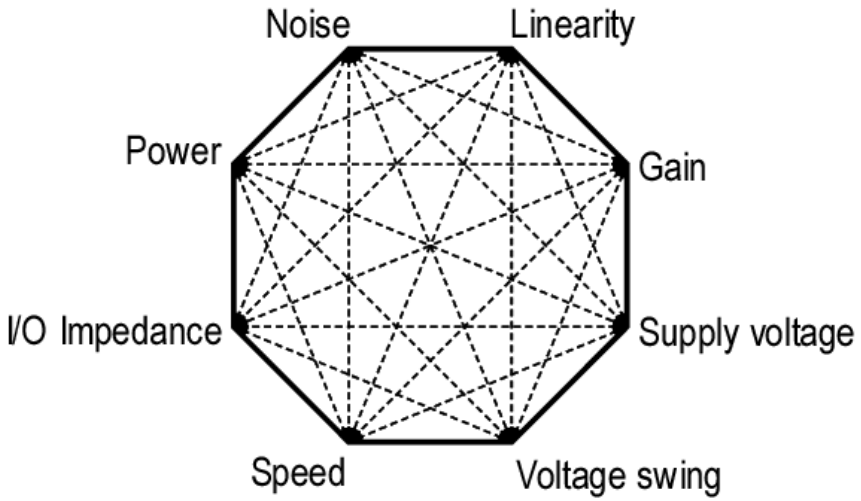
$$R_{on} = \frac{1}{\mu_n C_{OX}\frac{W}{L}(V_{GS} - V_{TH})}$$

Maximize g_m at the same I_D

- A large trans-conductance g_m is a good and desirable!
- **Maximizing g_m** is one of the most important task for analog designer

(1) g_m determines the thermal noise power: $8kT/3g_m$

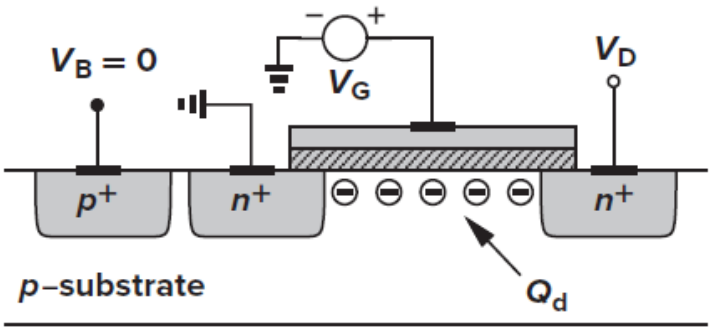
(2) g_m determines the unit gain bandwidth: g_m/C_O

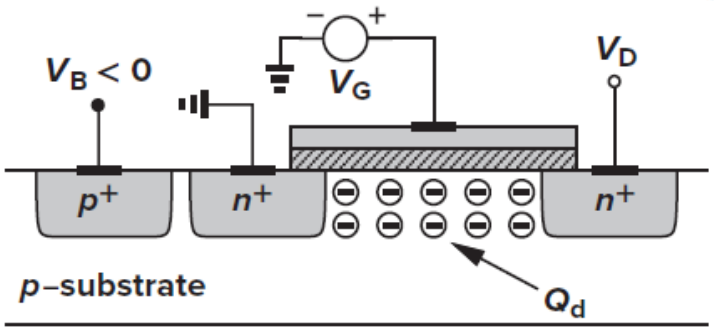


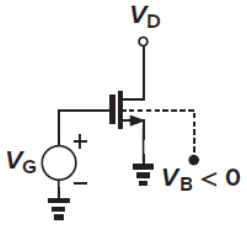
Outline

- Review：Diodes
- MOS I/V Characteristics
  - General Considerations
  - MOS I/V Characteristics
  - Second-Order Effects: Body effect, Channel length modulation; Subthreshold conduction
- MOS Device Models
- MOS Short-Channel Effect
- MOS SPICE Models

Body Effect（Back-Bias effect）







- V_B =0 $V_{TH} = \Phi_{MS} + 2\Phi_F + \frac{Q_{dep}}{C_{ox}}$ Page 22
- $V_B \downarrow$ -> $Q_d \uparrow$ -> $V_{TH} \uparrow$ $V_{TH} = V_{TH0} + \gamma\left(\sqrt{|2\Phi_F + V_{SB}|} - \sqrt{|2\Phi_F|}\right)$

- V_{TH0} is the threshold voltage at V_{SB} = 0 and is mostly a function of the manufacturing process
- V_{SB} is the source-bulk voltage
- Φ_F is the Fermi potential
- γ is the body-effect efficiency (Body Factor)

$$\gamma = \sqrt{2q\varepsilon_{si}N_{sub}}/C_{ox} \sim 0.3\text{-}0.4\text{V}^{1/2} \qquad N\uparrow \Rightarrow \gamma\uparrow$$

Body Effect: Example

$$V_{TH} = V_{TH0} + \gamma\left(\sqrt{|2\Phi_F + V_{SB}|} - \sqrt{|2\Phi_F|}\right)$$

$$V_{dd} = 2.5V \quad V_{bb} = -2.5V \quad V_{out} = 1.8V$$

Thus

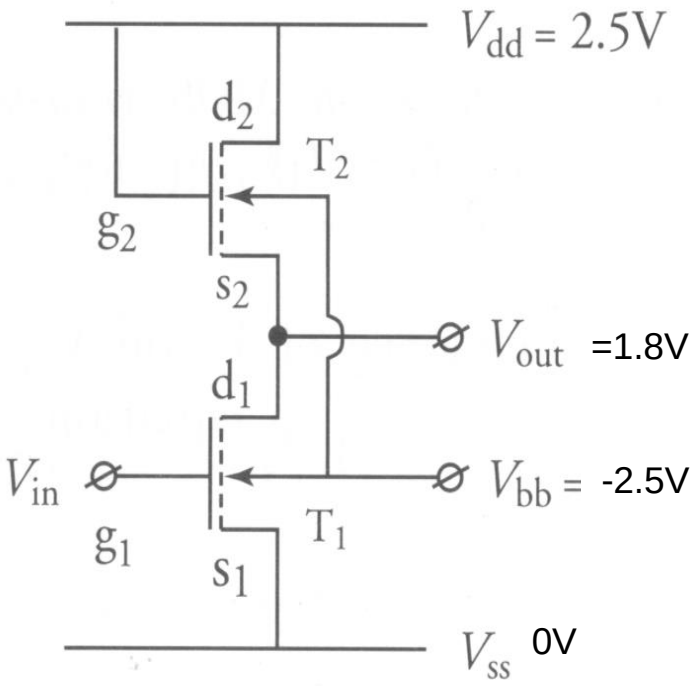
$$V_{SB1} = V_{ss} - V_{bb} = 2.5V$$

$$V_{SB2} = V_{out} - V_{bb} = 4.3V$$

$$V_{TH1} = V_{TH0} + \gamma\left(\sqrt{|2\Phi_F + V_{SB1}|} - \sqrt{|2\Phi_F|}\right)$$

$$V_{TH2} = V_{TH0} + \gamma\left(\sqrt{|2\Phi_F + V_{SB2}|} - \sqrt{|2\Phi_F|}\right)$$

$$Obviously, V_{TH2} > V_{TH1}$$

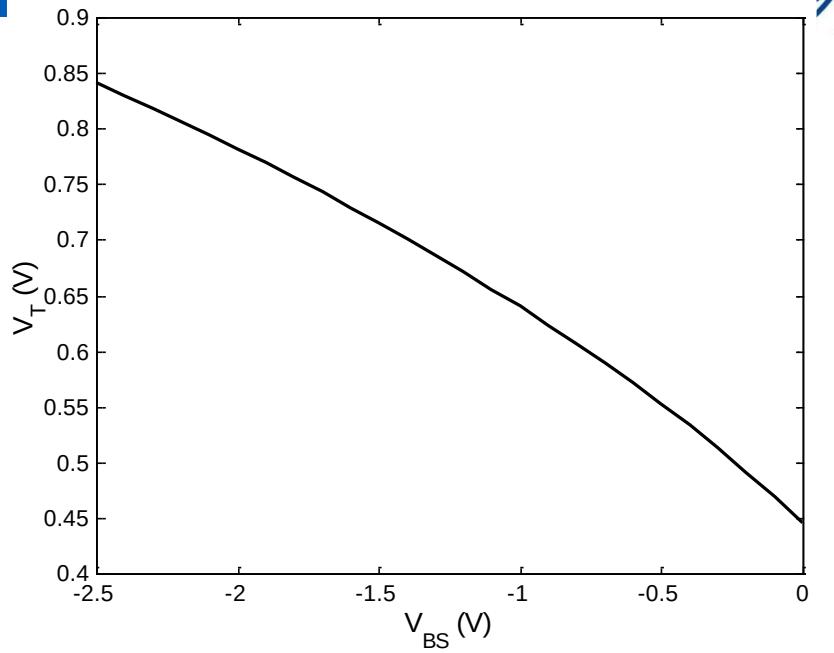


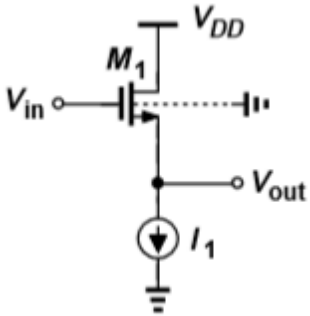
N阱工艺中NMOS的衬底接最低电位，但源极可能不接最低电位，造成体效应。

一般体效应使设计复杂化；
利用体效应的模拟集成电路。。。

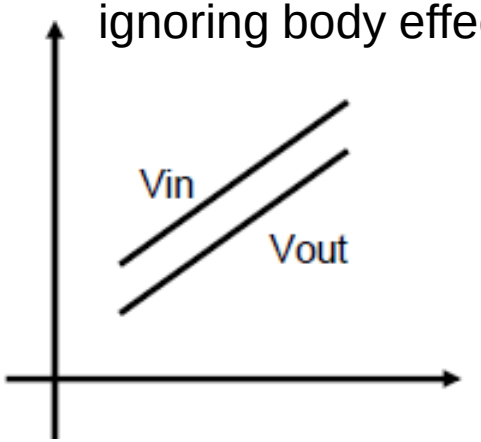
Body Effect: V_S vs. V_B (1)

- V_{SB} is the substrate bias voltage (normally positive for n-channel devices with the body tied to ground)
- A bias causes V_{TH} to increase from 0.45V to 0.85V

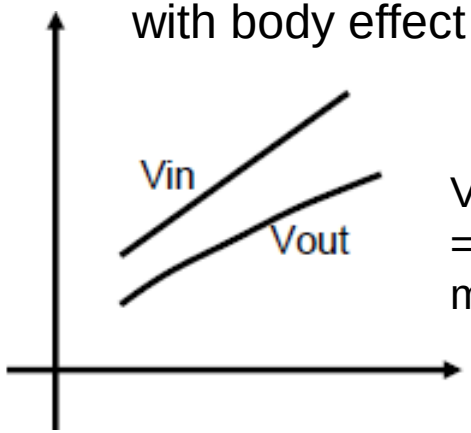




ignoring body effect

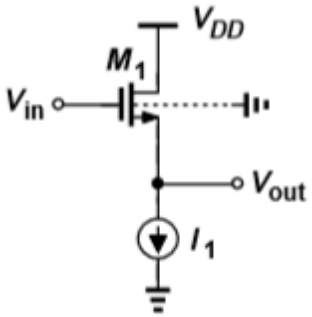


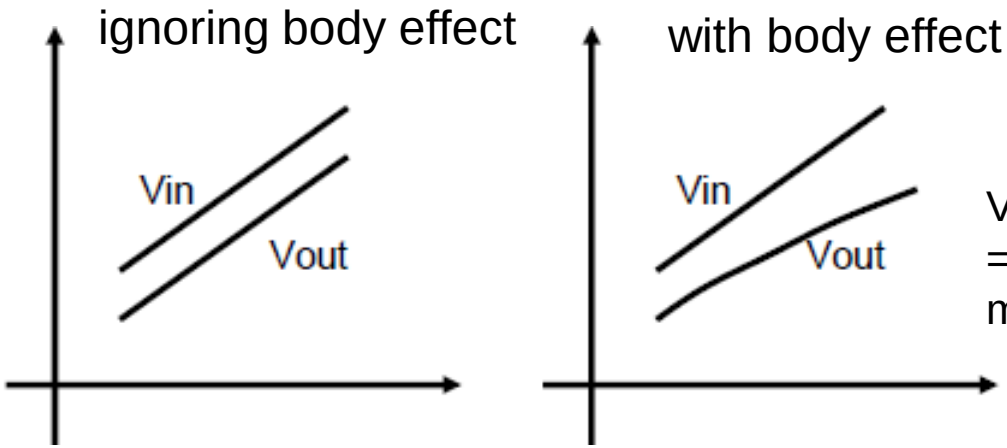
with body effect



$V_{in}\uparrow$ => $V_{out}\uparrow$ => $V_{SB}\uparrow$ => $V_{TH}\uparrow$ => $V_{in} - V_{out}\uparrow$ to maintain a constant I_D.

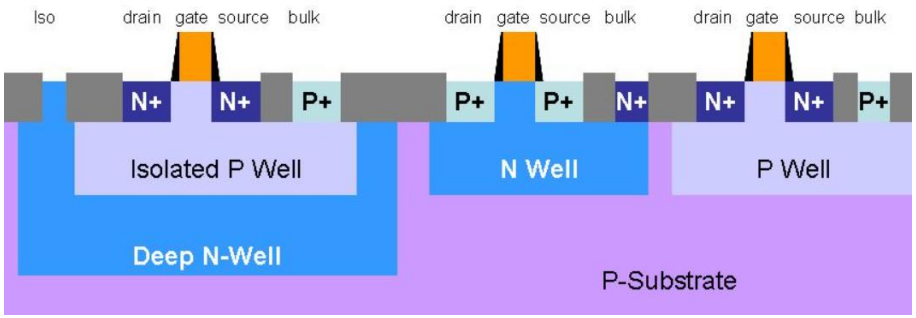
Body Effect: V_S vs. V_B (2)





$V_{in}\uparrow$ => $V_{out}\uparrow$ => $V_{SB}\uparrow$ => $V_{TH}\uparrow$ => $V_{in} - V_{out}\uparrow$ to maintain a constant I_D.

- *Short the B and S can eliminate the body effect*
- *Short the B and S is only allowed in dual well* (deep nwell) *technology and it can lead to* ***large area***



Body Effect: V_S vs. V_B (3)

- *Make use of body effect to reduce the Vth for **low voltage** operation*

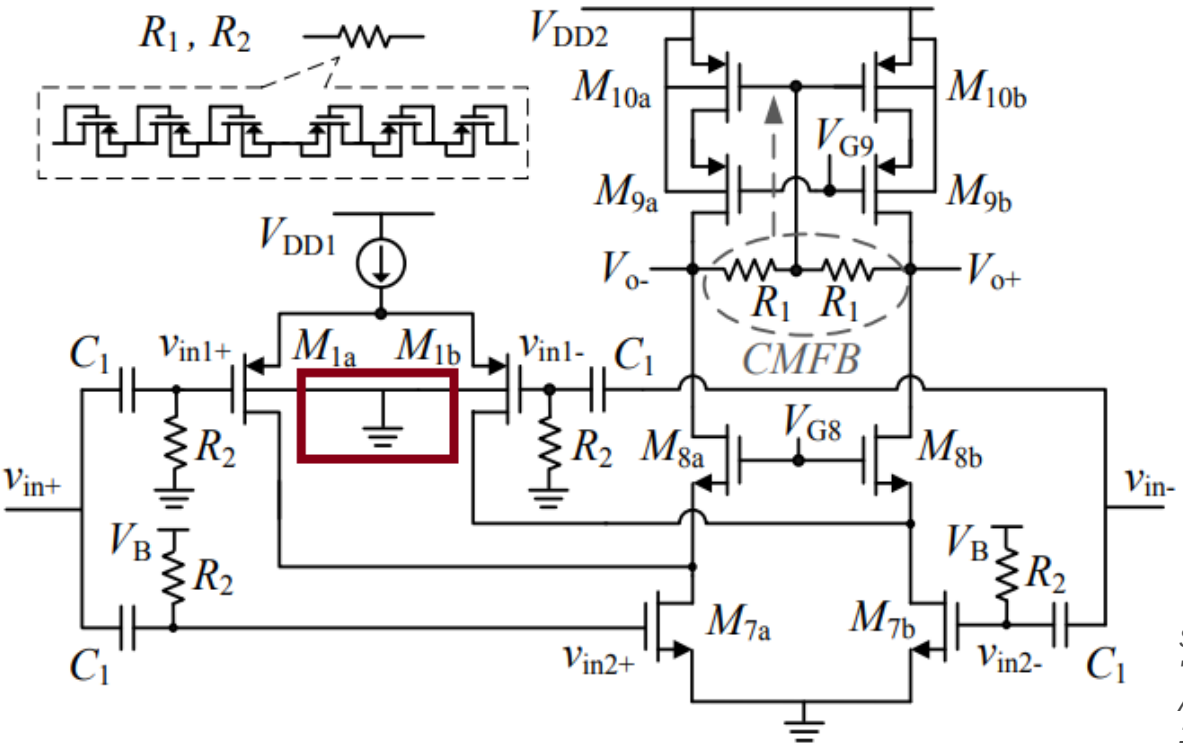


Figure 38 The proposed current reuse low voltage folded cascode amplifier

Shuang Song, Michaël Rooijakkers, etc, "A Low-Voltage Chopper-Stabilized Amplifier for Fetal ECG Monitoring With a 1.41 Power Efficiency Factor," in IEEE Transactions on Biomedical Circuits and Systems, vol. 9, no. 2, 2015.

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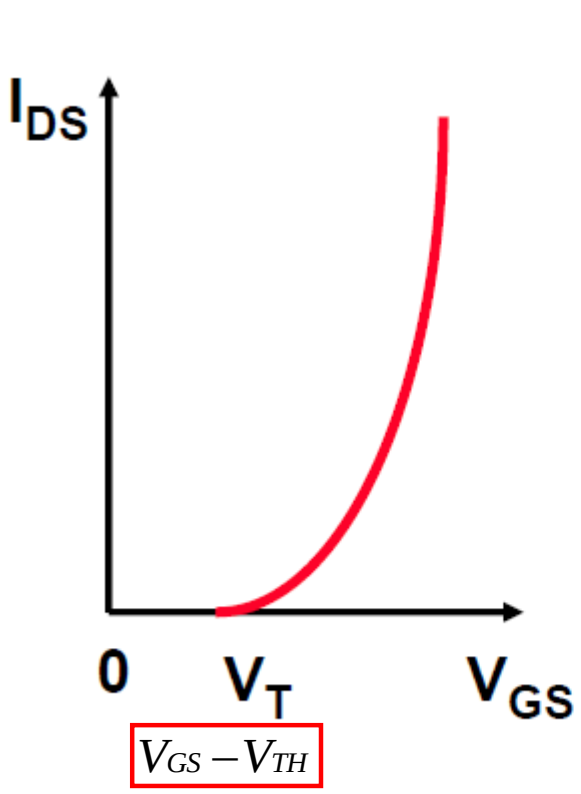
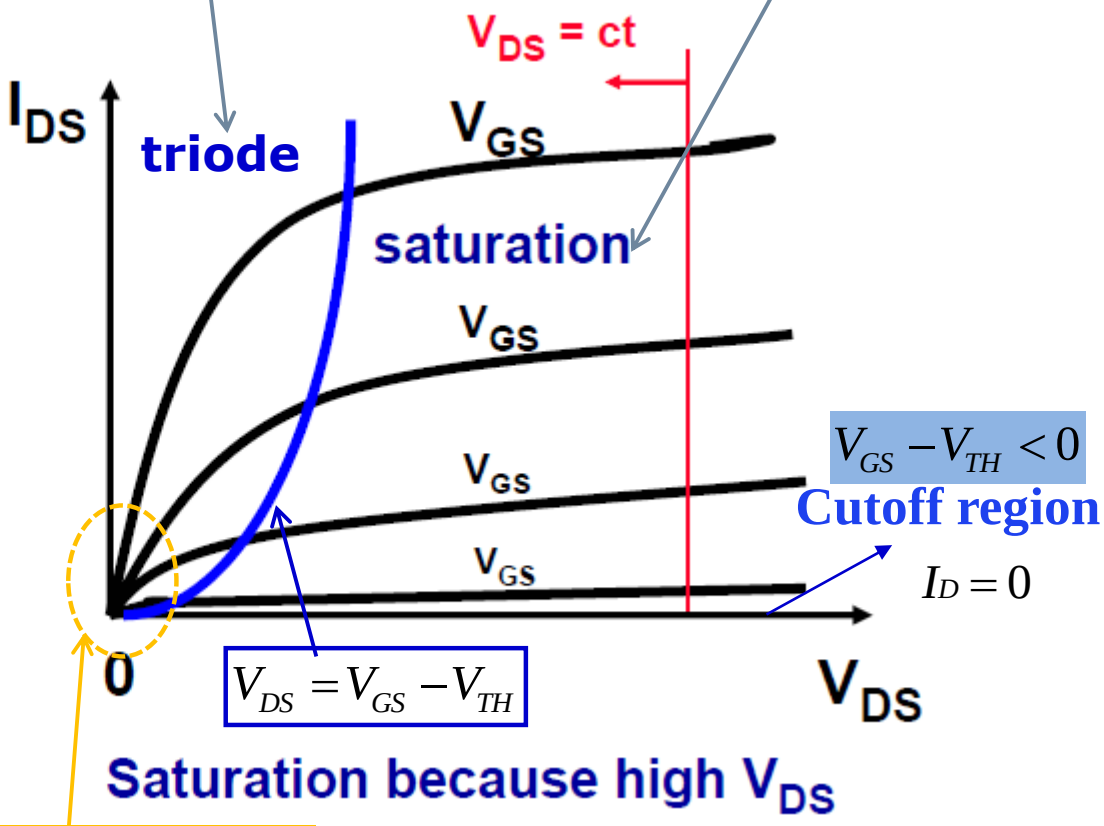
$$I_D = \mu_n C_{OX} \frac{W}{L}\left[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

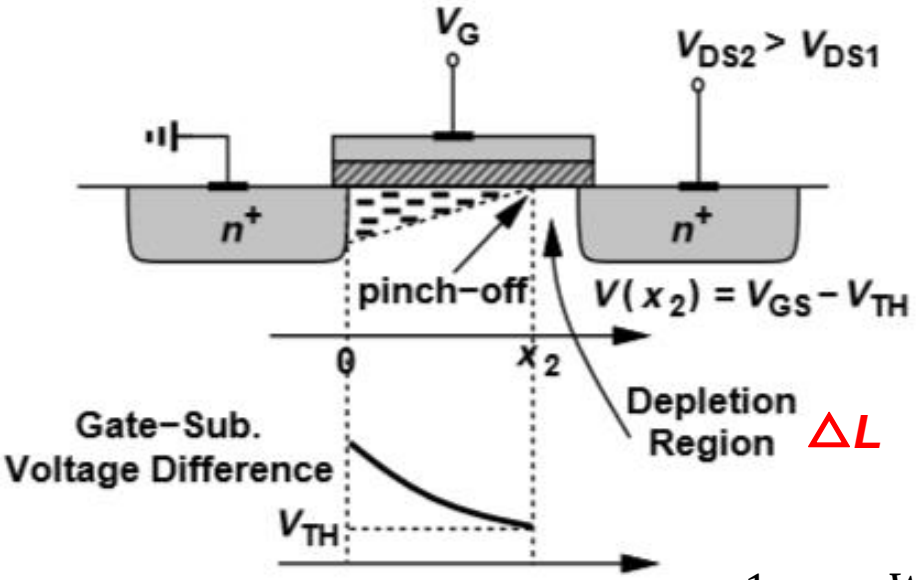
$$I_D = \frac{1}{2}\mu_n C_{OX} \frac{W}{L}(V_{GS} - V_{TH})^2$$





$$I_D \approx \mu_n C_{OX} \frac{W}{L}(V_{GS} - V_{TH})V_{DS}$$

Channel-Length Modulation



当$V_{DS} > V_{GS} - V_{TH}$时，pinch-off从Drain向Source移动，有效沟道长度下降，电流增加

the actual length: $L' = L - \Delta L$

$$1/L' \approx (1 + \Delta L/L)/L$$

Assuming $\Delta L/L = \lambda V_{DS}$ $\quad I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L'}(V_{GS} - V_{TH})^2$

$$\Rightarrow \quad I_D \approx \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS})$$

λ: the channel-length modulation coefficient

$$\Rightarrow \quad g_m = \mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})(1 + \lambda V_{DS}) = \sqrt{2\mu_n C_{ox}(W/L) I_D (1 + \lambda V_{DS})}$$

Channel-Length Modulation

$$I_D \approx \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2(1+\lambda V_{DS})$$

- I_D is not a constant current, depending on V_{DS}

$$\lambda \propto \frac{1}{L}\frac{\sqrt{V_{DS}-V_{D,sat}+\Phi}}{V_{DS}}$$

$$L \uparrow \Rightarrow \lambda \downarrow$$

- λ changes with L => V_E

$$g_{ds}=\frac{\partial i_D}{\partial v_{DS}}\bigg|_{V_{GS},const}=g_0=\frac{I_D\lambda}{1+\lambda V_{DS}}\approx I_D\lambda$$

$$r_O=\frac{1}{I_{DS}\lambda}$$

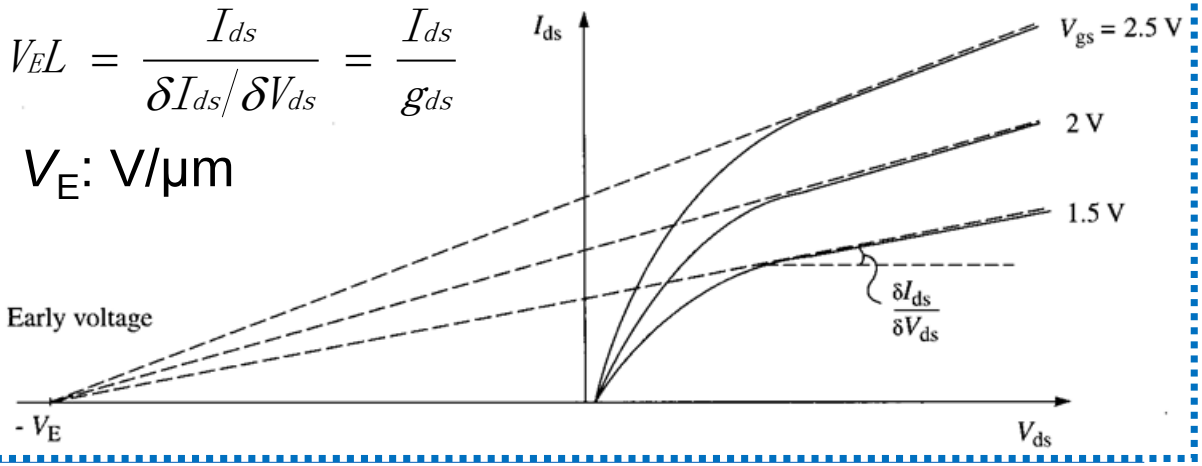
Early Voltage

工艺参数

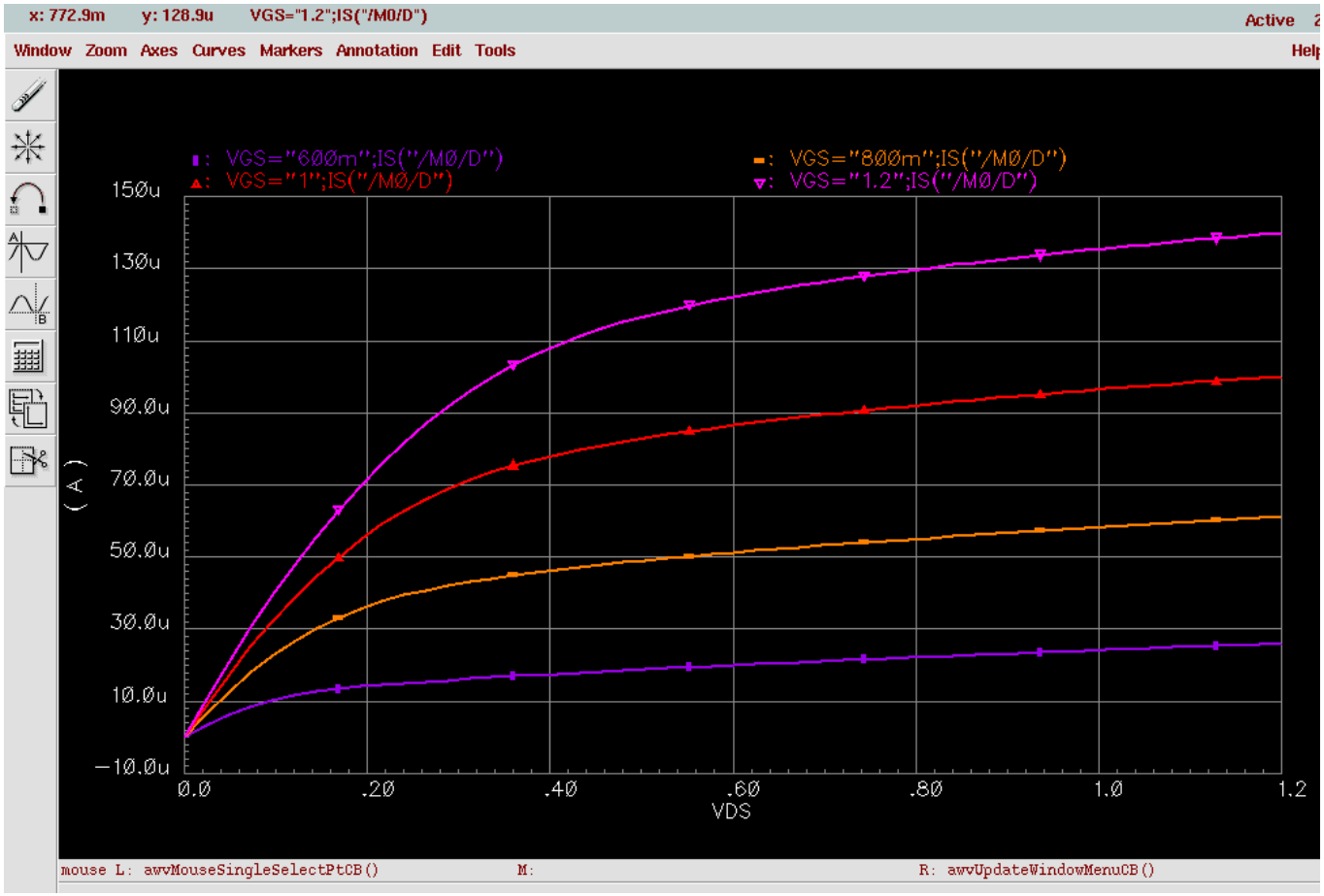
$$\lambda=\frac{1}{V_E L}\qquad r_O=\frac{V_E L}{I_{DS}}$$

$$V_E L=\frac{I_{ds}}{\delta I_{ds}/\delta V_{ds}}=\frac{I_{ds}}{g_{ds}}$$

V_E: V/μm



Channel-Length Modulation



90 nm Devices, W/L = 2, V_{DD} = 1.2V

Channel-Length Modulation: Example

Example 求漏源电流

① 若参数：$\mu_n C_{ox} = 92\mu A/V^2, W/L = 20\mu/2\mu, V_{TH} = 0.8V$

$$V_{GS} = 1.2V, V_{DS} = V_{eff} \Rightarrow V_{DS} = 0.4V$$

$$I_D = \frac{1}{2} \times 92 \times 10^{-6} \times \left(\frac{20}{2}\right) \times (1.2 - 0.8)^2 = 73.6\mu A$$

② 若：$V_{GS} = 1.8V, V_{DS} = V_{eff}$

$$I_D = \frac{1}{2} \times 92 \times 10^{-6} \times \left(\frac{20}{2}\right) \times (1.8 - 0.8)^2 = 460\mu A$$

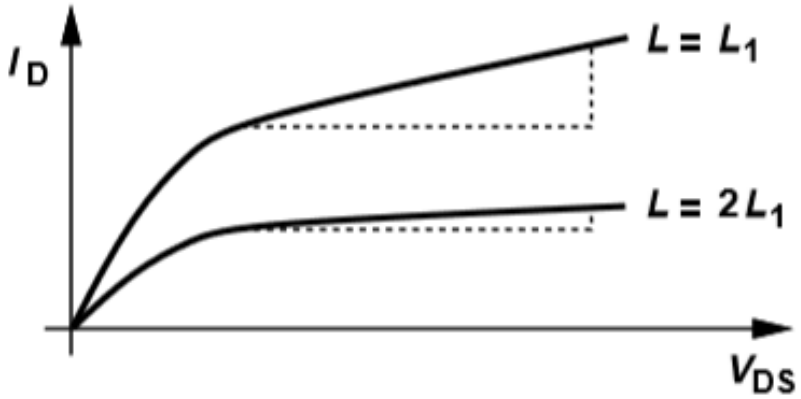
③ 若在条件①　$\lambda = 95 \times 10^{-3} V^{-1}, V_{DS} - V_{eff} = 0.5V \Rightarrow V_{DS} = 0.9V$

$$I_D = 73.6\mu A \times \left(1 + 0.9 \times 95 \times 10^{-3}\right) = 79.9\mu A$$

Channel-Length Modulation: Example

Example

$L=L_1$ vs. $L=2L_1$ ⇨ $I_D \sim V_{DS}$



$$I_D \approx \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2(1+\lambda V_{DS})$$

$$\lambda \propto 1/L, \qquad \frac{\partial I_D}{\partial V_{DS}} \propto \frac{1}{L^2}$$

and keeping all other parameters constant,

⇨ if the length L is doubled, the slope of I_D vs. V_{DS} is divided by *4*. why?

Channel-Length Modulation: Ron & Ro

- *Ron is the on resistance of triode region*

  the small signal resistance and large signal resistance are identical

- *Ro is the small signal resistance of saturation region*

  the small signal resistance is much larger than the large signal resistance in this case

- *If there is no channel-length modulation, the analog design becomes much simpler!*

Subthreshold Conduction

- MOSFETs do not turn off abruptly when $V_{GS} < V_{TH}$
- **"Weak" inversion layer**: finite current flows from drain to source with an exponential dependence on V_{GS}.

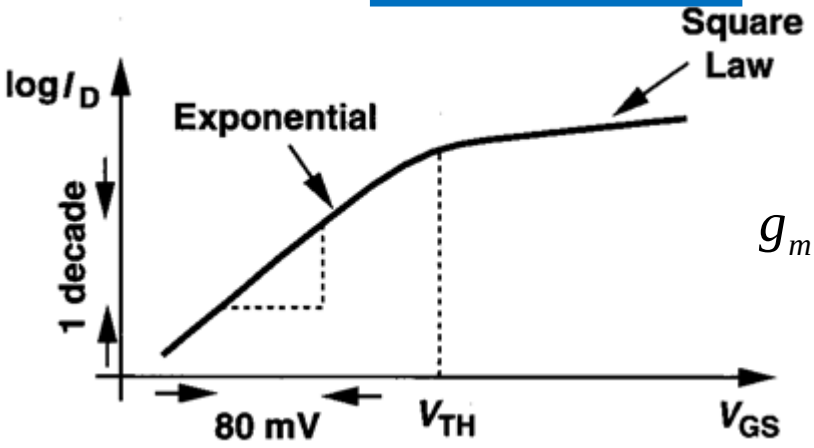
漏电对静态功耗、动态电路不利

Weak Inversion Region (Subthreshold Region)

$V_{GS} < V_{TH}$

$$I_D = I_0 \exp \frac{V_{GS}}{\varsigma V_T}$$

where $I_0 \propto$ W/L ,
ζ>1 is a nonideality factor
$V_T = kT/q$.



$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \frac{I_{DS}}{\xi\, kT/q}$$

Bipolar:

$$I_{CE} = I_S \exp \frac{V_{BE}}{kT/q}$$

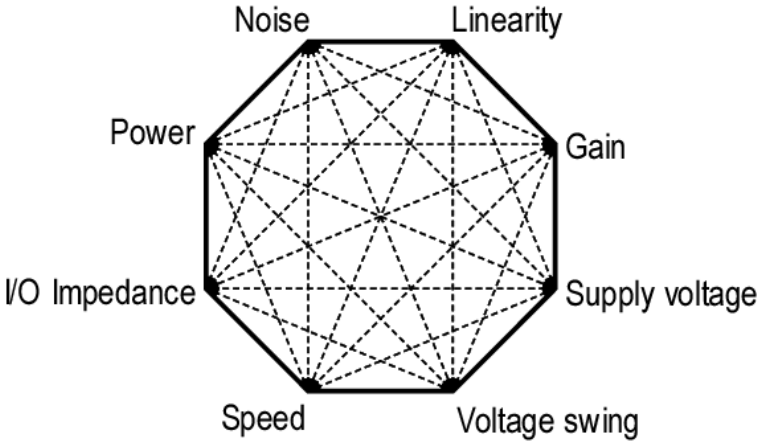
$$g_m = \frac{\partial I_{CE}}{\partial V_{BE}} = \frac{I_{CE}}{kT/q}$$

$V_{GS} - V_{TH} = ?$: weak inversion -> strong inversion transition point : $V_{GS} - V_{TH} = 2\zeta V_T \approx 80$mV

Subthreshold operation (1)

- MOSFETs do not turn off abruptly when $V_{GS} < V_{TH}$
- **"Weak" inversion layer**: finite current flows from drain to source with an exponential dependence on V_{GS}.

- **Making use of** subthreshold operation



(1) Good for Achieving a large Gm

g_m/I_D can be as large as 25 ~ 30

(2) Good for opamp bandwidth (till ~ 100MHz)

g_m/C_O can be maximized

Subthreshold operation (2)

- MOSFETs do not turn off abruptly when $V_{GS} < V_{TH}$
- **"Weak" inversion layer**: finite current flows from drain to source with an exponential dependence on V_{GS}.

- **Avoiding the use of** subthreshold operation

(1) Poor matching & sensitive to process variation

Because (V_{GS} - V_{th}) is small

V_{th} variation can lead to a large overall variation

Current mirrors usually use **large devices** and small W/L ratio

(2) Usually not good for speed in RF circuit

because of inherent bandwidth limitation of the transistor itself

Summary

- Diode and its application
- I/V curve and operation region of MOSFET
- Body Effect
- Channel Length Modulation
- Weak inversion

集成电路原理与设计

2. 器件模型一

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