浙江大学 20 13–20 14 学年秋冬学期

《数字系统设计 II》课程期末考试试卷

课程号：**111C0130**，开课学院：_信息与电子工程学系_

考试试卷：√A 卷、B 卷（请在选定项上打√）

考试形式：√闭、开卷（请在选定项上打√）

允许带 1 张 A4 大小的手写资料和计算器入场

考试日期：_2014_ 年 _1_ 月 __18__ 日，考试时间：_120_ 分钟

诚信考试，沉着应考，杜绝违纪。

考生姓名：_____学号：_____ 所属院系（专业）：_____

题序	一	二	三	四	五	六	总分
得分							
评卷人							

1. TRUE (T) OR FLASE (F) (15 points):

[ ] (1) Both multithreading and multicore rely on parallelism to get more efficiency from a chip.

[ ] (2) As for dependability, if a system is up, then all its components are accomplishing their expected service.

[ ] (3) Hardware error exception should be recognized first in every processor.

[ ] (4) Caches take advantage of temporal locality.

[ ] (5) The shorter the memory latency, the smaller the cache block.

[ ] (6) First-level caches are more concerned about hit time, and second-level caches are more concerned about miss rate.

[ ] (7) Fully associative caches have no conflict misses.

[ ] (8) Reliability is a quantitative measure of continuous service accomplishment by a system.

[ ] (9) Unlike processor benchmarks, I/O benchmarks concentrate on throughput rather than latency.

[ ] (10) To benefit from a multiprocessor, an application must be concurrent.

2. PROCESSOR (12 points):

Refer to figure 1, assume the latencies for logic blocks in the datapath are as follows:

I-Mem	Add	Mux	ALU	Regs	D-Mem	Sign-extend	Shift-left-2
500ps	150ps	100ps	180ps	220ps	1000ps	90ps	20ps

(1) What is the clock cycle time if the only type of instructions we need to support are ALU instructions (add, and, etc.)?

(2) What is the clock cycle time if we only had to support lw instructions?

(3) What is the clock cycle time if we must support add, beq, lw, and sw instructions?

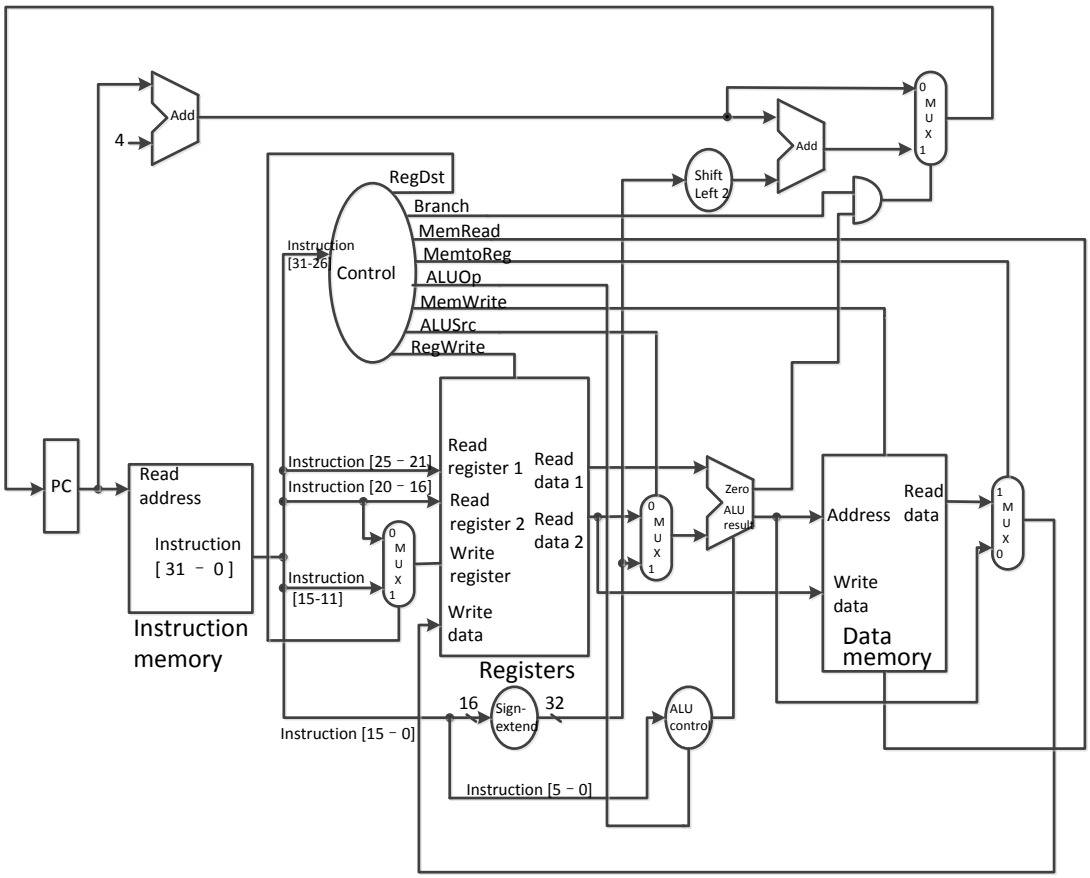

Figure 1 The datapath of a processor

3. PIPELINE (18 points):

Consider an improvement to the fully bypassed 5-stage MIPS processor pipelines with the goal of eliminating all hazards (See Figure 2). The Dual ALU Pipeline has two ALUs: ALU1 is in the 3rd pipeline stage (EX1) and ALU2 is in the 4th pipeline stage (EX2/MEM). A memory instruction always uses ALU1 to compute its address. An ALU instruction uses either ALU1 or ALU2, but never both. *If an ALU instruction's operands are available (either from the register file or the bypass network) by the end of the ID stage, the instruction uses ALU1; otherwise, the instruction uses ALU2.*

In this problem, assume that the control logic is optimized to stall only when necessary, and that the pipeline is fully bypassed. You may ignore branch and jump instructions in this problem.

IF	ID	EX1	EX2/MEM	WB
Instruction fetch	Instruction decode and register read	ALU1 execution and address calculation	ALU2 execution and memory access	Write back to register file

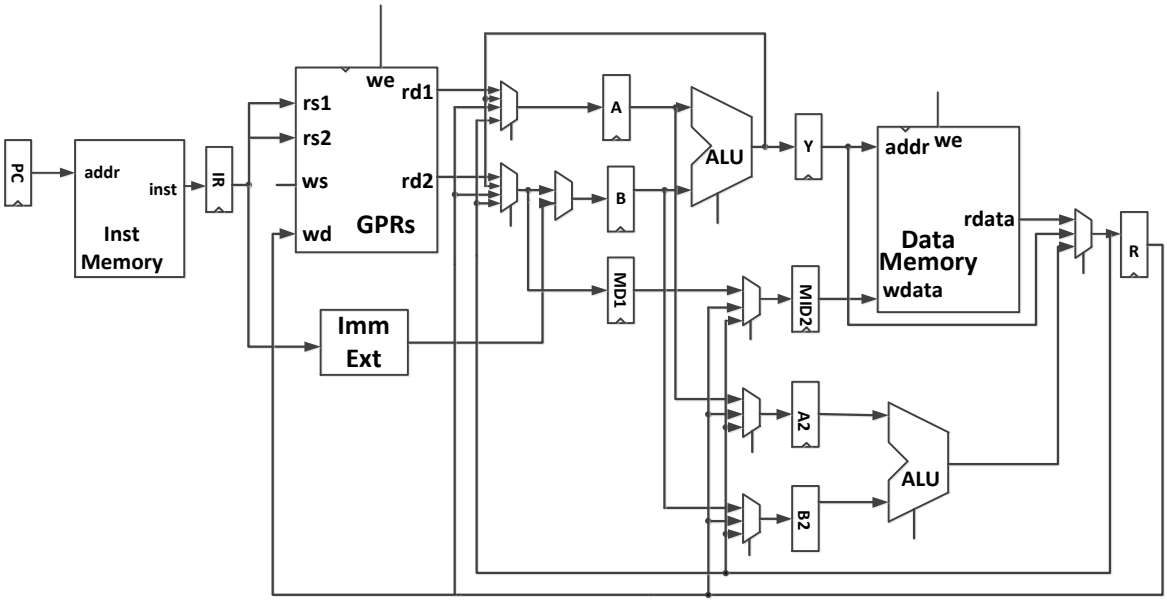

Figure 2 A fully bypassed 5-stage MIPS processor

(1) For the following instruction sequence, indicate which ALU each add instruction uses. Assume that the pipeline is initially idle (for example, it has been executing nothing but nop instructions). Registers involved in inter-instruction dependencies are highlighted in bold.

	ALU1 or ALU2?
`add **r1**, r2, r3`	
`lw **r4**, 0(**r1**)`	
`add **r5**, **r4**, r6`	
`add r7, **r5**, r8`	
`add **r1**, r2, r3`	
`lw r4, 0(**r1**)`	
`add r5, **r1**, r6`	

(2) Indicate whether each of the following instruction sequences causes a stall in the pipeline and **a short summary of the reason why**. Consider each sequence separately and assume that the pipeline is initially idle (for example, it has been executing nothing but nop instructions). Registers involved in inter-instruction dependencies are highlighted in bold.

	stall? (yes/no)
`add **r1**, r2, r3` `lw r4, 0(**r1**)`	

`lw **r1**, 0(r2)`
`add r3, **r1**, r4`
`lw r5, 0(**r1**)`	

`lw **r1**, 0(r2)` `lw r3, 0(**r1**)`	
`lw **r1**, 0(r2)` `sw **r1**, 0(r3)`	

`lw **r1**, 0(r2)`
`add **r3**, **r1**, r4`
`sw r5, 0(**r3**)`	

`lw **r1**, 0(r2)` `add r3, **r1**, r4`	

4. CACHE (12 points):

You are building a system around a processor with in-order execution that runs at 1.1 GHz and has a CPI of 0.7 excluding memory accesses. The only instructions the read or write data from memory are loads (20% of all instructions) and stores (5% of all instructions).

The memory system for this computer is composed of a split L1 cache that imposes no penalty on hits. Both the I-cache and D-cache are direct mapped and hold 32 KB each. The I-cache has a2% miss rate and 32-byte blocks, and the D-cache is write through with a 5% miss rate and16-byte blocks. There is a write buffer on the D-cache that eliminates stalls for 95% of all writes.

The 512 KB write-back and write-allocate, unified L2 cache has 64-byte blocks and an access time of 15ns. It is connected to the L1 cache by a 128-bit data bus that runs at 266 MHz and can transfer on 128-bit per bus cycle. Of all memory references sent to the L2 cache in this system, 80% are satisfied without going to main memory. Also 50% of all blocks replaced are dirty.

The 128-bit-wide main memory has an access latency of 60 ns, after which any number of bus words may be transferred at the rate of one per cycle on the 128-bit-wide 133 MHz main memory bus.

(1) What is the average memory access time for instruction accesses?

(2) What is the average memory access time for data reads?

(3) What is the average memory access time for data writes?

(4) What is the overall CPI, including memory accesses?

5. Virtual Memory (13 points):

Consider a system with 40-bit virtual addresses, 36-bit physical addresses, and 64 KB (2^{16}bytes) pages. The system uses a page map to translate virtual addresses to physical addresses; each page map entry includes dirty (D) and resident (R) bits.

(1) Assuming a flat page map, what is the size of each page map entry, and how many entries does the page map have?

Size of page map entry in bits:

Number of entries in the page map:

(2) If changed the system to use 16 KB (2^{14} bytes) pages instead of 64 KB pages, how would the number of entries in the page map change? Please give the ratio of the new size to the old size.

(# entries with 16 KB pages) / (# entries with 64 KB pages):

(3) Assume we still use 64 KB pages. The contents of the page map and TLB are shown to the right. The page map uses an LRU replacement policy and the LRU page (shown below) will be chosen for replacement. For each of these four accesses, compute its corresponding physical address and indicate whether the access causes a TLB miss and/or a page fault. Assume each access starts with the TLB and Page Map state shown to the right.

TLB

VPN (tag)	V	D	PPN
0x0	1	0	0xBE7A
0x3	0	0	0x7
0x5	1	1	0xFF
0x2	1	0	0x900

Page Map

VPN	R	D	PPN	
0	1	0	0xBE7A	
1	0	0	---	
2	1	0	0x900	
3	1	0	0x8	⇦ LRU PAGE
4	0	0	---	
5	1	1	0xFF	
6	1	0	0x70	

Fill in table below

	Virtual Addr	PPN (in hex)	PhysAddr (in Hex)	TLB Miss? (Y/N)	Page Fault? (Y/N)
1.	0x06004				
2.	0x30286				
3.	0x68030				
4.	0x4BEEF				

6. CHOICE (30 points) (note: only one is correct):

(1) Which one is not one of the five classic components of a computer? ( )

A: Input B: Bus C: Memory D: Output

(2) What is the range of exponent of IEEE 745 single precision? ( )

A: 1~254 B: -128~126 C: -126 ~127 D:-127~128

(3)x = 0100 0110 1101 1000 0000 0000 0000 0000_2 and y = 1011 0110 1110 0000 0000 0000 0000 0000_2. Assume x and y are single precision IEEE754 floating-point numbers. What is the result of x*y in binary? ( )

A: 1111 1101 1011 1101 0000 0000 0000 0000_2

B: 1010 1101 1001 1101 0000 0000 0000 0000_2

C: 1011 1110 0011 1101 0000 0000 0000 0000_2

D: 1111 1101 1010 1101 0000 0000 0000 0000_2

(4) Computer A has an overall CPI of 1.5 and can be run at a clock rate of 750MHz. Computer B has a CPI of 2.5 and can be run at a clock rate of 1GHz. A program has exactly 100,000 instructions when compiled for computer A. How many instructions would the program need to have when compiled for Computer B, in order for the two computers to have exactly the same execution time for this program? ( )

A: 20000 B: 50000 C: 80000 D:100000

(5) Given the following MIPS assembly code (and assuming all registers start at 0):

```
        addi $1, $0, 20
        add $2, $1, $1
repeat:
        addi $2, $2, -4
        nand $3, $2, $2
        addi $1, $1, -2
        bne $0, $1, repeat
```

What is the final value of $3? ( )

A: 0 B: -6 C: 6 D: -1

(6) Beta user-mode applications should not use the XP register. What problems may they cause if they write to XP? ( )

A: Interrupt handlers might loop forever in the operating system (OS) kernel

B: Application data stored in XP may be corrupted

C: OS kernel data stored in XP may be corrupted

D: All of the above

(7) Assume the current PC is 0x10000010, what's next value of PC after execution of "j 255"? ( )

A: 0x000000FF B: 0x10000021 C: 0x100003FC D: 0x100000FF

(8) Pipeline processors increase performance by ( )

A: Increasing instructions per cycle

B: Reducing instruction latency

C: Reducing clock cycle time

D: Reducing context-switch latency

(9) For a 32-bit cache-memory system, a 32KB, 4-way set-associative cache has 2 words cache line size, how many bits are there in such cache's tag? ( )

A: 19 B: 21 C: 23 D: 25

(10) For the following memory access pattern: 1, 5, 1, 6, 3, what's the content of a 4-entries, direct-mapped cache, assuming cache is vacant at the beginning. ( )

A:

	1	6	3

B:

1	6	3	5

C:

5	6	3	

D:

	6	3	

(11) How the cache conflict misses will be affected by the following modifications? Assume the baseline cache is set associative. ( )

(a). Double the associativity while keep the capacity and line size constant

(b). Double the number of sets while keep the capacity and line size constant

A: Decrease; Increase B: Increase; Decrease

C: Increase; Increase D: Decrease; Decrease

(12)A government agency simultaneously monitors 100cellular phone conversations and multiplexes the data onto a network with a bandwidth of 1 MB/sec and an overhead latency of 350 micro-sec per 1KBmessage. Calculate the transmission time per message. Assume that the phone conversation data consists of 2 bytes sampled at a rate of 4 KHz. ( )

A: 0.8s B: 1.35s C: 1s D: 1.08s

(13) Here is a series of address references given as word addresses: 2, 3, 11, 16, 21, 13, 64, 48, 19, 11, 3, 22, 4, 27, 6, 11. Determine how many misses will happen in each condition.

(a)A direct-mapped cache with 16 one-word blocks that is initially empty. ( )

A: 7 B: 8 C: 13 D: 15

(b)A direct-mapped cache with four-word blocks and a total size of 16 words. ( )

A: 7 B: 8 C: 13 D: 15

(c)A two-way set-associative cache with four-word blocks and a total size of 16 words. Use LRU replacement. ( )

A: 7 B: 8 C: 13 D: 15