Exercise 2

2-1. An NMOS with W=50μm and L=0.5μm operates in the saturated region and its layout is folded shown as Fig. 2-1. Calculate the all capacitances by using the parameters in Table2-1 and C_{ox}=3.8×10^{-3} F/m^2, V_R=0.6V. Assume that the minimum size (lateral) of S/D region is 1.5μm.

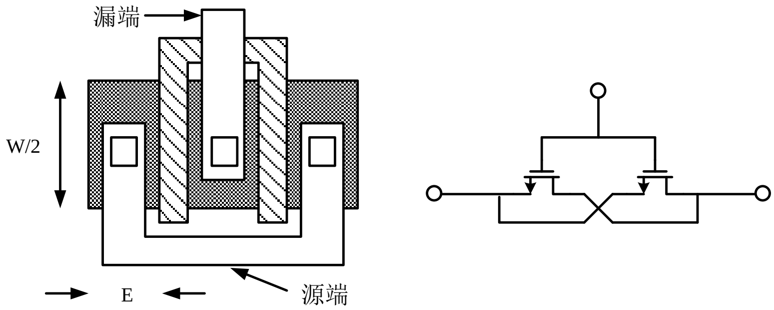


Figure 2-1

Answer:

$$C_{j0}=0.56\times10^{-3}F/m^2, C_{jsw0}=0.35\times10^{-11}F/m, m_j=0.45, m_{jsw}=0.2,$$
$$C_{ov}=0.4\times10^{-9}F/m, W=50\mu m, L=0.5\mu m, L_D=0.08\mu m, E=1.5\times10^{-6}\mu m,$$
$$V_R=0.6V, 2\Phi_F=0.9V, C_{ox}=3.8\times10^{-3}F/m^2, P_{SUB}=9\times10^8 m^{-3},$$
$$\varepsilon_{si}=11.9\times8.85\times10^{-12}F/m, q=1.6\times10^{-19}C$$

$$C_j=\frac{C_{j0}}{(1+V_R/2\Phi_F)^{m_j}} \qquad C_{jsw}=\frac{C_{jsw0}}{(1+V_R/2\Phi_F)^{m_{jsw}}}$$

$$L_{eff}=L-2L_D \qquad C_d=WL_{eff}\sqrt{q\varepsilon_{si}P_{SUB}/4\Phi_F}$$

$$C_{DB}=\frac{W}{2}EC_j+2(\frac{W}{2}+E)C_{jsw}=16.9\,fF$$

$$C_{SB}=2(\frac{W}{2}EC_j+2(\frac{W}{2}+E)C_{jsw})=33.7\,fF$$

$$C_{GD}=2(\frac{W}{2}C_{ov})=20.0\,fF$$

$$C_{GS}=\frac{2}{3}WL_{eff}C_{ox}+WC_{ov}=63.1\,fF$$

C_{GB}：栅-衬底电容在三极管区和饱和区通常被忽略，因为反型层在栅和衬底之间起了“屏蔽”的作用。换句话说，如果栅电压发生变化，电荷是由源和漏提供，而不是由衬底提供。

2-2. There is an N-type current source, I_D is 0.5mA, and the drain-source voltage V_{DS} must larger than 0.4V when it works as a current source. If the minimum output resistance is 20 KΩ, determine the length and width of the device by using the parameters in Table 2.1.

Answer:

$$\begin{cases} r_o = \dfrac{1}{\lambda I_D} = 20K\Omega \\ I_D = 0.5mA \end{cases} \quad \Rightarrow \quad \lambda=0.1$$

From the table2.1, L can be determined as L=0.5um.

$$L_{eff} = L - 2L_D = 0.5\mu m - 2\times 0.08\mu m = 0.34\mu m$$

Calculating W

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L_{eff}}(V_{GS}-V_{TH})^2, \qquad V_{GS}-V_{TH}=V_{DSAT}=0.4V$$

$$\frac{W}{L_{eff}} = \frac{I_D}{\frac{1}{2}\mu_n C_{ox}(V_{GS}-V_{TH})^2} = \frac{0.5\times 10^{-3}}{\frac{1}{2}\times 350\times 10^{-4}\times 3.8\times 10^{-3}\times 0.4^2} = 47$$

$$\therefore\ W = 47L_{eff} = 16\mu m$$

2-3. The layout of an n-channel MOSFET is shown in Fig.2.3. What is this device's width and length?

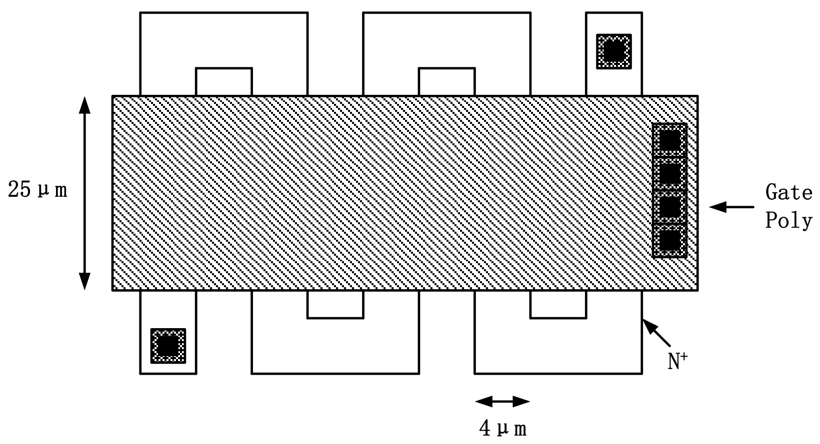


Figure 2.3

Answer:

$$Length = 5\times 25\mu m = 125\mu m$$

$$Width = 4\mu m$$

2-4. A “ring” MOS structure is shown in Fig. 2.4. Explain how the device operations and estimate its equivalent aspect ratio. Calculate the drain junction capacitance of the structure.

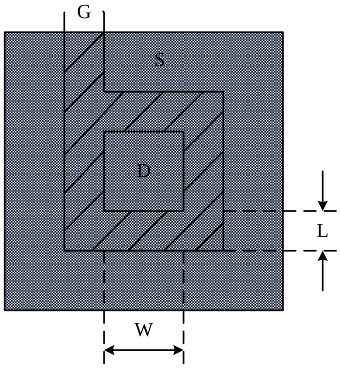


Figure 2.4

Answer:

Width/length ratio is 4W/L

$$C_{DB} = W^2 C_j + 4WC_{jsw}$$

2-5. The layout of a circuit fabricated in n-well technology is shown as Fig.2.5. Give the corresponding schematic and mark the W/L sizes of each transistor. Assume $L = 2\lambda$, $\lambda = 0.4\mu m$.

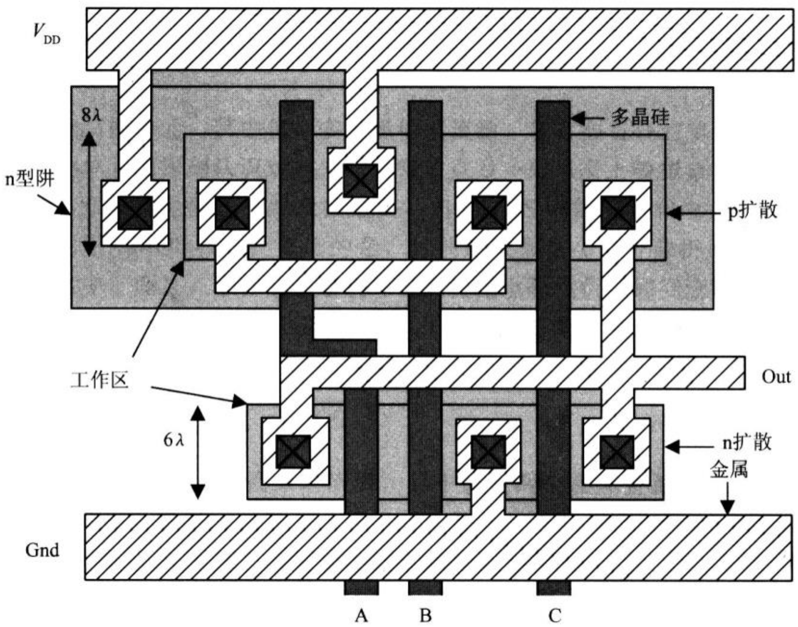
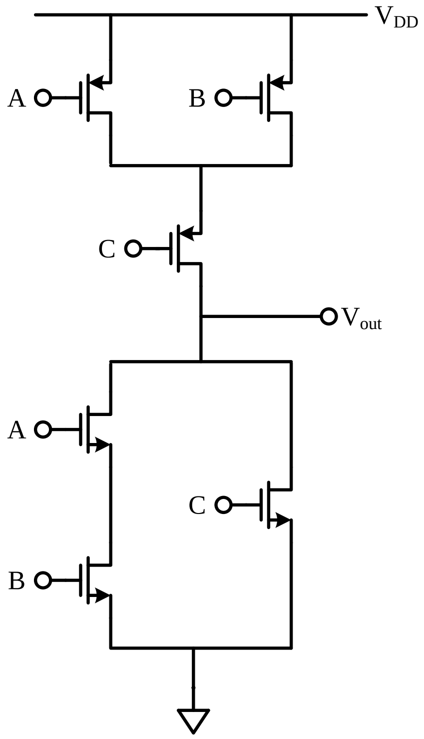


Figure 2.5

Answer:

Schematic



$$\text{Out}=\overline{AB+C}$$

W/L of N-MOSFET:

$$\frac{6\lambda}{2\lambda}=\frac{6\times 0.4}{2\times 0.4}=\frac{2.4}{0.8}$$

W/L of P-MOSFET:

$$\frac{8\lambda}{2\lambda}=\frac{8\times 0.4}{2\times 0.4}=\frac{3.2}{0.8}$$

Table 2.1

NMOS Model			
LEVEL=1	VTO=0.7	GAMMA=0.45	PHI=0.9
PSUB=9e+14	LD=0.08e-6	UO=350	LAMBDA=0.1
TOX=9e-9	PB=0.9	CJ=0.56e-3	CJSW=0.35e-11
MJ=0.45	MJSW=0.2	CGDO=0.4e-9	JS=1.0e-8
PMOS Model			
LEVEL=1	VTO=-0.8	GAMMA=0.4	PHI=0.8
PSUB=5e+14	LD=0.09e-6	UO=100	LAMBDA=0.2
TOX=9e-9	PB=0.9	CJ=0.94e-3	CJSW=0.32e-11
MJ=0.5	MJSW=0.3	CGDO=0.3e-9	JS=0.5e-8

上表给出的是 0.5μm 工艺 level 1 MOS SPICE 模型参数的典型值，其中的参数定义如下：

VTO:	VSB=0 时的阈值电压	（单位：V）
GAMMA:	体效应系数	（单位：$V^{1/2}$）
PHI:	$2\Phi_F$	（单位：V）
TOX:	栅氧厚度	（单位：m）
NSUB:	衬底掺杂浓度	（单位：cm^{-3}）
LD:	源/漏侧扩散长度	（单位：m）
UO:	沟道迁移率	（单位：cm2/(v/s)）
LAMBDA:	沟道长度调制系数	（单位：V^{-1}）
CJ:	单位面积的源/漏结电容	（单位：F/m^2）
CJSW:	单位长度的源/漏侧壁结电容	（单位：F/m）
PB:	源/漏结内建电势	（单位：V）
MJ:	CJ 公式中的幂指数	（无单位）
MJSW:	CJSW 等式中的幂指数	（无单位）
CGDO:	单位宽度的栅/漏交叠电容	（单位：F/m）
CGSO:	单位宽度的栅/源交叠电容	（单位：F/m）
JS:	源/漏结单位面积的漏电流	（单位：A/m^2）