集成电路原理与设计
7.单级放大器

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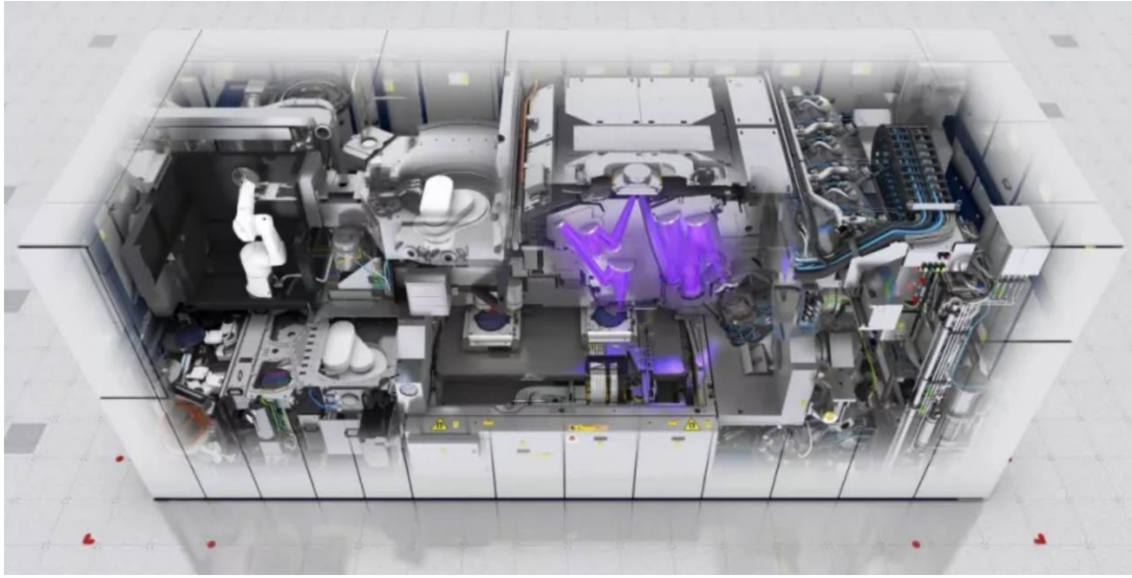
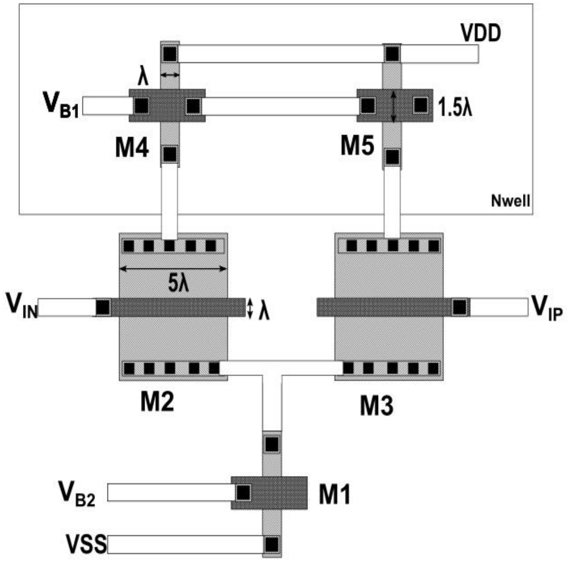
Syllabus

课数	内容	课数	内容
1	导论	9	差分放大器
2	工艺流程	10	运算放大器
3	器件模型一	11	逻辑门
4	器件模型二	12	组合逻辑
5	模拟基本单元	13	时序逻辑
6	电流镜与基准	14	加法器/乘法器
7	单级放大器	15	集成电路专题讲座一
8	课堂测验	16	集成电路专题讲座二

Recall the main points (1)

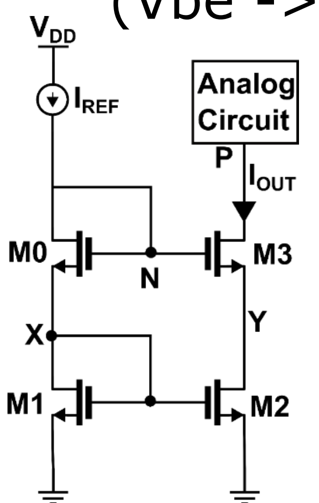
- Moore's Law
- Analog vs. digital in technology scaling down
- Transistor operation region and Equations
- Second order effect (body, channel length, short channel)
- Basic technology steps, lithography first, recognize layout

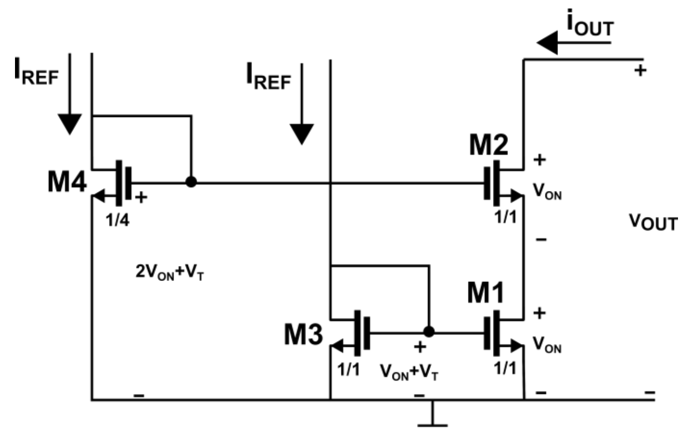


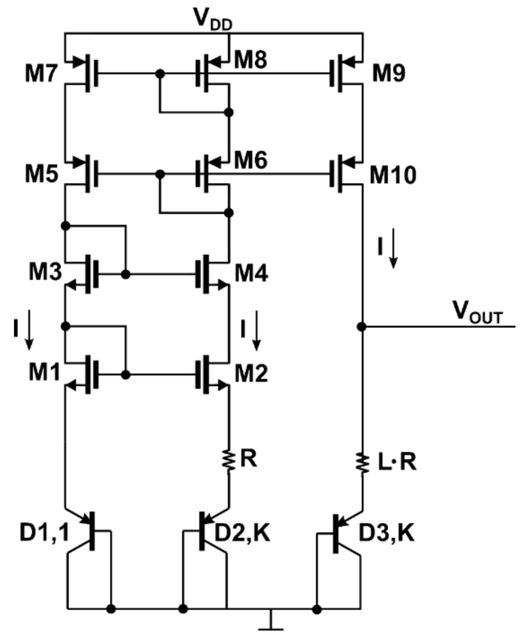


Recall the main points (2)

- Transistor as switches -> Linear region
- Transistor as diodes -> saturation region (1/gm)
- Transistor as current sink/source -> saturation region (rds)
- Current reference and mirror, matching considerations
- Cascode current mirror, Low voltage current mirror
- Bandgap reference
  (Vbe -> Neg. TC, ΔVbe -> Pos. TC)







Outline

- General Consideration
- Common-Source Stage
  - CS Stage with Resistive Load
  - CS Stage with Diode-Connected Load
  - CS Stage with Current-Source Load
  - CS Stage with Source Degeneration
- Source Follower
- Common-Gate Stage

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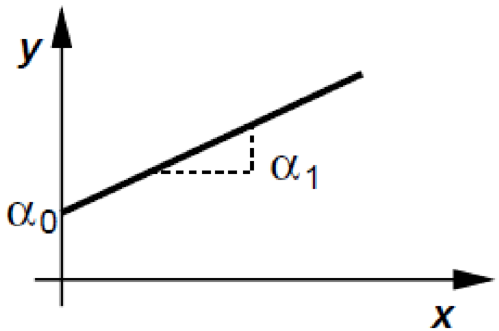
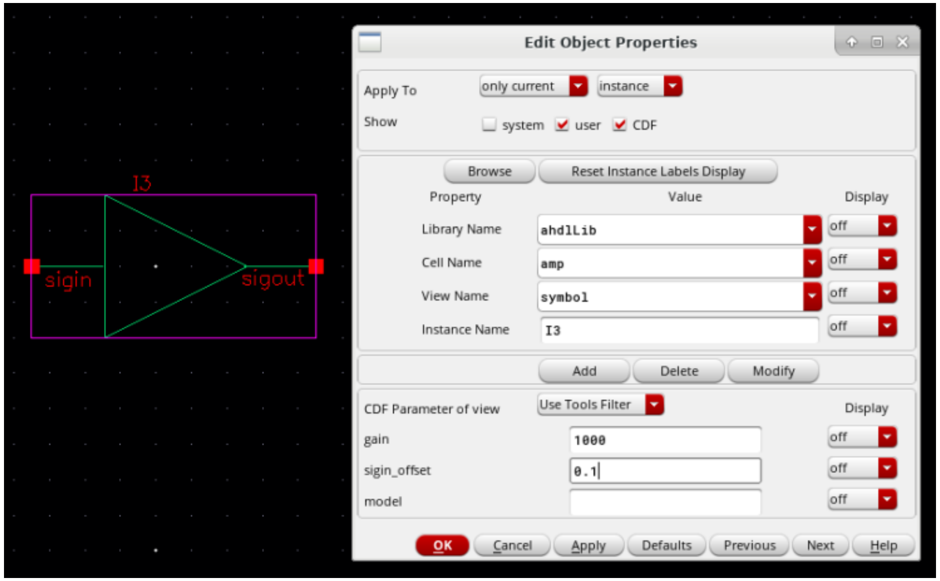
Amplifier: Ideal vs. Non-ideal (1)



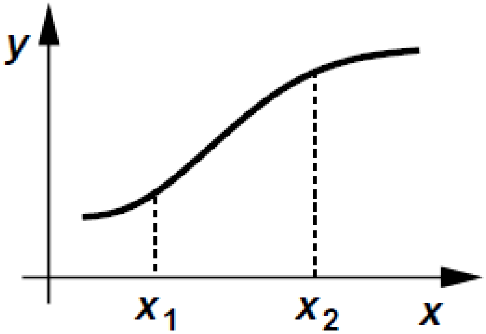
Ideal amplifier:

$$y(t) = a_0 + a_1 x(t)$$

- Large-signal characteristic:
  a straight line
- α_1: the “gain”
- α_0: the “DC bias”



Amplifier: Ideal vs. Non-ideal (2)



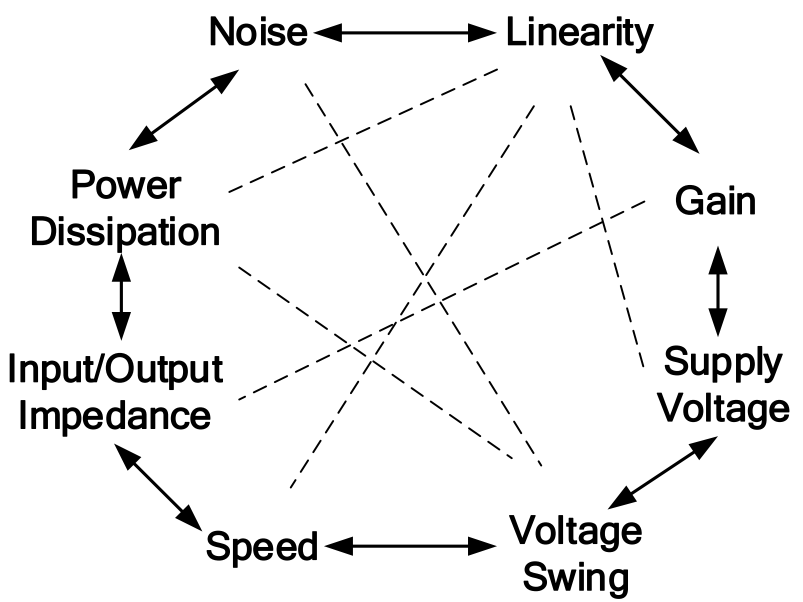
Nonlinear amplifier

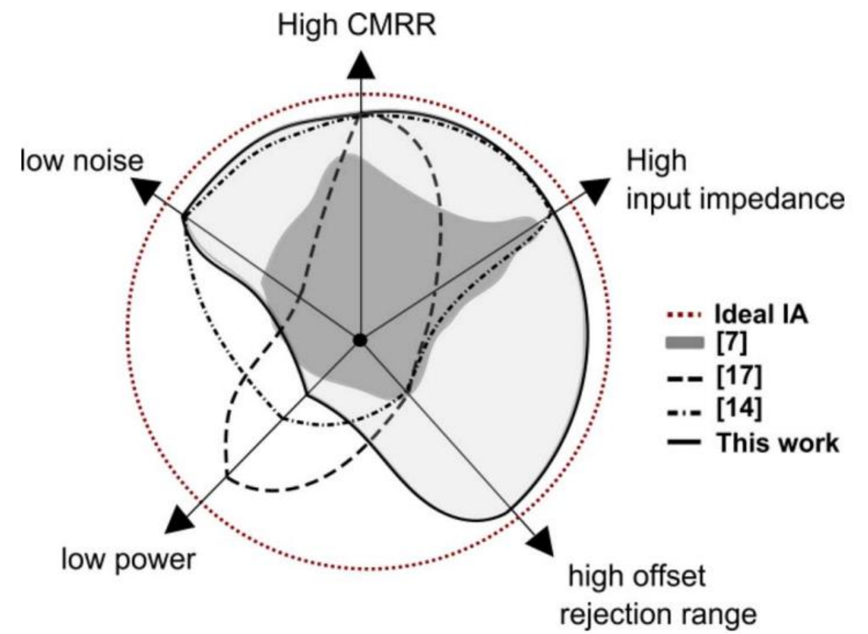
$$y(t) = a_0 + a_1 x(t) + a_2 x^2(t) + \ldots + a_n x^n(t)$$

- Large signal excursions around bias point
- **Varying "gain",** approximated by polynomial
- Causes distortion of signal of interest
- In a sufficiently narrow range, *x* varies very little, and

$$\Delta y(t) = a_1 \Delta x(t)$$

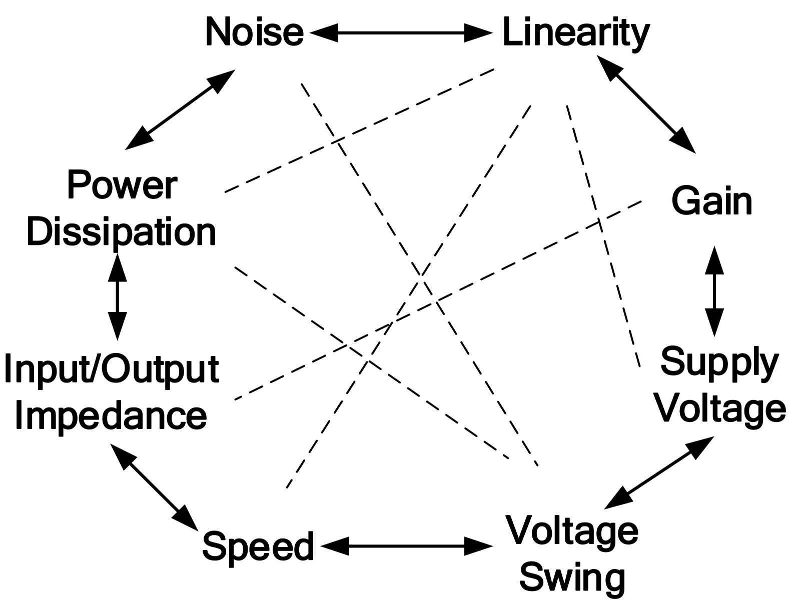
Analog Design Octagon (1)





- Performance parameters trade with each other (via Gm)
- Multi-dimensional optimization problem

Analog Design Octagon (2)



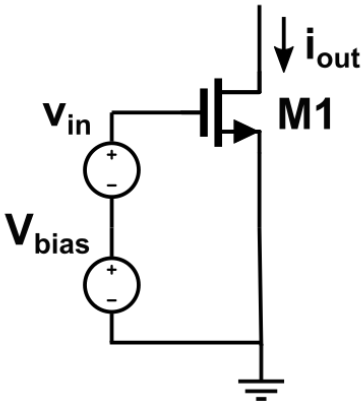
- Power <-> Gm <-> Noise
- Power <-> Gm <-> Bandwidth <-> Speed
- Power <-> Supply <-> Swing
- Gain <-> Bandwidth <-> Power
- Gm <-> W/L <-> Zin

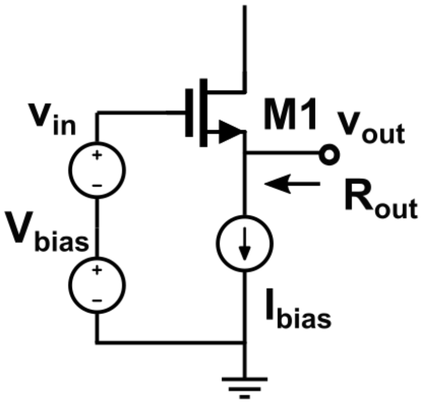
- Difficult to be done by AI

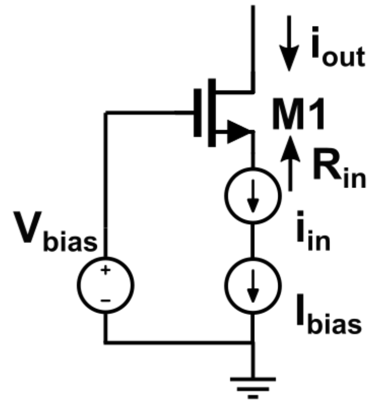
Single-Stage Amplifier

Common-Source Stage	Source Follower	Common-Gate Stage	Cascode
With Resistive Load With Diode-Connected Load With Current-Source Load With Active Load With Source Degeneration	With Resistive Bias With Current-Source Bias	With Resistive Load With Current-Source Load	Telescopic Folded

Common source **Common drain** **Common gate**







$i_{out} = g_m v_{in}$

vout = vin

$R_{out} \approx 1/g_m$

$i_{out} = i_{in}$

$R_{in} \approx 1/g_m$

Inverse gain **Unit gain** **Current Buffer**

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Outline

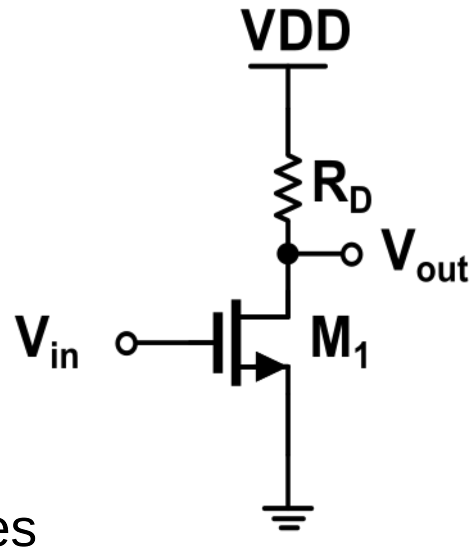
- For Common source/drain/gate
- From large signal to small signal to frequency behaviour
- Trade-offs

CS Stage with Resistive Load

- Common-Source Amplifier：
- Input voltage: V_{GS}
- Output voltage: V_{DS}

Via Gm

$$V_{GS} \xrightarrow{g_m} I_{DS} \xrightarrow{R_D} V_{DS}$$

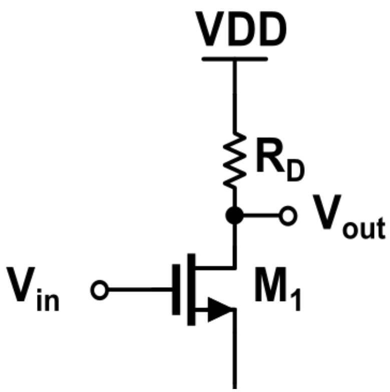


- Very high input impedance at low frequencies

  parasitic **C**in = **C**gs + A***C**gd

- Two Kinds of Analysis Method
  - Large-signal Analysis
  - Small-signal Analysis

Large-signal Analysis (1)



V_{in} increases from 0

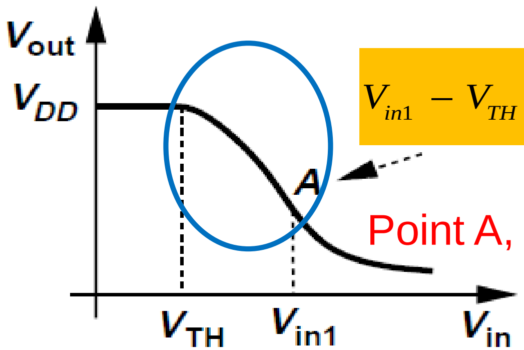
① $V_{in} < V_{TH}$: M_1--off, $I_D = 0$, $V_{out} = V_{DD}$

② $V_{in} > V_{TH}$: $V_{out} = V_{DS} > V_{in} - V_{TH}$

M_1--saturation region,

$$\boxed{V_{out} = V_{DD} - \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{in} - V_{TH}\right)^2 R_D}$$

$V_{in}\uparrow$, $V_{out}\downarrow$



$$V_{in1} - V_{TH} = V_{DD} - R_D\frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{in1} - V_{TH}\right)^2$$

Point A, $V_{out} = V_{in1} - V_{TH}$

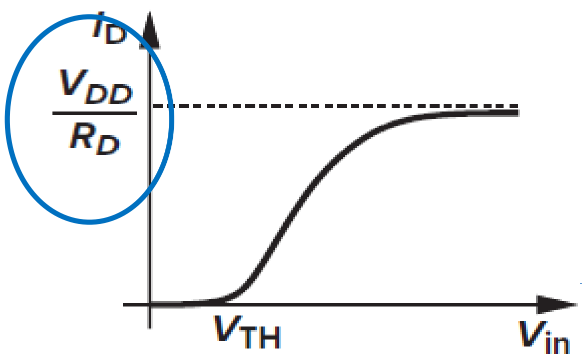
③ $V_{in} > V_{in1}$: M_1-- triode region

$$V_{out} = V_{DD} - \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left[2\left(V_{in} - V_{TH}\right)V_{out} - V_{out}^2\right]R_D$$

④ V_{in} is high enough: M_1--deep triode region

$V_{out} << 2(V_{in} - V_{TH})$

$$V_{out} = \frac{R_{on}}{R_{on} + R_D}V_{DD} = \frac{V_{DD}}{1 + \mu_n C_{ox}\frac{W}{L}R_D\left(V_{in} - V_{TH}\right)}$$

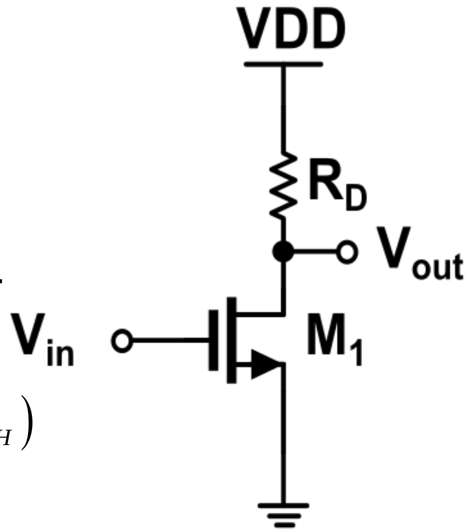


Large-signal Analysis (2)

- **In saturation region, small-signal gain:**

$$V_{out} = V_{DD} - \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in} - V_{TH})^2 R_D$$

$$\boxed{A_v = \frac{\partial V_{out}}{\partial V_{in}} = -\mu_n C_{ox}\frac{W}{L}(V_{in} - V_{TH}) R_D = -g_m R_D}$$



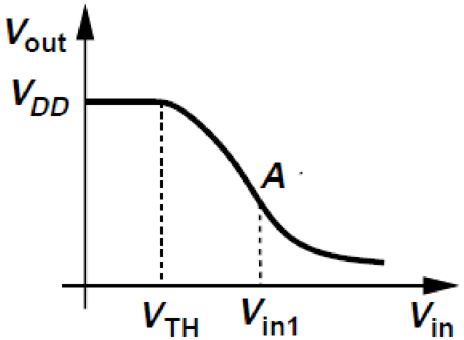
- A_v increases linearly with V_{in};
- When the signal swing of V_{in} is large, non-linearity is an undesirable effect.

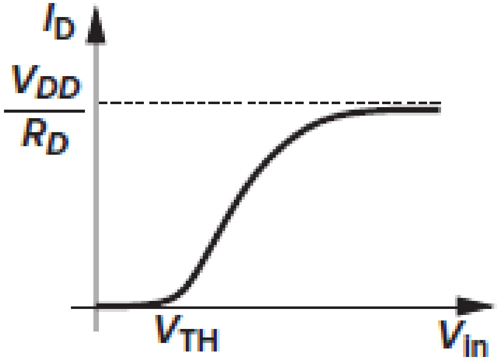
- ***g_m with the input voltage***

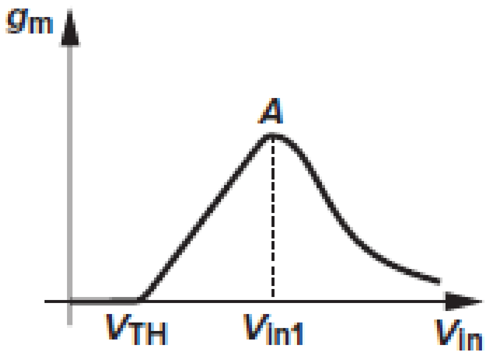
Saturation: $g_m = \mu_n C_{ox}\frac{W}{L} R_D (V_{GS} - V_{TH}) = \mu_n C_{ox}\frac{W}{L} R_D (V_{in} - V_{TH})$

Linear: $g_m = \mu_n C_{ox}\frac{W}{L} V_{DS} = \mu_n C_{ox}\frac{W}{L} V_{out}$

$$V_{out} = V_{DD} - R_D \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left[2(V_{in} - V_{TH})V_{out} - V_{out}^2\right]$$







Frequency & Noise Behavior

- The bandwidth of the Common Source Stage

- $A = G_m * r_o / (1+s*r_o*C_o)$

- C_o ~ W*L（Parasitic capacitance）

- Current Noise: $I^2 = (2/3) * 4kT/Gm$

- Voltage Noise: $V^2 = (2/3) * 4kTGm$

How to maximize the gain?

$$A_v = -g_m R_D = -\sqrt{2\mu_n C_{ox}\frac{W}{L}I_D}\,\frac{V_{RD}}{I_D} = -\sqrt{2\mu_n C_{ox}\frac{W}{L}}\,\frac{V_{RD}}{\sqrt{I_D}}$$

- Increase W/L: **Parasitic capacitance**
- Increase V_{RD}: **Output swing decrease -> 0.5*V_{DD}**
- Decrease I_D: **The circuit get slower**

Trade-off : Gain, bandwidth and voltage swing!

Channel length modulation:

$$V_{out} = V_{DD} - \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{in} - V_{TH}\right)^2 \left(1 + \lambda V_{out}\right) R_D$$

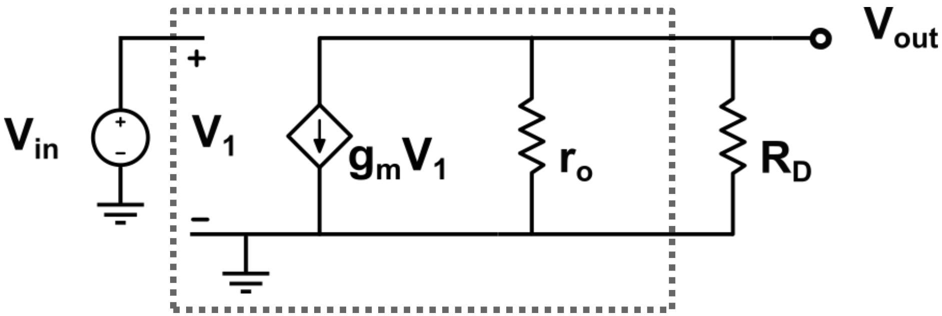
$$r_O = \frac{1}{\lambda I_D}$$

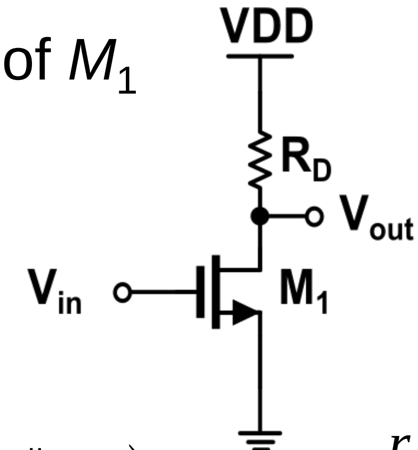
$$A_v = \frac{\partial V_{out}}{\partial V_{in}} = -g_m \frac{r_O R_D}{r_O + R_D} = -g_m \left(r_O \parallel R_D\right)$$

$\Rightarrow$ $g_m \uparrow, R_D \uparrow \Rightarrow A_V \uparrow$

Small-signal Analysis

- Including channel-length modulation of M_1





$$V_{out} = -g_m V_1 \left(r_O \| R_D\right)$$

$V_{in}=V_1$

$$A_v = -g_m \left(r_O \| R_D\right) = -g_m \frac{r_O R_D}{r_O + R_D}$$

$$= -g_m R_{out}$$

- **Output impedance:**
  - When zero input, apply voltage at output and get output current

$V_{in}=0$

$$\frac{V_o}{I_o} = \left(r_O \| R_D\right)$$

$$R_{out} = \left(r_O \| R_D\right)$$

if $\lambda=0$, $r_o=\infty$

$$R_{out} = R_D$$

Why??

Channel-Length Modulation

$$I_D \approx \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{GS}-V_{TH}\right)^2\left(1+\lambda V_{DS}\right)$$

- I_D is not a constant current, depending on V_{DS}

$$\lambda \propto \frac{1}{L}\frac{\sqrt{V_{DS}-V_{D,sat}+\Phi}}{V_{DS}}$$

$$\boxed{L\uparrow \Rightarrow \lambda\downarrow}$$

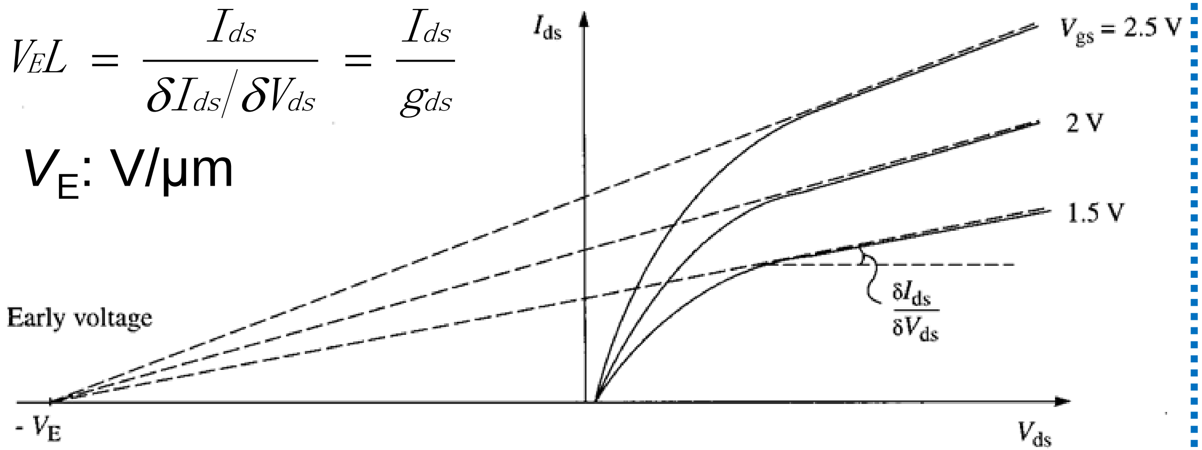
- λ changes with L => V_E

$$g_{ds}=\frac{\partial i_D}{\partial v_{DS}}\bigg|_{V_{GS},const}=g_0=\frac{I_D\lambda}{1+\lambda V_{DS}}\approx I_D\lambda$$

$$\boxed{r_O=\frac{1}{I_{DS}\lambda}}$$

$$V_E L=\frac{I_{ds}}{\delta I_{ds}/\delta V_{ds}}=\frac{I_{ds}}{g_{ds}}$$

V_E: V/μm



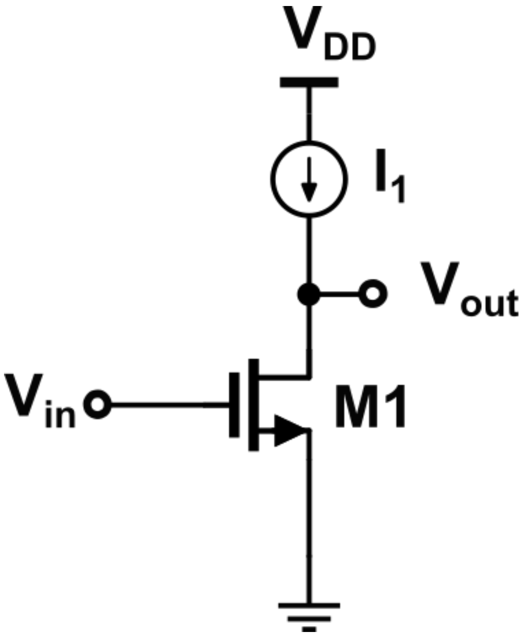
Early Voltage

工艺参数

$$\boxed{\lambda=\frac{1}{V_E L}\qquad r_O=\frac{V_E L}{I_{DS}}}$$

Example

Ideal Current Source Load. M1 is biased in saturation



$$R_D \to \infty$$

$$A_v = -g_m \left(R_D \| r_O\right) = -g_m r_O$$

Intrinsic Gain:

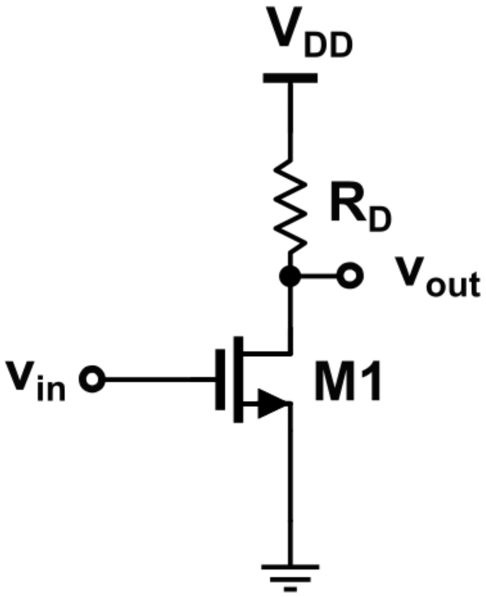
- the maximum voltage gain that can be achieved using a single device.

$$I_{D1} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{in} - V_{TH}\right)^2\left(1 + \lambda V_{out}\right) = I_1$$

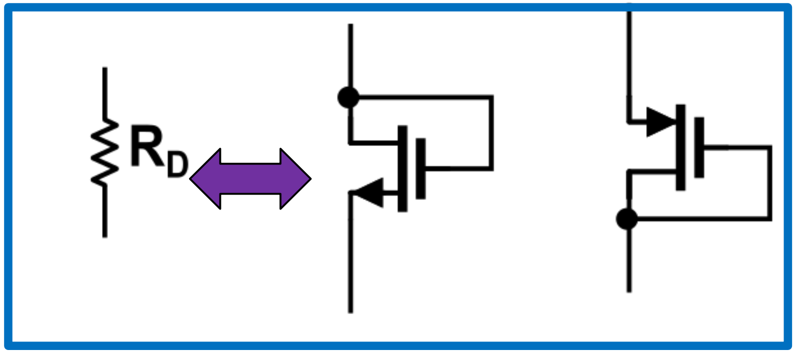
$V_{in} \uparrow$ $\quad$ $V_{out} \downarrow\downarrow$ $\quad$ **Again**

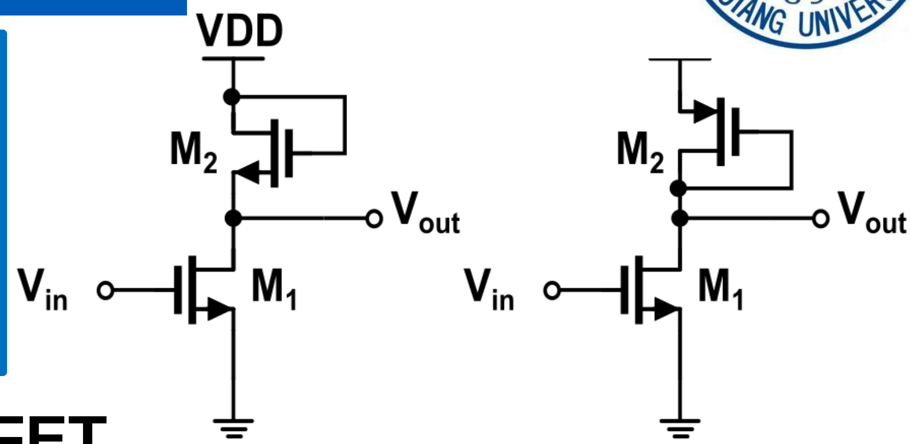
How to improve?

- Disadvantage of CS with resistive load
  - Be difficult to fabricate resistors with tightly-controlled value
  - Limited resistor value, reduce the swing of output
  - A reasonable physical size
- How to improve ?
  - Resistor -> **MOS device**
    - Diode-connected load
    - Current source
    - MOS in triode load
    - ……



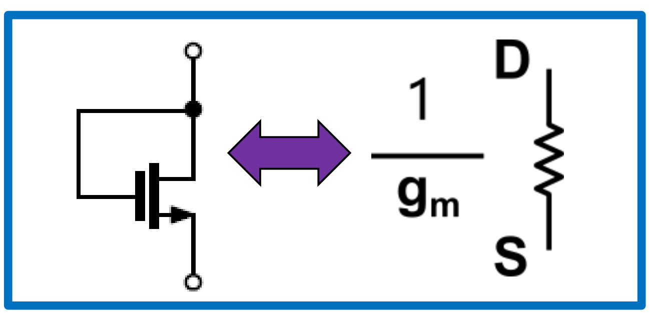
CS Stage with Diode-Connected

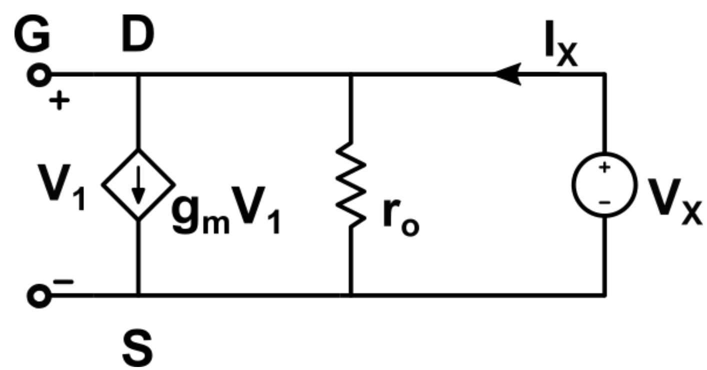




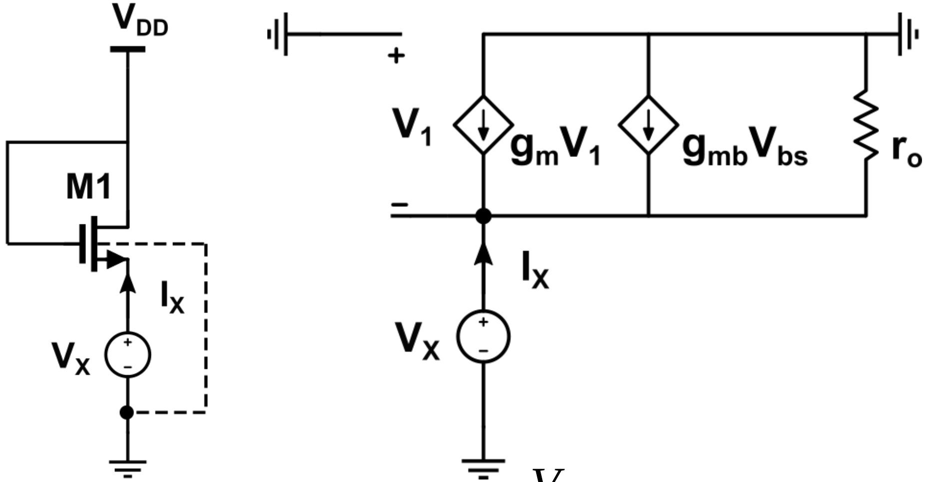
Diode-Connected MOSFET

- the gate and drain are shorted -> **transistor always operates in saturation**
- as a small-signal resistor (**Active Resistor**)
- a "diode-connected" device





Measure of the Equivalent Impedance



$$V_1 = -V_X$$

$$V_{bs} = -V_X$$

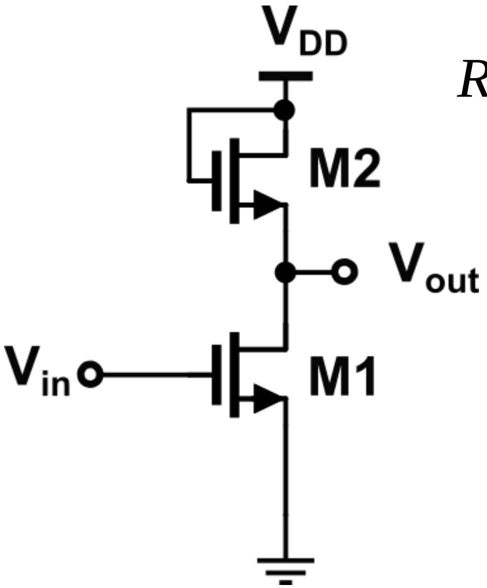
$$(g_m + g_{mb})V_X + \frac{V_X}{r_O} = I_X$$

$$\frac{V_X}{I_X} = \frac{1}{g_m + g_{mb} + r_O^{-1}} = \frac{1}{g_m + g_{mb}} // r_O$$

$$\boxed{R_X \approx \frac{1}{g_m + g_{mb}}}$$

($g_m >> g_{mbs}$, $g_m >> 1/r_O$)

CS with Diode-Connected Load: NMOS



$$R_D \Leftrightarrow \frac{1}{g_{m2}} // \frac{1}{g_{mb2}}$$

$$\boxed{R_{out} = \left(\frac{1}{g_{m2}} // \frac{1}{g_{mb2}}\right) // r_{O1} \approx \frac{1}{g_{m2}} // \frac{1}{g_{mb2}}}$$

$$A_v \approx \frac{-g_{m1}}{g_{m2} + g_{mb2}} = -\frac{g_{m1}}{g_{m2}} \frac{1}{1+\eta} \qquad \eta = g_{mb2}/g_{m2}$$

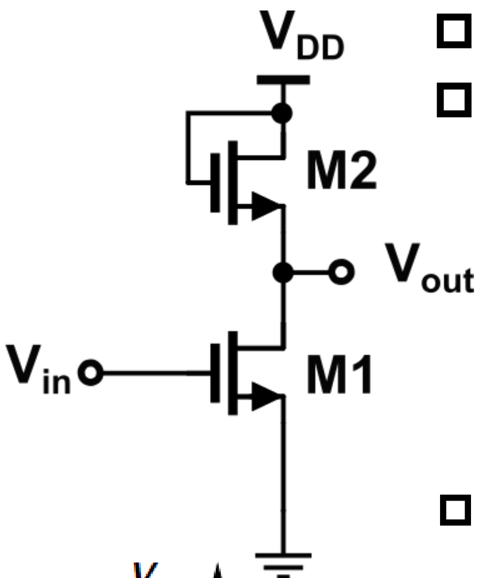
$$A_v = -\sqrt{\frac{2\mu_n C_{ox} (W/L)_1 I_{D1}}{2\mu_n C_{ox} (W/L)_2 I_{D2}}} \frac{1}{1+\eta} = -\sqrt{\frac{(W/L)_1}{(W/L)_2}} \frac{1}{1+\eta}$$

If η is neglected

Body-effect !

- the gain is independent of the bias current and voltages
  - *As the input and output signal levels vary, the gain remains relative constant*
- the gain is decided by **the ratio** of (W/L) of M_1 and M_2 (accurate)
- the input-output characteristic is relatively linear

Large-signal Analysis

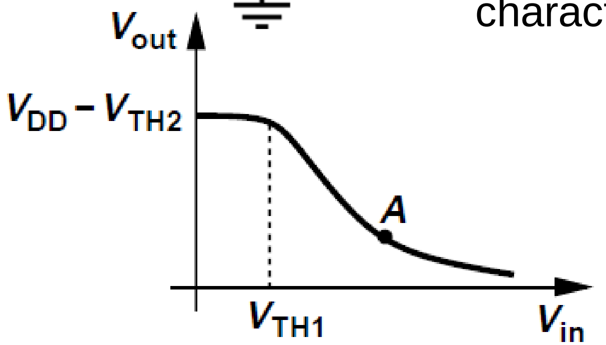


- $V_{in} < V_{TH1}$: $V_{out} = V_{DD} - V_{TH2}$
- $V_{in} > V_{TH1}$, M_1 and M_2 in saturation region, V_{out} approximately follows a single line

$$\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{in} - V_{TH1})^2 = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{DD} - V_{out} - V_{TH2})^2$$

$$\sqrt{\left(\frac{W}{L}\right)_1}(V_{in} - V_{TH1}) = \sqrt{\left(\frac{W}{L}\right)_2}(V_{DD} - V_{out} - V_{TH2})$$

- If V_{TH2} does not vary much with V_{out}, input-output characteristic is relatively linear.



$$\sqrt{\left(\frac{W}{L}\right)_1} = \sqrt{\left(\frac{W}{L}\right)_2}\left(-\frac{\partial V_{out}}{\partial V_{in}} - \frac{\partial V_{TH2}}{\partial V_{in}}\right)$$

$$\partial V_{TH2}/\partial V_{in} = (\partial V_{TH2}/\partial V_{out})(\partial V_{out}/\partial V_{in}) = \eta(\partial V_{out}/\partial V_{in})$$

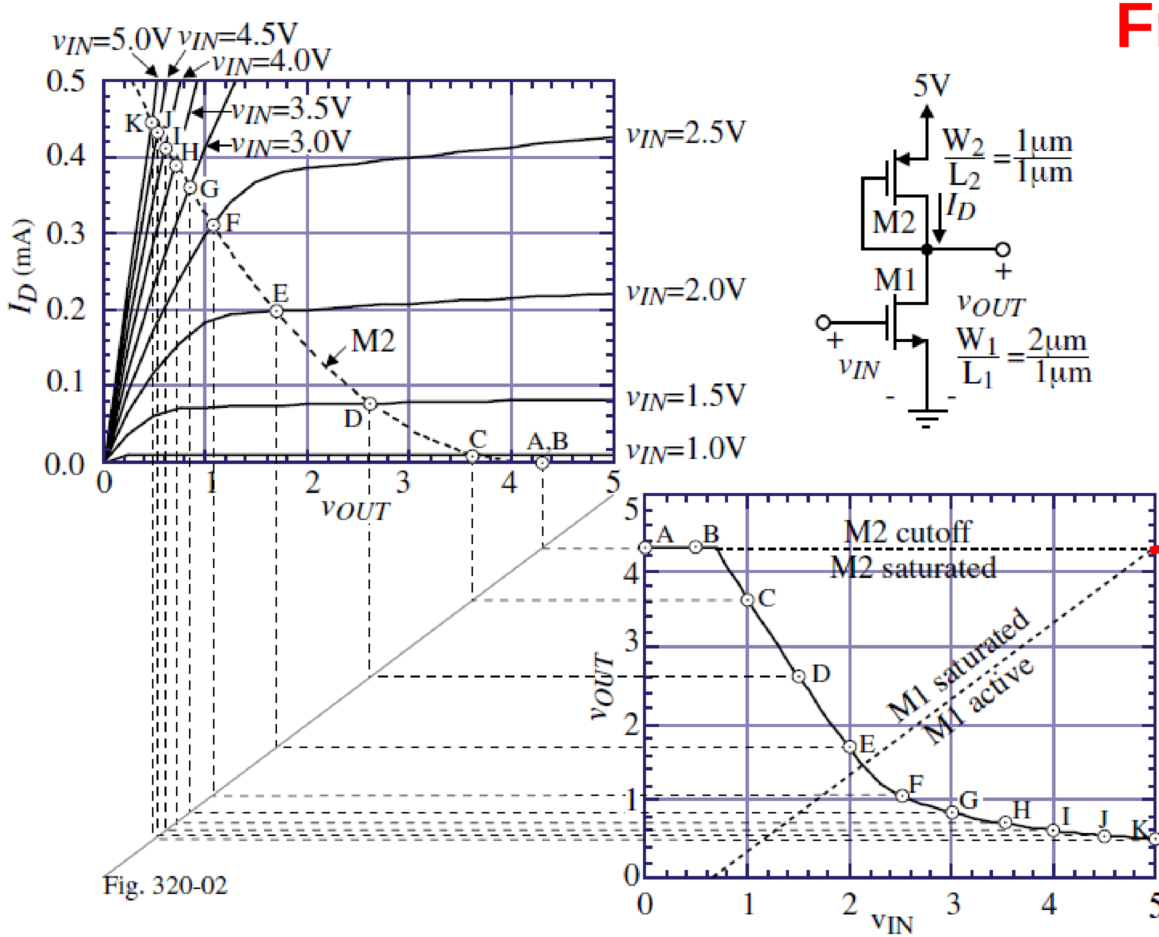
$$\Rightarrow \quad \frac{\partial V_{out}}{\partial V_{in}} = -\sqrt{\frac{(W/L)_1}{(W/L)_2}}\frac{1}{1+\eta}$$

- $V_{in} > V_{out} + V_{TH1}$, M_1 enters the triode region => the characteristic becomes nonlinear

CS with Diode-Connected Load - PMOS

- **Transfer function**

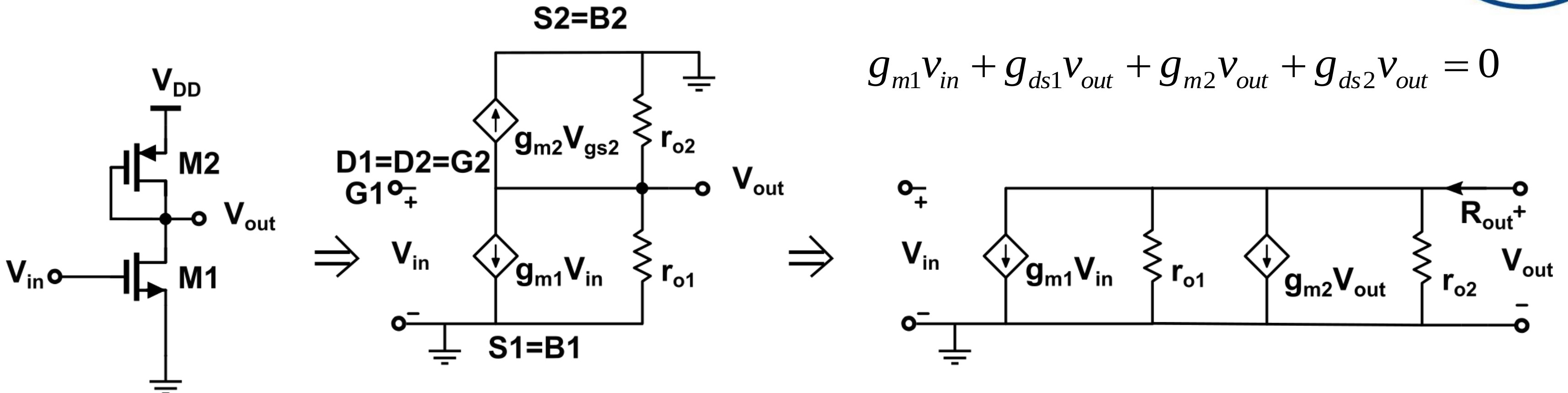
Free of body-effect !



$$v_{DS1} \geq v_{GS1} - V_{TN}$$

$$v_{OUT} \geq v_{IN} - 0.7\text{V}$$

Small-signal Analysis



$$g_{m1}v_{in}+g_{ds1}v_{out}+g_{m2}v_{out}+g_{ds2}v_{out}=0$$

$$\frac{v_{out}}{v_{in}}=\frac{-g_{m1}}{g_{O1}+g_{O2}+g_{m2}}$$

$$R_{out}=\frac{1}{g_{O1}+g_{O2}+g_{m2}}=\frac{1}{g_{m2}}//r_{O1}//r_{O2}\approx\frac{1}{g_{m2}}$$

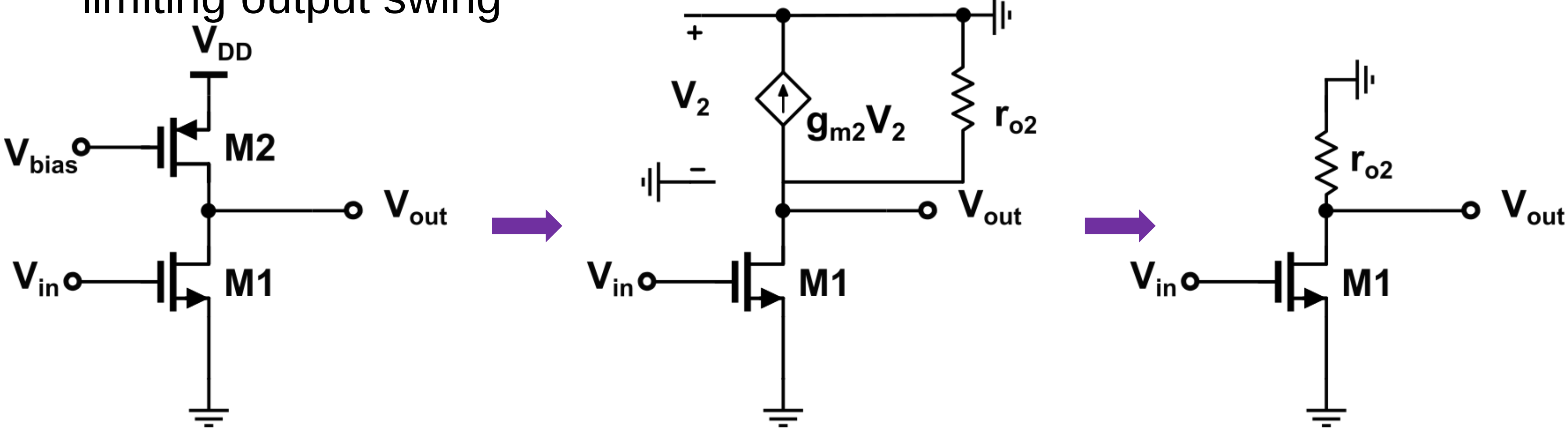
$$A_v=\frac{-g_{m1}}{g_{O1}+g_{O2}+g_{m2}}\approx-\frac{g_{m1}}{g_{m2}}=-\sqrt{\frac{\mu_n(W/L)_1}{\mu_p(W/L)_2}}$$

$$\boxed{A_v=-g_{m1}R_{out}}$$

- Gain is a relatively weak function of device dimensions
- High gain => $(W/L)_1 >> (W/L)_2$
- =>disproportionately wide or long transistor (large input or load capacitor)
  reduction in **allowable voltage swing (the same as R as the load)**

CS Stage with Current Source Load

- Current-source load allows a **high load resistance (why?)** without limiting output swing



$$r_{out} = r_{O1} // r_{O2}$$

$$A_v = -g_{m1} r_{out} = -g_{m1}\left(r_{O1} // r_{O2}\right)$$

- Longer transistors yield a higher voltage gain

r_{o2} can be increased by increasing its length $\because L\uparrow, \lambda\downarrow \Rightarrow r_o\uparrow \Rightarrow A_V\uparrow$

CS Stage with Current Source Load

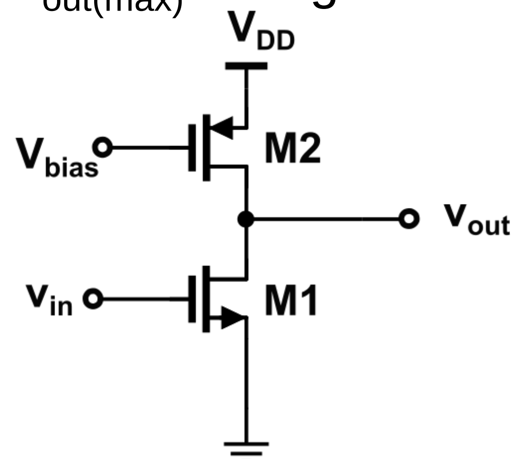
$$A_v = -g_{m1} r_{out} = -g_{m1}\left(r_{O1} // r_{O2}\right)$$

- For M_2, $I = \frac{1}{2}\mu_n C_{OX}\frac{W}{L}V_{ON}^2 = \frac{1}{2}\beta V_{ON}^2 \propto \frac{W}{L}V_{ON}^2$

  -- if I is constant, $W_2\uparrow$ -> $V_{ON2}\downarrow$ $V_{DS2,sat} \approx V_{ON2}$, $V_{out(max)}$ is large

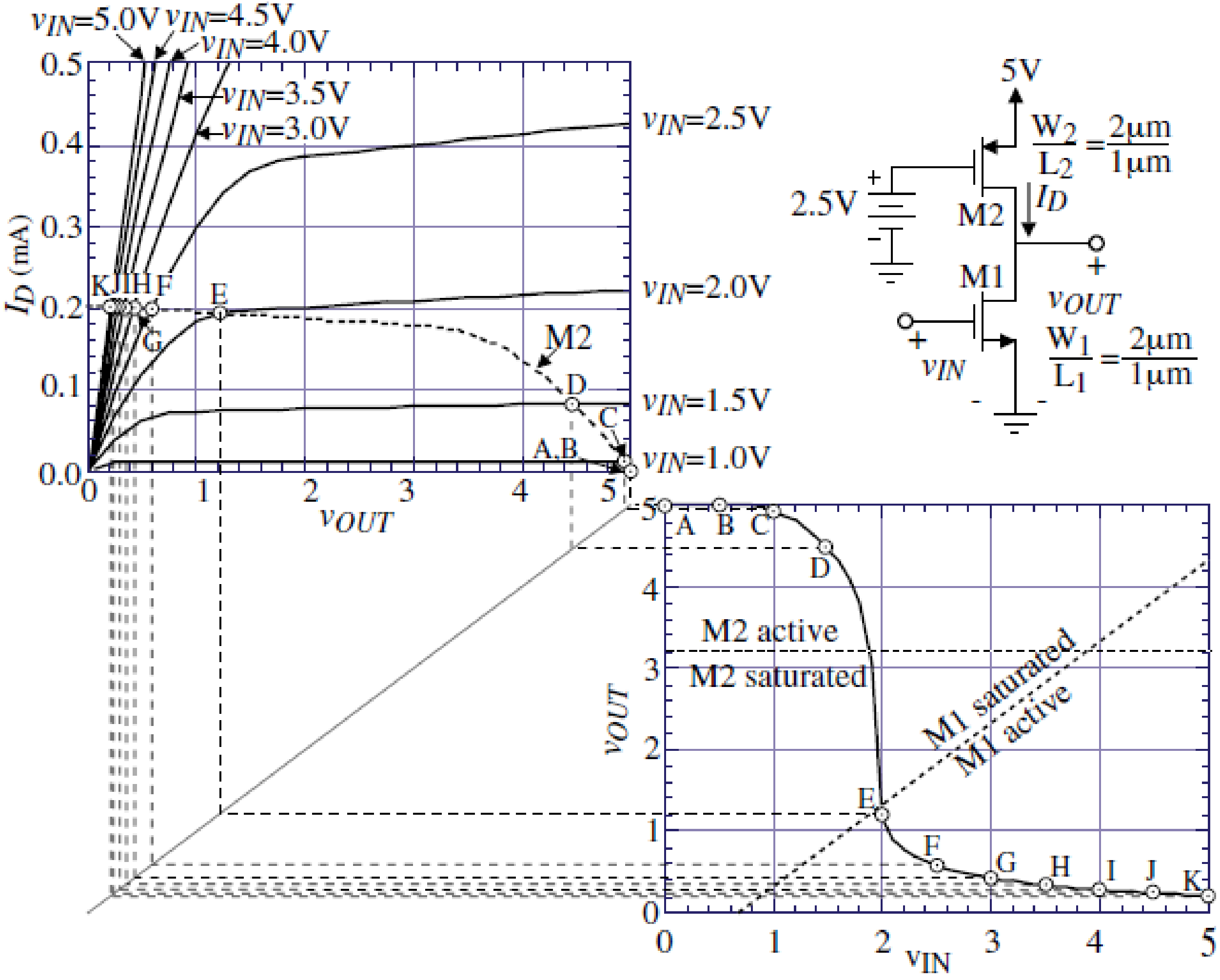
  200~300 mV

  -- $W_2\uparrow$ $L_2\uparrow$ -> parasitic capacitor of $M_2\uparrow$



- For M_1, $g_m = \sqrt{2\beta I_D}$ $\left(\frac{W}{L}\right)_1 \uparrow \Rightarrow g_{m1}\uparrow$
  - I is constant, $\because I = \frac{1}{2}\beta V_{ON}^2$ $\left(\frac{W}{L}\right)_1 \uparrow \Rightarrow V_{ON}\downarrow$

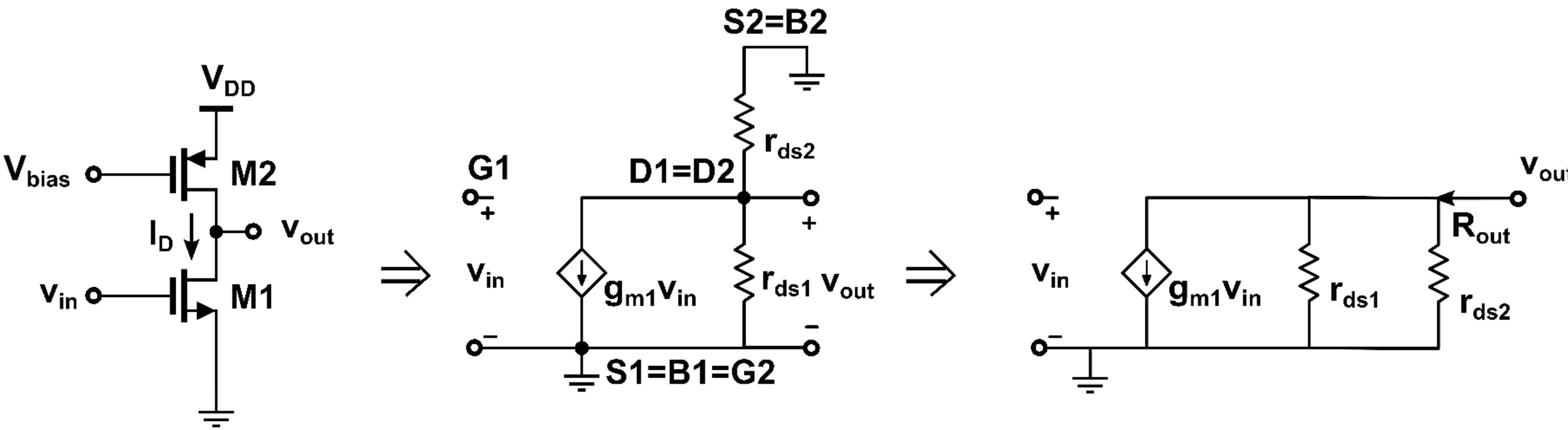
Transfer function



High Gain

Small input range

Small-signal Performance



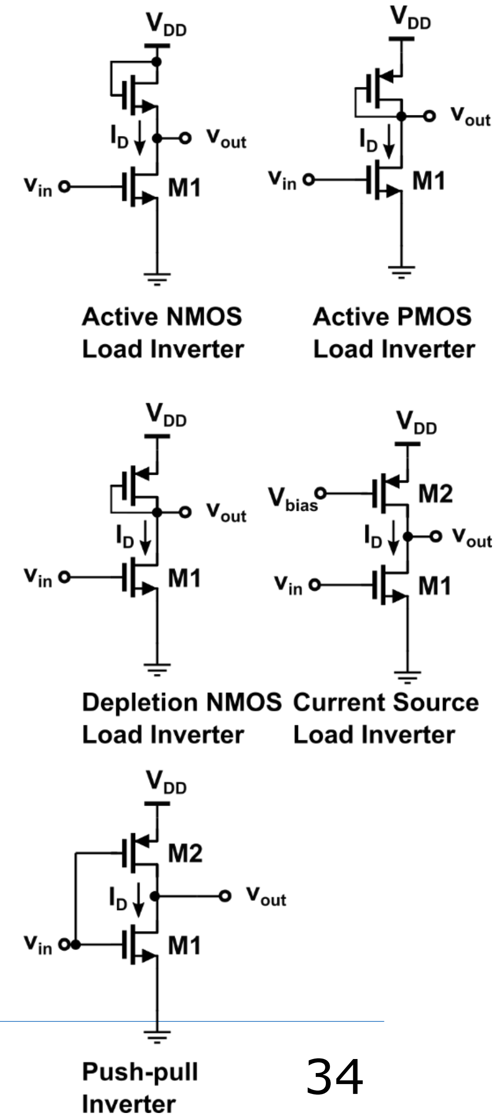
$$\frac{v_{out}}{v_{in}} = \frac{-g_{m1}}{g_{ds1} + g_{ds2}} = \left(\frac{2K'_N W_1}{L_1 I_D}\right)^{1/2} \left(\frac{-1}{\lambda_1 + \lambda_2}\right) \propto \frac{1}{\sqrt{I_D}} \text{ !!!} \quad \text{and } R_{out} = \frac{1}{g_{ds1} + g_{ds2}} \cong \frac{1}{I_D(\lambda_1 + \lambda_2)}$$

$$\boxed{A_v = -g_{m1} R_{out} = -g_{m1}\left(r_{o1} \| r_{o2}\right)}$$

Summary 1

Summary of CMOS Inverting Amplifiers

Inverter	AC Voltage Gain	AC Output Resistance	Bandwidth (CGB=0)
p-channel active load inverter	$\frac{-gm1}{gm2}$	$\frac{1}{gm2}$	$\frac{gm2}{CBD1+CGS1+CGS2+CBD2}$
n-channel active load inverter	$\frac{-gm1}{gm2+gmb2}$	$\frac{1}{gm2+gmb2}$	$\frac{gm2+gmb2}{CBD1+CGD1+CGS2+CBS2}$
Current source load inverter	$\frac{-gm1}{gds1+gds2}$	$\frac{1}{gds1+gds2}$	$\frac{gds1+gds2}{CBD1+CGD1+CDG2+CBD2}$
n-channel depletion load inverter	$\sim\frac{-gm1}{gmb2}$	$\frac{1}{gmb2+gds1+gds2}$	$\frac{gmb2+gds1+gds2}{CBD1+CGD1+CGS2+CBD2}$
Push-Pull inverter	$\frac{-(gm1+gm2)}{gds1+gds2}$	$\frac{1}{gds1+gds2}$	$\frac{gds1+gds2}{CBD1+CGD1+CGS2+CBD2}$



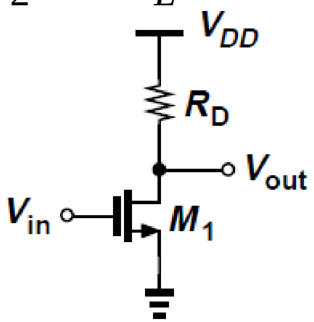
Summary 2

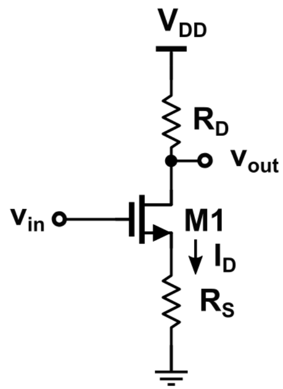
	CS - R	CS - Diode	CS Biased
DC gain			↑
Output Swing		↑	
Input Swing	↑	↑	
Area (large passive R)		↑	↑
Bandwidth -3dB		↑	
Bandwidth GBW	↑	↑	↑

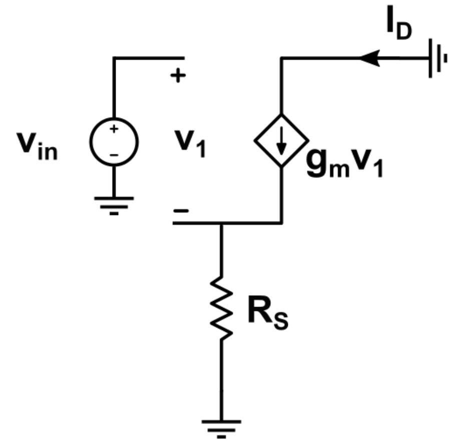
CS Stage with Source Degeneration

- Nonlinearity of circuit is due to nonlinear dependence of I_D upon V_{ON}

$$I_{DS} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{in} - V_{TH}\right)^2$$







$$A_v = -\mu_n C_{ox}\frac{W}{L}\left(V_{in} - V_{TH}\right)R_D = g_m R_D$$

$$V_{in} = V_{GS} + I_D R_S$$

$$V_{out} = V_{DD} - I_D R_D$$

$$A_v = ?$$

- R_S in series with the source -> input device more linear
  - As V_{in} increases, so do I_D and the voltage drop across R_S

    Part of the change in V_{in} appears across R_S rather than gate-source overdrive, making variation in I_D smoother
  - <u>**Gain is now a weaker function of g_m**</u>

Large-signal Analysis

$$V_{out} = V_{DD} - I_D R_D \qquad A_V = \frac{\partial V_{out}}{\partial V_{in}} = -\frac{\partial I_D}{\partial V_{in}} \times R_D$$

Define $G_m = -\dfrac{\partial I_D}{\partial V_{in}} \Rightarrow A_V = -G_m \times R_D$

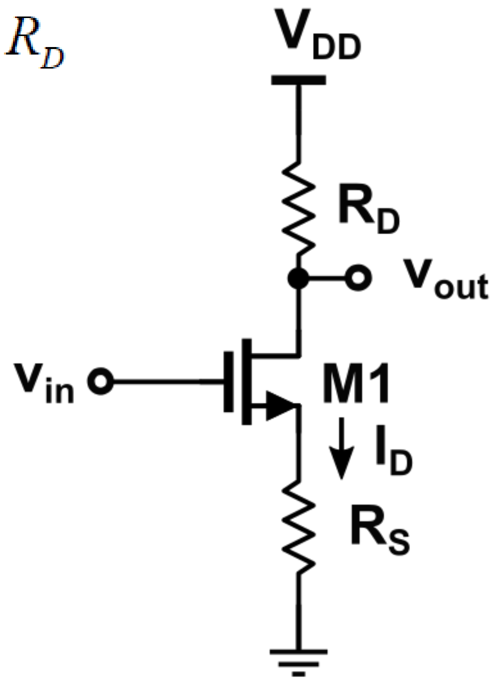
$$G_m = -\frac{\partial I_D}{\partial V_{in}} = -\frac{\partial I_D}{\partial V_{GS}}\frac{\partial V_{GS}}{\partial V_{in}} = -g_m \frac{\partial V_{GS}}{\partial V_{in}}$$

$$\because V_{in} = V_{GS} + I_D \times R_S$$

$$\frac{\partial V_{in}}{\partial V_{GS}} = 1 + \frac{\partial I_D}{\partial V_{GS}} \times R_S = 1 + g_m \times R_S$$

$$\therefore G_m = -g_m \frac{1}{1+g_m R_s} = -\frac{1}{\dfrac{1}{g_m} + R_S} \qquad R_s \uparrow \Rightarrow G_m \downarrow$$

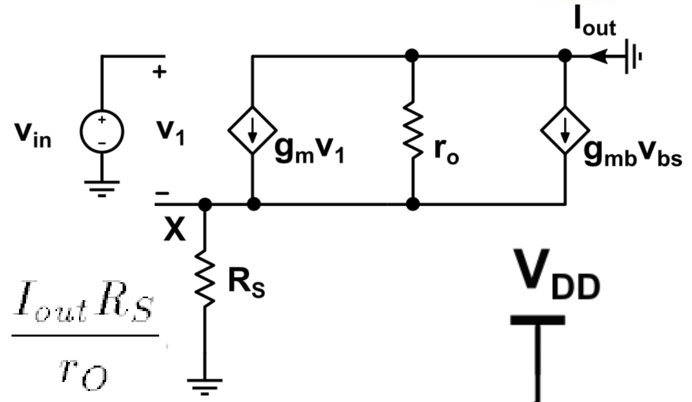
$$R_s >> 1/g_m \Rightarrow \Delta I_D = \frac{\Delta V_{in}}{R_S} \Rightarrow G_m = \frac{1}{R_s}$$



Trade-off

- **The cost of linearization: lower gain, lower swing**

Small-signal Analysis

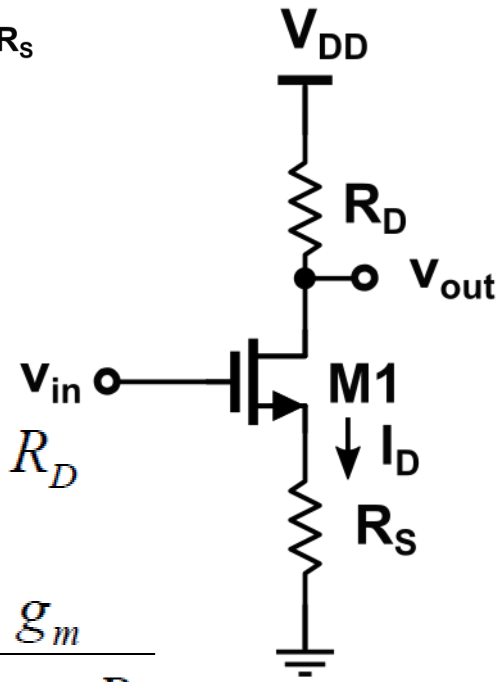


$$V_{in} = V_1 + I_{out} R_S$$

$$I_{out} = g_m V_1 - g_{mb} V_X - \frac{I_{out} R_S}{r_O}$$

$$= g_m (V_{in} - I_{out} R_S) + g_{mb}(-I_{out} R_S) - \frac{I_{out} R_S}{r_O}$$

$$G_m = \frac{I_{out}}{V_{in}} = \frac{g_m r_O}{R_S + [1 + (g_m + g_{mb}) R_S] r_O}$$



$$A_V = -G_m \times R_D = -\frac{g_m r_o}{R_s + [1 + (g_m + g_{mb}) R_s] r_o} R_D$$

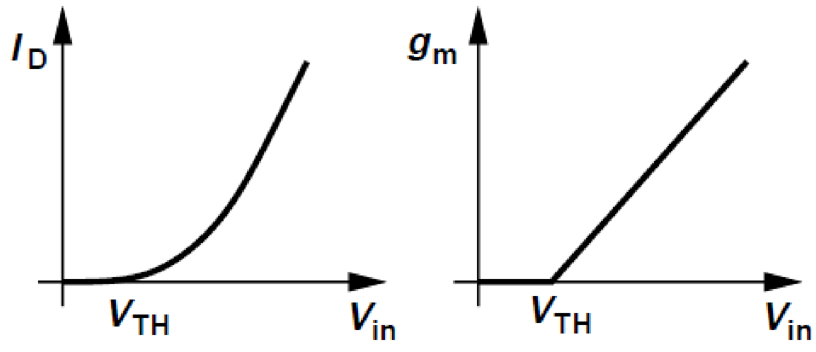
When $r_O >> R_S$, $A_V \approx -\dfrac{g_m}{1 + g_m R_s} R_D \qquad G_m = -\dfrac{g_m}{1 + g_m R_s}$

Small-signal Analysis

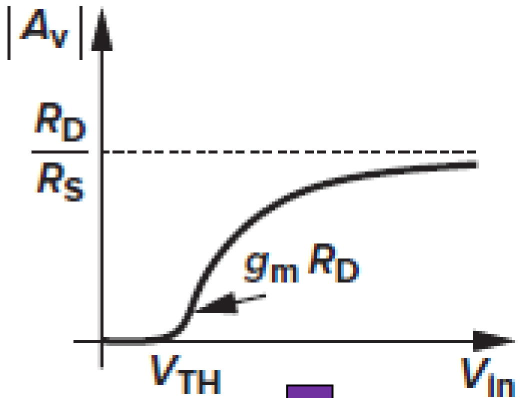
$$A_V = -G_m \times R_D = -\frac{g_m r_o}{R_s + [1 + (g_m + g_{mb})R_s] r_o} R_D \approx -\frac{g_m}{1 + g_m R_s} R_D$$

(1) R_S=0

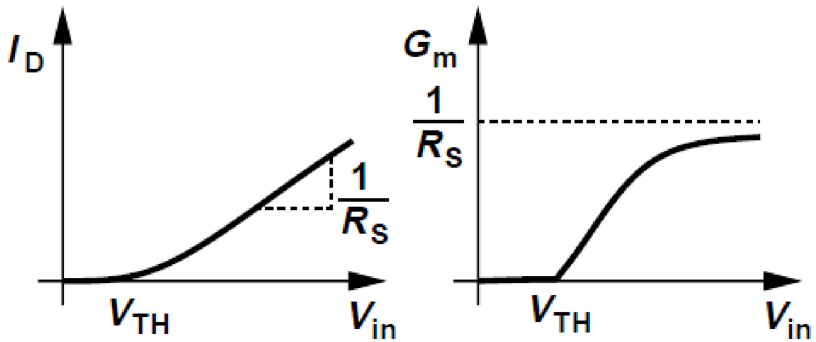
I_D and g_m vary with V_{in}



$$A_v = -g_{m1} R_D$$

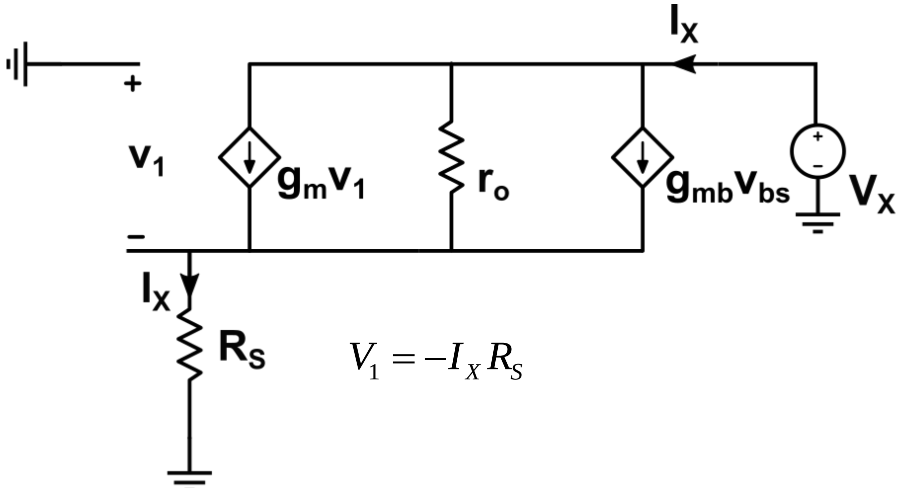


(2)R_S≠0



- V_{in} slightly great than V_{TH}, M1 is on,
- $1/g_m >> R_S$ $G_m \approx g_m$
- $V_{in} \uparrow$, $G_m = -\frac{g_m}{1 + g_m R_s}$
- V_{in} is very large, $R_S >> 1/g_m$ => $G_m = \frac{1}{R_s}$
- if $V_{in} > V_{out} - V_{TH}$, linear region, Av ↓

Output Resistance



$$V_1 = -I_X R_S$$

$$I_X - (g_m + g_{mb}) V_1 = I_X + (g_m + g_{mb}) R_S I_X$$

KVL: $r_O \left[I_X + (g_m + g_{mb}) R_S I_X \right] + R_S I_X = V_X$

$$R_{out} = \frac{V_X}{I_X} = \left[1 + (g_m + g_{mb}) R_S \right] r_O + R_S$$

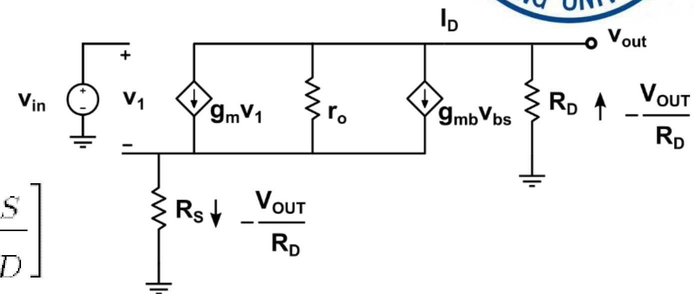
$$= \left[1 + (g_m + g_{mb}) r_O \right] R_S + r_O$$

$$= r_O + R_S + (g_m + g_{mb}) R_S r_O$$

- r_O is boosted by a factor of $1+(g_m+g_{mb})R_S$, then added R_S
- R_S is boosted by a factor of $1+(g_m+g_{mb})\, r_O$, then added r_O
- $if\,(g_m + g_{mb}) r_O > 1$ $\quad R_{out} \approx \left[1 + (g_m + g_{mb}) R_S \right] r_O \approx g_m R_S r_O$

- Compare $R_S = 0$ with $R_S > 0$
- If $R_S = 0$, $g_m V_1 = g_{mb} V_{bs} = 0$ and $I_X = V_X / r_O$
- If $R_S > 0$, $I_X R_S > 0$ and $V_1 < 0$, obtaining negative $g_m V_1$ and $g_{mb} V_{bs}$
- Thus, current supplied by V_X is less than V_X/r_o and hence output impedance is greater than r_o

Small signal model of degenerated CS with finite output resistance



$$V_1 = V_{in} + V_{out} R_S / R_D$$

$$\begin{aligned} I_{ro} &= -\frac{V_{out}}{R_D} - (g_m V_1 + g_{mb} V_{bs}) \\ &= -\frac{V_{out}}{R_D} - \left[g_m \left(V_{in} + V_{out}\frac{R_S}{R_D} \right) + g_{mb} V_{out} \frac{R_S}{R_D} \right] \end{aligned}$$

- Since voltage drops across r_O and R_S must add up to V_{out},

$$\begin{aligned} V_{out} &= I_{ro} r_O - \frac{V_{out}}{R_D} R_S \\ &= -\frac{V_{out}}{R_D} r_O - \left[g_m \left(V_{in} + V_{out}\frac{R_S}{R_D} \right) + g_{mb} V_{out} \frac{R_S}{R_D} \right] r_O - V_{out}\frac{R_S}{R_D} \end{aligned}$$

- voltage gain is therefore

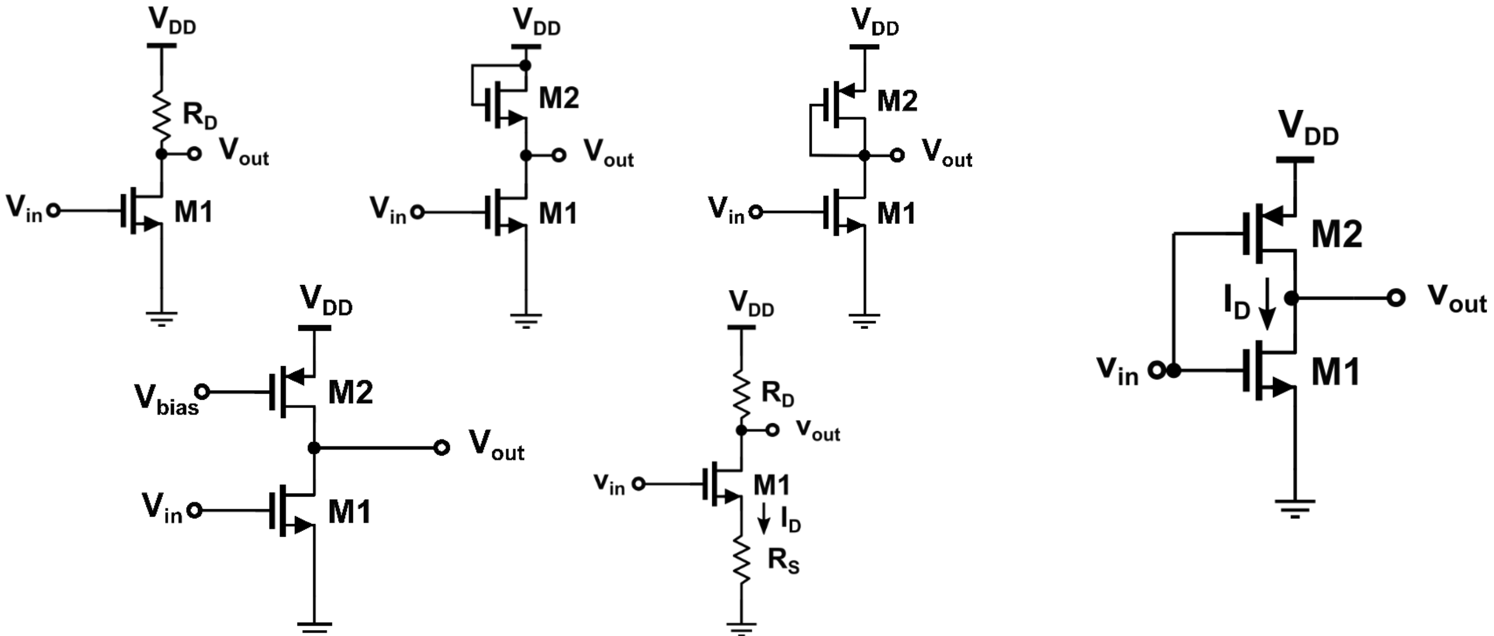
$$\boxed{\frac{V_{out}}{V_{in}} = \frac{-g_m r_O R_D}{R_D + R_S + r_O + (g_m + g_{mb}) R_S r_O}}$$

$$A_V = -\frac{g_m r_o}{R_s + [1 + (g_m + g_{mb}) R_s] r_o} \frac{R_D \{ R_s + [1 + (g_m + g_{mb}) R_s] r_o \}}{R_D + R_s + [1 + (g_m + g_{mb}) R_s] r_o} = -G_m R_{out}$$

- G_m: the transconductance when the output is shorted to ground
- R_{out}: the output resistance when the input voltage is set to zero

Summary

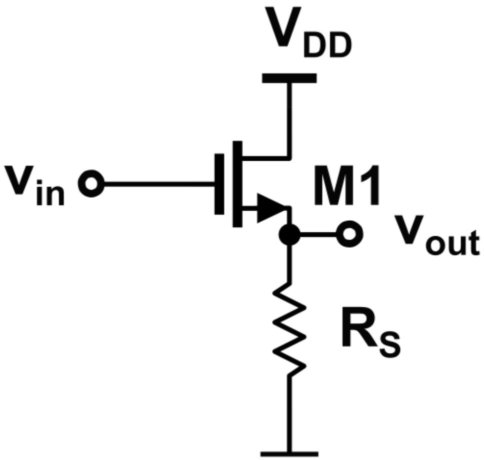
- Two kinds of analysis method: **large-signal analysis** and **small-signal analysis**
- Small-signal analysis
  - Small-signal equivalent circuits
  - Based on the equivalent circuits, deduct the gain, the output impedance, …
- The main structures of common-source amplifier:



Outline

- General Consideration
- Common-Source Stage
  - CS Stage with Resistive Load
  - CS Stage with Diode-Connected Load
  - CS Stage with Current-Source Load
  - CS Stage with Source Degeneration
- Source Follower
- Common-Gate Stage

Source follower



- ☐ Input voltage: V_{GD}
- ☐ Output voltage: V_{SD}

Via Gm

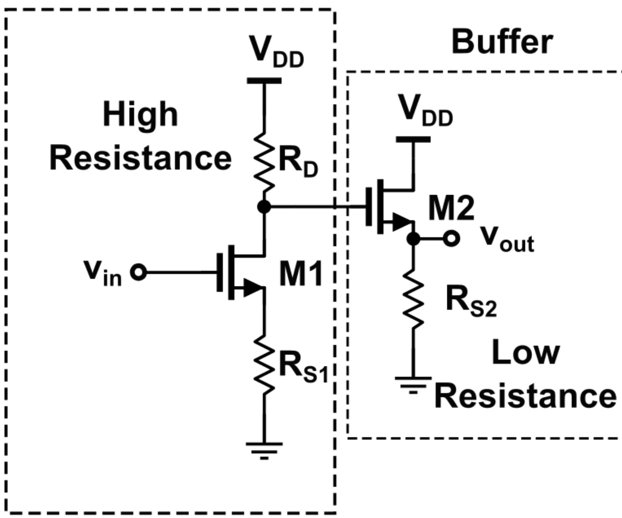
Main Features:

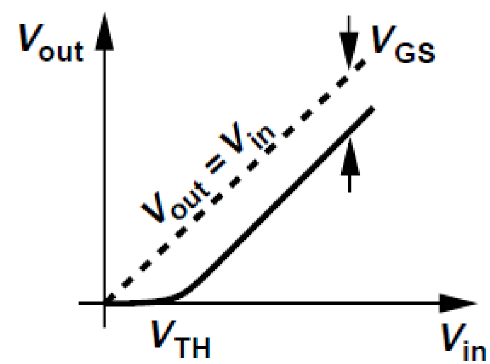
- ☐ High input impedance
- ☐ **Low output impedance**
- ☐ Allowing the "source" potential to follow the "gate" voltage ⟹ $A_V \leq 1$,

  Voltage buffer -> Level shifter

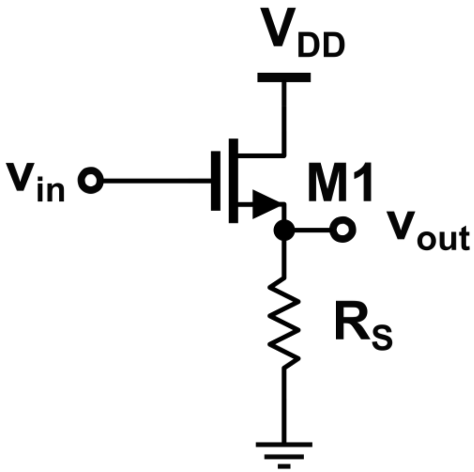
Gain Stage

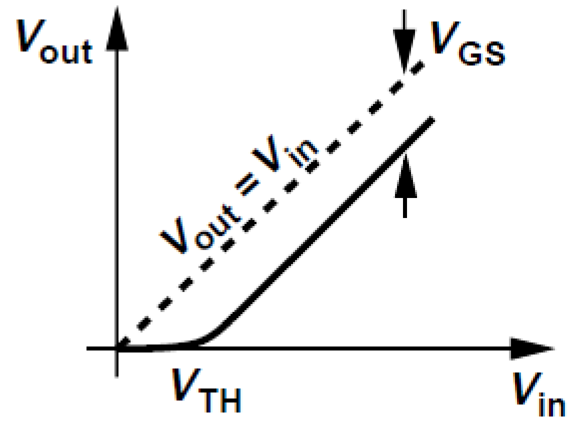
Buffer





Large-signal analysis





- $V_{in} < V_{TH}$: M_1 is off and $V_{out} = 0$
- $V_{in} > V_{TH}$: M_1 turns on in saturation

  $V_{DS} = V_{DD}$ and $V_{GS} - V_{TH} \approx 0$ and I_{D1} flows through R_S
- V_{in} increases further: $V_{out} = V_{in} - V_{GS}$ (**level shifter**)

$$\frac{1}{2}\mu_n C_{OX}\frac{W}{L}\left(V_{in}-V_{TH}-V_{out}\right)^2 R_S = V_{out}$$

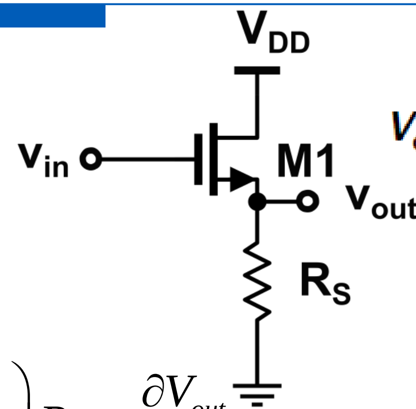
neglecting channel-length modulation

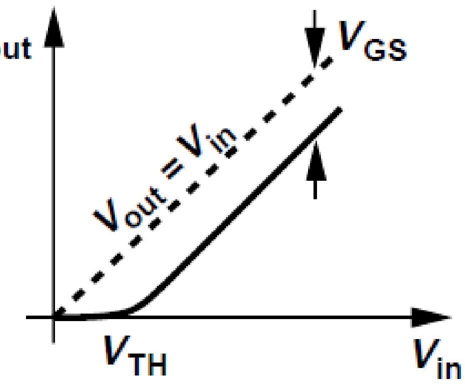
Body effect?

Large-signal analysis

neglecting channel-length modulation

$$\frac{1}{2}\mu_n C_{OX}\frac{W}{L}\left(V_{in}-V_{TH}-V_{out}\right)^2 R_S=V_{out}$$



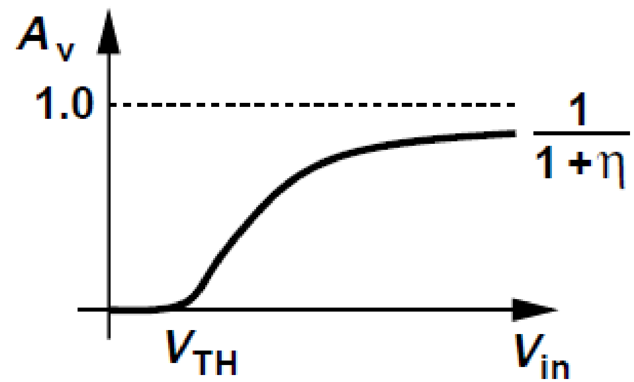


differentiating both sides:

$$\frac{1}{2}\mu_n C_{OX}\frac{W}{L}2\left(V_{in}-V_{TH}-V_{out}\right)\left(1-\frac{\partial V_{TH}}{\partial V_{in}}-\frac{\partial V_{out}}{\partial V_{in}}\right)R_S=\frac{\partial V_{out}}{\partial V_{in}}$$

$$\because \frac{\partial V_{TH}}{\partial V_{in}}=\frac{\partial V_{TH}}{\partial V_{SB}}\frac{\partial V_{SB}}{\partial V_{in}}=\eta\frac{\partial V_{out}}{\partial V_{in}} \qquad g_m=\mu_n C_{ox}\frac{W}{L}\left(V_{in}-V_{TH}-V_{out}\right)$$

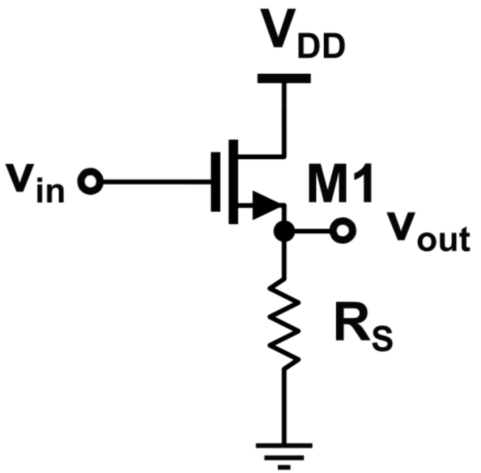
$$\therefore \frac{\partial V_{out}}{\partial V_{in}}=\frac{\mu_n C_{ox}\frac{W}{L}\left(V_{in}-V_{TH}-V_{out}\right)R_S}{1+\mu_n C_{ox}\frac{W}{L}\left(V_{in}-V_{TH}-V_{out}\right)R_S\left(1+\eta\right)}$$



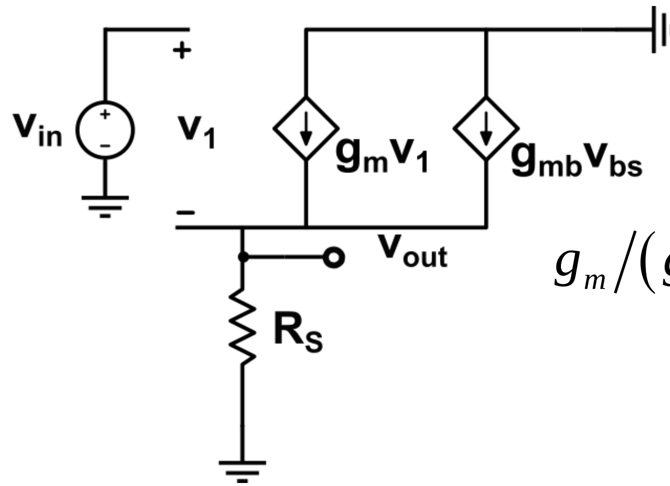
$$\boxed{A_v=\frac{\partial V_{out}}{\partial V_{in}}=\frac{g_m R_S}{1+\left(g_m+g_{mb}\right)R_S}}=\frac{g_m}{\frac{1}{R_S}+g_m+g_{mb}}$$

Small-signal analysis

A. Voltage Gain



neglecting channel-length modulation



$$g_m/(g_m+g_{mb})=1/(1+\eta)$$

$$KVL: V_{in}-V_1=V_{out}, \quad V_{bs}=-V_{out}$$

$$KCL: g_m V_1-g_{mb}V_{out}=V_{out}/R_S$$

$$\boxed{A_v=\frac{\partial V_{out}}{\partial V_{in}}=\frac{g_m R_S}{1+(g_m+g_{mb})R_S}}$$

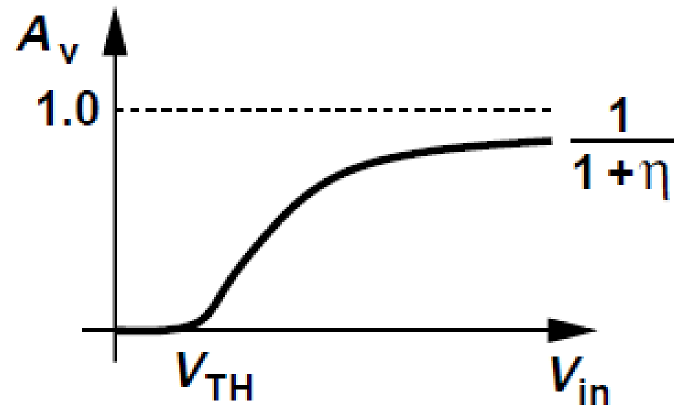
From feedback system point of view

Small-signal analysis

- **Nonlinear of Gain**

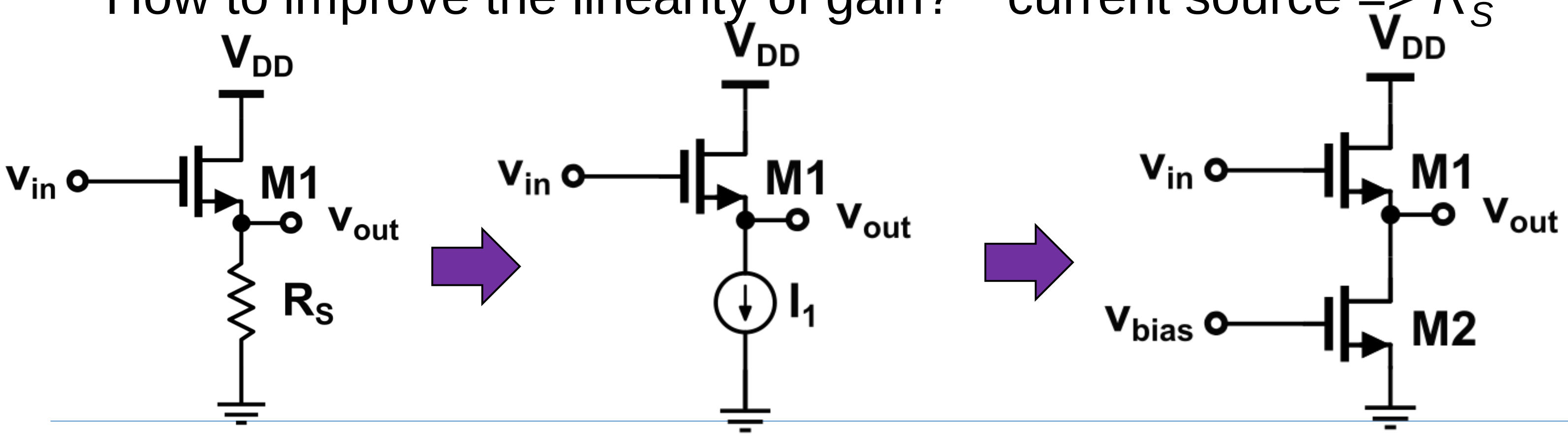
$$A_v = \frac{g_m R_S}{1+(g_m+g_{mb})R_S}$$

$$= \frac{1}{\frac{1}{g_m R_s}+\left(1+\frac{g_{mb}}{g_m}\right)} \approx \frac{1}{1+\eta} \le 1$$



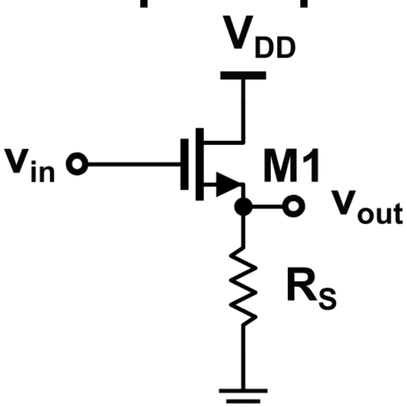
- For typical V_{SB}, η ~ 0.2
- Even if $R_S = \infty$, A_v is not equal to 1

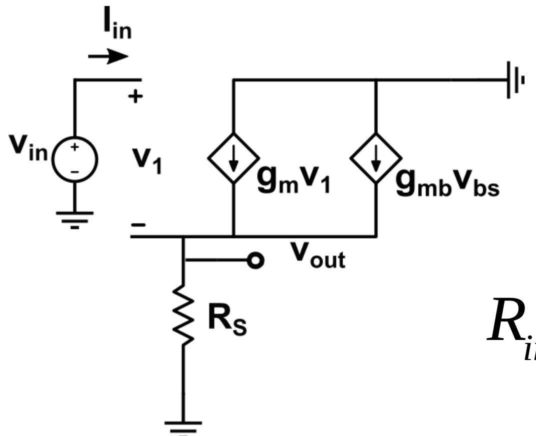
How to improve the linearity of gain? current source => R_S



Small-signal analysis

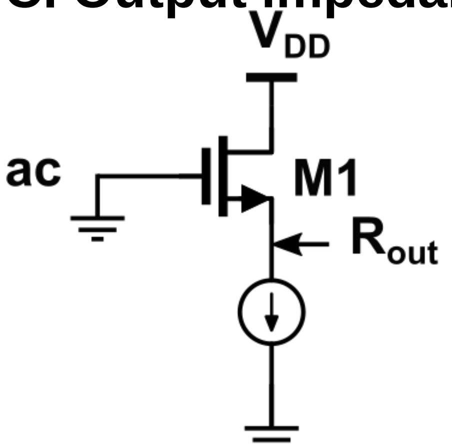
B. Input impedance

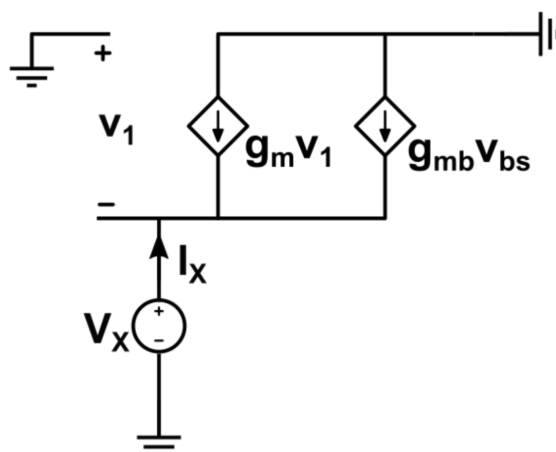




$$R_{in} = \frac{V_{in}}{I_{in}} \rightarrow \infty \quad \text{(in low frequency)}$$

C. Output impedance





$$V_1 = -V_X$$

$$I_X - g_m V_X - g_{mb} V_X = 0$$

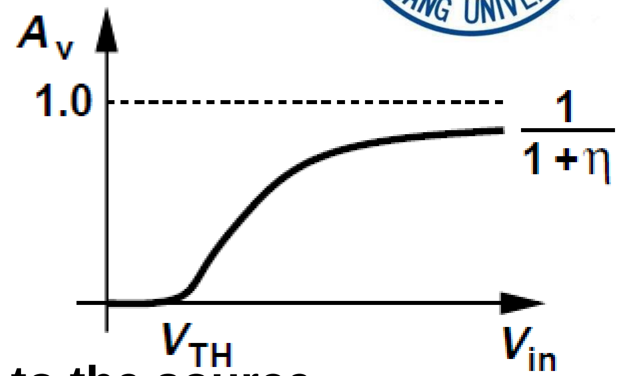
$$R_{out} = \frac{1}{g_m + g_{mb}} = \frac{1}{g_m} \bigg\| \frac{1}{g_{mb}}$$

- Body effect ***decreases*** R_{out} of SF

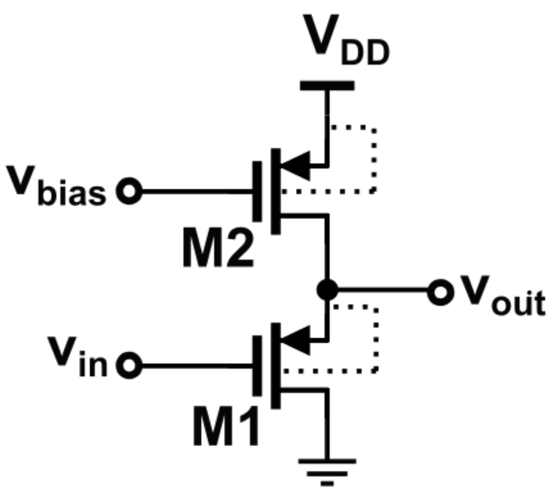
High input impedance =>Low output impedance

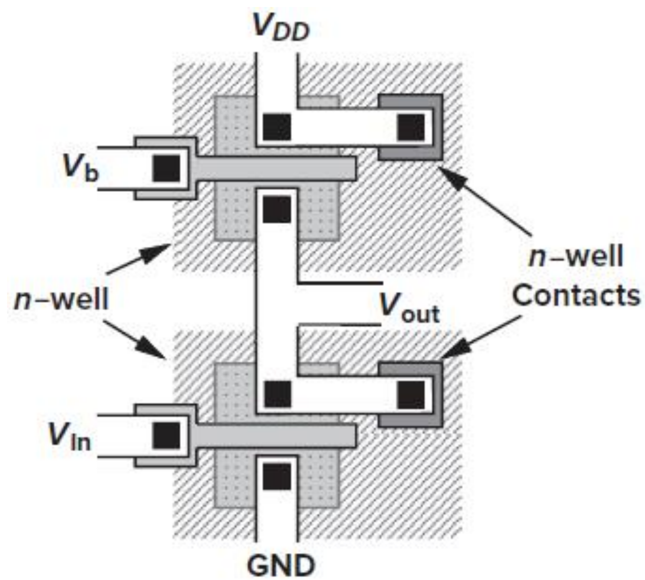
Issues with Source follower

- **Drawback 1: Nonlinearity**
  - Nonlinear **dependence** of V_{TH} on the **source potential** **(body effect)**
  - r_O changes substantially with V_{DS}



- Nonlinearity can be eliminated if the **bulk is tied to the source**
- Lower mobility of PFETs yields a higher output impedance than that available in the NMOS counterpart

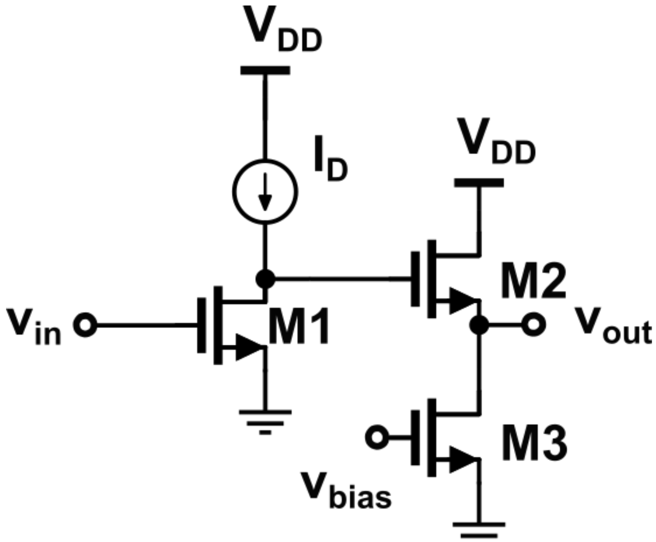




*Possible only for PFETs since all NFETs usually share the same substrate -> **DNW***

Issues with Source follower

- **Drawback 2: Voltage headroom limitation**
  - Source followers shift the DC level of V_{GS}, thereby **consuming voltage headroom**



CS stage + Source follower

M_1 in saturation:

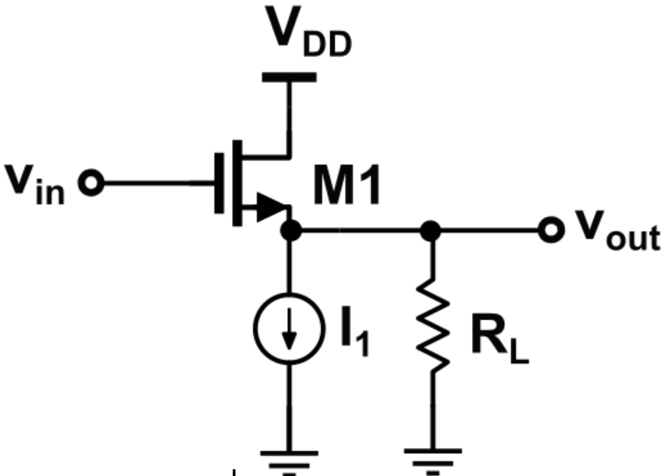
V_X (min) $> V_{GS1} - V_{TH1}$

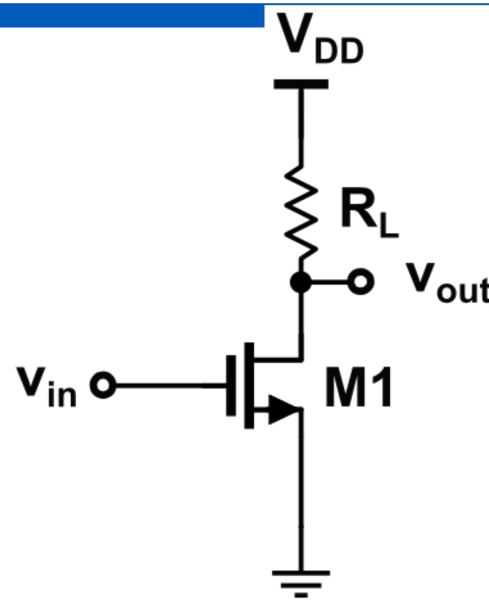
M_2 M_3 : in saturation

V_X (min) $> V_{GS2} + (V_{GS3} - V_{TH3})$

  - **A DC level of V_{GS2}**
  - The voltage **swing is decreased**

Comparison of SF and CS with low load





$$R_L = 50\Omega$$

$$\left.\frac{V_{out}}{V_{in}}\right|_{SF} \approx \frac{R_L}{R_L + 1/g_m}$$

if $R_L = 1/g_m$

$$\left.\frac{V_{out}}{V_{in}}\right|_{SF} = \frac{R_L}{R_L + 1/g_m} = 0.5 \qquad \left.\frac{V_{out}}{V_{in}}\right|_{CS} = -g_m R_L \approx 1$$

Source followers are not necessarily efficient drivers

Frequency behavior

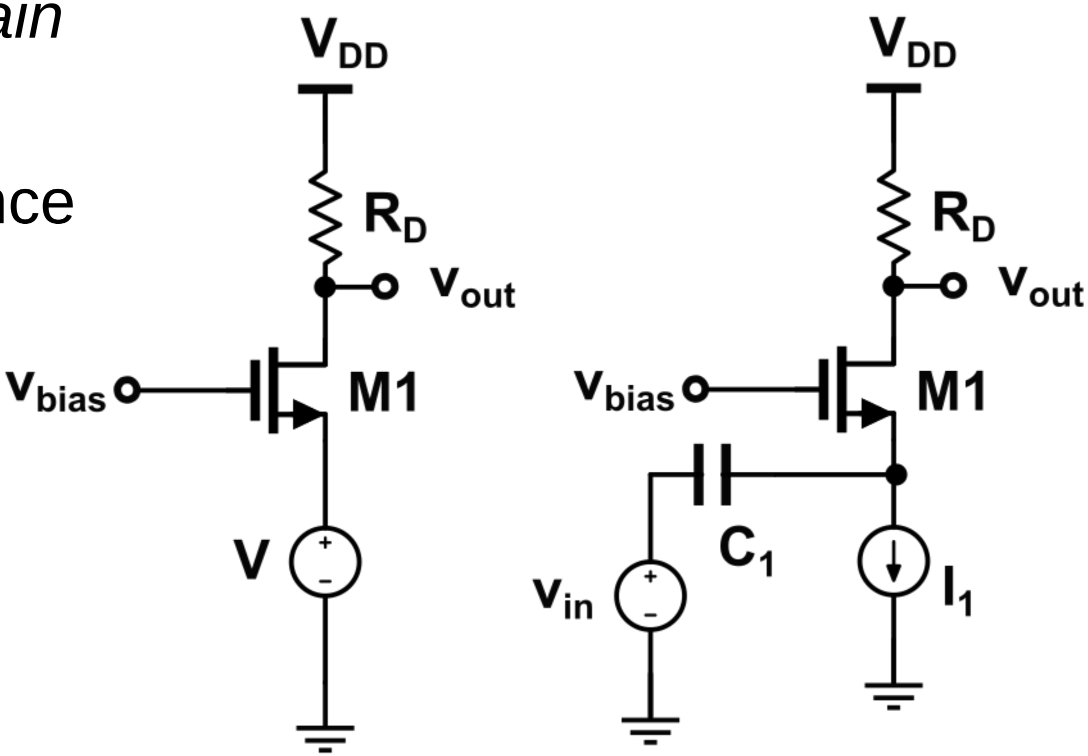
- SF can provide some phase lead
- Rs -> Rs // 1/sCs

Outline

- General Consideration
- Common-Source Stage
  - CS Stage with Resistive Load
  - CS Stage with Diode-Connected Load
  - CS Stage with Current-Source Load
  - CS Stage with Source Degeneration
- Source Follower
- Common-Gate Stage

Common-Gate Stage

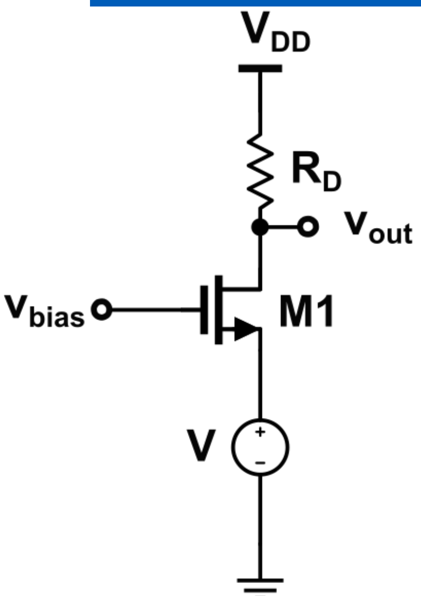
- Input voltage: *source*
- Output voltage: *drain*
- **Current buffer**
- Low input impedance



Via Gm

$I_{in} = I_{out}$

Large-signal analysis



Assume V_{in} decreases from a large positive value and $\lambda=0$

1) $V_{in} \geq V_b - V_{TH}$: M_1 is off, $V_{out} = V_{DD}$

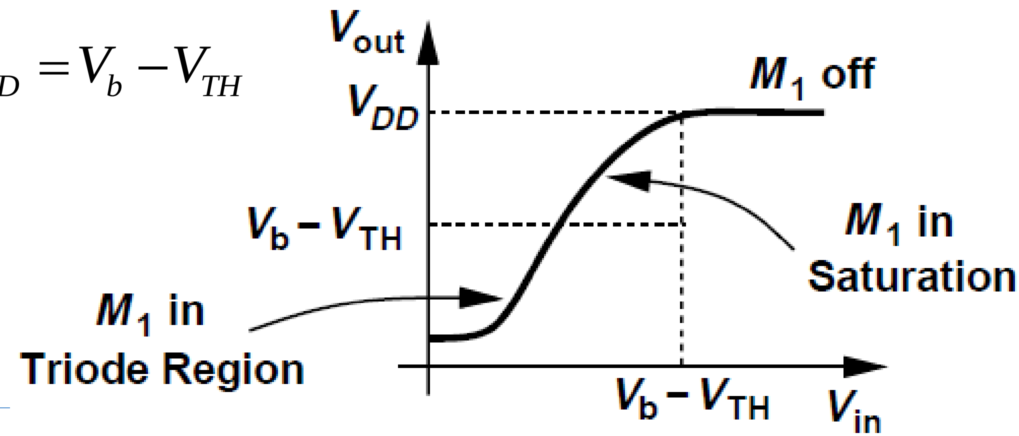
2) For lower V_{in}, M_1: in saturation $I_D \uparrow, \ V_{out} \downarrow$

$$I_D = \frac{1}{2}\mu_n C_{OX}\frac{W}{L}(V_b - V_{in} - V_{TH})^2$$

$$V_{out} = V_{DD} - \frac{1}{2}\mu_n C_{OX}\frac{W}{L}(V_b - V_{in} - V_{TH})^2 R_D$$

3) As V_{in} decreases further, $V_{GS1} \uparrow \Rightarrow I_D \uparrow, \ V_{out} \downarrow$, M_1 : the triode region

$$V_{DD} - \frac{1}{2}\mu_n C_{OX}\frac{W}{L}(V_b - V_{in} - V_{TH})^2 R_D = V_b - V_{TH}$$



A. Input-output Characteristics

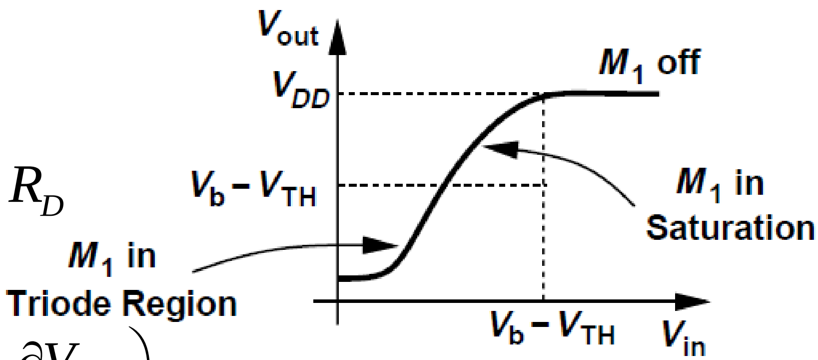
Large-signal analysis

B. Gain

- For M_1 in saturation,

$$V_{out} = V_{DD} - \frac{1}{2}\mu_n C_{OX}\frac{W}{L}\left(V_b - V_{in} - V_{TH}\right)^2 R_D$$

$$\frac{\partial V_{out}}{\partial V_{in}} = -\mu_n C_{OX}\frac{W}{L}\left(V_b - V_{in} - V_{TH}\right)\left(-1 - \frac{\partial V_{TH}}{\partial V_{in}}\right)R_D$$



$$\because \frac{\partial V_{TH}}{\partial V_{in}} = \frac{\partial V_{TH}}{\partial V_{SB}} = \eta$$

$$\therefore \frac{\partial V_{out}}{\partial V_{in}} = \mu_n C_{OX}\frac{W}{L}\left(V_b - V_{in} - V_{TH}\right)R_D\left(1+\eta\right) = g_m\left(1+\eta\right)R_D$$

! positive

- ☐ Body effect increases the effective g_m
- ☐ For a given bias current and supply voltage, A_V can be maximized by
  - -- Increasing g_m by widening the input device
  - -- Increasing R_D
- ☐ V_{out} (min)=V_{GS}-V_{TH}+V_{I1}, where V_{I1} denotes the minimum voltage required by I_1

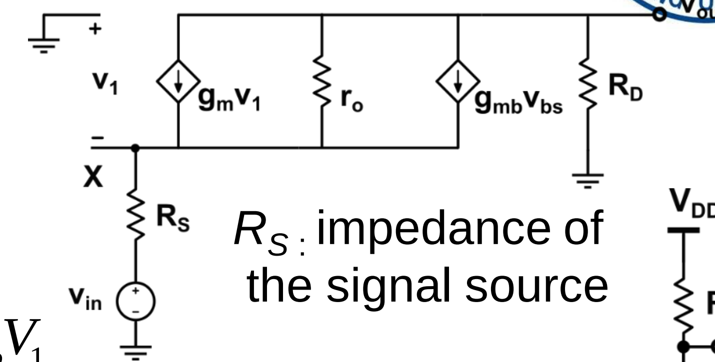
Small-signal analysis

A. Gain

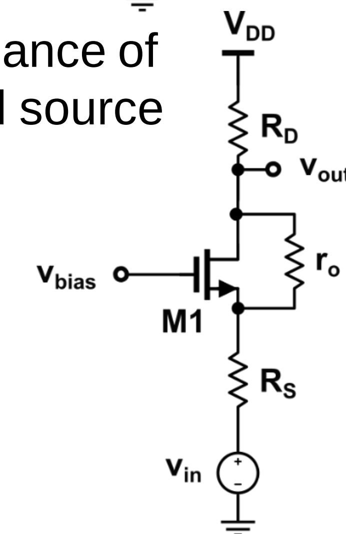
Current through R_S: $-V_{out}/R_D$,

$$V_1 - \frac{V_{out}}{R_D}R_S + V_{in} = 0$$

Current through r_O: $-V_{out}/R_D - g_m V_1 - g_{mb} V_1$



R_S : impedance of the signal source



KVL:

$$r_O\left(-V_{out}/R_D - g_m V_1 - g_{mb} V_1\right) - \frac{V_{out}}{R_D}R_S + V_{in} = V_{out}$$

$$r_O\left[-\frac{V_{out}}{R_D} - \left(g_m + g_{mb}\right)\left(V_{out}\frac{R_S}{R_D} - V_{in}\right)\right] - \frac{V_{out}}{R_D}R_S + V_{in} = V_{out}$$

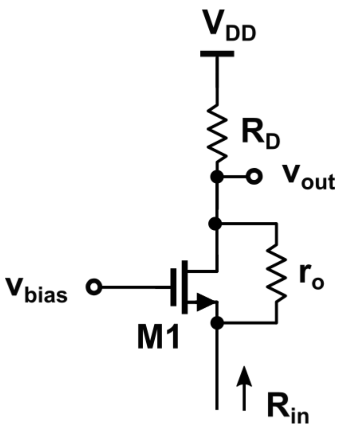
$$\frac{V_{out}}{V_{in}} = \frac{\left(g_m + g_{mb}\right)r_O + 1}{r_O + \left(g_m + g_{mb}\right)r_O R_S + R_S + R_D}R_D$$

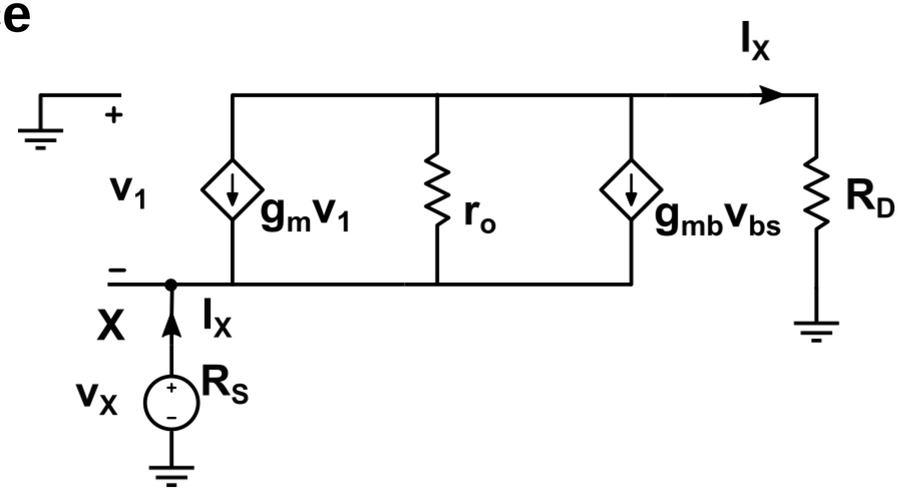
Be similar to that of a degenerated CS stage

Via Gm: ***Input resistance = 1/Gm*** ***$I_{in} = I_{out}$***

Small-signal Performance

B. Input impedance





$$V_1 = -V_X$$

Current through r_O : $I_X + g_m V_1 + g_{mb} V_1 = I_X - (g_m + g_{mb}) V_X$, So

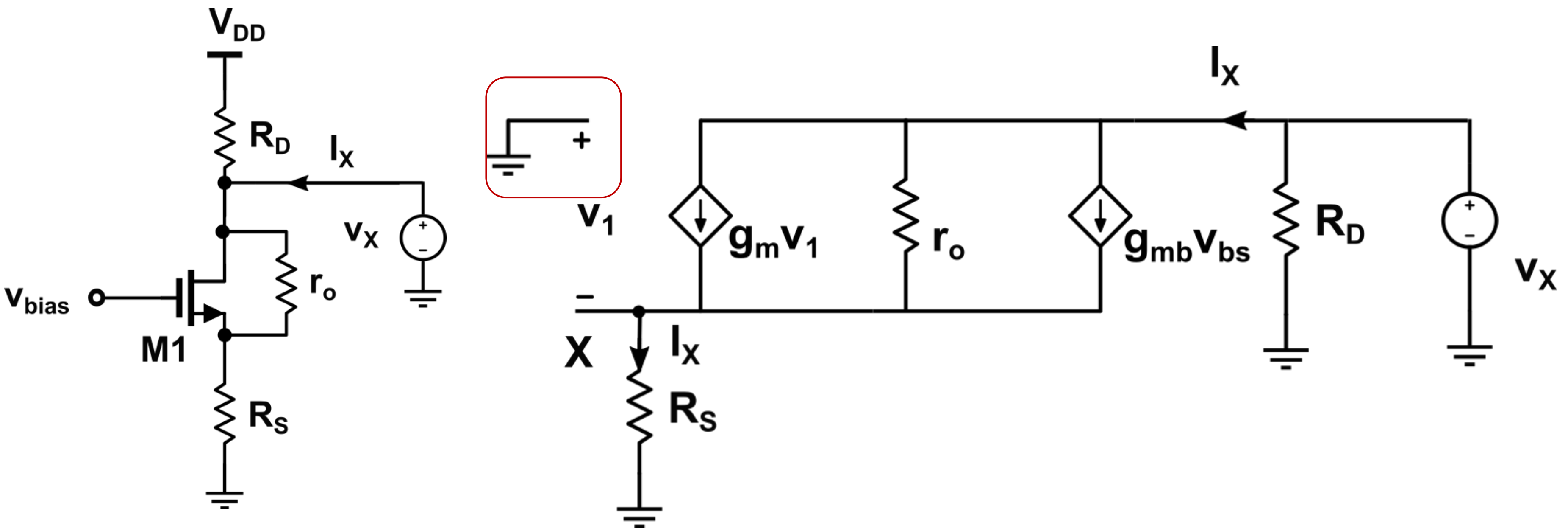
$$R_D I_X + r_O \left[I_X - \left(g_m + g_{mb} \right) V_X \right] = V_X$$

$$\frac{V_X}{I_X} = \frac{R_D + r_O}{1 + \left(g_m + g_{mb} \right) r_O} = \frac{1}{g_O + g_m + g_{mb}} \left(1 + \frac{R_D}{r_O} \right)$$

$$\approx \frac{R_D}{\left(g_m + g_{mb} \right) r_O} + \frac{1}{\left(g_m + g_{mb} \right)}$$

if $(g_m + g_{mb}) r_O >> 1$

Output impedance



$$R_{out} = \left\{\left[1+\left(g_m + g_{mb}\right)R_S\right]r_O + R_S\right\} // R_D \approx \left(g_m R_S r_O\right) // R_D$$

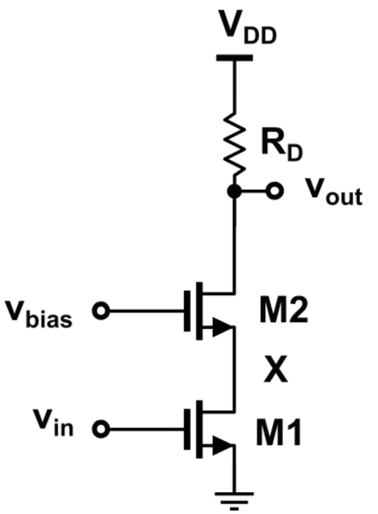
- *Be similar to that of a degenerated CS stage*
- *When Calculate Zout, short the input !!*

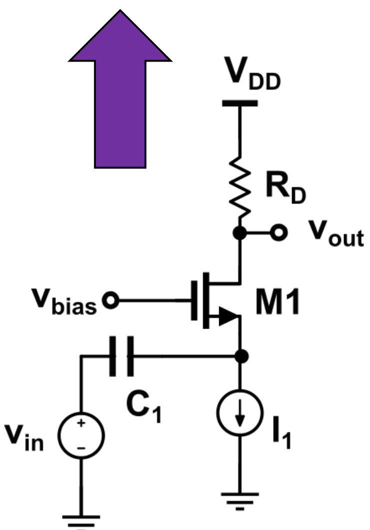
Outline

- General Consideration
- Common-Source Stage
  - CS Stage with Resistive Load
  - CS Stage with Diode-Connected Load
  - CS Stage with Current-Source Load
  - CS Stage with Source Degeneration
- Source Follower
- Common-Gate Stage

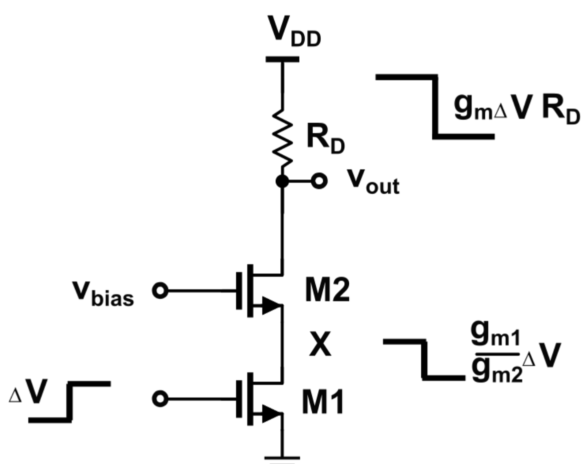
Combination of all above

Cascode Stage





- **CS stage + CG stage**
- M_1 : the input device $\quad V_{in} \text{->} I_1 = g_{m1}V_{in}$
- M_2 : the cascode device, routing the current to R_D $\quad I_1 = I_2$
- $V_{out} = V_{DD} - I_2 R_D$
- **telescopic cascode**



M_1, M_2 : in saturation $\quad \lambda = \gamma = 0$

- V_{in}: ΔV ➡ I_{D1}: $g_{m1}\Delta V$
- V_X falls $g_{m1}\Delta V\cdot(1/g_{m2})$
- V_{out}: $g_{m1}\Delta V R_D$ as in a simple CS stage

Bias Conditions

M_1, M_2 : in saturation

- M_1 : in saturation, $V_X \geq V_{in} - V_{TH1}$

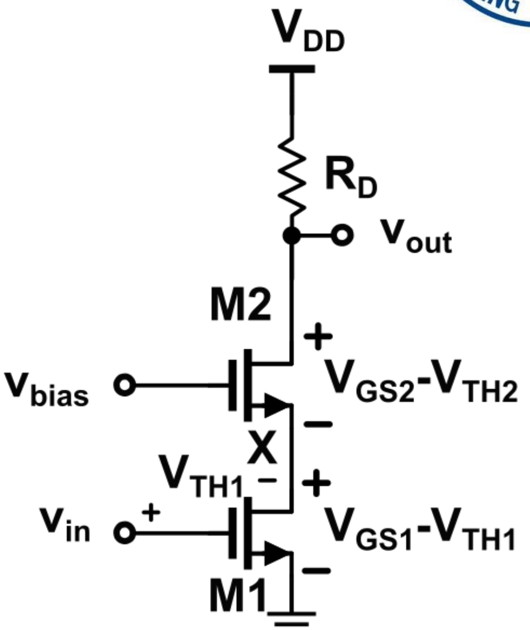
  If M_1 and M_2: both in saturation

  --M_2 operates as a source follower

  --V_X is determined by V_b: $V_X = V_b - V_{GS2}$

  $\Rightarrow$ $V_b - V_{GS2} \geq V_{in} - V_{TH1}$

  so $V_b \geq V_{GS2} + V_{in} - V_{TH1}$



- M_2: in saturation, $V_{out} \geq V_b - V_{TH2}$

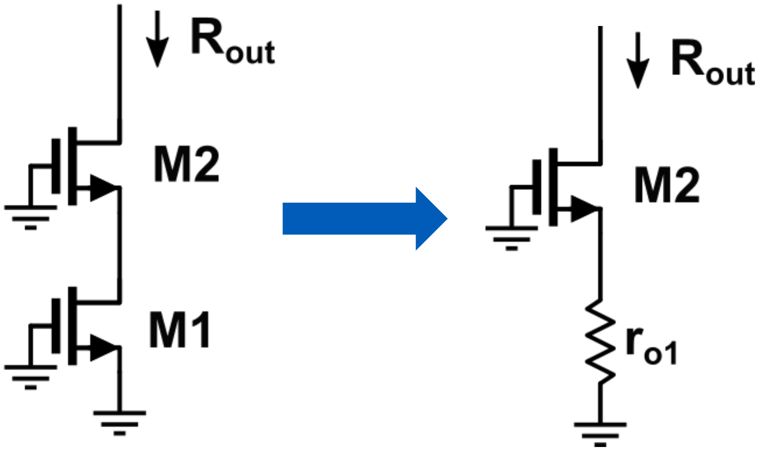
  if V_b is chosen to place M_1 at the edge of saturation

  $$V_{out} \geq V_{in} + V_{GS2} - V_{TH2} - V_{TH1} = (V_{GS1} - V_{TH1}) + (V_{GS2} - V_{TH2})$$

- Minimum output: $V_{ov1} + V_{ov2} \approx 2V_{ov}$ ~ 0.4-0.6V

  Reduce the output voltage swing (at least V_{ov})

Output Impedance



high output impedance!

- A common-source stage with a degeneration resistor (r_{O1})

$$R_{out} = \left[1 + \left(g_{m2} + g_{mb2}\right) r_{O2}\right] r_{O1} + r_{O2}$$

$$\approx \left(g_{m2} + g_{mb2}\right) r_{O2} r_{O1}$$

assuming $g_m r_O >> 1$,

- M2 boosts the output impedance of M1 by a factor of $(g_{m2}+g_{mb2})r_{O2}$

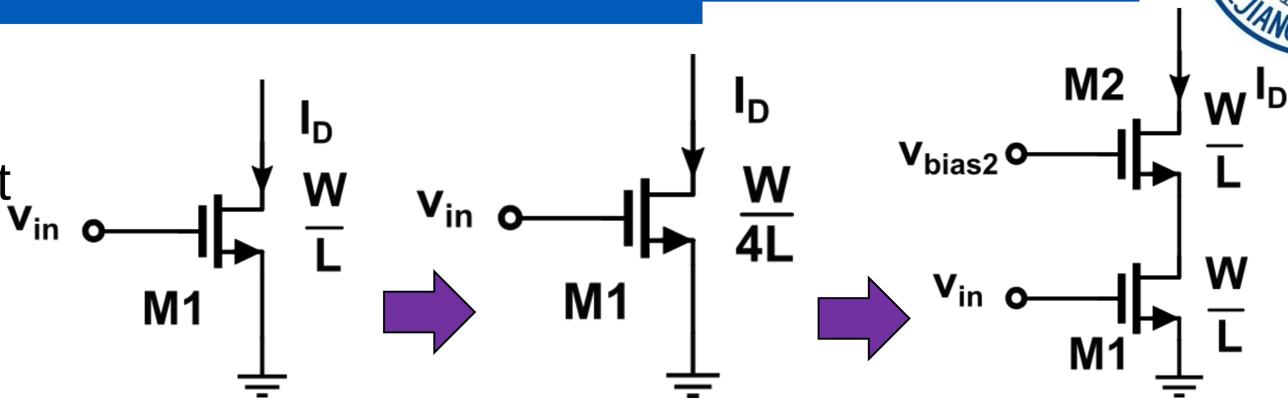
$$A_v = -G_m R_{out}$$

$$= -g_{m1}\left[r_{O1} + r_{O2} + \left(g_{m2} + g_{mb2}\right) r_{O1} r_{O2}\right]$$

$$\approx g_{m1} g_{m2} r_{O1} r_{O2} \approx \left(g_m r_O\right)^2$$

How to get high voltage gain?

I_D: constant



A. Increasing length of the input transistor

r_o: double

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{GS} - V_{TH}\right)^2$$

V_{ov}: double, Swing ↓

$$g_m r_o = \sqrt{2\mu_n C_{ox}\frac{W}{L}I_D}\,\frac{1}{\lambda I_D}, \lambda \propto \frac{1}{L} \Rightarrow g_m r_o \propto \sqrt{L}$$

gain: double

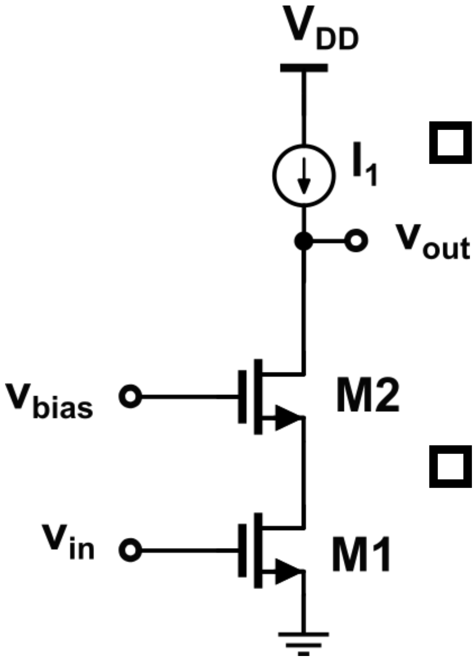
B. Cascode stage

$$A_v \approx \left(g_m r_O\right)^2 \qquad r_O -> g_m r_O{}^2$$

Increase gain by $g_m r_O$

V_{ov}: double, Swing ↓

Cascode Stage with current source load



- How to get high voltage gain in Cascode stage?
  - maximizing G_m and/or R_{out}
- G_m
  - determined by g_m of a transistor
  - trade-offs: the bias current and device capacitances
- If both M_1 and M_2 operate in saturation

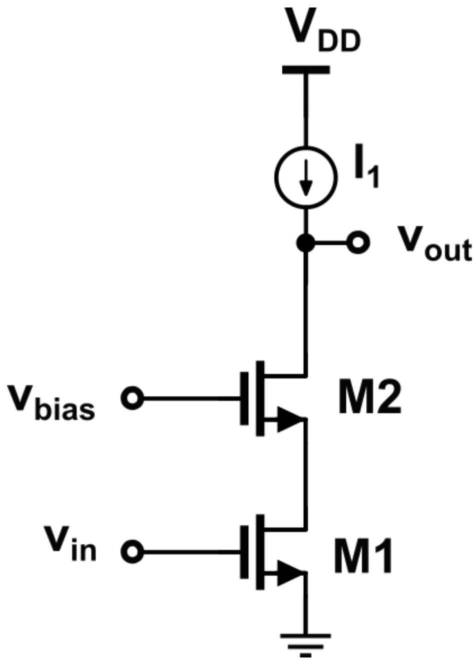
$$G_m = g_{m1}$$

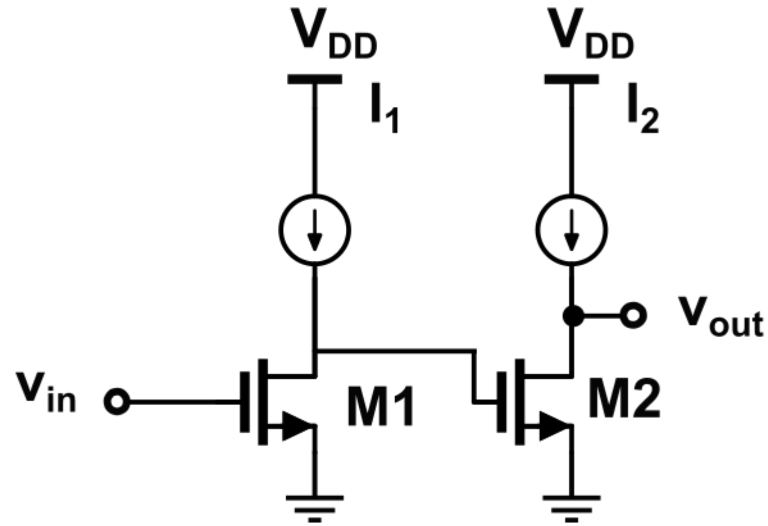
$$R_{out} \approx (g_{m2} + g_{mb2}) r_{O2} r_{O1}$$

$$A_v \approx g_{m1} (g_{m2} + g_{mb2}) r_{O1} r_{O2} \approx (g_m r_O)^2$$

- Maximum gain is roughly equal to the square of the **intrinsic gain of the transistors**

Cascode vs. Cascade

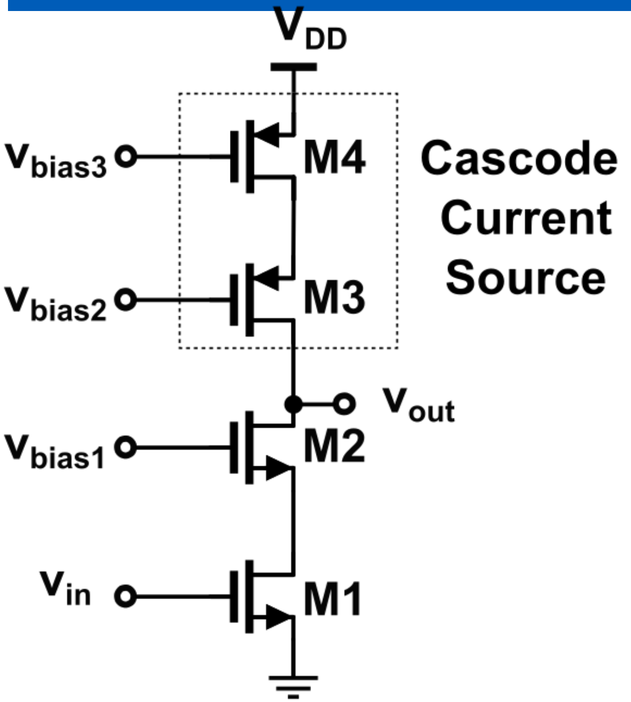




$$A_v = (g_m r_{DS})_1 (g_m r_{DS})_2 \qquad A_v = (g_m r_{DS})_1 (g_m r_{DS})_2$$

Trade-off between ? and ?

Cascode Structure as Current Source



- High output impedance
- Low voltage headroom

- PMOS cascode

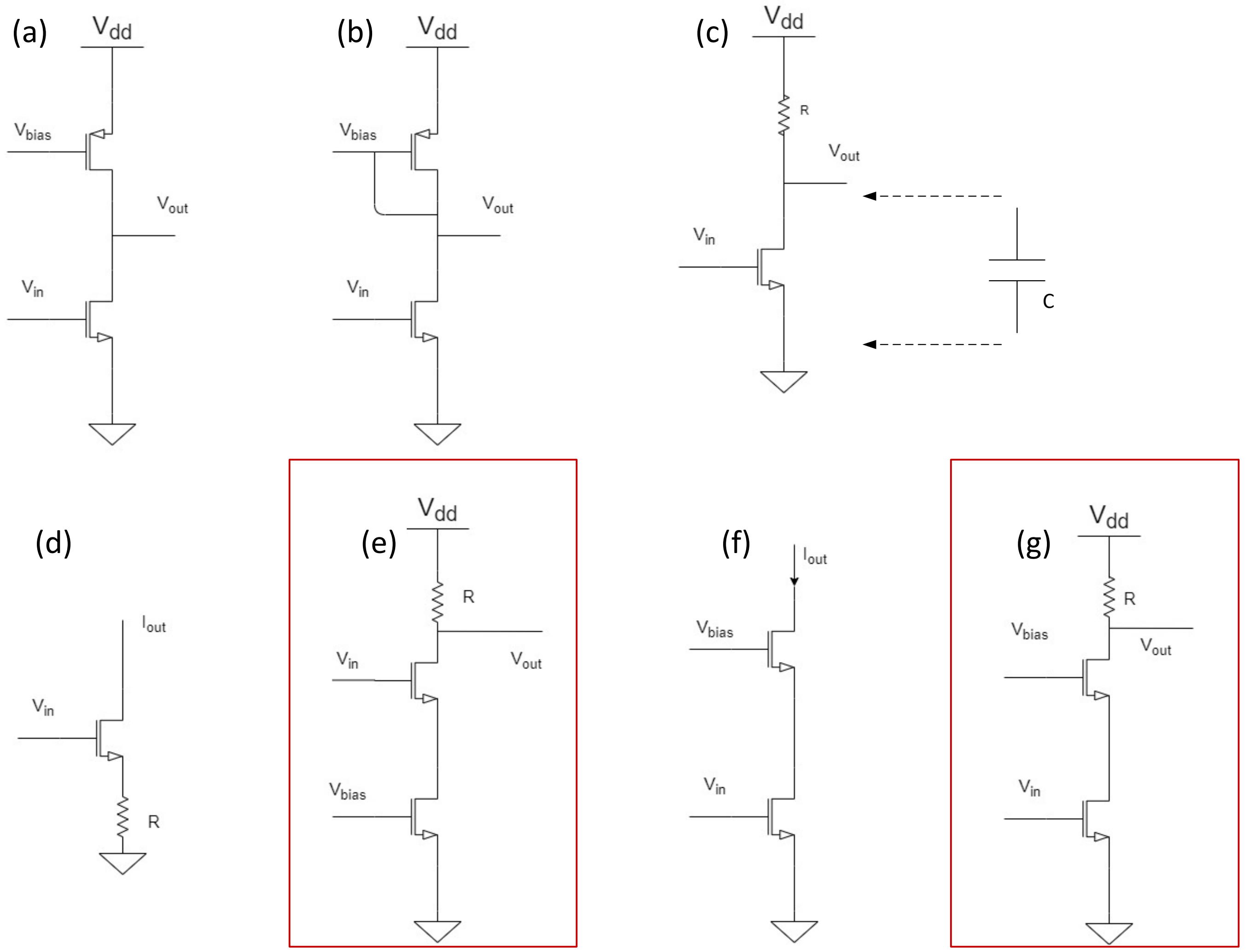
$$\left[1+\left(g_{m3}+g_{mb3}\right)r_{O3}\right]r_{O4}+r_{O3}$$

$$R_{out}=\left\{\left[1+\left(g_{m2}+g_{mb2}\right)r_{O2}\right]r_{O1}+r_{O2}\right\}\parallel\left\{\left[1+\left(g_{m3}+g_{mb3}\right)r_{O3}\right]r_{O4}+r_{O3}\right\}$$

$$\left|A_V\right|=g_{m1}R_{out}$$

$$A_V=g_{m1}\left[\left(g_{m2}r_{O2}r_{O1}\right)\parallel\left(g_{m3}r_{O3}r_{O4}\right)\right]$$

More examples



Summary

- **Common-Source Stage**

  Inverse Gain -> I-V curve

  why $R_D < r_o$ of a transistor

- **Source Follower**

  $Gm = gm/1+gm^* R_D$

  With high output resistance
  Similar to Cascode

- **Common-Gate Stage**

  Current input with (1/Gm) -> Iout = Iin

集成电路原理与设计
7.单级放大器

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