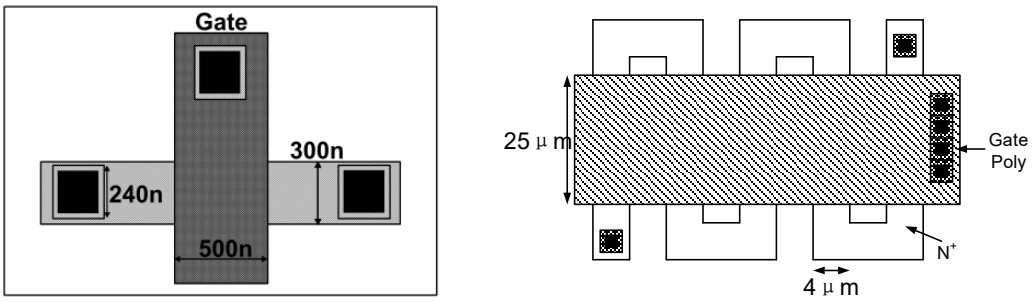
Exercise 1

1-1. Two layouts of n-channel MOSFET are shown in Fig.1.1. What is the width and length of the two devices?



(a) (b)

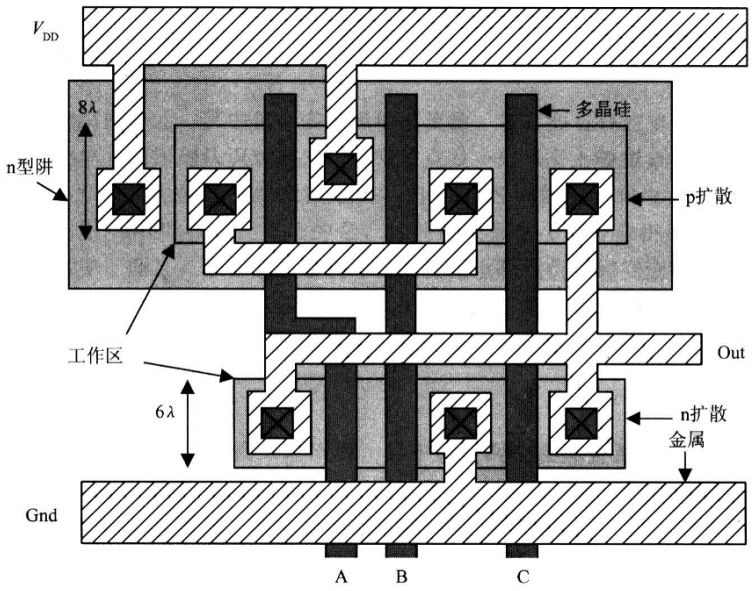
Fig.1.1

Answer:

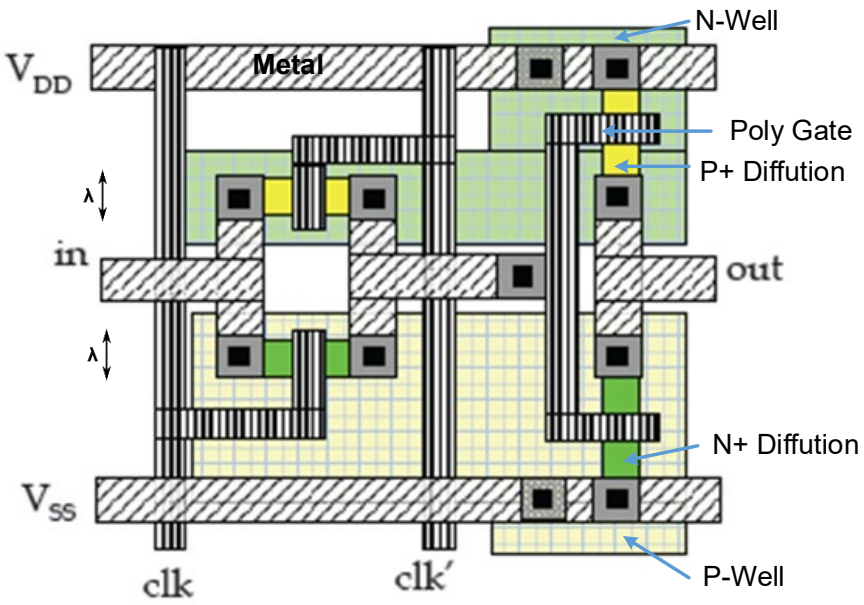
(a) Length=500n; Width=300n

(b) Length=5 × 25μm = 125μm; Width=4μm

1-2. The layouts of a circuit are shown in Fig.1.2. Give the corresponding schematics and its function, and mark the *W*/*L* sizes of each transistor. Assume $L=2\lambda$, $\lambda=0.4\mu m$.



(a) p-sub, n-well technology

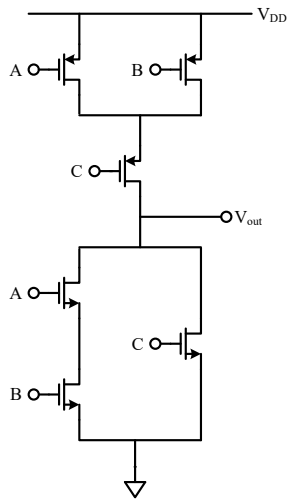


(b) dual-well technology, and $clk' = \overline{clk}$

Fig.1.2

Answer:

(a)



Out= $\overline{AB+C}$

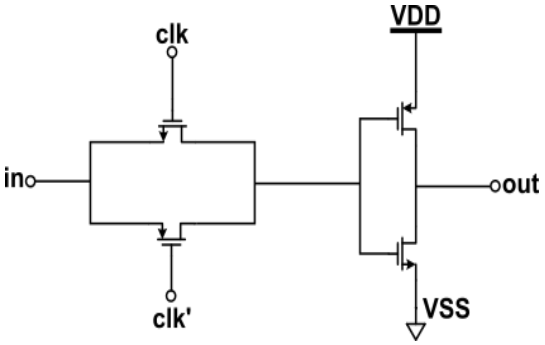
W/L of N-MOSFET:

$$\frac{6\lambda}{2\lambda}=\frac{6\times0.4}{2\times0.4}=\frac{2.4}{0.8}$$

W/L of P-MOSFET:

$$\frac{8\lambda}{2\lambda}=\frac{8\times0.4}{2\times0.4}=\frac{3.2}{0.8}$$

(b)



CLK high: Out=$\overline{IN}$

CLK low: Out=0

W/L of N-MOSFET:

$$\frac{\lambda}{2\lambda}=\frac{0.4}{2\times0.4}=\frac{0.4}{0.8}$$

W/L of P-MOSFET:

$$\frac{\lambda}{2\lambda}=\frac{0.4}{2\times0.4}=\frac{0.4}{0.8}$$

1-3. Layout of a different pair with PMOS current source loads in p-sub N-well technology is shown as Fig.1.3. Give the corresponding schematics and mark the W/L sizes of each transistor. Assume λ=0.4μm.

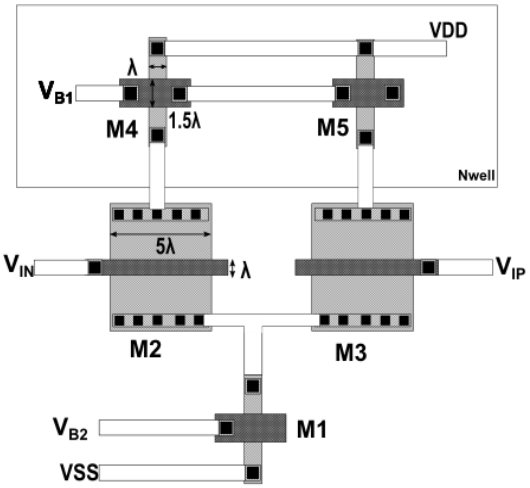
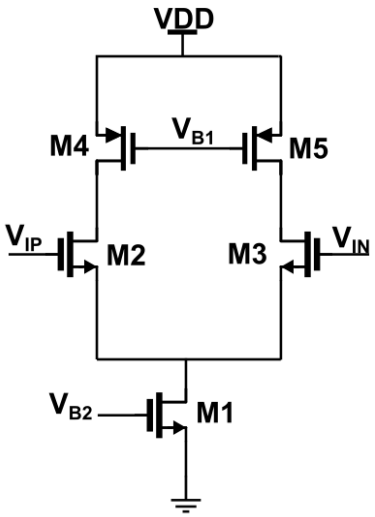


Fig.1.3

Answer:



M2=M3 $\frac{W}{L} = \frac{5\lambda}{\lambda}$