1-1. If the aspect ratio of an enhancement n-channel MOSFET is 4 μm/1 μm, (the relative model parameters can be seen in Table 1.1) the voltages of drain, gate, source and bulk are 3V, 2V, 0V and 0V respectively, calculate the drain current in this device. Then given the result of another p-channel MOSFET, whose voltages of drain, gate, source, and bulk are -3V, -2V, 0V and 0V respectively.

Table 1.1

Parameter	Description	n-channel	p-channel	Units
V_{TH0}	Threshold voltage (V_{BS}=0)	0.7	-0.7	V
$K=\mu C_{OX}$	Transconductance Parameter (in saturation)	110	50	$\mu A/V^2$
γ	Bulk threshold parameter	0.4	0.57	
λ	Channel length modulation parameter	0.04(L=1μm) 0.01(L=2μm)	0.05(L=1μm) 0.01(L=2μm)	$V^{1/2}$
$2\lvert\Phi_F\rvert$	Surface potential at strong inversion	0.7	0.8	V

Solution:

NMOS：As V_D=3V，V_G=2V，V_S=0V，V_B=0V

So V_{DS}=3V，V_{GS}=2V，V_{SB}=0V

$$V_{THN}=V_{TH0}+\gamma(\sqrt{|2\phi_F+V_{SB}|}-\sqrt{|2\phi_F|})=0.7\text{V}$$

$\therefore V_{DS}\geq V_{GS}-V_{THN}$，the NMOS works in saturation region and have

$$I_D=\frac{1}{2}K_N'\frac{W}{L}(V_{GS}-V_{THN})^2(1+\lambda_N V_{DS})$$

$$=\frac{1}{2}\times 110\times\frac{4}{1}\times(2-0.7)^2(1+0.04\times 3)=416.4\mu A$$

PMOS：As V_D=-3V，V_G=-2V，V_S=0V，V_B=0V

So V_{SD}=3V，V_{SG}=2V，V_{SB}=0V

$$V_{THP}=V_{TH0}+\gamma(\sqrt{|2\phi_F+V_{SB}|}-\sqrt{|2\phi_F|})=-0.7\text{V}$$

$\therefore V_{SD}\geq V_{SG}-|V_{THP}|$，the PMOS works in saturation region and have

$$I_D=\frac{1}{2}K_P'\frac{W}{L}(V_{SG}-|V_{THP}|)^2(1+\lambda_P V_{SD})$$

$$=\frac{1}{2}\times 50\times\frac{4}{1}\times(2-0.7)^2(1+0.05\times 3)=194.35\mu A$$

1-2. Find the small-signal model (gm, gmb, gds) for an n-channel transistor with the drain at 4 V,

gate at 4 V, source at 2 V, and the bulk at 0 V. Assume the model parameters from Table 1.1, and W/L = 10 μm/1 μm.

Solution:

$$V_T = V_{T0} + \gamma[\sqrt{2|\Phi_F| + v_{SB}} - \sqrt{2|\Phi_F|}]$$
$$V_T = 0.7 + 0.4[\sqrt{0.7 + 2.0} - \sqrt{0.7}] = 1.02$$
$$I_D = \frac{K'W}{2L}(v_{GS} - v_T)^2(1 + \lambda v_{DS})$$
$$I_D = \frac{110 \times 10^{-6} \times 10}{2}(2 - 1.02)^2(1 + 0.04 \times 2) = 570 \times 10^{-6}$$
$$g_m = \sqrt{2\frac{K'W}{L}(1 + \lambda Vds)I_D}$$
$$g_m = \sqrt{2 \times 110 \times 10^{-6} \times 10 \times 570 \times (1 + 0.04 \times 2) \times 10^{-6}} = 1.16 \times 10^{-3}$$
$$g_{mb} = g_m \frac{\gamma}{2(2|\Phi_F| + V_{SB})^{1/2}}$$
$$g_{mb} = 1.16 \times 10^{-3} \frac{0.4}{2(0.7 + 2.0)^{1/2}} = 141 \times 10^{-6}$$
$$g_{ds} = \lambda I_D$$
$$g_{ds} = 570 \times 10^{-6} \times 0.04 = 22.8 \times 10^{-6}$$

1-3. Current I_{ds} in a transistor is 62.5μA when its gate-source voltage is 1V. The current is 1mA when V=2.5V.

a) Which operating region (linear or saturated) of the transistor is these values of V correspond to?

b) Calculate β and V_T for given transistor.

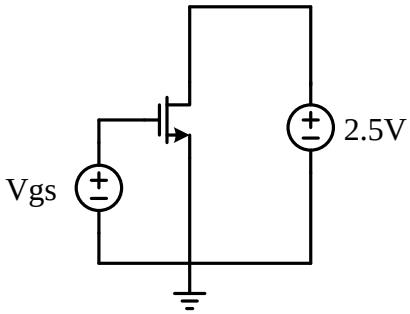


Figure 1.3

Solution:

a) Both V_1 and V_2 are larger than V_T, and

$$1 - V_T \le 2.5$$
$$2.5 - V_T \le 2.5$$

Therefore, the transistor works in saturated region in both circumstances.

b) Since

$$\frac{1}{2}\beta_N(1 - V_T)^2 = 62.5 \times 10^{-6}$$
$$\frac{1}{2}\beta_N(2.5 - V_T)^2 = 1 \times 10^{-3}$$

It can be derived from above equations that

$V_T = 0.5V$

$\beta_N = 500\,\mu A/V^2$

1-4. An NMOS device is plugged into the test configuration shown below in Fig .1.4 The input Vin is 2V. The current source draws a constant current of 50 μA. R is a variable resistor between 10kΩ and 30 kΩ. Transistor M1 has following transistor parameters: k'= 110μ V/A2, VT = 0.7V, and VDSAT = 0.6V, and has a W/L = 2.5μm/0.25um. For simplicity, the body effect and channel length modulation can be neglected, i.e λ=0, γ=0.

a) When R =10kΩ find the operation region, V_D and V_S.

b) For the case of R = 10kΩ, would V_S increase or decrease if $\lambda \neq 0$. Explain qualitatively.

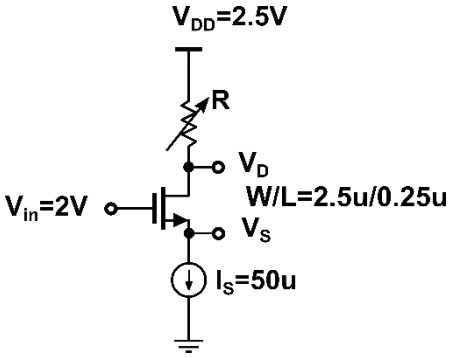


Fig.1.4

Solution:

a. When R =10K, $V_D = V_{DD} - IR = 2.5 - 50 \times 10^{-6} \times 10^4 = 2.5 - 0.5 = 2V$.Assume the device is in saturation $I_D = \frac{1}{2}K\frac{W}{L}(V_{GS} - V_{TH})^2 = 50uA$ find $V_{GS} - V_{TH} = 0.302V$, so $V_{GS} = 0.302 + 0.7V = 1.002V$,

$V_S = 0.998V$. V_{GS}=1.002V, V_{DS}=1.002V device in the saturation.

b. Increase. V_D is fixed due to constant current. $1 + \lambda V_{DS}$ form would try to increase the current more then 50uA, thus V_{GS} needs to reduce by increase V_S.

1-5. Fig. 1.5 shows how that two MOS transistors connected in parallel with channel widths of W_1 and W_2 and identical channel lengths of L can be modeled as one equivalent MOS transistor whose width is W_1+W_2 and whose length is L. Assume the transistors are identical except for their channel widths.

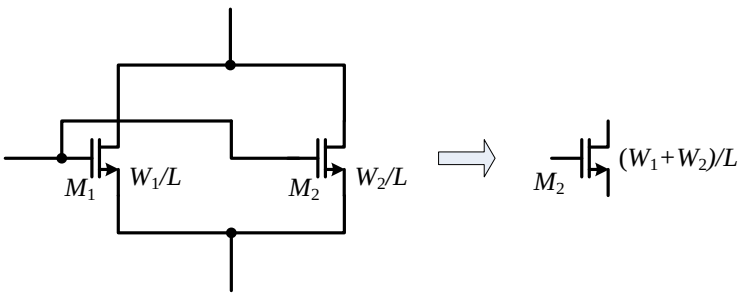


Figure 1.5

Demonstration:

For $V_{DS} \le V_{GS} - V_{TH}$

$$I_{D1} = \mu C_{OX} \frac{W_1}{L}[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}{}^2]$$

$$I_{D2} = \mu C_{OX} \frac{W_2}{L}[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}{}^2]$$

……

$$I_{Dn} = \mu C_{OX} \frac{W_n}{L}[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}{}^2]$$

$$\therefore I_D = I_{D1} + I_{D2} + \ldots + I_{Dn} = \mu C_{OX} \frac{W_1 + W_2 + \ldots + W_n}{L}[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}{}^2]$$

For $V_{DS} \ge V_{GS} - V_{TH}$

$$I_D = I_{D1} + I_{D2} + \ldots + I_{Dn} = \frac{1}{2}\mu C_{OX} \frac{W_1 + W_2 + \ldots + W_n}{L}(V_{GS} - V_{TH})^2$$

Thus the equivalent length = L and the equivalent width = $W_1 + W_2 + \ldots + W_n$.

1-6. A) Fig. 1.6 shows the real and ideal I-V characteristics of two enhancement N-MOSFETs by real line and broken line respectively. Compare the difference of the two MOSFETs and explain why different.

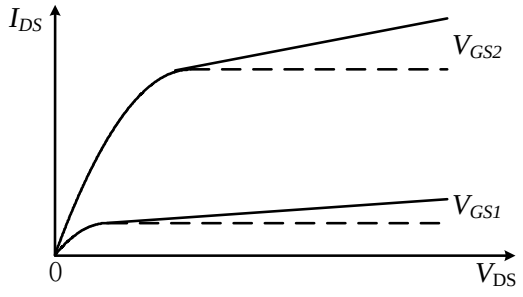


Figure 1.6

B) In Table 1.1, why is γ_P greater than γ_N for a n-well, CMOS technology?

Solution:

A) Consider channel length modulation effect:

V_{GS1}——long channel device

V_{GS2}——Short channel device

B) The expression for γ is:

$$\gamma = \frac{\sqrt{2\varepsilon_{si} q N_{SUB}}}{C_{ox}}$$

Because γ is a function of substrate doping, a higher doping results in a larger value for γ. In general, for an nwell process, the well has a greater doping concentration than the substrate and therefore devices in the well will have a larger γ. That's why γ_P is greater than γ_N.

1-7. Given

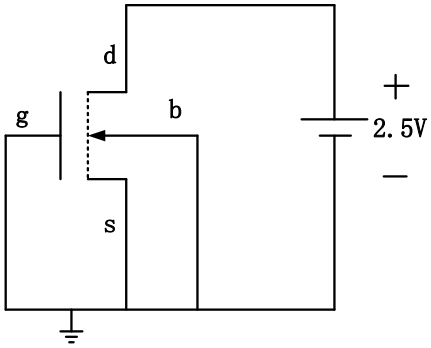


Fig. 1.7

A) What type (NMOS or PMOS) is transistor shown in Fig. 1.7?

B) Calculate I_{ds} when this transistor has the same β as the transistor in exercise 1-1 and V_T=-2V.

Solution:

A) From its polarity of power supply of V_{ds} it can be seen that the transistor is an n-channel MOS transistor.

B) From V_{gs} it can be seen that the transistor is a depletion transistor.

$$\because V_{ds} > V_{gs} - V_T$$

$$\therefore I_d = \frac{1}{2}\beta_N (V_{gs} - V_T)^2$$

$$= 880uA$$

[思考题]

1-8. Fig. 1.8 shows that two MOS transistors connected in series with channel lengths of L_1 and L_2 and identical channel widths of W can be modeled as one equivalent MOS transistor whose width is W and whose length is L_1+L_2. Assume the transistors are identical except for their channel lengths. Ignore the body effect and channel-length modulation.

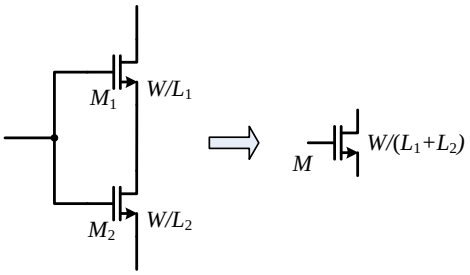
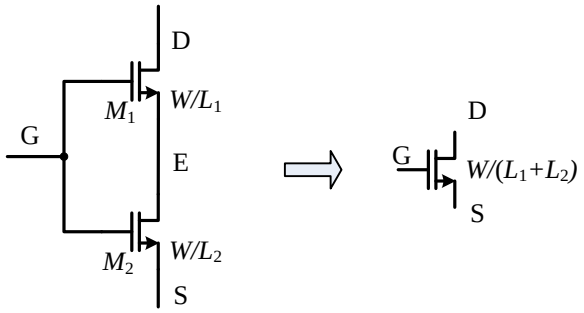


Figure 1.5

Solution:



(1) When $V_{GS}<V_{TH}$ and $V_{GE}<V_{GS}<V_{TH}$, the MOSFETs are in cut off.

(2) While M1 operates in triode ($V_{DE} < V_{GE} - V_{THN}$), that is equivalent to $V_{DE} + V_{ES} < V_{GE} + V_{ES} - V_{THN}$, i.e. $V_{DS} < V_{GS} - V_{THN}$.

Thus M2 operates in triode, too.

Thus

$$I_{D1} = \mu_n C_{OX} \frac{W}{L_1}[(V_{GE} - V_{TH})V_{DE} - \frac{1}{2}V_{DE}^2] \quad (1)$$

$$I_{D2} = \mu_n C_{OX} \frac{W}{L_2}[(V_{GS} - V_{TH})V_{ES} - \frac{1}{2}V_{ES}^2] \quad (2)$$

Since

$$V_{DS} = V_{DE} + V_{ES} \quad (3)$$

$$V_{GE} = V_{GS} - V_{ES} \quad (4)$$

$$I_{D1} = I_{D2} = I_D \quad (5)$$

It can be derived from equations (1), (2), (3), (4) and (5) that

$$(V_{GS} - V_{TH})V_{ES} - \frac{1}{2}V_{ES}^2 = \frac{L_2}{L_1}[(V_{GS} - V_{TH} - V_{ES})(V_{DS} - V_{ES}) - \frac{1}{2}(V_{DS} - V_{ES})^2]$$

$$= \frac{L_1}{L_1 + L_2}[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2]$$

So we can get $I_D = \mu_n C_{OX} \frac{W}{L_1 + L_2}[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2]$

(3) While M1 operates in saturation ($V_{DE} > V_{GE} - V_{THN}$). It means $V_{DE} + V_{ES} > V_{GE} + V_{ES} - V_{THN}$, i.e. $\boldsymbol{V_{DS} > V_{GS} - V_{THN}}$.

$V_E = V_G - V_{GE} < V_G - V_{THN}$, it means $\boldsymbol{V_{ES} < V_{GS} - V_{THN}}$. M2 operates in triode.

So

$$I_{D1} = \frac{1}{2}\mu_n C_{OX} \frac{W}{L_1}(V_{GE} - V_{TH})^2 \quad (1)$$

$$I_{D2} = \frac{1}{2}\mu_n C_{OX} \frac{W}{L_2}[2(V_{GS} - V_{TH})V_{ES} - V_{ES}^2] \quad (2)$$

$$V_{DS} = V_{DE} + V_{ES} \quad (3)$$

$$V_{GE} = V_{GS} - V_{ES} \quad (4)$$

$$I_{D1} = I_{D2} = I_D \quad (5)$$

It can be derived from equations (1), (2), (3), (4) and (5) that

$$I_D = \frac{1}{2}\mu_n C_{OX} \frac{W}{L_1 + L_2}(V_{GS} - V_{TH})^2$$

That just like a MOSFET operating in saturation, which has a length of L_1+L_2 and a width of W. It can be deducted similarly that n MOSFETs in series acts as a MOSFET with an aspect ratio of $W/(L_1+L_2+\ldots L_n)$.