集成电路原理与设计

11. 反相器

宋爽

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Syllabus

课数	内容	课数	内容
1	导论	9	差分放大器
2	器件模型	10	运算放大器
3	电容特性，小信号模型	11	导线
4	工艺流程	12	反相器
5	模拟基本单元	13	组合逻辑
6	电流镜与基准	14	时序逻辑
7	单级放大器	15	集成电路专题讲座一
8	课堂测验	16	集成电路专题讲座二

Goals

- Quantification of integrity, performance and energy metrics of an inverter
- Optimization of an inverter design (**delay optimization**)

Design metrics of the gate

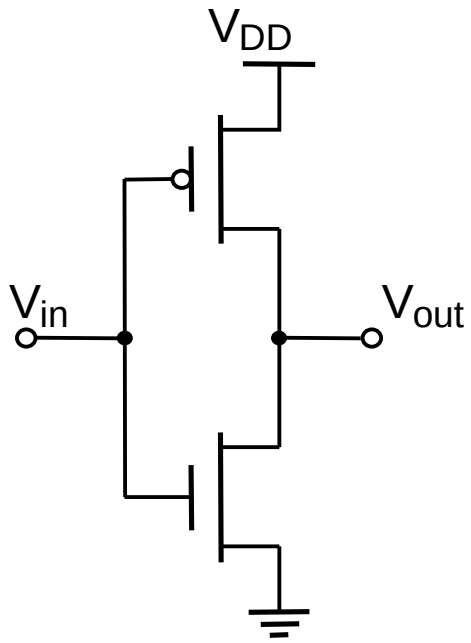
- ***Cost:*** *complexity, area*
- ***Integrity and robustness:*** *static (or steady-state) behavior*
- ***Performance:*** *dynamic (or transient) response*
- ***Energy efficiency:*** *energy and power consumption*

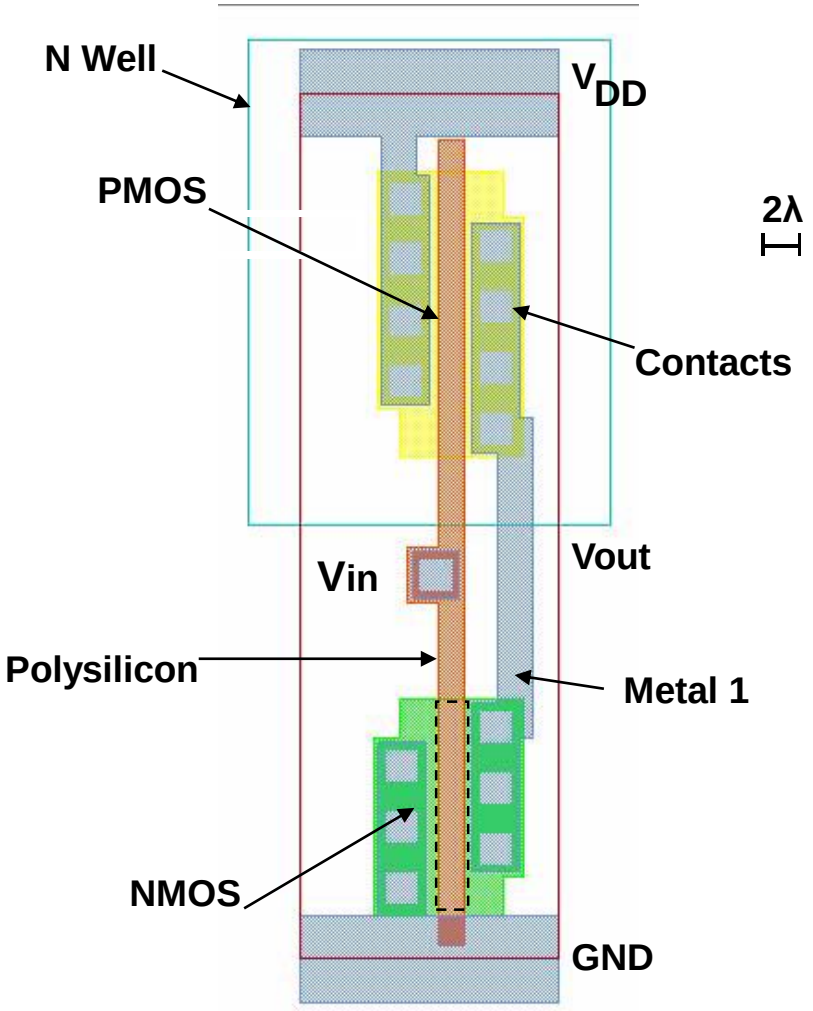
Outline

- **Inverter Basic Characteristics**
- **Static Behavior**
- **Dynamic Behavior**
- **Power, Energy**

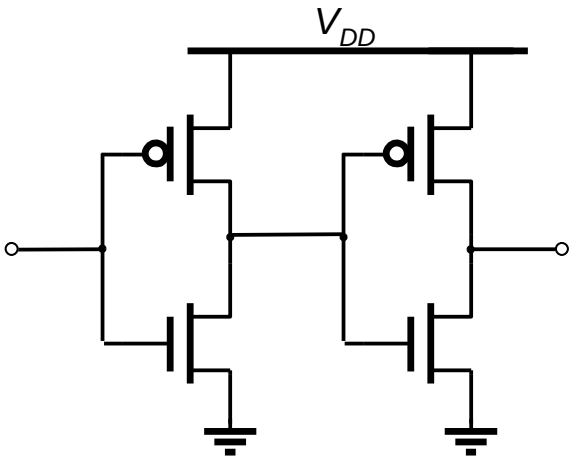
Reference:
Chapter 5, <Digital Integrated Circuits: A design perspective> Rabaey著

CMOS Inverter: A first glance

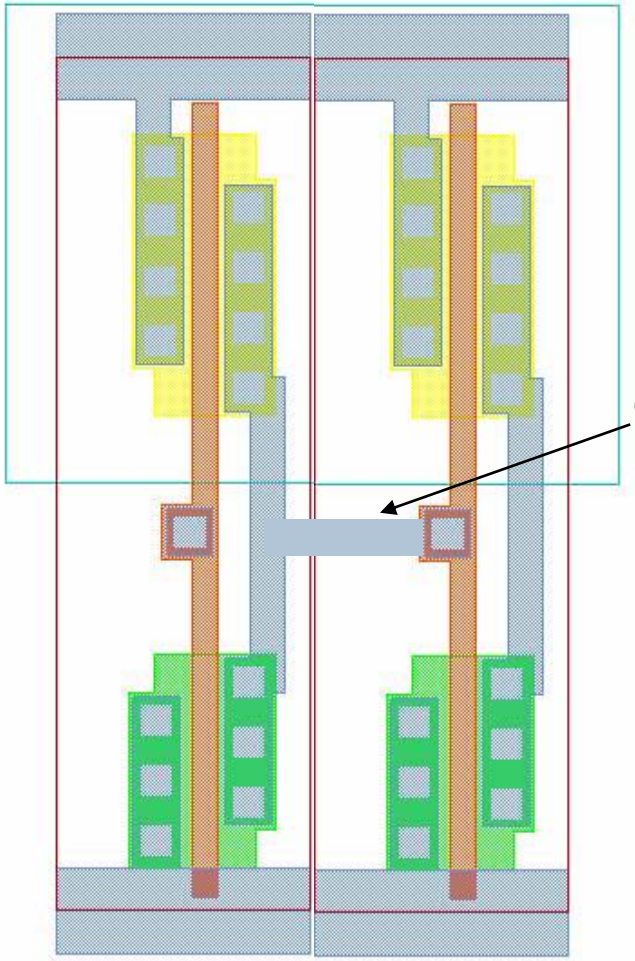




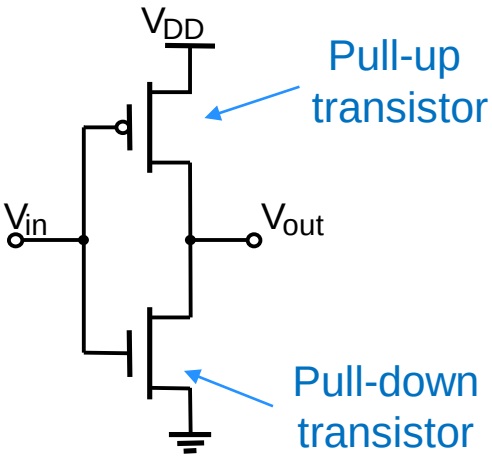
Appendix :Two Inverters

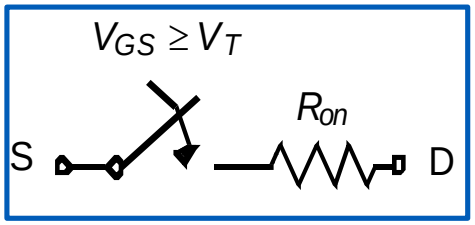


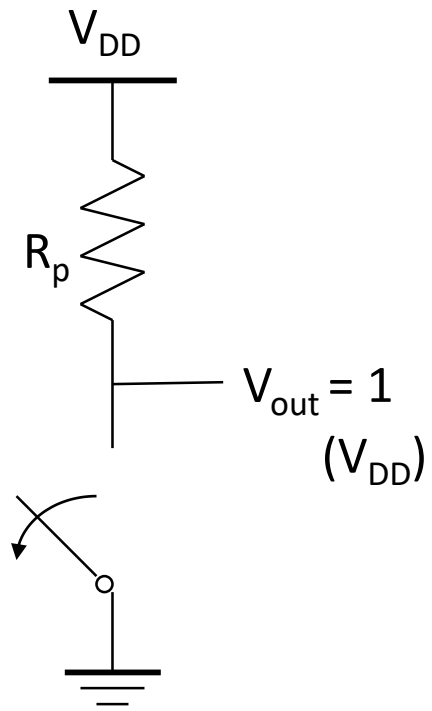
Share power and ground



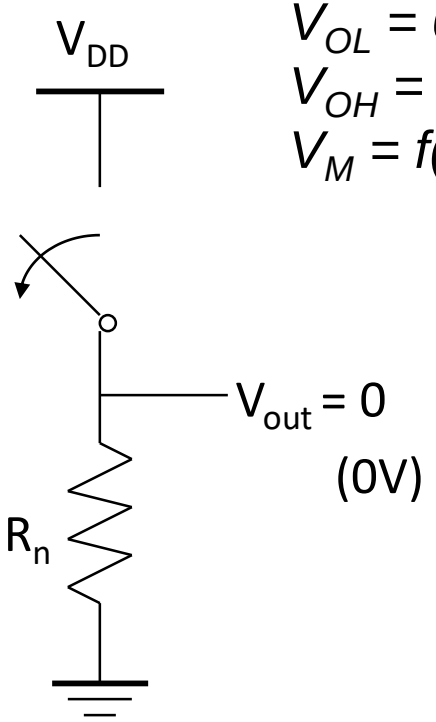
First-Order DC Analysis







$V_{in} = 0$



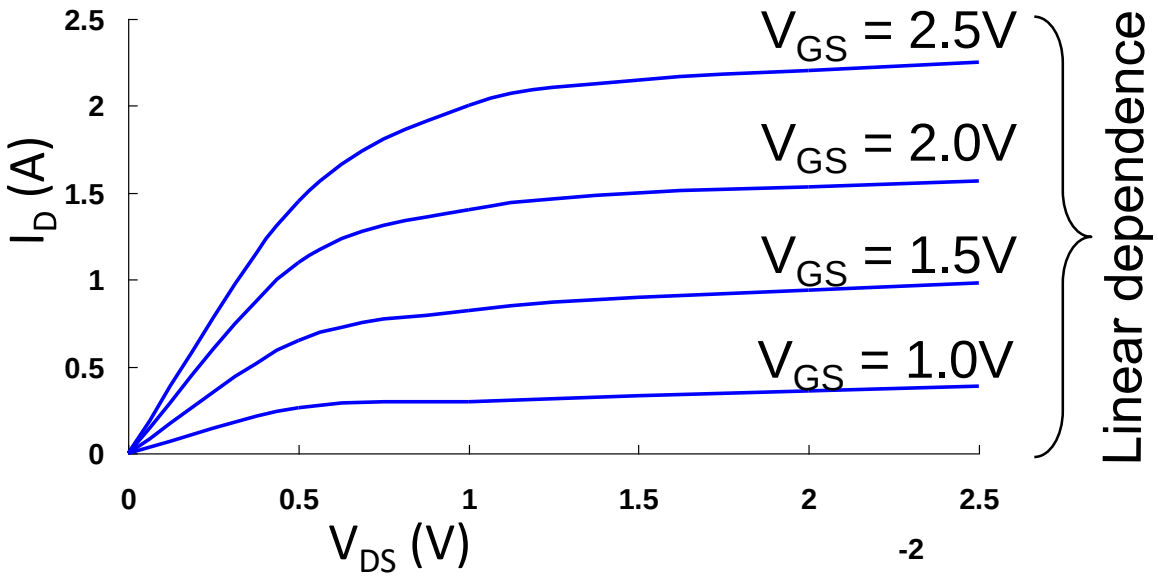
$V_{in} = V_{DD}$

$V_{OL} = 0$
$V_{OH} = V_{DD}$
$V_M = f(R_n, R_p)$

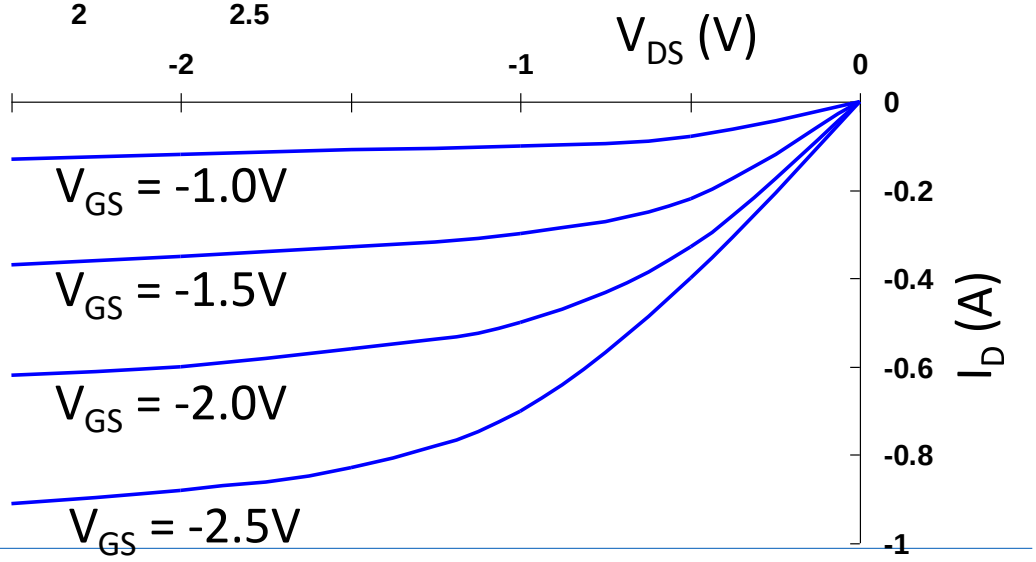
First-Order DC Analysis: Properties

- Full **rail-to-rail** swing ⇒ high noise margins
- Logic levels not dependent upon the relative device sizes
  - ⇒ transistors can be minimum size *ratioless无比电路*
- Always a path between V_{out} to V_{DD} or GND in steady state
  - ⇒ low output impedance (~kΩ)
  - ⇒ less sensitive to noise and disturbances
- Extremely high input resistance
  - ⇒ nearly zero steady-state input current
  - ⇒ large fan-out (albeit it with degraded performance: delay)
- No direct path in steady-state between power and ground
  - ⇒ no static power dissipation (ignores leakage current)
- Propagation delay function of load capacitance and resistance of transistors

Review: Short Channel I-V Plot (NMOS/PMOS)



NMOS transistor 0.25um,
L_d = 0.25um, W/L = 1.5,
V_{DD} = 2.5V, V_T = 0.4V

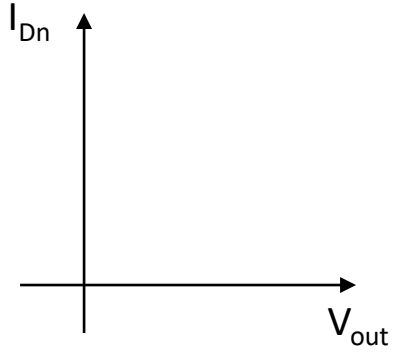


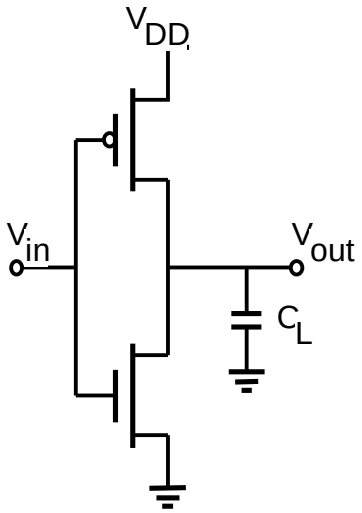
PMOS transistor 0.25um,
L_d = 0.25um, W/L = 1.5,
V_{DD} = 2.5V, V_T = -0.4V

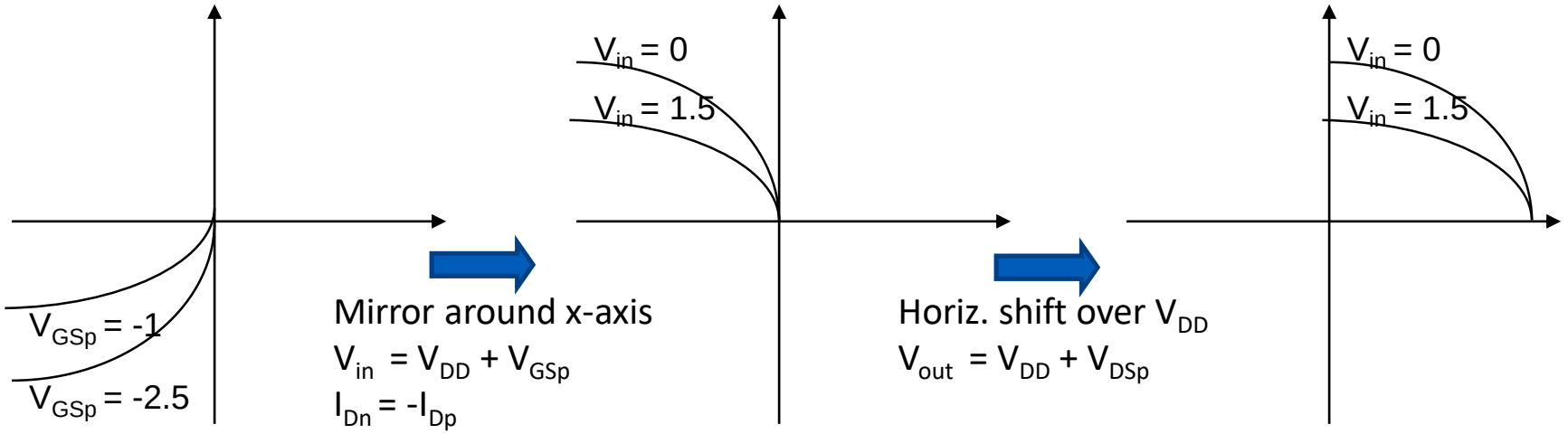
Review: Transforming PMOS I-V Lines

- Want common coordinate set V_{in}, V_{out}, and I_{Dn}

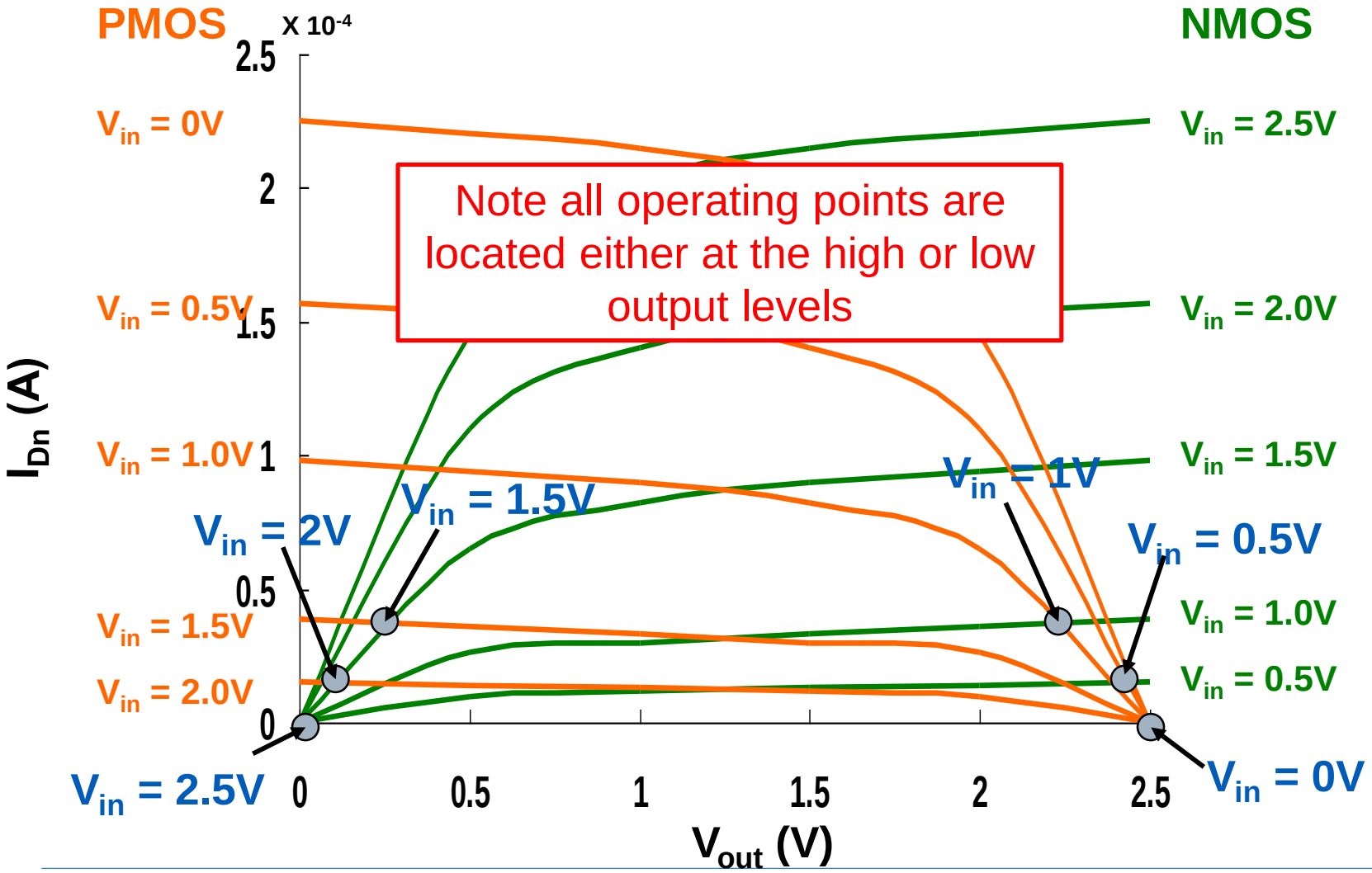
$I_{DSp} = -I_{DSn}$
$V_{GSn} = V_{in}$; $V_{GSp} = V_{in} - V_{DD}$
$V_{DSn} = V_{out}$; $V_{DSp} = V_{out} - V_{DD}$





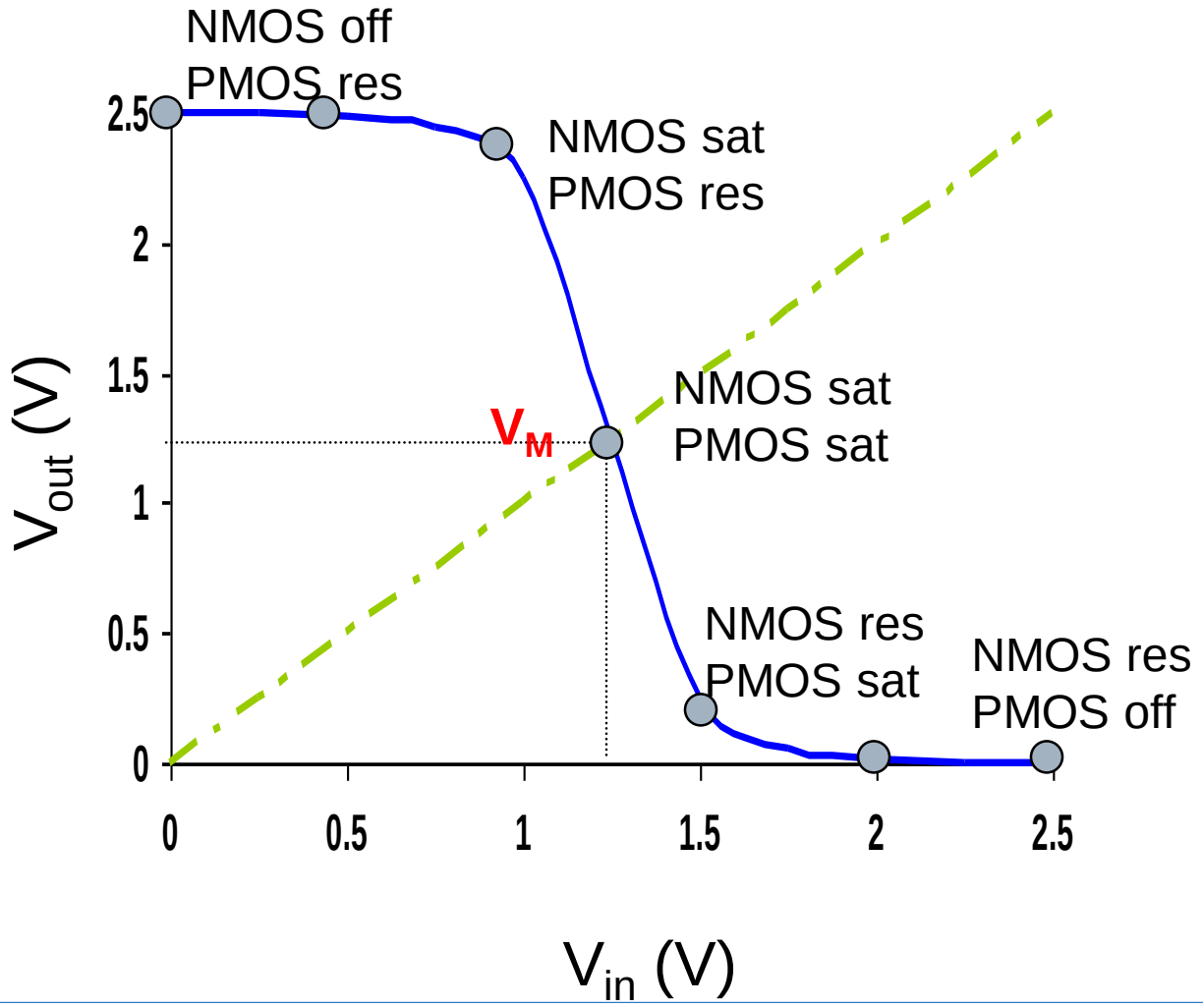


CMOS Inverter Load Lines

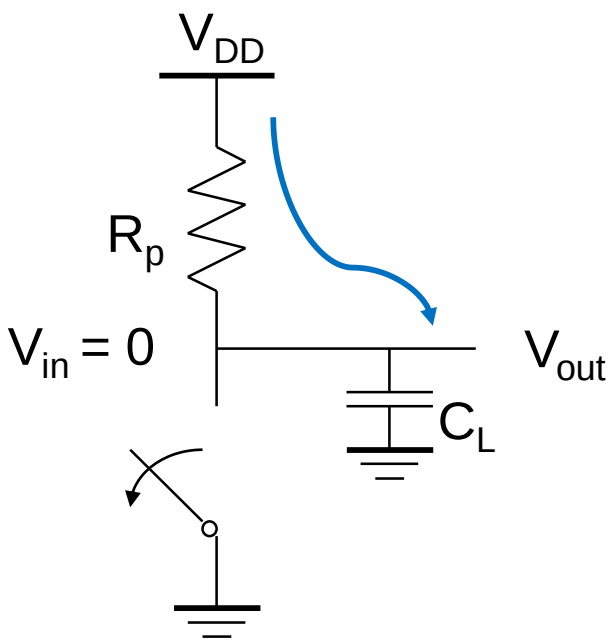


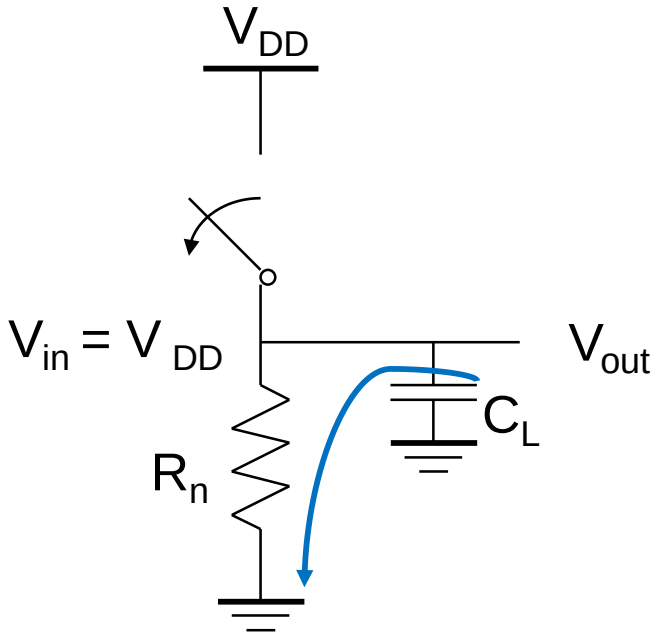
0.25um, $W/L_n = 1.5$, $W/L_p = 4.5$, $V_{DD} = 2.5V$, $V_{Tn} = 0.4V$, $V_{Tp} = -0.4V$

CMOS Inverter VTC



Switch Model of Dynamic Behavior





Gate response time is determined by the time to

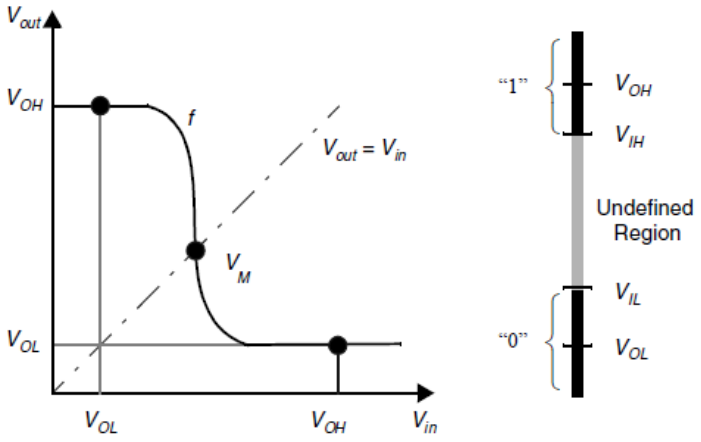
-- charge C_L through R_p

-- discharge C_L through R_n

A fast gate is build either by keeping the output capacitance small and by decreasing the on-resistance of the transistor

Outline

- Inverter Basic Characteristics
- Static Behavior
  - Switching Threshold
  - Noise Margin
  - Robustness Revisited
- Dynamic Behavior
- Power, Energy



Switching Threshold

- V_M: $V_{in} = V_{out}$ (both PMOS and NMOS in saturation, $V_{DS} = V_{GS}$) assumed to be velocity-saturated ($V_{DSAT} < V_M - V_T$) ,and ignore the channel length modulation effects

$$k_n V_{DSATn}\left(V_M - V_{Tn} - \frac{V_{DSATn}}{2}\right) + k_p V_{DSATp}\left(V_M - V_{DD} - V_{Tp} - \frac{V_{DSATp}}{2}\right) = 0$$

Solving for V_M yields

$$V_M = \frac{\left(V_{Tn} + \frac{V_{DSATn}}{2}\right) + r\left(V_{DD} + V_{Tp} + \frac{V_{DSATp}}{2}\right)}{1 + r} \quad \text{with} \quad r = \frac{k_p V_{DSATp}}{k_n V_{DSATn}} = \frac{\upsilon_{satp} W_p}{\upsilon_{satn} W_n}$$

$$V_M \approx r V_{DD} / (1 + r)$$

r: the relative driving strengths of PMOS/NMOS

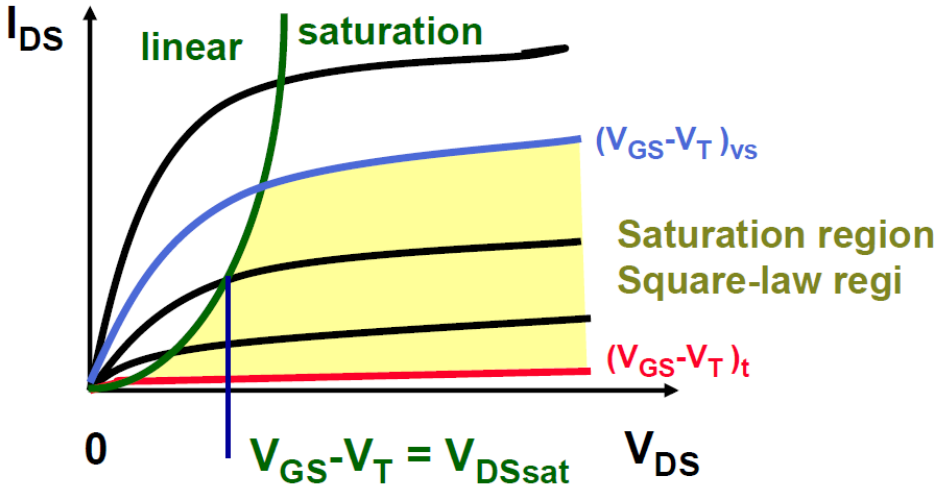
-- ***r*** set the switching threshold

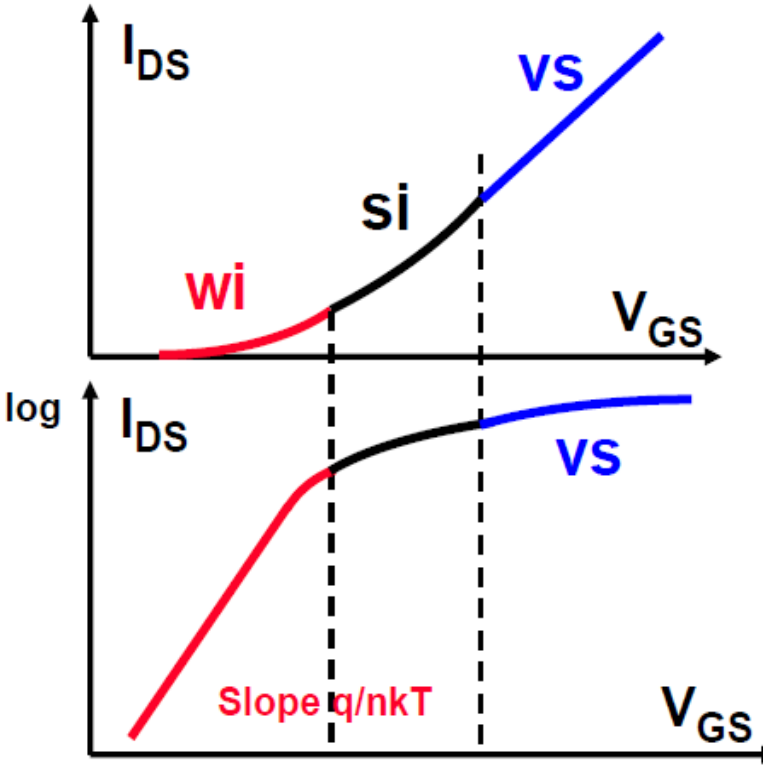
-- ***r*** **≈ 1**: $V_M = V_{DD}/2 \Rightarrow$ comparable high and low noise margins

--To move V_M upwards, a larger r is required making PMOS wider

--Increasing the strength of NMOS, moves V_M closer to GND

Recall the Velocity Saturation





Velocity Saturation	$I_{DS} = v_{sat} W C_{ox} \left(V_{GS} - V_{TH}\right)$
Strong Inversion	$I_{DS} = \frac{1}{2} \mu_n C_{OX} \frac{W}{L} \left(V_{GS} - V_{TH}\right)^2$
Weak Inversion	$I_{DS} = I_0 \exp \frac{V_{GS}}{n kT/q}$

Switching Threshold: *r*

$$V_M \approx rV_{DD}/(1+r) \qquad where\ r = k_p V_{DSATp}/k_n V_{DSATn}$$

Example

In generic 0.25μm CMOS process, V_{DD} = 2.5V, and a minimum size NMOS device: $(W/L)_n$ = 1.5

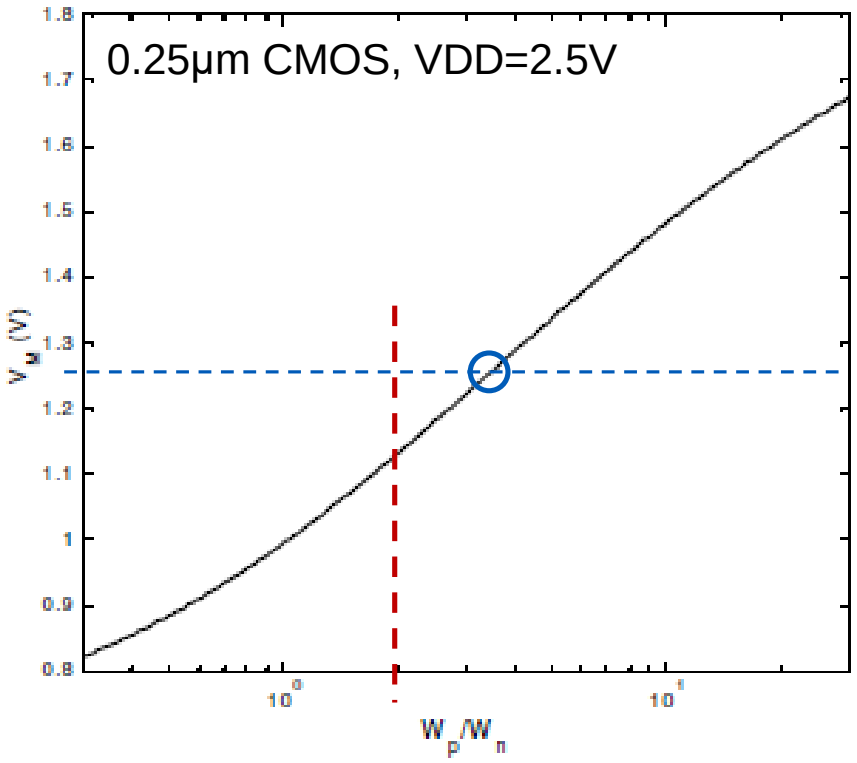
	V_{T0}(V)	γ($V^{0.5}$)	V_{DSAT}(V)	k'(A/V^2)	λ(V^{-1})
NMOS	0.43	0.4	0.63	115 x 10^{-6}	0.06
PMOS	-0.4	-0.4	-1	-30 x 10^{-6}	-0.1

$$\frac{(W/L)_p}{(W/L)_n} = \frac{115\times10^{-6}\times0.63\times(1.25-0.43-0.63/2)}{30\times10^{-6}\times1.0\times(1.25-0.4+1.0/2)} = 3.5 \Rightarrow (W/L)_p = 3.5 \text{ x } 1.5 = 5.25$$

Velocity saturation does not occur: $V_M = \dfrac{V_{Tn} + r(V_{DD} + V_{Tp})}{1+r}$ with $r = \sqrt{\dfrac{-k_p}{k_n}}$

When designing static CMOS circuits, to balance the driving strengths of the transistors by **making PMOS wider than NMOS**, if one wants to maximize the noise margins and obtain symmetrical characteristics

Simulated Inverter V_M



- V_M is relatively insensitive to variations in device ratio

r	3.4	3	2.5	2
V_M	1.25	1.22	1.18	1.13

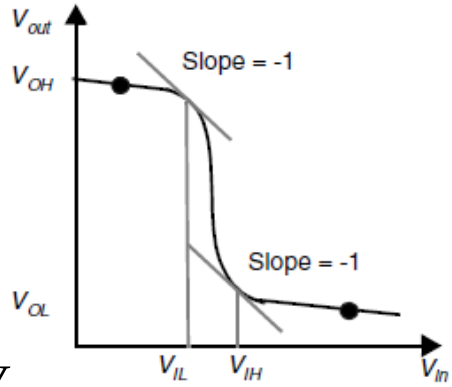
- r: shift the transient region of VTC

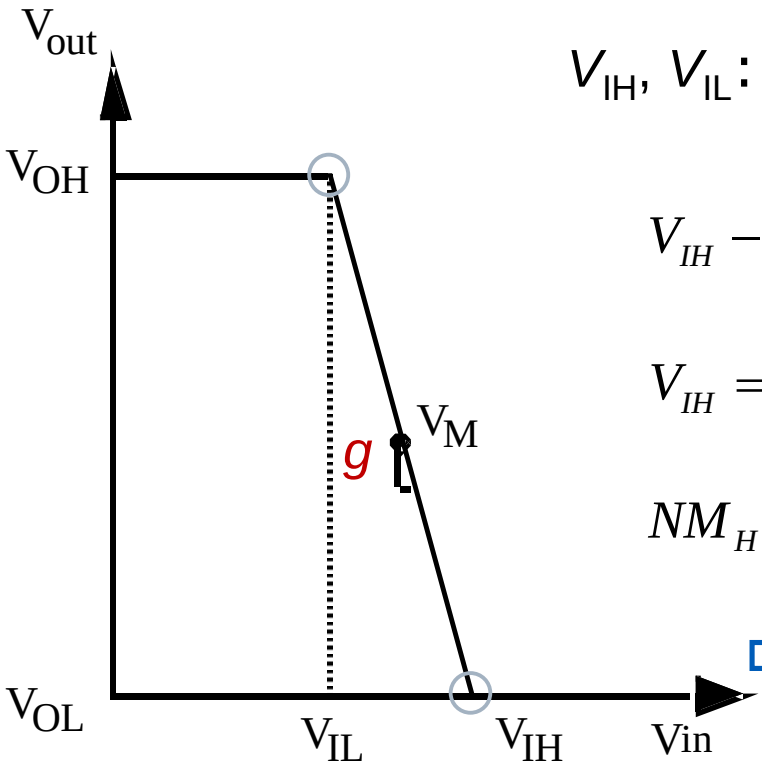
-- Increasing Wp moves V_M towards VDD

-- Increasing Wn moves V_M towards GND

inverter with asymmetrical V_M

Noise Margins





A simplified approach

V_{IH}, V_{IL}: $\dfrac{dV_{out}}{dV_{in}} = -1$

$$V_{IH} - V_{IL} = -\frac{V_{OH} - V_{OL}}{g} = -\frac{V_{DD}}{g}$$

$$V_{IH} = V_M - \frac{V_M}{g} \qquad V_{IL} = V_M + \frac{V_{DD} - V_M}{g}$$

$$NM_H = V_{DD} - V_{IH} \qquad NM_L = V_{IL}$$

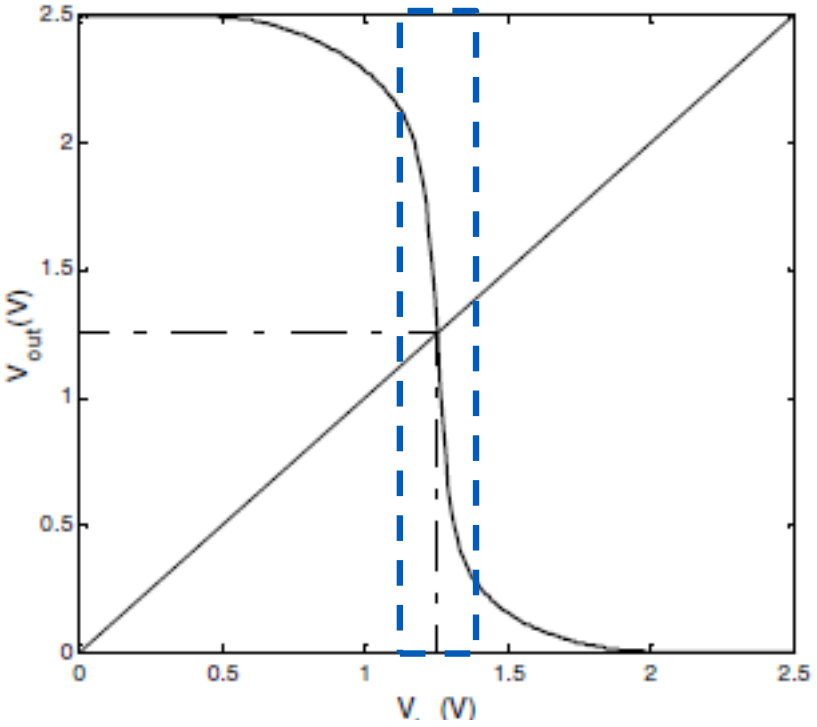
⇨ a high gain in transition region

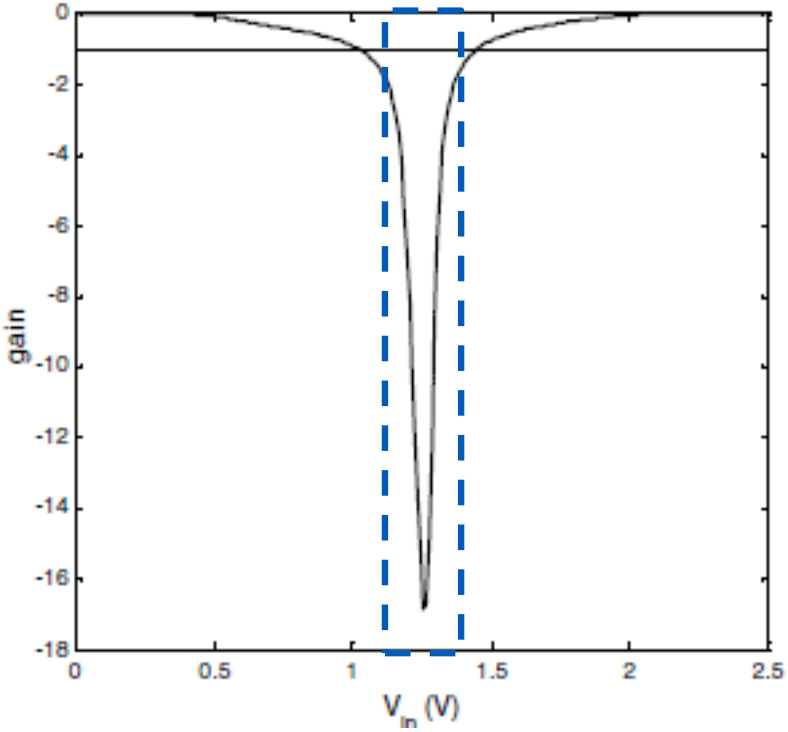
V_M: $g \approx \dfrac{1+r}{(V_M - V_{Tn} - V_{DSATn}/2)(\lambda_n - \lambda_p)}$

? $g \to \infty$ $\qquad NM_H = V_{OH} - V_M$

$$NM_L = V_M - V_{OL}$$

Inverter Gain

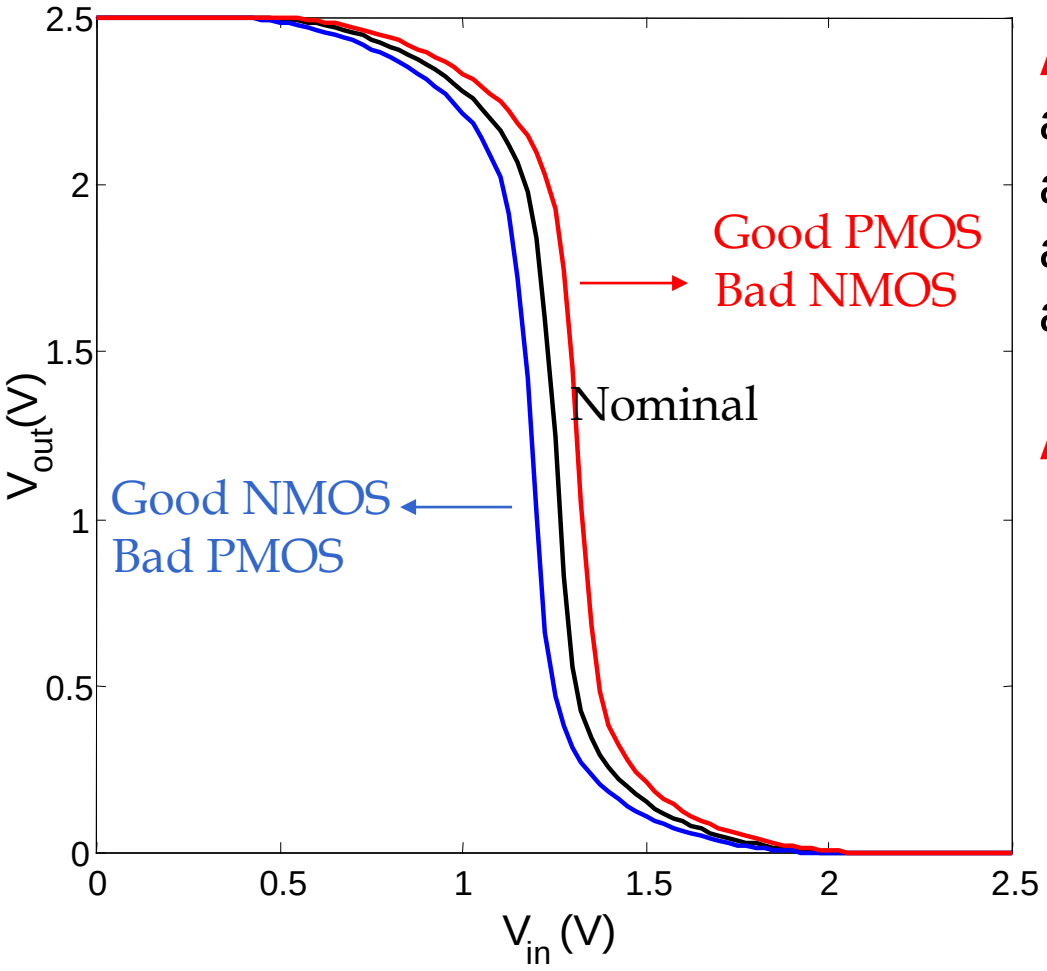




$$g = -\frac{1}{I_D(V_M)}\frac{k_n V_{DSATn} + k_p V_{DSATp}}{\lambda_n - \lambda_p} \approx \frac{1+r}{\left(V_M - V_{Tn} - V_{DSATn}/2\right)\left(\lambda_n - \lambda_p\right)}$$

Analog IC vs. Digital IC

Impact of Process Variations



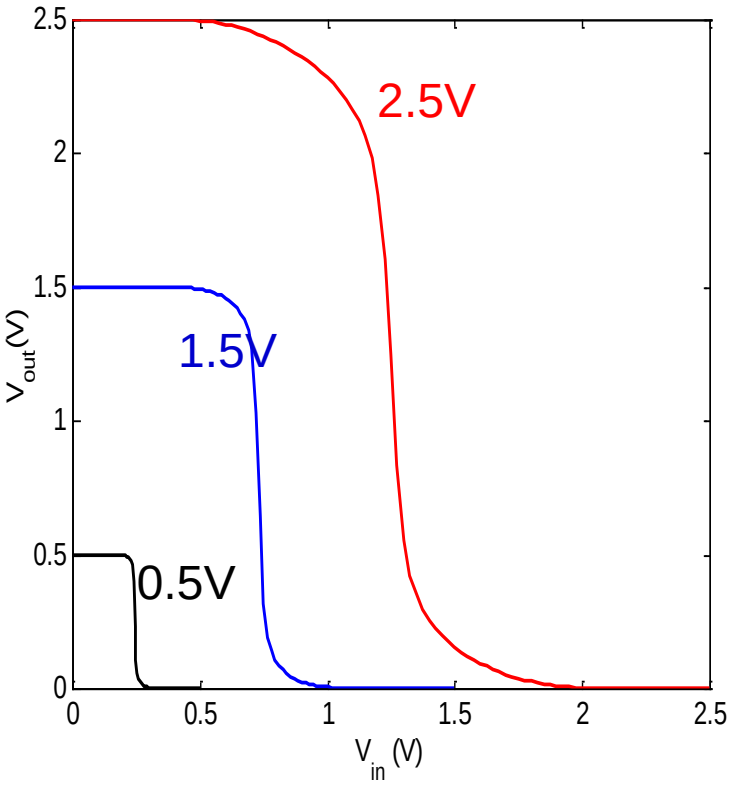
Corner model

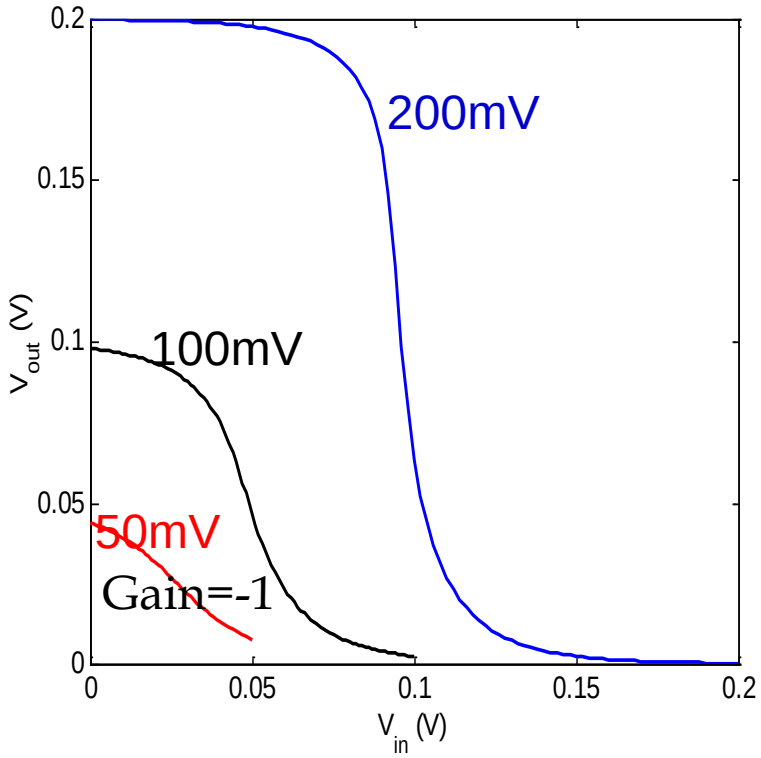
A good device:
a small oxide thickness (-3nm),
a small length (-25nm),
a higher width (+30nm)
a smaller threshold (-60mV).

A bad device: the opposite

⇨ **a shift in V_M**

Gain as a function of V_{DD}





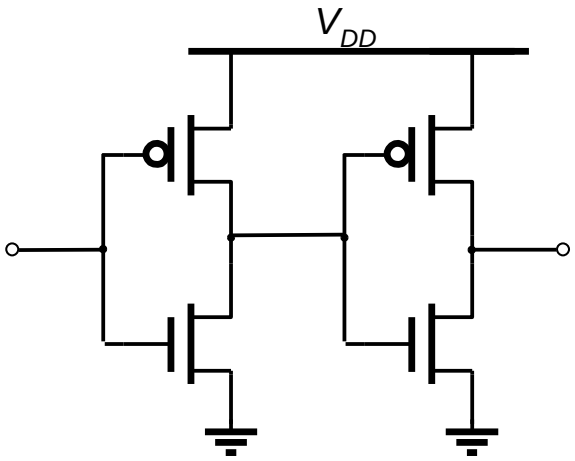
V_{TH}=±0.4V

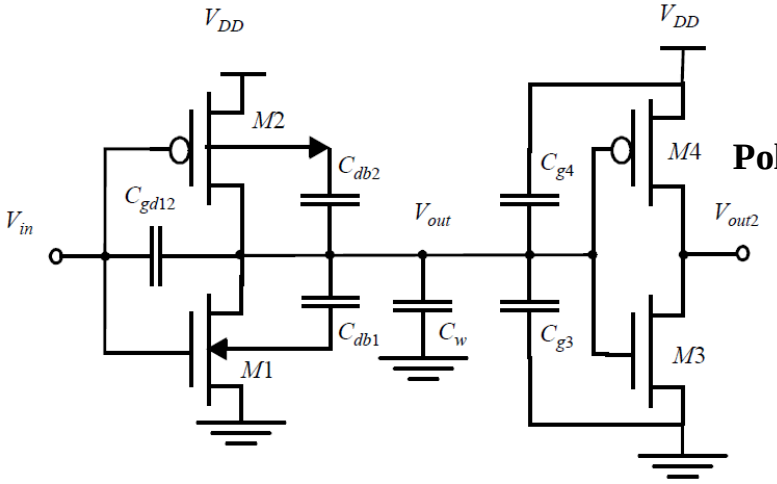
$$V_{DD\min} > (2 \sim 4)\frac{kT}{q} \qquad \phi_T = \frac{kT}{q} = 26mV \text{ (300K)}$$

Outline

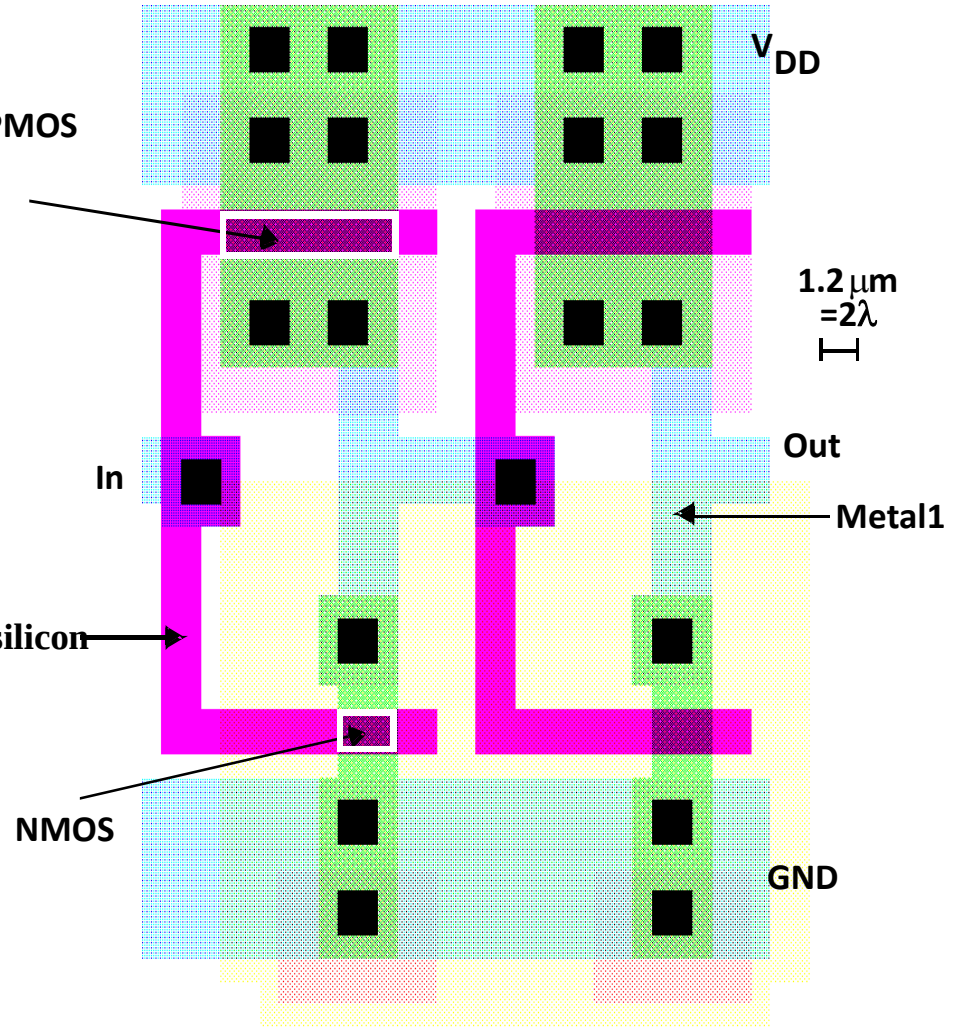
- Inverter Basic Characteristics
- Static Behavior
- Dynamic Behavior
  - Propagation delay: first-order analysis
  - Propagation delay from perspective
- Power, Energy

C_L in CMOS Inverters



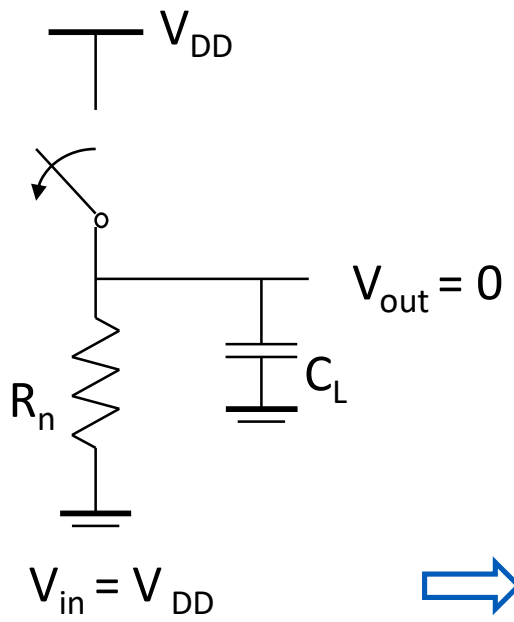


$$C_L = C_{inc} + C_{ext}$$



Inverter Propagation Delay

- Propagation delay is proportional to the time-constant of the network formed by the pull-down resistor and the load capacitance



$$t_p = \int_{v_1}^{v_2} \frac{C_L(v)}{i(v)} dv = f(R_n, C_L)$$

first-order linear RC-network:

$$t_{pHL} = \ln(2) R_{eqn} C_L = 0.69 R_{eqn} C_L$$

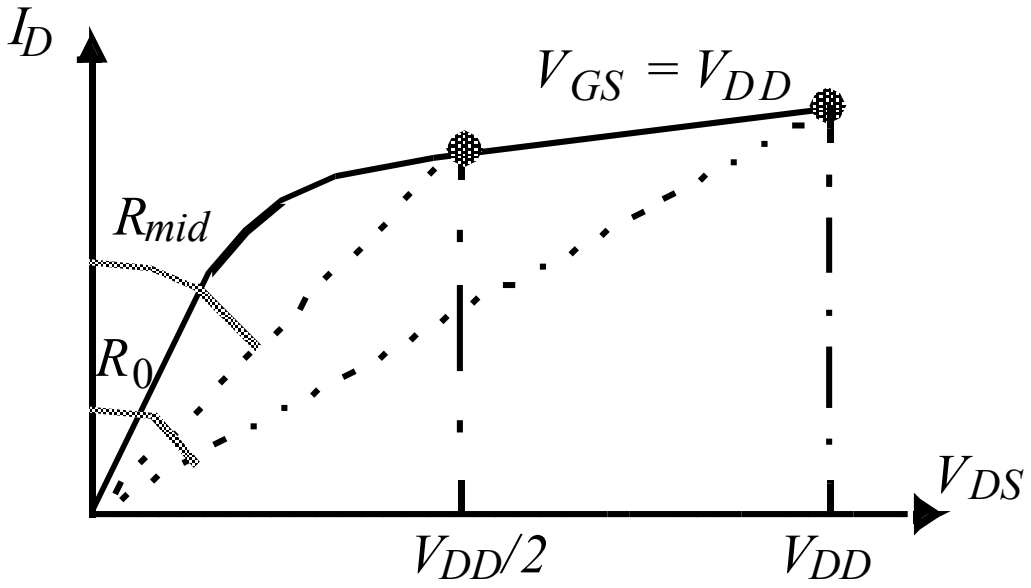
$$t_{pLH} = \ln(2) R_{eqp} C_L = 0.69 R_{eqp} C_L$$

$$t_p = \left(t_{pHL} + t_{pLH}\right)/2 = 0.69 C_L \left(R_{eqn} + R_{eqp}\right)/2$$

$\Rightarrow$ $t_{pHL} = t_{pLH}$ $\quad R_{eqn} = R_{eqp}$

a symmetrical VTC

Appendix :Equivalent Resistance

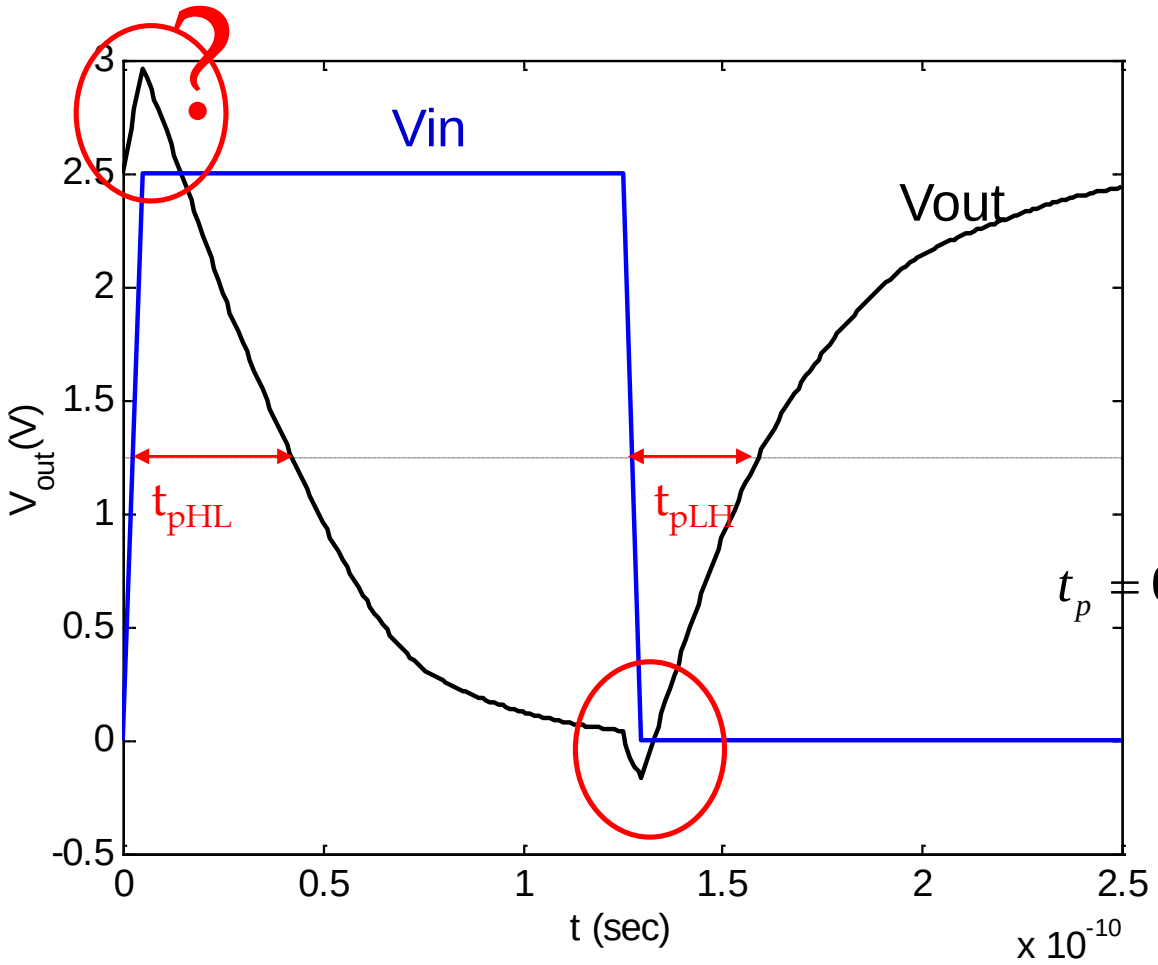


$$R_{eq} = \frac{1}{-V_{DD}/2}\int_{V_{DD}}^{V_{DD}/2} \frac{V}{I_{DSAT}(1+\lambda V)}dV \approx \frac{3}{4}\frac{V_{DD}}{I_{DSAT}}(1-\frac{7}{9}\lambda V_{DD})$$

$$R_{eq} = \frac{1}{2}\left(\frac{V_{DD}}{I_{DSAT}(1+\lambda V_{DD})} + \frac{V_{DD}/2}{I_{DSAT}(1+\lambda V_{DD}/2)}\right) \approx \frac{3}{4}\frac{V_{DD}}{I_{DSAT}}\left(1-\frac{5}{6}\lambda V_{DD}\right)$$

$$I_{DSAT} = k'\frac{W}{L}\left((V_{DD}-V_T)V_{DSAT} - \frac{V_{DSAT}^2}{2}\right)$$

Transient Response



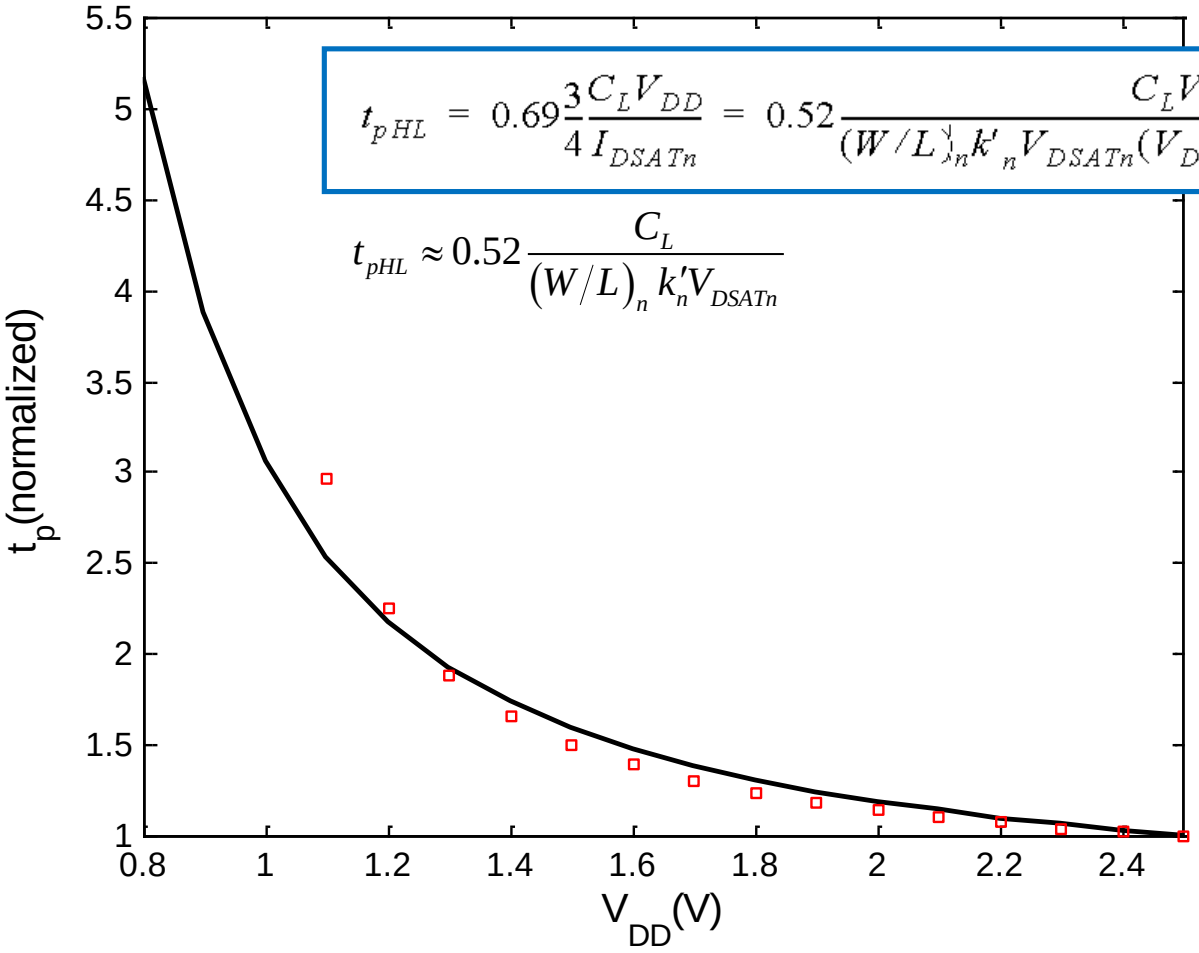
$$t_p = 0.69 C_L \left(R_{eqn} + R_{eqp} \right) / 2$$

Delay as a function of VDD

? How to manipulate or optimize the delay?

$$t_{pHL} = 0.69\frac{3}{4}\frac{C_L V_{DD}}{I_{DSATn}} = 0.52\frac{C_L V_{DD}}{(W/L)_n k'_n V_{DSATn}(V_{DD} - V_{Tn} - V_{DSATn}/2)}$$

$$t_{pHL} \approx 0.52\frac{C_L}{(W/L)_n k'_n V_{DSATn}}$$



Design for Propagation Delay

- Reduce C_L
  - internal diffusion capacitance of the gate itself
    - ⇨ *keep the drain diffusion as small as possible*
  - interconnect capacitance
  - Fanout capacitance
- Increase W/L ratio of the transistor

  the most powerful and effective performance optimization tool in the hands of the designer
  - self-loading! $C_{inc} > C_{ext}$

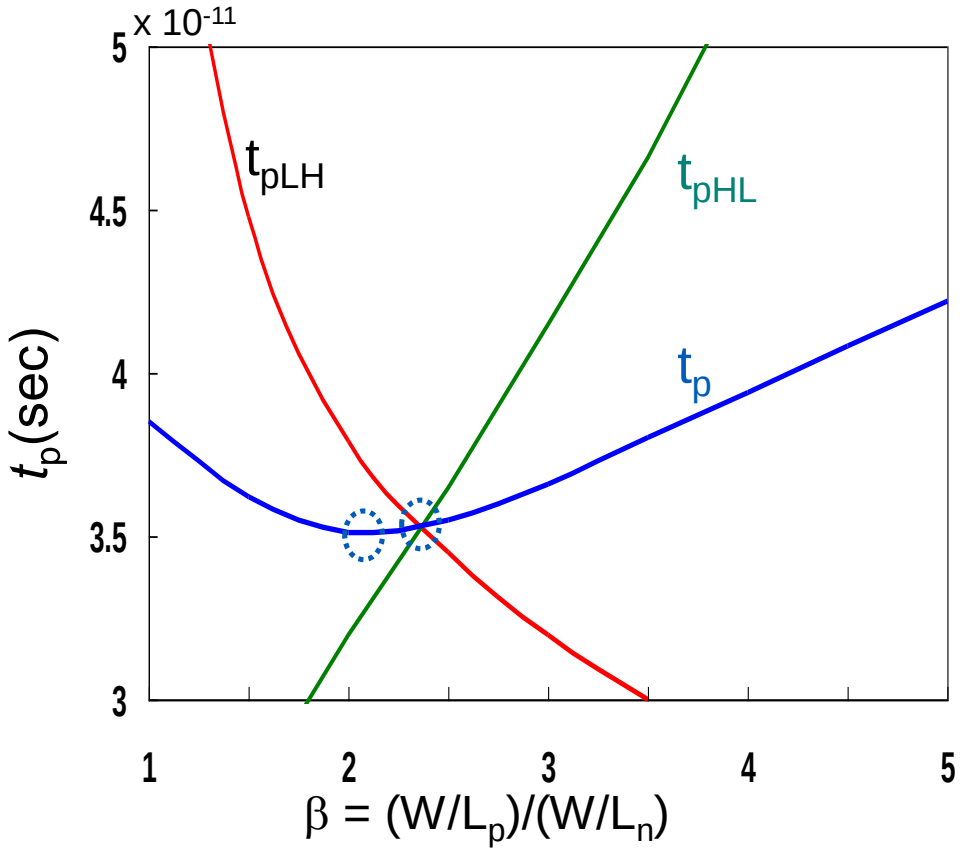
- Increase V_{DD}
  - trade-off: **energy** vs. **performance**
  - increasing V_{DD} above a certain level yields only very minimal improvements
  - reliability: oxide breakdown, hot-electron effects

Outline

- Inverter Basic Characteristics
- Static Behavior
- Dynamic Behavior
  - Propagation Delay: First-order Analysis
  - Propagation Delay from Perspective
    - ✓ NMOS/PMOS Ratio
    - ✓ Sizing Inverters for Performance
    - ✓ Sizing a Chain of Inverters and its Stage
    - ✓ Rise/fall Time of Input Signal
    - ✓ Delay in Long Interconnect Wires

NMOS/PMOS Ratio

- Symmetrical VT and t_{pHL}= t_{pLH}: β = $(W/L_p)/(W/L_n)$=3~3.5
- If speed is the only concern, reduce the width of the PMOS device



$$t_p = \left(t_{pHL} + t_{pLH}\right)/2$$

widening PMOS degrades t_{pHL} due to larger parasitic capacitance

$$\frac{\partial t_p}{\partial \beta} = 0 \Rightarrow \beta_{opt} = \sqrt{\gamma(1+\frac{C_w}{C_{dn1}+C_{gn2}})}$$

- β of 2.4 (= 31 kΩ/13 kΩ): symmetrical response
- β of 1.6 to 1.9: optimal performance

Device Sizing for Performance

- Divide capacitive load, C_L, into C_L,= C_{int}+ C_{ext}
  - C_{int}: intrinsic (self-loading) cap - diffusion and gate-drain (Miller) effect
  - C_{ext}: extrinsic load cap- wiring and fanout

    $t_p = 0.69\ R_{eq}\ C_{int}\ (1 + C_{ext}/C_{int}) = t_{p0}\ (1 + C_{ext}/C_{int})$
  - intrinsic delay (unloaded, C_{ext}=0)

    $t_{p0} = 0.69\ R_{eq}\ C_{int}$
- Size factor: S (reference gate)

$C_{int} = SC_{iref}$

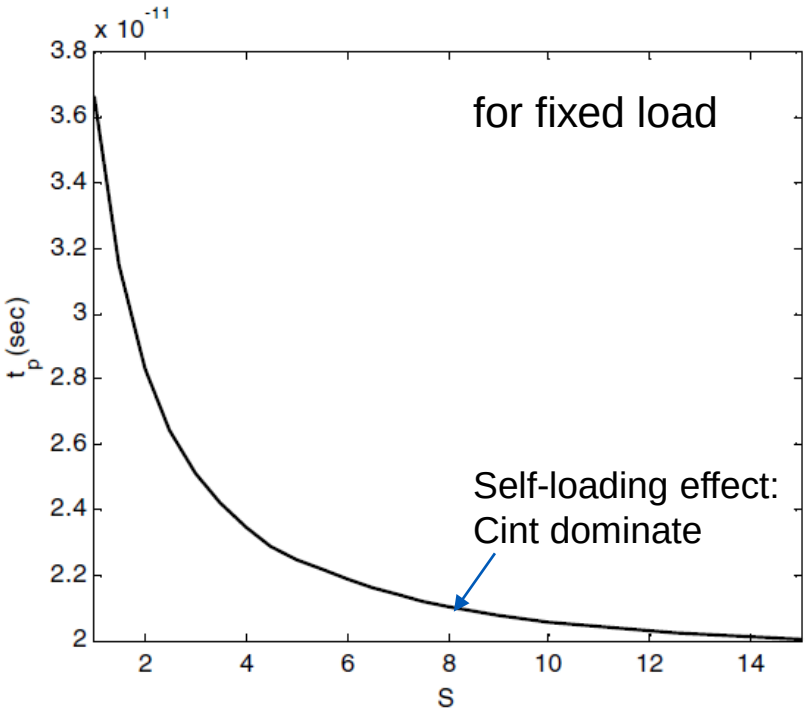
$t_p = 0.69\ R_{eq}\ C_{int}\ (1 + C_{ext}/C_{int})$

$= t_{p0}\ (1 + C_{ext}/SC_{iref})$

-- t_{p0} : the size of gate ✗

technology and layout ✓

-- S↑, t_p -> t_{p0}



Impact of Fanout on Delay

- C_{ext}: a function of the fanout of the gate

  The larger the fanout, the larger the external load.

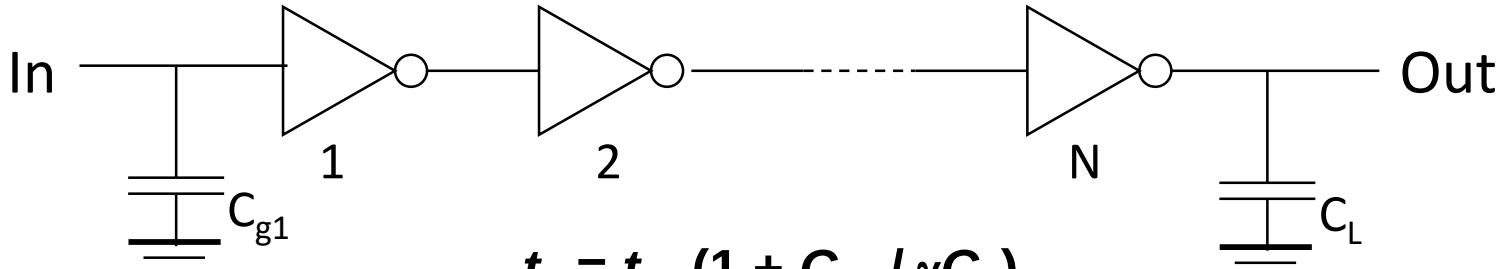
- Determine the input loading effect of the inverter.
  - Both C_g and C_{int} are proportional to the **gate sizing** $C_{int} = \gamma C_g$

    $t_p = t_{p0}(1 + C_{ext}/\gamma C_g) = t_{p0}(1 + f/\gamma)$

    the effective fan-out: $\boldsymbol{f = C_{ext}/C_g}$
  - The delay of an inverter is a function of f

Apply to Inverter Chain

- Goal: minimize the delay through an inverter chain



$$t_p = t_{p0}(1 + C_{ext}/\gamma C_g)$$

The delay of the *j*-th inverter stage:

$$t_{p,j} = t_{p0}(1 + C_{g,j+1}/(\gamma C_{g,j})) = t_{p0}(1 + f_j/\gamma)$$

and $t_p = t_{p1} + t_{p2} + \ldots + t_{pN}$ ⇨ $t_p = \Sigma t_{p,j} = t_{p0} \Sigma (1 + C_{g,j+1}/(\gamma C_{g,j}))$

$$\frac{\partial t_p}{\partial C_{g,j}} = 0 \Rightarrow C_{g,j+1}/C_{g,j} = C_{g,j}/C_{g,j-1}$$

$$C_{g,j} = \sqrt{C_{g,j-1} C_{g,j+1}}$$

- The optimum size of each inverter is the **geometric mean of its neighbors sizes**.

Apply to Inverter Chain

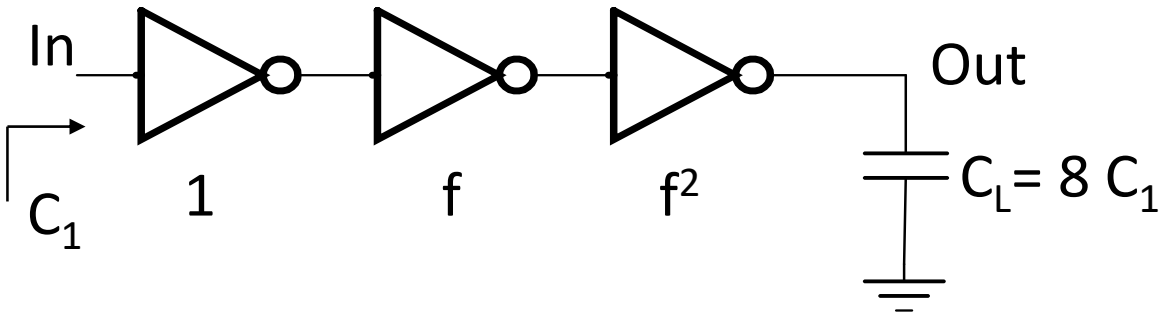
- The optimum size of each inverter will have the same effective fan-out and the same delay $f = \sqrt[N]{C_L / C_{g,1}} = \sqrt[N]{F}$

  F: the overall effective fan-out of the circuit ($F = C_L/C_{g,1}$)

- The minimum delay through the inverter chain is

$$t_p = N t_{p0} \left(1 + \sqrt[N]{F} / \gamma\right)$$

Example



C_L/C_1 has to be evenly distributed across N = 3 stages: $f = \sqrt[3]{8} = 2$

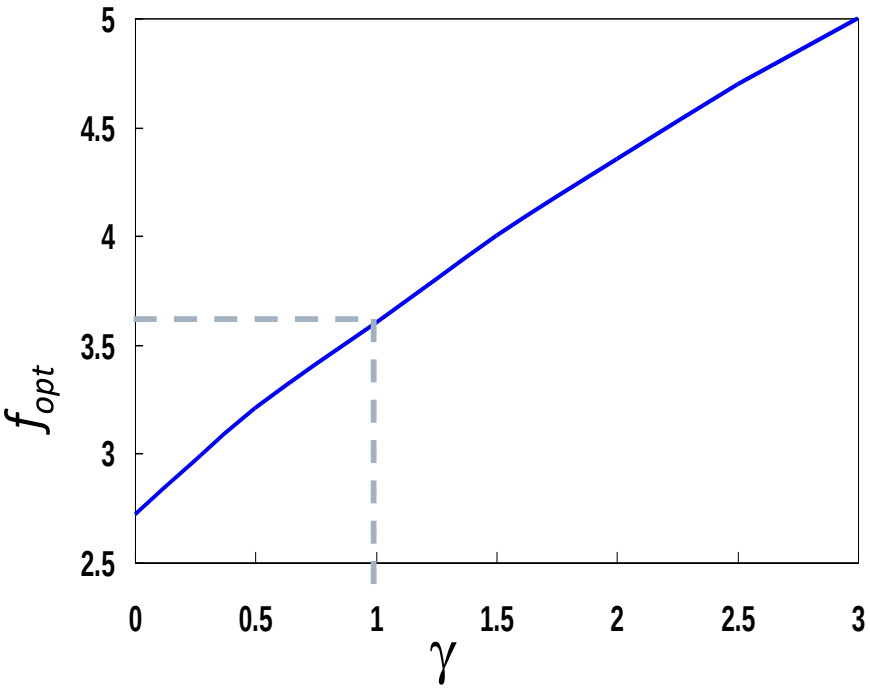
Optimum Stages *N* in Inverter Chain

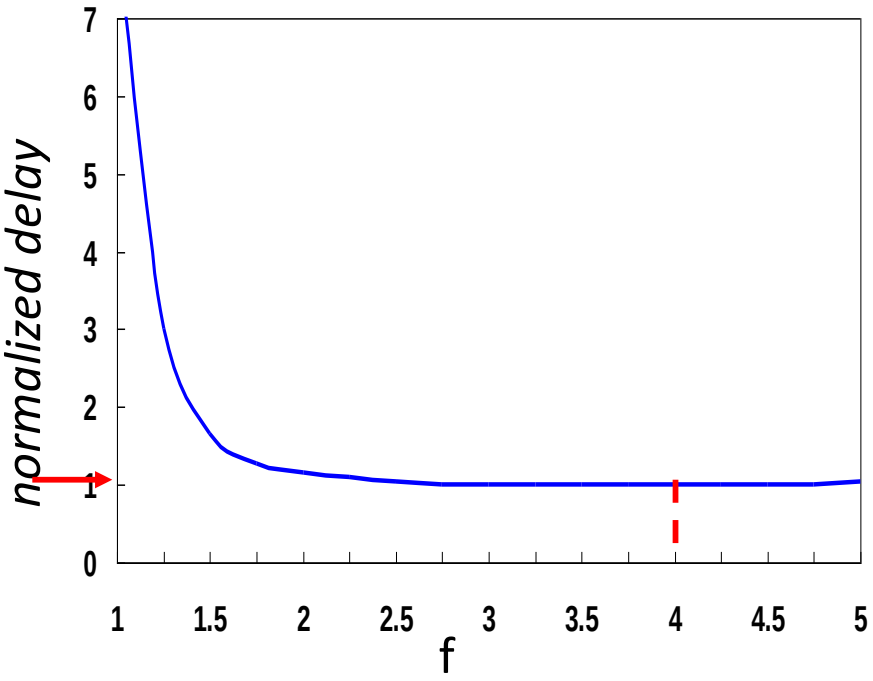
- What is the optimal value for *N* given *F* (=f^N) ?

$$t_p = Nt_{p0}\left(1+\sqrt[N]{F}/\gamma\right) \qquad f = \exp\left(1+\gamma/f\right)$$

  - if *N* is too large, the **intrinsic delay** of the stages becomes dominate
  - if *N* is too small, the **effective fan-out** of each stage becomes dominate
  - The optimal number of stages: ***N* = ln(*F*)**
    the effective fanout of each stage *f* = 2.71828 = *e*

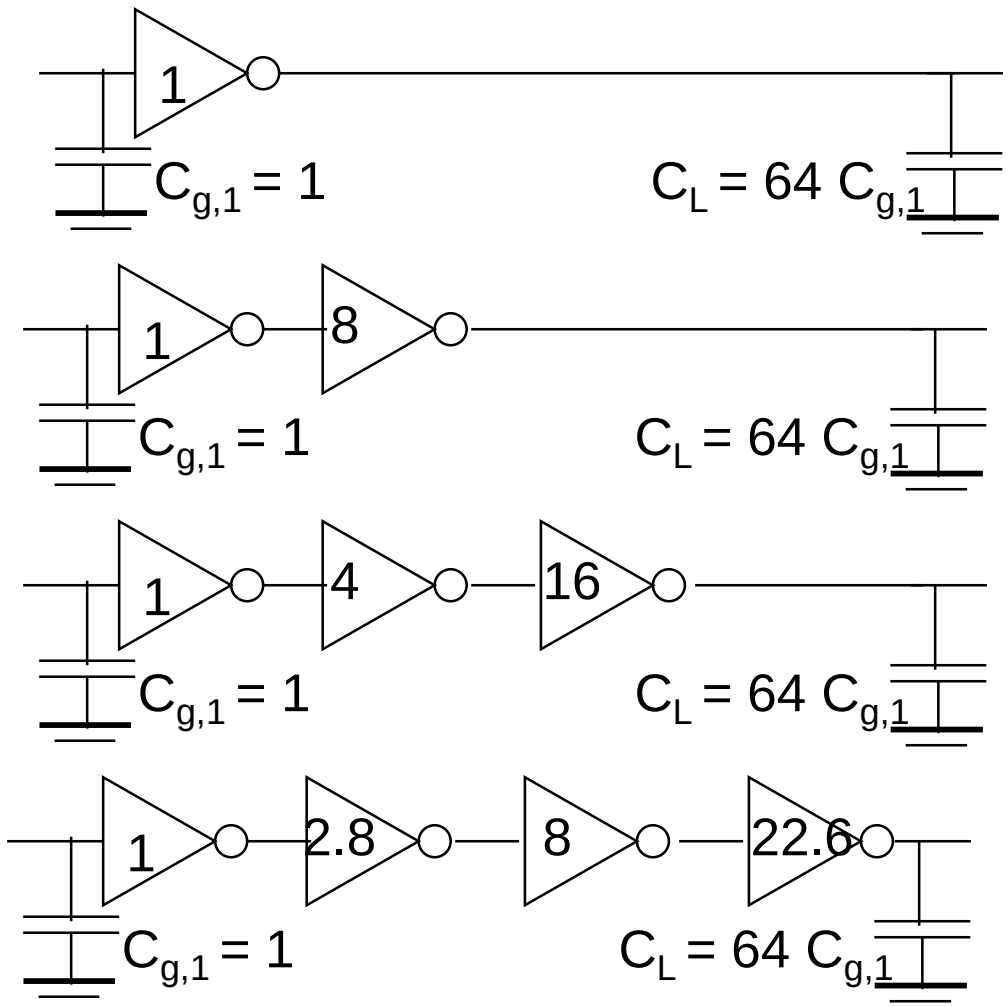
Optimum Effective Fan-Out





- Choosing f larger than optimum has little effect on delay and reduces the number of stages (and area).
  - **Common practice to use: f = 4 (for γ = 1)**
  - But too many stages has a substantial negative impact on delay

Example：Inverter (Buffer) Staging



$$t_p = N * t_{p0}(1 + f_j/\gamma)$$

N	f	t_p
1	64	65
2	8	18
3	4	15
4	2.8	15.2

$$f = \sqrt[N]{F}$$

Example: Impact of Buffer Staging

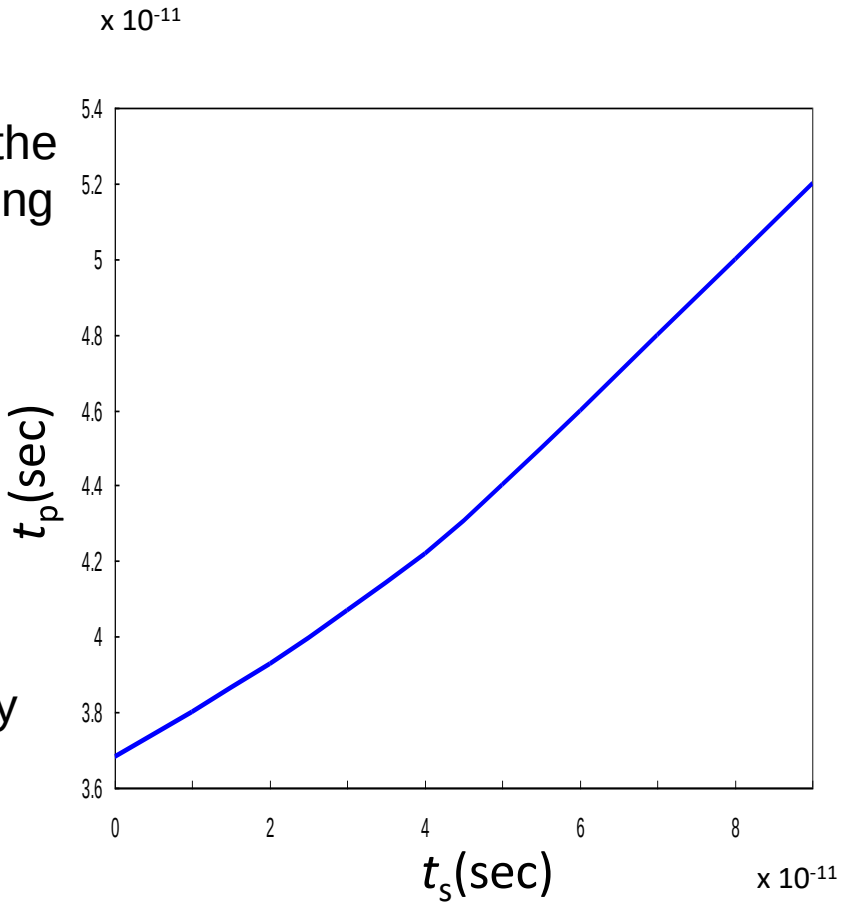
$t_{p,opt}/t_{p0}$	F (γ = 1)	Unbuffered	Two Stage Chain	Opt. Inverter Chain
	10	11	8.3	8.3
	100	101	22	16.5
	1,000	1001	65	24.8
	10,000	10,001	202	33.1

$$t_p = Nt_{p0}\left(1+\sqrt[N]{F}/\gamma\right)$$

When driving very large C_L, the impressive speed-up obtained with cascaded inverters.

Input Signal Rise/Fall Time

- In reality, the input signal changes gradually (and both PMOS and NMOS conduct for a brief time). This affects the current available for charging/discharging C_L and impacts propagation delay.



for a minimum-size inverter with a fan-out of a single gate

- t_p increases linearly with increasing input slope, t_s, once $t_s > t_p$
- t_s is due to the limited driving capability of the preceding gate

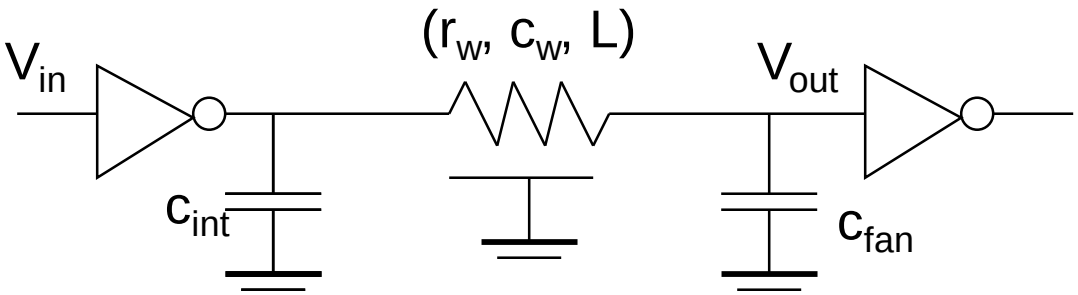
$$t_p^i = t_{step}^i + \eta t_{step}^{i-1}$$

Design Challenge

- Keep signal rise times smaller than or equal to the gate propagation delays.
  - Good for performance
  - Good for power consumption
- Keep rise and fall times of the signals small and of approximately equal values is one of the major challenges in high-performance designs - slope engineering.

Delay with Long Interconnects

- When gates are farther apart, wire capacitance and resistance can no longer be ignored.



$$t_p = 0.69R_{dr}C_{int} + (0.69R_{dr}+0.38R_w)C_w + 0.69(R_{dr}+R_w)C_{fan}$$
$$= 0.69R_{dr}(C_{int}+C_{fan}) + 0.69(R_{dr}c_w+r_wC_{fan})L + 0.38r_wc_wL^2$$

where $R_{dr} = (R_{eqn} + R_{eqp})/2$

Wire delay rapidly becomes the dominate factor (due to the quadratic term) in the delay budget for longer wires.

Add buffer per > 200μm wire

Outline

- Inverter Basic Characteristics
- Static Behavior
- Dynamic Behavior
- Power, Energy
  - Dynamic Power Consumption
  - Static Consumption

Where Does Power Go?

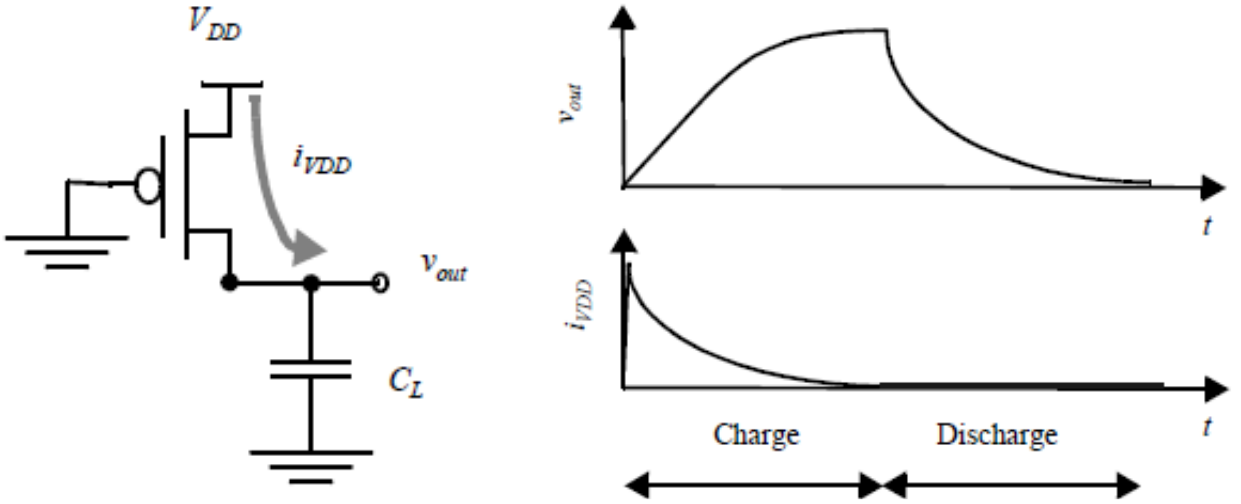
- Dynamic Power: $P_{dynamic} = P_{switching} + P_{shortcircuit}$
  - Charging and Discharging Capacitors
  - Short Circuit Currents: Short Circuit Path between Supply Rails during Switching
- Static Power: $P_{static} = (I_{sub} + I_{junct} + I_{gate})V_{DD}$
  - Leakage Static Consumption: OFF devices

    Subthreshold Leakage

    Junction Leakage

    Gate Leakage

Dynamic Power Consumption



- When the gate output rises

$$E_{VDD} = \int_0^\infty i_{VDD} V_{DD} dt = \ldots = C_L V_{DD}^{\ 2}$$

taken from the supply during the transition.

$$E_C = \int_0^\infty i_{VDD} V_{out} dt = \ldots = C_L V_{DD}^{\ 2} / 2$$

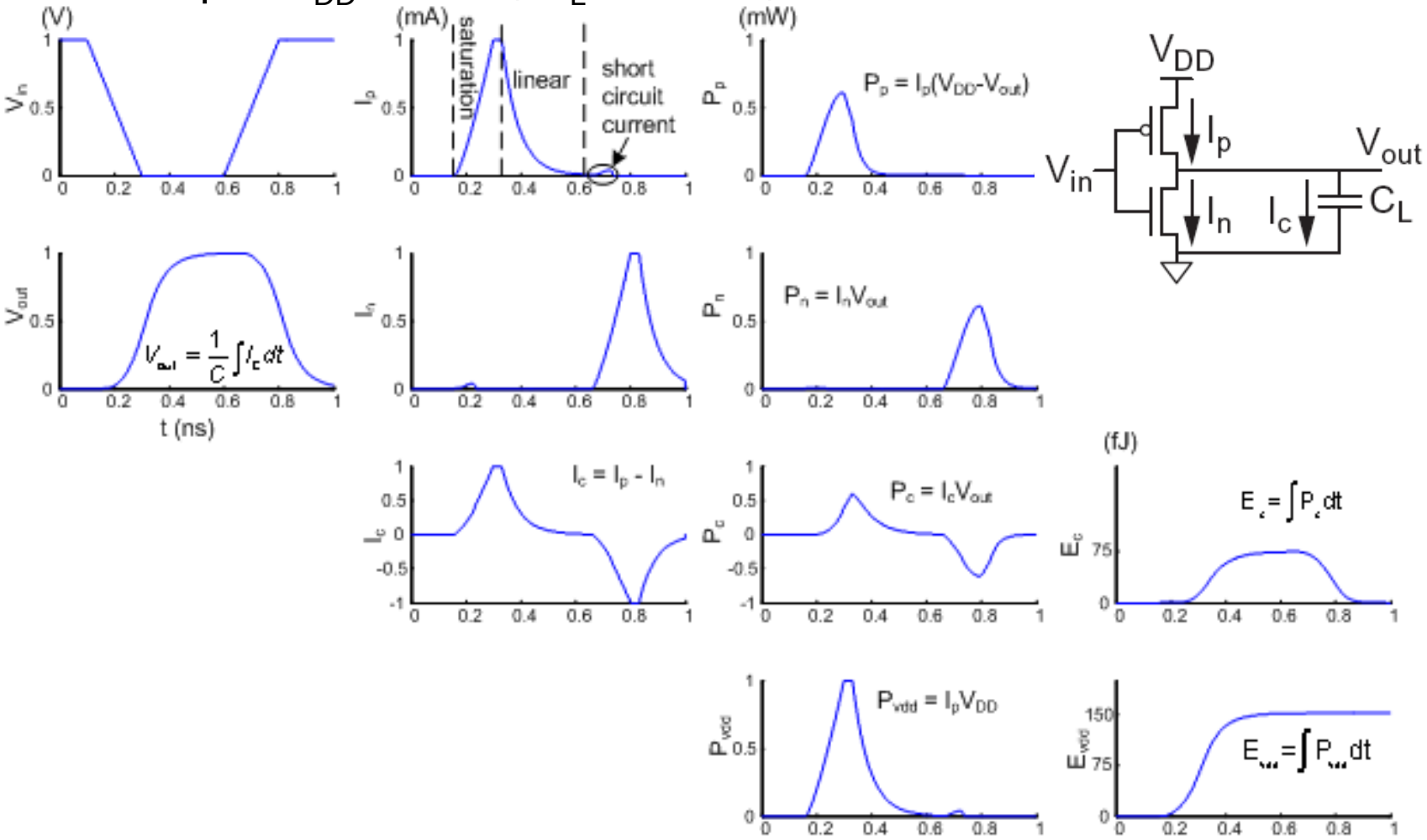
stored on the capacitor at the end of the transition

Half the energy from V_{DD} is dissipated in the PMOS transistor as heat, other half stored in capacitor

- When the gate output falls
  - -- Energy in capacitor is dumped to GND
  - -- Dissipated as heat in the nMOS transistor

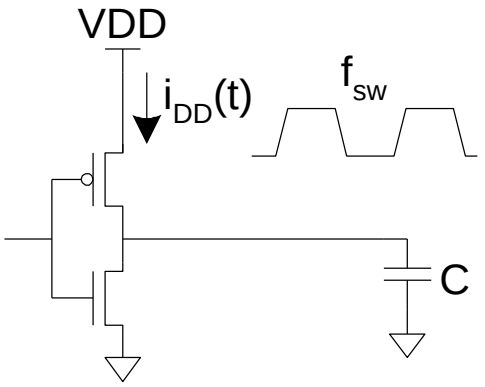
Switching Waveforms

- Example: V_{DD} = 1.0 V, C_L = 150 fF, f = 1 GHz



Switching Power and Activity Factor

$$P_{\text{switching}} = \frac{1}{T}\int_0^T i_{DD}(t)V_{DD}dt = \frac{V_{DD}}{T}\int_0^T i_{DD}(t)dt = \frac{V_{DD}}{T}\left[Tf_{\text{sw}}CV_{DD}\right]$$
$$= CV_{DD}{}^2 f_{\text{sw}}$$



Suppose the system clock frequency = f, $f_{sw} = \alpha f$ (a = activity factor)

If the signal is a clock, a = 1

If the signal switches once per cycle, a = ½

$$P_{\text{switching}} = \alpha CV_{DD}{}^2 f$$

$$P_{dyn} = C_L V_{DD}{}^2 f_{0->1}$$

the power consumption as the gate is switched on and off times per second

Switching activity开关活动性

Switching Power

Capacitance: function of fanout, wire length, transistor sizes

Supply voltage: scaling with generations

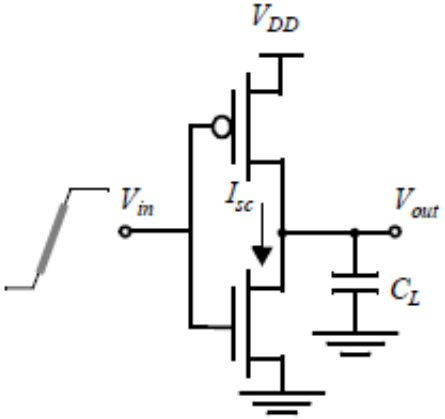
$$P_{\text{switching}} = \alpha C V_{DD}^{\ 2} f$$

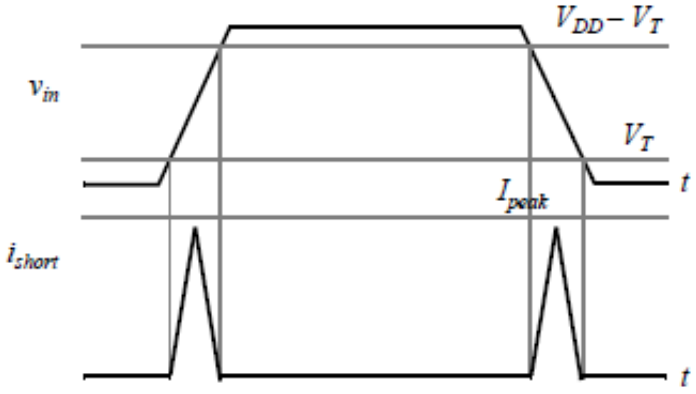
Activity factor: how often on average wires switch

Clock frequency: scaling with generations

Dissipation Due to Direct-Path Currents

- In actual designs, the assumption of the of the input wave forms is not correct. **zero rise and fall times**
- The finite slope of the input signal causes a **direct current** path between VDD and GND for a short period of time during switching, while the NMOS and PMOS are conducting simultaneously.
  - Leads to a blip of "short circuit" current.



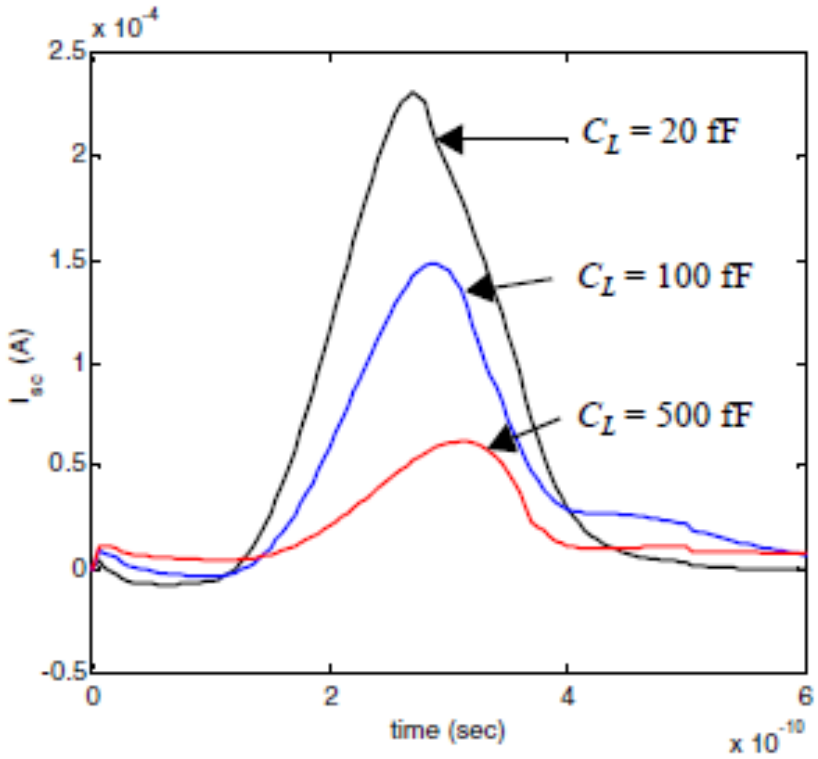


$$E_{dp} = t_{sc} V_{DD} I_{peak}$$

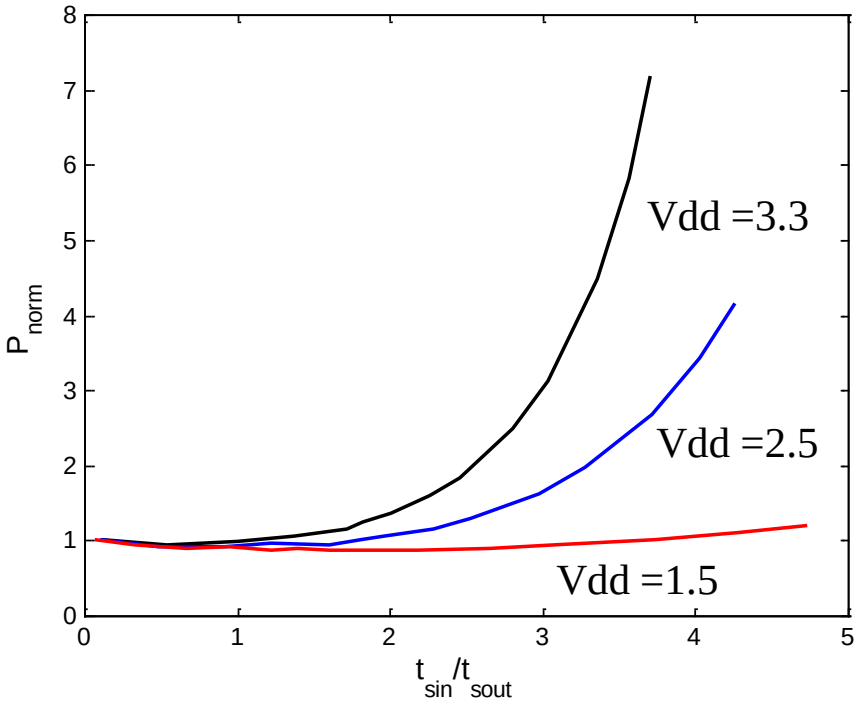
$$P_{dp} = t_{sc} V_{DD} I_{peak} f = C_{sc} V_{DD}{}^2 f$$

$$t_{sc} = \frac{V_{DD} - 2V_T}{V_{DD}} t_s$$

Short Circuit Currents



I_{peak} depends on the saturation current of P/N MOS and the ration between input and output slopes (C_L)



- Keep the input and output rise/fall times the same
- If Vdd < Vtn + |Vtp|, the short circuit power is eliminated since **both devices are never on at the same time**

Dynamic Power Example

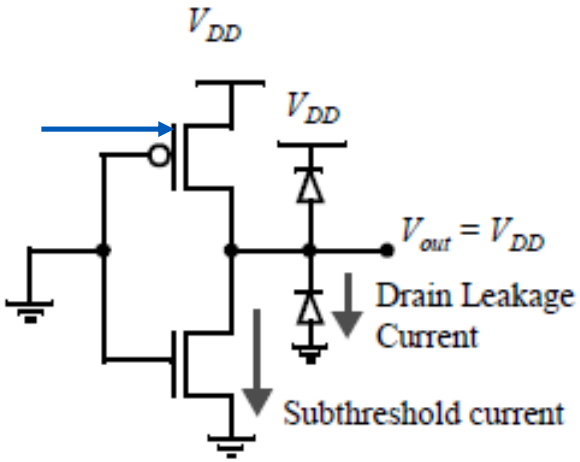
- 1 billion transistor chip
  - 50M logic transistors
    - Average width: 12 λ
    - Activity factor = 0.1
  - 950M memory transistors
    - Average width: 4 λ
    - Activity factor = 0.02
  - 1.0 V 65 nm process (with 50 nm drawn channel lengths and λ= 25 nm)
  - C = 1 fF/mm (gate) + 0.8 fF/mm (diffusion)
- Estimate dynamic power consumption @ 1 GHz. Neglect wire capacitance and short-circuit current.

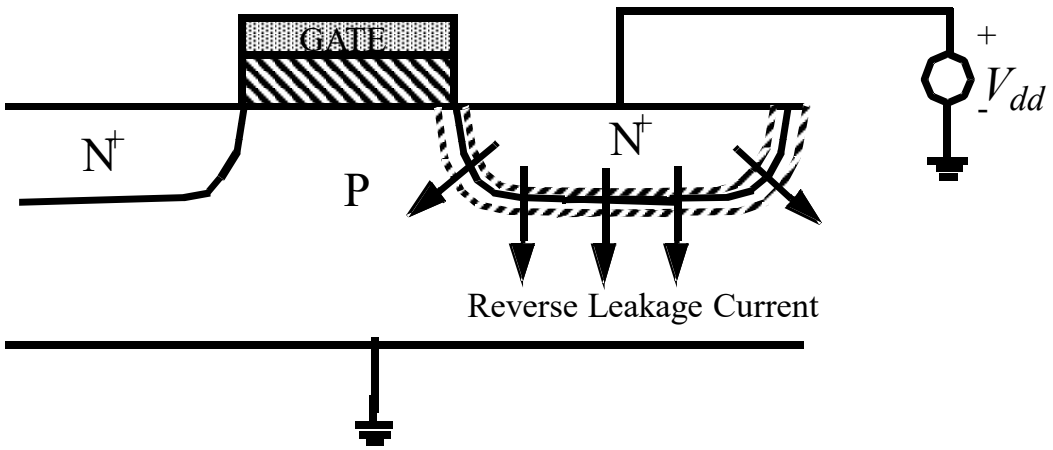
$$C_{\text{logic}} = \left(50\times10^{6}\right)\left(12\lambda\right)\left(0.025\mu m/\lambda\right)\left(1.8\,fF/\mu m\right) = 27\ \text{nF}$$

$$C_{\text{mem}} = \left(950\times10^{6}\right)\left(4\lambda\right)\left(0.025\mu m/\lambda\right)\left(1.8\,fF/\mu m\right) = 171\ \text{nF}$$

$$P_{\text{dynamic}} = \left[0.1C_{\text{logic}} + 0.02C_{\text{mem}}\right]\left(1.0\right)^{2}\left(1.0\ \text{GHz}\right) = 6.1\ \text{W}$$

Static Consumption



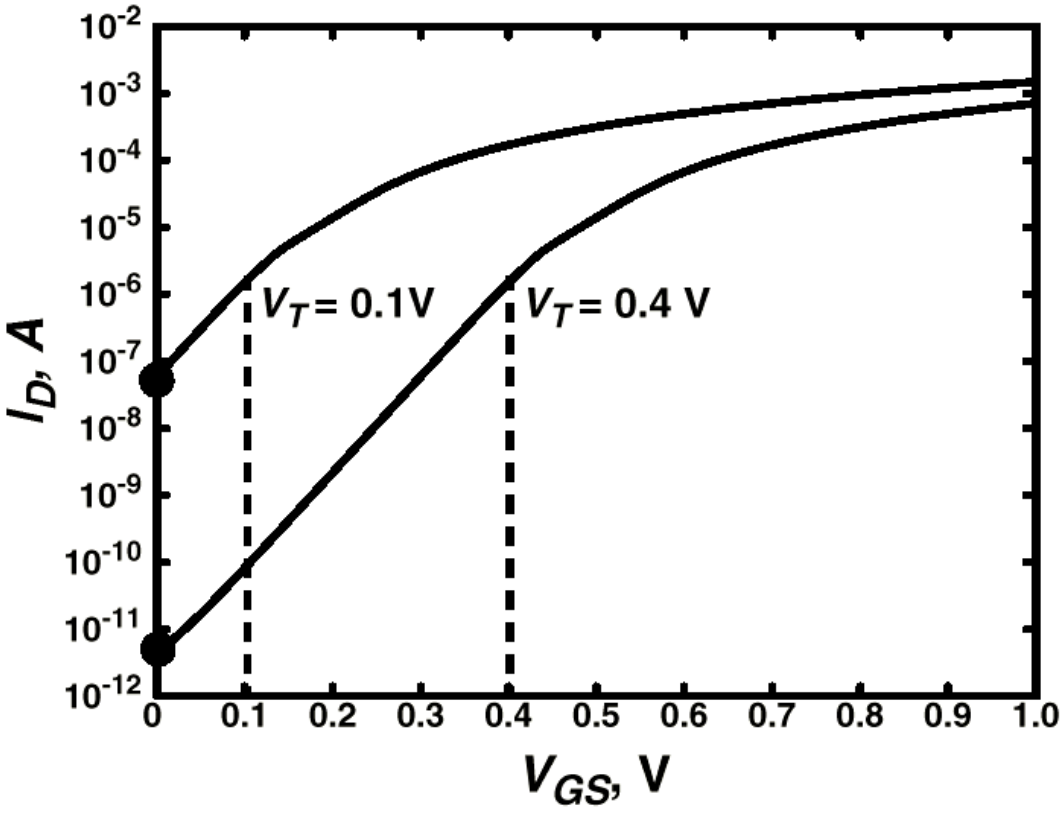


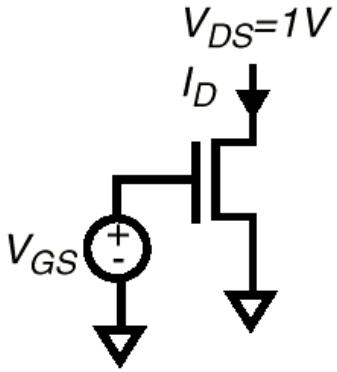
Sub-threshold current one of most compelling issues in low-energy circuit design!

Typical values in 65 nm
I_{off} = 100 nA/μm @ V_t = 0.3 V
I_{off} = 10 nA/μm @ V_t = 0.4 V
I_{off} = 1 nA/μm @ V_t = 0.5 V
η = 0.1 k_γ = 0.1
S = 100 mV/decade

Tunneling leakage from reverse-biased p-n junctions
-- Between diffusion and substrate or well

Static Consumption





Leakage control is critical for low-voltage operation

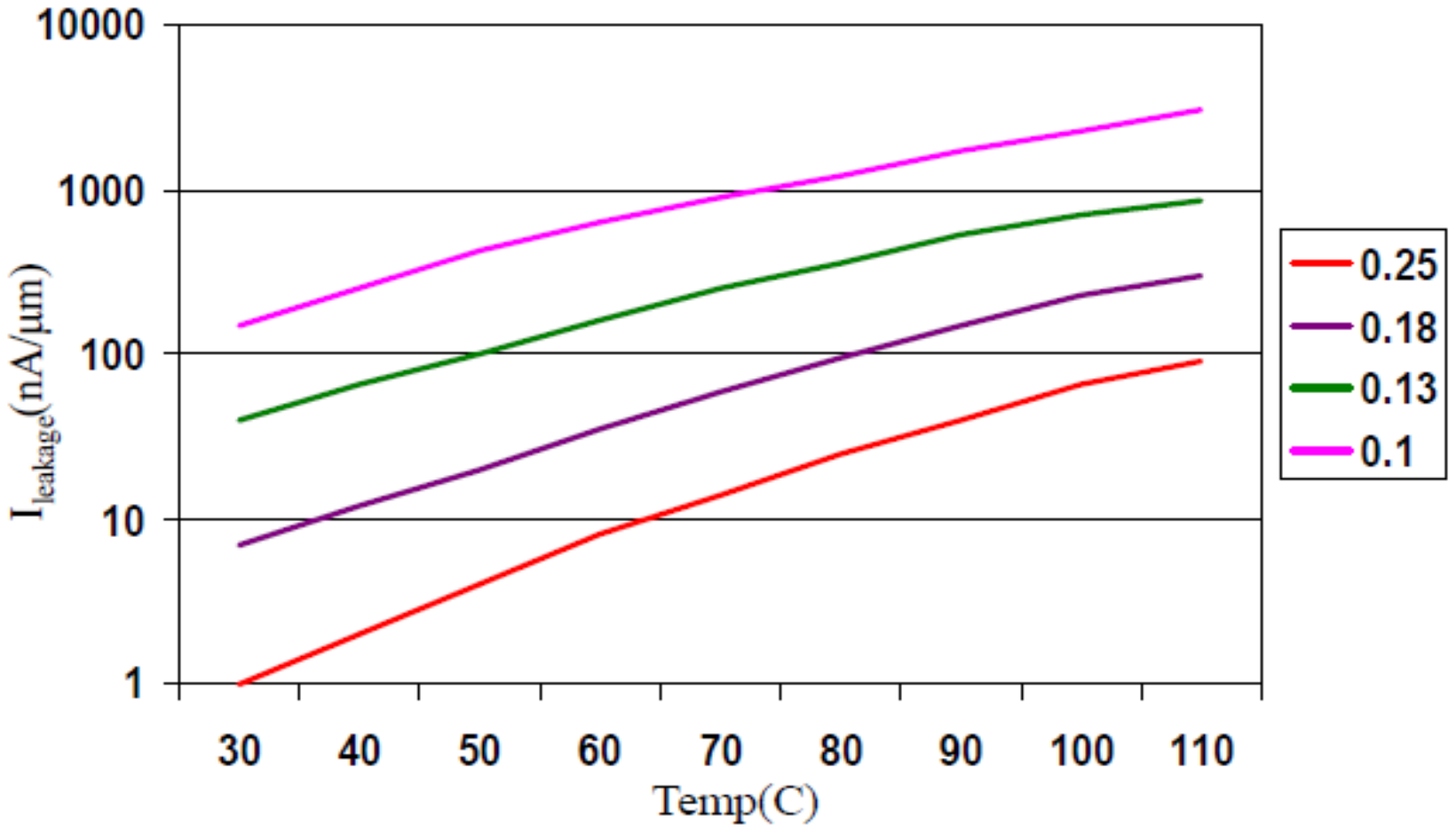
Leakage Dependence on Vt

TSMC Processes Leakage and Vt

	CL018 G	CL018 LP	CL018 ULP	CL018 HS	CL015 HS	CL013 HS
V_{dd}	1.8 V	1.8 V	1.8 V	2 V	1.5 V	1.2 V
T_{ox} (effective)	42 Å	42 Å	42 Å	42 Å	29 Å	24 Å
L_{gate}	0.16 µm	0.16 µm	0.18 µm	0.13 µm	0.11 µm	0.08 µm
I_{DSat} (n/p) (µA/µm)	600/260	500/180	320/130	780/360	860/370	920/400
I_{off} (leakage) (pA/µm)	20	1.60	0.15	300	1,800	13,000
V_{Tn}	0.42 V	0.63 V	0.73 V	0.40 V	0.29 V	0.25 V
FET Perf. (GHz)	30	22	14	43	52	80

Exponential dependence

Leakage Dependence on Temperature



Source: D. Borkar, Intel

Putting it all together

$$P_{total} = P_{dyn} + P_{dp} + P_{stat}$$

become more and more important

$$= (C_L V_{DD}^{\ 2} + V_{DD} I_{peak} t_s) f_{0->1} + V_{DD} I_{leak}$$

the dominant factor

can be kept within bounds
by careful design

Summary

- Inverter Basic Characteristics
- Static Behavior
  - Voltage transfer Characteristics
  - Switching threshold
- Dynamic Behavior
  - Propagation Delay: First-order Analysis
  - Propagation Delay from Perspective
- Power, Energy

集成电路原理与设计

11. 反相器

宋爽

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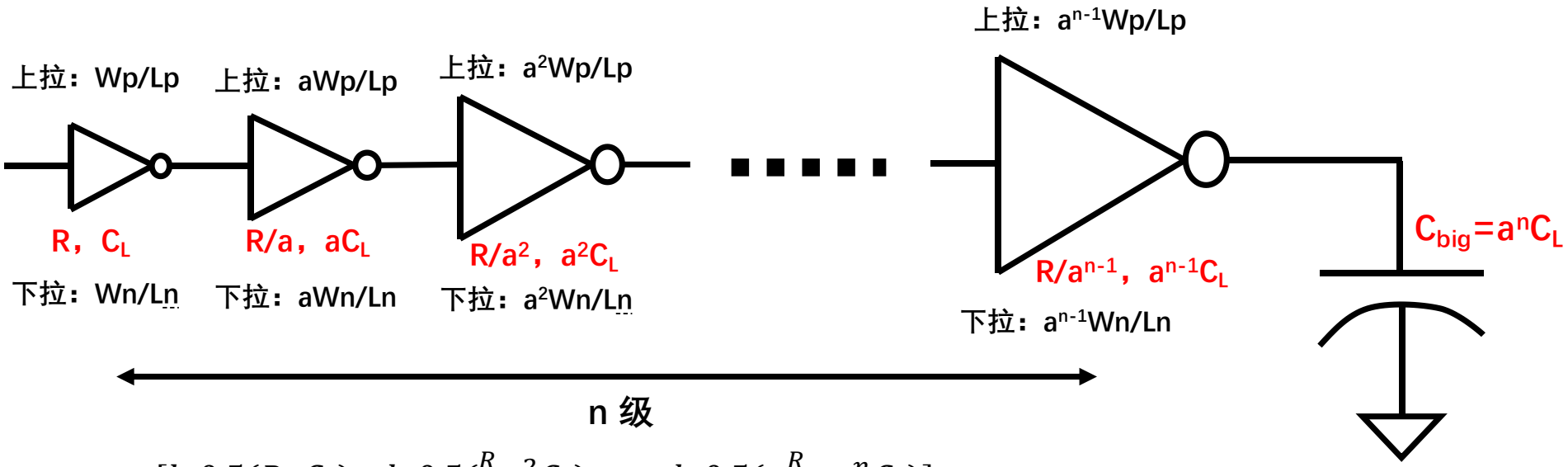
Cascaded driver circuit



$$t_{tot} = -[ln0.5(RaC_L) + ln0.5(\frac{R}{a}a^2C_L) + \cdots + ln0.5(\frac{R}{a^{n-1}}a^nC_L)]$$
$$= -naln0.5(RC_L)$$
$$= nat_{min}$$
$$= n(\frac{C_{big}}{C_L})^{\frac{1}{n}} t_{min} \xrightarrow{\text{求最小值}} \frac{dt_{tot}}{dn} = 0 \xrightarrow{\text{最佳级数}} n_{opt} = \ln(\frac{C_{big}}{C_L}) = lna^n \xleftarrow{\text{最优值}} a = e$$

Optimal sizing

- Use a chain of inverters, each stage has transistors a larger than previous stage.
- Minimize total delay through driver chain:
  - $t_{tot} = n(C_{big}/C_g)^{1/n} t_{min}$.
- Optimal number of stages:
  - $n_{opt} = \ln(C_{big}/C_g)$.
- Driver sizes are exponentially tapered with size ratio a.

Layout example of buffers insertion