期末复习

2024. 1. 8

考试题型

- 名词解释：6*2分 = 12 分 （IC CMOS PMOS NMOS …）
- 选择：　　11*2分 = 22 分
- 解答题：　5*X分 = 66 分 （Analog 2, Digital 2, Layout 1）
  - 模拟小信号模型与计算
  - 看版图，从版图画出 Schematic
  - 从布尔函数到数字逻辑门
  - 多输入逻辑门延时计算

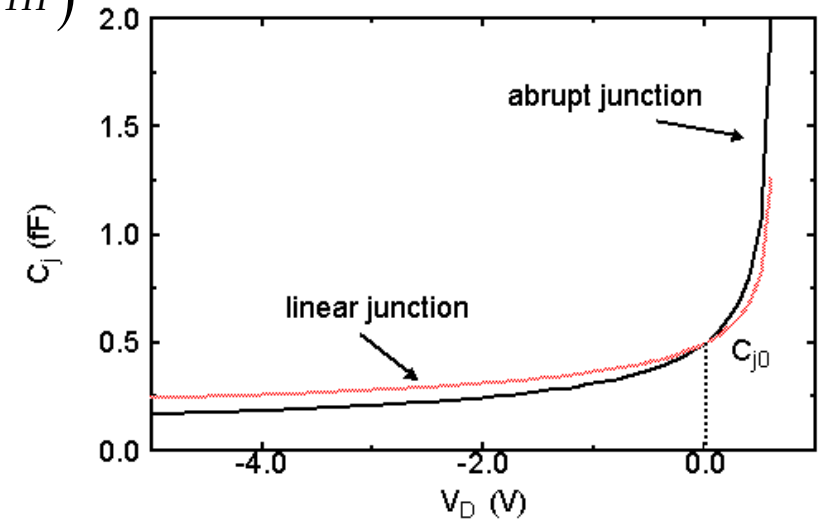
主要内容（1）

- Technology scaling down (digital driven) with Moore's Law
  But in recent decade more SoC, SiP and Chiplets
- Analog & Digital Design Flow (Transistor level vs. Behavior-RTL)
- Analog vs. Digital with technology scaling down
- I/V curve and operation region of MOSFET

$$I_D = \mu_n C_{OX} \frac{W}{L}\left[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2\right] \qquad I_D = \frac{1}{2}\mu_n C_{OX} \frac{W}{L}(V_{GS} - V_{TH})^2$$

- Diode and its capacitance

$$C_j = \frac{C_{j0}}{(1 - V_D/\phi_0)^m}$$



主要内容（2）

- **Body Effect & Channel Length Modulation & Weak inversion**

$$V_{TH} = V_{TH0} + \gamma\left(\sqrt{|2\Phi_F + V_{SB}|} - \sqrt{|2\Phi_F|}\right)$$

$$I_D \approx \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{GS} - V_{TH}\right)^2\left(1 + \lambda V_{DS}\right)$$

$$I_D = I_O \exp\frac{V_{GS}}{\varsigma V_T}$$

- **Small Signal Model**

  管子是一个压控电流源，主要由Vgs控制，受到Vds的影响

Single-Page MOSFET Model

$$I_{DS} = K'_n \frac{W}{L} (V_{GS}-V_T)^2 \qquad V_{GS}-V_T \approx 0.2\ V \qquad K'_n \approx 100\ \mu A/V^2,\ K'_p \approx 40\ \mu A/V^2$$

$$K'_n = \frac{1}{2}\mu_n C_{ox}$$

$$g_m = 2K'_n \frac{W}{L} (V_{GS}-V_T) = 2\sqrt{K'_n \frac{W}{L} I_{DS}} = \frac{2\,I_{DS}}{V_{GS}-V_T}$$

$$r_{DS} = r_o = \frac{V_E L}{I_{DS}} \qquad V_{En} \approx 5\ V/\mu mL\ \ V_{Ep} \approx 8\ V/\mu mL$$

$$r_O = \frac{1}{I_D \lambda}$$

$$v_{sat} = 10^7\ cm/s$$

$$f_T = \frac{1}{2\pi}\frac{3}{2n}\frac{\mu}{L^2}(V_{GS}-V_T) \quad \text{or now} \approx \frac{v_{sat}}{2\pi L}$$

$$f_T = \frac{g_m}{2\pi C_{GS}}$$

Willy Sansen 10-05 0170

主要内容（3）

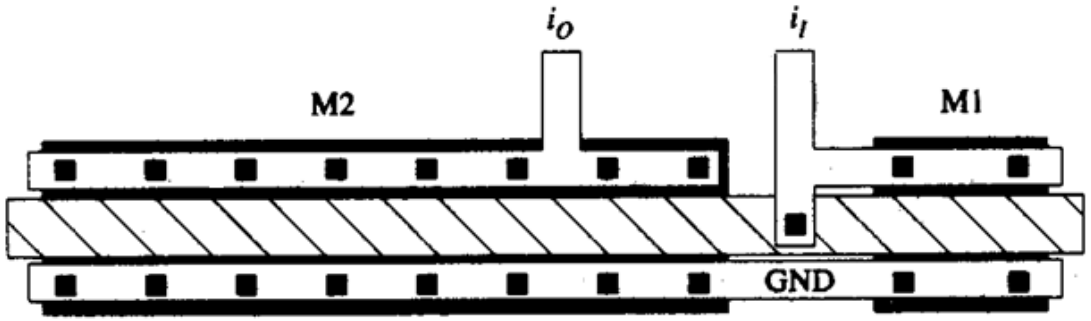
- PVT variation of parameters: (+) R, g_m, speed… (-) Vth, Vbe…
- Process Steps:

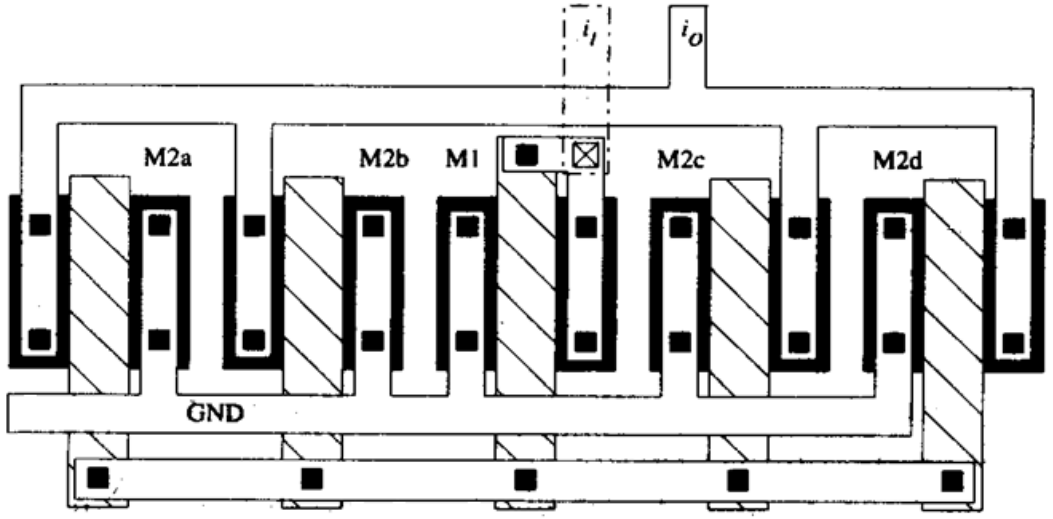
1. Wafer preparation
2. **Lithography** (defines the geometry)
3. Oxidation,
4. Diffusion, Ion immolations, Deposition
5. Etching **(2-5)不断循环**
6. Planarization

- DRC (minimum distance, matching etc.) LVS (Layout vs Schematic)

主要内容（4）

- Layout: from Layout to schematic
- Matching: **identical cells** are good for matching
  (用多个一样的-电流镜)





- Two dimensional matching (交差摆放-差分对)

主要内容（5）

$$r_{ON} = \left.\frac{1}{\partial i_D / \partial v_{DS}}\right|_Q = \frac{L}{K'W(V_{GS} - V_{TH} - V_{DS})}$$

- Switch (charge feedthrough) in linear:
- Active resistor (diode connected transistor) in saturation (1/gm)

- Current mirror: 一个由二极管连接的管子控制栅极的管子：rds

- Cascode current mirror：输出阻抗被提升至 rds 的 （gm*rds）倍 gm*rds 为上面管子的本征增益，PMOS则相反，为下面管子

- 一些电压关系计算，压低最小输出电压

主要内容（6）

- **Common-Source Stage**

  - Inverse Gain -> I-V curve （why $R_D < r_o$ of transistor）

  - 增益等于输入管gm*输出节点的阻抗（上下并联）

- **Source Follower**

  Gm = gm/(1+gm* R_S)

  With high output resistance
  Similar to Cascode

- **Common-Gate Stage**

  Current input with (1/gm) -> Iout = Iin

  With low input resistance: 1/gm

主要内容（7）

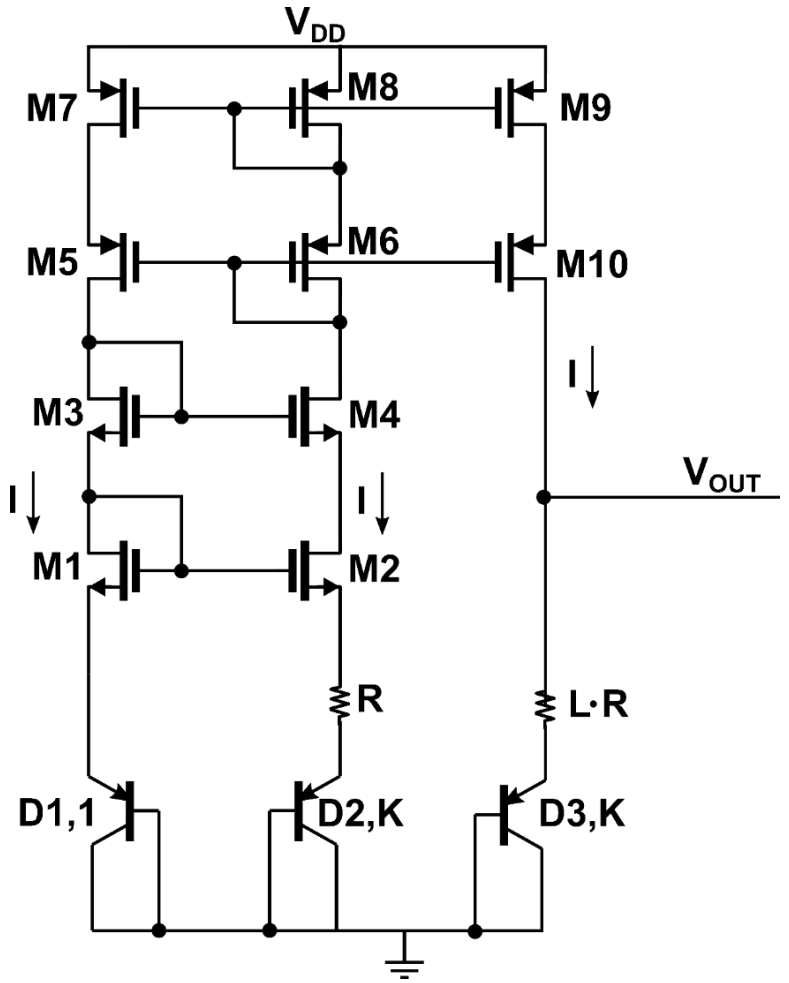
- **Bandgap reference (ZTC = PTAT+CTAT)**

$$V_{REF} = V_{BE} + KV_t$$

$$V_{ref} = V_{EB3} + I \times LR$$

$$= V_{EB3} + \frac{V_t \ln K}{R} \times LR$$

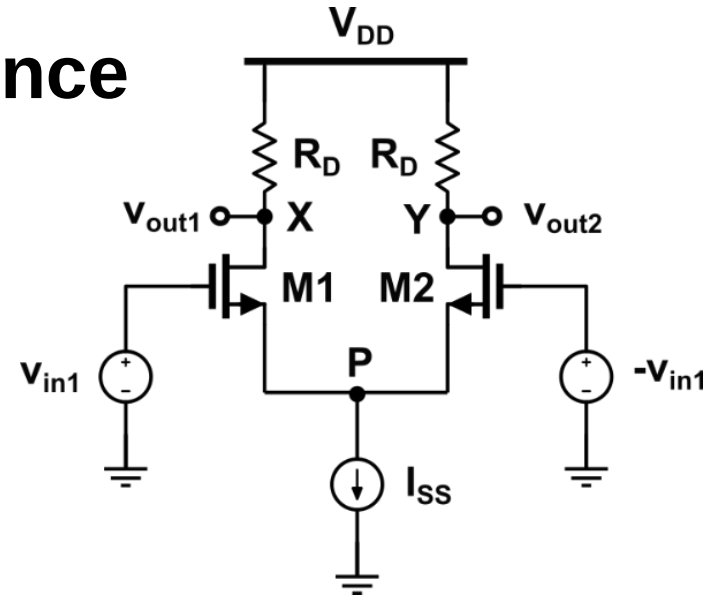
$$= V_{EB3} + LV_t \ln K$$



主要内容（8）

- **A differential signal is better in PSRR/Interference**
- **Virtual ground at node P with fixed I_{SS}**
- **V_{incm} Range:** $V_{GS1} + (V_{GS3} - V_{TH3}) \le V_{in,CM} \le V_{DD} - R_D \frac{I_{SS}}{2} + V_{TH3}$
- **DM small signal gain: $-G_m * R_{out}$**

  增益等于输入管gm*输出节点的阻抗（上下并联）
- **CM small signal gain: $(g_m/1+g_m r_{ss}) * R_{out}$**
- **OTA with five transistors**



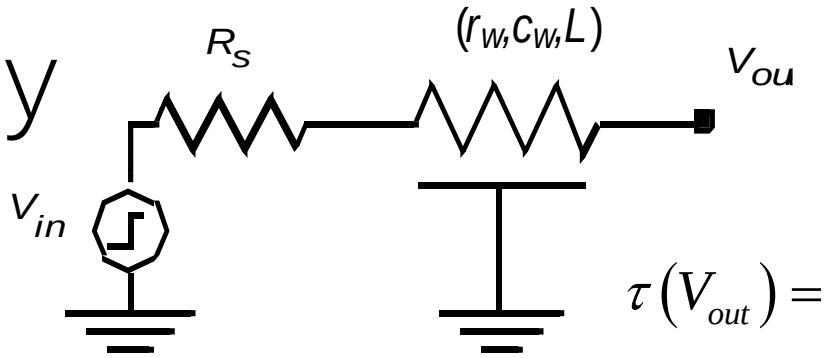
主要内容（9）运算放大器一般性了解即可

- Ideal Opamp
- DC gain and dominant pole of single stage, telescopic and folded-cascade amplifier
- DC gain and two poles of two stage amplifier, after miller compensation
- Input and output range

  (every transistor in saturation)
- Speed and Slew rate

  (small signal and large signal behavior)

主要内容（10）Elmore delay

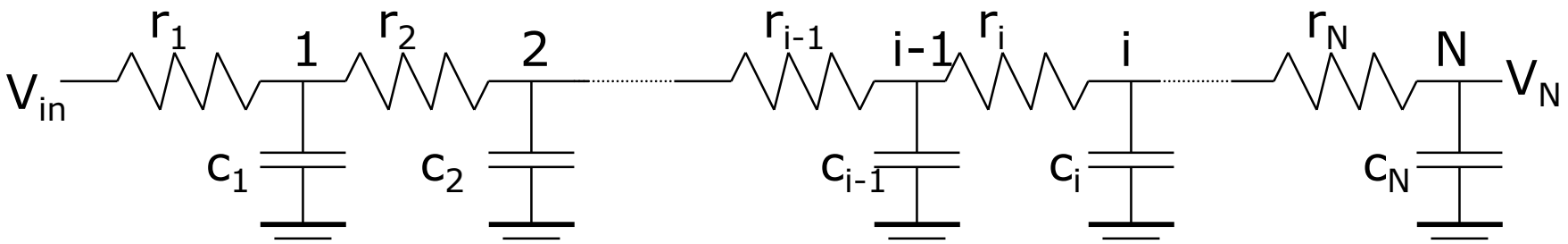


$$\tau(V_{out}) = \frac{rcL^2}{2}$$

- Wire parasitics
  - Capacitance, Resistance, Inductance
- Wire models (lumped, distributed)

$$\tau_D = R_s C_w + \frac{R_w C_w}{2} = R_s C_w + 0.5 r_w c_w L^2$$

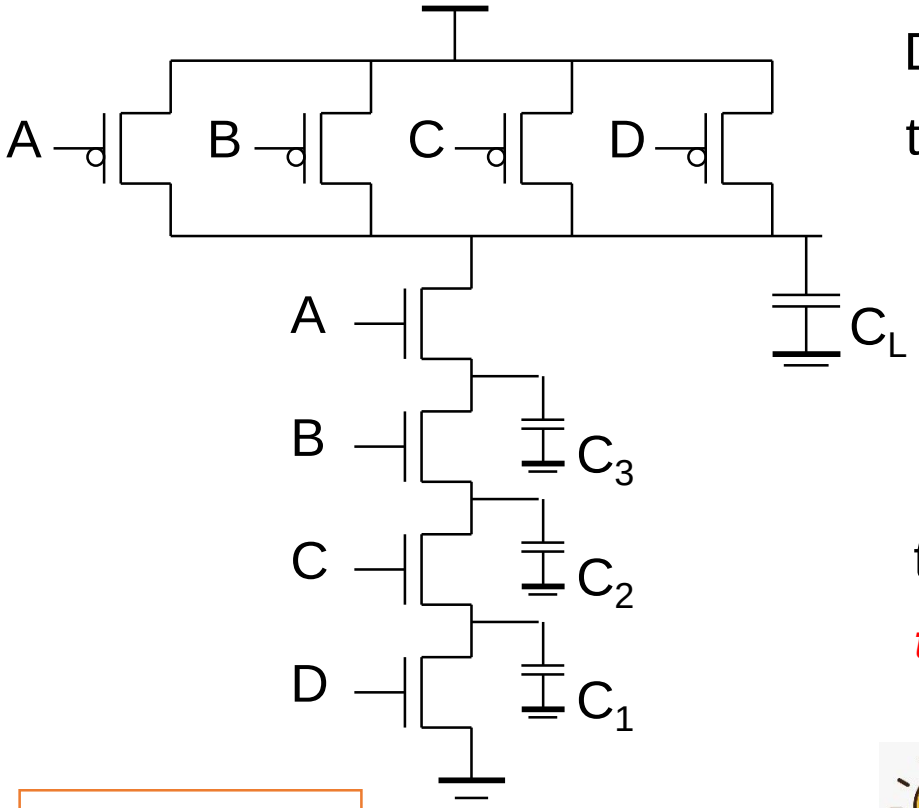
$$t_p = 0.69 R_s C_w + 0.38 R_w C_w$$

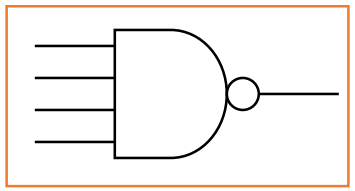


$\tau_{Di}=c_1r_1+ c_2(r_1+r_2)+\cdots+c_i(r_1+r_2+\cdots+r_i)$

$\tau_{Di}=c_1r_{eq}+ 2c_2r_{eq}+ 3c_3r_{eq}+\cdots+ ic_ir_{eq}$

主要内容（10）Elmore delay of gates





Distributed RC model (Elmore delay)

$t_{pHL} = 0.69\,[R_1C_1+(R_1+R_2)C_2+(R_1+R_2+R_3)C_3+(R_1+R_2+R_3+R_4)C_L]$

NMOS: same size R_{eqn}

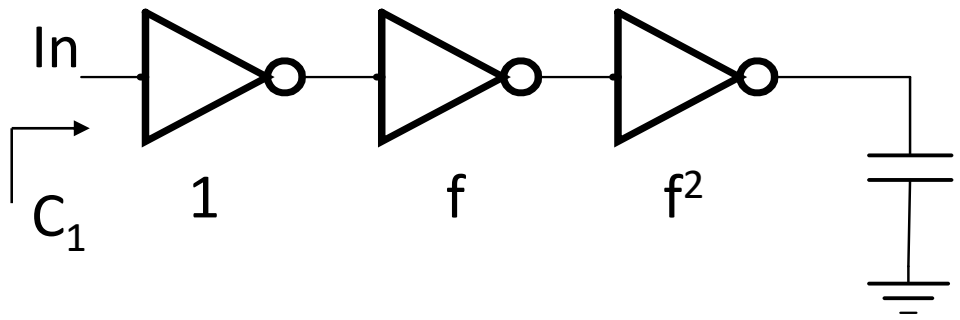
$t_{pHL} = 0.69\,R_{eqn}(C_1+2C_2+3C_3+4C_L)$

the worst-case

- The number of transistor required to implement an N fan-in is 2N =>area, capacitance
- Propagation delay deteriorates rapidly as a function of fan-in (# of inputs) – Quadratically

主要内容（11）

- Digital power consumption: $P_{\text{switching}} = \alpha C V_{DD}^{\ 2} f$
- Inverter: 反相器的阈值电压和 $(W/L)_{pmos} / (W/L)_{nmos}$ 为正比
- Delay: 反相器延时 $t_p = t_{p0}(1 + C_{ext}/\gamma C_g)$

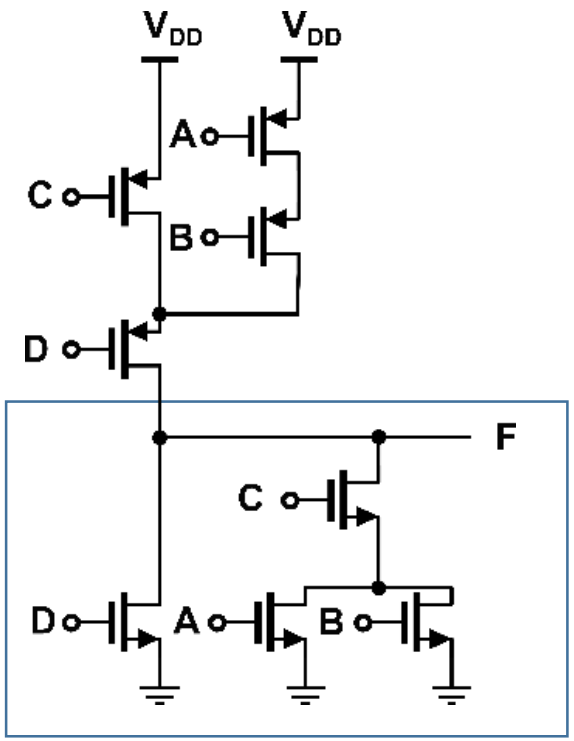


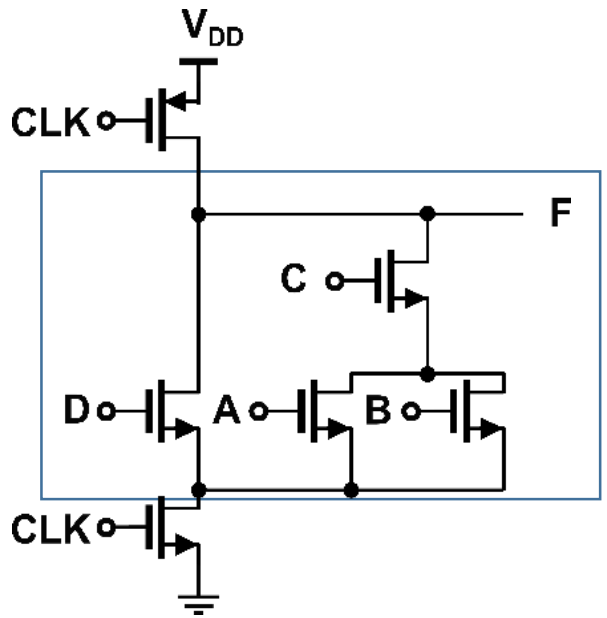
$N = \ln(F)$

$f = 2.71828 = e$

主要内容（12）

- 传输门，组合逻辑，动态逻辑 （两者的定义与区别）
- 从逻辑表达式 到电路拓扑图 到版图



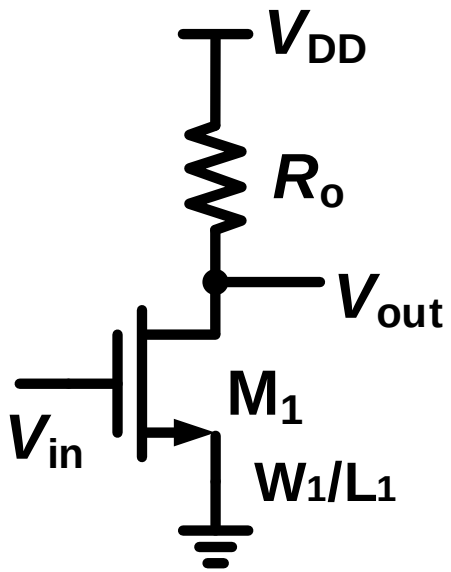


Analog Example (1)

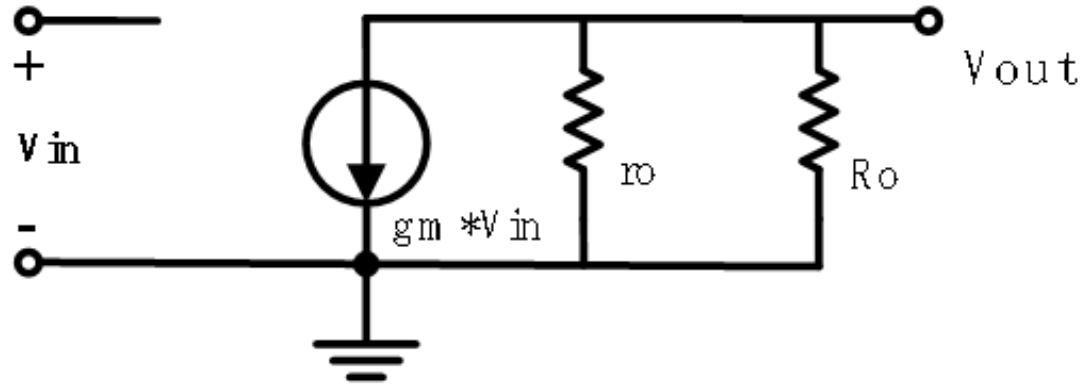
A single-stage amplifier is shown in Fig.4, assuming $\gamma=0, \lambda\neq0$ and $r_O>>1/g_m$.

(1) Please give its **equivalent small-signal circuits.** And calculate the symbolic small-signal **output resistance**, r_{out}, and **the voltage gain**, A_v;

(2) If the width W_1 of M_1 is increased, how does the gain change? Explain the reason;



(1) $r_{out}=r_o//R_o$（2 分），$A_v=g_m\times R_{out}=g_m\times(r_o//R_o)$（2 分）



(4 分，按实际绘图情况给分)，没有画 ro 扣 1 分

(2) $g_m=K\frac{W_1}{L_1}(V_{GS}-V_{TH})(1+\lambda V_{DS})$，$r_o=\frac{1}{\lambda I_D}=\frac{2}{\lambda K\frac{W_1}{L_1}(V_{GS}-V_{TH})^2(1+\lambda V_{DS})}$

$$A_v=g_m\frac{r_oR_o}{r_o+R_o}=K\left(\frac{W_1}{L_1}\right)(V_{GS}-V_{TH})(1+\lambda V_{DS})\frac{R_o}{1+\lambda I_DR_o}$$

$$=K(V_{GS}-V_{TH})(1+\lambda V_{DS})R_o\left(\frac{1}{\frac{L_1}{W_1}+\frac{1}{2}\lambda KR_o(V_{GS}-V_{TH})^2(1+\lambda V_{DS})}\right)$$

所以总体的增益是增加的 （2 分）

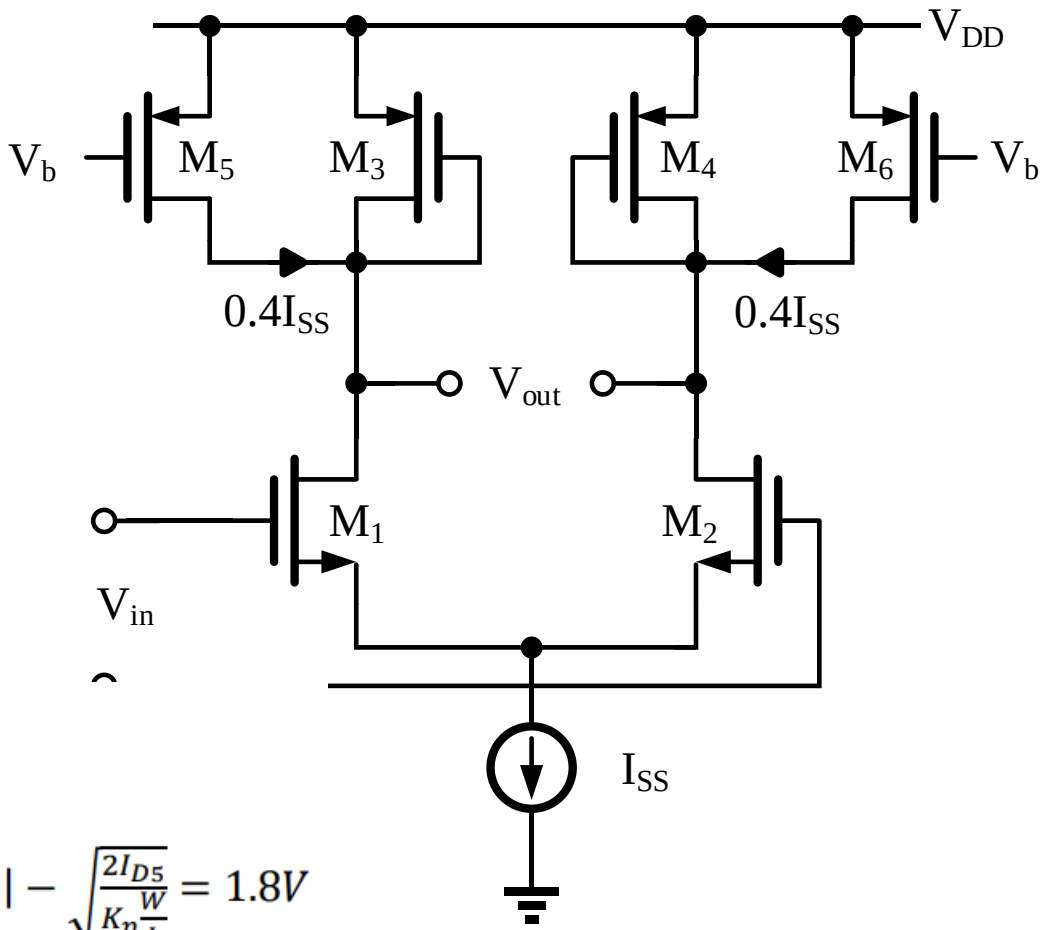
Analog Example (2)

In the circuit of Fig 6.3, assume that I_{SS}=1mA, V_{DD}=3V and W/L=50/0.5 for all the transistors. And I_{D5}=I_{D6}=0.8 (I_{SS}/2). Assuming **$\lambda \neq 0$**.

(a) Determine the **symbolic** voltage gain.

(b) Calculate V_b.

(c) What is the input common mode voltage range



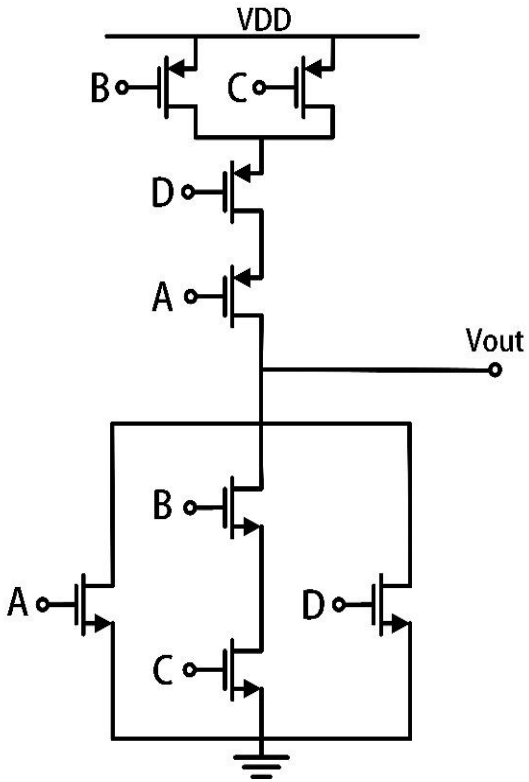
a) $A_V \approx -\frac{g_{m1}}{g_{m3}} = -\sqrt{\frac{K_n I_{D1}}{K_p I_{D3}}} = -\sqrt{\frac{134\times 0.5 I_{SS}}{50\times 0.2\frac{I_{SS}}{2}}} = -3.66$

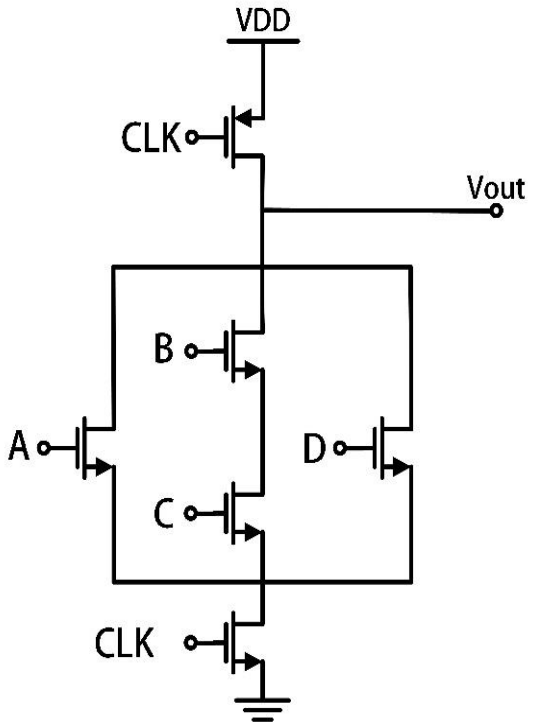
b) $I_{D5} = I_{D6} = 0.8\frac{I_{SS}}{2} = 0.4mA, V_b = V_{DD} - V_{SG5} = V_{DD} - |V_{TH}| - \sqrt{\frac{2I_{D5}}{K_p\frac{W}{L}}} = 1.8V$

Digital Example

(1) Please describe the concept of "**static logic circuit**" and "**dynamic logic circuit**" in digital circuits;

(2) Sketch 4-input gates $F = \overline{A + BC + D}$ using the circuit techniques of **static CMOS** and **dynamic gates**, respectively.





The *static* circuits class, which each gate output is connected to either *VDD* or *Vss* via a low-resistance path at every point in time.

The *dynamic* circuit class, which relies on temporary storage of signal values on the capacitance of high-impedance circuit nodes.

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