Using 4046-Type PLLs Successfully

The 4046/74HC4046-series phase-locked-loop ICs are extremely useful parts that can be used in a lot of applications like frequency synthesis/multiplication, signal synchronisation, data extraction etc.
Unfortunately, many first users have run into difficulties due to misleading (and very old/never revised) data sheets and erroneous application notes.
This note will show you how to interpret the information from the suppliers and let you use the 4046 successfully; all based on my own painful experiences.
At the end, we'll do a step-by-step design example.

The 4046 In Short

The 4046 contains two phase detectors (PD) and a voltage controlled oscillator (VCO).
This note will focus on the zero-phase-difference PD (phase detector II) and the VCO.
Other on-chip support circuitry will not be treated.

PLL Types

The 4046 is especially well-suited for the "Type 2, 2nd Order" phase-locked loop.
Type 2 means zero phase difference between the two input signals to the PLL when locked at a certain frequency, 2nd Order describes the PLLs response to changes in the input signals (frequency and phase) as well as the lock-in/transient characteristics.

PD

The phase detector II works well and fulfils its function, provided you use reasonable input frequencies. The 4046 up to a few hundred kilohertz, for the 74HC4046 up to a couple of megahertz. Higher cannot be recommended, although the data sheets suggest otherwise.

VCO

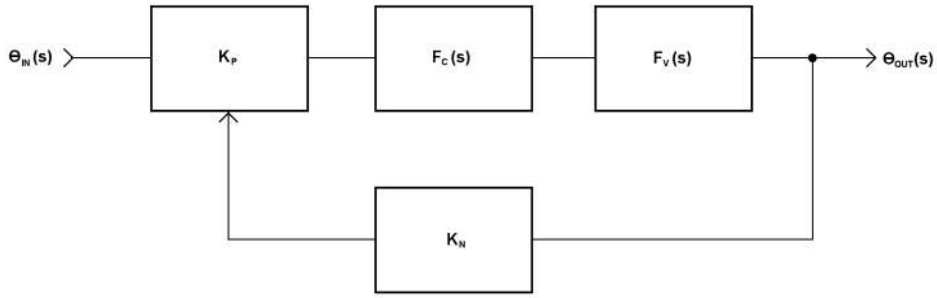
The 4046 voltage controlled oscillator runs well and is easy to use, provided it's set up for "zero-to-max" frequency span. A single resistor and capacitor is enough, but you should expect quite some frequency spread. +/-20% is not uncommon.
The datasheet, however, raises expectations that you can set an operating frequency range of say, 80...100 kHz by adding an extra resistor. Please forget this "feature"! The spread from batch to batch is so large that it's utopic. Also, the equations presented in the data sheet are off. Do not use this option in your design!

Loop Controller (aka Loop Filter)

The loop controller essentially defines the behaviour of your PLL system, and the often seen assumption that it's "just a low pass filter" won't fly.
Designing a loop controller is where the data sheets and application notes on the 4046 fail miserably. The documentation from the suppliers suggest that a simple RC or RRC passive filter is enough. Wrong! (The ambiguity in the data sheets is because it is not clearly stated that the simple filters only work with the Type I PD).
For a Type II response, the transfer function (servo theory) of the PLL dictates that an integrator is mandatory in the loop. It is indeed possible to build a passive integrator for the loop controller, but certainly not as shown in the data sheet or many application notes. And it's not a good solution, as it relies on device parameters that have large spread.

Analysing and synthesising a 4046-type PLL

There's no way around it – we need to do a bit of calculating when designing a PLL, but I will not go into deep theory. Refer to the sources in the appendix if you're really into the maths.
Fortunately, the PLL transfer function can be described in Laplace notation (using the complex operator *s*), which simplifies the calculations a lot.
Here's a simplified block diagram of a PLL system:



The individual gain/transfer function elements are:
K_P: phase detector
$F_C(s)$: loop controller
$F_V(s)$: voltage controlled oscillator
K_N: feedback divider (optional)

From basic feedback theory, the closed loop transfer function is:

$$\frac{G(s)}{1 + G(s)\cdot H(s)}$$ (G(s) is the forward function, H(s) is feedback)

Which yields:

$$\frac{K_P\cdot F_C(s)\cdot F_V(s)}{1 + K_P\cdot F_C(s)\cdot F_V(s)\cdot K_N} \quad (1)$$

The desired closed loop, 2nd order, type 2 PLL transfer function is:

$$\frac{2\cdot\zeta\cdot\omega_n\cdot s + \omega_n^2}{s^2 + 2\cdot\zeta\cdot\omega_n\cdot s + \omega_n^2} \quad (2)$$

Where ζ is the damping factor and ω_n is the natural loop angular frequency. Do not confuse ω_n with PD input or VCO frequency.

K_P:
The 4046-type phase detector will output ~V_{EE} (0 V) or ~V_{DD} (the on-state output voltage drop can be ignored).
Depending on which PD input is leading in phase, the input phase difference can be up to 2π in both directions.
So:

$$K_P = V_{DD} / 4\pi \qquad \text{(ie, } V_{DD} / \pm 2\pi\text{)}$$

For often used V_{DD} we have:

$K_{P(5\ V)} = 0.398\ V/rad$
$K_{P(12\ V)} = 0.955\ V/rad$

$F_V(s)$:
The VCO transfer function depends on the desired output frequency, but a general equation can be derived. Using rail-to-rail opamps (input and output) for the loop controller, the input voltage to the VCO ranges from V_{EE} to V_{DD}. Maximum frequency f_{MAX} is achieved when the VCO input is at V_{DD}. Minimum frequency is zero. Normal operating frequency should be chosen as $f_{MAX}/2$.
So:

$$F_V(s) = (2\pi \cdot f_{MAX}) / (V_{DD} \cdot s)$$

Note the complex Laplace operator *s* in the denominator. This converts the VCO output from frequency to phase.

For later calculations, it is convenient to also define K_V:

$$K_V = (2\pi \cdot f_{MAX}) / V_{DD} \qquad \text{(rad/s) / V}$$

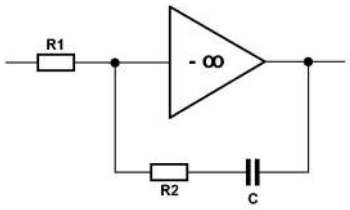
K_N:
For frequency multiplication or synthesis, a fixed or programmable counter is in the feedback loop of your PLL. With no counter, K_N is simply 1. N is the counter division ratio.
So:

$$K_N = 1 / N$$

$F_C(s)$:
This is where the fun begins. From the above derivation of K_P, $F_V(s)$ and K_N, it's obvious that they cannot influence loop behaviour, there are simply no variables to play with.
The loop controller is the key element.
Inspecting and combining equations (1) and (2) reveal that this transfer function will fulfil our criteria for a basic loop controller:

$$\frac{s + a}{s}$$

This simple circuit (using an ideal amplifier):



Will provide the desired transfer function:

$$F_C(s) = -\frac{R_2}{R_1}\,\frac{s + (1 / R_2C)}{s}$$

As a simplification for subsequent calculations, we define:

$$K_C = -\frac{R_2}{R_1}$$

Note the negative gain. For the calculations here it will treated as positive gain. The final practical implementation will solve this issue in a simple way.

The Final Analysis

Now that all the PLL elements have been identified, it's time to use equations (1) and (2) to extract expressions for ω_n and ζ. When those two parameters have been defined, it's easy to establish the desired loop behaviour.
Using equation (1), we insert the parameters/functions we found above and get:

$$\frac{(1 / K_N)\cdot(K_P\cdot K_C\cdot K_V\cdot K_N\cdot s + K_P\cdot K_C\cdot K_V\cdot K_N / [R_2\cdot C])}{s^2 + K_P\cdot K_C\cdot K_V\cdot K_N\cdot s + K_P\cdot K_C\cdot K_V\cdot K_N / [R_2\cdot C]}$$

It's obvious from equation (2) and replacing K_C and K_N that:

$$\boldsymbol{\omega_n = \sqrt{(K_P\cdot K_V)} / \sqrt{(N\cdot R_1\cdot C)}}$$

And:

$$\zeta = K_P\cdot K_V\cdot R_2 / (2\cdot\omega_n\cdot N\cdot R_1)$$

Inserting ω_n yields:

$$\boldsymbol{\zeta = \tfrac{1}{2}\cdot R_2\cdot\sqrt{(K_P\cdot K_V\cdot C)} / \sqrt{(N\cdot R_1)}}$$

Note that both ω_n and ζ change with $1/\sqrt{N}$. Keep this in mind when designing programmable frequency synthesizers.

Having found the equations for ω_n and ζ, we now use these to find the values of R_1, R_2 and C. Remember, they are the only variables left to play with.
Rearranging the equations for ζ and ω_n we get:

$$\boldsymbol{R_1\cdot C = (K_P\cdot K_V) / (N\cdot\omega_n^2)} \qquad (3)$$

$$\boldsymbol{R_2 = 2\cdot\zeta\cdot\sqrt{(N\cdot R_1)} / \sqrt{(K_P\cdot K_V\cdot C)}} \qquad (4)$$

It's now possible to find R_1, R_2 and C for the loop controller and design a PLL with predictable behaviour.

All equations above will work for any Type 2, 2nd Order PLL with the suggested loop controller, provided boundaries are respected (eg, $\omega_n << \omega_i$).

A Practical Example

In an analogue video system, we need to generate a 1 MHz clock signal, synchronized and in phase with the 15625 Hz horizontal synchronization pulses. A job for the 4046!
As the VCO frequency is at 1 MHz, the 74HC4046 running at 5 V is selected for the job.
We can already now determine some of the parameters:

$K_P = 0.398$
$K_V = 2\pi \cdot 2 \cdot 10^6 / 5 = 2.51 \cdot 10^6$ (f_{MAX} = 2 MHz)
$K_N = 15625/1000000 = 1/64$; N = 64

Looking at equations (3) and (4), we now only need to determine ω_n and ζ.
But how?

Well, ζ is relatively easy; there's a 'favourite' range for 2nd order PLL designs:
$\zeta = 0.707...1.0$.
$\zeta = 0.707$ gives the fastest lock-in, but exhibits ~20% frequency overshoot to an input step.
$\zeta = 1$ (also called "critical damping") exhibits no overshoot, but takes around twice as long to settle.
For your reference, 2nd order step response graphs can be found everywhere. Here's an example:
https://www.researchgate.net/figure/Unit-step-time-responses-of-a-second-order-system-with-various-damping-ratios-The_fig6_229817889

Choosing ω_n is not so easy without doing extremely tedious analysis.
I have a rule-of-thumb for a first approximation, based on my experience with the '4046, and it works every time (provided you stay within the damping factor range above):
Select $\omega_n \leq \omega_i / 200$, where ω_i is the angular input frequency to the PD. This is quite conservative, but will reward you with a reliably locking PLL from the start (if your PLL doesn't lock after 200 input cycles, something else is wrong!). Experimentally, you can increase ω_n later if you want a faster loop. Fast lock-in, though, is seldom a main criteria for 4046-type PLLs, loop stability tends to be more important.
My selection here is:

$\zeta = 0.8$
$\omega_n = 2\pi \cdot 15625/200 = 491$ rad/s

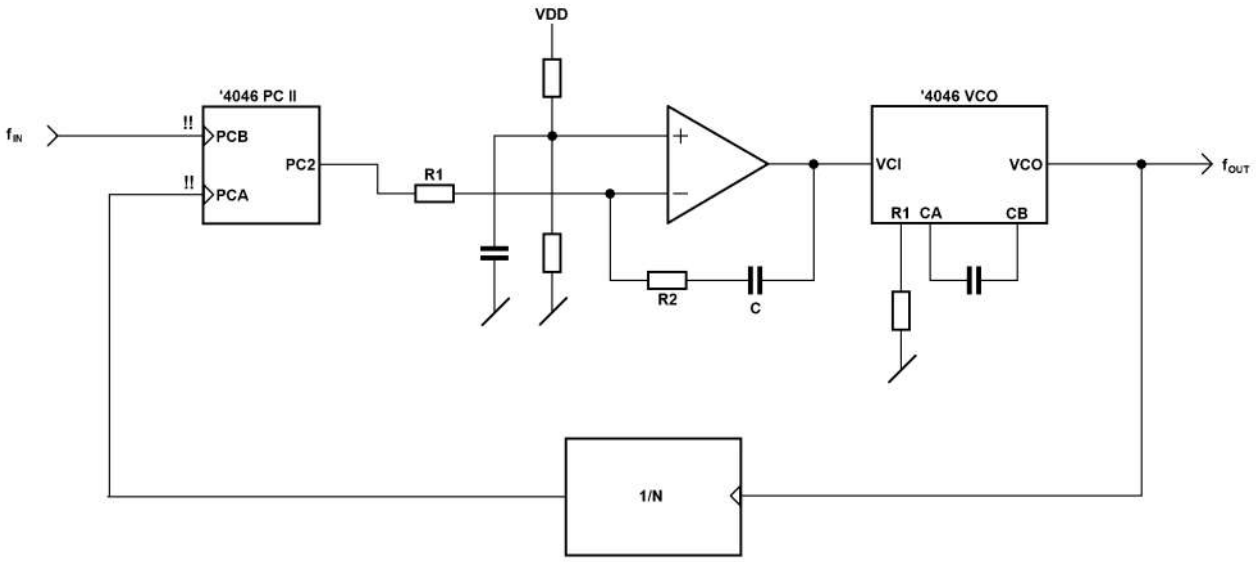
A reasonable value for R_1 is around 100 kΩ, plugging this into equation (3) gives:

$C = (0.398 \cdot 2.51 \cdot 10^6) / (64 \cdot 491^2 \cdot 100 \cdot 10^3) = 647$ nF ~ 680 nF

Solving for R_2 using equation (4):

$R_2 = 2 \cdot 0.8 \cdot \sqrt{(64 \cdot 100 \cdot 10^3)} / \sqrt{(0.398 \cdot 2.51 \cdot 10^6 \cdot 680 \cdot 10^{-9})} = 4.91$ kΩ ~ 5.1 kΩ

The final system block diagram looks like this:



R_1, R_2 and C have been calculated. The voltage divider at the non-inverting input of the amplifier sets the DC bias at $V_{DD}/2$, the two resistors should be chosen as $R_1 \cdot 2$ (= 200 kΩ). The decoupling capacitor at the voltage divider is uncritical, 10 nF is sufficient.
Determining the capacitor and resistor for setting the VCO frequency is an exercise for yourself.
The amplifier is single-supply, powered from V_{DD}. Choosing one is up to you, there are plenty around. Rail-to-rail input and output is mandatory (RRIO). For this application I used the LMC6482, which is an excellent low-power device, but due to it's low GBW almost at its limits here (~16 kHz input frequency).

Oh! I almost forgot: The problem of the negative gain of the loop controller mentioned in the $F_C(s)$ section?
Easily solved. Simply swap the PCA and PCB inputs to the '4046 phase detector as shown in the system block diagram.

Final remarks

By using the method described above, you'll be able to get a Type 2 PLL up and running reliably in no time.
For static phase locked loops (N is constant or 1), this way of finding ζ and ω_n is usually fully sufficient.
For programmable frequency synthesizers, lock-in time is much more important and a more aggressive approach to optimizing ω_n is necessary, but is outside the scope of this article (I promised to try and keep it simple).
Both ζ and ω_n will shift if the gain and bandwidth of the operational amplifier is insufficient.
Note that the '4046-type of phase detectors are very sensitive to noise. Additional or missing input pulses will cause them to drop out of lock within a few f_{IN} cycles (<10).

References:
"Phaselock Techniques", Floyd M. Gardner
"Phase-Locked Loop Design Fundamentals", AN-535, NXP Semiconductors