```
arch
+ reset n sync iq rdclk
+ rx_sample_nr_iq rdclk
+ en sync rx sample clk
+ en sync ig rdclk
+ pct loss flg clr sync
ig rdclk
+ mode sync iq rdclk
+ trxiqpulse sync iq
rdclk
+ ddr en sync ig rdclk
+ mimo_en_sync_iq_rdclk
+ fidm sync ig rdclk
and 18 more
+ PROCESS 567()
+ PROCESS 568()
+ PROCESS 569()
+ PROCESS 570()
+ PROCESS 571()
```