```
arch
+ inst0 fifo wrrea
+ inst0 fifo wdata
+ inst0 reset n
+ inst1 fifo wrrea
+ inst1 fifo wdata
+ inst1 reset n
+ mux fifo wrrea
+ mux fifo wdata
+ fifo wrrea rea
+ fifo wdata reg
+ int fifo wrrea
+ inst0 reset proc()
+ inst1 reset proc()
```

+ out reg fifo wdata()