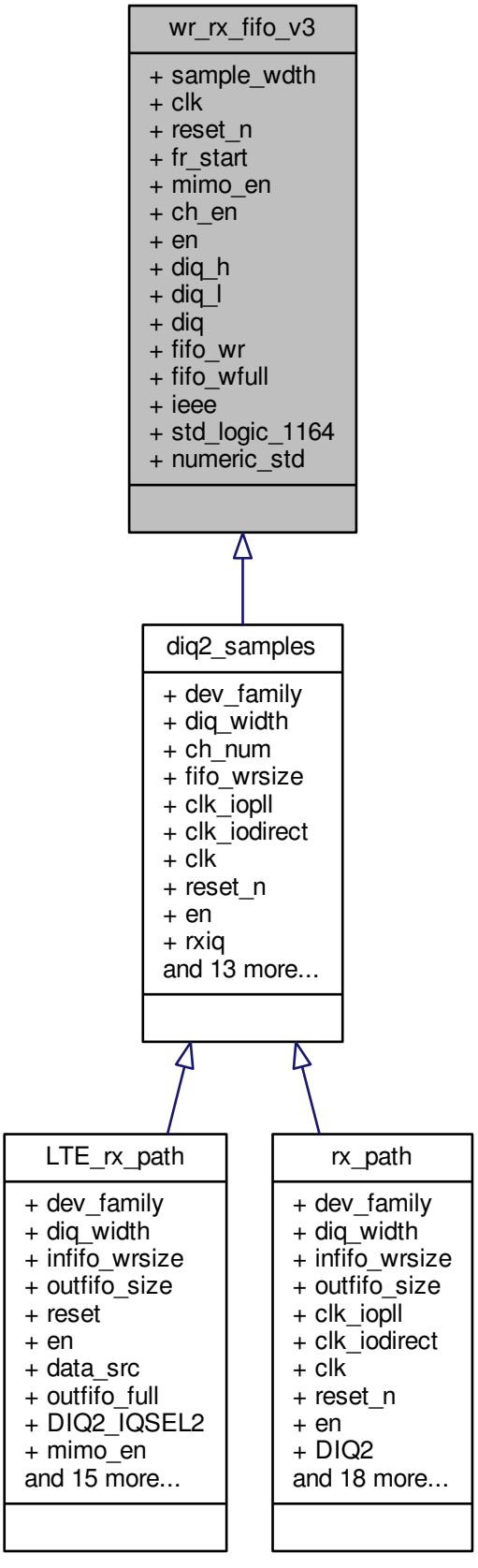
wr_rx_fifo_v3
+ sample_wdth
+ clk
+ reset_n
+ fr_start
+ mimo_en
+ ch_en
+ en
+ diq_h
+ diq_l
+ diq
+ fifo_wr
+ fifo_wfull
+ ieee
+ std_logic_1164
+ numeric_std
diq2_samples
+ dev_family
+ diq_width
+ ch_num
+ fifo_wrsize
+ clk_iopll
+ clk_iodirect
+ clk
+ reset_n
+ en
+ rxiq
and 13 more...
LTE_rx_path
+ dev_family
+ diq_width
+ infifo_wrsize
+ outfifo_size
+ reset
+ en
+ data_src
+ outfifo_full
+ DIQ2_IQSEL2
+ mimo_en
and 15 more...
rx_path
+ dev_family
+ diq_width
+ infifo_wrsize
+ outfifo_size
+ clk_iopll
+ clk_iodirect
+ clk
+ reset_n
+ en
+ DIQ2
and 18 more...