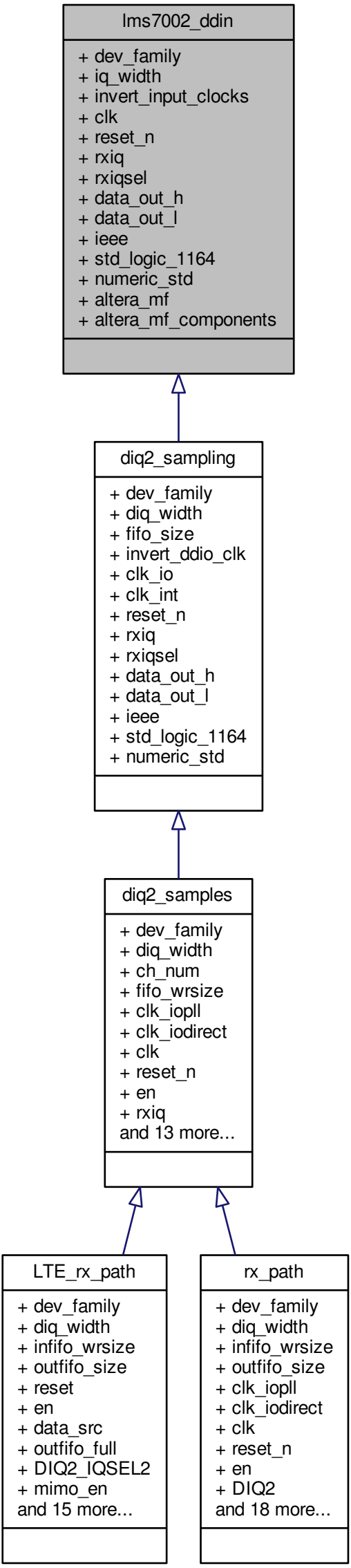
lms7002_ddin
+ dev_family
+ iq_width
+ invert_input_clocks
+ clk
+ reset_n
+ rxiq
+ rxiqsel
+ data_out_h
+ data_out_l
+ ieee
+ std_logic_1164
+ numeric_std
+ altera_mf
+ altera_mf_components
diq2_sampling
+ dev_family
+ diq_width
+ fifo_size
+ invert_ddio_clk
+ clk_io
+ clk_int
+ reset_n
+ rxiq
+ rxiqsel
+ data_out_h
+ data_out_l
+ ieee
+ std_logic_1164
+ numeric_std
diq2_samples
+ dev_family
+ diq_width
+ ch_num
+ fifo_wrsize
+ clk_iopll
+ clk_iodirect
+ clk
+ reset_n
+ en
+ rxiq
and 13 more...
LTE_rx_path
+ dev_family
+ diq_width
+ infifo_wrsize
+ outfifo_size
+ reset
+ en
+ data_src
+ outfifo_full
+ DIQ2_IQSEL2
+ mimo_en
and 15 more...
rx_path
+ dev_family
+ diq_width
+ infifo_wrsize
+ outfifo_size
+ clk_iopll
+ clk_iodirect
+ clk
+ reset_n
+ en
+ DIQ2
and 18 more...