```
arch
+ reg 0
+ reg 1
+ reg 2
+ reg 0 ld
+ reg_0_ld_f
+ reg 1 ld
+ reg_1_ld_f
+ reg 2 ld
+ reg 2 ld f
+ reg ld
and 14 more...
+ pct data wr cnt max proc()
+ pct end cnt proc()
+ pct data wr cnt proc()
+ reg_stage_0()
+ reg stage 1()
+ reg_stage_2()
+ fsm f()
+ fsm()
+ pct wrreq int proc()
+ PROCESS 333()
```