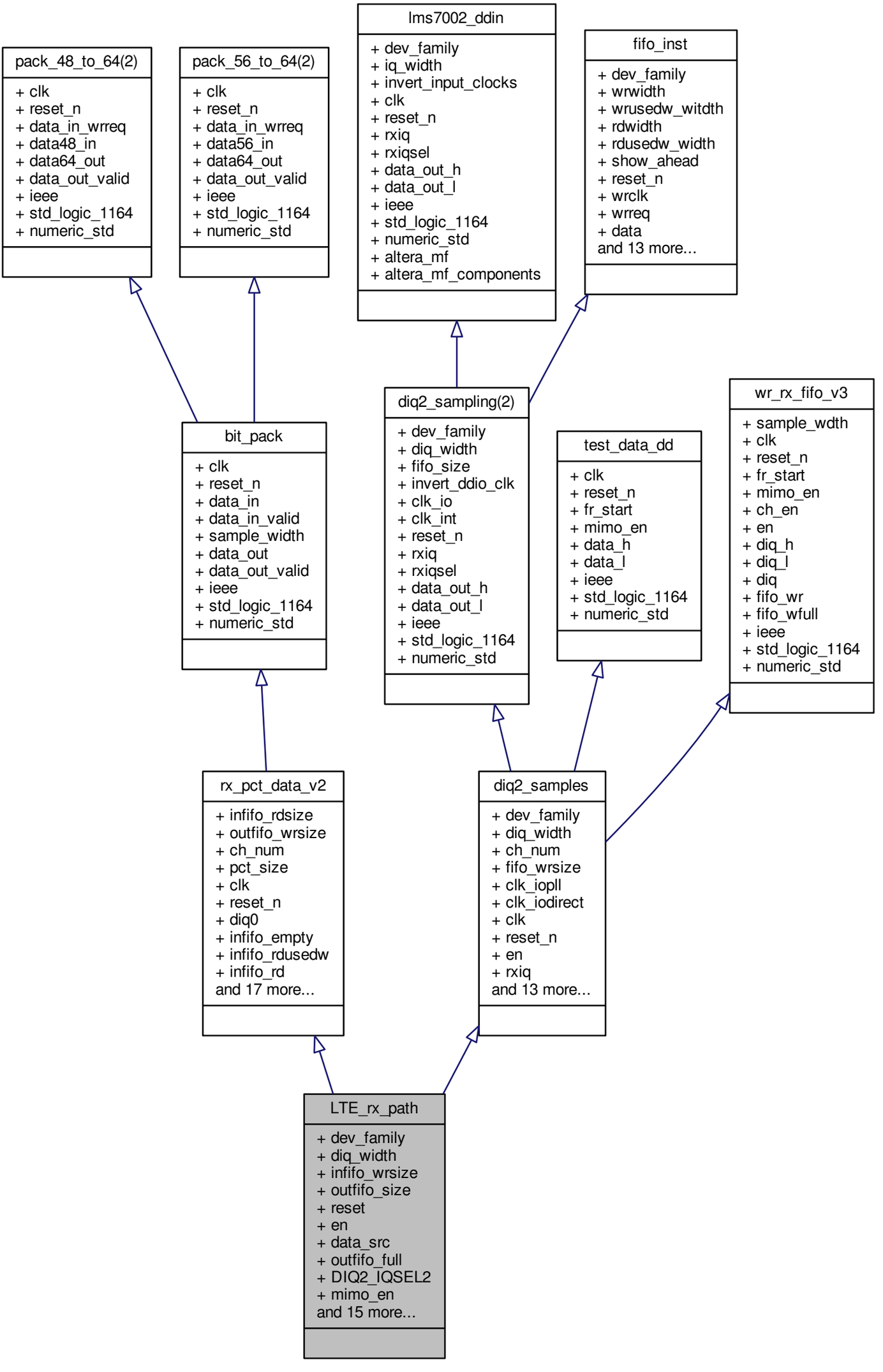
pack_48_to_64(2)
+ clk
+ reset_n
+ data_in_wrreq
+ data48_in
+ data64_out
+ data_out_valid
+ ieee
+ std_logic_1164
+ numeric_std
pack_56_to_64(2)
+ clk
+ reset_n
+ data_in_wrreq
+ data56_in
+ data64_out
+ data_out_valid
+ ieee
+ std_logic_1164
+ numeric_std
lms7002_ddin
+ dev_family
+ iq_width
+ invert_input_clocks
+ clk
+ reset_n
+ rxiq
+ rxiqsel
+ data_out_h
+ data_out_l
+ ieee
+ std_logic_1164
+ numeric_std
+ altera_mf
+ altera_mf_components
fifo_inst
+ dev_family
+ wrwidth
+ wrusedw_witdth
+ rdwidth
+ rdusedw_width
+ show_ahead
+ reset_n
+ wrclk
+ wrreq
+ data
and 13 more...
bit_pack
+ clk
+ reset_n
+ data_in
+ data_in_valid
+ sample_width
+ data_out
+ data_out_valid
+ ieee
+ std_logic_1164
+ numeric_std
diq2_sampling(2)
+ dev_family
+ diq_width
+ fifo_size
+ invert_ddio_clk
+ clk_io
+ clk_int
+ reset_n
+ rxiq
+ rxiqsel
+ data_out_h
+ data_out_l
+ ieee
+ std_logic_1164
+ numeric_std
test_data_dd
+ clk
+ reset_n
+ fr_start
+ mimo_en
+ data_h
+ data_l
+ ieee
+ std_logic_1164
+ numeric_std
wr_rx_fifo_v3
+ sample_wdth
+ clk
+ reset_n
+ fr_start
+ mimo_en
+ ch_en
+ en
+ diq_h
+ diq_l
+ diq
+ fifo_wr
+ fifo_wfull
+ ieee
+ std_logic_1164
+ numeric_std
rx_pct_data_v2
+ infifo_rdsize
+ outfifo_wrsize
+ ch_num
+ pct_size
+ clk
+ reset_n
+ diq0
+ infifo_empty
+ infifo_rdusedw
+ infifo_rd
and 17 more...
diq2_samples
+ dev_family
+ diq_width
+ ch_num
+ fifo_wrsize
+ clk_iopll
+ clk_iodirect
+ clk
+ reset_n
+ en
+ rxiq
and 13 more...
LTE_rx_path
+ dev_family
+ diq_width
+ infifo_wrsize
+ outfifo_size
+ reset
+ en
+ data_src
+ outfifo_full
+ DIQ2_IQSEL2
+ mimo_en
and 15 more...