```
tb behave
+ clk0 period
+ clk1 period
+ clk0
+ clk1
+ reset n
+ dut0 pll areset
+ dut0 inv c0
+ dut0 clk ena
+ dut0 drct clk en
+ dut0 rcnfig areset
and 16 more...
+ clock0()
+ clock()
+ res()
+ PROCESS 372()
+ PROCESS 373()
+ PROCESS 374()
```