```
arch
+ int fifo rdrea
+ int fifo g valid
+ dig smpl 0
+ dia smpl_1
+ dig smpl 2
+ dig smpl 3
+ mux pos0 L
+ mux pos1 L
+ mux pos2 L
+ mux pos3 L
and 23 more
+ rd wait cnt proc()
+ fsm f()
+ fsm()
+ PROCESS 504()
+ PROCESS 505()
+ PROCESS 506()
+ dig L reg x proc()
+ dig H reg x proc()
```