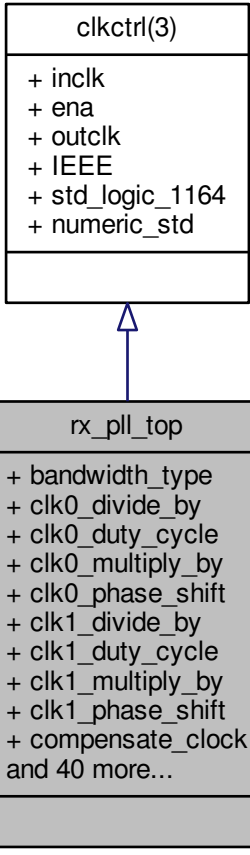
clkctrl(3)
+ inclk
+ ena
+ outclk
+ IEEE
+ std_logic_1164
+ numeric_std
rx_pll_top
+ bandwidth_type
+ clk0_divide_by
+ clk0_duty_cycle
+ clk0_multiply_by
+ clk0_phase_shift
+ clk1_divide_by
+ clk1_duty_cycle
+ clk1_multiply_by
+ clk1_phase_shift
+ compensate_clock
and 40 more...