```
pack 56 to 64
           + clk
           + reset_n
           + data in wrreq
           + data56_in
           + data64_out
           + data_out_valid
           + ieee
           + std_logic_1164
           + numeric_std
                   Δ
                bit_pack
           + clk
           + reset_n
           + data_in
           + data_in_valid
           + sample width
           + data_out
           + data_out_valid
           + ieee
           + std logic 1164
           + numeric_std
            rx_pct_data_v2
           + infifo rdsize
           + outfifo_wrsize
           + ch num
           + pct size
           + clk
           + reset n
           + diq0
           + infifo_empty
           + infifo_rdusedw
           + infifo rd
           and 17 more...
 LTE_rx_path
                            rx_path
+ dev_family
                         + dev_family
+ dig width
                         + diq_width
+ infifo wrsize
                         + infifo wrsize
+ outfifo size
                         + outfifo size
+ reset
                         + clk_iopll
+ en
                         + clk_iodirect
+ data src
                         + clk
+ outfifo_full
                         + reset n
+ DIQ2_IQSEL2
                         + en
                         + DIQ2
+ mimo en
and 15 more...
                         and 18 more...
```