```
ddr2_phy_alt_mem_phy_seq
+ FAMILY
+ MEM IF MEMTYPE
+ SPEED GRADE
+ FAMILYGROUP ID
+ MEM IF DQS WIDTH
+ MEM IF DWIDTH
+ MEM_IF_DM_WIDTH
+ MEM IF DQ PER DQS
+ DWIDTH RATIO
+ CLOCK INDEX WIDTH
and 121 more...
             +seg report prefix
          struct
  + altera attribute

    altera attribute

  + rsu multiple valid
  latencies err
  + rsu grt one dvw err
  + rsu no dvw err
  + rsu codvw phase
  + rsu codvw size
  + rsu read latency
  + dgrb mmi
  + regs admin ctrl rec
  and 113 more...
  + capabilities_override()
  + PROCESS 54()
  + PROCESS 55()
  + PROCESS
               56()
  + PROCESS 57()
  + decode cl()
  + decode al()
  + decode cwl()
  + oct delay proc()
  + PROCESS 58()
  and 25 more...
```