```
clkctrl(3)
 + inclk
  + ena
 + outclk
 + IEEE
 + std logic 1164
 + numeric std
     tx pll top
+ bandwidth type
+ clk0 divide by
+ clk0_duty_cycle
+ clk0 multiply by
+ clk0 phase shift
+ clk1 divide by
+ clk1 duty cycle
+ clk1 multiply by
+ clk1 phase shift
+ compensate clock
and 41 more...
```