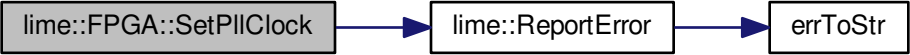


lime::FPGA::SetPllClock



```
graph LR; A[lime::FPGA::SetPllClock] --> B[lime::ReportError]; B --> C[errToStr];
```

lime::ReportError

errToStr