

NANYANG TECHNOLOGICAL UNIVERSITY

SEMESTER 2 EXAMINATION 2020-2021

CE1106/CZ1106 – COMPUTER ORGANIZATION AND ARCHITECTURE

Apr/May 2021

Time Allowed: 1 hour

INSTRUCTIONS

1. This paper contains 2 questions and comprises 8 pages.
2. Answer **ALL** questions. Questions carry **unequal** marks.
3. This is a closed-book examination.
4. The ARM Instruction Set Summary Chart is provided in Appendix 1 on page 8.

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1. (a) The current Trace Together Token used for contact tracing has the following specifications and features.

- 64Mhz ARM Cortex M4F Processor with 16Kbyte cache
- 1 Mbyte on-chip Flash and 256Kbyte on-chip SRAM
- External 64Mbyte NAND Flash
- 1000mAh battery that can last for 6 months
- For contact tracing purpose, the token is able to store the identity information of other tokens in its vicinity, for the past 25 days.

- (i) What is the main function of the on-chip 64Mbyte NAND flash in this system? (4 marks)

Storage (4 marks)

- (ii) What is the difference between the function of the 16Kbyte cache and the 256Kbyte on-chip SRAM? (4 marks)

16 Kb is buffer between CPU & SRAM to ↑ mem spd (4 marks)

- (iii) What is the average current consumption of the Trace Together Token? Assume 1 month = 30 days. (4 marks)

6x 30x 2⁴ = 4320 0.231 mA (4 marks)

- (iv) Which flash type would the 1 Mbyte on-chip flash be made of? (4 marks)

NOR . XIP

(4 marks)

Note: Question No. 1 continues on Page 2

- (b) Figure Q1a shows the wave form of the signal transmitted from a UART transmitter.

- 5V corresponds to Logic ‘1’.
- Baud rate of the transmitter is 4800 bps
- UART configuration used is 7O1 i.e. 7 DATA bits, Odd Parity scheme and 1 STOP bit.
- However, baud rate of the UART receiver is wrongly configured to 9600 bps.
- Assume that UART receiver will continue to receive UART data even if error is detected.

- (i) What is the time duration of one UART bit if the waveform is captured on the oscilloscope?

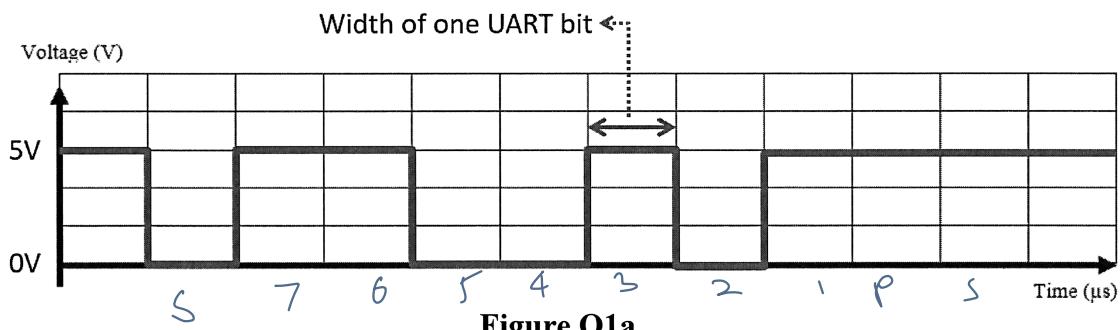
0.208 ms (4 marks)

- (ii) What is the first data sampled by the receiver? What is/are the errors (if any) detected?

(8 marks)

- (iii) What is the second data sampled by the receiver? What is/are the errors (if any) detected?

(8 marks)



11 00 11 11 00 00 11 00 11 11 11
 5 7 6 5 4 3 2 1 p? 5 5 5 7 6 5 4 3 2 1

Note: Question No. 1 continues on Page 3

(c) Consider a system with the following characteristics.

- Direct mapped cache of 32 cache blocks and block size 16 bytes
- Cache uses Physical Address for address mapping
- Virtual Memory page size 1024bytes → 10
- Virtual Memory size 1Mbyte. Physical Memory size 64 KByte
- Extracts of Page Table (valid entries) → 20 → 16
- Virtual Page 1 → Physical Frame 2
- Virtual Page 2 → Physical Frame 3
- Virtual Page 3 → Physical Frame 5
- Virtual Page 4 → Physical Frame 1
- Virtual Page 5 → Physical Frame 8
- Cache access time = 5ns
- Physical Memory access time = 100ns
- Page table is stored in Physical memory. No TLB in this system.
- Access to Cache and Physical Memory do not overlap.

6 | 10

$0x01111 : 0001\ 0001\ 0001\ 0001$
 $0x0111\ A : 0001\ 0001\ 0001\ 1010$

(i) A character array of 10 elements, $x[]$, is stored at locations starting from virtual memory address $0x01111$, what is the physical memory address of the first and last element of the array $x[]$? $0x51A$

(8 marks)

(ii) What is the time required to read the entire array? Assume that the entire array $x[]$ is not in the cache when the first element read is carried out. State any assumptions used.

(8 marks)

Note: Question No. 1 continues on Page 4

- (d) Consider a processor with 4 pipeline stages: Fetch Instruction (F), Decode (D), Execute (E) and Store (S). Assume that

- Branch target address is calculated at the execute stage
- Instruction length for every instruction is one word long
- Each pipeline stage takes 1 cycle to complete
- No resource conflicts
- Delayed branching is enabled
- This processor is not an ARM processor

How many cycles does the CPU takes to execute the program in Figure Q1b?

3 load pipe

(8 marks)

	MOV	R0, #0	;I1	4
	MOV	R1, #0x400	;I2	
	MOV	R2, #0x200	;I3	
	MOV	R6, #0x300	;I4	
Loop	LDR	R3, [R2]	;I5	
	LDR	R4, [R3]	;I6	$(6+2) \times 10$
	ADD	R4, R4, R3	;I7	
	ADD	R0, R0, #1	;I8	
	CMP	R0, #10	;I9	
	BNE	Loop	;I10	
	ADD	R6, R6, #1	;I11	
	ADD	R2, R2, #1	;I12	
	STR	R5, [R1]	;I13	+ 1

Figure Q1b

2. Answer all 10 Multiple-Choice Questions below (4 marks each). Write your answers in the Answer Booklet provided. Note that there is only one correct answer for each question.

(a) Which of the following statement below is FALSE?

- A. Differential signal has higher noise tolerance than that of single-ended signal. T
- B. VIL of a device is always higher than VOL of the same device. T
- C. Driving a 3V digital signal into a 5V device will not damage the device but may result in wrong data at the receiver end. T
- D. VOH of a device is always lower than VIH of the same device to cater for loss in electrical potential due to transmission line resistance. F
- E. None of the above

(b) A UART transmission line uses a configuration of 1 Start, 8 Data, No Parity and 1 STOP bit. Its baud rate is 57600 bps. How many 7-bit ASCII characters can be transmitted in one second? 10

- A. 5236
- B. 5760
- C. 6400
- D. 8228
- E. None of the above

(c) Which statement below about NOR flash is FALSE?

- A. NAND flash has lower cost per bit than that of NOR flash T
- B. Erasure in NOR flash is done at block level. T
- C. NOR flash does not support Execute in Place F
- D. NAND Flash layout is more compact than NOR flash T
- E. None of the above

Note: Question No. 2 continues on Page 6

- A
- (d) Which of the following is not recommended when designing PCB?
- A. Increase the length of high speed PCB traces
 - B. Separate high and low speed PCB traces
 - C. Reduce the length of one or more PCB traces in the data bus so that the propagation delay of the entire bus is kept the same
 - D. Increase the length of one or more PCB traces in the data bus so that the propagation delay of the entire bus is kept the same.
 - E. None of the above
- C
- (e) What is the range of an 8-bit binary, fixed point, 2's complement number system with 5 integer bits and 3 fractional bits? That is, "XXXXX.XXX".
- A. 0 to +255
 - B. -16 to +15.222
 - C. -16 to +15.875
 - D. -128 to +127
 - E. None of the above
- C
- (f) If the CPU's interrupt latency is $5\mu s$ and the UART interrupt service routine takes $20\mu s$ to transfer the received data from the UART buffer to processor memory, how many UART packets can the CPU transfer in one second?
- A. 20000
 - B. 25000
 - C. 40000
 - D. 50000
 - E. None of the above
- C
- (g) Which state of the floating gate transistor will yield a higher threshold voltage (V_t)?
- A. No electrons in the floating gate
 - B. Presence of Electrons in the floating gate
 - C. Decrease in gate electrical potential due to electron injection into the floating gate.
 - D. Increase in gate electrical potential due to electron removal from the floating gate
 - E. None of the above

Note: Question No. 2 continues on Page 7

(h) Which of the following USB device is paired wrongly with its corresponding USB device class driver?

- A. Mouse - HID
- B. External HDD - MSC
- C. Headset – USB Audio
- D. Virtual COM port on Arduino - CDC
- E. None of the above

(i) Which of the following statement is FALSE?

- A. Given the same number of bits, IEEE754 floating point number has a larger range than a fixed point number.
- B. A 32-bit fixed point number can represent a number nearer to zero compared to a 32-bit single precision IEEE754 number in normalized mode, due to underflow region created by normalization.
- C. Fixed point number has a uniform precision throughout its entire range while that of a floating number varies across the range.
- D. Given the same number of bits, IEEE 754 number is able to have higher precision than that of fixed point number when the number is small
- E. None of the above

(j) Which of the following measures will not improve the transmission range between Bluetooth Host and Device?

- A. Increase Bluetooth Host's transmission power
- B. Move Bluetooth Host away from Wifi Router that is in operation
- C. Shield external interference by putting Bluetooth Device in Metal Case.
- D. Move Bluetooth Host away from any microwave oven that is in operation
- E. None of the above

Appendix 1 - Summary of ARM Instruction Set

Summary	Opcode	Syntax
Move	MOV	MOV{S}{cond} dest, op1 {, SHIFT_op #expression}
Move Negated	MVN	MVN{S}{cond} dest, op1 {, SHIFT_op #expression}
Address Load	ADR	ADR{S}{cond} dest, expression
LDR Psuedo-Instruction	LDR	LDR{S}{cond} dest, =expression
Add	ADD	ADD{S}{cond} dest, op1, op2 {, SHIFT_op #expression}
Add with Carry	ADC	ADC{S}{cond} dest, op1, op2 {, SHIFT_op #expression}
Subtract	SUB	SUB{S}{cond} dest, op1, op2 {, SHIFT_op #expression}
Subtract with Carry	SBC	SBC{S}{cond} dest, op1, op2 {, SHIFT_op #expression}
Reverse Subtract	RSB	RSB{S}{cond} dest, op1, op2 {, SHIFT_op #expression}
Reverse Subtract with Carry	RSC	RSC{S}{cond} dest, op1, op2 {, SHIFT_op #expression}
Bitwise And	AND	AND{S}{cond} dest, op1, op2 {, SHIFT_op #expression}
Bitwise Exclusive Or	EOR	EOR{S}{cond} dest, op1, op2 {, SHIFT_op #expression}
Bitwise Clear	BIC	BIC{S}{cond} dest, op1, op2 {, SHIFT_op #expression}
Bitwise Or	ORR	ORR{S}{cond} dest, op1, op2 {, SHIFT_op #expression}
Logical Shift Left	LSL	LSL{S}{cond} dest, op1, op2
Logical Shift Right	LSR	LSR{S}{cond} dest, op1, op2
Arithmetic Shift Right	ASR	ASR{S}{cond} dest, op1, op2
Rotate Right	ROR	ROR{S}{cond} dest, op1, op2
Rotate Right and Extend	RRX	RRX{S}{cond} op1, op2
Compare	CMP	CMP{cond} op1, op2 {, SHIFT_op #expression}
Compare Negated	CMN	CMN{cond} op1, op2 {, SHIFT_op #expression}
Test Bit(s) Set	TST	TST{cond} op1, op2 {, SHIFT_op #expression}
Test Equals	TEQ	TEQ{cond} op1, op2 {, SHIFT_op #expression}
Load Register	LDR	LDR{B}{cond} dest, [source {, OFFSET}] Offset addressing LDR{B}{cond} dest, [source, OFFSET]! Pre-indexed addressing LDR{B}{cond} dest, [source], OFFSET Post-indexed addressing
Store Register	STR	STR{B}{cond} source, [dest {, OFFSET}] Offset addressing STR{B}{cond} source, [dest, OFFSET]! Pre-indexed addressing STR{B}{cond} source, [dest], OFFSET Post-indexed addressing
Load Multiple Registers	LDM[dir]	LDM[dir]{cond} source, {list of registers}
Store Multiple Registers	STM[dir]	STM[dir]{cond} dest, {list of registers}
Branch	B	B{cond} target
Branch with Link	BL	BL{cond} target
Declare Word(s) in Memory	DCD	name DCD value_1, value_2, ... value_N
Declare Constant	EQU	name equ expression
Declare Empty Word(s) in	FILL	{name} FILL N
Stop Emulation	END	END{cond}

Table 1. Condition code suffixes

Suffix	Flags	Meaning	Suffix	Flags	Meaning
EQ	Z = 1	Equal	VC	V = 0	No overflow
NE	Z = 0	Not equal	HI	C = 1 and Z = 0	Higher, unsigned
CS or HS	C = 1	Higher or same, unsigned	LS	C = 0 or Z = 1	Lower or same, unsigned
CC or LO	C = 0	Lower, unsigned	GE	N = V	Greater than or equal, signed
MI	N = 1	Negative	LT	N != V	Less than, signed
PL	N = 0	Positive or zero	GT	Z = 0 and N = V	Greater than, signed
VS	V = 1	Overflow	LE	Z = 1 and N != V	Less than or equal, signed
VS	V = 1	Overflow	AL	Can have any value	Always. This is the default

END OF PAPER

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Please read the following instructions carefully:

- 1. Please do not turn over the question paper until you are told to do so. Disciplinary action may be taken against you if you do so.**
2. You are not allowed to leave the examination hall unless accompanied by an invigilator. You may raise your hand if you need to communicate with the invigilator.
3. Please write your Matriculation Number on the front of the answer book.
4. Please indicate clearly in the answer book (at the appropriate place) if you are continuing the answer to a question elsewhere in the book.