NANYANG TECHNOLOGICAL UNIVERSITY

SEMESTER 2 EXAMINATION 2016-2017

CE1005/CZ1005 – DIGITAL LOGIC

Apr/May 2017 Time Allowed: 2 hours

INSTRUCTIONS

1. This paper contains 4 questions and comprises 5 pages.
2. Answer **ALL** questions.
3. This is a closed-book examination.
4. All questions carry equal marks.

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1. (a) Represent the signed decimal value -59 in each format below:

(i) 8-bit sign-magnitude

(2 marks)

(ii) 8-bit two's complement

(2 marks)

(b) Determine the 3 bits for code (i) and code (ii) in the following gray code sequence. Briefly state how you arrive at each answer.

000 -> 100 -> code (i) -> 010 -> 011 -> 111 -> code (ii) -> 001 and repeats.

(4 marks)

(c) Simplify the following Boolean expression algebraically. Show each step clearly and give your answer in minimum-cost sum-of-product (SOP) form.

$$Z = (a + b + c)' \, [\, (a + bc' + d')' \, (a'c + b'd') \,]'$$

(8 marks)

Note: Question No. 1 continues on Page 2

(d) A logic circuit has four inputs: w, x*, y*, z and one output F*. * denotes active-low signals. The output F* is asserted only when at least three of the four inputs are asserted. Otherwise F* is negated.

(i) Write the canonical product-of-maxterm expression for output F*.

(2 marks)

(ii) Using appropriate logic symbols, sketch a logic circuit diagram to clearly illustrate the input conditions for F* to be asserted. You are not required to simplify the circuit.

(5 marks)

(iii) An active-low enable input EN* is to be added to the circuit in Q1(d)(ii) such that the new output G* is High whenever EN* is High, regardless of the inputs w, x*, y*, z. When EN* is Low, G* follows the same logic level as F*. Sketch a diagram to show how this may be achieved.

(2 marks)

2. (a) A Schmitt-trigger buffer has threshold voltages V_{T-} and V_{T+}, where $V_{T-} < V_{T+}$.

Sketch a set of input and output waveforms to clearly illustrate how the buffer output may change from logic 0 to 1 and back to 0 as the input voltage of the buffer changes.

Show also in your sketch how the output may respond to minor input voltage fluctuations around V_{T-} and V_{T+}.

(7 marks)

(b) Use Karnaugh map to simplify the following Boolean expression and obtain a minimum-cost sum-of-product expression. Show each loop on the Karnaugh map clearly.

$$F(a, b, c, d) = a'c'd' + a'bc + a'b'cd + ab'c'd'$$

(8 marks)

Note: Question No. 2 continues on Page 3

(c) A logic device that performs unsigned magnitude comparison is available. It compares two 4-bit inputs A and B, and produces an output U such that U is 1 if the magnitude of A is larger than or equal to that of B. Otherwise U is 0. Table Q2a gives several examples of the comparator's behavior. You are not required to design this comparator.

Table Q2a: Unsigned 4-bit comparison

Input A3,A2,A1,A0	Input B3,B2,B1,B0	Comparison result	Output U
1 0 1 0	1 0 1 0	A = B	1
1 0 0 0	0 1 1 1	A > B	1
0 1 0 0	1 0 0 1	A < B	0

A logic circuit is required to compare two 5-bit signed numbers X and Y, both in two's-complement representation. The circuit output W is 1 only when the numerical value represented by X is larger than or equal to that represented by Y. Otherwise W is 0. Table Q2b gives several examples of the circuit's behavior.

Table Q2b: Signed 5-bit two's complement comparison

Input X4,X3,X2,X1,X0	Input Y4,Y3,Y2,Y1,Y0	Comparison result	Output W
0 1 0 1 0	0 1 0 1 0	X = Y	1
0 0 1 1 1	1 1 0 0 0	X > Y	1
1 0 1 0 0	1 1 0 0 1	X < Y	0

(i) Design the required 5-bit circuit using logic gates and the available 4-bit comparator. Sketch a logic circuit diagram to clearly illustrate your design. Label all logic signals clearly. You may use a block diagram for the 4-bit comparator.

(6 marks)

(ii) Briefly describe how your circuit in Q2(c)(i) works.

(4 marks)

3. (a) Identify and correct the errors in the following combinational Verilog module.

```
module finderrors (input [2:0] a, b, c,
                   input [1:0] sel,
                   output  [1:0] result);
                always @ (a,b,c)
                begin
                        case (sel)
                        2'b00 : result <= a;
                        2'b01 : result = b;
                        2'b10 : result = c;
                        endcase
                end
        endmodule
```

(7 marks)

(b) What is wrong with the following combinational Verilog module? Fix the module such that it produces the desired circuit when synthesized.

```
module fixit (input p, q, r, z,
                    output  reg X, Y);
                always @ *
                begin
                        if(p)
                          X = q & r;
                        else
                          begin
                           X = z;
                           Y= q ^ z;
                           end
                end
        endmodule
```

(6 marks)

(c) (i) Draw a schematic diagram to show how the function ***F(a,b,c)*** = ***a'b'c'*** + ***a'bc'*** + ***ab'c'*** + ***abc*** is implemented using only a 8x1 multiplexer.

(5 marks)

(ii) Write the Verilog module for ***F*** in Q3(c)(i) using a **case** statement.

(7 marks)

4. (a) An autonomous vehicle developed in NTU moves students between five designated locations across the campus. The movement of the vehicle is controlled by a 1-bit input *MOVE* which is sent wirelessly from the control room. The 3-bit output *LOC* of the FSM shows the current location of the autonomous vehicle. Table Q4 shows the rules to perform a test run of this vehicle which will start from location SCSE.

Table Q4

Current Location	**Next Location**	
	MOVE = 0	***MOVE = 1***
SCSE	Student Gym	Innovation Center
Student Gym	SCSE	Auditorium
Auditorium	Auditorium	Library
Innovation Center	SCSE	Library
Library	Innovation Center	Auditorium

(i) Draw a Finite State Machine (FSM) for the autonomous vehicle.

(6 marks)

(ii) What should be the input sequence such that the vehicle visits each location once and returns to SCSE?

(2 marks)

(iii) Write the Verilog module for the *FSM* designed in Q4(a)(i) with inputs *MOVE, RESET, CLK* and output *LOC*. Assume the vehicle returns to SCSE when *RESET* is high.

(10 marks)

(b) Write the Verilog module *PISO* which is a parallel-in/serial-out register. The inputs to the module are *IN[3:0]*, *CLK* and *LOAD*. When *LOAD* is high, the register is loaded with the value of *IN*. The output of this module is *OUT*.

(7 marks)

END OF PAPER

(a) i) 1111 1011

ii) 1100 0101

b) Code i = 110

Code ii = 101

c) $Z = (a+b+c)'[(a+bc'+d')'(a'c+b'd')]'$

$= (a'b'c')[(a+bc'+d')+(a'c+b'd')']$

$= (a'b'c')[a+bc'+d'+(a+c')(b+d)]$

$= (a'b'c')[a+bc'+d'+ab+ad+c'b+c'd]$

$= (a'b'c')[a+d'+c'(b+d)]$

$= 0 + a'b'c'd' + a'b'c'(b+d)$

$= a'b'c'd' + 0 + a'b'c'd$

$= a'b'c'(d'+d)$

$= a'b'c'$ //

d)

in	w	x	y	z	out	F
	0	0	0	1		0
	1	1	0	1		0
	1	0	1	1		0
	1	1	1	0		0

wx \ yz	00	01	11	10
00	1	0	1	1
01	1	1	1	1
11	1	0	1	0
10	1	1	0	1