Note: Do not refer to the processor configuration in the case study notes for this tutorial. A smaller system will be used instead.

8.1 Cache

1. Given a processor system with the following characteristics
   - Processor has a direct-mapped cache with 32 cache blocks and a cache size of 512 bytes.
   - Cache Memory Access time = 5ns.
   - Cache Hit rate = 0.9
   - 64Kbyte DRAM used as the main memory.
   - DRAM Memory access time = 200ns

   a. In doing cache mapping analysis, how many **blocks** would the main memory be partitioned to?

   512 ÷ 32 = 16 bytes $64 \times 2^{10} \div 16 = 4096$

   b. What is the format of a memory address as seen by the cache (i.e. determine the sizes of the tag, block and offset fields)?

   7 | 5 | 4

   1101 1011 01100011

   c. CPU needs to read a byte from main memory address 0xDB63.

      i. Which cache block would CPU looked at to search for the required data? 22
      ii. How many main memory blocks could potentially be mapped to the same cache block as that of 0xDB63? 128
      iii. How does the CPU knows if the cache block identified in (i) above contains the data that it needs? Tag
      iv. What is the purpose of the 'offset' field in the cache mapping? find exact loc

   d. What is the effective access time of the memory in this system?

   5 ns + 0.1 x 200 ns = 25 ns

8.2 Virtual Memory

2. In a processor system with the following characteristics,
   - 1 MByte Virtual memory space → 20
   - 64 Kbyte DRAM as main memory → 16
   - Paging scheme used for virtual memory management, Page Table as shown in Table 8.2
   - Virtual Page size = 1 KByte → 10
   - TLB with 4 entries

Table 8.2 – Page Table

Virtual Page Number	Valid Bit	Page Frame Number
0	1	1
1	1	2
2	0	-
3	1	16
4	1	9

a. How many bits are required for each virtual address?
20

b. How many bits are required for each physical address?
16

c. What is the maximum number of entries in the page table in Table 7.2?
$2^{20} \div 2^{10} = 1024$

d. What is the maximum number of valid entries in the page table in Table 7.2?
64

e. With reference to Table 7.2, answer the following. Indicate when a page fault occurs.

0x5F0 = 0101 1111 0000
0x6FF = 0110 1111 1111
1001 1111 0000 → 9F0
1010 1111 1111 → AFF

(i) The compiler mapped the UART routine to virtual address 0x005F0 – 0x006FF, where in the DRAM would you be able to find the UART routine?

0x9C0 = 1001 1100 0000
0x9DF = 1001 1101 1111
Invalid.

(ii) The compiler mapped the I2C routine to virtual address 0x009C0 - 0x009DF, where in the DRAM would you be able to find the I2C routine?

(iii) What happens when there is a page fault?

f. What memory are the Page Table and TLB resided?
↳ mm ↳ Fast system

g. What is the function and effect of a TLB?
Speed

(Not necessary to be covered during tutorial)

[Optional, but students are encouraged to attempt these questions]

3. Consider a system with the following characteristics.
   - Direct mapped cache of 32 cache blocks and cache block size of 32 bytes
   - Cache uses Physical Address for address mapping
   - Virtual Memory page size 2048 bytes
   - Virtual Memory size is 1Mbyte. Physical Memory size is 64KByte
   - Extracts of Page Table (valid entries)
     - Virtual Page 0 → Physical Frame 9
     - Virtual Page 1 → Physical Frame 3
     - Virtual Page 2 → Physical Frame 5
     - Virtual Page 3 → Physical Frame 2
     - Virtual Page 4 → Physical Frame 7
   - The main program is 5KByte in size and starts at virtual address 0x01006

   (i) Assuming that the compiler allocates the program sequentially in the virtual memory, what is the physical address of the start and end of the main program?

   (ii) Which cache block should the CPU check in the cache for the start of the main program? What is the corresponding TAG value used to check for cache hit/miss?

(Not necessary to be covered during tutorial)

[Optional, but students are encouraged to attempt these questions]

3. Consider a system with the following characteristics.
    - Direct mapped cache of 32 cache blocks and cache block size of 32 bytes
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    - Virtual Memory size is 1Mbyte. Physical Memory size is 64KByte
    - Extracts of Page Table (valid entries)
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    (i) Assuming that the compiler allocates the program sequentially in the virtual memory, what is the physical address of the start and end of the main program?

    (ii) Which cache block should the CPU check in the cache for the start of the main program? What is the corresponding TAG value used to check for cache hit/miss?