LABORATORY MANUAL

SC1005 : Digital Logic

[Location: Hardware Laboratory 3, N4-B1a-05]

Experiment 2 :

4-bit Adder/Subtractor Circuit with MSI Binary Adder

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COMPUTER ENGINEERING COURSE
COMPUTER SCIENCE COURSE

SCHOOL OF COMPUTER SCIENCE & ENGINEERING
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4-BIT ADDER/SUBTRACTOR CIRCUIT WITH 74LS283

1. OBJECTIVES

1.1 To investigate the logic behaviour of the 74LS283 4-bit binary adder integrated circuit.

1.2 To build an adder/subtractor circuit using the binary adder IC.

1.3 To observe overflow in 2’s complement arithmetic.

2. LABORATORY

This experiment is conducted at **Hardware Laboratory 3**, N4-B1a-05.

3. EQUIPMENT

3.1 Instruments

RDA 2008A Digital-Analog Trainer
Oscilloscope
Digital Multimeter (DMM)

3.2 Components

Component		Unit Cost (in S$ for 100+ devices)
74LS283 IC	4-bit binary adder	0.75
74LS86 IC	Quad two-input exclusive-OR	0.45
74LS08 IC	Quad two-input AND	0.45
74LS32 IC	Quad two-input OR	0.45
74LS04 IC	Hex inverter	0.45

4. INTRODUCTION

4.1 In Experiment 1, you have implemented a full adder using SSI (small-scale integration) integrated circuit logic components such as AND, OR and XOR.

A full adder is only capable of adding 3 bits together. In most situations, a parallel adder (Figure 1) is needed to add two multi-bit values together. Implementing a parallel adder using SSI components will be too cumbersome and time consuming. Instead, you will implement it using an MSI (medium-scale integration) component 74LS283.

Note: SSI packs up to 10 logic gates into a component; MSI packs up to 100 logic gates into a component.

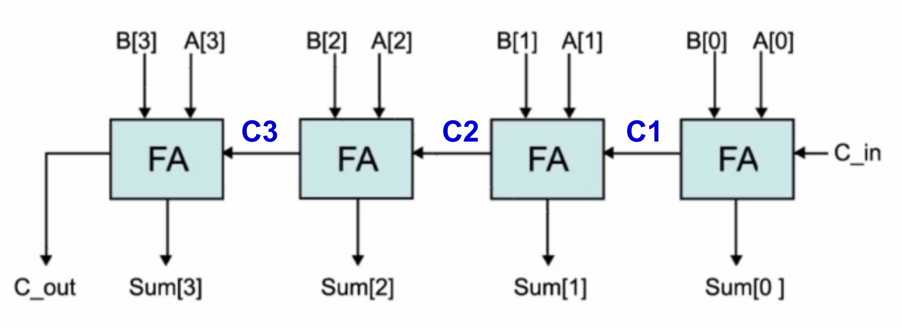


Figure 1: 4-bit parallel adder comprising 4x full adders

The 74LS283 is a 4-bit binary adder with fast carry. Figure 2 shows its functional block diagram.

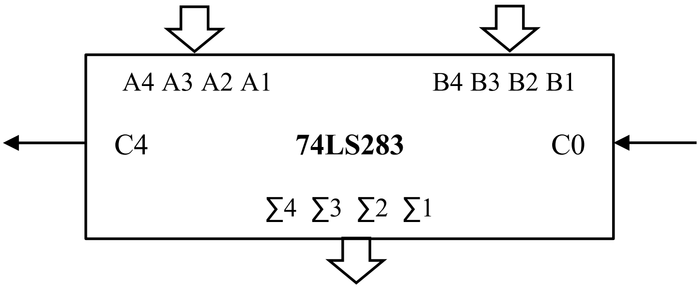


Figure 2: 4-bit adder integrated circuit

The 74LS283 device takes in two 4-bit values A and B, a carry input C0, and perform arithmetic addition as follows to produce a 4-bit result ∑ and a carry out bit C4. A4, B4 and ∑4 are the most significant bits.

		C3	C2	C1	C0
		A4	A3	A2	A1
+		B4	B3	B2	B1
	C4	∑4	∑3	∑2	∑1
		msb			lsb

C3, C2 and C1 are the carry bits that would be generated if four separate full adders are used to carry out the addition (e.g. in Figure 1). The 74LS283 integrated circuit does **NOT** provide these three signals as part of its output. They are included here to provide a clear illustration of the arithmetic addition of multi-bit values.

Example 1: if A=0011, B=0111, C0=1, the addition will be:

		1	1	1	1
		0	0	1	1
+		0	1	1	1
	0	1	0	1	1

Example 2: if A=1011, B=0111, C0=0, then the addition will be:

		1	1	1	0
		1	0	1	1
+		0	1	1	1
	1	0	0	1	0

4.2 The 74LS283 device merely adds a pair of binary values. The interpretation of the values are determined by the human user, not by the device.

In the two examples above, the decimal equivalent of the values depend on the number representation adopted by the human. This is illustrated in Table 1.

Table 1

	Human interpretation of values	
Binary values	Unsigned decimal	Signed decimal in two's complement representation
Example 1		
C0=1	1	1
A=0011	3	+3
B=0111	7	+7
∑=1011	11	-5
C4=0	0	C4 is ignored
		Note: overflow
Example 2		
C0=0	0	0
A=1011	11	-5
B=0111	7	+7
∑=0010	2	+2
C4=1	16	C4 is ignored
	Note: C4 has value	

4.3 In 2's complement arithmetic, the subtraction X-Y can be evaluated by X + (2's complement of Y). The 2's complement of Y can be obtained by inverting every bit of Y (i.e. 1's complement of Y) and add 1.

Example 3: if X=1000, Y=1101, X-Y is performed as such:

		0	0	0	1	C0=1
		1	0	0	0	
+		0	0	1	0	(1's complement of Y)
	0	1	0	1	1	

In this example, the signed decimal interpretation is: -8 – (-3) = -5

4.4 In this experiment, you will use the 74LS283 to implement a circuit that can perform two's complement addition/subtraction. To prepare for the lab, you are expected to refer to the datasheet of the device to note down the pin numbers for the various inputs and outputs. Record the pin numbers in Table 2 for reference. Most of the pin numbers are already recorded for you.

Table 2: 74LS283 pinouts

Pin function	**Pin name**	**74LS283 pin number**
Power supply	Vcc	16
Ground	Gnd	8
Carry input	C0	? 7
4-bit operand	A4, A3, A2, A1	12, 14, 3, 5
4-bit operand	B4, B3, B2, B1	11, 15, 2, 6
Sum output	$\sum$4, $\sum$3, $\sum$2, $\sum$1	10, 13, 1, 4
Carry output	C4	? 9

4.5 In two's complement arithmetic, overflow may occur in some cases. This happens when the result falls outside the range of values that can be represented given the number of bits.

Given n bits, the range of signed decimal values that can be represented in two's complement is:

$$\{ -(2^{n-1}), 2^{n-1} -1 \}$$

For example, if n=8, the range will be -128 to +127. Adding +98 with +99 will produce a result of +197 which cannot be represented in 8 bits. This means there is an overflow.

Arithmetic overflow can be easily detected by comparing the sign of the operands with the sign of the arithmetic result. Refer to example 1 in Table 1. When +3 is added with +7 as well as a carry input, the expected result is +11. Since the largest value that can be represented in 4 bits is +7, this is oviously a case of overflow. This can be seen from the binary result $\sum$=**1**011, which shows the sign bit as 1, contradicting with the positive sign bit of the two operands +3 and +7.

Since both subtraction and addition are performed as addition in the adder/subtractor circuit, the same method for overflow detection is used regardless whether the circuit performs X+Y or X-Y (which is essentially X+Y'+1).

5. EXPERIMENT

5.1 4-BIT BINARY ADDER

5.1.1 Figure 3 shows the experiment setup. Refer to steps 1-6 of *Lab 2 circuit connection guide.pdf* for a pictorial guide.

Mount one unit of the 74LS283 device on the breadboard. Connect its Vcc to 5V and Gnd to 0V. Connect one toggle switch to each of the inputs A4, A3, A2, A1, B4, B3, B2, B1 and C0. Connect one LED to each of the outputs ∑4, ∑3, ∑2, ∑1 and C4. Refer to Table 2 for the pin numbers and *Lab 2 Circuit connection guide.pdf* (steps 1 – 6).

Be very careful in connecting the switches/LEDs in the correct physical order (msb on the left, lsb on the right) so that it is **easier for you** to observe the input and output values.

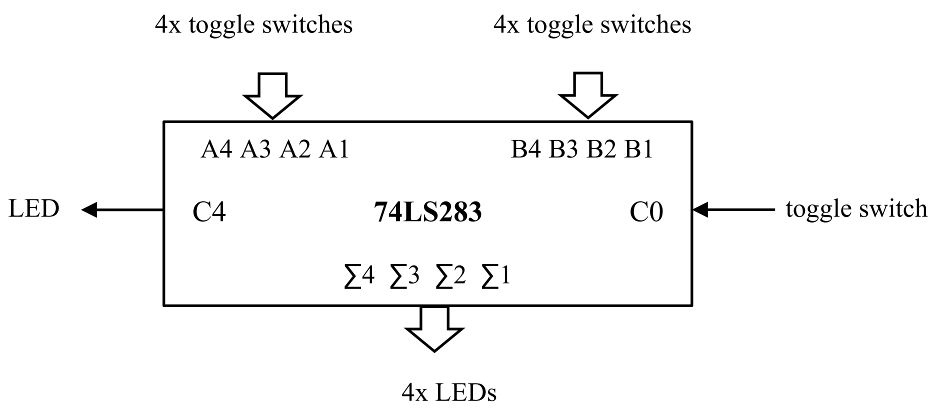


Figure 3: 4-bit binary adder with toggle switches and LEDs connected

5.1.2 Power up the circuit and check that it is adding correctly. Table 3 shows the values from the three examples in Section 4 that you may use to verify the results.

Table 3

	Inputs			Outputs	
Examples	A	B	C0	C4	∑
1	0011	0111	1	0	1011
2	1011	0111	0	1	0010
3	1000	0010	1	0	1011
4	0101	1010	1	1	1000
5	1110	1001	1	1	1000

Determine the output values of examples 4 & 5 in Table 3.

Pause and think: What is the largest binary result that can be obtained from this circuit? What is its decimal equivalent assuming unsigned representation is used?

Assessment (a): student to demonstrate addition circuit

5.2 <u>4-BIT 2'S COMPLEMENT ADDITION/SUBTRACTION CIRCUIT</u>

5.2.1 The next few steps will modify the circuit you have built in section 5.1 such that it can perform 2's complement addition (X+Y) and subtraction (X-Y), as shown in Figure 4. For your convenience, the pin numbers on the 74LS283 device are provided.

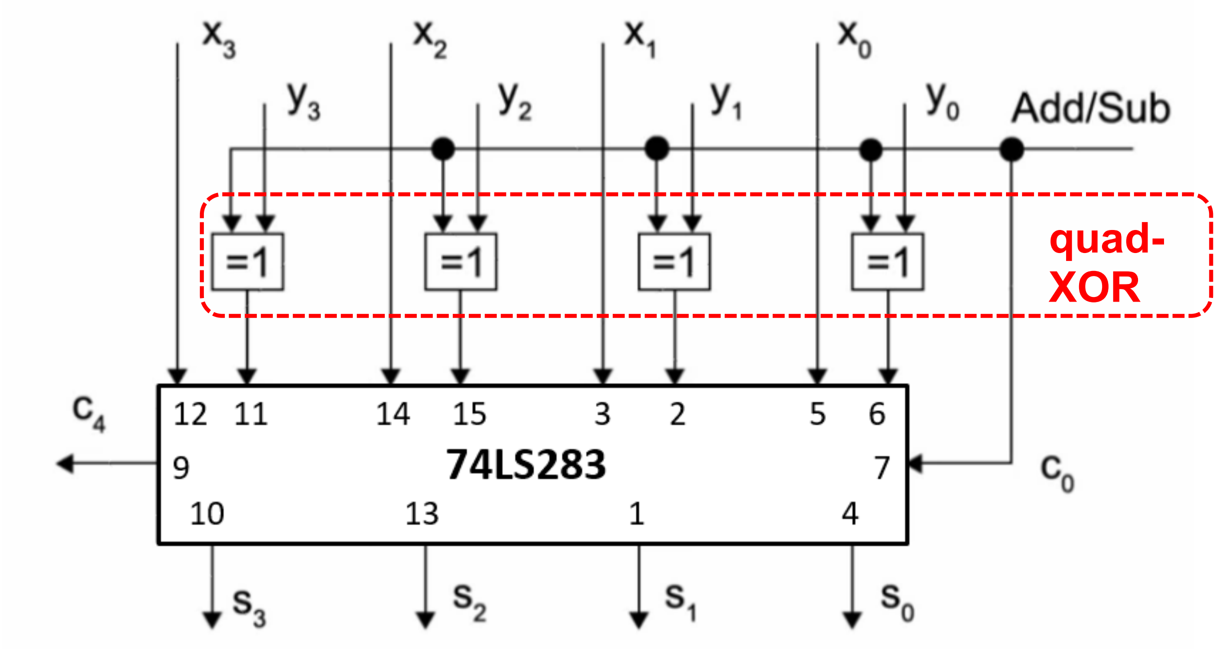


Figure 4: 4-bit adder/subtractor circuit

5.2.2 Refer to steps 7-11 of *Lab 2 circuit connection guide.pdf* for a pictorial guide. Mount a 74LS86 IC (quad XOR) on the circuit board and connect its Vcc and GND to 5V and 0V respectively..

5.2.3 <u>Remove</u> the connections between the toggle switches and inputs B4,B3,B2,B1 in Figure 3. Instead, connect these toggle switches to one input of each of the four XOR gates on the 74LS86 IC. These form the inputs y3, y2 y1,y0 in Figure 4.

5.2.4 Connect the other input of each of the four XOR gates together, and connect it to the same toggle switch that has been earlier connected to C0 in section 5.1 (see Figure 3). This forms the Add/Sub input in Figure 4.

5.2.5 Connect the output of each of the four XOR gates to inputs B4,B3,B2,B1 of the binary adder device, in the correct order.

5.2.6 In the connections above, take special care to ensure that the inputs y3, y2, y1 and y0 (from toggle switches) enter the inputs B4,B3,B2,B1 of the binary adder device <u>via the XOR gates</u>, in the **correct order from msb to lsb. Many students make connection error for this part.**

5.2.7 Power up the circuit and check that it is adding and subtracting correctly.

Pause and think: What purpose do the XOR gates serve? What should be the correct logic level (0 or 1) at the input Add/Sub for addition and subtraction, respectively?

1 1
0 1 1 1
0 1 1 0
1 1 0 1

c4 c3 c2 c1
1 1 0 0
0 1 1 0
~~1~~ 0 0 1 0

1010
0110
~~1 0 1 0~~
0 1 0 1
1
0 1 1 0

1100 - 1010
$\underbrace{1100}_{100}$ + 0110
-4 + 6 = 2

0001 1 | 1001 9
0010 2 | 1010 10
0011 3 | 1011 11
0100 4 | 1100 12
0101 5 | 1101 13
0110 6 | 1110 14
0111 7 | 1111 15
1000 8

0 1010
1 0110
1010

Toggle the switches to vary the inputs (x, y, Add/Sub) and observe the corresponding outputs on the LEDs. Verify that the circuit is correct by using the test cases in Table 4. Calculate the expected results. Are the observed results same as what you have expected? Are you able to determine the overflow cases?

30: x
40: T

Table 4

Test case	x +/- y	Calculated Sum	S3 S2 S1 S0	C4	Overflow (Y/N)
1	0 1 0 1 + 0 0 0 1	0 1 1 0	0 1 1 0	0	N
2	0 1 0 1 - 0 0 0 1	4 0 1 0 0	0 1 0 0	1	N
3	0 0 0 1 - 0 1 0 1	-4 1 1 0 0	1 1 0 0	0	N
4	1 1 1 1 – 0 0 0 1	-2 1 1 1 0	1 1 1 0	1	N
5	0 1 0 1 + 0 1 0 0	9 1 0 0 1	1 0 0 1	0	Y
-5-5=-10 6 -101	1 0 1 1 – 0 1 0 1	-10 1 0 1 1 0	0 1 1 0	1	Y
7	1 0 1 1 – 1 0 0 0	-4 0 0 1 1	0 0 1 1	1	N
8	1 0 1 1 + 1 0 0 0	-13 1 0 0 1 1	0 0 1 1	1	Y

-5 -8

Assessment (b): student to demonstrate addition/subtraction circuit

if 1 + 1 = 0 0 + 0 = 1

1 - 0 = 0

5.3 IMPLEMENTATION OF AN OVERFLOW BIT (OPTIONAL)

Complete this part only if time permits and you have understood the earlier parts of this experiment.

5.3.1 Obtain a Boolean expression for output V, such that V=1 when there is an overflow in the result of the add/subtractor circuit in section 5.2. V=0 when there is no overflow.

Hint: both subtraction and addition are performed as addition by the circuit. If the sign bits A4 and B4 are the same, but different from S3, then it is a clear indication of overflow. You may make use of XOR to compare two bits.

5.3.2 Implement the Boolean expression of V obtained in 5.3.1. Connect output V to an LED. Additional logic components are available for the implementation.

5.3.3 Power up the circuit and check that the overflow bit is working correctly by comparing with the entries made earlier in Table 4.

5.3.4 Pause and think: Is V = C4? Why?

XOR →

6. PREPARATION AND OBSERVATIONS

Maintain proper records of your preparation (e.g. circuit connection diagram for the 74LS86 IC) and observations (e.g. truth tables) throughout the experiment. You may refer to these records during the lab quiz.

7. LAB ASSESSMENT AND QUIZ

Each student is required to demonstrate the completion of sections **5.1 and 5.2** to the lab instructor.

There will be a 10-minute written lab quiz at the end of this experiment. The quiz will include (but not limited to) concepts, components, equipment and observations covered in this experiment.

8. REFERENCES

8.1 SC1005 Digital Logic Supplementary Laboratory Manual – Wiring & Troubleshooting Digital Circuits.

8.2 SC1005 Lab 2 circuit connection guide.pdf, Digital Logic Couse Site, NTULearn.

8.3 Digital Design Principles and Practices, Ed. 4, John F Wakerly, Prentice Hall, 2007.

8.4 Fundamentals of Digital Logic with Verilog Design, 2nd Ed., by Stephen Brown and Zvonko Vranesic, McGraw Hill, 2008.

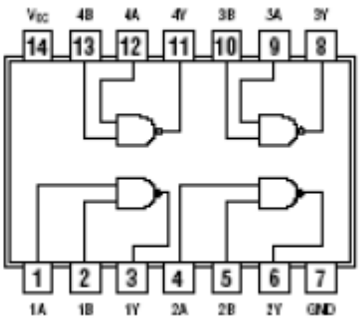
8.5 https://byjus.com/boolean-algebra-calculator/ (free online tool)

Appendix

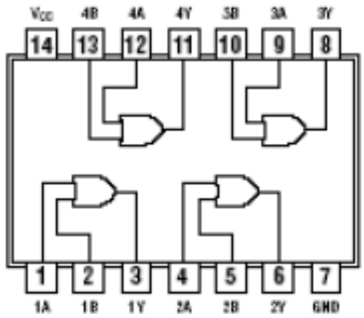
<u>Pin assignments (from TI Digital Logic Pocket Data Book 2003)</u>

Follow the pinouts when connecting up a logic component

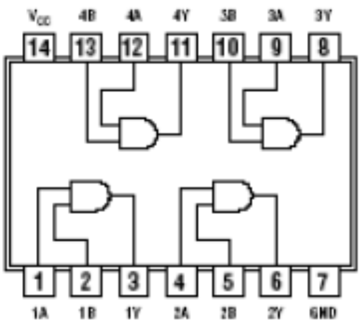
7400: quad 2-input NAND



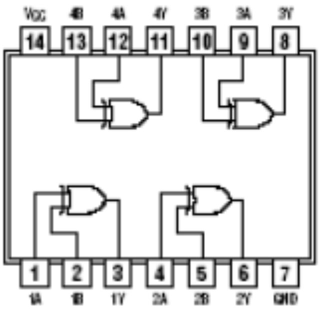
7432: quad 2-input OR



7408: quad 2-input AND



7486: quad 2-input XOR



7404: hex inverter