

SC1005 Digital Logic revision Practice Problems

1.

- 3-32. A jet aircraft employs a system for monitoring the rpm, pressure, and temperature values of its engines using sensors that operate as follows:

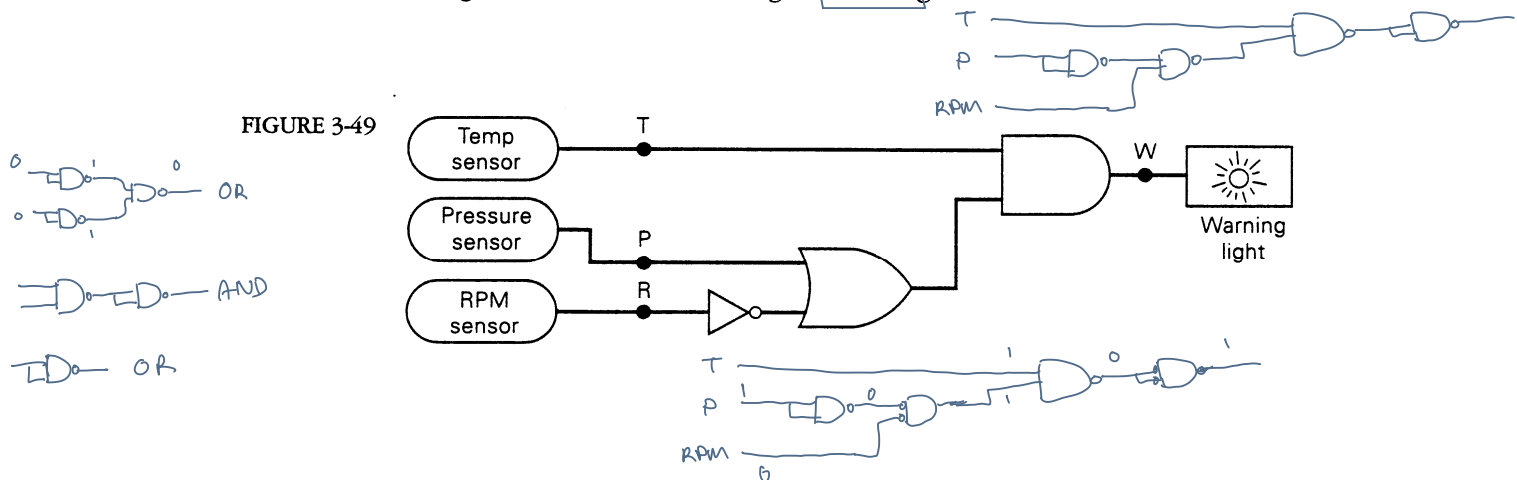
RPM sensor output = 0 only when speed < 4800 rpm

P sensor output = 0 only when pressure < 220 psi

T sensor output = 0 only when temperature < 200°F

Figure 3-49 shows the logic circuit that controls a cockpit warning light for certain combinations of engine conditions. Assume that a HIGH at output *W* activates the warning light.

- (a) Determine what engine conditions will give a warning to the pilot. $T \cdot (P + R')$
 (b) Change this circuit to one using all NAND gates.



2. An alarm system operates such that the alarm output is HIGH whenever
- the PANIC input is HIGH, or
 - the ACTIVATE input is HIGH while the EXITING input is LOW, and the house is not secure.

The house is secure when the WINDOW, DOOR and GARAGE inputs are all HIGH. Write the logic expression for the ALARM output without using truth table.

$$\text{Alarm} = \text{Panic} + (\text{Activate} \cdot \text{Exiting}' \cdot (\text{window} + \text{door} + \text{garage})')$$

3. A shopping centre carpark has the following redemption scheme: A customer may redeem the carpark fee either at anytime on Sunday, or after 5pm on any day. However, he/she must have made a purchase above \$50 at the shopping centre to qualify for the redemption.

Using the input Boolean variables **Sunday**, **After5** and **Above50**, express the output **Redeem** as a Boolean function of **Sunday**, **After5** and **Above50**. All input and output signals are logic 1 when the corresponding condition is true, i.e. active High.

$$\text{Redeem} = \text{Above50} \cdot (\text{Sunday} + \text{After5})$$

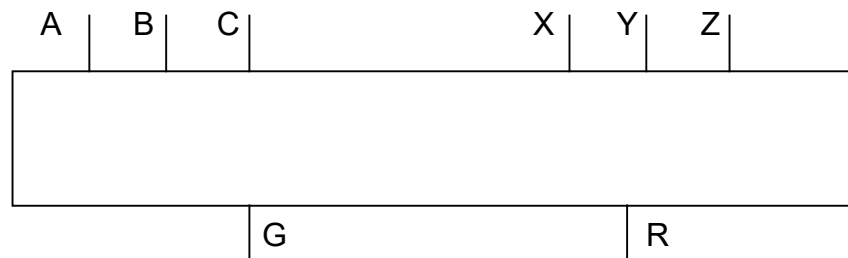
$$\text{Redeem}^* = \text{Above50}^* + (\text{Sunday}^* \cdot \text{After5}^*)$$

Rewrite **Redeem*** as a function of **Sunday***, **After5*** and **Above50*** assuming all input and output signals are active low, i.e. true when low.

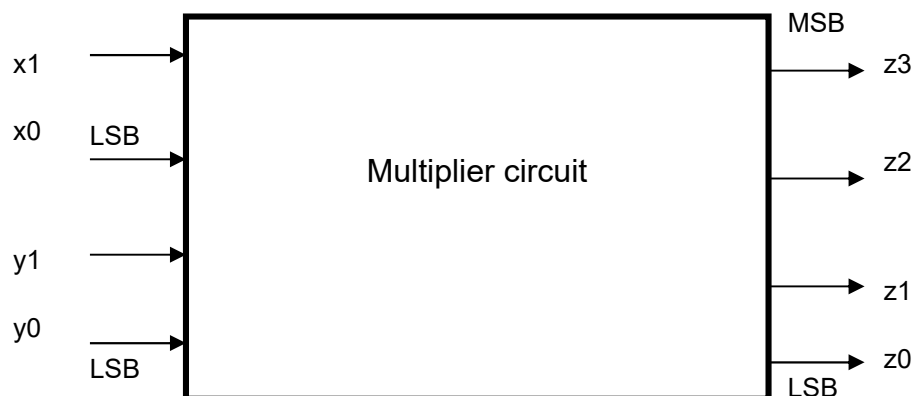
4. A certain logic circuit in the NASA shuttle is supposed to turn ON a green indicator in the astronauts' cabin to indicate that the pressure in the fuel tanks is equal to the desired pressure for lift-off. The desired pressure is set by the on-board computer and is contained in a 3-bit binary number ABC. A transducer monitors the pressure in the fuel tanks and relays this information to the computer via another 3-bit binary number XYZ. Design the logic circuit necessary to turn on the green indicator G.

$$6 = 110$$

The weight of the LSB of the number XYZ is equivalent to 100 psi. Design the necessary logic for the situation if a red indicator R is to turn ON when the pressure in the tanks rises above 600 psi.



5. The following figure shows a multiplier circuit that takes two 2-bit binary numbers x_1x_0 and y_1y_0 and produces an output binary number $z_3z_2z_1z_0$ that is equal to the arithmetic product of the two input numbers. Design the logic circuit for the multiplier.

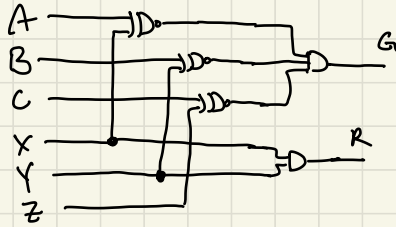


$$11 = 3 \times 3 = 9 = 1000$$

4)

$$I + XYZ = ABC, G=1$$

$$XYZ > 110, R=1$$



5)

X_1	X_0	Y_1	Y_0	Z_3	Z_2	Z_1	Z_0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0
0	0	1	0	0	0	0	0
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	0
0	1	0	1	0	0	0	1
0	1	1	0	0	0	1	0
0	1	1	1	0	0	1	1
1	0	0	0	0	0	0	0
1	0	0	1	0	0	1	0
1	0	1	0	0	1	0	0
1	0	1	1	0	1	1	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	1	1
1	1	1	0	0	1	1	0
1	1	1	1	1	0	0	1

$$Z_3 = X_1 X_0 Y_1 Y_0$$

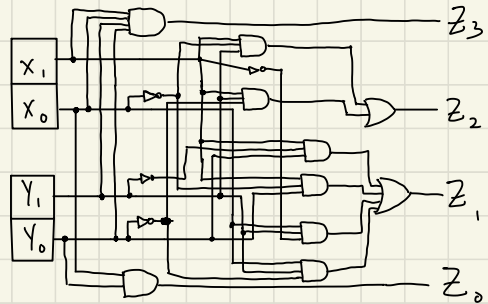
$$Z_2 = X_1 X_0' Y_1 + X_1 Y_1 Y_0'$$

$$Z_1 = X_1 Y_1' Y_0 + X_1 X_0' Y_0' + X_1 X_0 Y_1 + X_0 Y_1 Y_0'$$

$$Z_0 = X_0 \cdot Y_0$$

	$Y_1 Y_0$			
$X_1 X_0$	00	01	11	10
00				
01				
11				1
10			1	1

	$Y_1 Y_0$			
$X_1 X_0$	00	01	11	10
00				
01			1	1
11		1	1	1
10		1	1	1



6. Design a circuit with 5 inputs (A^* , B, C, D^* , E) and 2 outputs (X, Y^*).

Y^* is asserted when at least one of the following conditions are met:

- B is asserted and C is negated;
- D^* is asserted

Otherwise, Y^* is negated.

X is asserted when B is negated, and at the same time, at least one of the following conditions are met:

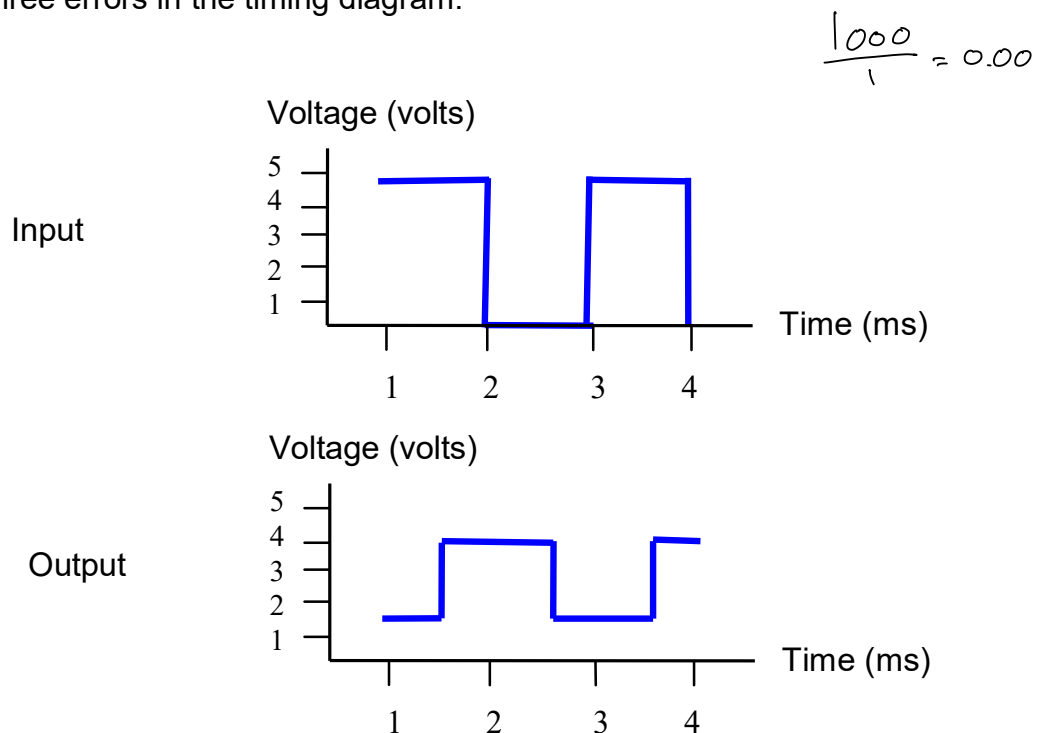
- Both A^* and E are asserted;
- D^* is negated

Otherwise, X is negated.

(a) Draw the K map for X and Y^* .

(b) Write the minimized POS for X and SOP for Y^* .

7. The input of a TTL inverter is a 1 kHz squarewave. The following timing diagram is supposed to show the observed input and output. Point out and correct the three errors in the timing diagram.



8. Simplify the following 5-variable logic expression using Karnaugh map:

$$Z = A'B'CE' + A'B'C'D' + B'D'E' + B'CD' + CDE' + BDE'$$

6. Design a circuit with 5 inputs (A^* , B , C , D^* , E) and 2 outputs (X , Y^*).

Y^* is asserted when at least one of the following conditions are met:

- B is asserted and C is negated;
- D^* is asserted

Otherwise, Y^* is negated.

X is asserted when B is negated, and at the same time, at least one of the following conditions are met:

- Both A^* and E are asserted;
- D^* is negated

Otherwise, X is negated.

(a) Draw the K map for X and Y^* .

(b) Write the minimized POS for X and SOP for Y^* .

$$\begin{aligned} X &= B' \cdot (A^*E + D^{*'}) \\ &= B' \cdot (A^*D^{*'} + E D^{*'}) \\ &= A^*B'D^{*'} + B'D^{*'}E \end{aligned}$$

$$Y^* = (BC') + D^*$$

X

		$D^* E$			
		00	01	11	10
$A^* B$	00	1	1	1	1
	01	0	0	0	0
	11	0	0	0	0
	10	0	0	1	1

$$X = B' (A^* + D^*) (D^* + E)$$

8. Simplify the following 5-variable logic expression using Karnaugh map:

$$Z = A'B'CE' + A'B'C'D' + B'D'E' + B'CD' + CDE' + BDE'$$

$$Z = B'A'CE' + B'A'C'D' + B'D'E' + B'CD' + (B+B)CDE' + BDE'$$

B

	DE			
	00	01	11	10
AC	00			1
	01			1
	11			1
	10			1

B'

	DE			
	00	01	11	10
AC	00			
	01			1
	11			1
	10			

Answers

1. a) $W = T \bullet (P + R')$

b) 4 x 2-input NAND gates required.
2. $ALARM = PANIC + [ACTIVATE \bullet EXITING' \bullet (WINDOW \bullet DOOR \bullet GARAGE)']$
3. Redeem = Above50 (Sunday + After5)
 $Redeem^* = Above50^* + (Sunday^*)(After5^*)$
4. $G = (A \text{ XNOR } X) \text{ AND } (B \text{ XNOR } Y) \text{ AND } (C \text{ XNOR } Z)$
 $R = XY$
5. msb $z3 = x1.x0.y1.y0$
lsb $z0 = x0.y0$
 $z1 = x1.y1'.y0 + x1.x0'.y0 + x1'.x0.y1 + x0.y1.y0'$
 $z2 = x1.x0'.y1 + x1.y1.y0'$
6. $X = B' (A^* + D^*) (D^* + E)$
 $Y^* = D^*B' + D^*C$
7. Errors:
 1. frequency
 2. Voltage range
 3. input/output time relation.
8. $Z = A'B'D' + B'D'E' + B'CD' + CDE' + BDE'$