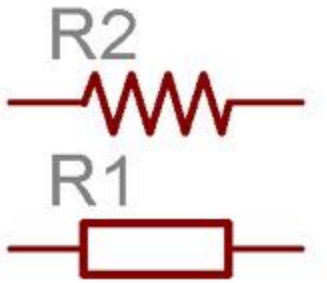
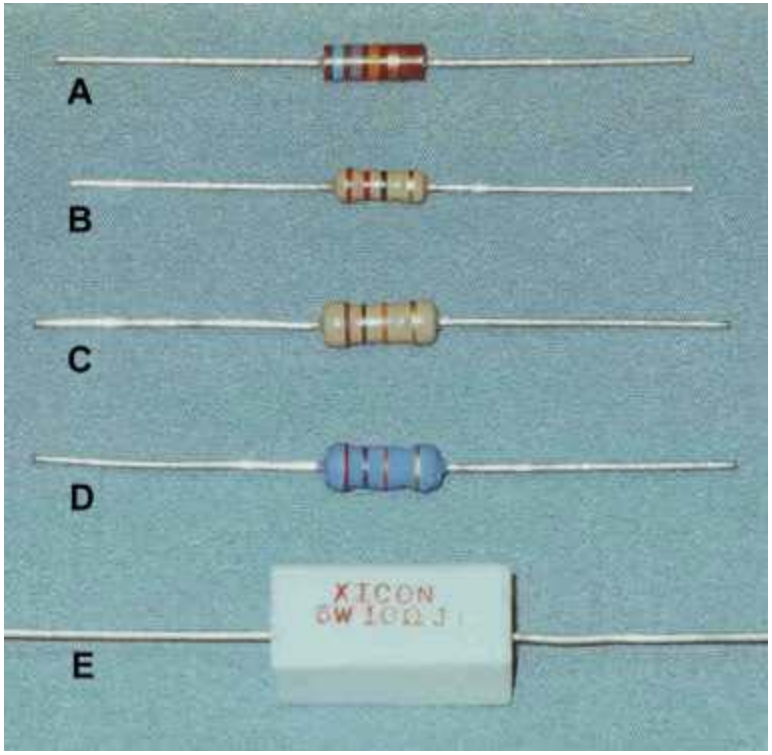
6. Digital Circuits

Integrated digital circuits are

- **made up of a collection of resistors, diodes and transistors**
- **fabricated on a single piece of semiconductor material (e.g. silicon) called substrate - also called die, or chip**

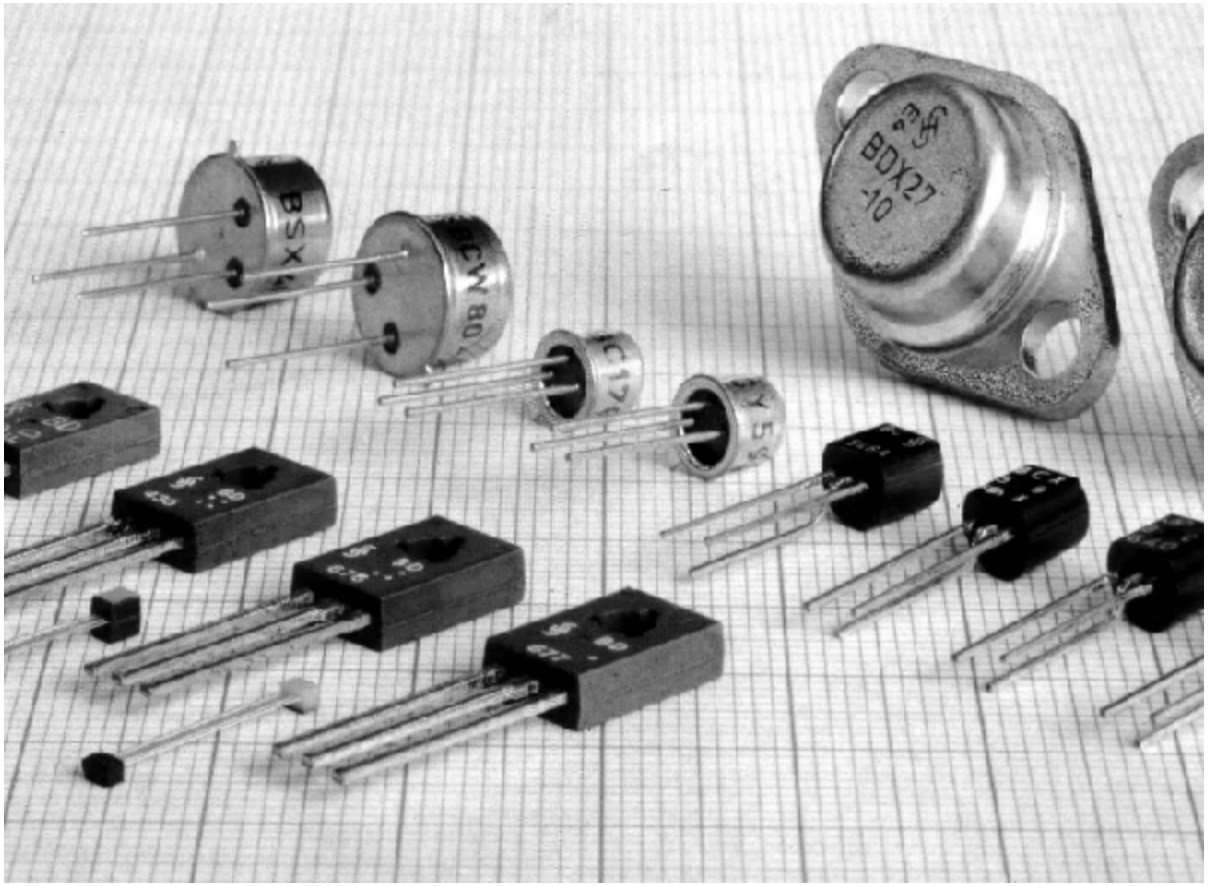
Discrete components: Resistors



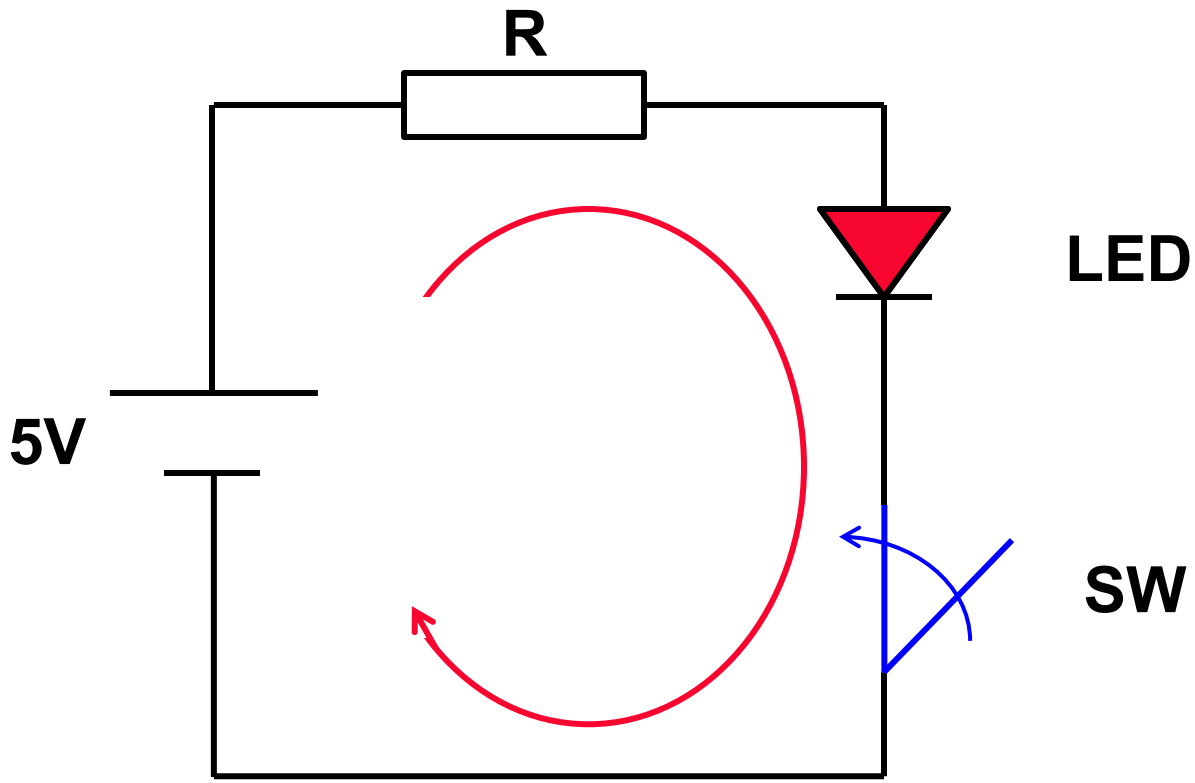


Discrete components: Diodes

Discrete components: transistors



Example of a simple circuit



Technology	State Representing Bit	
	0	1
Pneumatic logic	Fluid at low pressure	Fluid at high pressure
Relay logic	Circuit open	Circuit closed
Complementary metal-oxide semiconductor (CMOS) logic	0–1.5 V	3 .5–5.0 V
Transistor-transistor logic (TTL)	0–0.8 V	2 .0–5.0 V
Dynamic memory	Capacitor discharged	Capacitor charged
Nonvolatile, erasable memory	Electrons trapped	Electrons released
Microprocessor on-chip serial number	Fuse blown	Fuse intact
Polymer memory	Molecule in state A	Molecule in state B
Fiber optics	Light off	Light on
Magnetic disk or tape	Flux direction “north”	Flux direction “south”
Compact disc (CD)	No pit	Pit
Writeable compact disc (CD-R)	Dye in crystalline state	Dye in noncrystalline state

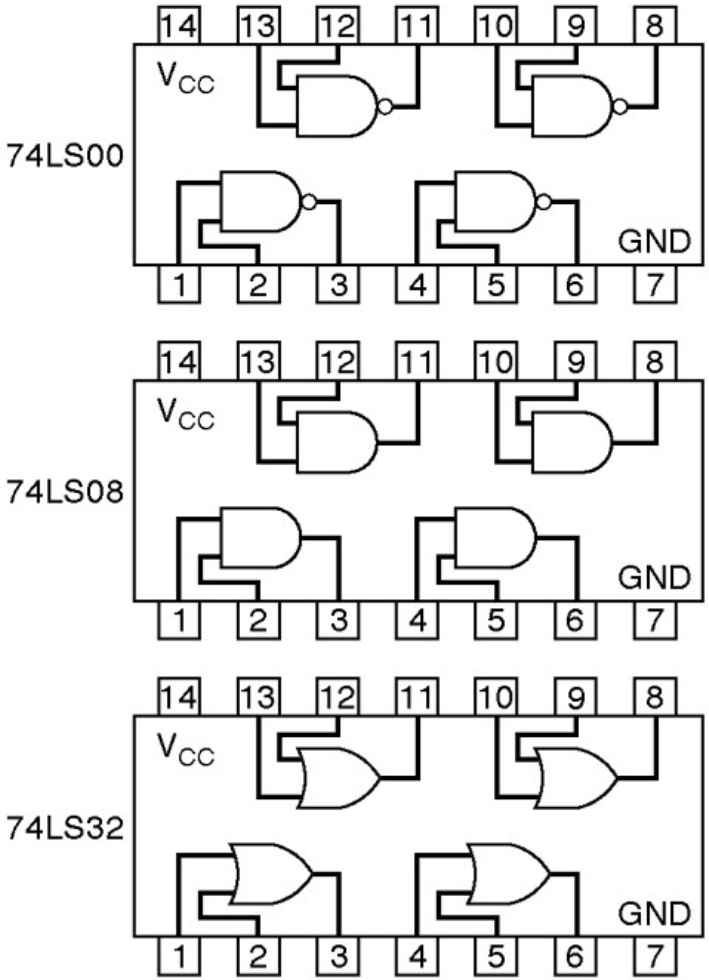
Table 3-1

Physical states representing bits in different logic and memory technologies.

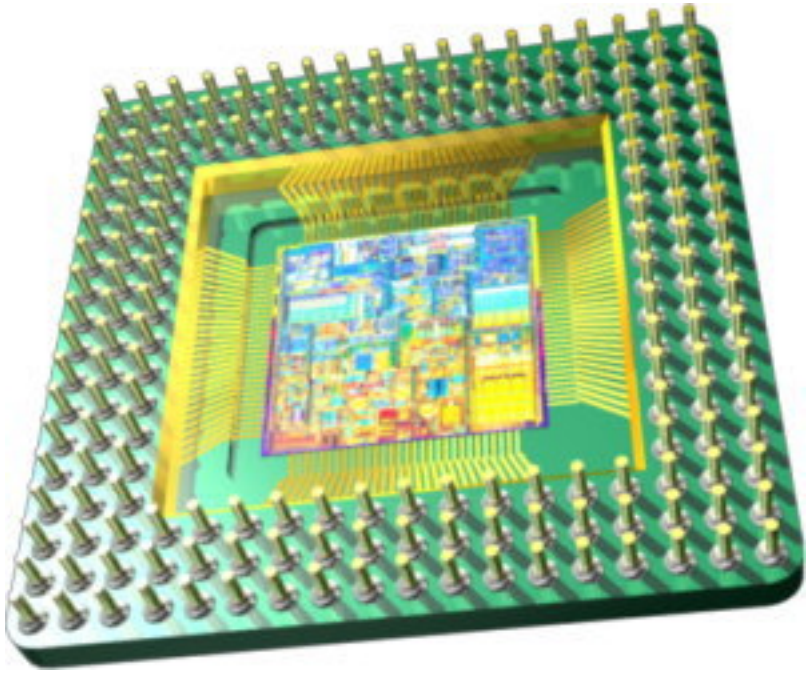
Scale of integration

Complexity	No. of gates
Small-scale (SSI)	< 12
Medium-scale (MSI)	12 - 99
Large-scale (LSI)	100 - 9999
Very large-scale (VLSI)	10,000 – 99,999
Ultra large-scale (ULSI)	100,000 – 999,999
Giga-scale (GSI)	≥ 1,000,000

Examples of SSI logic devices



Example of GSI device:
A microprocessor, MPU, CPU



To make logic outputs switch between High and Low (1 and 0), transistors are used.

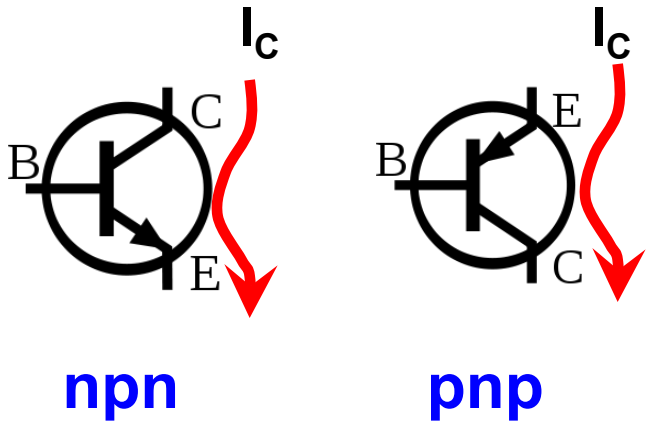
2 broad families:

- **use bipolar junction transistors**
- **e.g. TTL (transistor-transistor logic) circuits**

- **use unipolar field-effect transistors**
- **e.g. CMOS (complementary metal-oxide semiconductor) circuits**

Bipolar junction transistors (BJT)

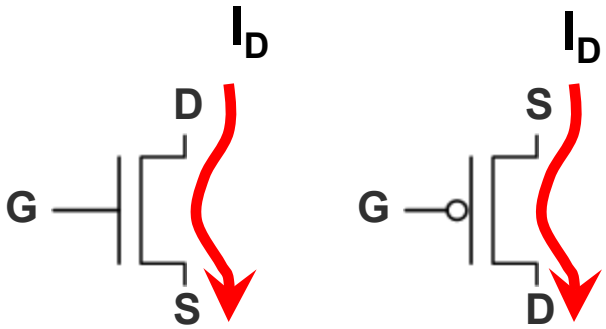
- Base, emitter, collector
- With correct voltage at B, current will flow between C and E



npn pnp

MOS Field-effect transistors (MOSFET)

- Gate, drain, source
- With correct voltage at G, current will flow between S and D



NMOS PMOS

TTL family

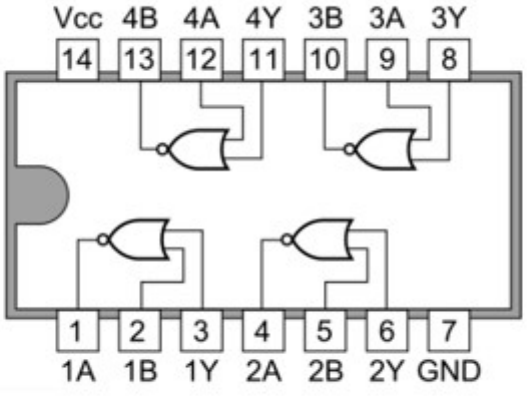
- different prefixes
- different in electrical characteristics such as power dissipation, delay time, switching speed
- do not differ in pin layout or logic function

- examples (hex inverters)

TTL series	Prefix	E.g.
Standard	74	7404
High-speed	74H	74H04
Low-power	74L	74L04
Advanced low-power Schottky	74ALS	74ALS04

CMOS family

- old series not compatible with TTL
- HC series pin-compatible with TTL: share same pin layout



examples (quad 2-input NOR)

CMOS series	Prefix	Example
Old (seldom used)	**40/140**	**4001** **14001**
Metal gate	**74C**	**74C02**
High speed	**74HC**	**74HC02**
Electrically compatible with TTL	**74HCT**	**74HCT02**

Logic-level Voltage Ranges

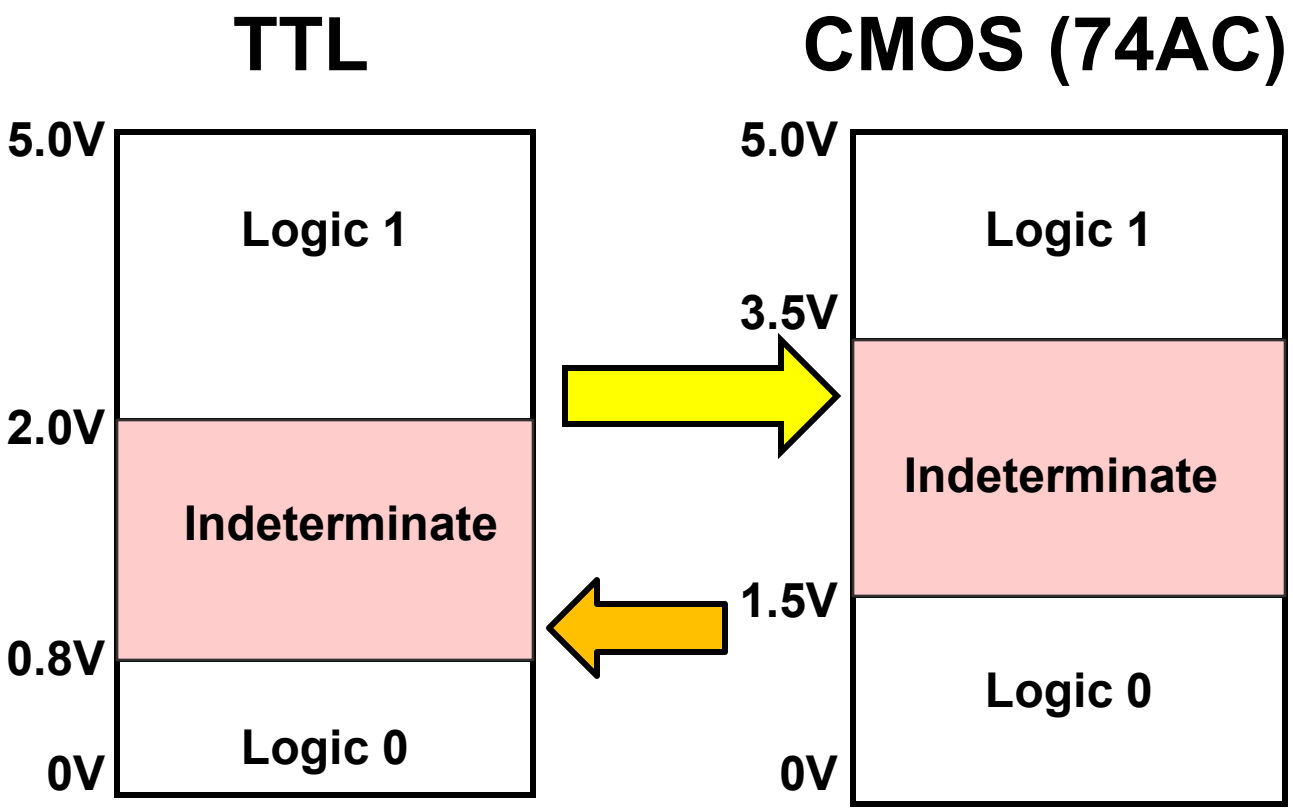
TTL

- **Vcc nominally +5v**

CMOS

- **V_{DD} ranges from +3 to +18v**
- **+5v is most often used when CMOS ICs are used in same circuit with TTL ICs**

Incompatible voltage ranges



Unconnected (floating) inputs

TTL

- **floating input acts like logic 1**
- **measures dc level between 1.4 to 1.8 volts**
- **not recommended due to noise pick-up**

CMOS

- **disastrous result**
- **IC may become overheated**
- **all unused input pins must be connected to V_{DD}, GND, or another input**

Active levels

- Recall 5.16: ODD and EVEN* example

A signal is said to be **active high** if	it produces the named effect or result when it is logic 1 **TRUE (asserted) when it is 1**
A signal is said to be **active low** if	it produces the named effect or result when it is logic 0 **TRUE (asserted) when it is 0**

Most signals that we encounter are active high

Active levels (examples)

Signal name	Effect/result when signal=0	Effect/result when signal=1	Active high/low
Subtract	Add Y to X	**Subtract** Y from X	Active high
Add*	**Add** Y to X	Subtract Y from X	Active low
Unmute	Mute a speaker	**Unmute** a speaker	Active high
Unmute*	**Unmute** a speaker	Mute a speaker	Active low
Read	Write data	**Read** data	Active high
Write*	**Write** data	Read data	Active low

Active high or active low depends on the signal name and effect/result

Active Low	*Active High*
READY–	READY+
ERROR.L	ERROR.H
ADDR15(L)	ADDR15(H)
RESET*	RESET
ENABLE~	ENABLE
~GO	GO
/RECEIVE	RECEIVE
TRANSMIT_L	TRANSMIT

RESET*

RESET

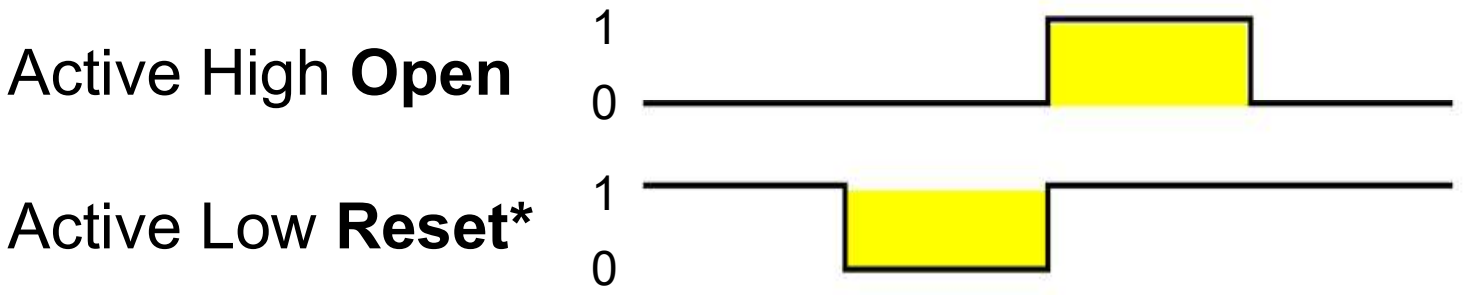
Each row shows a different naming convention for active levels.

Active low signals, being less common, are usually highlighted to draw our attention.

Asserted and negated

Asserted: when an active high signal is =1; or
when an active low signal is =0;
Negated: otherwise

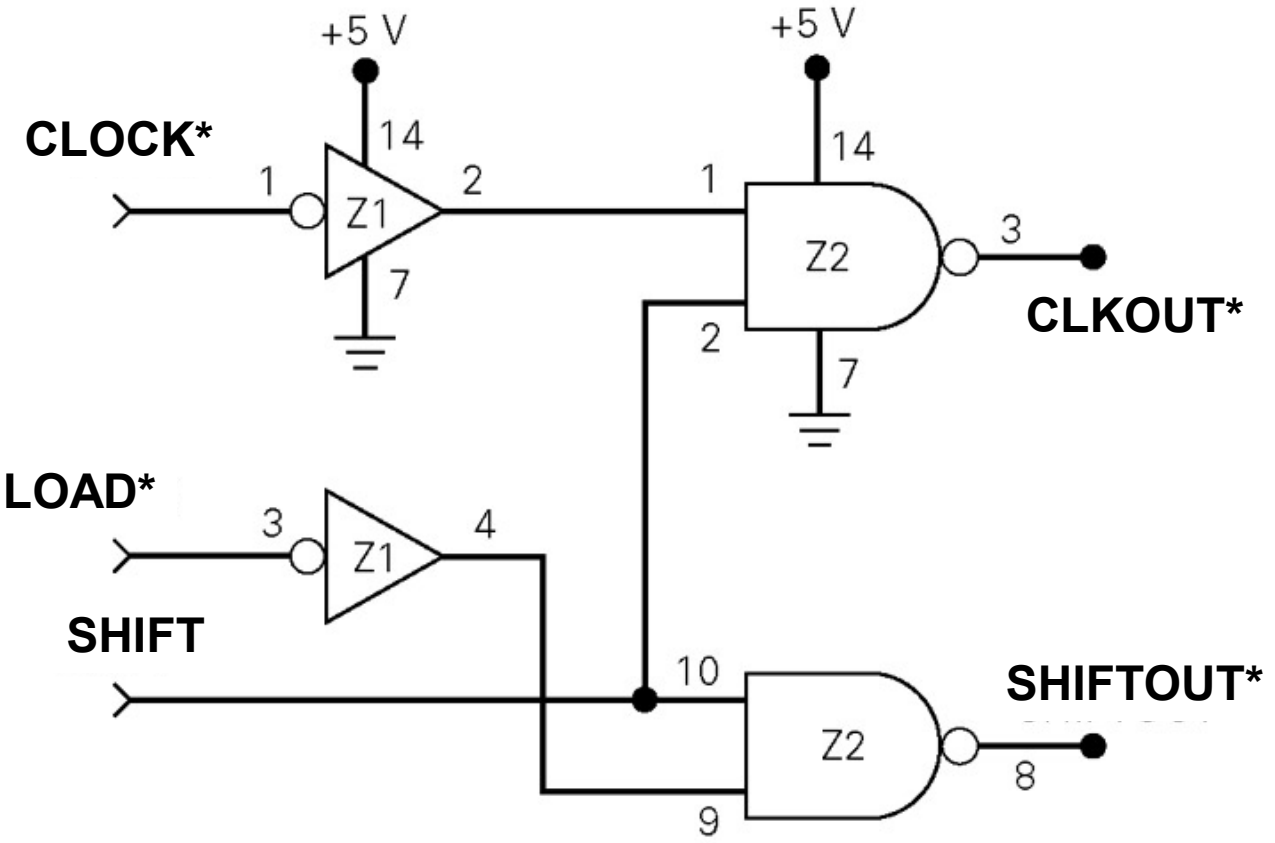
Example: the timing diagram below shows that the signals are **asserted** for a while and negated (or de-asserted) for the rest of the time



Logic circuit connection diagrams

Fig. 4-32 contains more information than the usual circuit diagram to facilitate circuit connection and troubleshooting

- **pin numbers, IC numbers, component values, signal names and power supply voltages are clearly indicated**
- **conform to bubble-to-bubble design rules**
- **active levels are clearly indicated**



IC	Type
Z1	74HC04 hex inverter
Z2	74HC00 quad nand

Fig. 4-32 Typical logic-circuit connection diagram

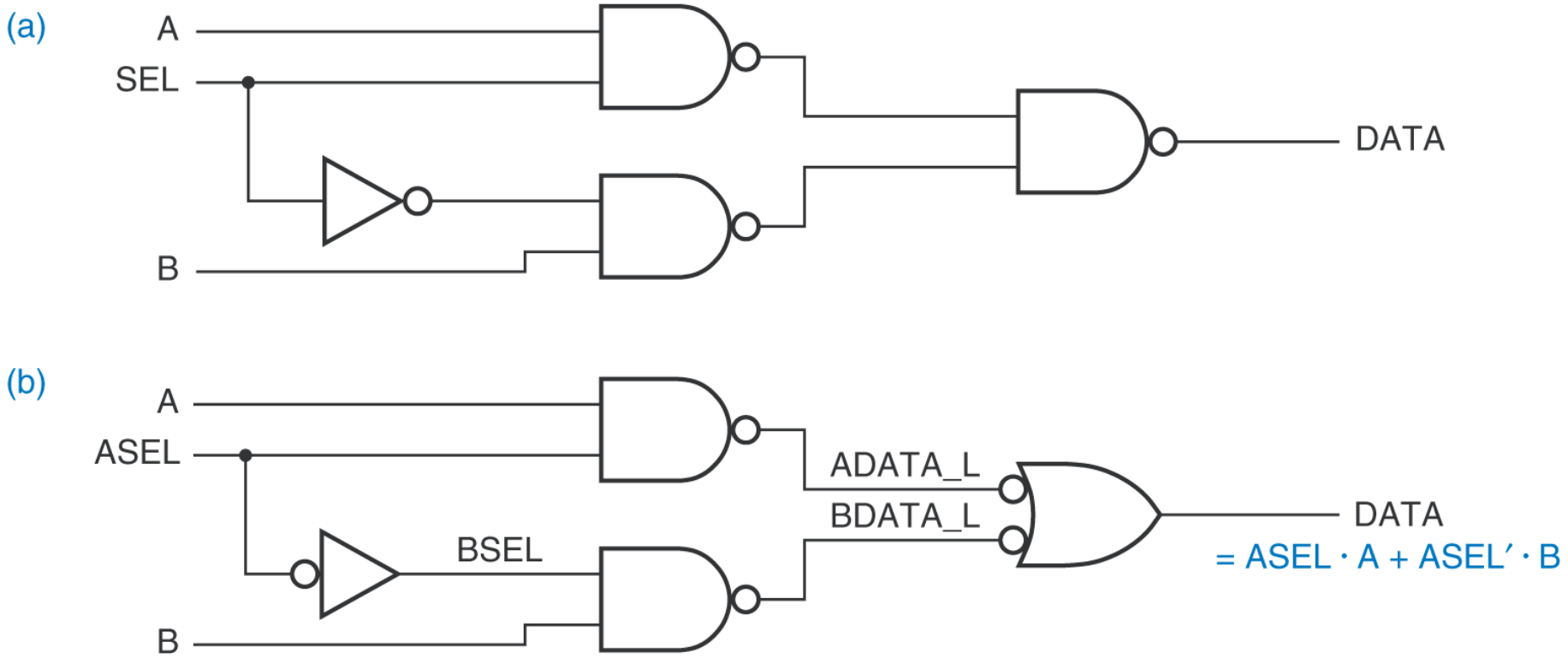


Figure 6-11

A 2-input multiplexer (you're not expected to know what that is yet): (a) cryptic logic diagram; (b) proper logic diagram using active-level designators and alternate logic symbols.

Fig. 6-11 Bubble-to-bubble logic diagram (Wakerly, 4th ed)

Troubleshooting Digital Systems

Read supplementary lab manual

- **Fault detection**
- **Fault isolation**
- **Fault correction**

Internal IC faults

- **malfunction in internal circuitry**
- **short circuit**
- **open circuit**
- **short between two pins**

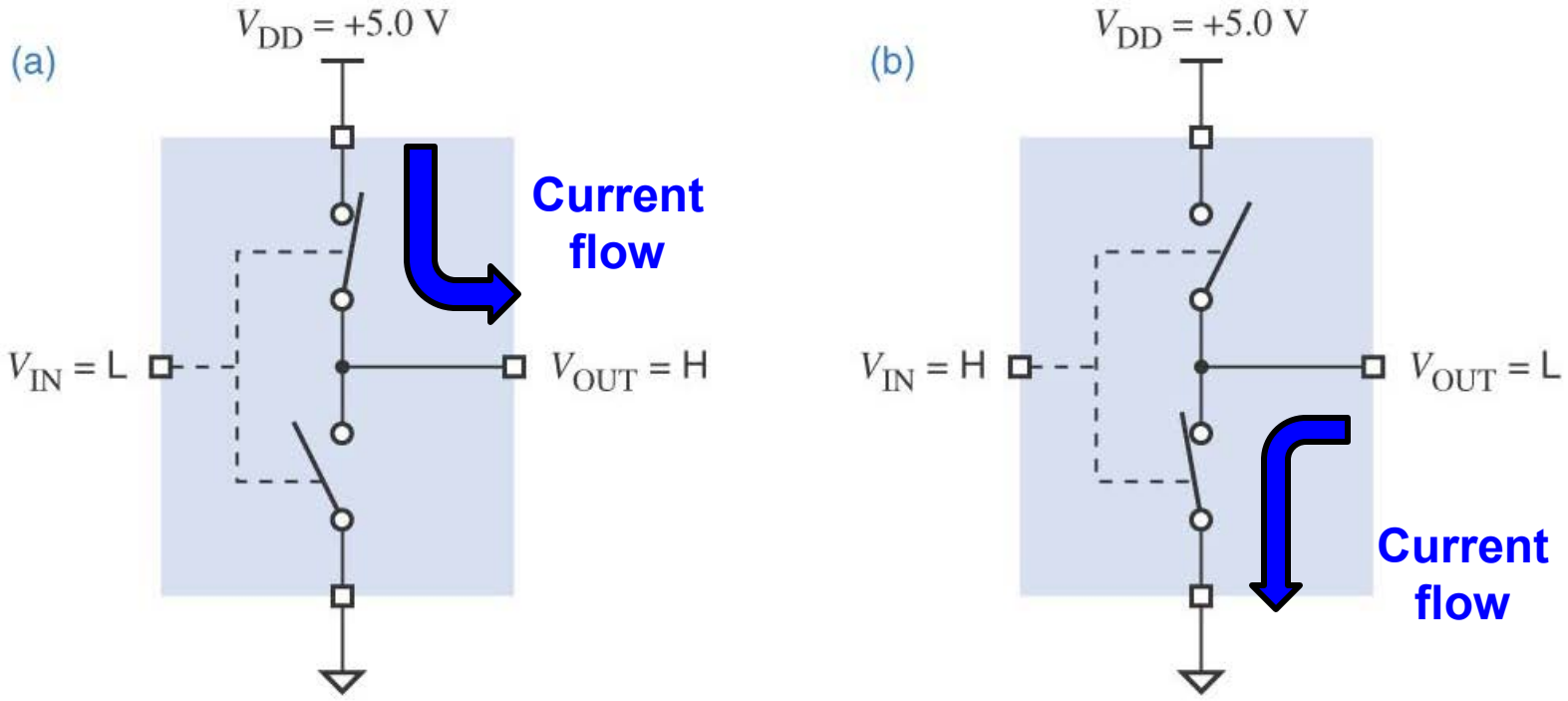
External IC faults

- open signal line
- shorted signal lines
- faulty power supply
- wrong connection

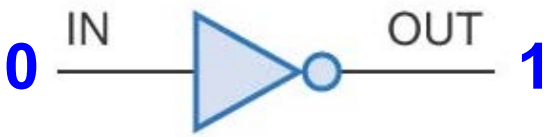
NEVER tie any circuit output to:

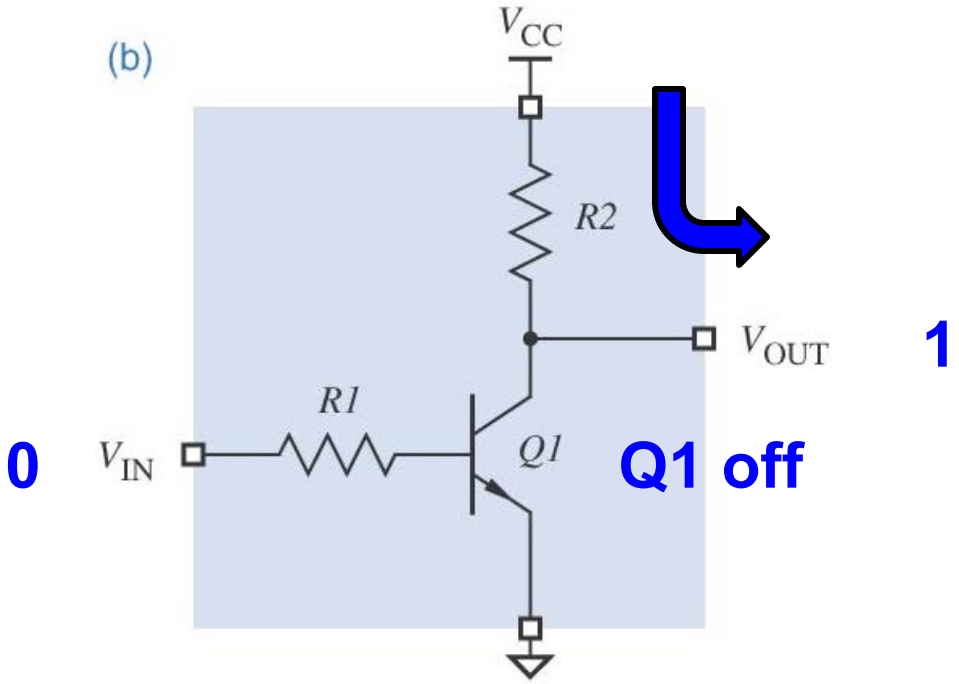
- another output unless you are very sure
- Vcc , GND or any other fixed voltage level

The transistor as a Switch

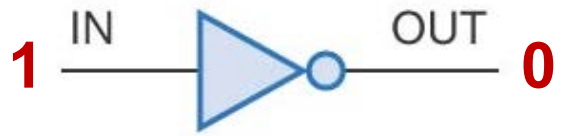


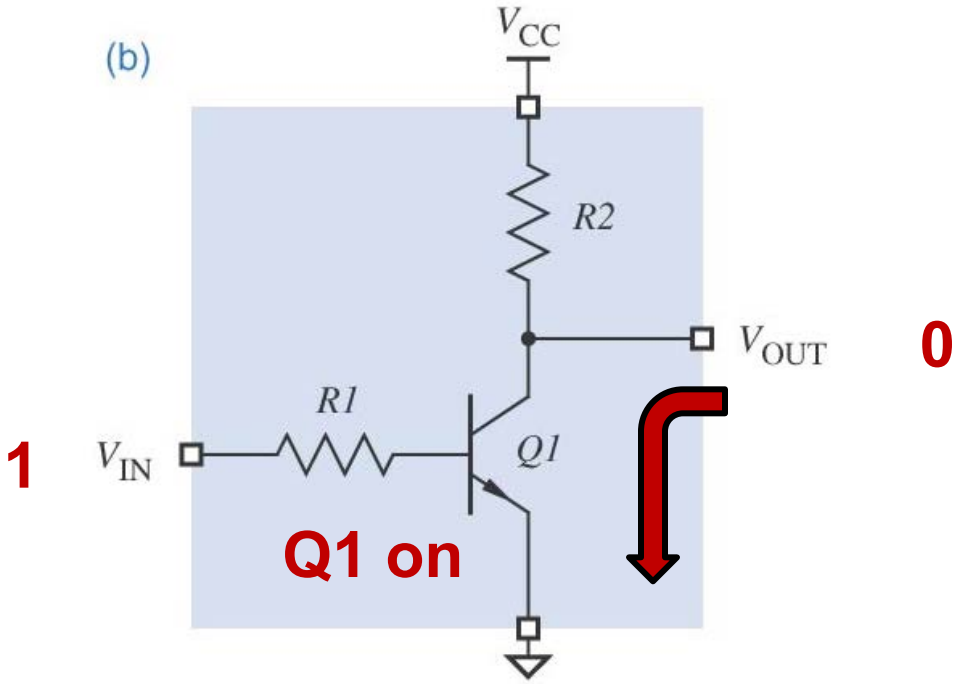
A simple BJT logic inverter



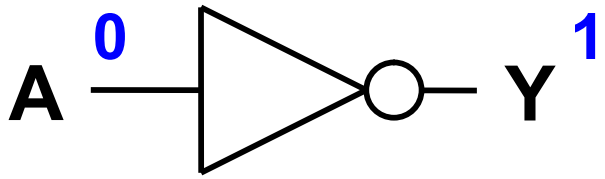


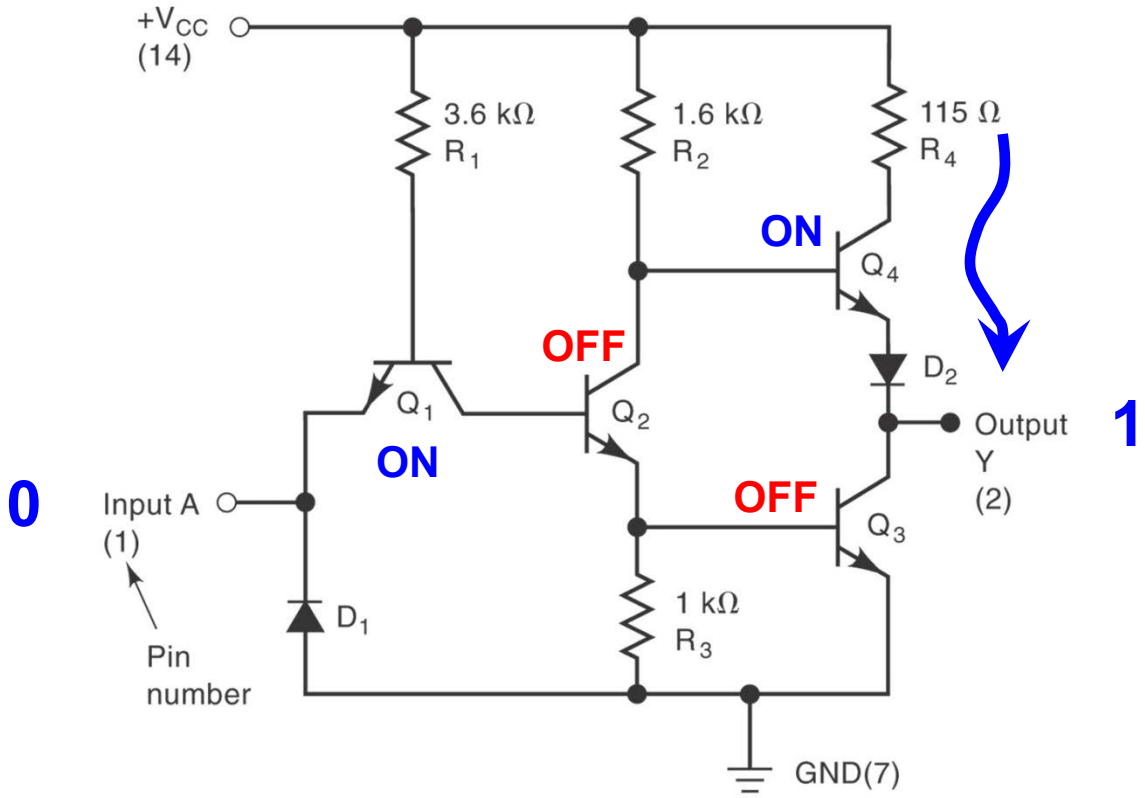
A simple BJT logic inverter



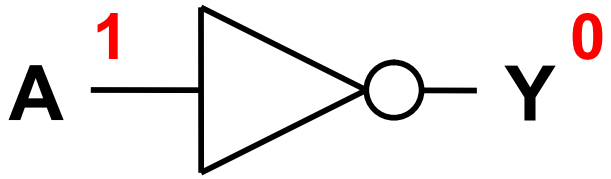


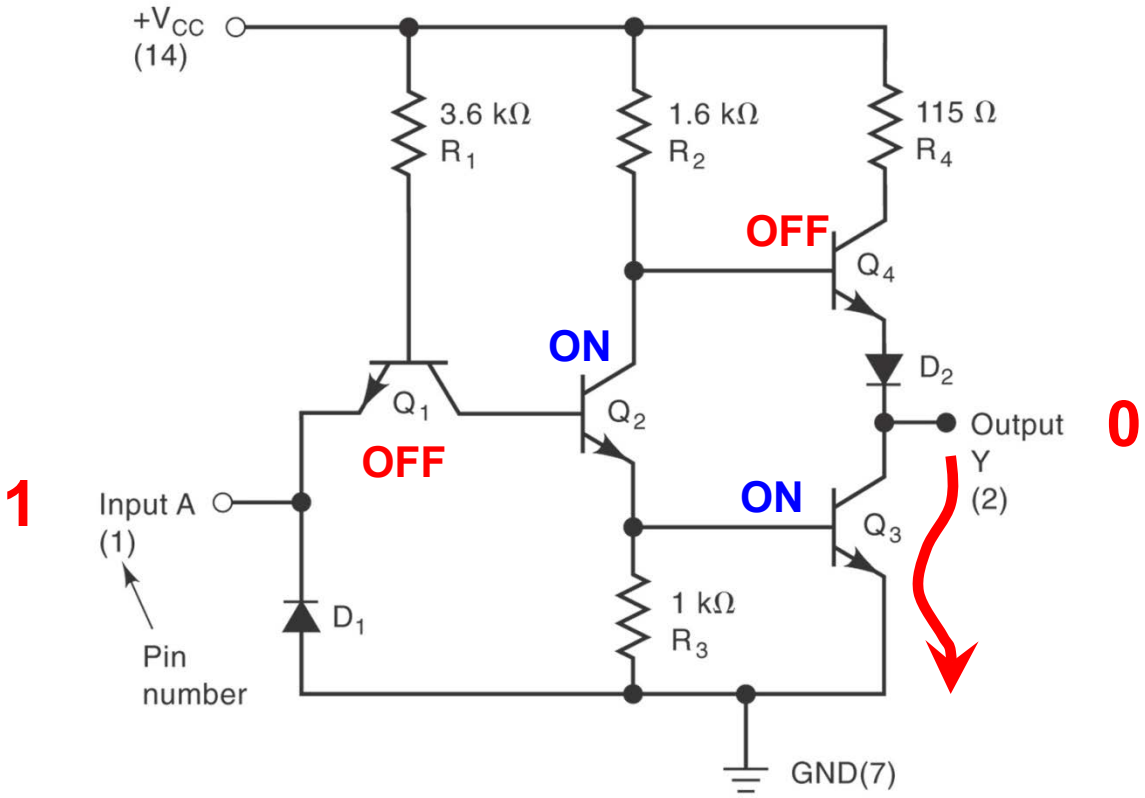
TTL inverter



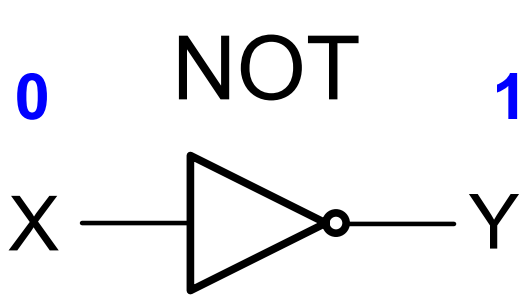


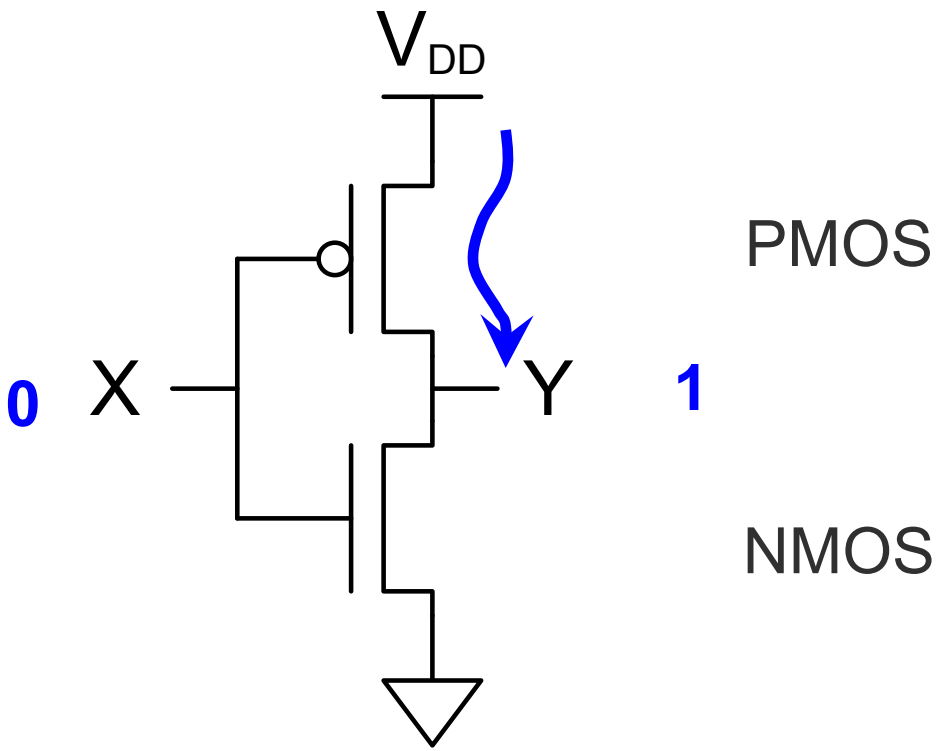
TTL inverter



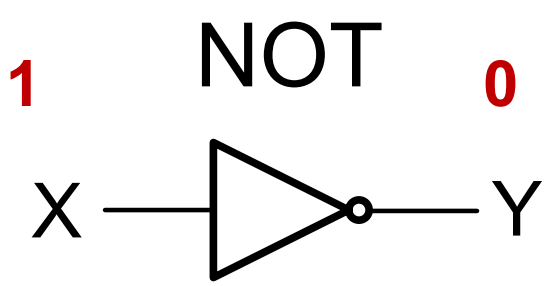


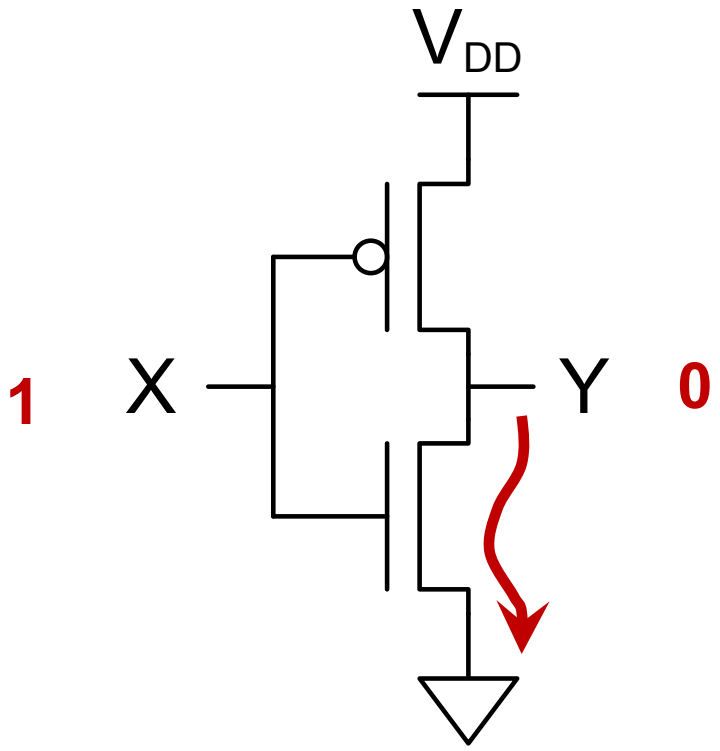
CMOS inverter



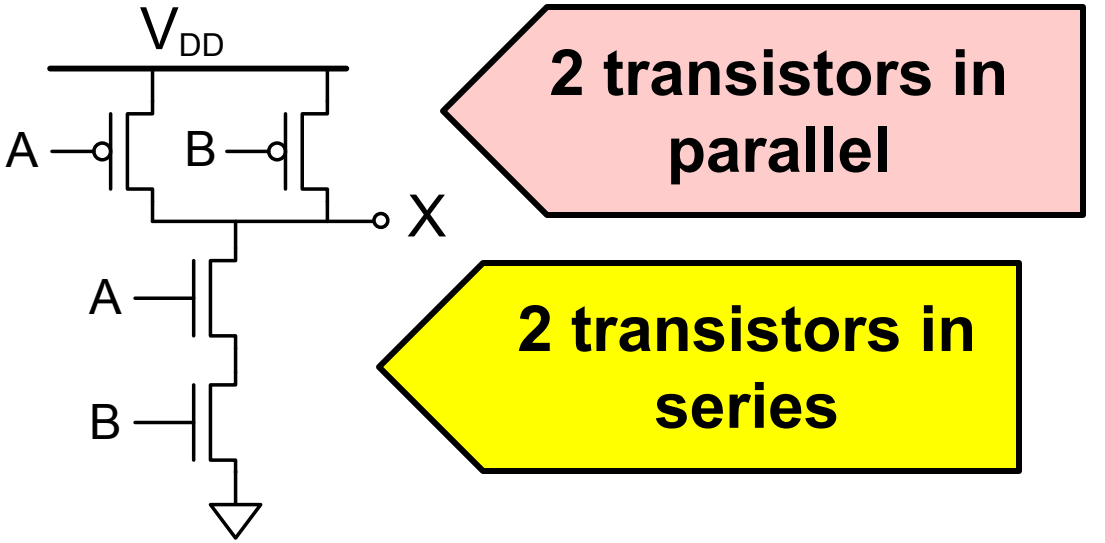


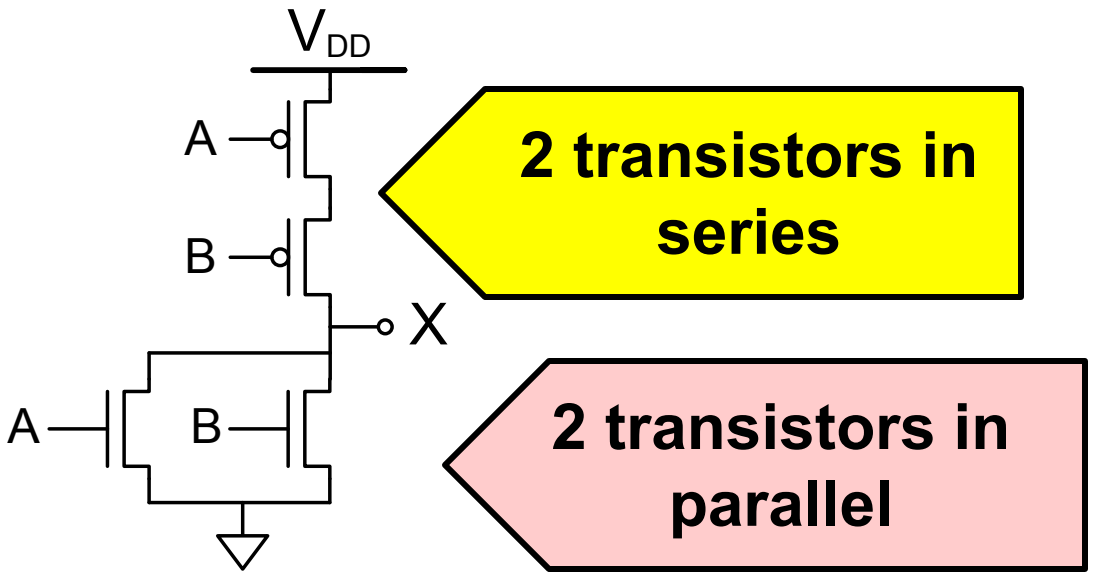
CMOS inverter

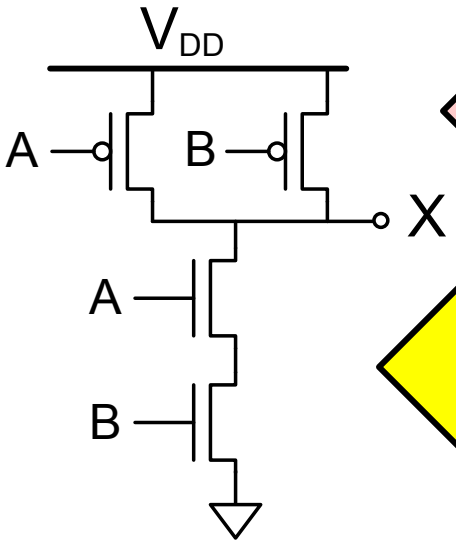




Examples of CMOS logic circuits

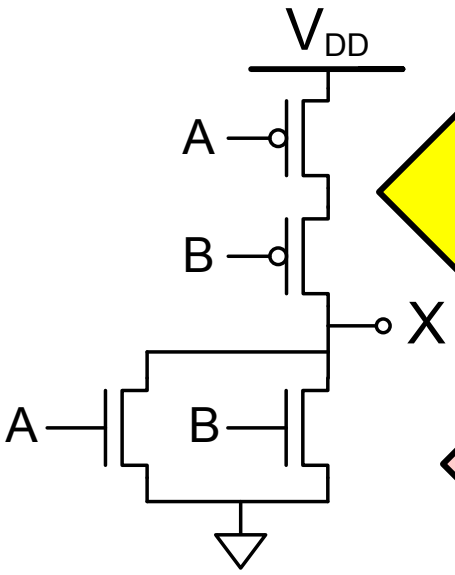

V_{DD}
A
B
X
A
B
2 transistors in parallel
2 transistors in series


V_{DD}
A
B
X
A
B
2 transistors in series
2 transistors in parallel



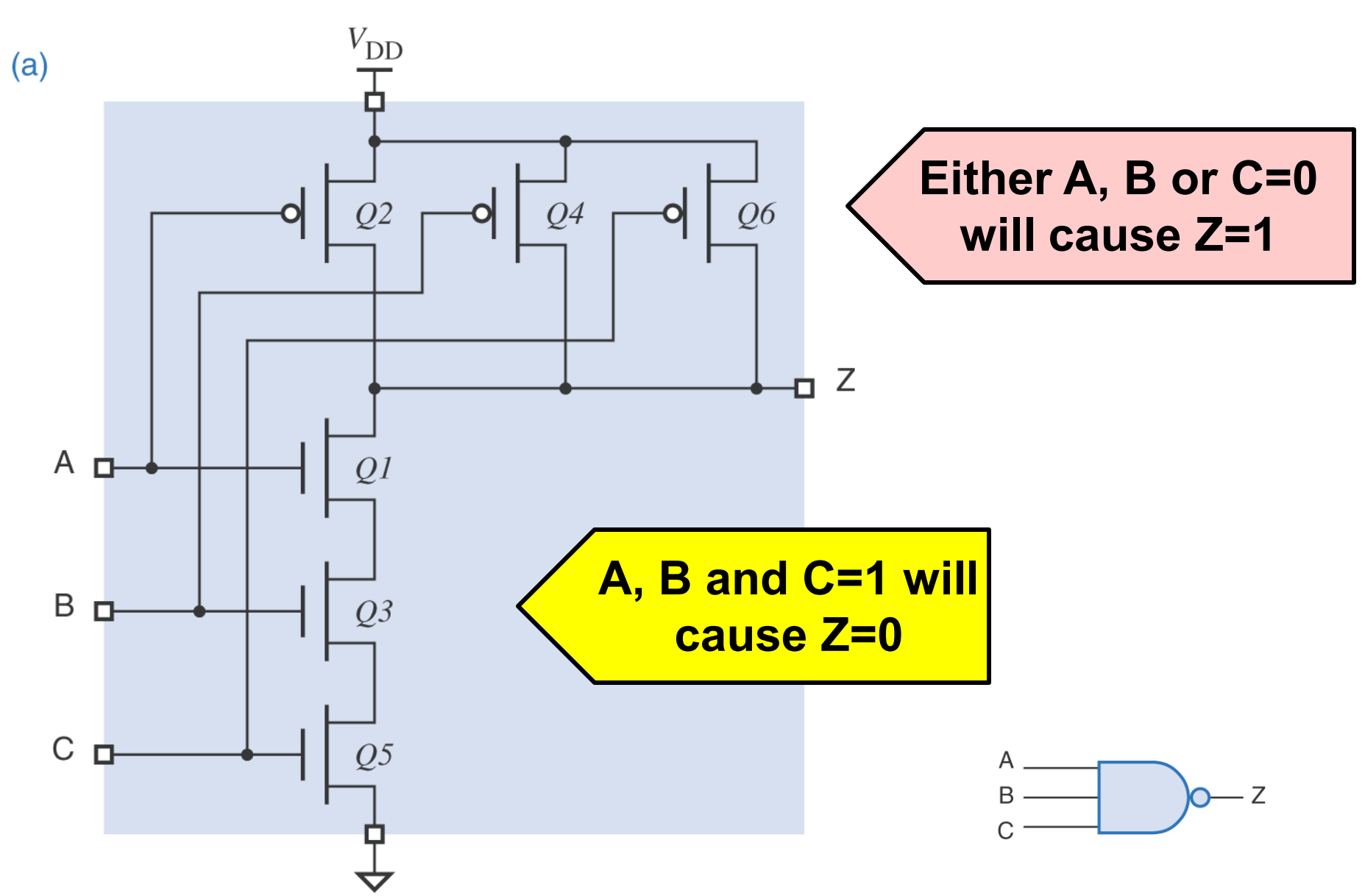
Either A or B=0
will cause X=1

Both A and B=1
will cause X=0



Both A and B=0
will cause X=1

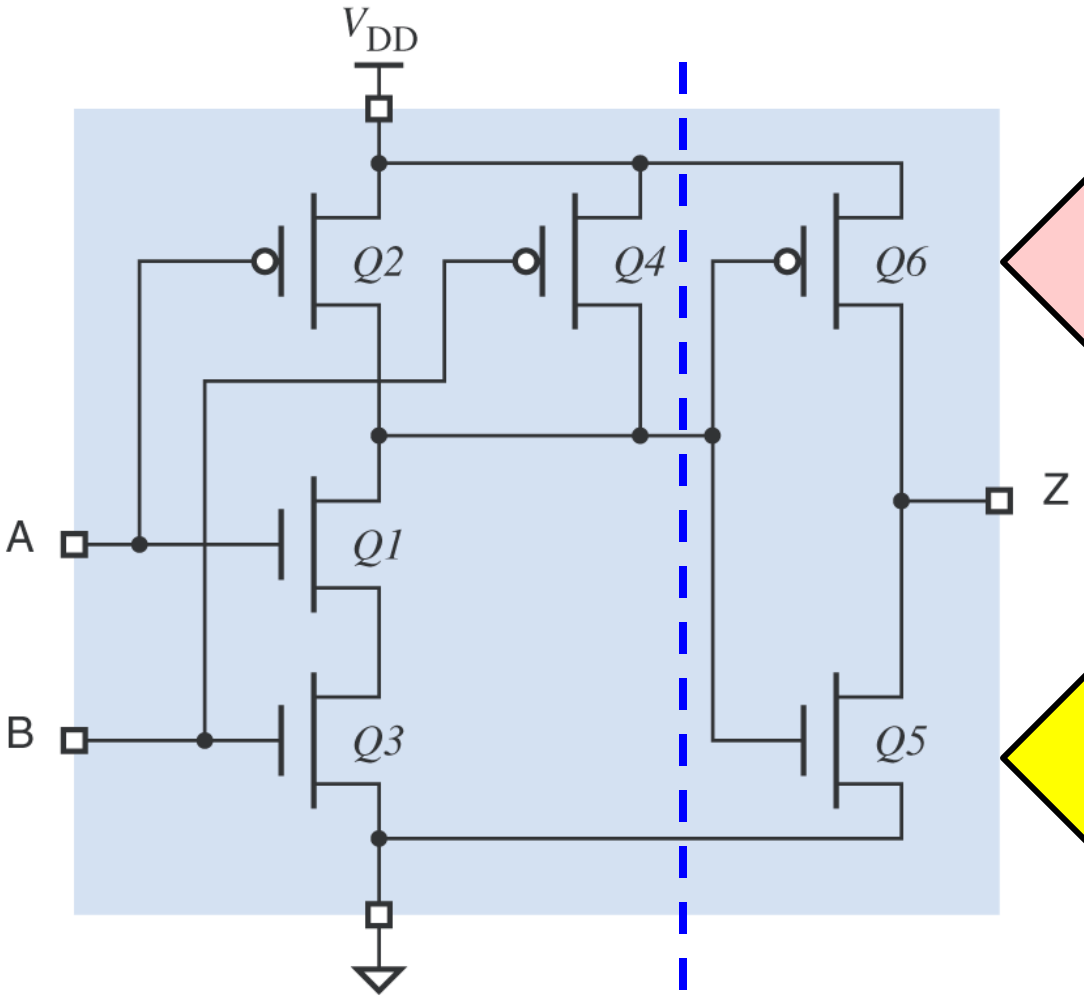
Either A or B=1
will cause X=0



Either A, B or C=0 will cause Z=1

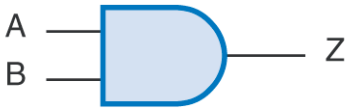
A, B and C=1 will cause Z=0

(a)



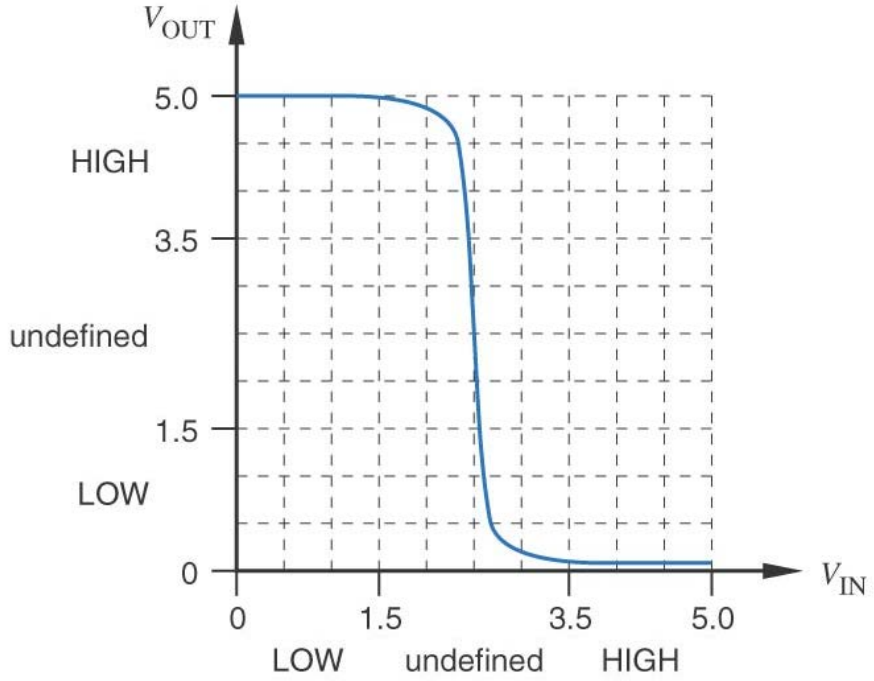
Either A or B=0 will cause Z=0

Both A and B=1 will cause Z=1



NAND NOT

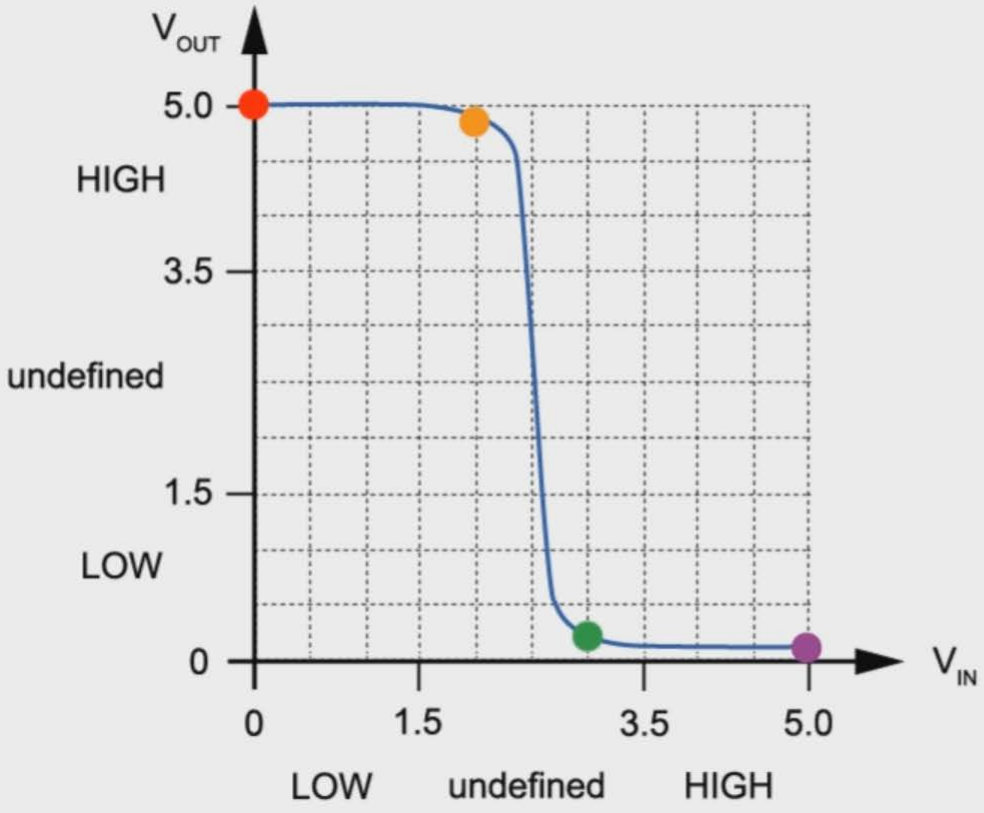
Digital Circuits Characteristics



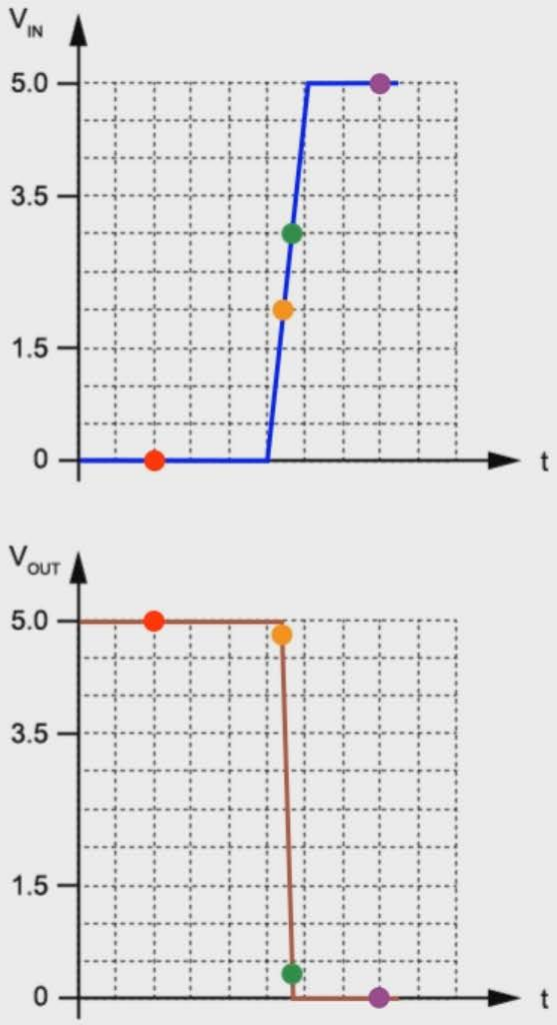
Not guaranteed

Fig. 3-25 Typical input-output transfer characteristic of a CMOS inverter

transfer characteristic:



time-based signals:



Voltage parameters:

V_{OH} (min) - Minimum output voltage produced for logic 1

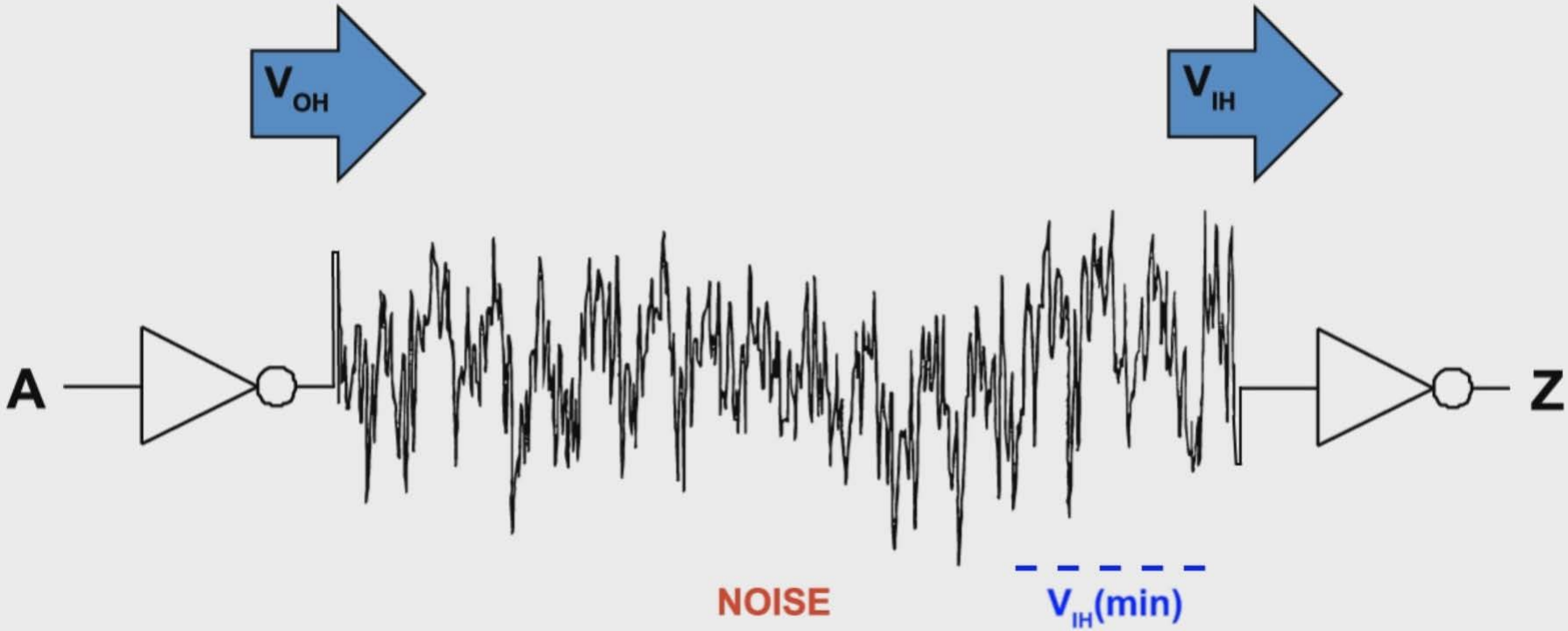
V_{IH} (min) - Minimum input voltage to be recognised as logic 1

V_{IL} (max) - Maximum input voltage to be recognised as logic 0

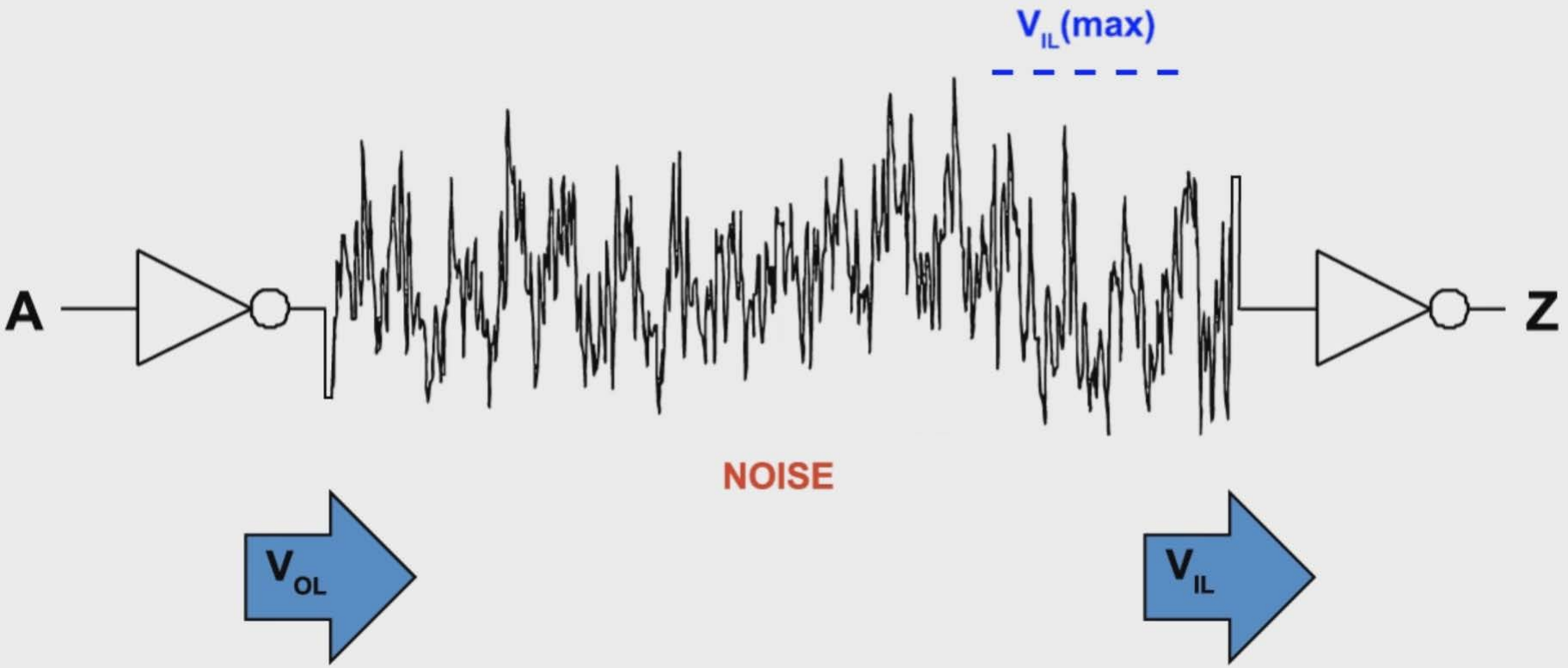
V_{OL} (max) – Maximum output voltage produced for logic 0

Voltage parameters and noise margin:

High-state DC noise margin = $V_{OH}(min) - V_{IH}(min)$

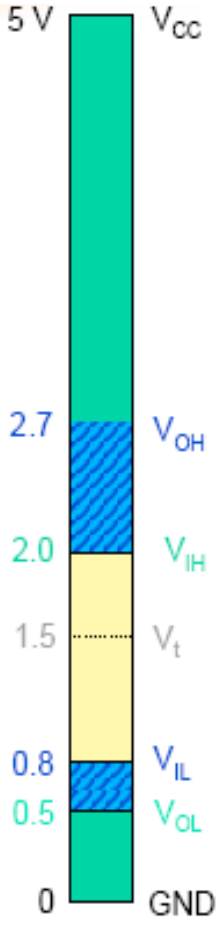


Voltage parameters and noise margin:

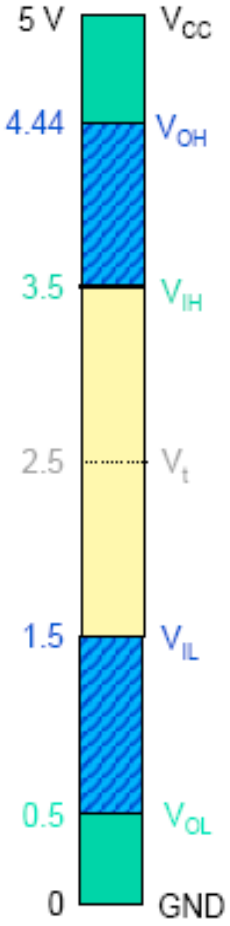


Low-state DC noise margin = V_{IL}(max) – V_{OL}(max)

Some typical values

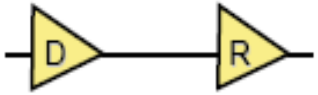


5-V LSTTL



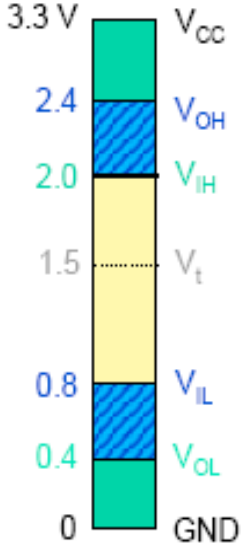
5-V CMOS

Is V_{OH} higher than V_{IH}?
Is V_{OL} less than V_{IL}?

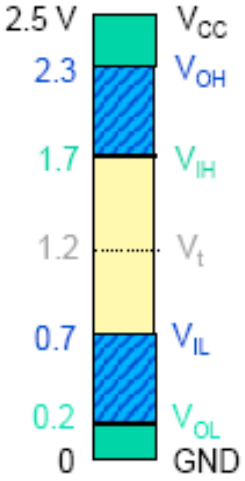


D \ R	5TTL	5CMOS	3LVTTL	2.5CMOS	1.8CMOS
5TTL	Yes	No	Yes *	Yes*	Yes*
5 CMOS	Yes	Yes	Yes*	Yes*	Yes*
3 LVTTL	Yes	No	Yes	Yes*	Yes*
2.5 CMOS	Yes	No	Yes	Yes	Yes*
1.8 CMOS	No	No	No	No	Yes

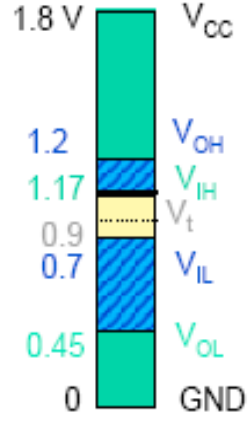
* Requires V_{IH} Tolerance



3.3-V LVTTL



2.5-V CMOS



1.8-V CMOS

Current parameters

I_{IH} – Maximum current that flows into the input at logic 1

I_{IL} - Maximum current that flows into the input at logic 0

I_{OH} – Maximum current that flows from the output at logic 1

I_{OL} – Maximum current that flows from the output at logic 0

Very small leakage current in CMOS (1μA)

0.02 - 24 mA depends on family

Other characteristics

Fan-out

- **specifies the number of standard loads that the output gate can drive**
- **More loads may reduce DC noise margins and switching speed**

Speed

- **Time taken for output to switch between 0 and 1**

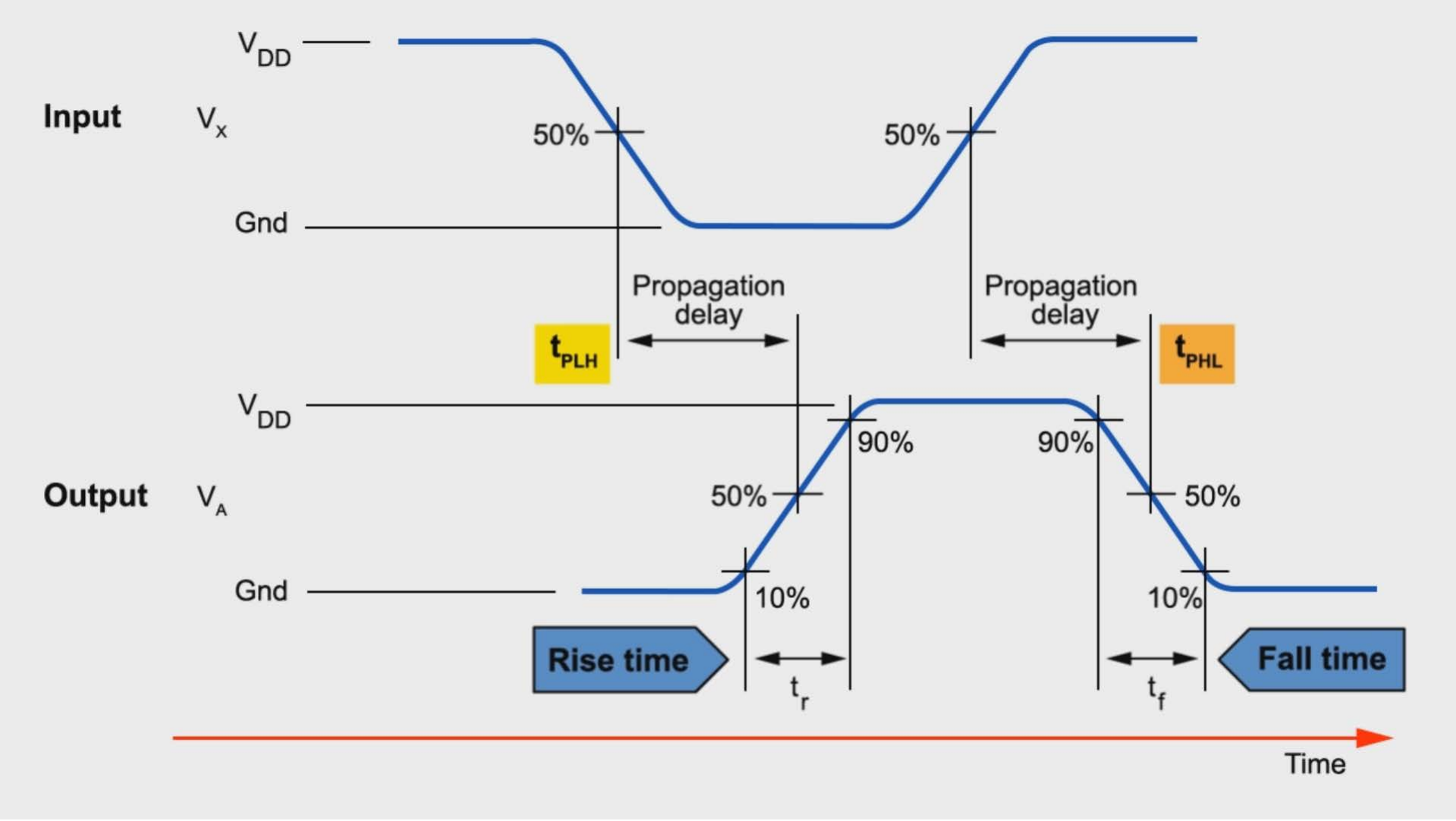
Power dissipation

- power consumed by the gate or device
- For CMOS, most of the power is consumed when output switches between 0 and 1 (dynamic power dissipation)
- $P = C V^2 f$
- Proportional to switching frequency f and square of power supply voltage V
- Static power dissipation (when there is no switching) is usually very small

Propagation delay

- average transition delay time for signal to propagate from input to output
- e.g. 9 – 19 ns for 74HC00
- t_{PD} , or t_{PHL} & t_{PLH}
- t_{PHL}= delay when output changes from High to Low
- t_{PLH}= delay when output changes from Low to High

Propagation delay (inverter):



Tristate outputs

3 output states:

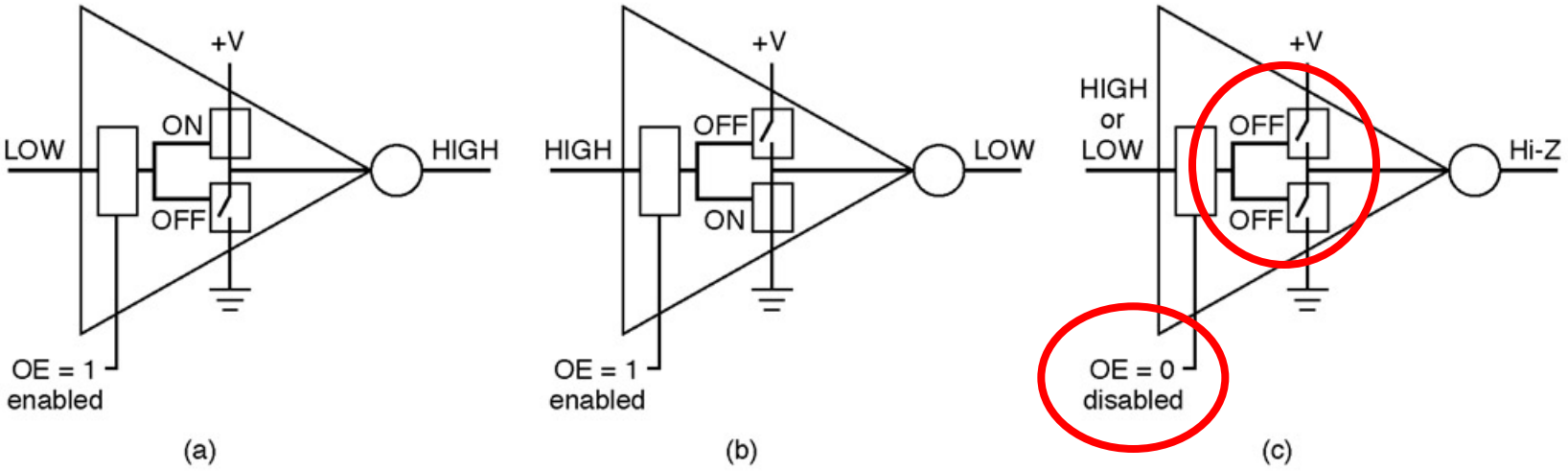
- logic 0
- logic 1
- high impedance (Hi-Z)
  - neither 0 nor 1
  - behaves like an open circuit

When a device is enabled, output is logic 0 or 1

When device is disabled, output is in Hi-Z

E.g. tristate buffer, tristate inverter

Tristate inverter

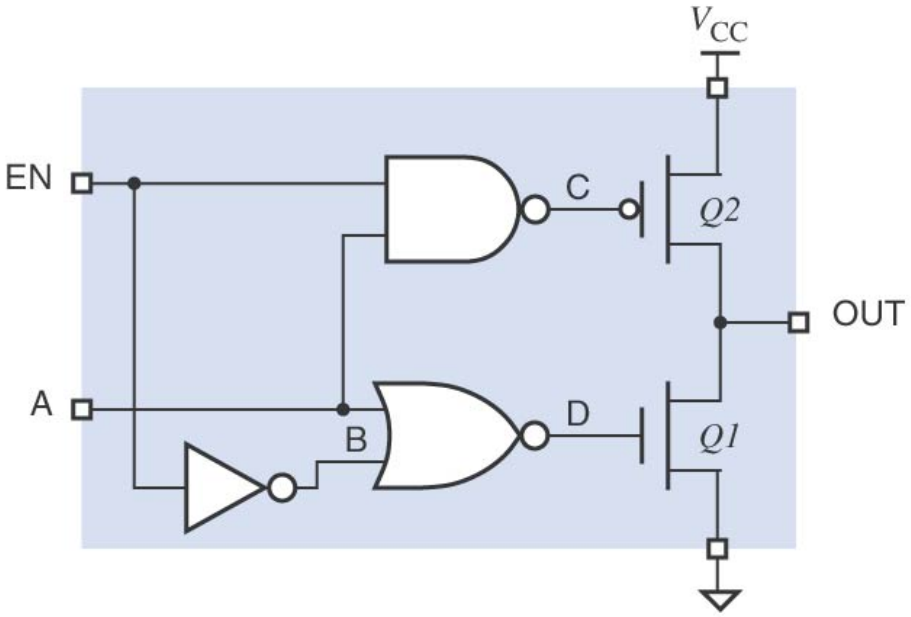


(a) & (b): Tristate device behaves as a normal inverter when enabled.

(c): Device output is in high-impedance when disabled.

CMOS Tristate buffer

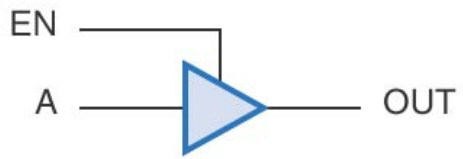
(a)



(b)

EN	A	B	C	D	Q1	Q2	OUT
L	L	H	H	L	off	off	Hi-Z
L	H	H	H	L	off	off	Hi-Z
H	L	L	H	H	on	off	L
H	H	L	L	L	off	on	H

(c)



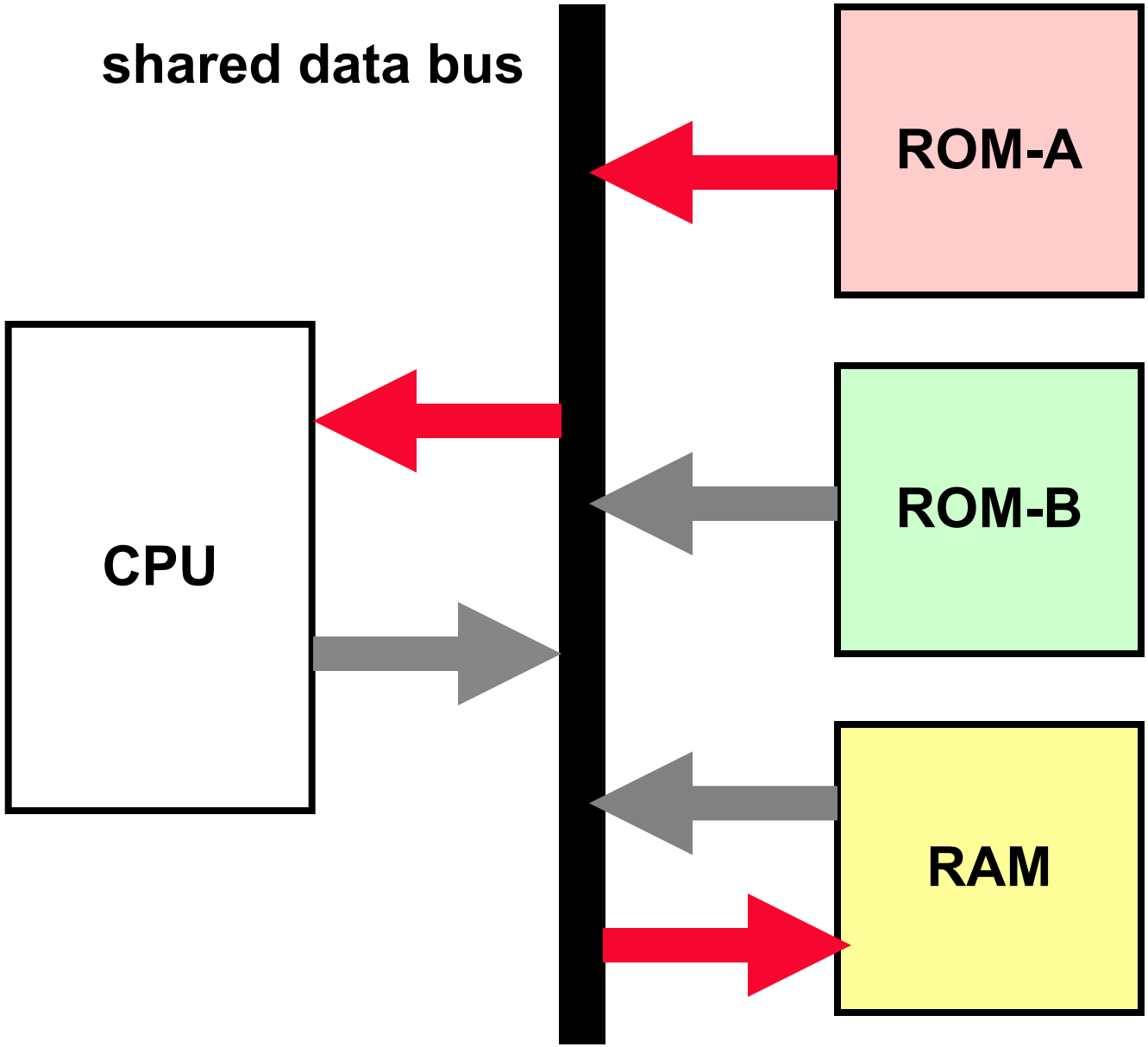
Advantage of using logic devices with tristate outputs

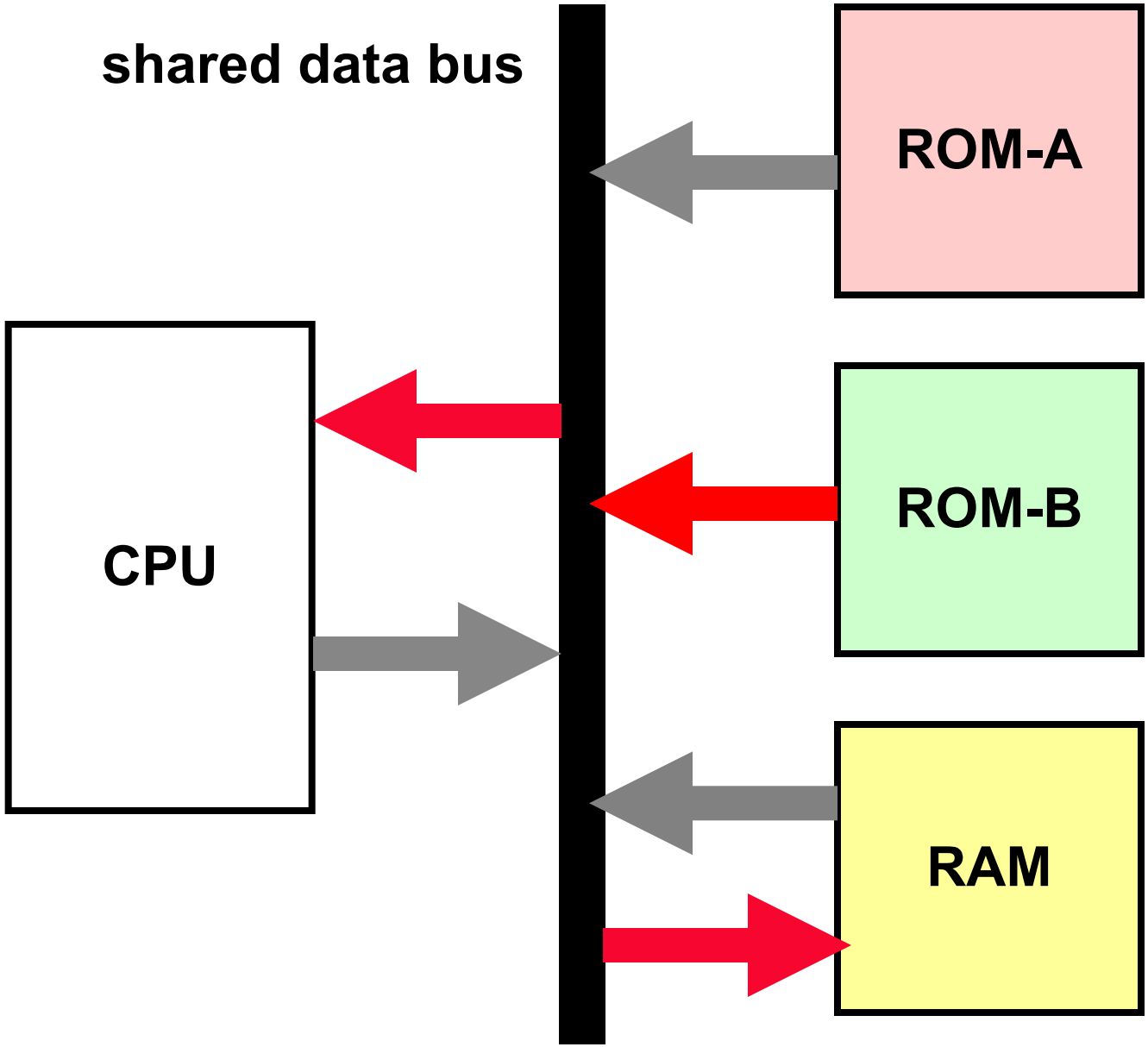
Two or more outputs can be connected together.

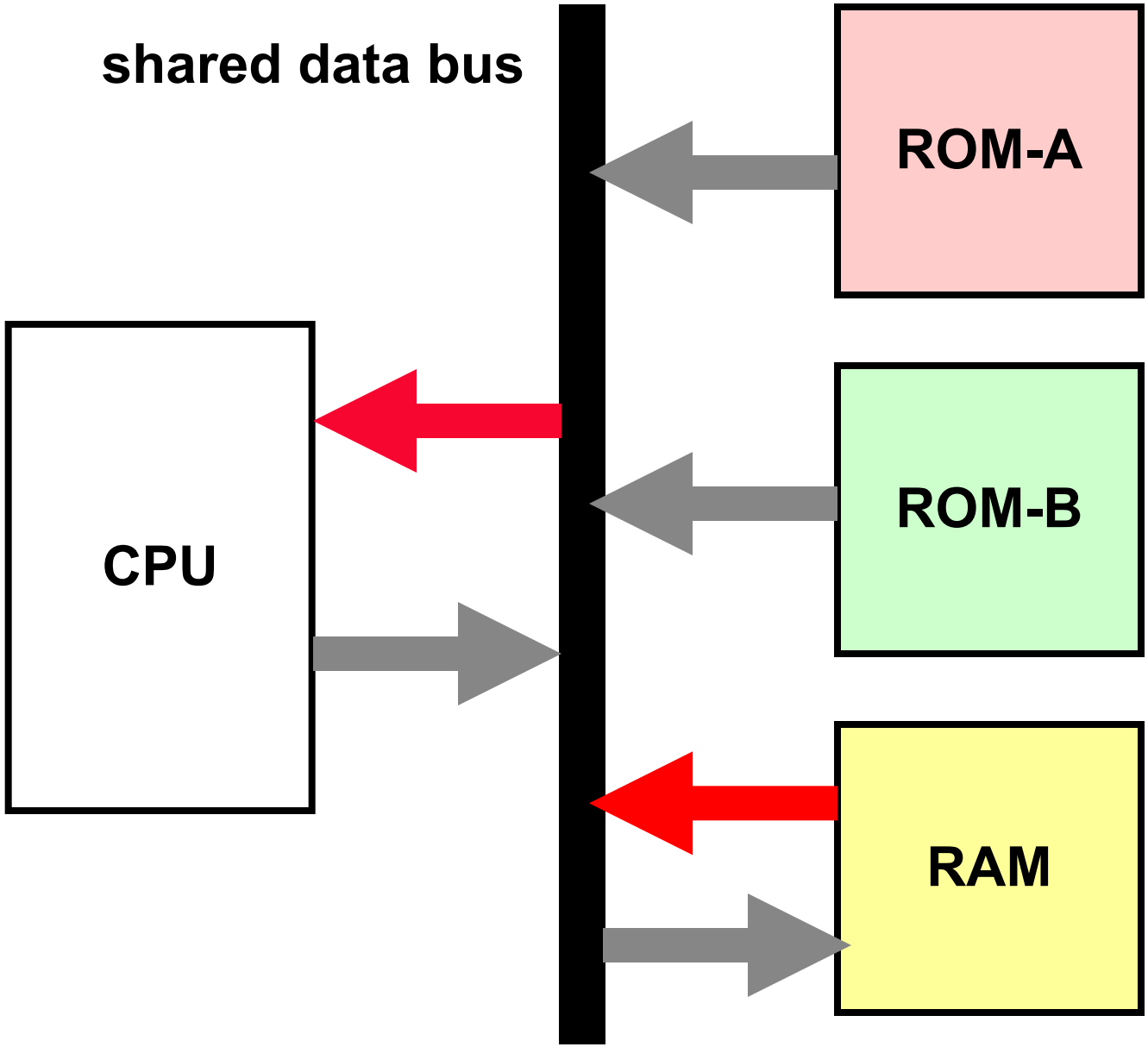
However, at any one time only one (or no) output should be enabled.

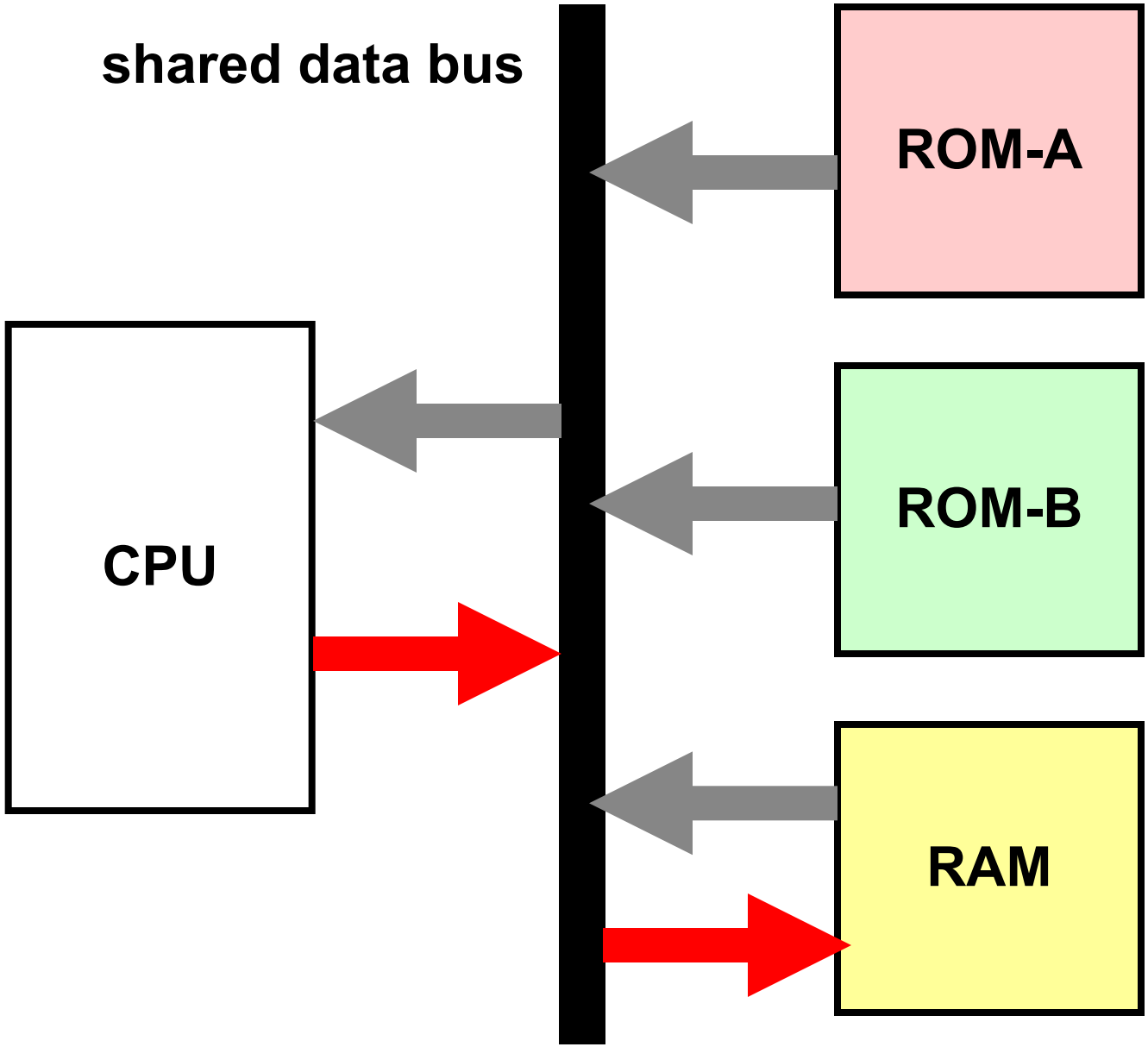
Otherwise, it can lead to bus contention and damage the devices.

Example: memory devices have tristate outputs to share the same data bus.


shared data bus
ROM-A
CPU
ROM-B
RAM

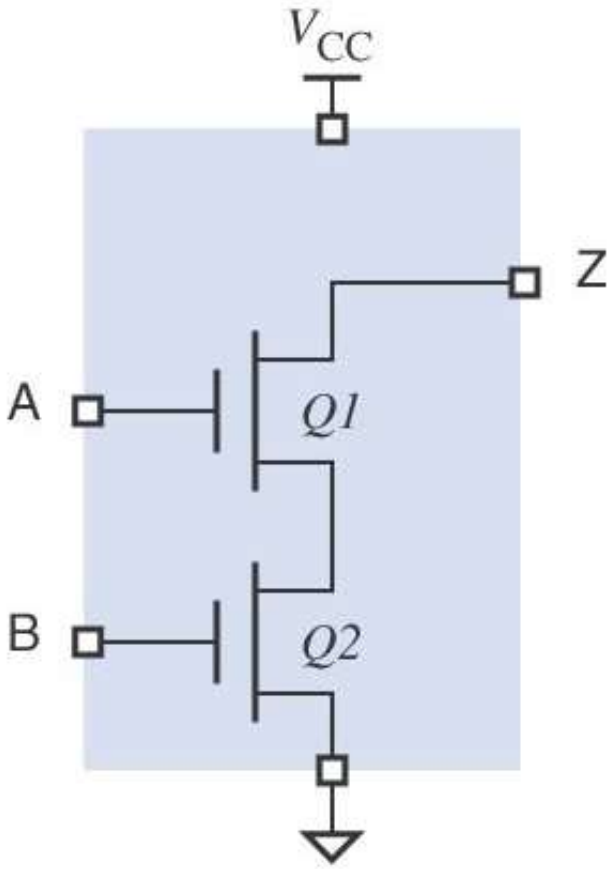

shared data bus
ROM-A
CPU
ROM-B
RAM


shared data bus
ROM-A
CPU
ROM-B
RAM


shared data bus
ROM-A
CPU
ROM-B
RAM

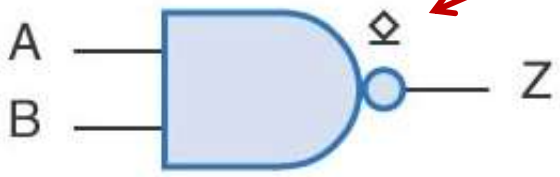
Open-collector/drain output

Need external pull-up resistor to make output=1



A	B	Q1	Q2	Z
L	L	off	off	open
L	H	off	on	open
H	L	on	off	open
H	H	on	on	L

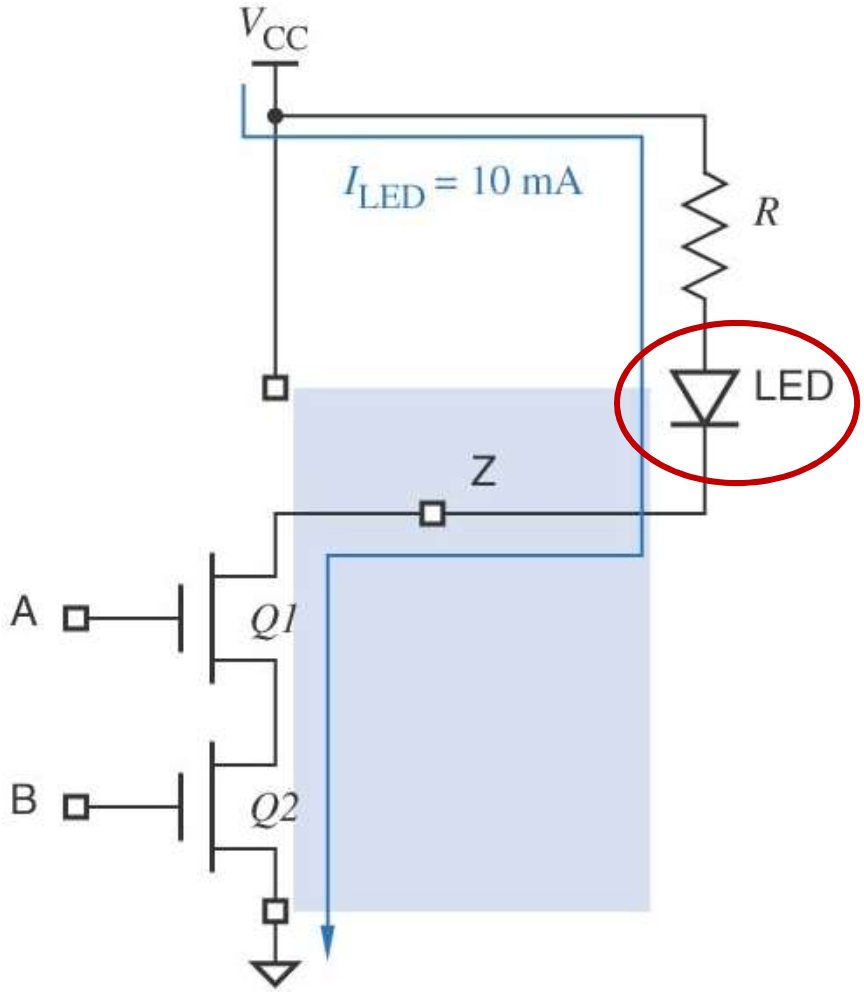
Symbol for open-drain



Application: open-drain output can drive LED

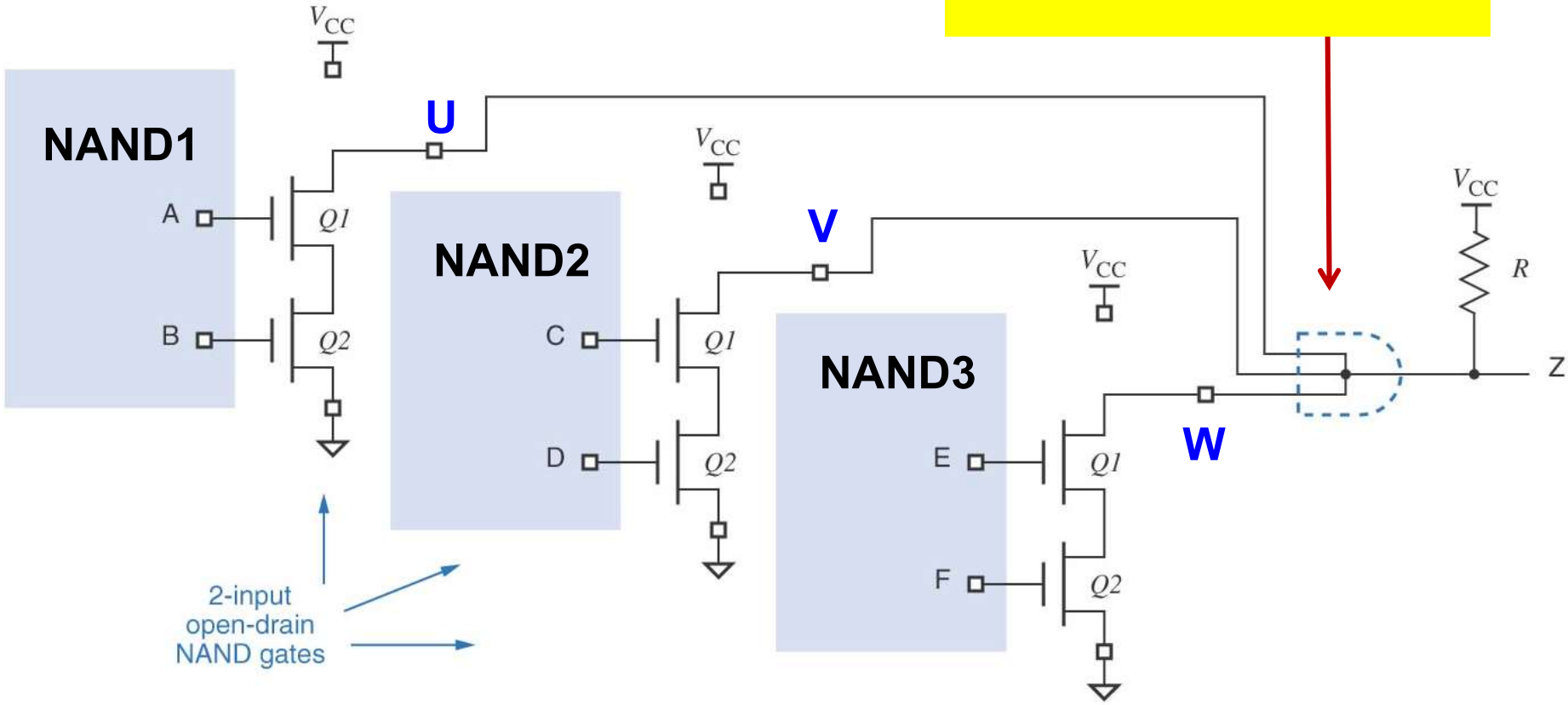
- If A=B=1
- Q1 and Q2 ON
- Z=0
- LED ON

- If A=0 or B=0
- Q1 or Q2 OFF
- Z=1
- LED OFF



Open-drain outputs can be tied together

wired-AND logic
Z = U•V•W



Summary of wired-AND circuit behaviour

Inputs of NAND gates			Outputs	
A=B=1	C=D=1	E=F=1	U, V, W	Z
No	No	No	U=1; V=1; W=1	1
No	No	Yes	W=(EF)'=0; => U=V=0	0
No	Yes	No	V=(CD)'=0; => U=W=0	0
No	Yes	Yes	V=(CD)'=0; W=(EF)'=0; => U=0	0
Yes	No	No	U=(AB)'=0; => V=W=0	0
Yes	No	Yes	U=(AB)'=0; W=(EF)'=0; => V=0	0
Yes	Yes	No	U=(AB)'=0; V=(CD)'=0; => W=0	0
Yes	Yes	Yes	U=(AB)'=0; V=(CD)'=0; W=(EF)'=0	0

Imagine an elastic band: