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NANYANG TECHNOLOGICAL UNIVERSITY

SEMESTER 1 EXAMINATION 2019-2020

CE1005/CZ1005 – DIGITAL LOGIC

Nov/Dec 2019 Time Allowed: 2 hours

INSTRUCTIONS

1. This paper contains 3 questions and comprises 9 pages.
2. Answer **ALL** questions.
3. This is a closed-book examination.
4. Questions do NOT carry equal marks.
5. A single sheet OMR answer sheet and an examination answer booklet are provided.

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1. **Multiple choice:** Answer all sub-questions from Question 1 on the optical mark recognition (OMR) answer sheet provided. There is only one completely correct answer. All sub-questions are worth 2 marks each.

(Total: 40 marks)

(1) Which binary value below is nearest to the decimal value 0.3456?

A. 0.0101 1000 0111 1001
B. 0.0101 1000 0111 1110
C. 0.0101 1000 1000 0001
D. 0.0101 1001 0110 0010
E. 0.0101 1001 1000 1000

(2) The 8-bit signed 2's complement addition (A8h + E7h) will produce:

A. No carry and no overflow
B. Overflow but no carry
C. Both carry and overflow
D. Carry but no overflow; the result is positive
E. Carry but no overflow; the result is negative

Note: Question No. 1 continues on Page 2

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(3) The 8-bit signed 2's complement addition (39h + 4Bh) will produce:

A. No carry and no overflow
B. Overflow but no carry
C. Both carry and overflow
D. Carry but no overflow; the result is positive
E. Carry but no overflow; the result is negative

(4) Which 8-bit signed 2's complement subtraction below will result in arithmetic overflow?

A. 20h – D5h
B. 6Ch – F1h
C. F0h – 29h
D. 83h – 6Ah
E. 54h – E3h

(5) Which requirement below is necessary for device W to drive device X?

A. $V_{IH(min)}$ of X $\geq$ $V_{OH(min)}$ of W
B. $V_{OL(max)}$ of W $\geq$ $V_{IL(max)}$ of X
C. $I_{IH(max)}$ of X $\leq$ $I_{OH(max)}$ of W
D. $I_{IL(max)}$ of W $\leq$ $I_{OL(max)}$ of X
E. All of the above

(6) Which set of parameter values below gives the best DC noise margin among them?

	$V_{IH(min)}$	$V_{OH(min)}$	$V_{OL(max)}$	$V_{IL(max)}$
A.	3.5V	3.8V	0.9 V	1.2V
B.	2.8V	3.2V	1.0 V	1.3V
C.	3.2V	3.6V	1.4 V	2.0V
D.	3.5V	4.0V	1.2 V	1.7V
E.	3.0V	3.5V	1.1V	1.5V

(7) Given that F = [(a'+b)c'd + (a'c)' + b'd']'. Its canonical Boolean expression is:

A. F (a,b,c,d) = $\sum$ m (1, 5, 12)
B. F (a,b,c,d) = $\sum$ m (3, 6, 7)
C. F (a,b,c,d) = $\sum$ m (4, 8, 13)
D. F (a,b,c,d) = $\sum$ m (5, 11, 14)
E. None of the above

Note: Question No. 1 continues on Page 3

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(8) The output G* is asserted only when both inputs A* and C* are asserted and at the same time, either input B* or input D is negated (* denotes active-low). Its canonical Boolean expression is:

A. G* (A*,B*,C*,D) = Π M (0, 4, 5)
B. G* (A*,B*,C*,D) = Π M (2, 4, 9)
C. G* (A*,B*,C*,D) = Π M (3, 9, 12)
D. G* (A*,B*,C*,D) = Π M (5, 10, 15)
E. None of the above

(9) Evaluate these 3 statements about an inverter's open-drain output:

(i) It is valid to connect it to all other types of logic outputs
(ii) It is Hi-Z when the inverter's enable input is negated
(iii) It is used with a pull-up resistor

A. Only statement (i) is true
B. Only statement (ii) is true
C. Only statement (iii) is true
D. Only statements (ii) and (iii) are true
E. None of the statements is true

(10) Evaluate these 3 statements about a Schmitt-trigger inverter's output:

(i) It switches from low to high when the input voltage falls below V_{T+}
(ii) It switches from high to low when the input voltage rises above V_{T-}
(iii) It is indeterminate when the input voltage is between V_{T-} and V_{T+}

A. Only statement (i) is true
B. Only statement (ii) is true
C. Only statement (iii) is true
D. Only statements (i) and (ii) are true
E. None of the statements is true

(11) In Verilog, if A=4'b1010 and B=4'b0110 then A&B is:

A. 1'b0
B. 1'b1
C. 4'b0000
D. 4'b0010
E. None of the above

Note: Question No. 1 continues on Page 4

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(12) Which is a legal negative number in Verilog?

A. 4'd-3
B. 4'-d3
C. 4d'-3
D. -4d'3
E. None of the above

(13) <= is used in Verilog as:

A. A blocking assignment
B. A non-blocking assignment
C. A combinational assignment
D. A conditional less than or equal operator
E. There are multiple correct answers

(14) In an **always @ *** block, if a variable is not assigned in all execution paths, then:

A. A don't care is inferred
B. A latch is inferred
C. The synthesis process will fail
D. The variable will be set to 0
E. There are multiple correct answers

(15) If X is an 8-bit number, which of the following will left extend X by three bits?

A. (X[7], X[7], X[7], X)
B. {3(X[7]), X}
C. {{3{X[7]}}, X}
D. Answers B. and C.
E. They are all correct

(16) Which of the following is true about an **always** statement?

A. There may be exactly one always block in a design
B. There may be exactly one always block in a module
C. Execution of an always block occurs exactly once
D. It may be used to generate a combinational circuit
E. There are no correct answers

Note: Question No. 1 continues on Page 5

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(17) If a=1, then **assign y=(a==2'b11);** results in y being:

A. 1
B. 1'b0
C. 2'b11
D. The value of y is unknown
E. None of the above

(18) A module (or gate level primitive) can be instantiated within an always block:

A. Anywhere within the body of the always block
B. Only at the top of the always block
C. Only for combinational always blocks
D. Answers B. and C.
E. None of the above

(19) If A=1'b0, B=2'b10 and C=2'b01 then y= {A, B[0], C[1]} equals:

A. 3'b000
B. 3'b001
C. 3'b010
D. 3'b011
E. 3'b111

(20) For a J-K flip-flop, what must the J and K inputs be set to for it to toggle?

A. J = 0, K = 0
B. J = 0, K = 1
C. J = 1, K = 0
D. J = 1, K = 1
E. A J-K flip-flop will not toggle. Only a T flip-flop will toggle

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2. (a) Give the **8-bit 2's complement representation** for the following signed decimal values:

(i) -74

(ii) +38

(2 marks)

(b) Use Boolean algebra to arrange the following expression into **POS** (product-of-sum) form. Show each step clearly.

F (w, x, y, z) = [z' (w + x + y')' + x y z (w z)' + w x' y' z']'

(6 marks)

(c) Sketch a logic circuit diagram for the function G = (a' + b)' (c d)' using **2-input NOR gates only**. Assuming each NOR gate has a propagation delay of T, what is the **total propagation delay** of this circuit?

(6 marks)

(d) Sketch **timing waveforms** to illustrate the following parameters clearly:

- t_r
- t_f
- t_{PHL}
- t_{PLH}

(4 marks)

(e) There are four logic components each with an active-low enable input. Any one of the four can be enabled but only one at a time. All four components may be disabled at the same time. Sketch a **logic circuit diagram with matched bubbles** to illustrate clearly how the above selection may be accomplished with a minimum number of logic inputs. State your assumption, if any.

(5 marks)

Note: Question No. 2 continues on Page 7

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(f) A logic circuit has 4 inputs A, B, C, D* and output Y, where * denotes active low. Its behavior is specified in Table Q2. Use a Karnaugh map to obtain a **minimum-cost SOP** (sum-of-product) expression for the output Y. Show the loops clearly.

(7 marks)

Table Q2

Inputs				**Output**
A	B	C	D*	Y
Asserted	X	Asserted	Asserted	Asserted
X	Asserted	Asserted	Asserted	Asserted
Asserted	Asserted	X	Asserted	Asserted
Asserted	Asserted	Asserted	X	Asserted
X	X	Negated	Negated	Negated
Negated	Negated	X	X	Negated
All other combinations not specified above				X

X denotes "don't care"

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3. (a) The circuit given in Figure Q3a uses a 3-8 decoder to implement a common logic function with two outputs, X and Y.

(i) Using a truth table, or any other means, determine the function of the circuit given in Figure Q3a.

(6 marks)

(ii) Write the Verilog code to perform the same function using just a single **assign** statement.

(2 marks)

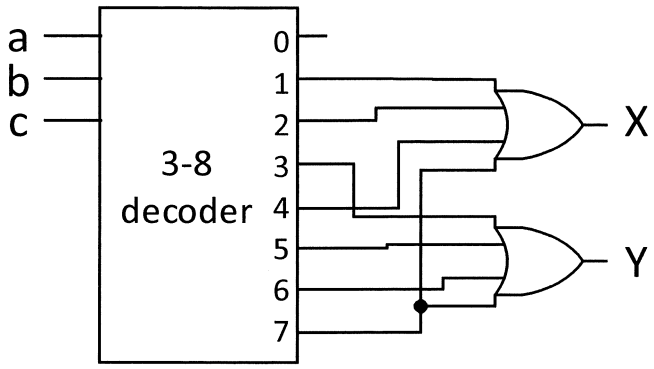

Figure Q3a

(b) A simple rising edge detector generates a pulse (P) with a 1 clock cycle duration whenever the input (I) changes from 0 to 1. The state diagram for the edge detector is given in Figure Q3b. A reset (rst) should force the detector to *state A*. A partial Verilog template is given in Figure Q3c.

(i) Using a single case statement within a single **always** block, implement the *next state* and *output* logic. There is no need to reproduce any of the code in Figure Q3c.

(9 marks)

(ii) Draw the state transition table for the state diagram given in Figure Q3b showing the *next state* and *output* transitions. Use signal names S1, S0, I for the inputs and N1, N0 and P for the outputs, respectively, with the same state assignment as defined in the parameter statement of Figure Q3c.

(4 marks)

(iii) Determine the minimum sum-of-products Boolean expressions for the *next state* and *output* signals.

(4 marks)

Note: Question No. 3 continues on Page 9

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(iv) Write the Verilog code for the *next state* and *output* signals using three separate **assign** statements.

(3 marks)

(v) In not more than two brief sentences, compare and contrast the readability of the two Verilog implementation styles in Q3(b)(i) and (iv), particularly in terms of understanding functionality when another programmer will be involved.

(2 marks)

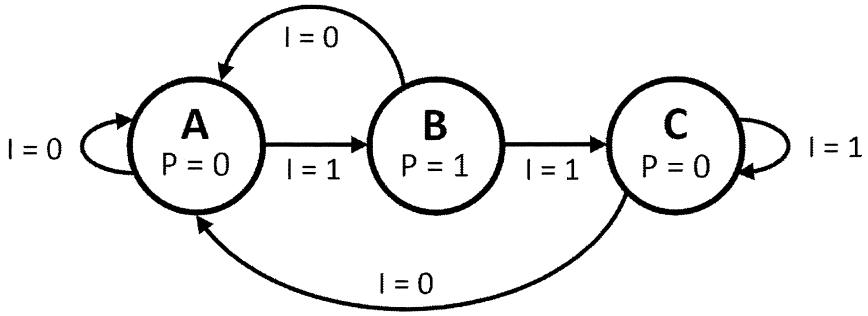

Figure Q3b

```
module edge_detector (input clk, rst, I, output reg P);
    parameter A=0, B=1, C=2;
    reg [1:0] nst, st;
    // Enter Next state and Output logic below


    always @ (posedge clk)          // State logic
    begin
        if (rst) st <= A;
        else st <= nst;
    end
endmodule
```

Figure Q3c

END OF PAPER

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1. **Please do not turn over the question paper until you are told to do so. Disciplinary action may be taken against you if you do so.**

2. You are not allowed to leave the examination hall unless accompanied by an invigilator. You may raise your hand if you need to communicate with the invigilator.

3. Please write your Matriculation Number on the front of the answer book.

4. Please indicate clearly in the answer book (at the appropriate place) if you are continuing the answer to a question elsewhere in the book.