NANYANG TECHNOLOGICAL UNIVERSITY

SEMESTER 1 EXAMINATION 2016-2017

CE1005/CZ1005 – DIGITAL LOGIC

Nov/Dec 2016 Time Allowed: 2 hours

INSTRUCTIONS

1. This paper contains 4 questions and comprises 6 pages.
2. Answer **ALL** questions.
3. This is a closed-book examination.
4. All questions carry equal marks.

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1. (a) A pair of transmitter and receiver uses odd parity to transmit data. In one instance, an 8-bit data CD (hexadecimal) is to be transmitted.

   (i) Determine the 9 bits to be transmitted, with the leftmost bit being the parity bit.

   (2 marks)

   (ii) The 9-bit binary value 111001001 is received, with the leftmost bit being the parity bit. Determine whether or not it is correct by comparing with the value in Q1(a)(i). Is the receiver able to correctly detect the absence or presence of error in this case using the parity method? Explain your answers clearly.

   (4 marks)

   (b) (i) Convert the unsigned decimal value 31.26 to binary. Give your answer in 12 significant bits. Show all steps clearly.

   (3 marks)

   (ii) Determine the minimum number of bits required to represent an unsigned 18-digit decimal integer. Show all steps clearly.

   (3 marks)

Note: Question No. 1 continues on Page 2

(c) Simplify the following Boolean expression using algebraic manipulation. Give your answer in SOP (sum-of-product) form.

$$F = [\ (x'\ y' + (w\ y\ z)\ '\ ]\ ' + (w\ z + x)\ (w' + y' + x\ z)\ '$$

(7 marks)

(d) Sketch the timing waveforms for the following logic signals for time interval t = 0-300ns. Label the time scale, signal names and show the timing relations between the signals clearly. Ignore any rise time, fall time and propagation delay.

- Active low RESET* is asserted for t = 0-150ns and negated thereafter.
- Active high EN is asserted for t = 100-250ns and negated otherwise.
- Active low AIN* is asserted for t = 50-200ns and negated otherwise.
- Active low XOUT* is asserted when both EN and AIN* are asserted and RESET* is negated. Otherwise it is negated.

(6 marks)

2. (a) A 5-digit decimal number is used to specify the export destination of a factory's products as shown in Table Q2, where x is a digit between 0 to 9 depending on the specific city.

Table Q2

5-digit number	Export destination
0xxxx	Local cities
1xxxx	Cities in Africa
2xxxx	Cities in Southeast Asia
3xxxx	Other cities in Asia
4xxxx	Cities in Australia
5xxxx	Cities in Western Europe
6xxxx	Other cities in Europe
7xxxx	Cities in North America
8xxxx	Cities in South America
9xxxx	Other destinations not included above

A logic circuit takes the most significant digit of the 5-digit number as a 4-bit BCD (Binary-Coded Decimal) input and produces an output Z such that Z=1 for any export destination in Asia (including Southeast Asia), Australia, North and South Americas; and Z=0 otherwise.

Note: Question No. 2 continues on Page 3

(i) Write the canonical sum-of-minterm expression for Z.

(1 mark)

(ii) Write the canonical product-of-maxterm expression for Z.

(1 mark)

(iii) Design the logic circuit with the use of a Karnaugh map. Take advantage of any "don't care" input conditions. Show the loops clearly and obtain a minimum-cost SOP (sum-of-product) expression for Z.

(8 marks)

(b) Figure Q2 shows a circuit with two tristate components.

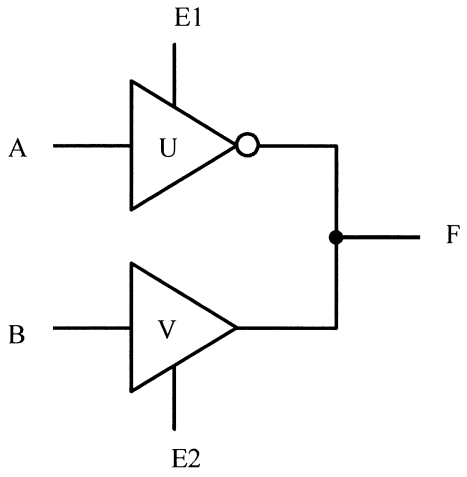

Figure Q2

(i) Identify the components U and V.

(1 mark)

(ii) Briefly describe the function of the inputs E1 and E2.

(2 marks)

(iii) Briefly explain what may happen to F if both E1 and E2 are set to logic 1 at the same time.

(2 marks)

(iv) Construct the truth table for the output F. Assume that E1=E2=1 cannot occur.

(4 marks)

Note: Question No. 2 continues on Page 4

(c) Two 8-bit signed numbers in the 2's complement format are given as follows:

- X = 63 (hexadecimal)
- Y = B5 (hexadecimal)

(i) Determine the signed decimal value of X and of Y.

(2 marks)

(ii) Perform the arithmetic operation X + Y and give the answer in hexadecimal. Show all steps clearly and state whether or not there is overflow.

(2 marks)

(iii) Perform the arithmetic subtraction X - Y and give the answer in hexadecimal. Show all steps clearly and state whether or not there is overflow.

(2 marks)

3. (a) For the circuit shown in Figure Q3, gate-delays of the NOT gates and the AND gate are 1ns and 2ns, respectively.

(i) Explain the functionality of the circuit shown in Figure Q3.

(3 marks)

(ii) Determine the output oscillation frequency of the circuit.

(3 marks)

(iii) Write a structural Verilog program to implement the circuit shown in Figure Q3.

(4 marks)

(b) For the given function F(a,b,c) = ab'c + a'bc' + a'b'c' + a'b'c + abc

(i) Without simplifying the Boolean equation, implement the function by using one 4x1 multiplexer. You may use NOT gate to invert any input if needed.

(8 marks)

Note: Question No. 3 continues on Page 5

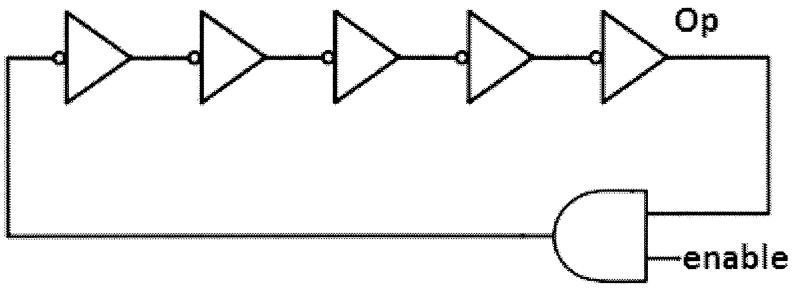

Figure Q3

(ii) Write a Verilog module for the circuit implemented in Q3(b)(i) using CASE statement.

(7 marks)

4. (a) Describe the difference between blocking and non-blocking assignment in Verilog.

(5 marks)

(b) You are required to design a special up-down counter. The counter never counts below 3 and above 11. The counter has a reset input (R) that sets it to 7 (that is, when R is 1), and a direction input (D) that determines whether it counts up or down (up if D is 0 and down if D is 1). If the counter is reset to 7 and D is 1, its successive states will then be 6, 5, 4, 3 and it will stay at 3 until R is 1 or D is 0. Similarly, if after reset D is 0, its successive states will then be 8, 9, 10, 11 and it will stay at 11 until R is 1 or D is 1.

(i) Draw the state transition diagram for the special up-down counter.

(7 marks)

(ii) Write a Verilog module to implement the special up-down counter.

(8 marks)

Note: Question No. 4 continues on Page 6

(c) Figure Q4 shows a Finite State Machine (FSM) that detects a particular bit sequence. Determine the output sequence for the following sequence of inputs:

1,1,0,0,0,1,0,0,0,1,1

(5 marks)

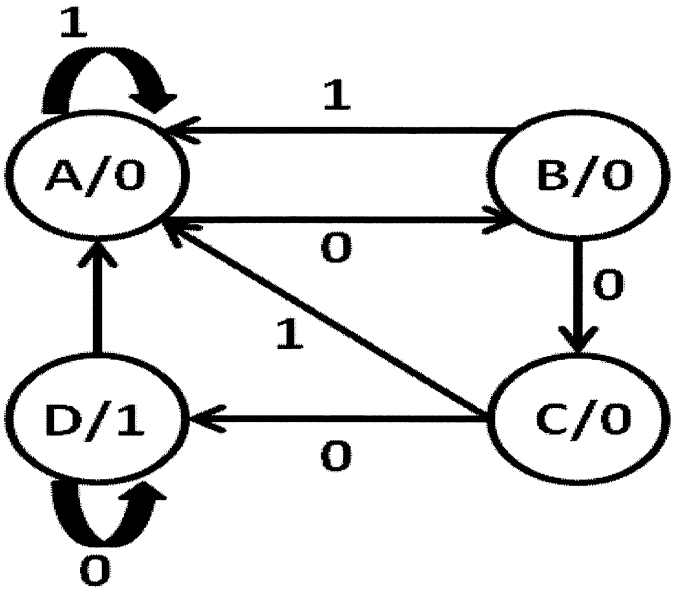

Figure Q4

END OF PAPER

1ai) odd parity

Xxxx xxxx
0 1100 1101

ii) cannot detect. The number has odd ones.

bi) dec → 31.26 ⇝ 11111.010001 0

31 ÷ 2 = 15 R1
15 ÷ 2 = 7 R1
7 ÷ 2 = 3 R1
3 ÷ 2 = 1 R1
1 ÷ 2 = 0 R1

0.26 × 2 = 0.52
0.52 × 2 = 1.04
0.04 × 2 = 0.08
0.08 × 2 = 0.16
0.16 × 2 = 0.32
0.32 × 2 = 0.64
0.64 × 2 = 1.28
0.28 × 2 = 0.56

ii) Unsigned 18-digit number, max is

$$999999999999999999 = 2^{n}$$

$$n = \frac{\ln(1\times10^{18}-1)}{\ln(2)}$$

$$n = 59.7947$$

$$\approx 60_{11}$$

c) $F = [(x'y' + (wyz)')' + (wz + x)(x' + y' + xz)'$

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