5.1 Input/Output (I/O) Interface

1) With reference to the computer system diagram (Figure 1) in the case study notes,

(a) What are the type (input, output or bi-directional) of processor pins you would connect each of the module's data signal to?

Table 1a

No.	Module	Type (Input, Output or Bidirectional)
i.	Buttons	Input
ii.	Wifi	Bidirectional
iii.	Touch Screen Controller	Input
iv.	System Memory	Bidirectional
v.	Display	Output

(b) Given the following interface requirement, select the appropriate module from the device information list in the case study notes to connect to the processor.

Table 1b

No.	Module	Interface Type	
i.	Wifi	SPI Serial	Sync
ii.	Touch Screen Controller	UART Serial	Async
iii.	System Memory	Parallel Bus Parallel	Sync

(c) For each of the interface shown in **Table 1b**, is the data transfer serial or parallel?

(d) Describe the difference between synchronous and asynchronous interface. Are the interfaces shown in **Table 1b** asynchronous or synchronous? Explain.

(e) With reference to the SPI wifi module chosen in 1(b) above, what is the maximum speed that data can be transferred between the wifi module and the processor?

(f) With reference to the device information of the system memory you have chosen in 1(b) above, what is the maximum data transfer rate achievable between the system memory and the processor? Assuming that data on the parallel bus gets transferred on each rising edge of the data strobe.

Q.

Touch Controller: TS002UART, 3V, UART

WIFI: WIFI0010AC, 3V, SPI

Memory: : DRAM0002-16M16 SRAM0002-2M16

EEPROM0001-256K NOR0001-1M

(e) With reference to the SPI wifi module chosen in 1(b) above, what is the maximum speed that data can be transferred between the wifi module and the processor?

SPI @ 50MHz, only WIFI10010AC compat

50 MHz = 50mbps

(f) With reference to the device information of the system memory you have chosen in 1(b) above, what is the maximum data transfer rate achievable between the system memory and the processor? Assuming that data on the parallel bus gets transferred on each rising edge of the data strobe.

: DRAM0002-16M16 16 bit @ 100 MHz = 1600 Mbps

SRAM0002-2M16 16 bit @ 200 MHz = 3200 Mbps

EEPROM0001-256K 50 MHz @ 1bit = 50 Mbps

NOR0001-1M 16 bit @ 10 MHz = 160 Mbps

5.2 Data Transfer

2) **Fig. 2** shows the logical waveform of an asynchronous data frame.

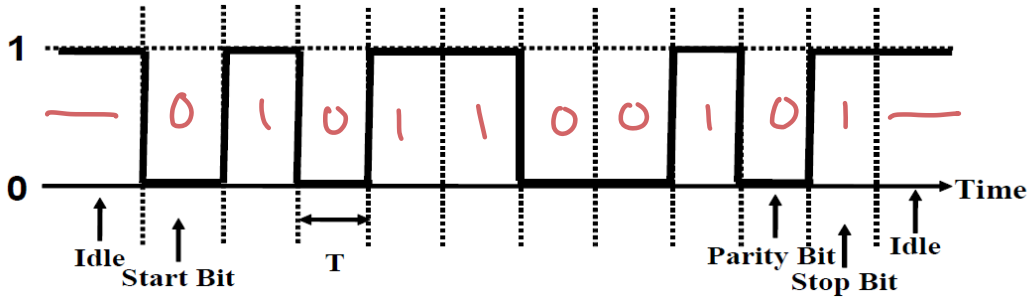


Fig. 2

Answer the following question with reference to **Fig. 2**:

(a) Specify the 7-bit ASCII character that is transmitted (LSB is transmitted first).

1001101 = 0x4D = 'M'

(b) Assume there are no errors in the transmitted waveform, state whether even or odd parity is being used.

Even

(c) Assume two of the bits received in the character are erroneous; can the receiver detect the error? Can you extend the example to determine the limitations of parity checking?

If 0/1 swap, dk error

(d) If 7-bit ASCII characters are transmitted continuously in the format shown (with no idle periods between the frames) at a baud rate of 9600, calculate the following:

i. The value of **T** in **Fig 2**.

ii. The data transfer rate of this serial interface in characters per second (cps).

i) $T = \frac{1}{9600} = 1.041$ ms ii) 9600 bps / 10 = 960 char per sec

(e) Re-compute the data transfer rate (cps) if the transmission does not use any parity bit. Compare the results with those obtained in Q3d(ii), and state your observation(s).

9600/9 = 1066.6 cps / Faster

(f) Assume the baud rate of the transmitter is 4800, but the baud rate of the receiver is configured as 9600. Based on **Fig. 2**, determine, if any, the ASCII character(s) that will be received.

recieve @ double...

7E1

00 11 00 11 11 00 00 11 00 11

0 11 00 11 (1) 0 00 11 00 (1) Both flag

'f' 'CAN'

(Not necessary to be covered during tutorial)

3) There has been a trend of 'serialization' of interface bus standard. E.g. USB replacing Parallel Port Interface, SATA replacing IDE in HDD.
   (a) What are the advantages that Serial Bus has over Parallel Bus interface that enticed industry player to move in this direction?
   (b) What are the scenarios in which Parallel bus will still be preferred over Serial bus? What are the design considerations that need to be put in place in such cases?

4) In Q3(f) above, a wrong sampling result is observed when a wrong baud rate is used. This can actually be used to implement auto baud rate detection. Briefly describe how this can be done.

TUTORIAL #6 Polling, Interrupts and DMA (SC1006/Cx1106)

6.1 Interrupts

1) Consider the system diagram in Figure 1 of case study notes.
   - The processor UART peripheral in its Serial I/O module is configured to receive data with format of 1 start-bit, 7 data-bits, 1 parity-bit and 1 stop-bit.
   - Each time the UART peripheral receives a character, it'll store the data into a buffer.
   - It will then interrupt the CPU to notify CPU that there is data available.
   - The CPU will then execute the Interrupt Service Routine (ISR) to read the character received.
   - Interrupt Latency is the term used to describe the time between interrupt request and entrance to ISR.
   - The minimum interrupt latency for the CPU is 10 μs and it takes 90 μs for the CPU to execute the instructions in the ISR (read the received data from the buffer).
   - Assume that the UART data is transferred back to back i.e. no delays between each UART packets.

   What is the maximum baud rate that can be supported with this UART interface?

2) The specifications of the system in Figure 1 (case study notes) requires the buttons to be asserted 400 times over a 24-hour period. Given that the processor consumes 0.1mA current when it is idling and 50mA when it is in active mode i.e. running code, answer the following.

   (a) Supposed polled IO technique is used to sample the button status. Given that the processor poll the buttons every 100ms, each poll requires the processor to be active for 10ms, what is the average current consumed over the 24-hour period?

   (b) If interrupt-driven I/O is used to sample the button status, what is the average current consumed in the same 24-hour period? Given that it takes 20ms to service each interrupt, including interrupt latency and ISR execution.

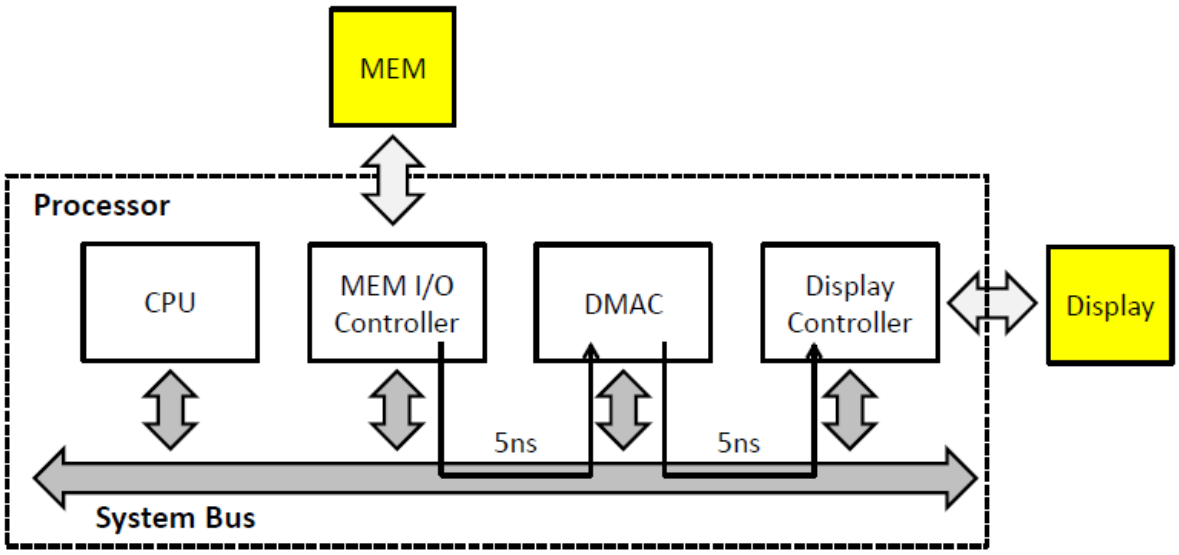
   (c) Given that a battery with capacity of 2000mAh means that it can supply 2000mA continuously for 1 hour, or 1000mA continuously for 2 hours. How long would a battery of 2000mAh last when used in (a) and (b) above?

6.2 Direct Memory Access (DMA)

3) Given that DMAC and CPU share one system bus, list four possible factors that might affect the transfer rate of a DMAC and explain how they affect the DMAC transfer rate.

4) Consider the system in Figure 1 (Case study notes). Given that

- The processor's system bus is capable of supporting simultaneous transfer of up to 3 bytes of data at one time.
- DMA is used to transfer video data from Memory to Display Controller module.
- Each video pixel data consist of three bytes (Red, Green, Blue) and are transferred simultaneously on the system bus on each bus cycle.
- Each transfer on the system bus takes 5ns and transfer of the bus control between the CPU and the DMAC takes 100ns.
- Assume that DMAC is using Fetch-and-Deposit DMA.
- Note that 1Kbyte = 1024 Byte.



(a) Given that the video is output at a rate of 30 frames per second and each video frame has a resolution of 1920x1080 pixels. If burst-mode was used by the DMAC to burst one frame of video data at a time, would the DMAC be able to transfer each video frame completely?

(b) Repeat the calculation if the DMAC is using cycle-stealing mode, assume that DMAC needs to wait at least 5 instructions before it could request for control of the system bus again.