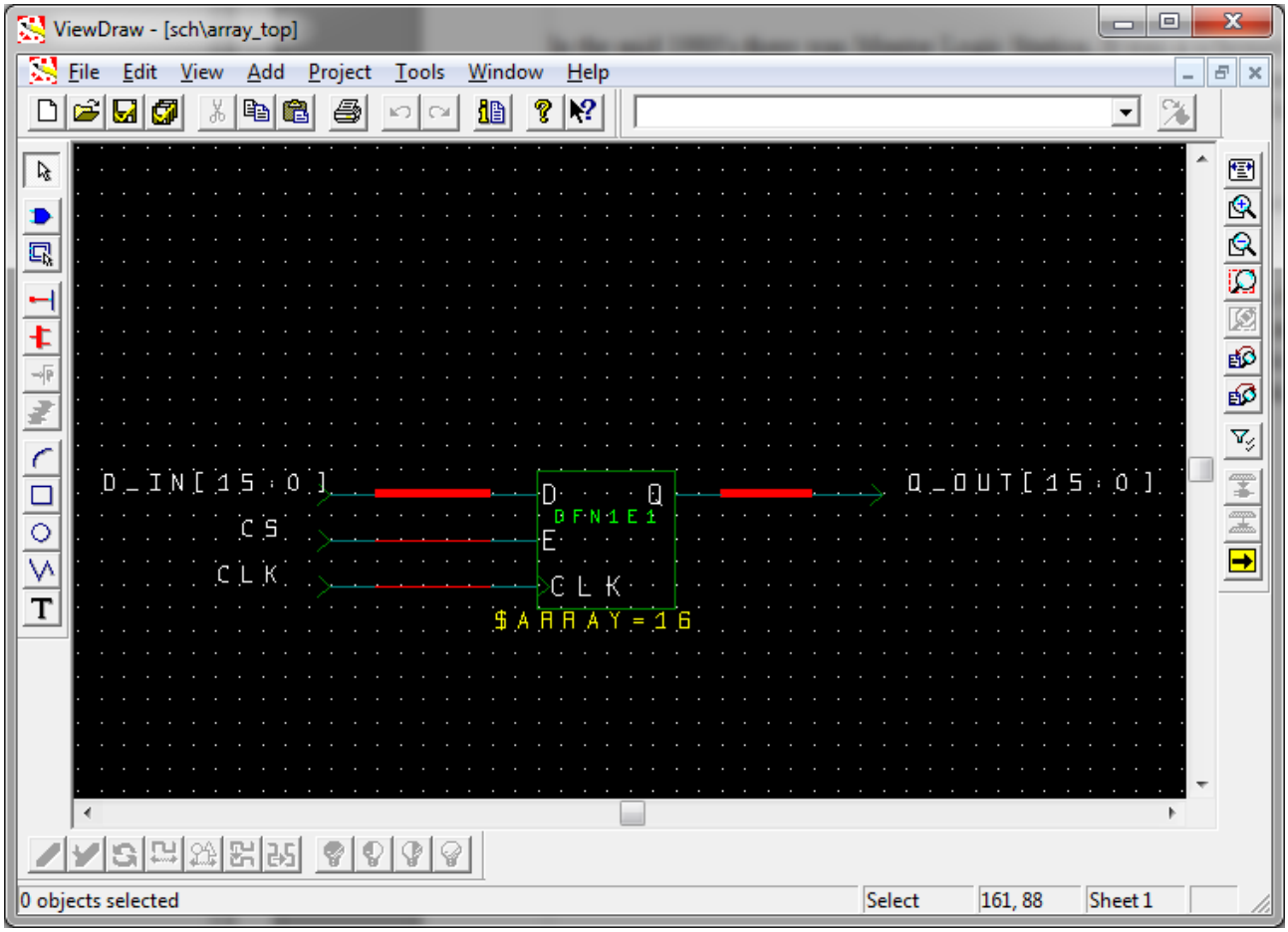
A Proposal to Simplify the Instance Array Syntax of PHDL

Guys, I have been thinking about the instance array syntax we have now and trying to figure out what bothers me about it. Now I believe it just lacks the obvious simplicity of the rest of the language. We are not the first look for such a syntax but others were working on the problem of logic design.

In the mid 1980's there was Mentor Logic Station. It was a schematic editor that allowed you to put "for", "if" and "while" blocks on the schematic. The blocks contained these statements and provided dummy variables to the schematic within. This worked very well for logic design and was a forerunner to VHDL and Verilog.

VHDL provides "for...generate" and "if...generate" control structures for instantiating logic. This also works well for logic design.

ViewDraw was another schematic editor for logic design also became available in the early 1980's. ViewDraw is still around and it is bundled with the Actel FPGA design tools. ViewDraw provides a very simple and natural mechanism for replicating logic. I think this approach is very similar to what we are trying to accomplish in PHDL so I will include an example schematic.



If you look at the schematic you see there is a normal D flip-flop with clock enable. A ViewDraw attribute is added to the flip-flop to indicate that it is replicated 16 times, $ARRAY=16. The D input and Q output of the flip-flop are each connected to 16 bit busses. In this way we form a 16 bit register. The E and CLK pins of the flip-flop are connected to single nets. This means that the E pin of all 16 flip-flops is connected to the same net, CS. The same situation with the CLK pin, the same clock net drives all 16 flip-flops of the register.

In the old days you could also put an arrayed name on the component, say "DFF[15:0]", and that would get expanded onto the individual flip-flops as "DFF15", "DFF14", ... That funtionality has been removed from ViewDraw as it exists today.

I suggest we simplify the instance array capability of PHDL to support only this style of replication. In effect, what I am saying is that we do not need the combine() function or the this() function. The code would look like this for an array of flip-flop chips (if such things even exist anymore).

```
************************************************************
design myDesign {
        net[15:0] d_in, q_out;
        net cs, clk;

        inst(15:0) flip_flops of flip_flop_chip {
                attribute REFDES =
                "U45,U44,U43,U42,U41,U40,U39,U38,U37,U36,U35,U34,U33,U32,U31,U30";

                d = d_in; q = q_out; clk = <clk>; en = <cs>; vcc = <+3v3>; gnd = <gnd>;
        }
}
************************************************************************
```

Please notice that I have suggested a syntax for controlling reference designators for an arrayed component.

My feeling is that this simple functionality will cover 99% of the use cases. If you really need something like this() or combine() you probably really should not use an inst array anyway for readability reasons.