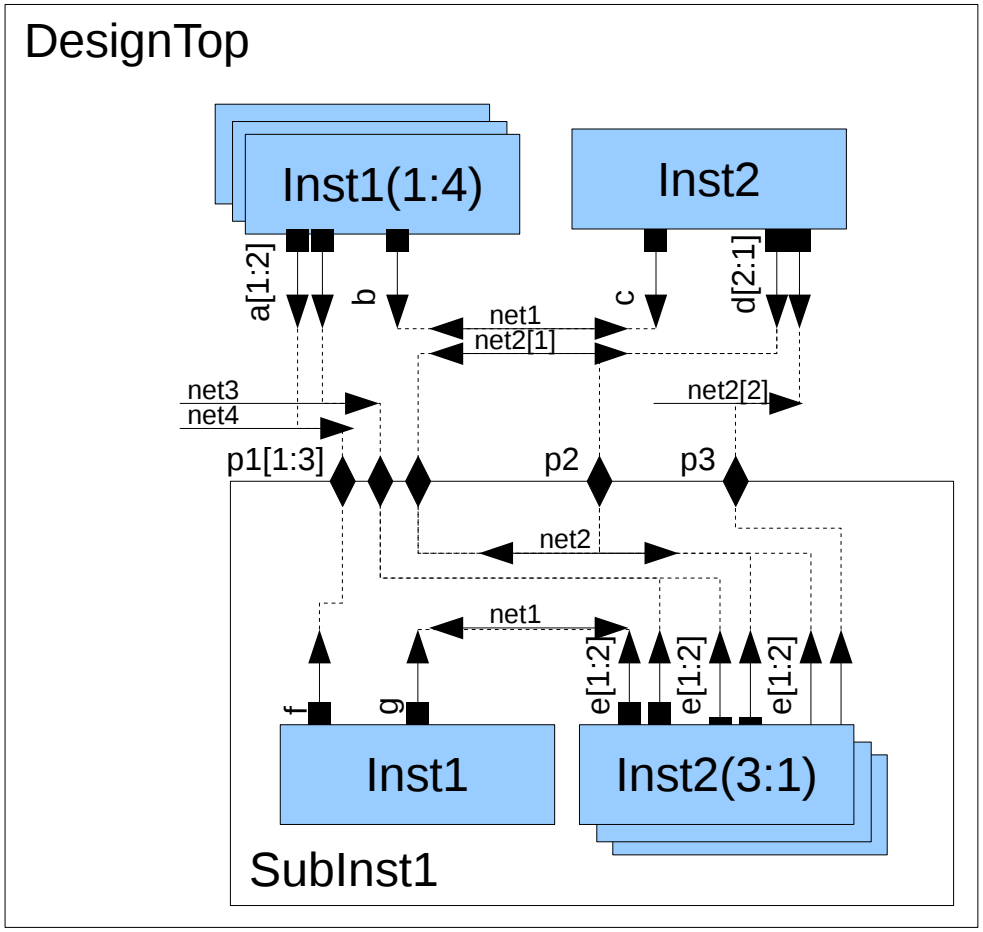
NetListGenerator Test Case 04



Reference Designations		Package	Device	Pin Mappings	
Inst1(1)	A1	pkg1	dev1	Inst1(1:4).a[1]	1
Inst1(2)	A2	pkg1	dev1	Inst1(1:4).a[2]	2
Inst1(3)	A3	pkg1	dev1	Inst1(1:4).b	3
Inst1(4)	A4	pkg1	dev1	Inst2.c	1
Inst2	B1	pkg2	dev2	Inst2.d[2]	2
SubInst1.Inst1	C1	pkg3	dev3	Inst2.d[1]	3
SubInst1.Inst2(3)	D3	pkg4	dev4	SubInst1.Inst1.f	1
SubInst1.Inst2(2)	D2	pkg4	dev4	SubInst1.Inst1.g	2
SubInst1.Inst2(1)	D1	pkg4	dev4	SubInst1.Inst2(3:1).e[1]	1
				SubInst1.Inst2(3:1).e[2]	2

```
!PADS-POWERPCB-V9.0-MILS! NETLIST FILE...
*PART*
  A1 dev1@pkg1
  A2 dev1@pkg1
  A3 dev1@pkg1
  A4 dev1@pkg1
  B1 dev2@pkg2
  C1 dev3@pkg3
  D3 dev4@pkg4
  D2 dev4@pkg4
  D1 dev4@pkg4
*CONNECTION*
*SIGNAL* NET1
  A1.3 A2.3
  A2.3 A3.3
  A3.3 A4.3
  A4.3 B1.1
*SIGNAL* NET2[1]
  B1.2 D2.2
  D2.2 D1.1
*SIGNAL* NET2[2]
  B1.3 D1.2
*SIGNAL* NET3
  A1.2 A2.2
  A2.2 A3.2
  A3.2 A4.2
  A4.2 D3.2
  D3.2 D2.1
*SIGNAL* NET4
  A1.1 A2.1
  A2.1 A3.1
  A3.1 A4.1
  A4.1 C1.1
*SIGNAL* SUBINST1.NET1
  C1.2 D3.1

*END*
```