

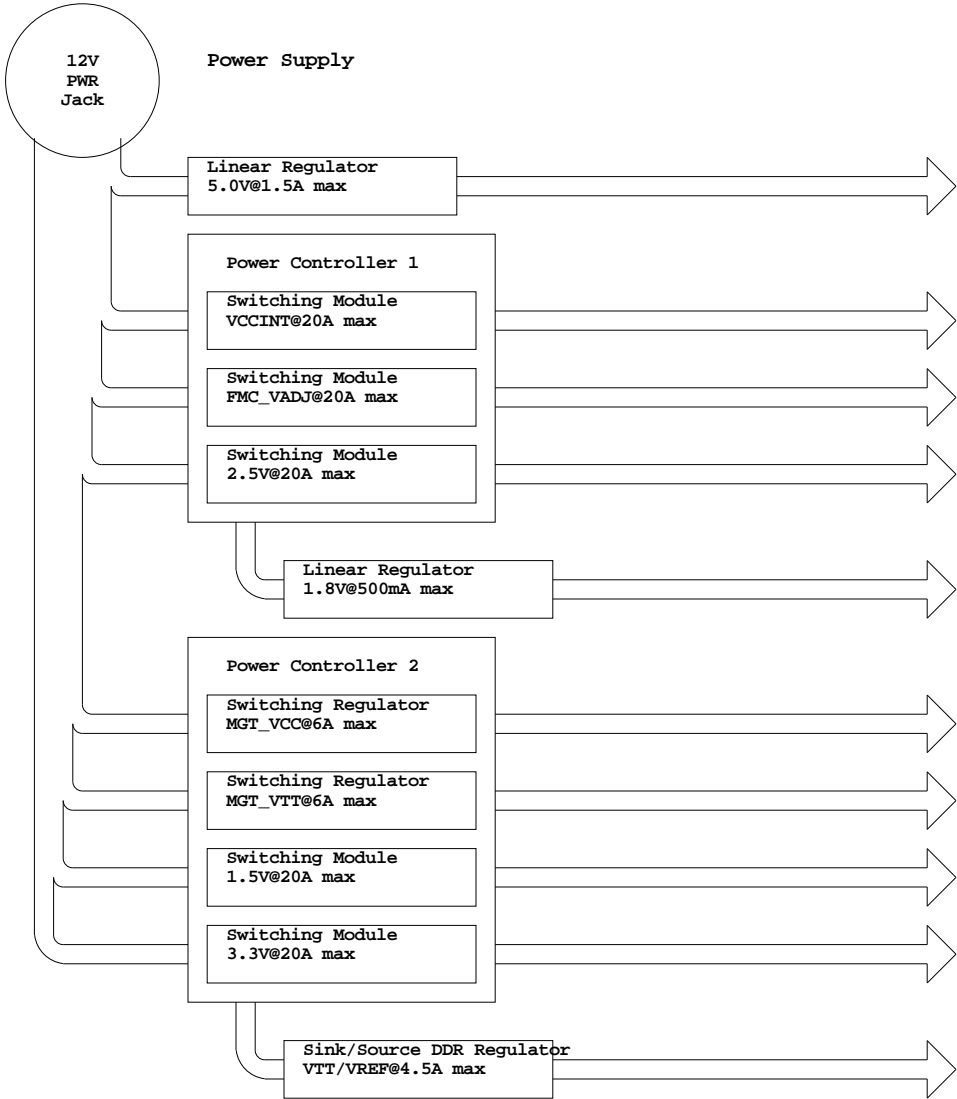
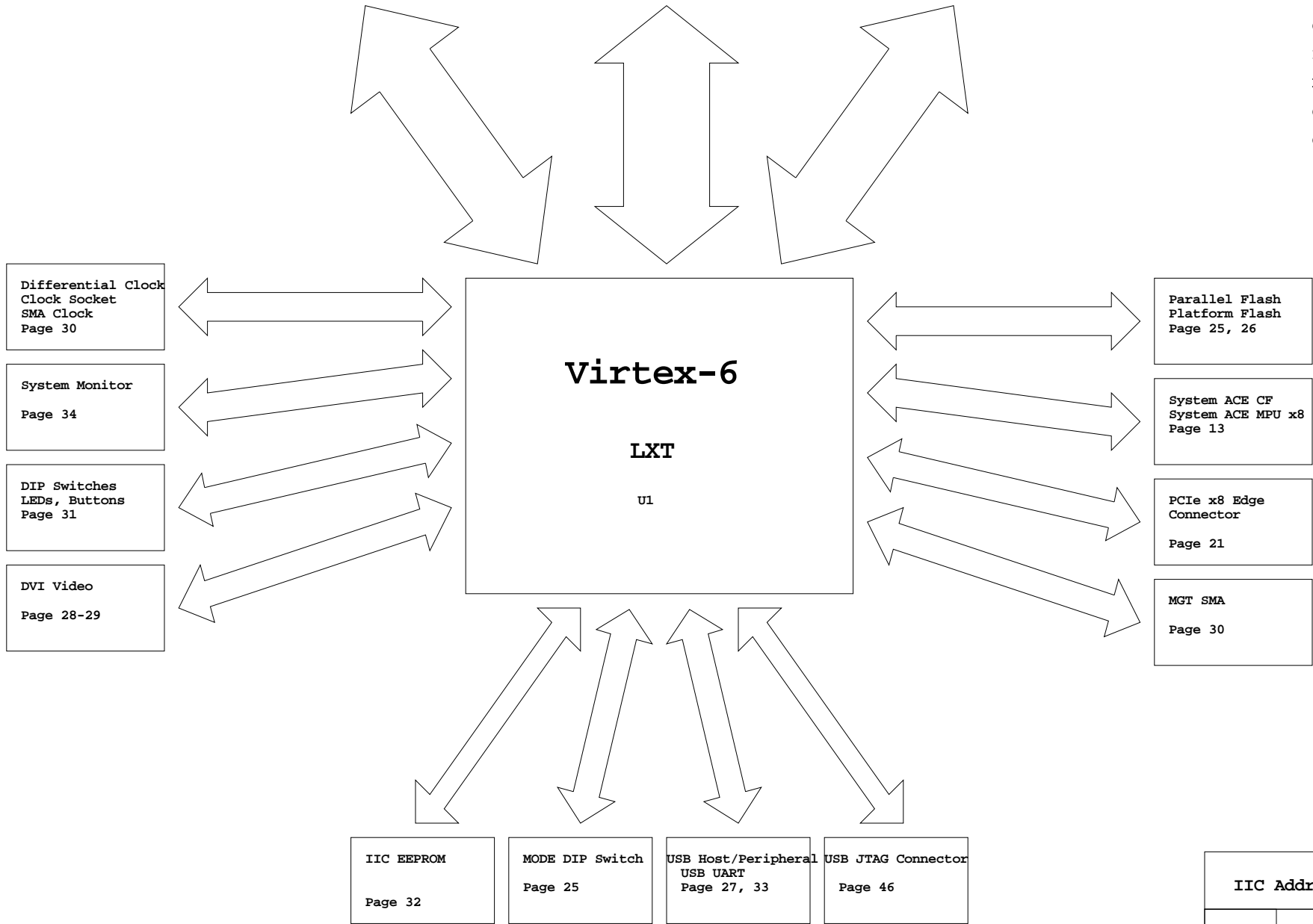
DDR3 SODIMM
Page 15

FMC HPC/LPC Expansion
Connectors
Page 16-20

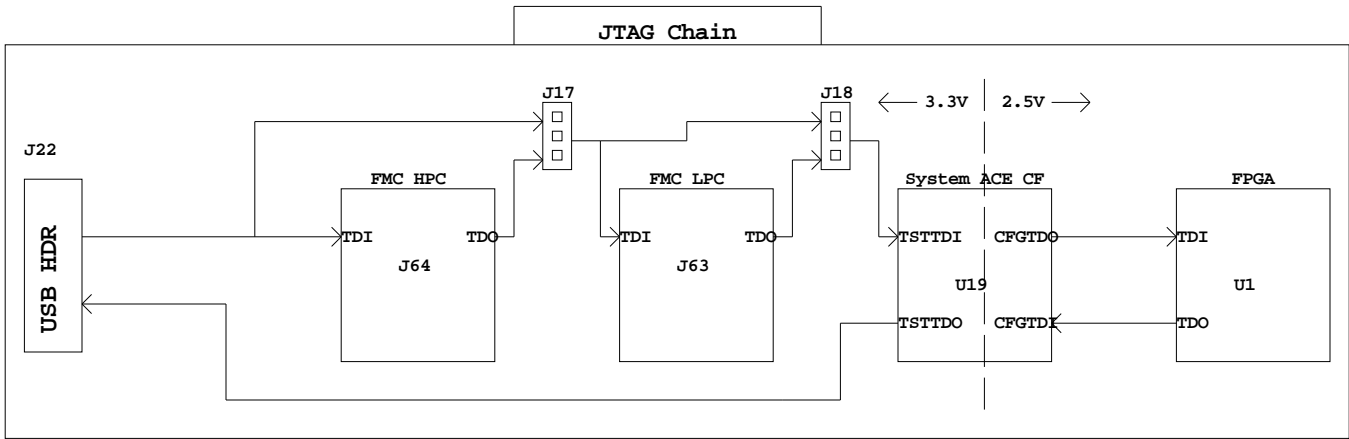
10/100/1000 Ethernet
MII/GMII/RGMII/SGMII
Page 24

Disclaimer:

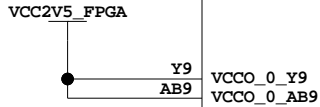
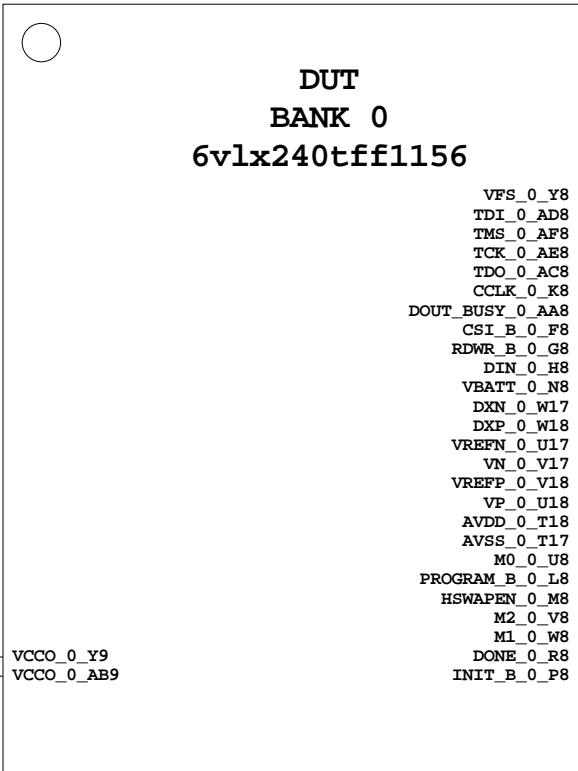
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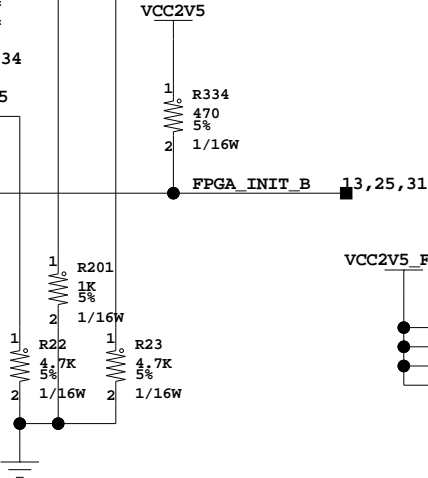
| IIC Addressing | |
|----------------|------------------------|
| U6 | 0b1010100 |
| J63 | 0bXXXXX01 |
| J64 | 0bXXXXX00 |
| J1 | 0b0101011 0b0011011 |



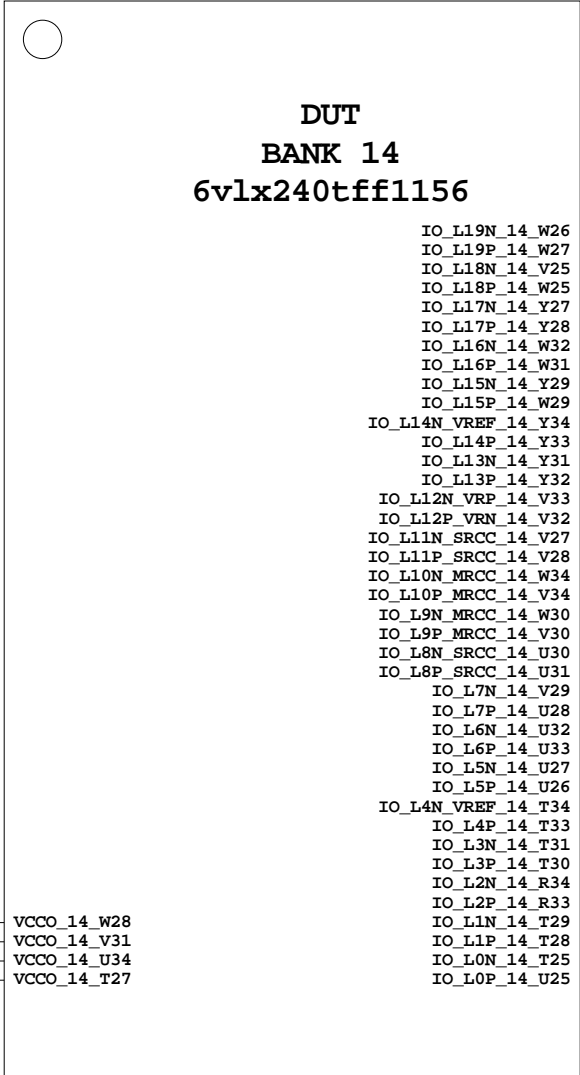
| | | |
|--|-------------|---|
| Title: ML605 Block Diagram SCHEM, ROHS COMPLIANT ML605 EVALUATION PLATFORM | | ASSY P/N: 0431540 PCB P/N: 1280479 SCH P/N: 0381311 |
| Date: 9-17-2009_15:45 | Ver: D | |
| Sheet Size: B | Rev: 04 | |
| Sheet 1 of 48 | Drawn By BF | |




U1



U1



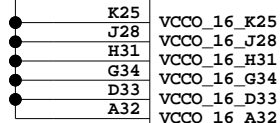
FPGA Banks 0, 14

| | | |
|---|-------------|---|
|  | | |
| Title: FPGA Banks 0, 14 SCHEM, ROHS COMPLIANT ML605 | | ASSY P/N: 0431540 PCB P/N: 1280479 SCH P/N: 0381311 |
| Date: 9-17-2009_15:43 | Ver: D | |
| Sheet Size: B | Rev: 04 | |
| Sheet 2 of 48 | Drawn By BF | |

DUT
BANK 16
6v1x240tff1156

| | | | |
|---------------------|-----|--------------------|----|
| IO_L19N_16_J32 | J32 | FMC_LPC_LA03_N | 20 |
| IO_L19P_16_J31 | J31 | FMC_LPC_LA03_P | 20 |
| IO_L18N_16_L26 | L26 | FMC_LPC_LA09_N | 20 |
| IO_L18P_16_L25 | L25 | FMC_LPC_LA09_P | 20 |
| IO_L17N_16_H32 | H32 | FMC_LPC_LA07_N | 20 |
| IO_L17P_16_G32 | G32 | FMC_LPC_LA07_P | 20 |
| IO_L16N_16_J34 | J34 | FMC_LPC_LA06_N | 20 |
| IO_L16P_16_K33 | K33 | FMC_LPC_LA06_P | 20 |
| IO_L15N_16_D32 | D32 | FMC_LPC_LA11_N | 20 |
| IO_L15P_16_D31 | D31 | FMC_LPC_LA11_P | 20 |
| IO_L14N_VREF_16_H33 | H33 | FMC_LPC_LA05_N | 20 |
| IO_L14P_16_H34 | H34 | FMC_LPC_LA05_P | 20 |
| IO_L13N_16_K29 | K29 | FMC_LPC_LA08_N | 20 |
| IO_L13P_16_J30 | J30 | FMC_LPC_LA08_P | 20 |
| IO_L12N_VRP_16_F34 | F34 | VRP_16 | 3 |
| IO_L12P_VRN_16_E34 | E34 | VRN_16 | 3 |
| IO_L11N_SRCC_16_E31 | E31 | FMC_LPC_LA01_CC_N | 20 |
| IO_L11P_SRCC_16_F31 | F31 | FMC_LPC_LA01_CC_P | 20 |
| IO_L10N_MRCC_16_G33 | G33 | FMC_LPC_CLK1_M2C_N | 20 |
| IO_L10P_MRCC_16_F33 | F33 | FMC_LPC_CLK1_M2C_P | 20 |
| IO_L9N_MRCC_16_K27 | K27 | FMC_LPC_LA00_CC_N | 20 |
| IO_L9P_MRCC_16_K26 | K26 | FMC_LPC_LA00_CC_P | 20 |
| IO_L8N_SRCC_16_C34 | C34 | FMC_LPC_LA13_N | 20 |
| IO_L8P_SRCC_16_D34 | D34 | FMC_LPC_LA13_P | 20 |
| IO_L7N_16_J29 | J29 | FMC_LPC_LA04_N | 20 |
| IO_L7P_16_K28 | K28 | FMC_LPC_LA04_P | 20 |
| IO_L6N_16_B34 | B34 | FMC_LPC_LA14_N | 20 |
| IO_L6P_16_C33 | C33 | FMC_LPC_LA14_P | 20 |
| IO_L5N_16_H30 | H30 | FMC_LPC_LA02_N | 20 |
| IO_L5P_16_G31 | G31 | FMC_LPC_LA02_P | 20 |
| IO_L4N_VREF_16_B33 | B33 | FMC_LPC_LA16_N | 20 |
| IO_L4P_16_A33 | A33 | FMC_LPC_LA16_P | 20 |
| IO_L3N_16_G30 | G30 | FMC_LPC_LA10_N | 20 |
| IO_L3P_16_F30 | F30 | FMC_LPC_LA10_P | 20 |
| IO_L2N_16_E33 | E33 | FMC_LPC_LA12_N | 20 |
| IO_L2P_16_E32 | E32 | FMC_LPC_LA12_P | 20 |
| IO_L1N_16_J27 | J27 | FMC_HPC_PG_M2C_LS | 32 |
| IO_L1P_16_J26 | J26 | FLASH_WAIT | 26 |
| IO_L0N_16_B32 | B32 | FMC_LPC_LA15_N | 20 |
| IO_L0P_16_C32 | C32 | FMC_LPC_LA15_P | 20 |

VCC2V5_FPGA

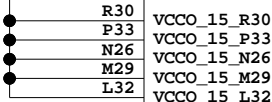


VCCO_16_K25
VCCO_16_J28
VCCO_16_H31
VCCO_16_G34
VCCO_16_D33
VCCO_16_A32

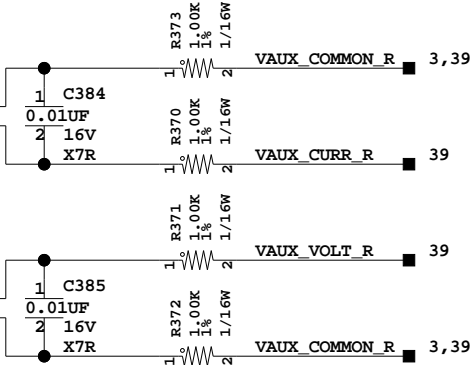
DUT
BANK 15
6v1x240tff1156

| | | | |
|----------------------|-----|-------------------|----|
| IO_L19N_15_R29 | R29 | FMC_LPC_LA20_N | 20 |
| IO_L19P_15_P29 | P29 | FMC_LPC_LA20_P | 20 |
| IO_L18N_15_P34 | P34 | FMC_LPC_LA29_N | 20 |
| IO_L18P_15_N34 | N34 | FMC_LPC_LA29_P | 20 |
| IO_L17N_15_N30 | N30 | FMC_LPC_LA19_N | 20 |
| IO_L17P_15_M30 | M30 | FMC_LPC_LA19_P | 20 |
| IO_L16N_VRP_15_L34 | L34 | VRP_15 | 3 |
| IO_L16P_VRN_15_K34 | K34 | VRN_15 | 3 |
| IO_L15N_SM15N_15_T26 | T26 | FMC_LPC_LA21_N | 20 |
| IO_L15P_SM15P_15_R26 | R26 | FMC_LPC_LA21_P | 20 |
| IO_L14N_VREF_15_R32 | R32 | FMC_LPC_LA27_N | 20 |
| IO_L14P_15_R31 | R31 | FMC_LPC_LA27_P | 20 |
| IO_L13N_SM14N_15_R27 | R27 | FMC_LPC_LA23_N | 20 |
| IO_L13P_SM14P_15_R28 | R28 | FMC_LPC_LA23_P | 20 |
| IO_L12N_SM13N_15_P26 | P26 | VAUX_CURR_N | 20 |
| IO_L12P_SM13P_15_P25 | P25 | VAUX_CURR_P | 20 |
| IO_L11N_SRCC_15_L30 | L30 | FMC_LPC_LA18_CC_N | 20 |
| IO_L11P_SRCC_15_L29 | L29 | FMC_LPC_LA18_CC_P | 20 |
| IO_L10N_MRCC_15_M33 | M33 | FMC_LPC_LA28_N | 20 |
| IO_L10P_MRCC_15_N33 | N33 | FMC_LPC_LA28_P | 20 |
| IO_L9N_MRCC_15_N29 | N29 | FMC_LPC_LA17_CC_N | 20 |
| IO_L9P_MRCC_15_N28 | N28 | FMC_LPC_LA17_CC_P | 20 |
| IO_L8N_SRCC_15_P32 | P32 | FMC_LPC_LA24_N | 20 |
| IO_L8P_SRCC_15_N32 | N32 | FMC_LPC_LA24_P | 20 |
| IO_L7N_SM12N_15_M28 | M28 | VAUX_VOLT_N | 20 |
| IO_L7P_SM12P_15_L28 | L28 | VAUX_VOLT_P | 20 |
| IO_L6N_SM11N_15_M32 | M32 | FMC_LPC_LA26_N | 20 |
| IO_L6P_SM11P_15_L33 | L33 | FMC_LPC_LA26_P | 20 |
| IO_L5N_SM10N_15_P27 | P27 | FMC_LPC_LA22_N | 20 |
| IO_L5P_SM10P_15_N27 | N27 | FMC_LPC_LA22_P | 20 |
| IO_L4N_VREF_15_P30 | P30 | FMC_LPC_LA25_N | 20 |
| IO_L4P_15_P31 | P31 | FMC_LPC_LA25_P | 20 |
| IO_L3N_SM9N_15_M27 | M27 | FMC_LPC_LA30_N | 20 |
| IO_L3P_SM9P_15_M26 | M26 | FMC_LPC_LA30_P | 20 |
| IO_L2N_SM8N_15_K31 | K31 | FMC_LPC_LA33_N | 20 |
| IO_L2P_SM8P_15_K32 | K32 | FMC_LPC_LA33_P | 20 |
| IO_L1N_15_M25 | M25 | FMC_LPC_LA32_N | 20 |
| IO_L1P_15_N25 | N25 | FMC_LPC_LA32_P | 20 |
| IO_L0N_15_L31 | L31 | FMC_LPC_LA31_N | 20 |
| IO_L0P_15_M31 | M31 | FMC_LPC_LA31_P | 20 |

VCC2V5_FPGA



VCCO_15_R30
VCCO_15_P33
VCCO_15_N26
VCCO_15_M29
VCCO_15_L32



Place above components near FPGA

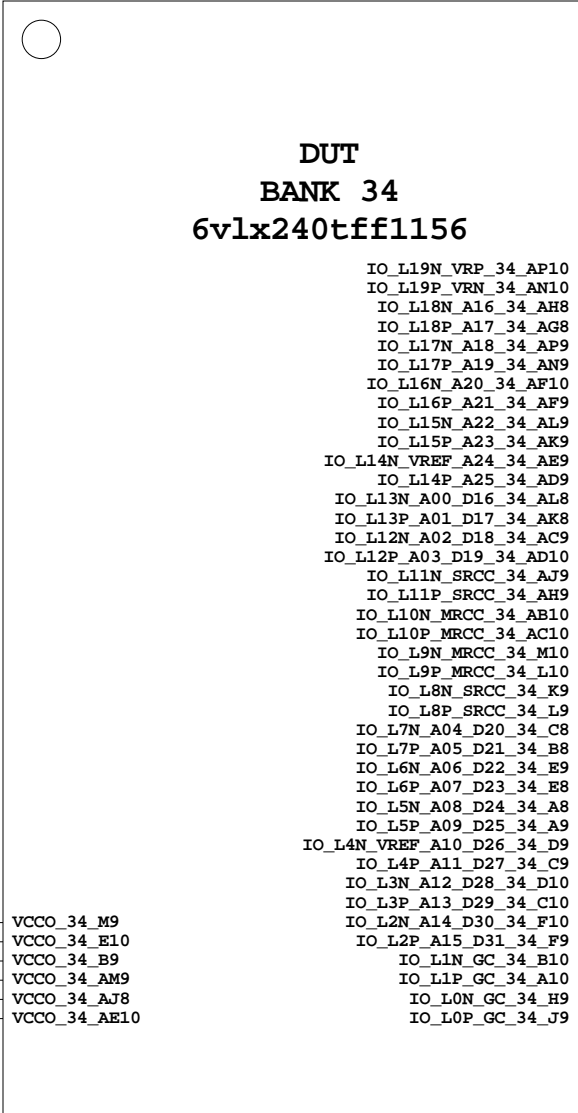
FPGA Banks 15, 16



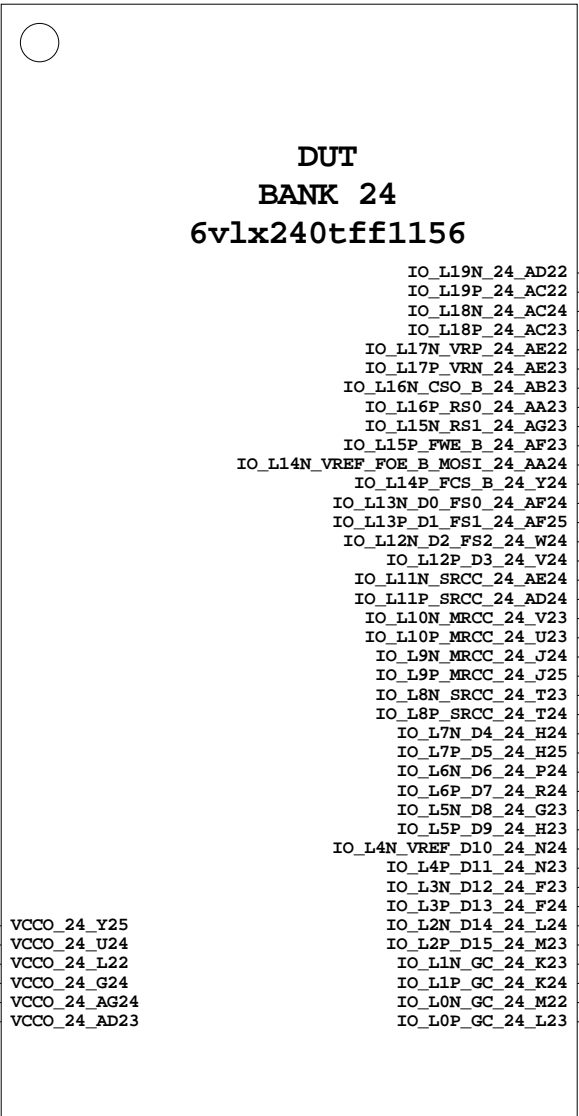
Title: FPGA Banks 15, 16
SCHEM, ROHS COMPLIANT
ML605

ASSY P/N: 0431540
PCB P/N: 1280479
SCH P/N: 0381311

Date: 9-17-2009_15:43 Ver: D
Sheet Size: B Rev: 04
Sheet 3 of 48 Drawn By BF



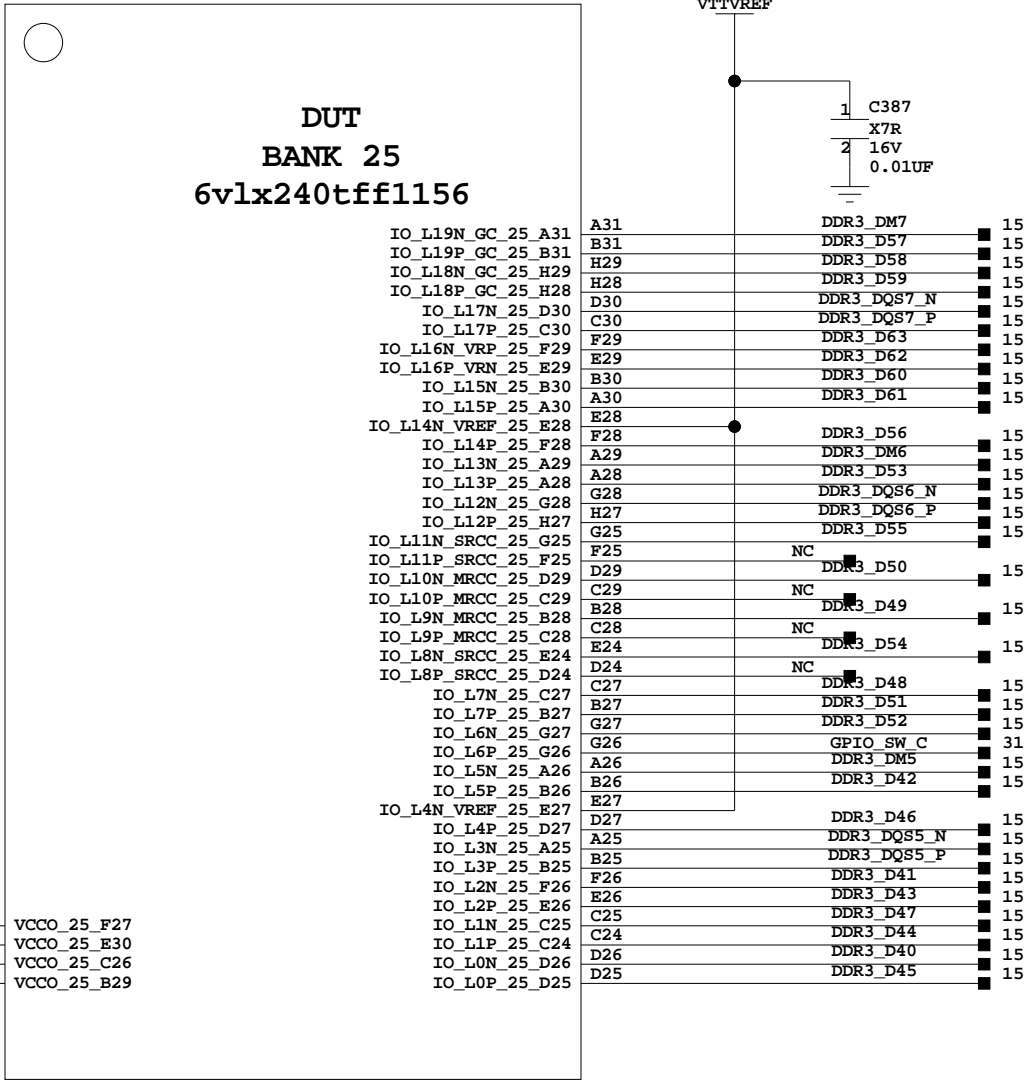
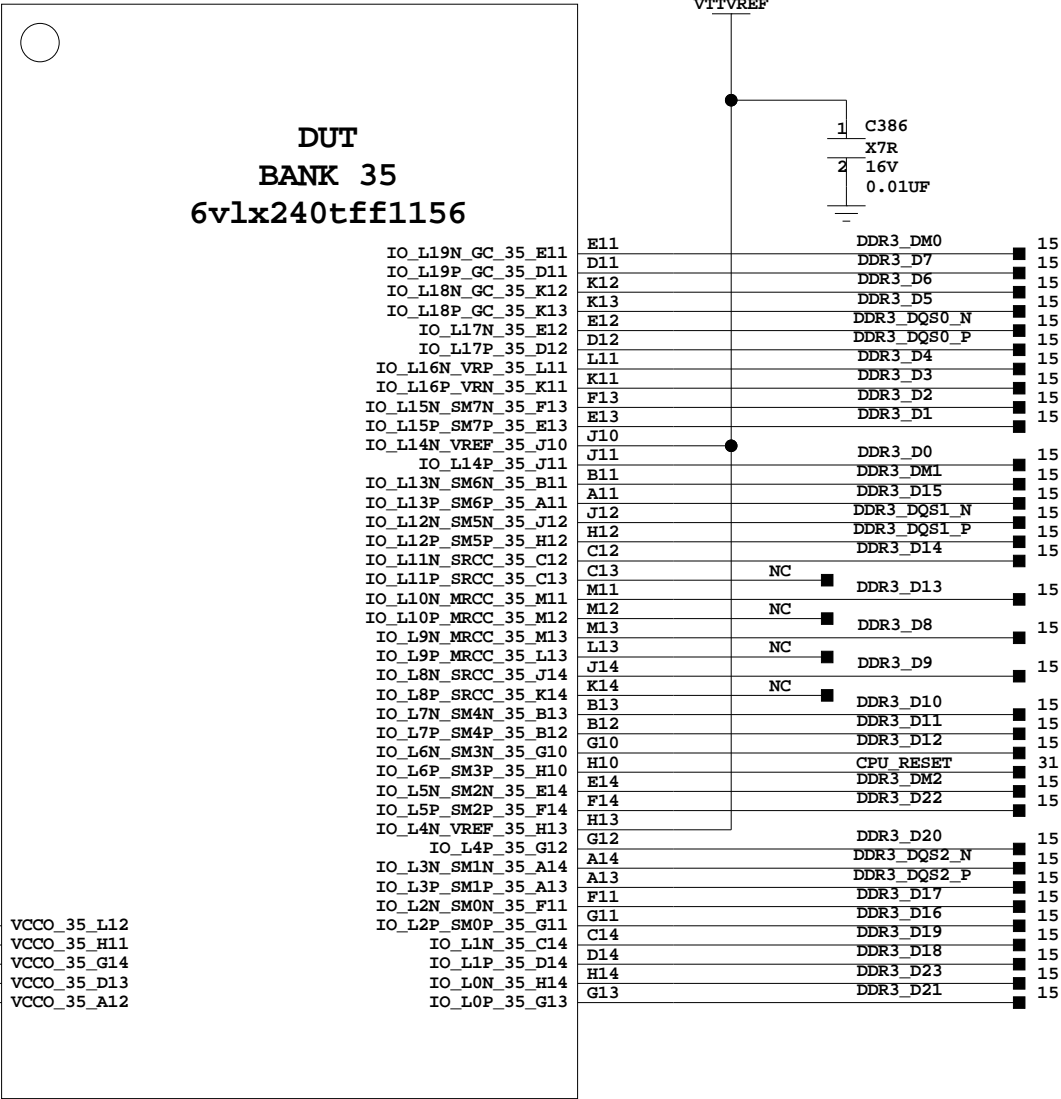
| | | |
|------|--------------------------|-------|
| AP10 | IIC_SDA_DVI | 28,29 |
| AN10 | IIC_SCL_DVI | 28,29 |
| AH8 | FLASH_A16 | 25,26 |
| AG8 | FLASH_A17 | 25,26 |
| AP9 | FLASH_A18 | 25,26 |
| AN9 | FLASH_A19 | 25,26 |
| AF10 | FLASH_A20 | 25,26 |
| AF9 | FLASH_A21 | 25,26 |
| AL9 | FLASH_A22 | 25,26 |
| AK9 | IIC_SCL_MAIN_LS | 32 |
| AE9 | IIC_SDA_MAIN_LS | 32 |
| AD9 | FMC_LPC_PRSNF_M2C | 20 |
| AL8 | FLASH_A0 | 25,26 |
| AK8 | FLASH_A1 | 25,26 |
| AC9 | FLASH_A2 | 25,26 |
| AD10 | FLASH_A3 | 25,26 |
| AJ9 | PMBUS_CTRL_LS | 32 |
| AH9 | PMBUS_ALERT_LS | 32 |
| AB10 | PMBUS_DATA_LS | 32 |
| AC10 | PMBUS_CLK_LS | 32 |
| M10 | SM_FAN_TACH | 39 |
| L10 | SM_FAN_PWM | 39 |
| K9 | DVI_GPIO1_FMC_C2M_PG_L32 | 13 |
| L9 | SYSACE_MPIRQ | 13 |
| C8 | FLASH_A4 | 25,26 |
| B8 | FLASH_A5 | 25,26 |
| E9 | FLASH_A6 | 25,26 |
| E8 | FLASH_A7 | 25,26 |
| A8 | FLASH_A8 | 25,26 |
| A9 | FLASH_A9 | 25,26 |
| D9 | FLASH_A10 | 25,26 |
| C9 | FLASH_A11 | 25,26 |
| D10 | FLASH_A12 | 25,26 |
| C10 | FLASH_A13 | 25,26 |
| F10 | FLASH_A14 | 25,26 |
| F9 | FLASH_A15 | 25,26 |
| B10 | FMC_LPC_CLK0_M2C_N | 20 |
| A10 | FMC_LPC_CLK0_M2C_P | 20 |
| H9 | SYSCLK_N | 30 |
| J9 | SYSCLK_P | 30 |




| | | |
|------|--------------------|-------|
| AD22 | PCIE_WAKE_B_LS | 32 |
| AC22 | GPIO_LED_0 | 31 |
| AC24 | GPIO_LED_1 | 31 |
| AC23 | PLATFLASH_L_B | 25 |
| AE22 | GPIO_LED_2 | 31 |
| AE23 | GPIO_LED_3 | 31 |
| AB23 | GPIO_LED_4 | 31 |
| AA23 | FLASH_A23 | 25,26 |
| AG23 | GPIO_LED_5 | 31 |
| AF23 | FPGA_FWE_B | 25,26 |
| AA24 | FPGA_FOE_B | 25,26 |
| Y24 | FPGA_FCS_B | 25 |
| AF24 | FLASH_D0 | 25,26 |
| AF25 | FLASH_D1 | 25,26 |
| W24 | FLASH_D2 | 25,26 |
| V24 | FLASH_D3 | 25,26 |
| AE24 | GPIO_LED_6 | 31 |
| AD24 | GPIO_LED_7 | 31 |
| V23 | SFP_LOS | 23 |
| U23 | USER_CLOCK | 30 |
| J24 | USB_1_TX | 33 |
| J25 | USB_1_RX | 33 |
| T23 | USB_1_RTS | 33 |
| T24 | USB_1_CTS | 33 |
| H24 | FLASH_D4 | 25,26 |
| H25 | FLASH_D5 | 25,26 |
| P24 | FLASH_D6 | 25,26 |
| R24 | FLASH_D7 | 25,26 |
| G23 | FLASH_D8 | 25,26 |
| H23 | FLASH_D9 | 25,26 |
| N24 | FLASH_D10 | 25,26 |
| N23 | FLASH_D11 | 25,26 |
| F23 | FLASH_D12 | 25,26 |
| F24 | FLASH_D13 | 25,26 |
| L24 | FLASH_D14 | 25,26 |
| M23 | FLASH_D15 | 25,26 |
| K23 | FMC_HPC_CLK0_M2C_N | 18 |
| K24 | FMC_HPC_CLK0_M2C_P | 18 |
| M22 | USER_SMA_CLOCK_N | 30 |
| L23 | USER_SMA_CLOCK_P | 30 |

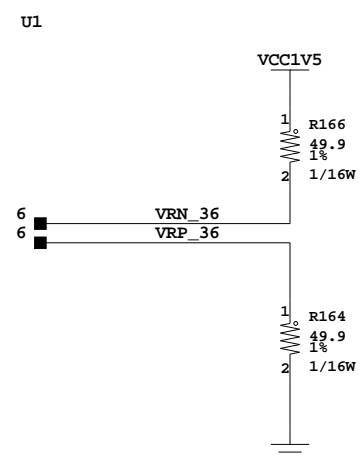
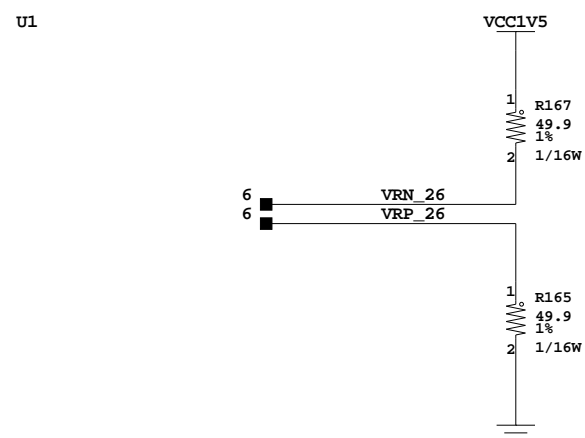
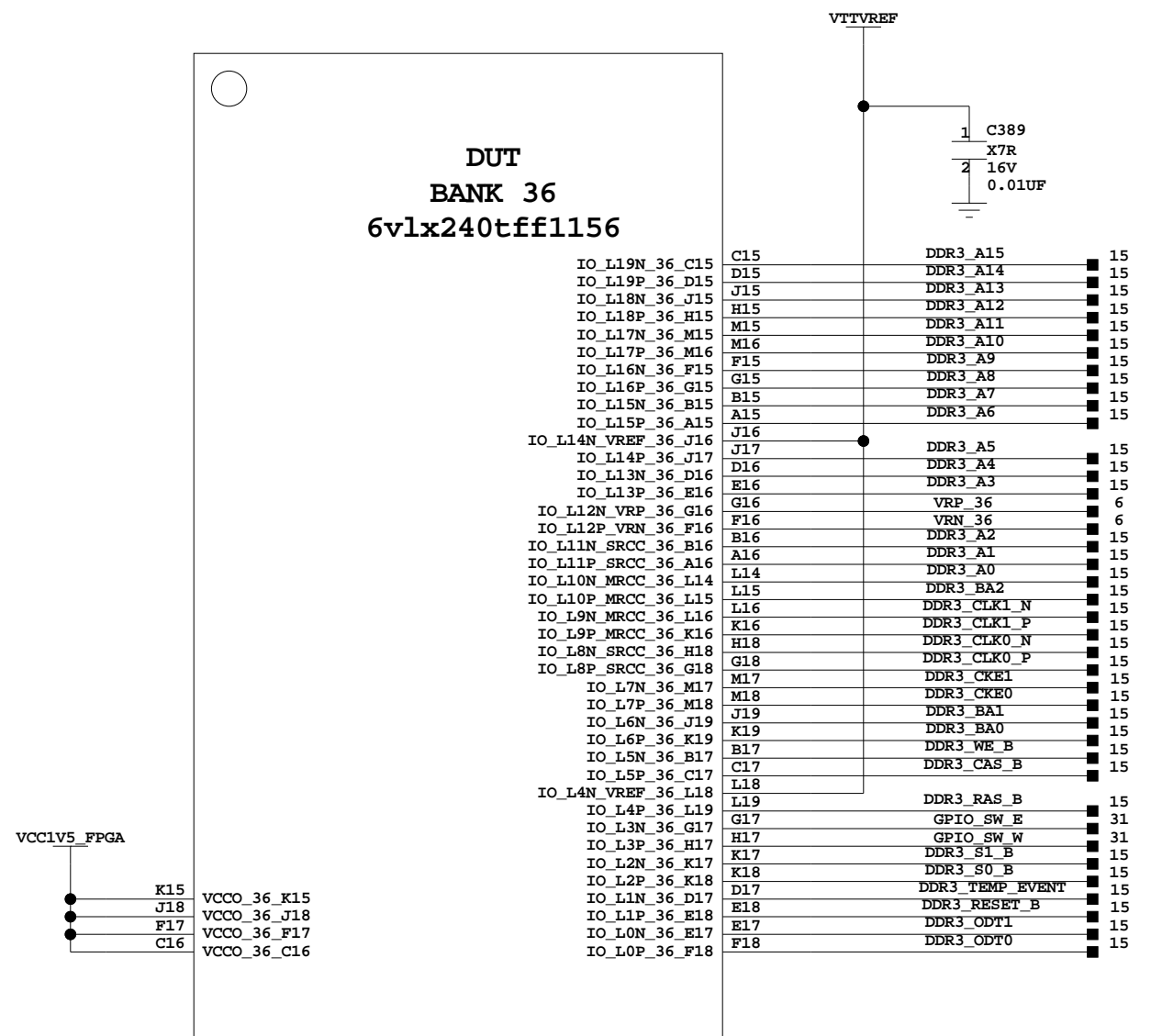
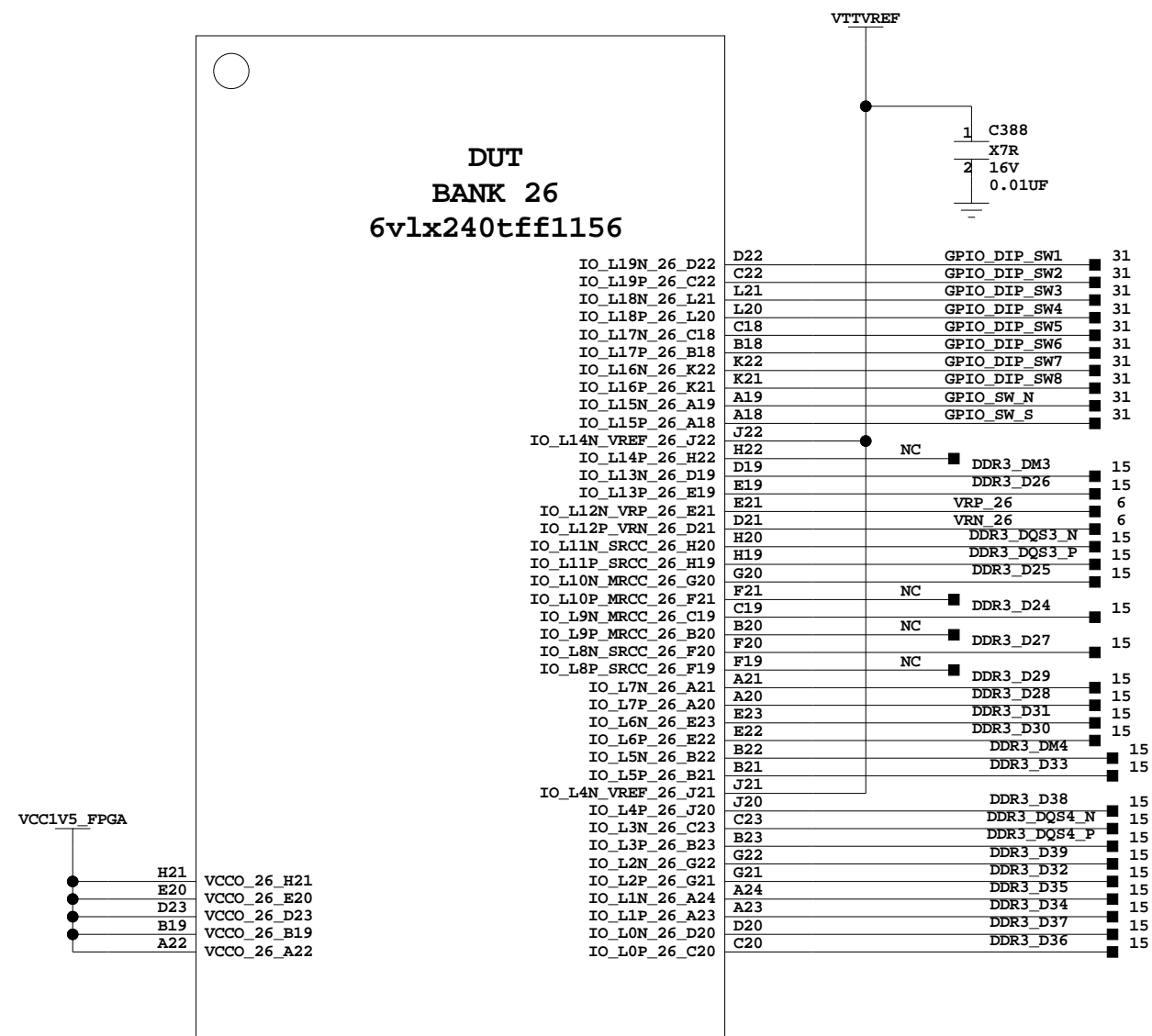
FPGA Banks 24, 34

| | | |
|--|-------------|---------|
| | | |
| Title: FPGA Banks 24, 34 SCHEM, ROHS COMPLIANT ML605 | | |
| ASSY P/N: 0431540 PCB P/N: 1280479 SCH P/N: 0381311 | | |
| Date: 9-17-2009_15:43 | Ver: D | |
| Sheet Size: B | | Rev: 04 |
| Sheet 4 of 48 | Drawn By BF | |



FPGA Banks 25, 35

| | | | |
|---|-----------------|---|----|
|  | | | |
| Title: | | FPGA Banks 25, 35 SCHEM, ROHS COMPLIANT ML605 | |
| | | ASSY P/N: 0431540 PCB P/N: 1280479 SCH P/N: 0381311 | |
| Date: | 9-17-2009_15:43 | Ver: | D |
| Sheet Size: | B | Rev: | 04 |
| Sheet | 5 of 48 | Drawn By | BF |



FPGA Banks 26, 36



| | | |
|---------------|-----------------------|-------------------|
| Title: | FPGA Banks 26, 36 | ASSY P/N: 0431540 |
| | SCHEM, ROHS COMPLIANT | PCB P/N: 1280479 |
| | ML605 | SCH P/N: 0381311 |

| | | | |
|---------------|-----------------|----------|----|
| Date: | 9-17-2009_15:43 | Ver: | D |
| Sheet Size: B | | Rev: | 04 |
| Sheet | 6 of 48 | Drawn By | BF |

LX240T ONLY

LX240T ONLY

DUT
BANK 12
6v1x240tff1156

| | | | |
|----------------------|------|-------------------|----|
| IO_L19N_12_AM31 | AM31 | FMC_HPC_HB03_N | 17 |
| IO_L19P_12_AL30 | AL30 | FMC_HPC_HB03_P | 17 |
| IO_L18N_12_AP33 | AP33 | FMC_HPC_HB02_N | 17 |
| IO_L18P_12_AP32 | AP32 | FMC_HPC_HB02_P | 17 |
| IO_L17N_12_AM32 | AM32 | FMC_HPC_HB01_N | 18 |
| IO_L17P_12_AN32 | AN32 | FMC_HPC_HB01_P | 18 |
| IO_L16N_12_AL33 | AL33 | FMC_HPC_HB04_N | 17 |
| IO_L16P_12_AM33 | AM33 | FMC_HPC_HB04_P | 17 |
| IO_L15N_12_AK31 | AK31 | FMC_HPC_HB19_N | 17 |
| IO_L15P_12_AL31 | AL31 | FMC_HPC_HB19_P | 17 |
| IO_L14N_VREF_12_AK32 | AK32 | FMC_HPC_HB08_N | 17 |
| IO_L14P_12_AK33 | AK33 | FMC_HPC_HB08_P | 17 |
| IO_L13N_12_AJ30 | AJ30 | FMC_HPC_HB11_N | 18 |
| IO_L13P_12_AJ29 | AJ29 | FMC_HPC_HB11_P | 18 |
| IO_L12N_VRP_12_AJ32 | AJ32 | FMC_HPC_HB12_N | 17 |
| IO_L12P_VRN_12_AJ31 | AJ31 | FMC_HPC_HB12_P | 17 |
| IO_L11N_SRCC_12_AE26 | AE26 | FMC_HPC_HB06_CC_N | 18 |
| IO_L11P_SRCC_12_AF26 | AF26 | FMC_HPC_HB06_CC_P | 18 |
| IO_L10N_MRCC_12_AG30 | AG30 | FMC_HPC_HB00_CC_N | 18 |
| IO_L10P_MRCC_12_AF30 | AF30 | FMC_HPC_HB00_CC_P | 18 |
| IO_L9N_MRCC_12_AG28 | AG28 | FMC_HPC_HB17_CC_N | 18 |
| IO_L9P_MRCC_12_AG27 | AG27 | FMC_HPC_HB17_CC_P | 18 |
| IO_L8N_SRCC_12_AN34 | AN34 | FMC_HPC_HB05_N | 17 |
| IO_L8P_SRCC_12_AN33 | AN33 | FMC_HPC_HB05_P | 17 |
| IO_L7N_12_AH30 | AH30 | FMC_HPC_HB16_N | 17 |
| IO_L7P_12_AH29 | AH29 | FMC_HPC_HB16_P | 17 |
| IO_L6N_12_AK34 | AK34 | FMC_HPC_HB09_N | 17 |
| IO_L6P_12_AL34 | AL34 | FMC_HPC_HB09_P | 17 |
| IO_L5N_12_AF29 | AF29 | FMC_HPC_HB10_N | 18 |
| IO_L5P_12_AF28 | AF28 | FMC_HPC_HB10_P | 18 |
| IO_L4N_VREF_12_AH34 | AH34 | FMC_HPC_HB07_N | 18 |
| IO_L4P_12_AJ34 | AJ34 | FMC_HPC_HB07_P | 18 |
| IO_L3N_12_AE29 | AE29 | FMC_HPC_HB15_N | 18 |
| IO_L3P_12_AE28 | AE28 | FMC_HPC_HB15_P | 18 |
| IO_L2N_12_AH32 | AH32 | FMC_HPC_HB13_N | 17 |
| IO_L2P_12_AH33 | AH33 | FMC_HPC_HB13_P | 17 |
| IO_L1N_12_AD27 | AD27 | FMC_HPC_HB14_N | 18 |
| IO_L1P_12_AE27 | AE27 | FMC_HPC_HB14_P | 18 |
| IO_L0N_12_AD26 | AD26 | FMC_HPC_HB18_N | 18 |
| IO_L0P_12_AD25 | AD25 | FMC_HPC_HB18_P | 18 |

| | | | |
|-------|---------------|------|--------------|
| 14,18 | FMC_VIO_B_M2C | AL32 | VCCO_12_AL32 |
| | | AH31 | VCCO_12_AH31 |
| | | AG34 | VCCO_12_AG34 |
| | | AF27 | VCCO_12_AF27 |

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DUT
BANK 13
6v1x240tff1156

| | | | |
|----------------------|------|-----------------------|----|
| IO_L19N_13_AC25 | AC25 | FMC_HPC_HA02_N | 18 |
| IO_L19P_13_AB25 | AB25 | FMC_HPC_HA02_P | 18 |
| IO_L18N_13_AF31 | AF31 | FMC_HPC_HA08_N | 17 |
| IO_L18P_13_AG31 | AG31 | FMC_HPC_HA08_P | 17 |
| IO_L17N_13_AB26 | AB26 | FMC_HPC_HA07_N | 18 |
| IO_L17P_13_AA26 | AA26 | FMC_HPC_HA07_P | 18 |
| IO_L16N_13_AG32 | AG32 | FMC_HPC_HA11_N | 18 |
| IO_L16P_13_AG33 | AG33 | FMC_HPC_HA11_P | 18 |
| IO_L15N_13_AC27 | AC27 | FMC_HPC_HA05_N | 17 |
| IO_L15P_13_AB27 | AB27 | FMC_HPC_HA05_P | 17 |
| IO_L14N_VREF_13_AE32 | AE32 | FMC_HPC_HA12_N | 17 |
| IO_L14P_13_AD32 | AD32 | FMC_HPC_HA12_P | 17 |
| IO_L13N_13_AC28 | AC28 | FMC_HPC_HA04_N | 17 |
| IO_L13P_13_AB28 | AB28 | FMC_HPC_HA04_P | 17 |
| IO_L12N_VRP_13_AC32 | AC32 | FMC_HPC_HA15_N | 17 |
| IO_L12P_VRN_13_AB32 | AB32 | FMC_HPC_HA15_P | 17 |
| IO_L11N_SRCC_13_AC29 | AC29 | FMC_HPC_HA01_CC_N | 17 |
| IO_L11P_SRCC_13_AD29 | AD29 | FMC_HPC_HA01_CC_P | 17 |
| IO_L10N_MRCC_13_AF33 | AF33 | FMC_HPC_HA00_CC_N | 17 |
| IO_L10P_MRCC_13_AE33 | AE33 | FMC_HPC_HA00_CC_P | 17 |
| IO_L9N_MRCC_13_AC30 | AC30 | FMC_HPC_CLK2_M2C_IO_N | 22 |
| IO_L9P_MRCC_13_AD30 | AD30 | FMC_HPC_CLK2_M2C_IO_P | 22 |
| IO_L8N_SRCC_13_AF34 | AF34 | FMC_HPC_CLK3_M2C_IO_N | 22 |
| IO_L8P_SRCC_13_AE34 | AE34 | FMC_HPC_CLK3_M2C_IO_P | 22 |
| IO_L7N_13_AA29 | AA29 | FMC_HPC_HA06_N | 18 |
| IO_L7P_13_AA28 | AA28 | FMC_HPC_HA06_P | 18 |
| IO_L6N_13_Y26 | Y26 | FMC_HPC_HA03_N | 18 |
| IO_L6P_13_AA25 | AA25 | FMC_HPC_HA03_P | 18 |
| IO_L5N_13_AD31 | AD31 | FMC_HPC_HA13_N | 17 |
| IO_L5P_13_AE31 | AE31 | FMC_HPC_HA13_P | 17 |
| IO_L4N_VREF_13_AB33 | AB33 | FMC_HPC_HA16_N | 17 |
| IO_L4P_13_AC33 | AC33 | FMC_HPC_HA16_P | 17 |
| IO_L3N_13_AB31 | AB31 | FMC_HPC_HA09_N | 17 |
| IO_L3P_13_AB30 | AB30 | FMC_HPC_HA09_P | 17 |
| IO_L2N_13_AC34 | AC34 | FMC_HPC_HA10_N | 18 |
| IO_L2P_13_AD34 | AD34 | FMC_HPC_HA10_P | 18 |
| IO_L1N_13_AA31 | AA31 | FMC_HPC_HA14_N | 18 |
| IO_L1P_13_AA30 | AA30 | FMC_HPC_HA14_P | 18 |
| IO_L0N_13_AA33 | AA33 | IIC_SDA_SFP | 23 |
| IO_L0P_13_AA34 | AA34 | IIC_SCL_SFP | 23 |

| | | |
|-------------|------|--------------|
| VCC2V5_FPGA | AE30 | VCCO_13_AE30 |
| | AD33 | VCCO_13_AD33 |
| | AC26 | VCCO_13_AC26 |
| | AB29 | VCCO_13_AB29 |
| | AA32 | VCCO_13_AA32 |

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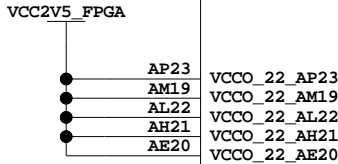
FPGA Banks 12, 13

| | | | |
|---|-----------------|---|---|
|  | | | |
| Title: | | FPGA Banks 12, 13 SCHEM, ROHS COMPLIANT ML605 | ASSY P/N: 0431540 PCB P/N: 1280479 SCH P/N: 0381311 |
| Date: | 9-17-2009_15:43 | Ver: | D |
| Sheet Size: | B | Rev: | 04 |
| Sheet | 7 of 48 | Drawn By | BF |

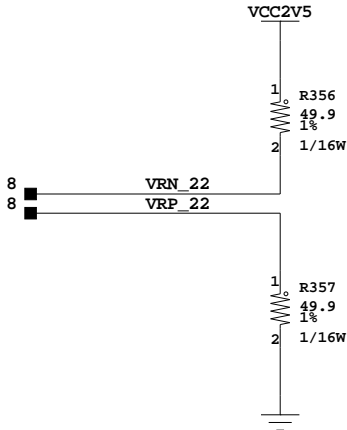
LX240T ONLY

DUT
BANK 22
6vlx240tff1156

| | | | |
|-----------------|------|--------------------|----|
| IO_L19N_22 | AN23 | FMC_HPC_LA16_N | 17 |
| IO_L19P_22 | AP22 | FMC_HPC_LA16_P | 17 |
| IO_L18N_22 | AG21 | FMC_HPC_LA06_N | 16 |
| IO_L18P_22 | AG20 | FMC_HPC_LA06_P | 16 |
| IO_L17N_22 | AN22 | FMC_HPC_LA11_N | 18 |
| IO_L17P_22 | AM22 | FMC_HPC_LA11_P | 18 |
| IO_L16N_22 | AJ21 | FMC_HPC_LA07_N | 18 |
| IO_L16P_22 | AK21 | FMC_HPC_LA07_P | 18 |
| IO_L15N_22 | AL23 | FMC_HPC_LA15_N | 18 |
| IO_L15P_22 | AM23 | FMC_HPC_LA15_P | 18 |
| IO_L14N_VREF_22 | AD19 | FMC_HPC_LA03_N | 17 |
| IO_L14P_22 | AC19 | FMC_HPC_LA03_P | 17 |
| IO_L13N_22 | AL21 | FMC_HPC_LA12_N | 17 |
| IO_L13P_22 | AM21 | FMC_HPC_LA12_P | 17 |
| IO_L12N_VRP_22 | AH20 | VRP_22 | 8 |
| IO_L12P_VRN_22 | AJ20 | VRN_22 | 8 |
| IO_L11N_SRCC_22 | AF21 | FMC_HPC_LA00_CC_N | 17 |
| IO_L11P_SRCC_22 | AF20 | FMC_HPC_LA00_CC_P | 17 |
| IO_L10N_MRCC_22 | AL19 | FMC_HPC_LA01_CC_N | 16 |
| IO_L10P_MRCC_22 | AK19 | FMC_HPC_LA01_CC_P | 16 |
| IO_L9N_MRCC_22 | AP21 | FMC_HPC_CLK1_M2C_N | 17 |
| IO_L9P_MRCC_22 | AP20 | FMC_HPC_CLK1_M2C_P | 17 |
| IO_L8N_SRCC_22 | AE19 | FMC_HPC_LA04_N | 18 |
| IO_L8P_SRCC_22 | AF19 | FMC_HPC_LA04_P | 18 |
| IO_L7N_22 | AL20 | FMC_HPC_LA10_N | 16 |
| IO_L7P_22 | AM20 | FMC_HPC_LA10_P | 16 |
| IO_L6N_22 | AD20 | FMC_HPC_LA02_N | 18 |
| IO_L6P_22 | AC20 | FMC_HPC_LA02_P | 18 |
| IO_L5N_22 | AN20 | FMC_HPC_LA14_N | 16 |
| IO_L5P_22 | AN19 | FMC_HPC_LA14_P | 16 |
| IO_L4N_VREF_22 | AJ22 | FMC_HPC_LA08_N | 17 |
| IO_L4P_22 | AK22 | FMC_HPC_LA08_P | 17 |
| IO_L3N_22 | AN18 | FMC_HPC_LA13_N | 16 |
| IO_L3P_22 | AP19 | FMC_HPC_LA13_P | 16 |
| IO_L2N_22 | AH22 | FMC_HPC_LA05_N | 16 |
| IO_L2P_22 | AG22 | FMC_HPC_LA05_P | 16 |
| IO_L1N_22 | AL18 | FMC_HPC_LA09_N | 16 |
| IO_L1P_22 | AM18 | FMC_HPC_LA09_P | 16 |
| IO_L0N_22 | AD21 | GPIO_LED_W | 31 |
| IO_L0P_22 | AE21 | GPIO_LED_E | 31 |



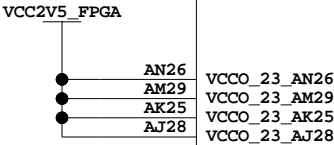
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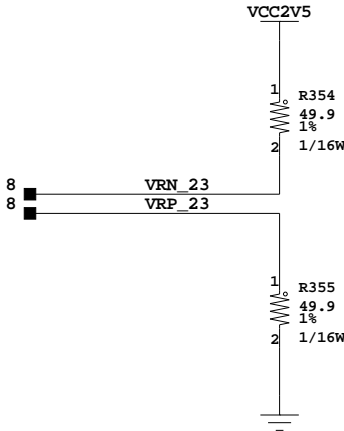
LX240T ONLY

DUT
BANK 23
6vlx240tff1156

| | | | |
|-----------------|------|---------------------|----|
| IO_L19N_23 | AP24 | GPIO_LED_C | 31 |
| IO_L19P_23 | AP25 | FMC_HPC_PRSNT_M2C_L | 18 |
| IO_L18N_23 | AL24 | FMC_HPC_LA20_N | 17 |
| IO_L18P_23 | AK23 | FMC_HPC_LA20_P | 17 |
| IO_L17N_23 | AN24 | FMC_HPC_LA19_N | 18 |
| IO_L17P_23 | AN25 | FMC_HPC_LA19_P | 18 |
| IO_L16N_23 | AL25 | FMC_HPC_LA26_N | 16 |
| IO_L16P_23 | AM25 | FMC_HPC_LA26_P | 16 |
| IO_L15N_23 | AP26 | FMC_HPC_LA22_N | 17 |
| IO_L15P_23 | AP27 | FMC_HPC_LA22_P | 17 |
| IO_L14N_VREF_23 | AK24 | FMC_HPC_LA30_N | 18 |
| IO_L14P_23 | AJ24 | FMC_HPC_LA30_P | 18 |
| IO_L13N_23 | AM26 | FMC_HPC_LA23_N | 16 |
| IO_L13P_23 | AL26 | FMC_HPC_LA23_P | 16 |
| IO_L12N_VRP_23 | AJ26 | VRP_23 | 8 |
| IO_L12P_VRN_23 | AK26 | VRN_23 | 8 |
| IO_L11N_SRCC_23 | AH24 | FMC_HPC_LA33_N | 17 |
| IO_L11P_SRCC_23 | AH23 | FMC_HPC_LA33_P | 17 |
| IO_L10N_MRCC_23 | AJ27 | FMC_HPC_LA28_N | 18 |
| IO_L10P_MRCC_23 | AK27 | FMC_HPC_LA28_P | 18 |
| IO_L9P_MRCC_23 | AM27 | FMC_HPC_LA17_CC_N | 16 |
| IO_L9N_MRCC_23 | AN27 | FMC_HPC_LA17_CC_P | 16 |
| IO_L8N_SRCC_23 | AJ25 | FMC_HPC_LA18_CC_N | 16 |
| IO_L8P_SRCC_23 | AH25 | FMC_HPC_LA18_CC_P | 16 |
| IO_L7N_23 | AM28 | FMC_HPC_LA25_N | 17 |
| IO_L7P_23 | AN28 | FMC_HPC_LA25_P | 17 |
| IO_L6N_23 | AK28 | FMC_HPC_LA29_N | 17 |
| IO_L6P_23 | AL28 | FMC_HPC_LA29_P | 17 |
| IO_L5N_23 | AP29 | FMC_HPC_LA21_N | 18 |
| IO_L5P_23 | AN29 | FMC_HPC_LA21_P | 18 |
| IO_L4N_VREF_23 | AK29 | FMC_HPC_LA31_N | 17 |
| IO_L4P_23 | AL29 | FMC_HPC_LA31_P | 17 |
| IO_L3N_23 | AP31 | FMC_HPC_LA27_N | 16 |
| IO_L3P_23 | AP30 | FMC_HPC_LA27_P | 16 |
| IO_L2N_23 | AG26 | FMC_HPC_LA32_N | 18 |
| IO_L2P_23 | AG25 | FMC_HPC_LA32_P | 18 |
| IO_L1N_23 | AM30 | FMC_HPC_LA24_N | 18 |
| IO_L1P_23 | AN30 | FMC_HPC_LA24_P | 18 |
| IO_L0N_23 | AH28 | GPIO_LED_S | 31 |
| IO_L0P_23 | AH27 | GPIO_LED_N | 31 |



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FPGA Banks 22, 23

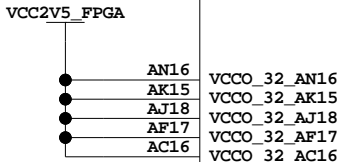


| | | |
|--|-------------|---|
| Title: FPGA Banks 22, 23 SCHEM, ROHS COMPLIANT ML605 | | ASSY P/N: 0431540 PCB P/N: 1280479 SCH P/N: 0381311 |
| Date: 9-17-2009_15:43 | Ver: D | |
| Sheet Size: B | Rev: 04 | |
| Sheet 8 of 48 | Drawn By BF | |

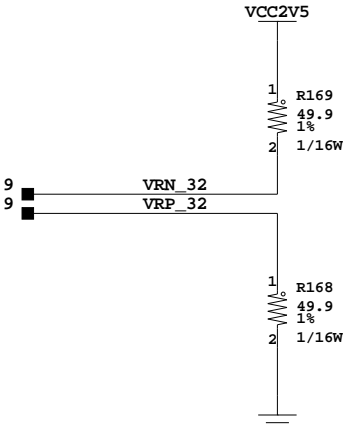
LX240T ONLY

DUT
BANK 32
6vlx240tfff1156

| | | | |
|----------------------|------|------------------|----|
| IO_L19N_32_AK16 | AK16 | DVI_D11 | 29 |
| IO_L19P_32_AL16 | AL16 | DVI_D10 | 29 |
| IO_L18N_32_AF18 | AF18 | DVI_D9 | 29 |
| IO_L18P_32_AE18 | AE18 | DVI_D8 | 29 |
| IO_L17N_32_AK17 | AK17 | DVI_D7 | 29 |
| IO_L17P_32_AK18 | AK18 | DVI_D6 | 29 |
| IO_L16N_32_AE17 | AE17 | DVI_D5 | 29 |
| IO_L16P_32_AD17 | AD17 | DVI_D4 | 29 |
| IO_L15N_32_AM16 | AM16 | DVI_D3 | 29 |
| IO_L15P_32_AM17 | AM17 | DVI_D2 | 29 |
| IO_L14N_VREF_32_AH19 | AH19 | DVI_D1 | 29 |
| IO_L14P_32_AJ19 | AJ19 | DVI_D0 | 29 |
| IO_L13N_32_AP17 | AP17 | DVI_RESET_B_LS | 32 |
| IO_L13P_32_AN17 | AN17 | DVI_H | 29 |
| IO_L12N_VRP_32_AG18 | AG18 | VRP_32 | 9 |
| IO_L12P_VRN_32_AH18 | AH18 | VRN_32 | 9 |
| IO_L11N_SRCC_32_AC17 | AC17 | DVI_XCLK_N | 29 |
| IO_L11P_SRCC_32_AC18 | AC18 | DVI_XCLK_P | 29 |
| IO_L10N_MRCC_32_AD16 | AD16 | DVI_DE | 29 |
| IO_L10P_MRCC_32_AE16 | AE16 | CLK_33MHZ_SYSACE | 13 |
| IO_L9N_MRCC_32_AD15 | AD15 | DVI_V | 29 |
| IO_L9P_MRCC_32_AC15 | AC15 | SYSACE_MPA00 | 13 |
| IO_L8N_SRCC_32_AG17 | AG17 | SYSACE_MPA02 | 13 |
| IO_L8P_SRCC_32_AH17 | AH17 | SYSACE_MPA03 | 13 |
| IO_L7N_32_AP15 | AP15 | SYSACE_MPA01 | 13 |
| IO_L7P_32_AP16 | AP16 | SYSACE_D3 | 13 |
| IO_L6N_32_AJ16 | AJ16 | SYSACE_D2 | 13 |
| IO_L6P_32_AJ17 | AJ17 | SYSACE_D1 | 13 |
| IO_L5N_32_AM15 | AM15 | SYSACE_D0 | 13 |
| IO_L5P_32_AN15 | AN15 | SYSACE_D7 | 13 |
| IO_L4N_VREF_32_AF16 | AF16 | SYSACE_D6 | 13 |
| IO_L4P_32_AG16 | AG16 | SYSACE_D4 | 13 |
| IO_L3N_32_AL14 | AL14 | SYSACE_MPWE | 13 |
| IO_L3P_32_AL15 | AL15 | SYSACE_MPOE | 13 |
| IO_L2N_32_AH15 | AH15 | SYSACE_D5 | 13 |
| IO_L2P_32_AJ15 | AJ15 | SYSACE_MPBRDY | 13 |
| IO_L1N_32_AJ14 | AJ14 | SYSACE_MPCE | 13 |
| IO_L1P_32_AK14 | AK14 | SYSACE_MPA06 | 13 |
| IO_L0N_32_AF15 | AF15 | SYSACE_MPA05 | 13 |
| IO_L0P_32_AG15 | AG15 | SYSACE_MPA04 | 13 |



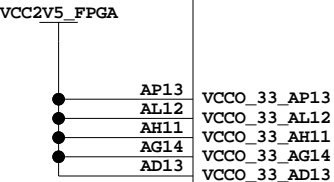
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LX240T ONLY


DUT
BANK 33
6vlx240tfff1156

| | | | |
|----------------------|------|---------------------|----|
| IO_L19N_33_AN14 | AN14 | PHY_MDIO | 24 |
| IO_L19P_33_AP14 | AP14 | PHY_MDC | 24 |
| IO_L18N_33_AH14 | AH14 | PHY_INT | 24 |
| IO_L18P_33_AH13 | AH13 | PHY_RESET | 24 |
| IO_L17N_33_AL13 | AL13 | PHY_CRS | 24 |
| IO_L17P_33_AK13 | AK13 | PHY_COL | 24 |
| IO_L16N_33_AH12 | AH12 | PHY_TXC_GTXCLK | 24 |
| IO_L16P_33_AG12 | AG12 | PHY_RXER | 24 |
| IO_L15N_33_AM13 | AM13 | PHY_RXCTL_RXDV | 24 |
| IO_L15P_33_AN13 | AN13 | PHY_RXD0 | 24 |
| IO_L14N_VREF_33_AF14 | AF14 | PHY_RXD1 | 24 |
| IO_L14P_33_AE14 | AE14 | PHY_RXD2 | 24 |
| IO_L13N_33_AN12 | AN12 | PHY_RXD3 | 24 |
| IO_L13P_33_AM12 | AM12 | PHY_RXD4 | 24 |
| IO_L12N_VRP_33_AG13 | AG13 | FMC_LPC_IIC_SDA_LS | 32 |
| IO_L12P_VRN_33_AF13 | AF13 | FMC_LPC_IIC_SCL_LS | 32 |
| IO_L11N_SRCC_33_AP12 | AP12 | SFP_TX_DISABLE_FPGA | 23 |
| IO_L11P_SRCC_33_AP11 | AP11 | PHY_RXCLK | 24 |
| IO_L10N_MRCC_33_AD11 | AD11 | PHY_RXD5 | 24 |
| IO_L10P_MRCC_33_AD12 | AD12 | PHY_TXCLK | 24 |
| IO_L9N_MRCC_33_AC12 | AC12 | PHY_RXD6 | 24 |
| IO_L9P_MRCC_33_AC13 | AC13 | PHY_RXD7 | 24 |
| IO_L8N_SRCC_33_AH10 | AH10 | PHY_TXER | 24 |
| IO_L8P_SRCC_33_AJ10 | AJ10 | PHY_TXCTL_TXEN | 24 |
| IO_L7N_33_AM11 | AM11 | PHY_TXD0 | 24 |
| IO_L7P_33_AL11 | AL11 | PHY_TXD1 | 24 |
| IO_L6N_33_AG10 | AG10 | PHY_TXD2 | 24 |
| IO_L6P_33_AG11 | AG11 | PHY_TXD3 | 24 |
| IO_L5N_33_AL10 | AL10 | PHY_TXD4 | 24 |
| IO_L5P_33_AM10 | AM10 | PHY_TXD5 | 24 |
| IO_L4N_VREF_33_AE11 | AE11 | PHY_TXD6 | 24 |
| IO_L4P_33_AF11 | AF11 | PHY_TXD7 | 24 |
| IO_L3P_33_AJ12 | AJ12 | P30_CS_SEL | 25 |
| IO_L3P_33_AK12 | AK12 | LCD_E_LS | 32 |
| IO_L2N_33_AC14 | AC14 | LCD_RW_LS | 32 |
| IO_L2P_33_AD14 | AD14 | LCD_DB4_LS | 32 |
| IO_L1N_33_AK11 | AK11 | LCD_DB5_LS | 32 |
| IO_L1P_33_AJ11 | AJ11 | LCD_DB6_LS | 32 |
| IO_L0N_33_AE12 | AE12 | LCD_DB7_LS | 32 |
| IO_L0P_33_AE13 | AE13 | PCIE_PERST_B_LS | 32 |

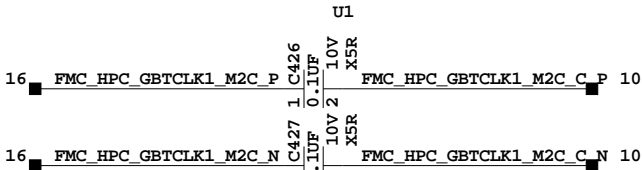
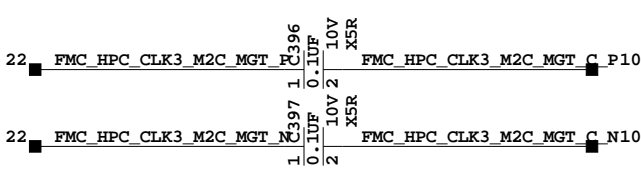
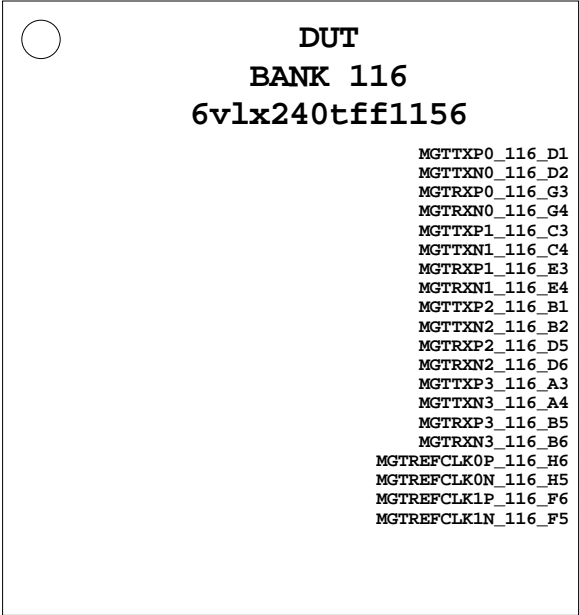
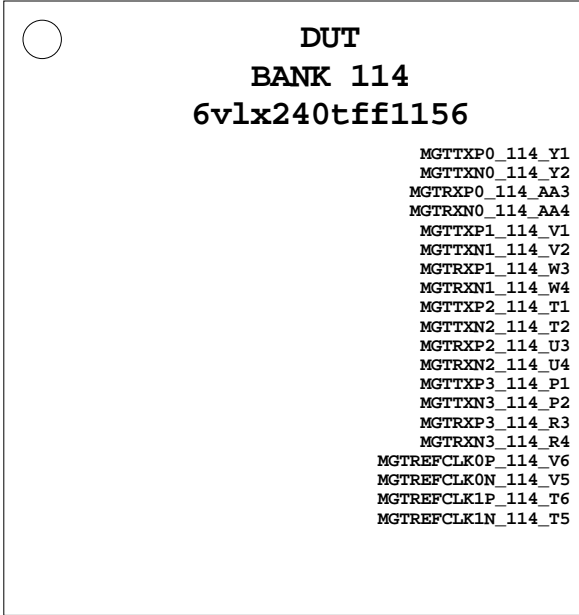
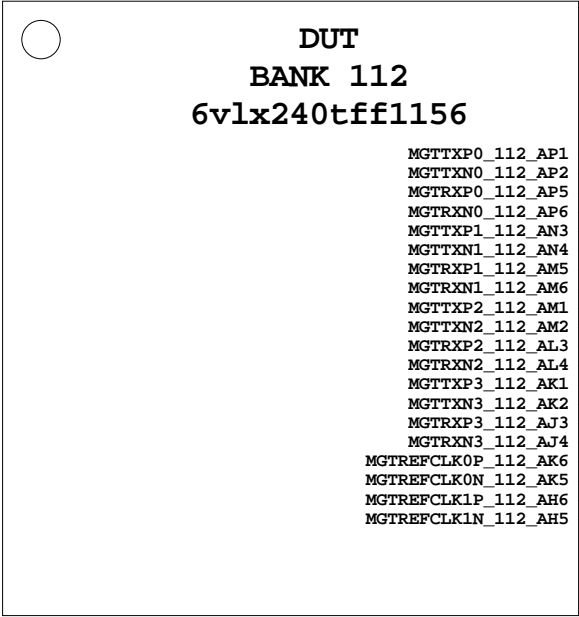


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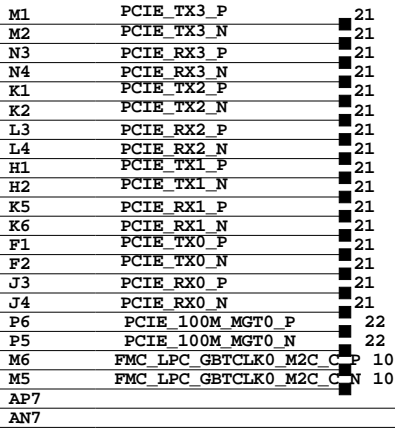
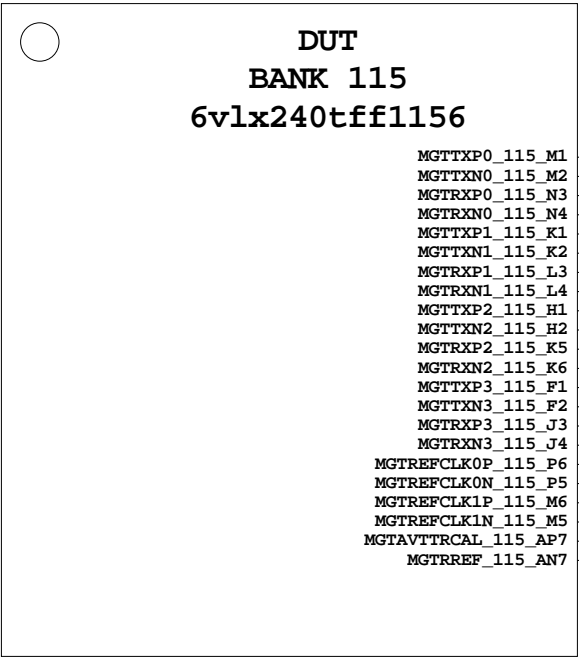
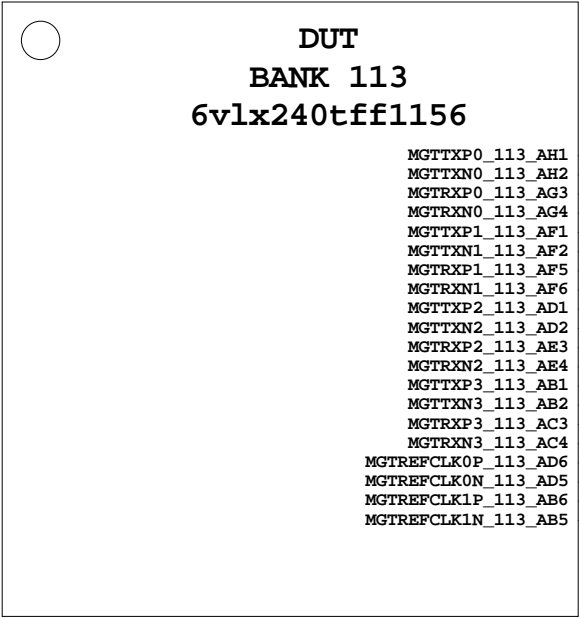
FPGA Banks 32, 33

| | | |
|---|---|---|
|  | | |
| Title: | FPGA Banks 32, 33 SCHEM, ROHS COMPLIANT ML605 | ASSY P/N: 0431540 PCB P/N: 1280479 SCH P/N: 0381311 |
| Date: | 9-17-2009_15:42 | Ver: D |
| Sheet Size: | B | Rev: 04 |
| Sheet | 9 of 48 | Drawn By BF |

LX240T ONLY



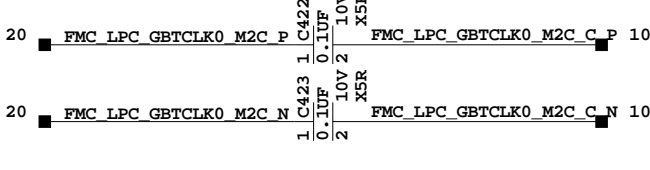
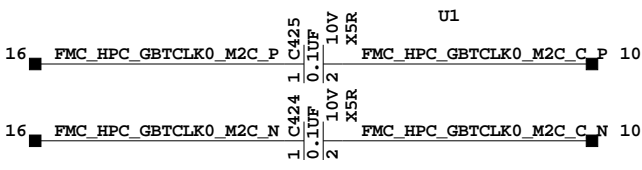
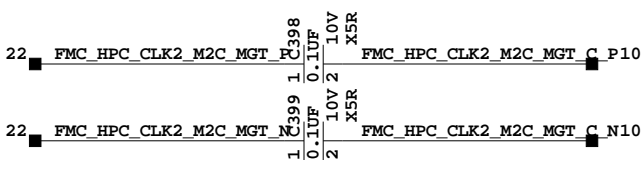
LX240T ONLY

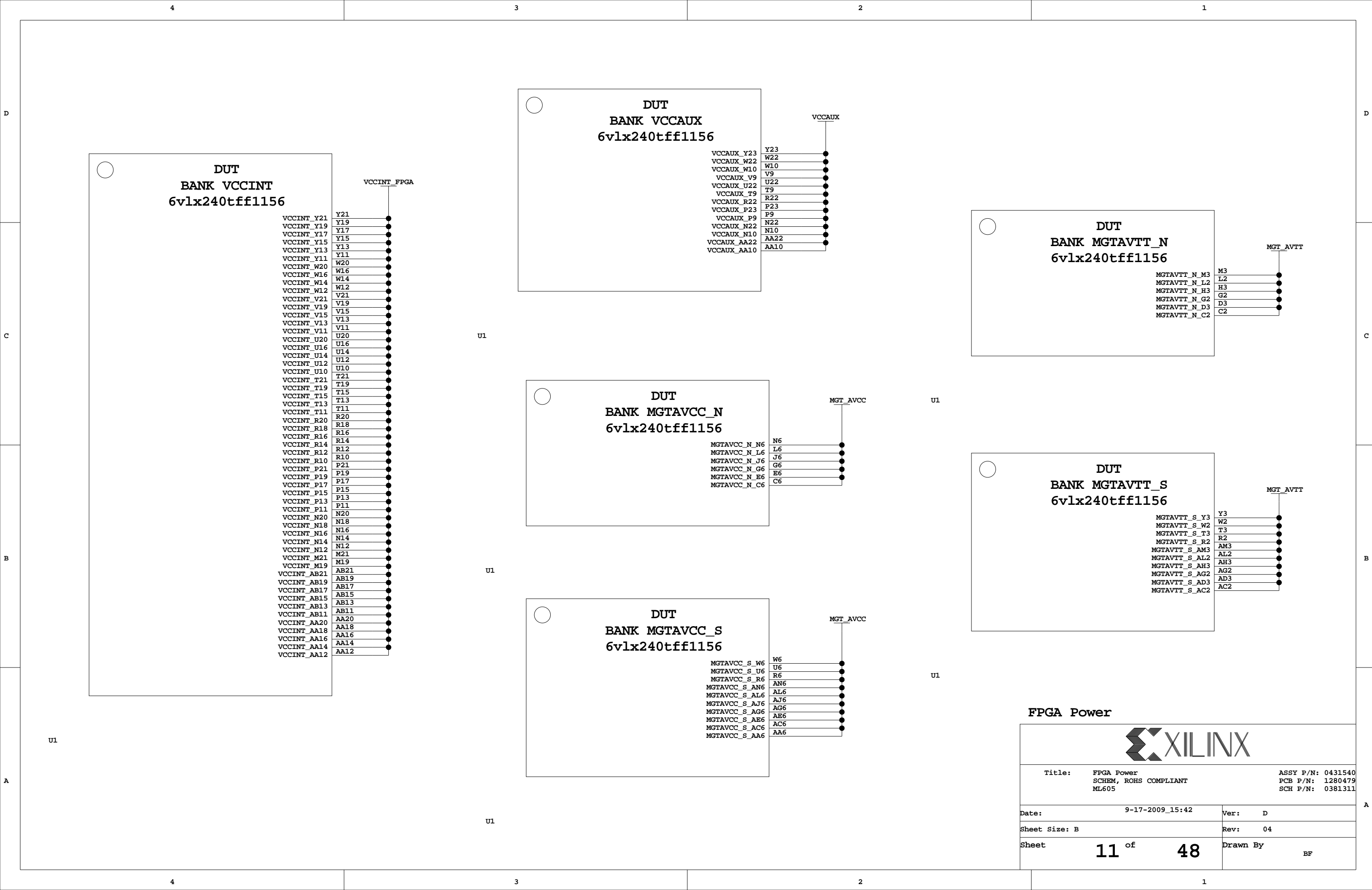


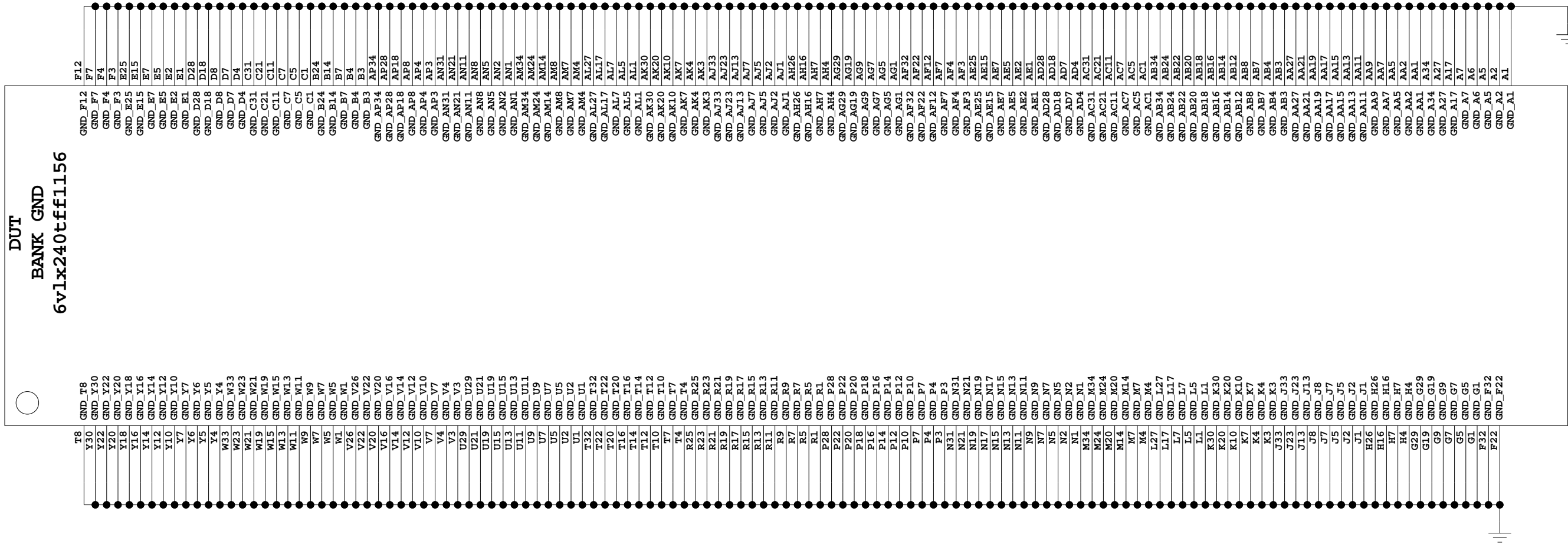
FPGA MGT Banks



| | | | |
|---|-------------|---|--|
| Title: FPGA MGT Banks SCHEM, ROHS COMPLIANT ML605 | | ASSY P/N: 0431540 PCB P/N: 1280479 SCH P/N: 0381311 | |
| Date: 9-17-2009_15:42 | Ver: D | | |
| Sheet Size: B | Rev: 04 | | |
| Sheet 10 of 48 | Drawn By BF | | |







FPGA GND

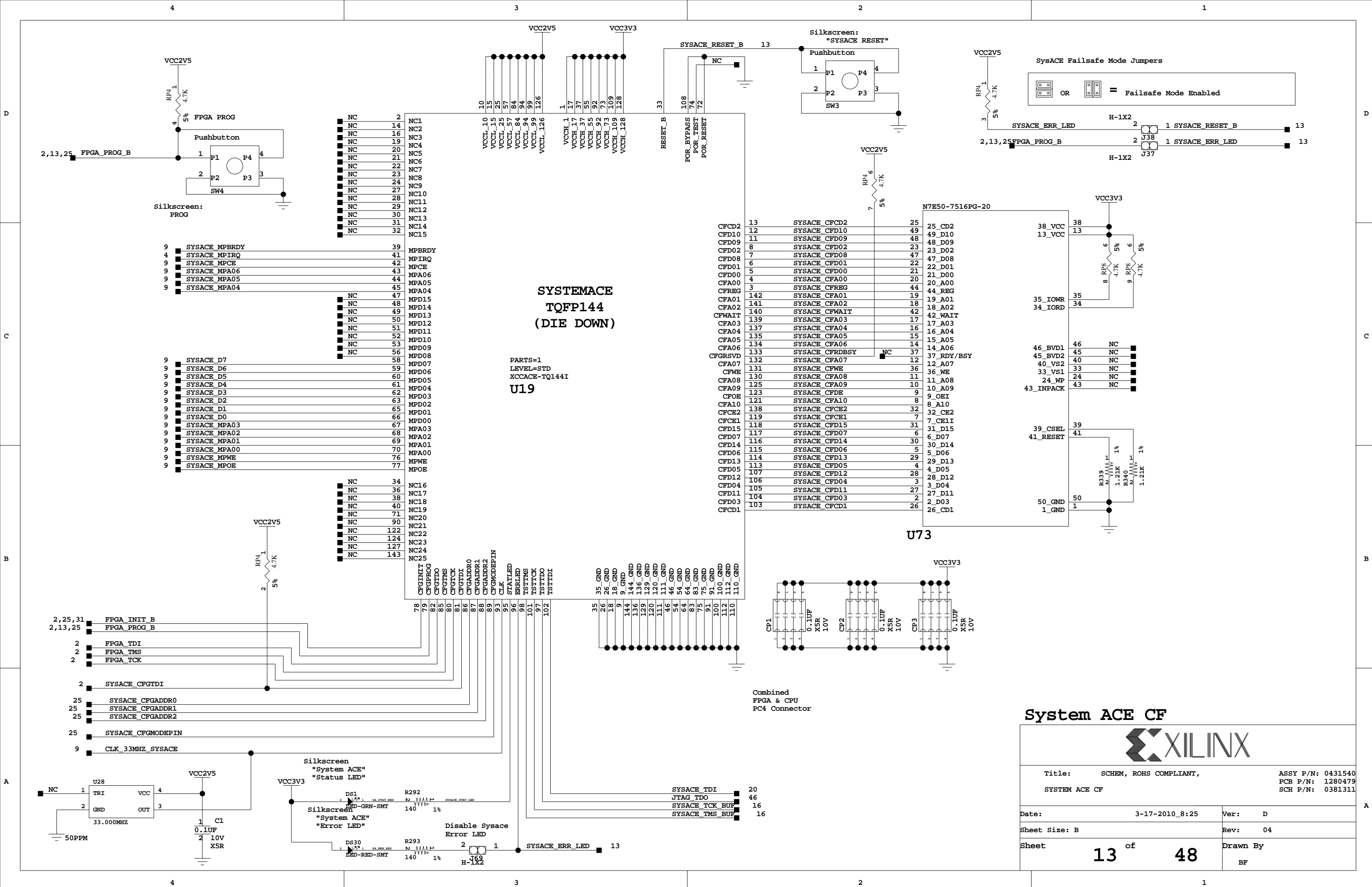


| | | |
|--------|-----------------------|-------------------|
| Title: | FPGA GND | ASSY P/N: 0431540 |
| | SCHEM, ROHS COMPLIANT | PCB P/N: 1280479 |
| | ML605 | SCH P/N: 0381311 |

| | | | |
|-------|-----------------|------|---|
| Date: | 9-17-2009_15:42 | Ver: | D |
|-------|-----------------|------|---|

| | |
|---------------|---------|
| Sheet Size: B | Rev: 04 |
|---------------|---------|

Sheet **12** of **48** Drawn By **BF**



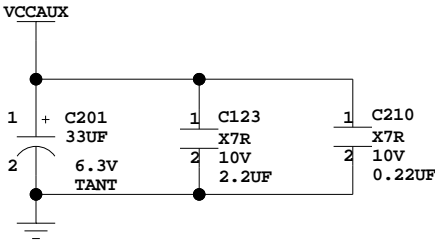
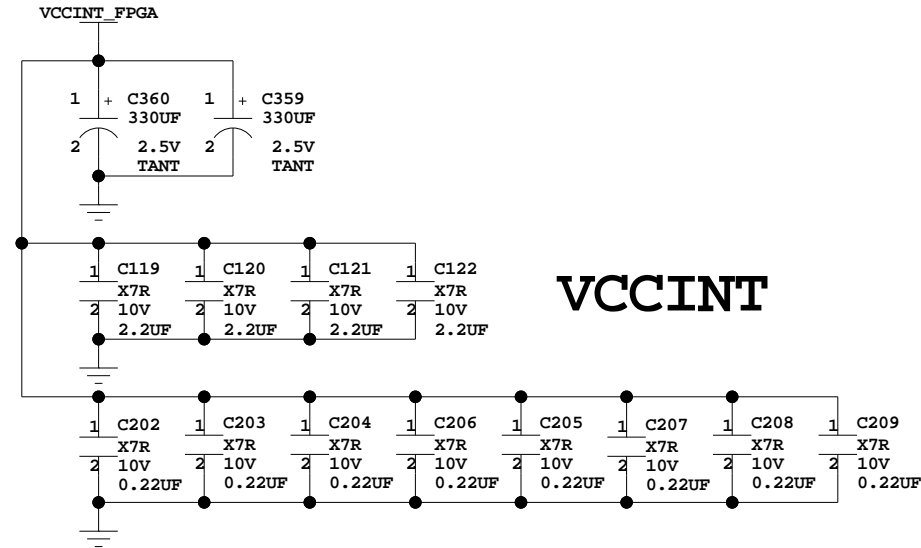
V-6 FF1156 DECOUPLING

PLACEMENT
RULES

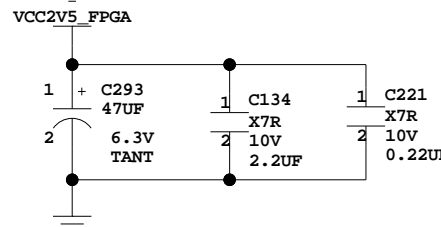
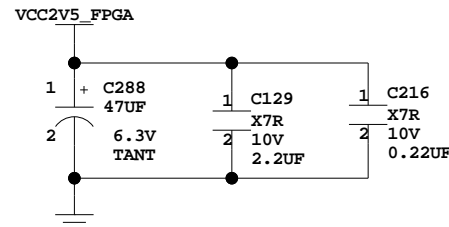
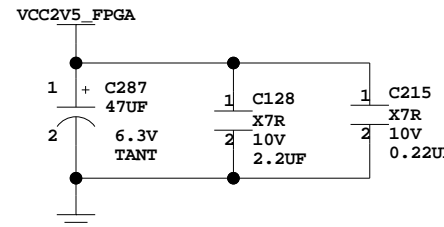
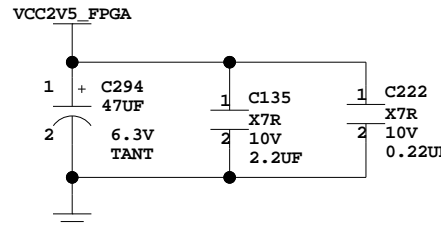
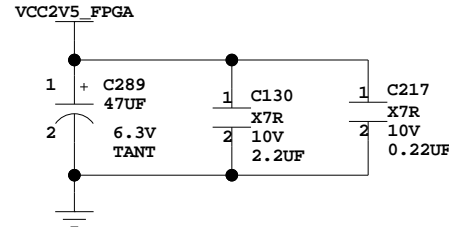
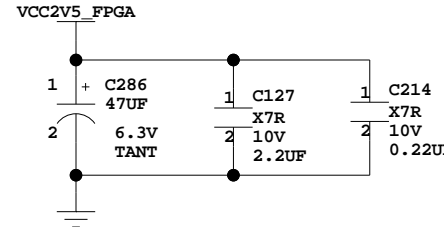
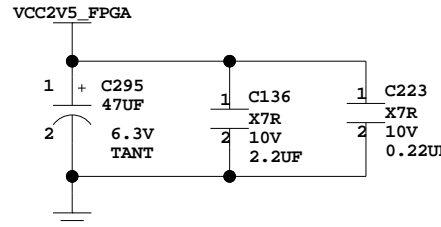
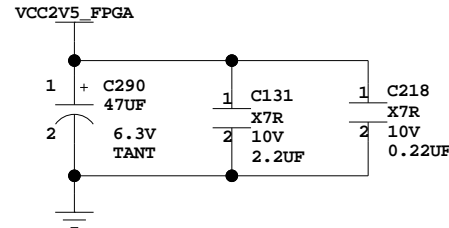
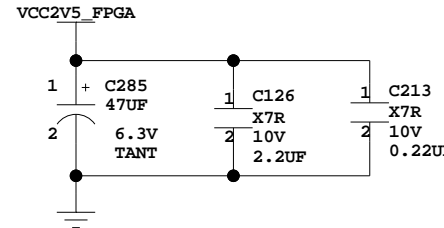
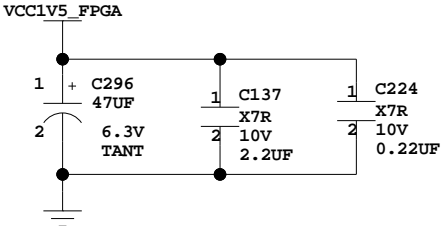
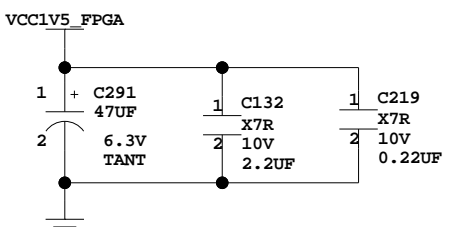
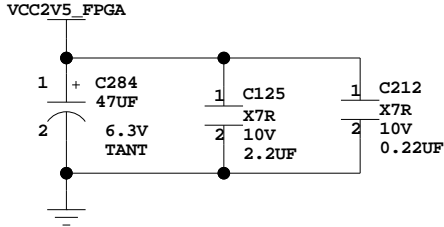
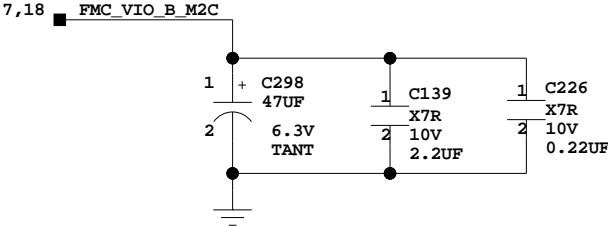
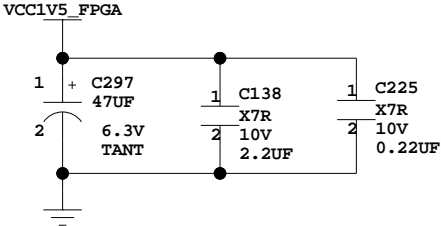
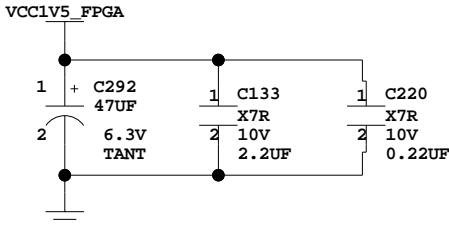
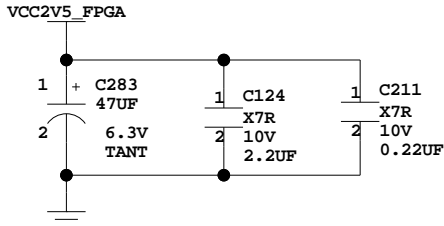
330uF, 100uF, 47uF, 33uF: Anywhere on board,
but as close as possible to FPGA.

2.2uF: No more than 3" from periphery of FPGA,
but as close as possible.

0.22uF: No more than 1" from periphery of FPGA,
but as close as possible.

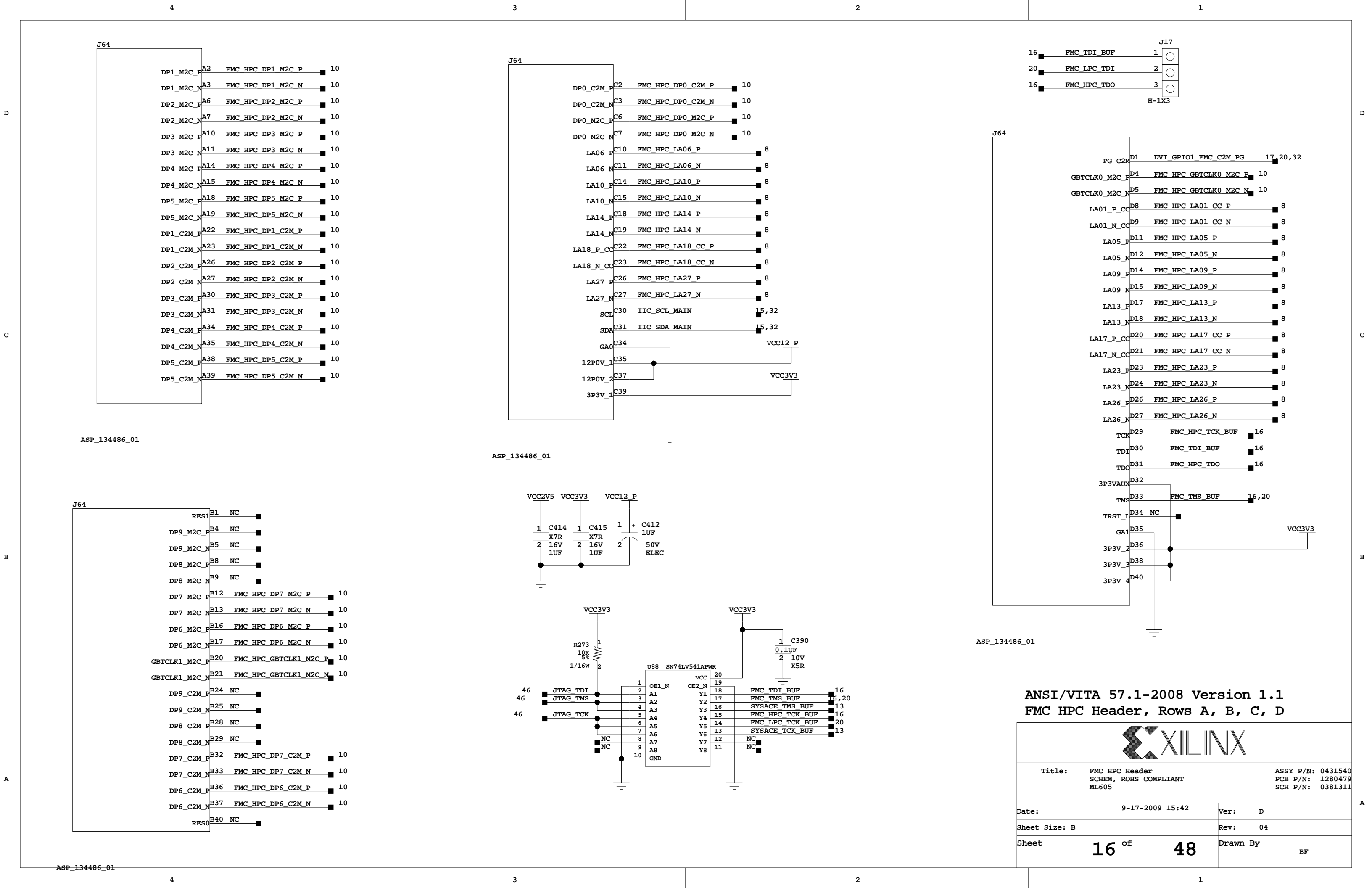


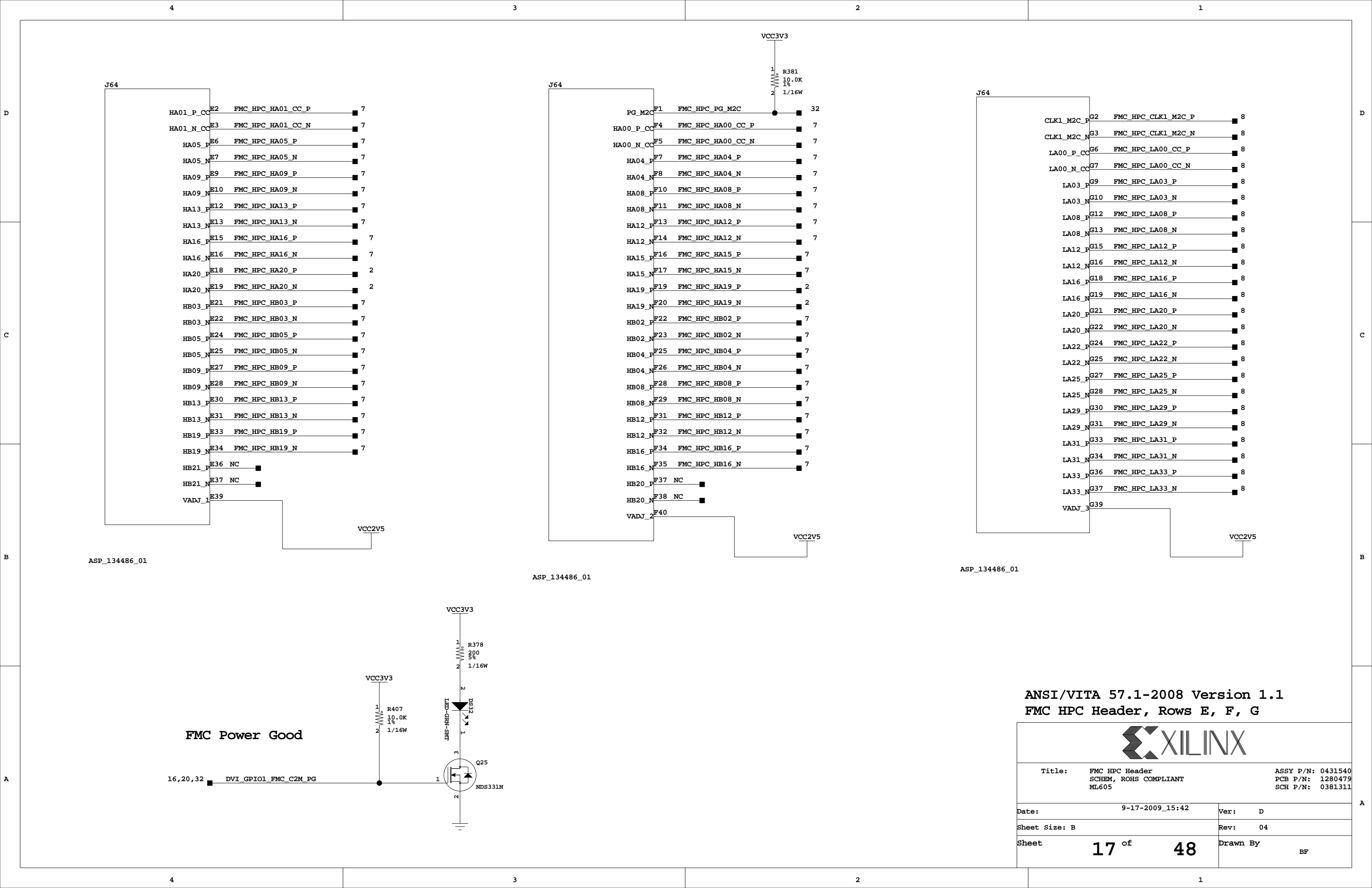
VCCO

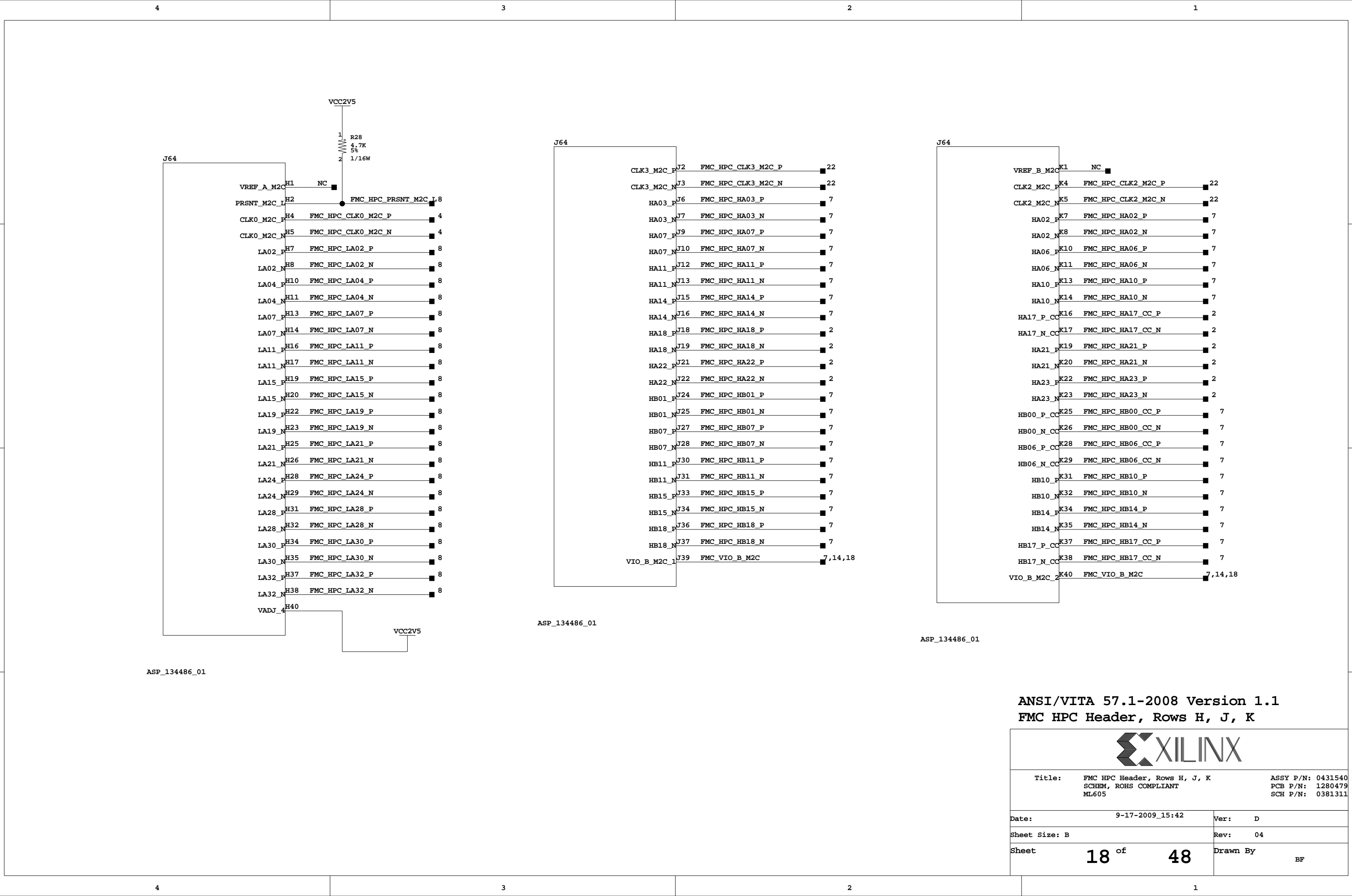


FPGA Decoupling


| | | |
|--|--------|---|
| | | |
| Title: FPGA Decoupling SCHEM, ROHS COMPLIANT ML605 | | ASSY P/N: 0431540 PCB P/N: 1280479 SCH P/N: 0381311 |
| Date: 9-17-2009_15:42 | Ver: D | |
| Sheet Size: B | | Rev: 04 |
| Sheet 14 of 48 | | Drawn By BF |







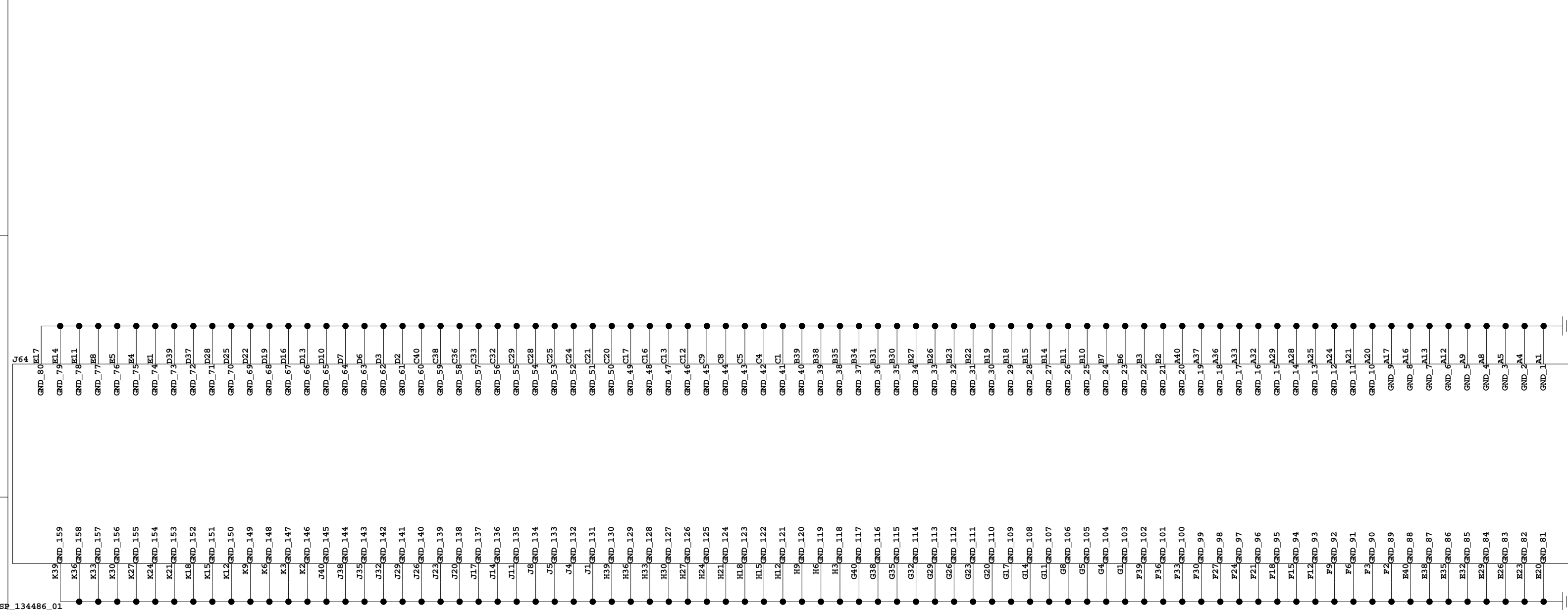
ANSI/VITA 57.1-2008 Version 1.1
FMC HPC Header, GND

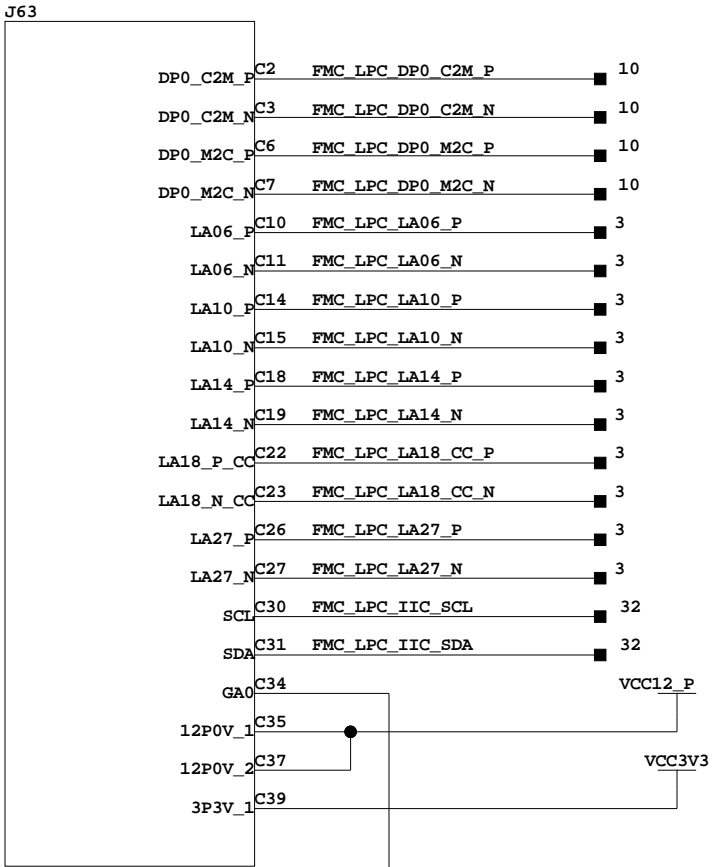


Title: FMC HPC Header
SCHEM, ROHS COMPLIANT
ML605

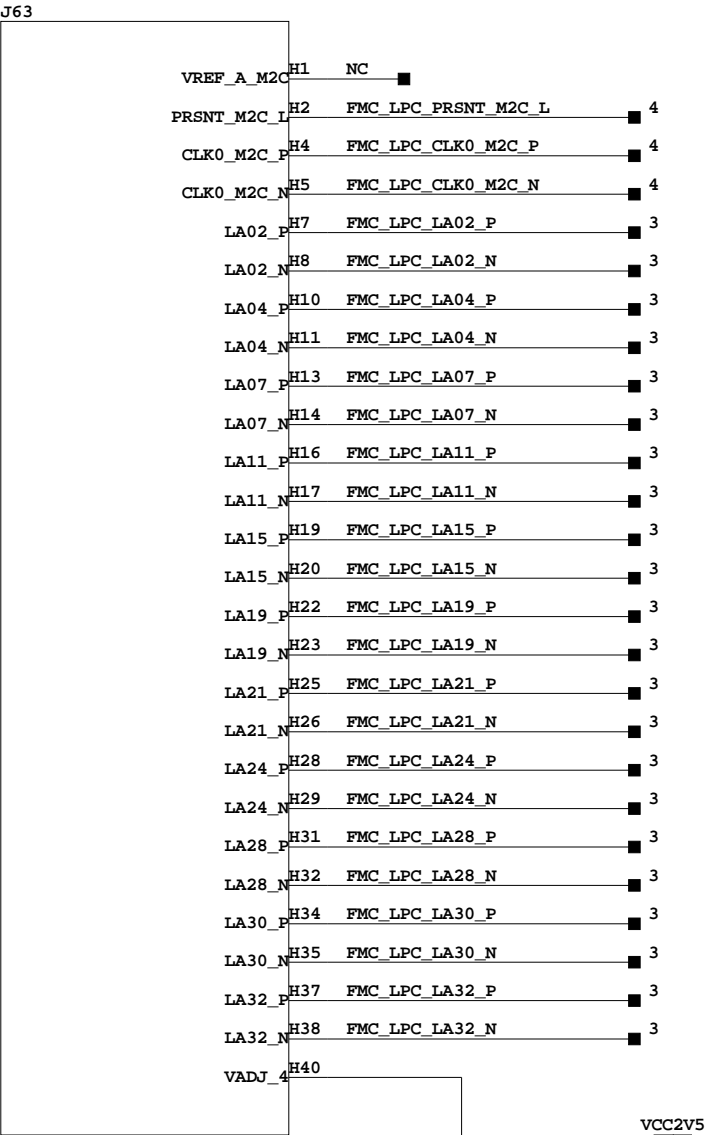
ASSY P/N: 0431540
PCB P/N: 1280479
SCH P/N: 0381311

| | |
|-----------------------|-------------|
| Date: 9-17-2009_15:42 | Ver: D |
| Sheet Size: B | Rev: 04 |
| Sheet 19 of 48 | Drawn By BF |

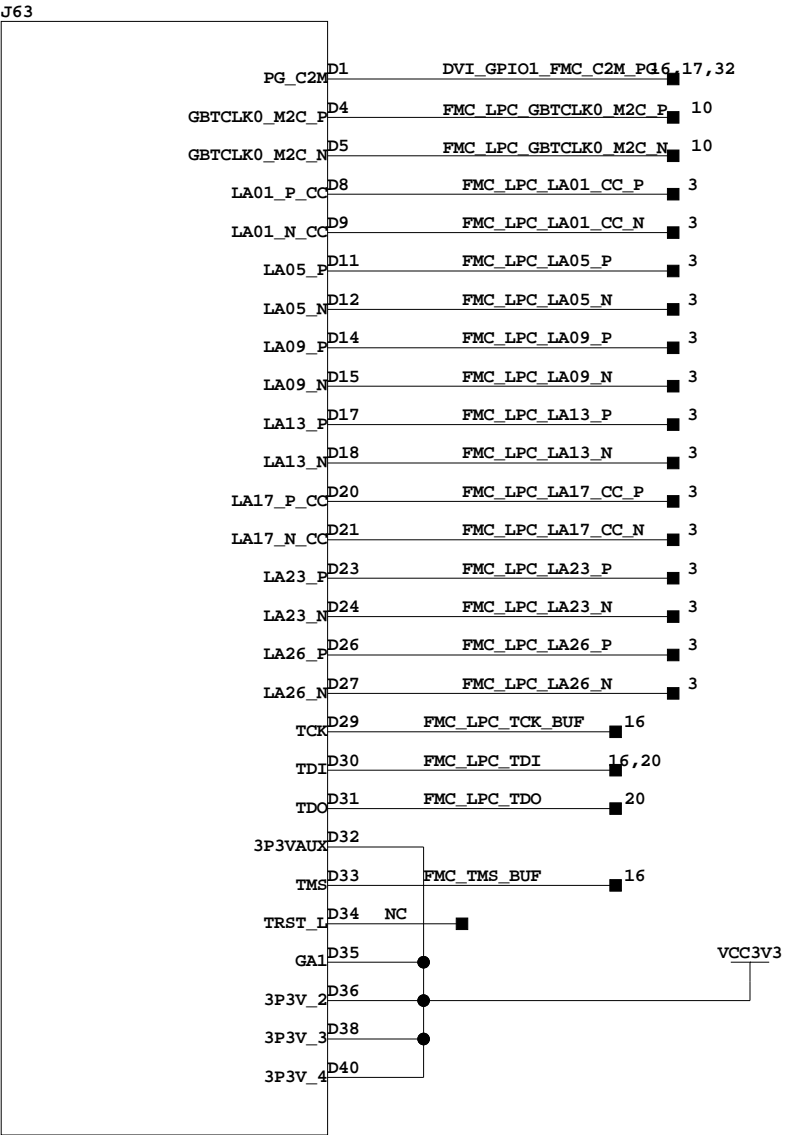




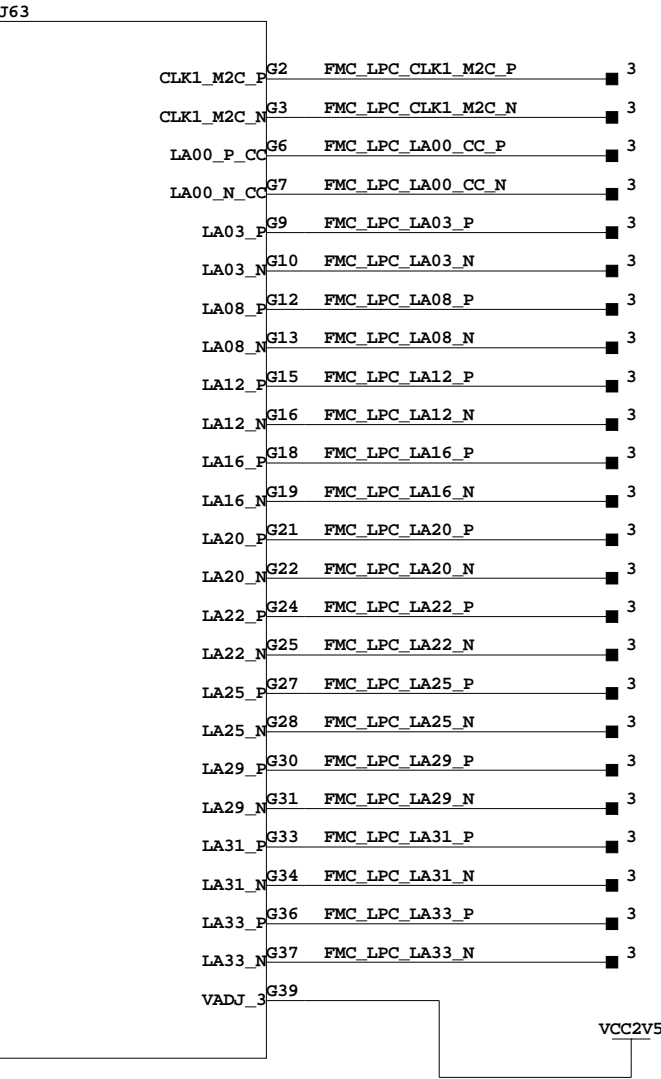
ASP_134603_01



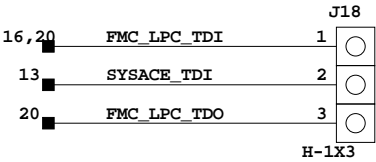
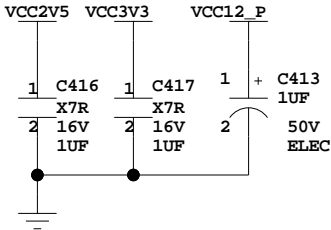
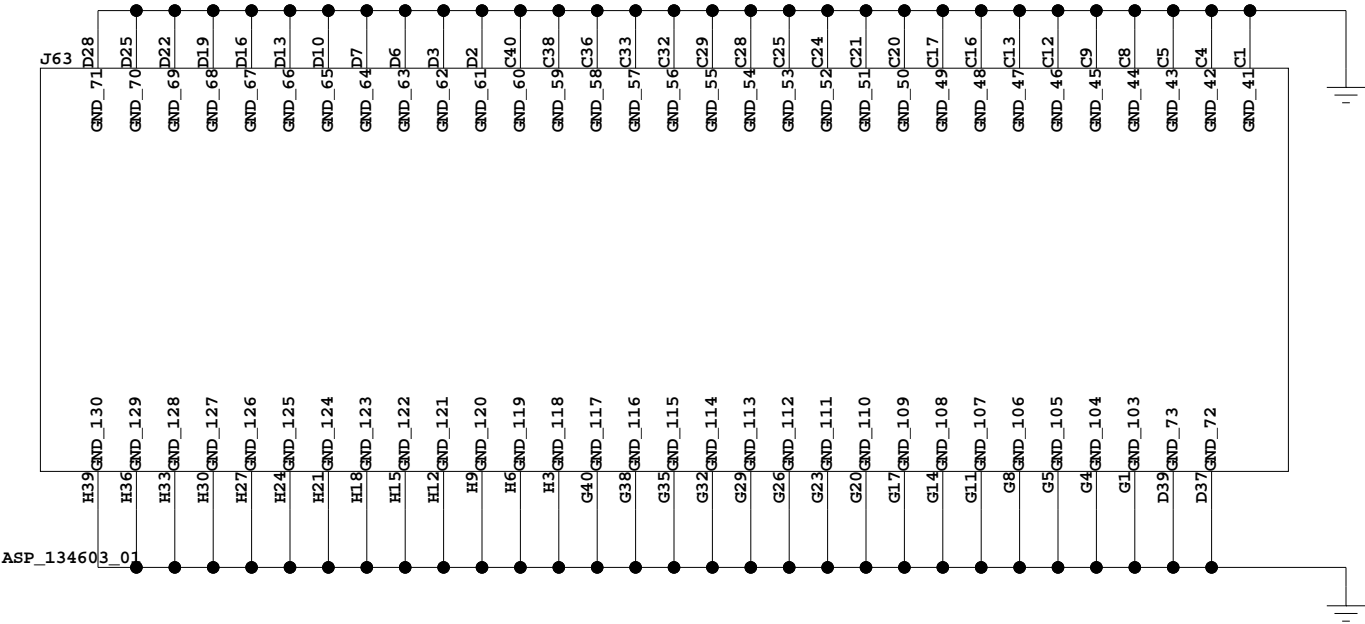
ASP_134603_01



ASP_134603_01




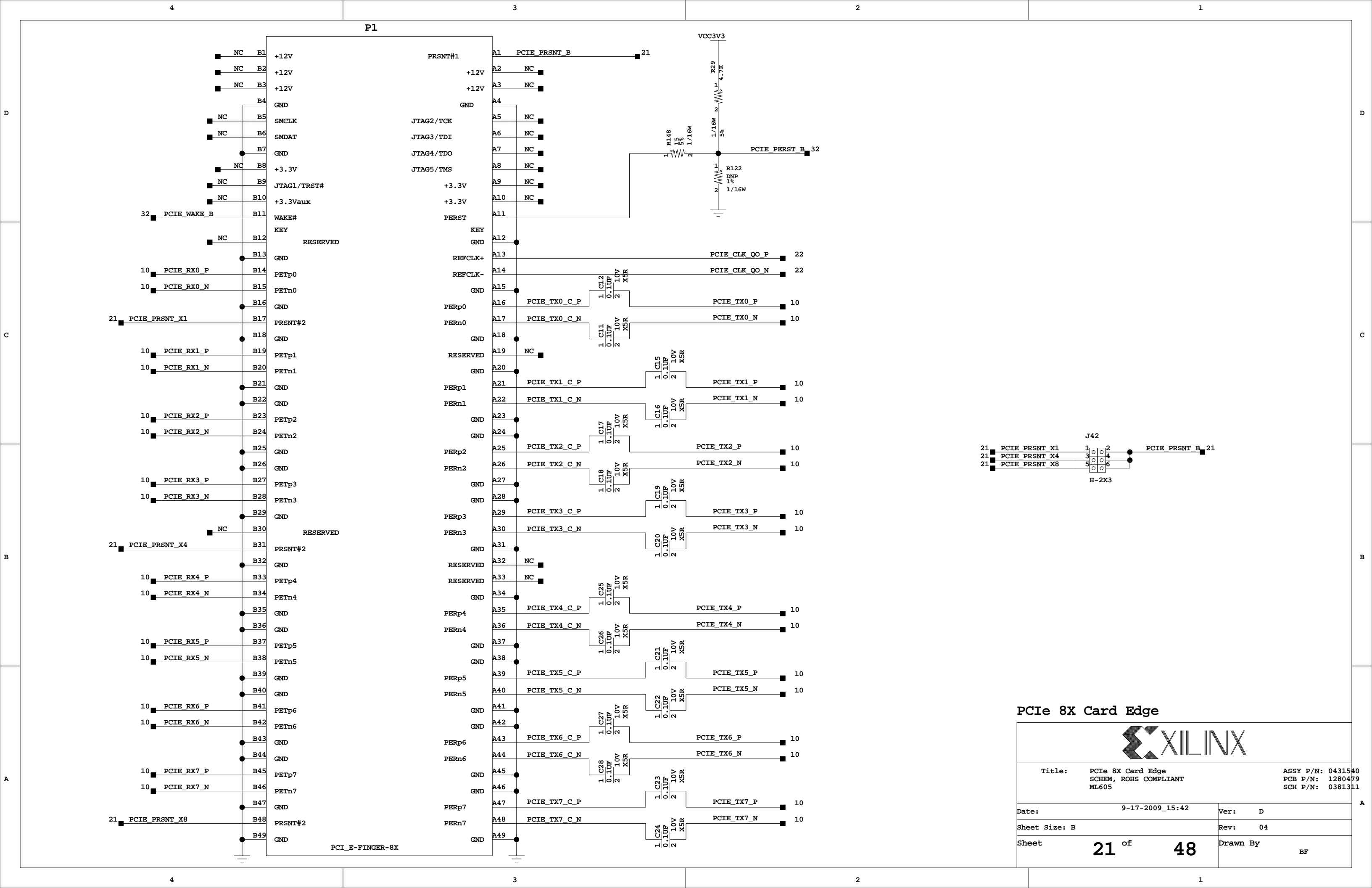
ASP_134603_01

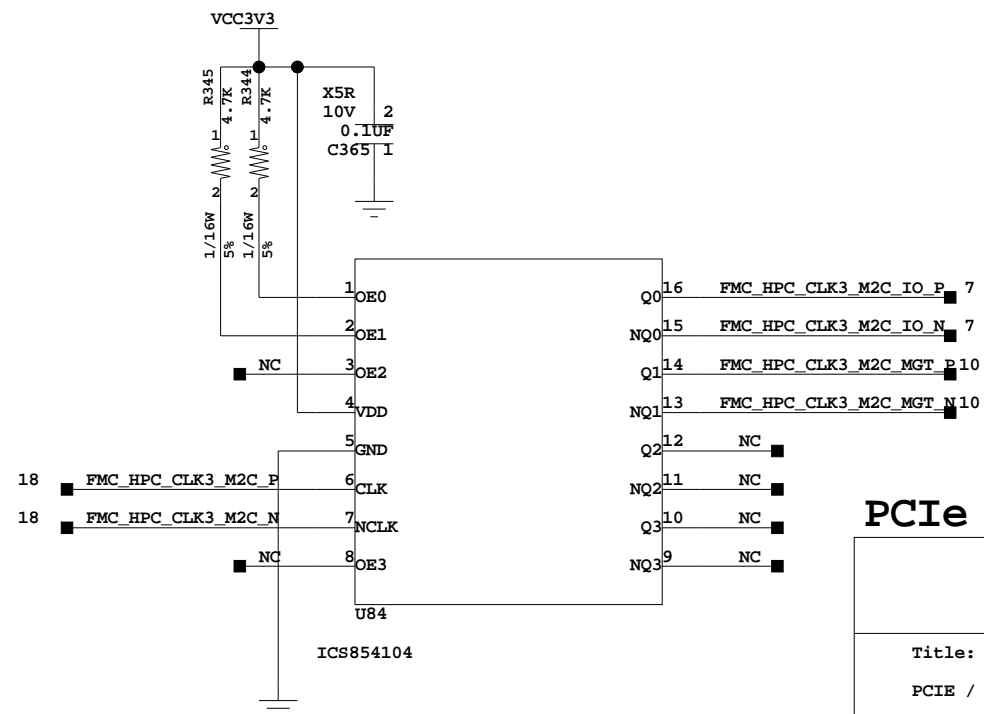
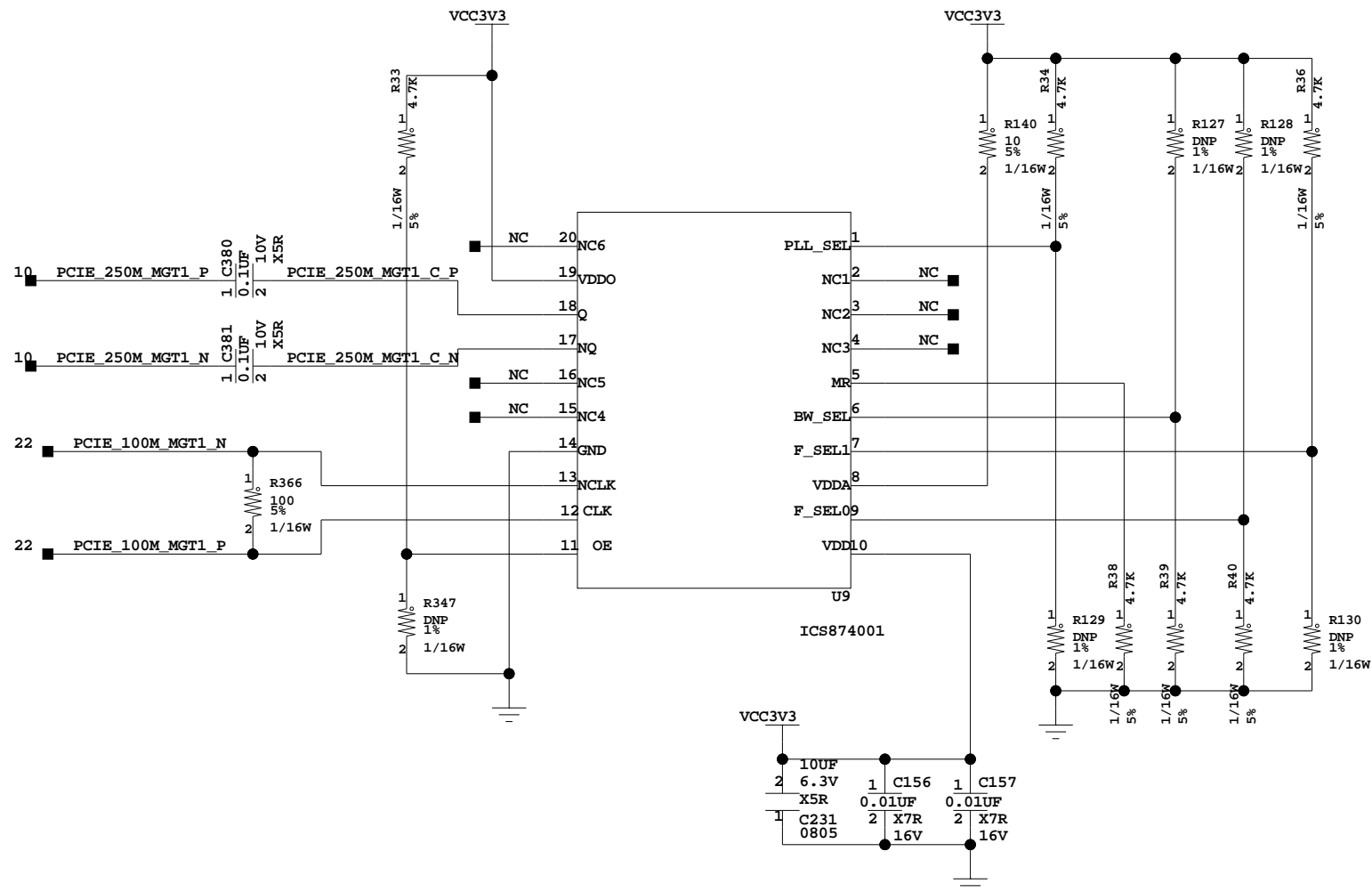
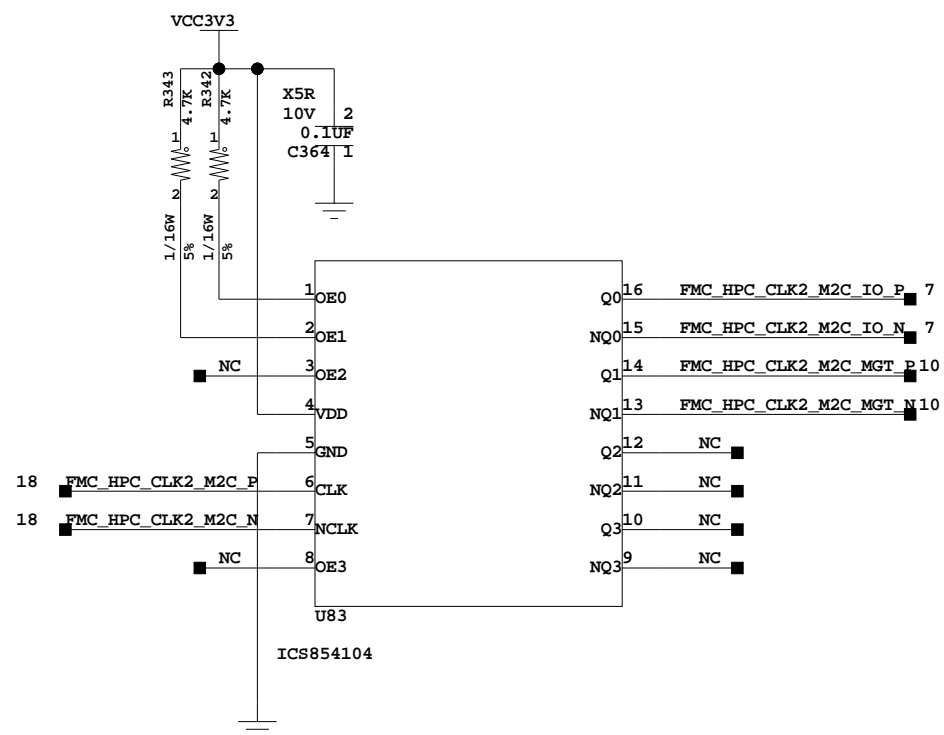
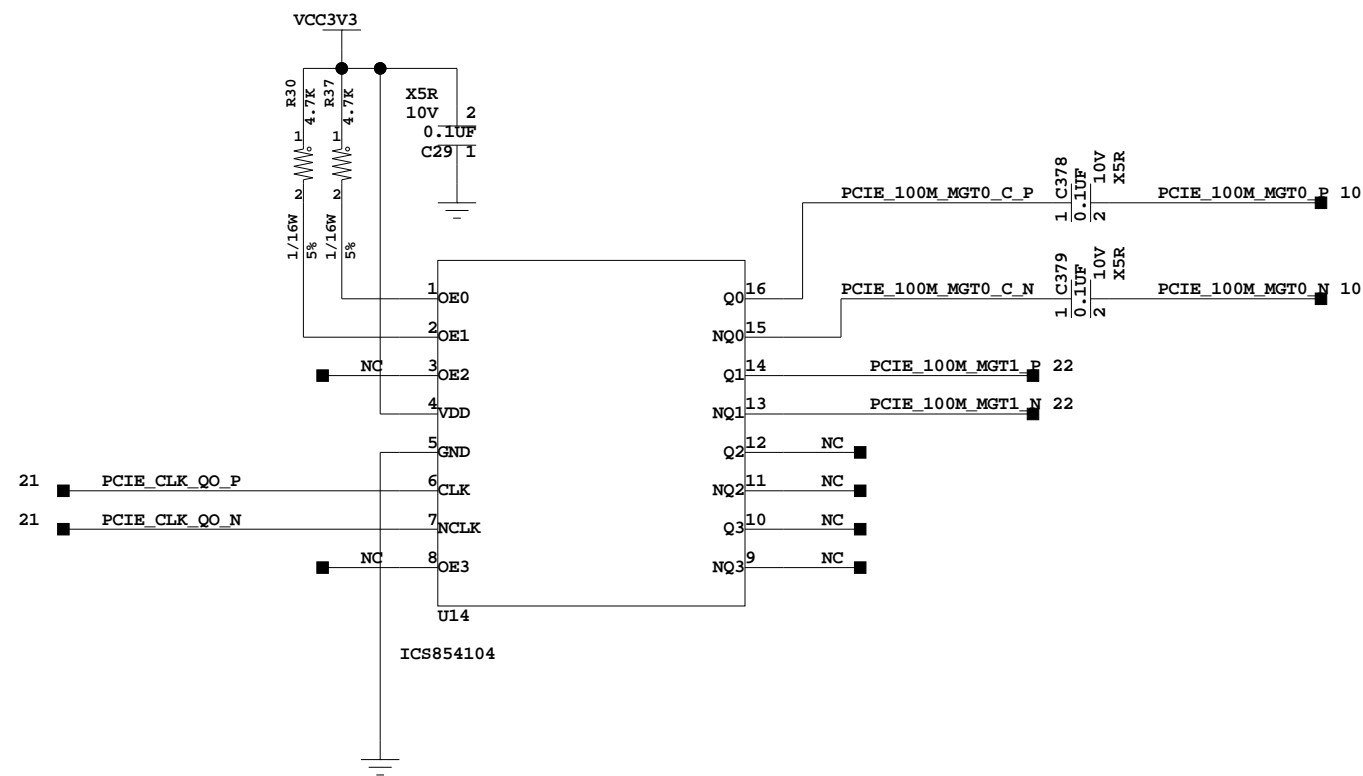


ANSI/VITA 57.1-2008 Version 1.1

FMC LPC Connector

| | | |
|---|-------------|---|
|  | | |
| Title: FMC LPC Connector SCHEM, ROHS COMPLIANT SA605 EVALUATION PLATFORM | | ASSY P/N: 0431540 PCB P/N: 1280479 SCH P/N: 0381311 |
| Date: 9-17-2009_15:42 | Ver: D | |
| Sheet Size: B | Rev: 04 | |
| Sheet 20 of 48 | Drawn By BF | |





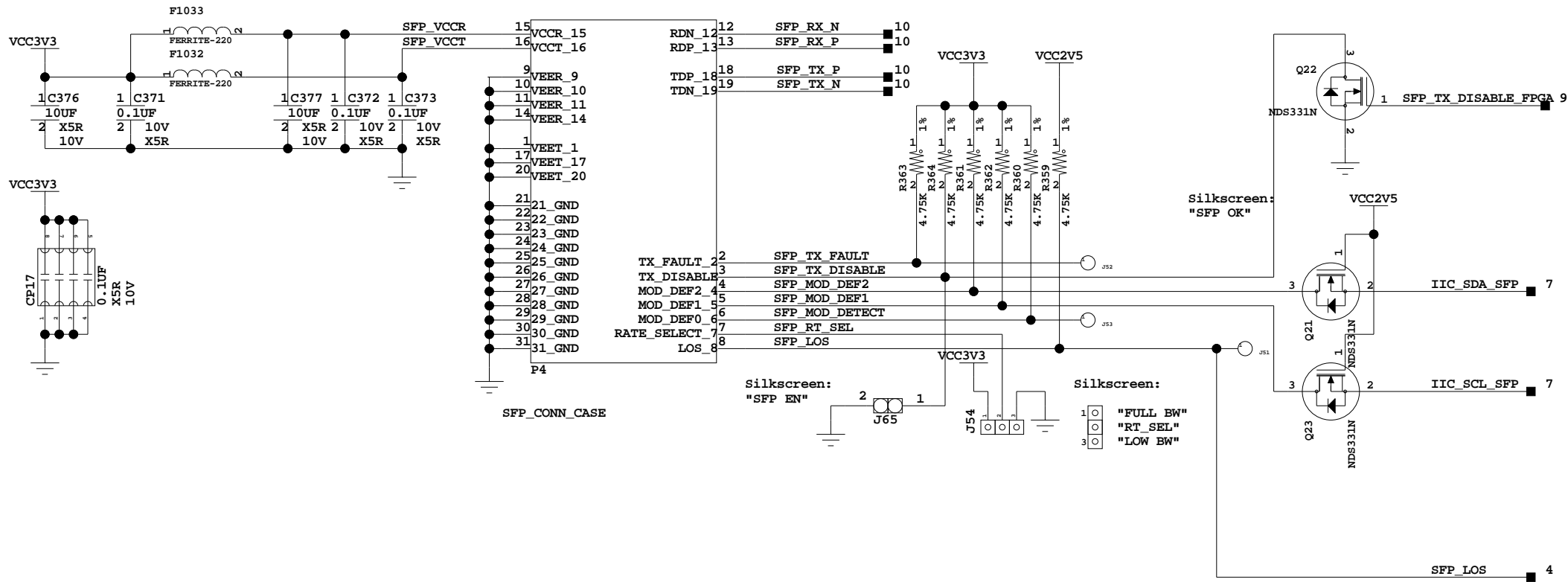
PCIe / MGT Clocking



| | | |
|---------------------|------------------------|-------------------|
| Title: | SCHEM, ROHS COMPLIANT, | ASSY P/N: 0431540 |
| | | PCB P/N: 1280479 |
| PCIE / MGT CLOCKING | | SCH P/N: 0381311 |

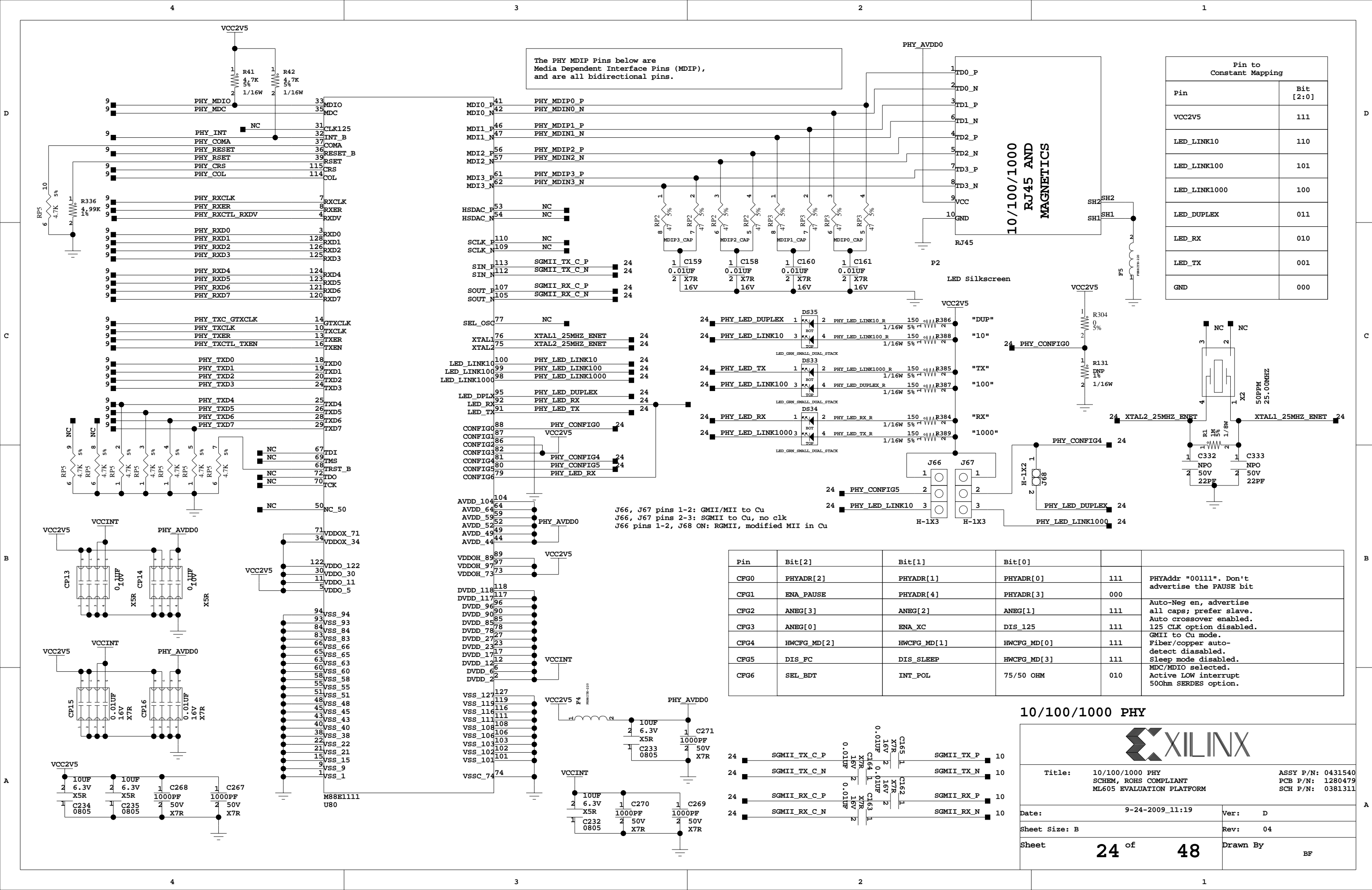
| | | | |
|-------------|-----------------|----------|----|
| Date: | 9-24-2009_11:18 | Ver: | D |
| Sheet Size: | B | Rev: | 04 |
| Sheet | 22 of 48 | Drawn By | BF |

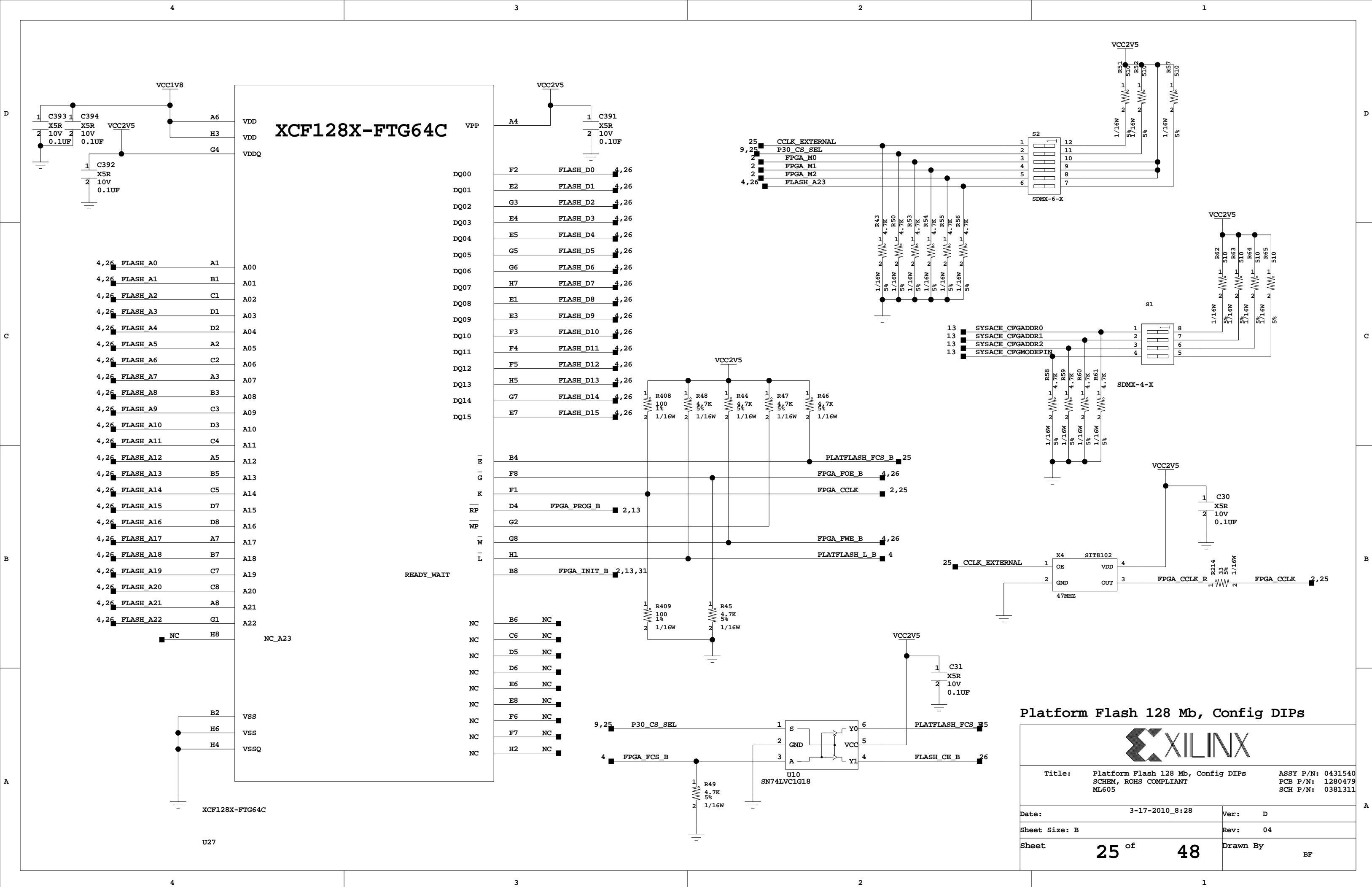
SFP MODULE

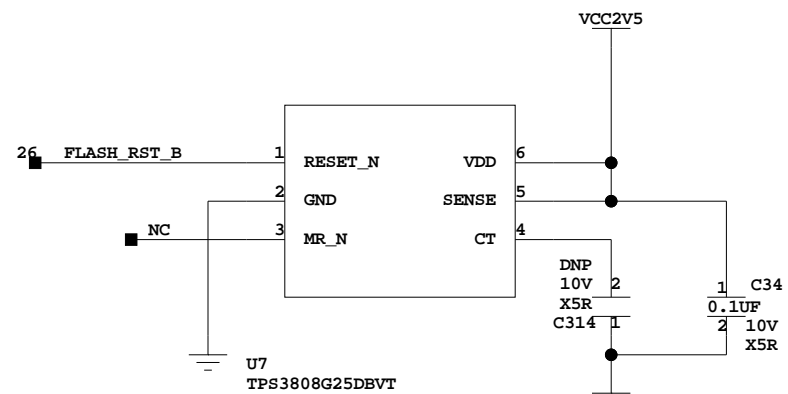


SFP Cage

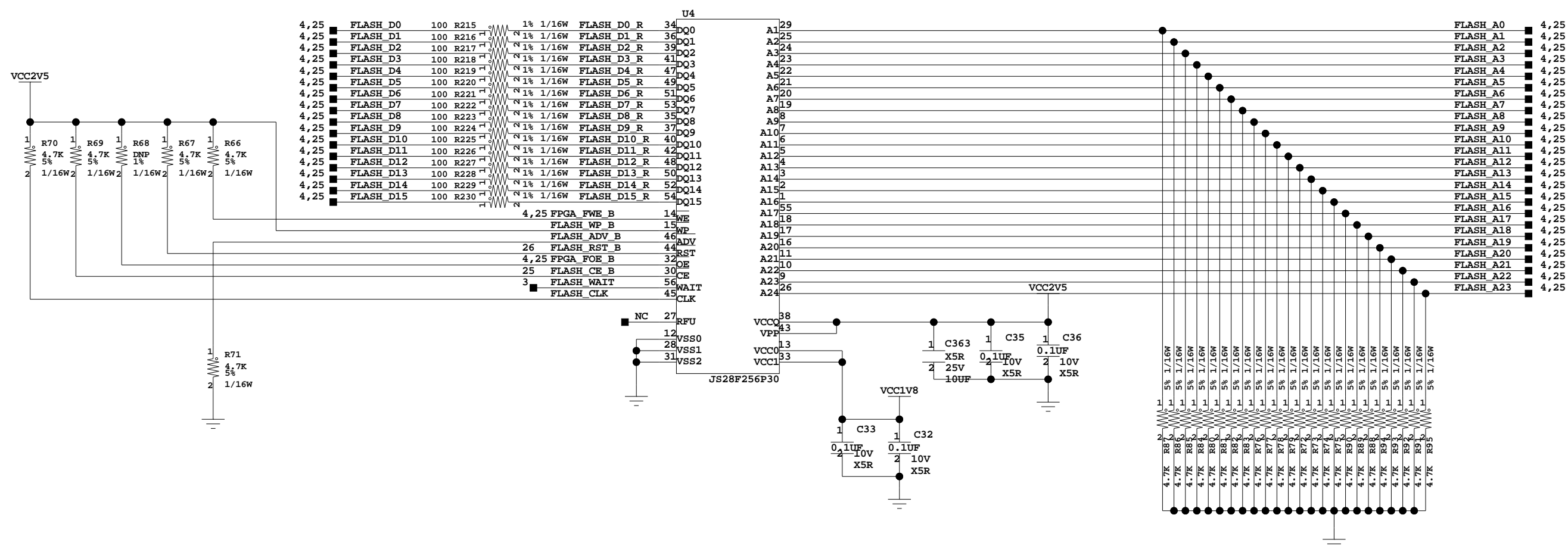
| | | |
|--|-------------|---|
| | | |
| Title: SCHEM, ROHS COMPLIANT SFP Cage | | ASSY P/N: 0431540 PCB P/N: 1280479 SCH P/N: 0381311 |
| Date: 9-24-2009_11:18 | Ver: D | |
| Sheet Size: B | Rev: 04 | |
| Sheet 23 of 48 | Drawn By BF | |







$$\text{Cap Value in nF} = (((\text{DELAY in S}) - (0.5 * 0.001)) * 175)$$



BPI FLASH



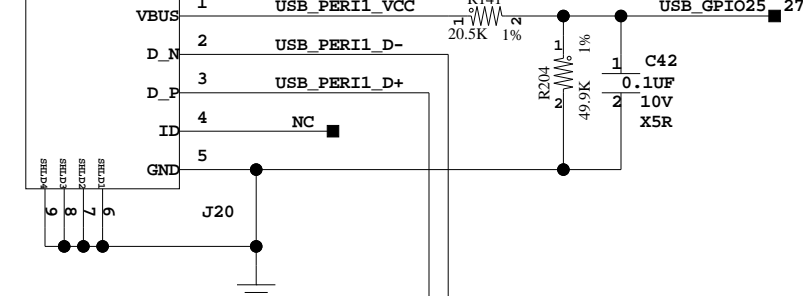
| | | |
|--------|-----------------------|-------------------|
| Title: | BPI Flash | ASSY P/N: 0431540 |
| | SCHEM, ROHS COMPLIANT | PCB P/N: 1280479 |
| | ML605 | SCH P/N: 0381311 |

| | | | |
|-------------|-----------------|----------|----|
| Date: | 9-17-2009_15:42 | Ver: | D |
| Sheet Size: | B | Rev: | 04 |
| Sheet | 26 of 48 | Drawn By | BF |

Silkscreen:

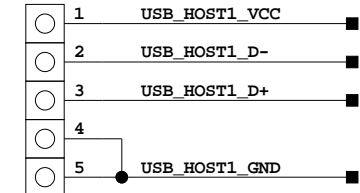
"USB Peripheral 1"

USB_MINI_B



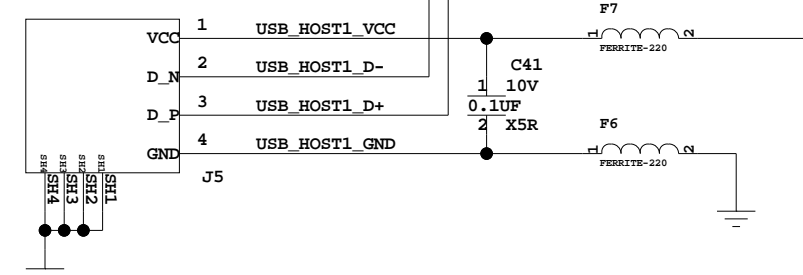
HDR1x5

J36

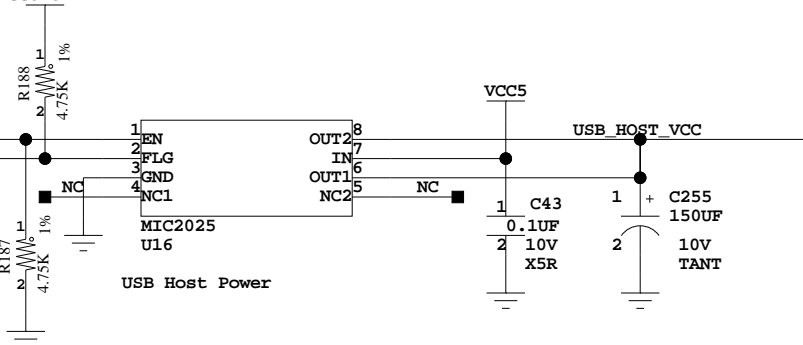


Silkscreen:

"USB Host"



VCC3V3



USB Host Power



USB Host Power

USB Host Power

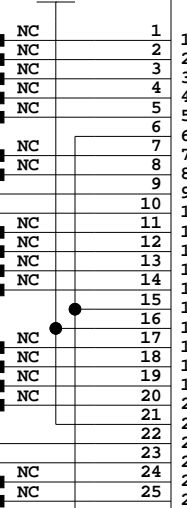
USB Host Power

USB Host Power

USB Host Power

USB Host Power

VCC3V3



CY7C67300-100AI

(DIE UP)

CY7C67300-100AI

(DIE UP)

CY7C67300-100AI

(DIE UP)

CY7C67300-100AI

(DIE UP)

CY7C67300-100AI

(DIE UP)

CY7C67300-100AI

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CY7C67300-100AI

(DIE UP)

CY7C67300-100AI

(DIE UP)

CY7C67300-100AI

(DIE UP)

CY7C67300-100AI

(DIE UP)

CY7C67300-100AI

(DIE UP)

CY7C67300-100AI

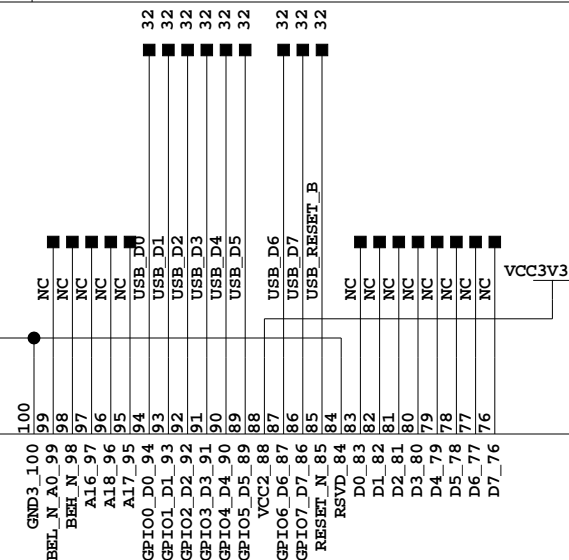
(DIE UP)

CY7C67300-100AI

(DIE UP)

CY7C67300-100AI

(DIE UP)



CY7C67300-100AI

(DIE UP)

CY7C67300-100AI

(DIE UP)

CY7C67300-100AI

(DIE UP)

CY7C67300-100AI

(DIE UP)

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(DIE UP)

CY7C67300-100AI

(DIE UP)

CY7C67300-100AI

(DIE UP)

CY7C67300-100AI

(DIE UP)

CY7C67300-100AI

(DIE UP)

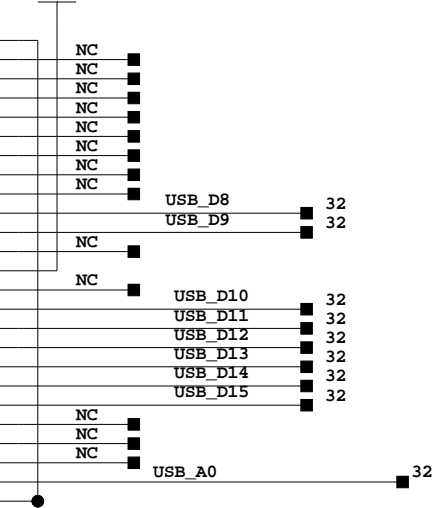
CY7C67300-100AI

(DIE UP)

CY7C67300-100AI

(DIE UP)

VCC3V3



CY7C67300-100AI

(DIE UP)

CY7C67300-100AI

(DIE UP)

CY7C67300-100AI

(DIE UP)

CY7C67300-100AI

(DIE UP)

CY7C67300-100AI

(DIE UP)

CY7C67300-100AI

(DIE UP)

CY7C67300-100AI

(DIE UP)

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CY7C67300-100AI

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CY7C67300-100AI

(DIE UP)

CY7C67300-100AI

(DIE UP)

CY7C67300-100AI

(DIE UP)

CY7C67300-100AI

(DIE UP)

CY7C67300-100AI

(DIE UP)

CY7C67300-100AI

(DIE UP)

USB Controller



Title: USB Controller
SCHEM, ROHS COMPLIANT
ML605

ASSY P/N: 0431540
PCB P/N: 1280479
SCH P/N: 0381311

Date: 9-17-2009_15:42

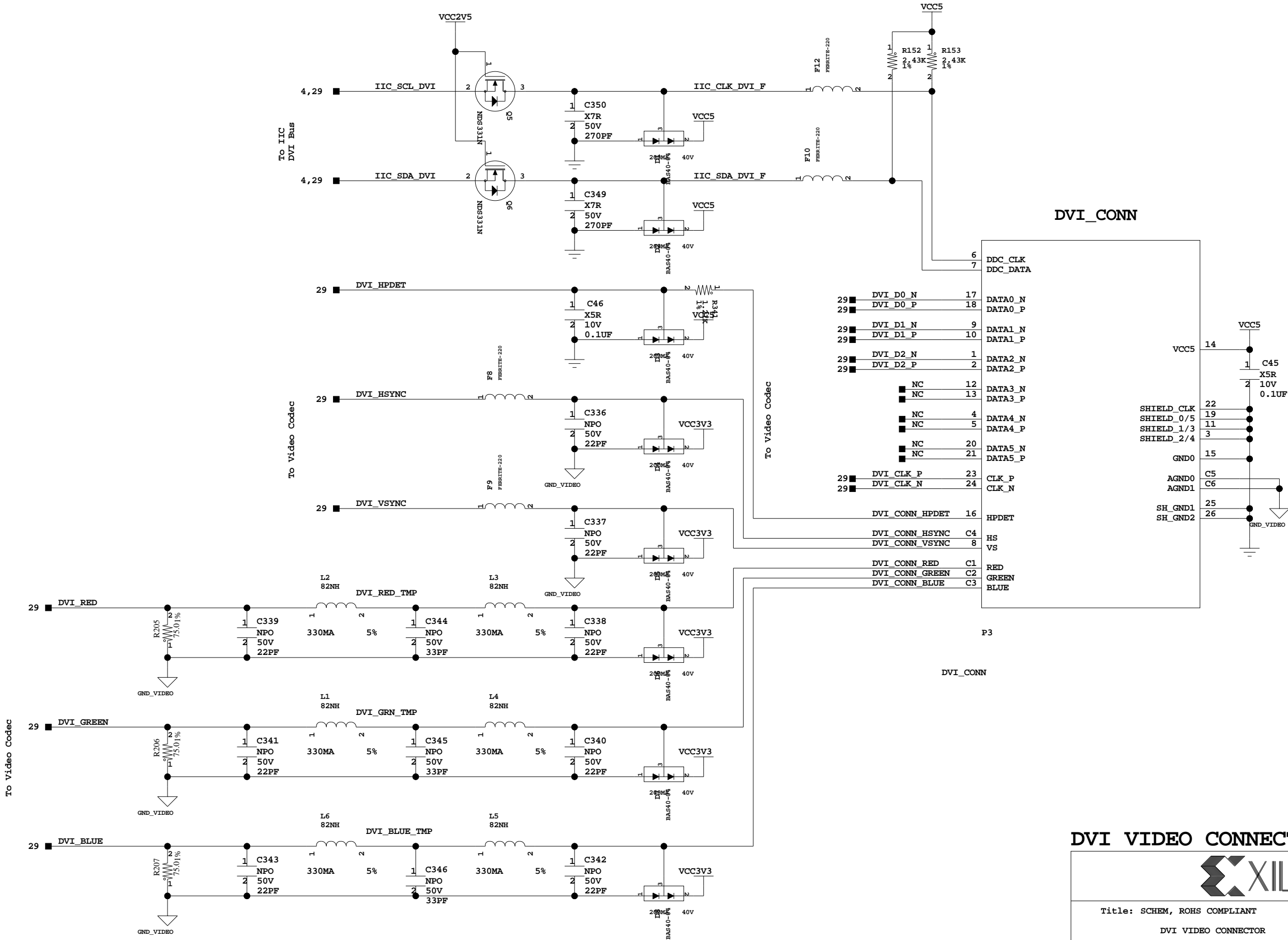
Ver: D

Sheet Size: B

Rev: 04

Sheet 27 of 48

Drawn By BF



DVI VIDEO CONNECTOR

Title: SCHEM, ROHS COMPLIANT

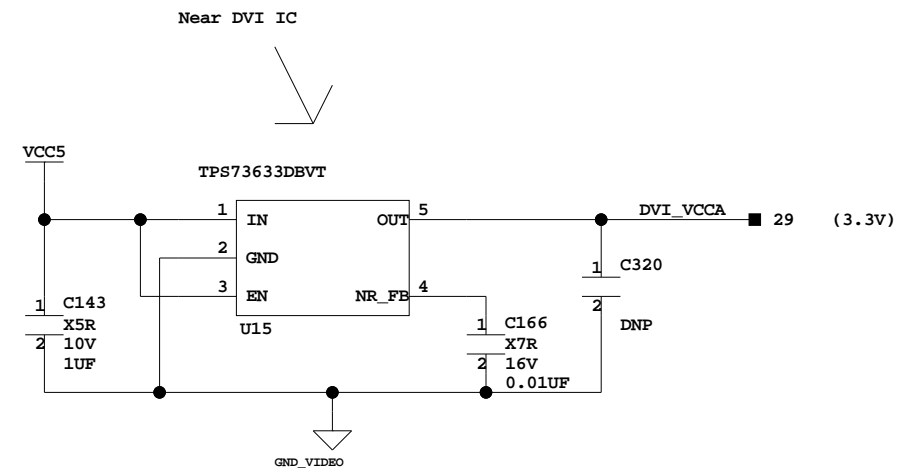
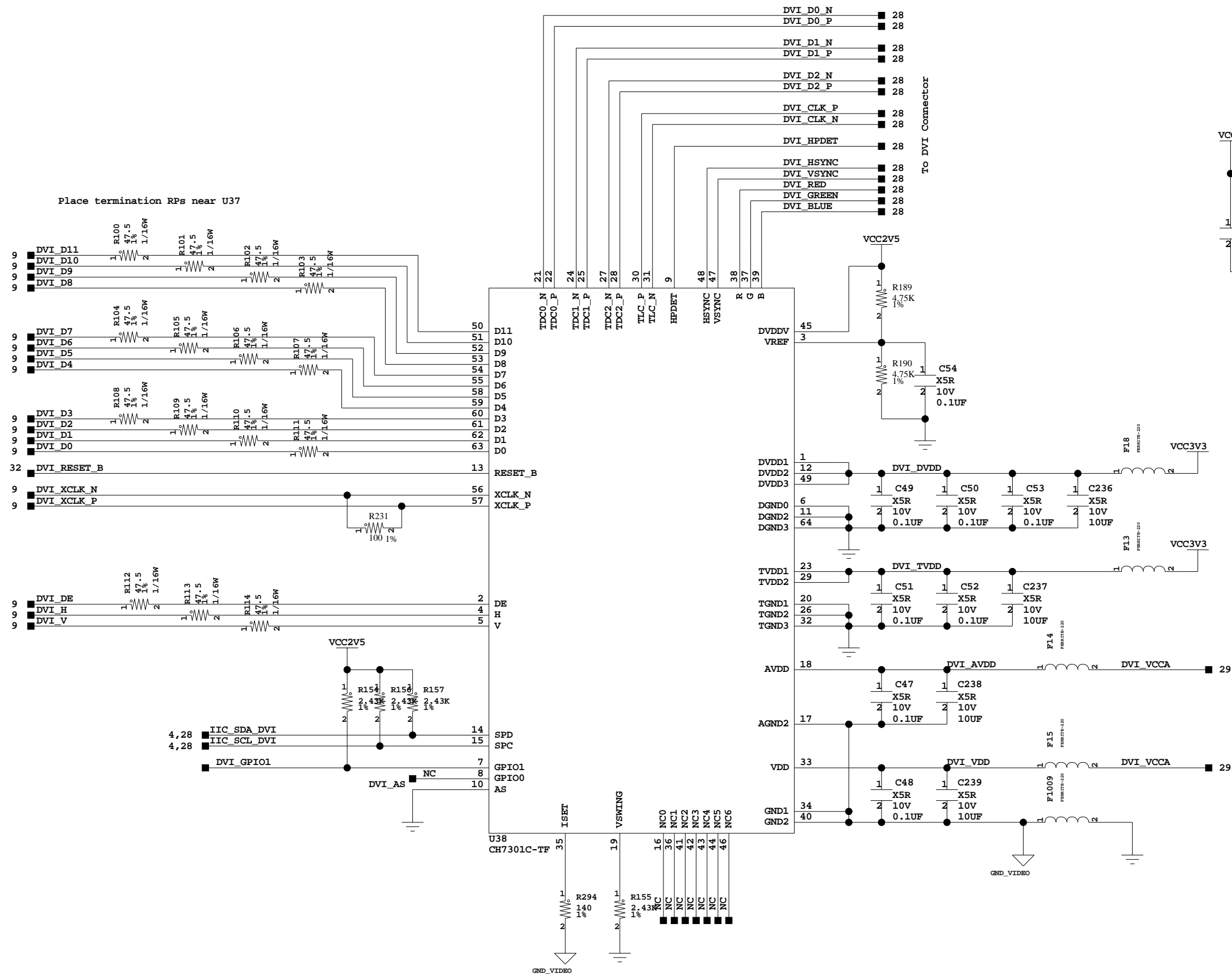
ASSY P/N: 0431540

DVI VIDEO CONNECTOR

PCB P/N: 1280479

SCH P/N: 0381311

| | | | |
|-------------|-----------------|----------|----|
| Date: | 9-17-2009_15:42 | Ver: | D |
| Sheet Size: | B | Rev: | 04 |
| Sheet | 28 of 48 | Drawn By | BF |

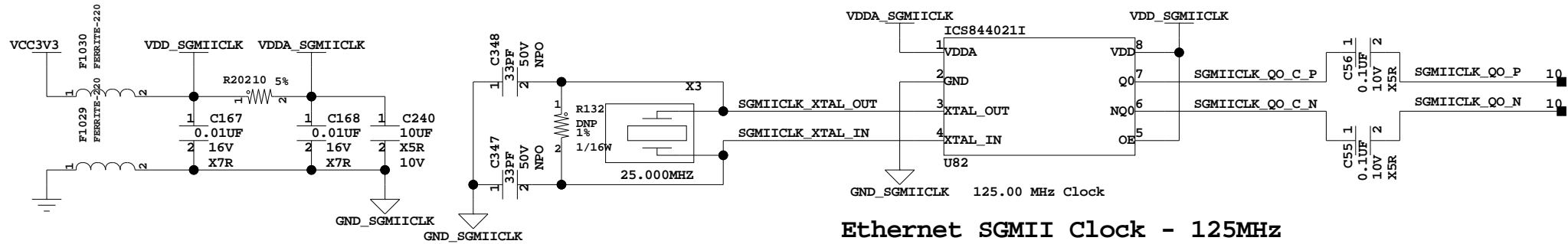


DVI CODEC

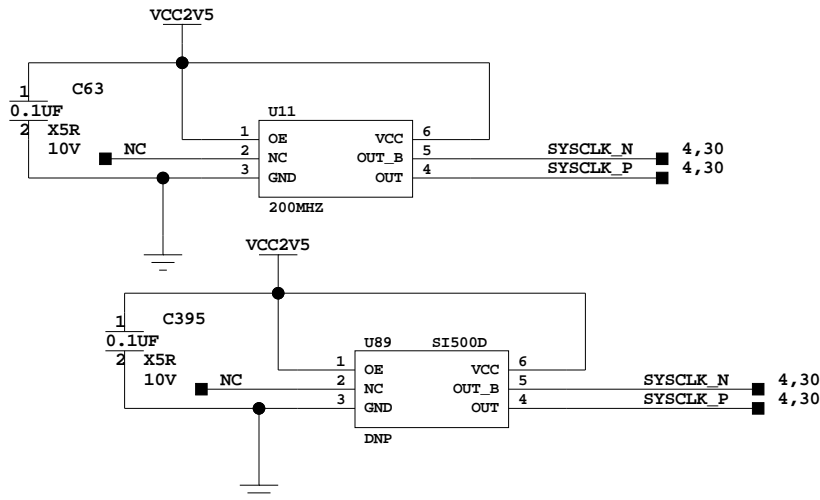


| | | |
|-----------|------------------------|-------------------|
| Title: | SCHEM, ROHS COMPLIANT, | ASSY P/N: 0431540 |
| | | PCB P/N: 1280479 |
| DVI CODEC | | SCH P/N: 0381311 |

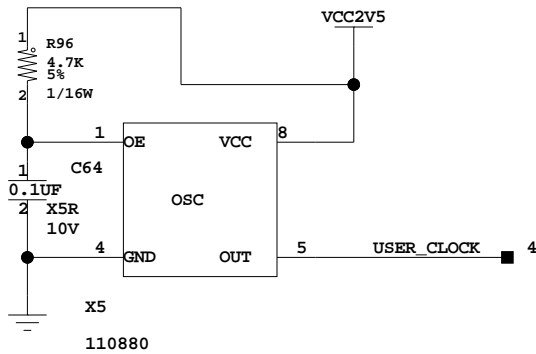
| | | | |
|-------------|-----------------|----------|----|
| Date: | 9-17-2009_15:42 | Ver: | D |
| Sheet Size: | B | Rev: | 04 |
| Sheet | 29 of 48 | Drawn By | BF |



Ethernet SGMII Clock - 125MHz

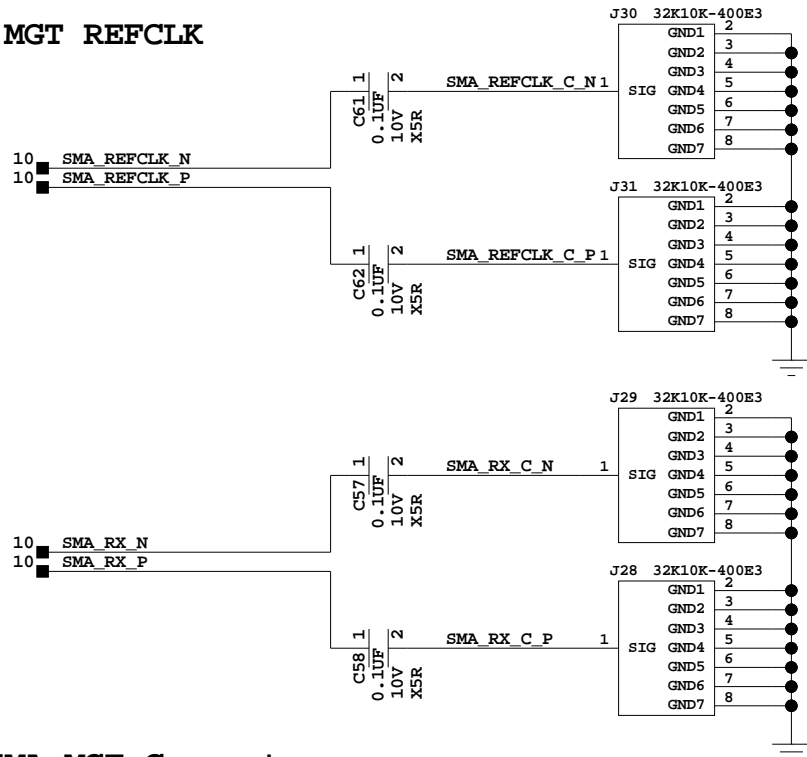


Differential System Clock

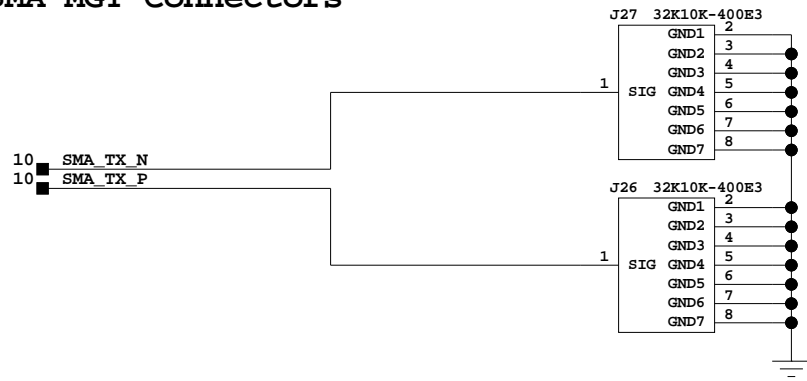


Single Ended User Clock

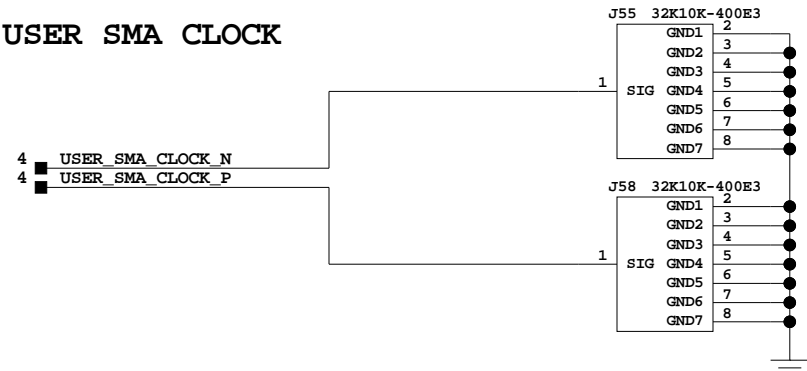
MGT REFCLK



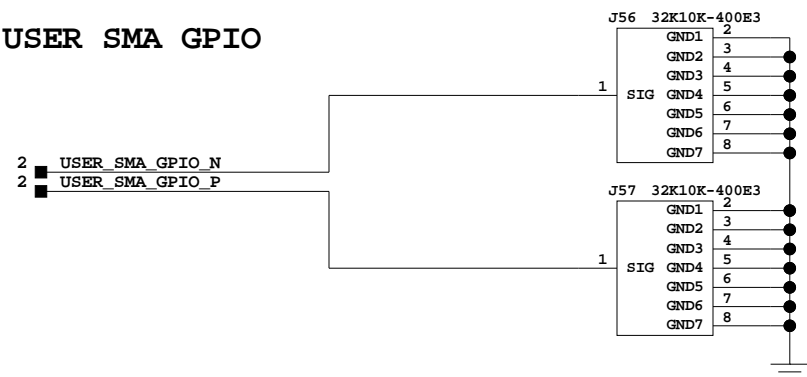
SMA MGT Connectors



USER SMA CLOCK



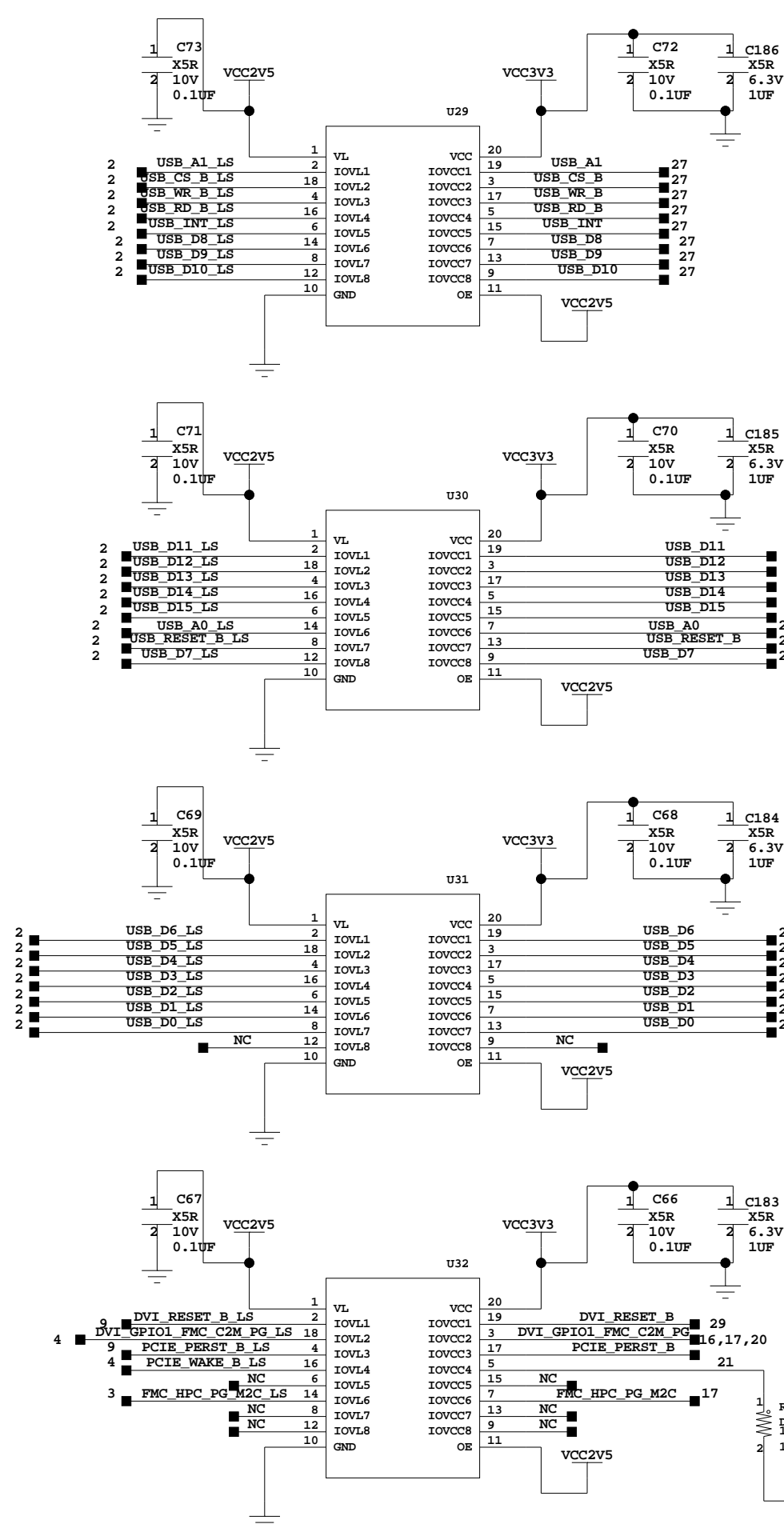
USER SMA GPIO



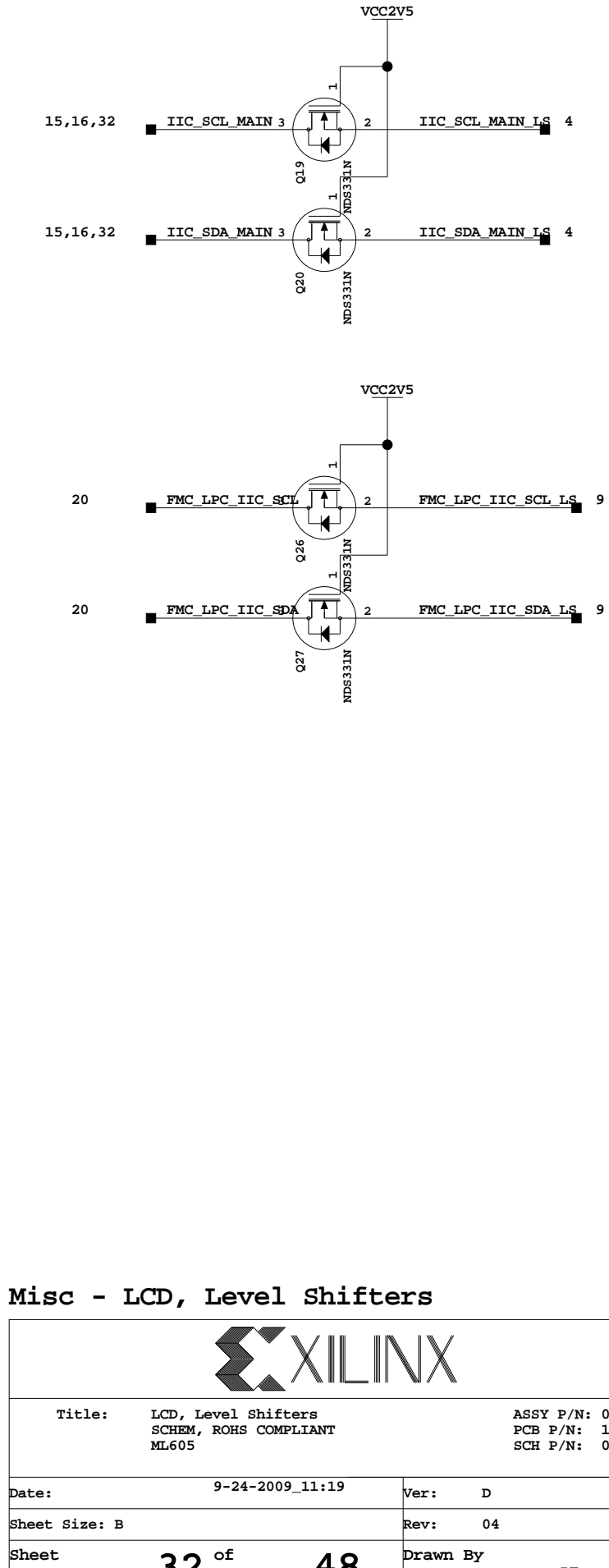
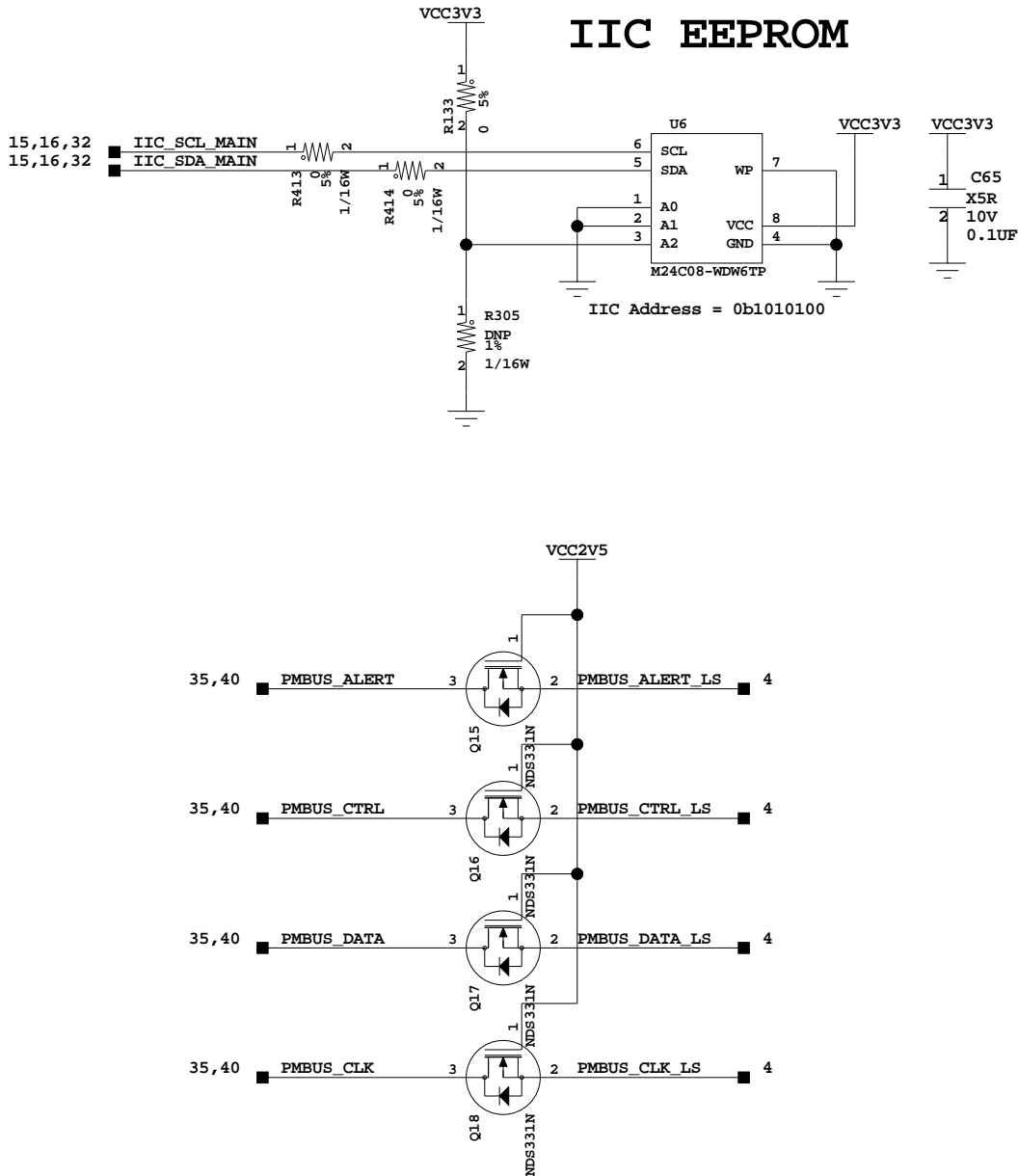
Clocks and MGTs

| | | |
|--|-------------|---|
| | | |
| Title: Clocks and MGTs SCHEM, ROHS COMPLIANT ML605 | | ASSY P/N: 0431540 PCB P/N: 1280479 SCH P/N: 0381311 |
| Date: 3-17-2010_8:28 | Ver: D | |
| Sheet Size: B | Rev: 04 | |
| Sheet 30 of 48 | Drawn By BF | |

3.3V to 2.5V Level Shifters



IIC EEPROM

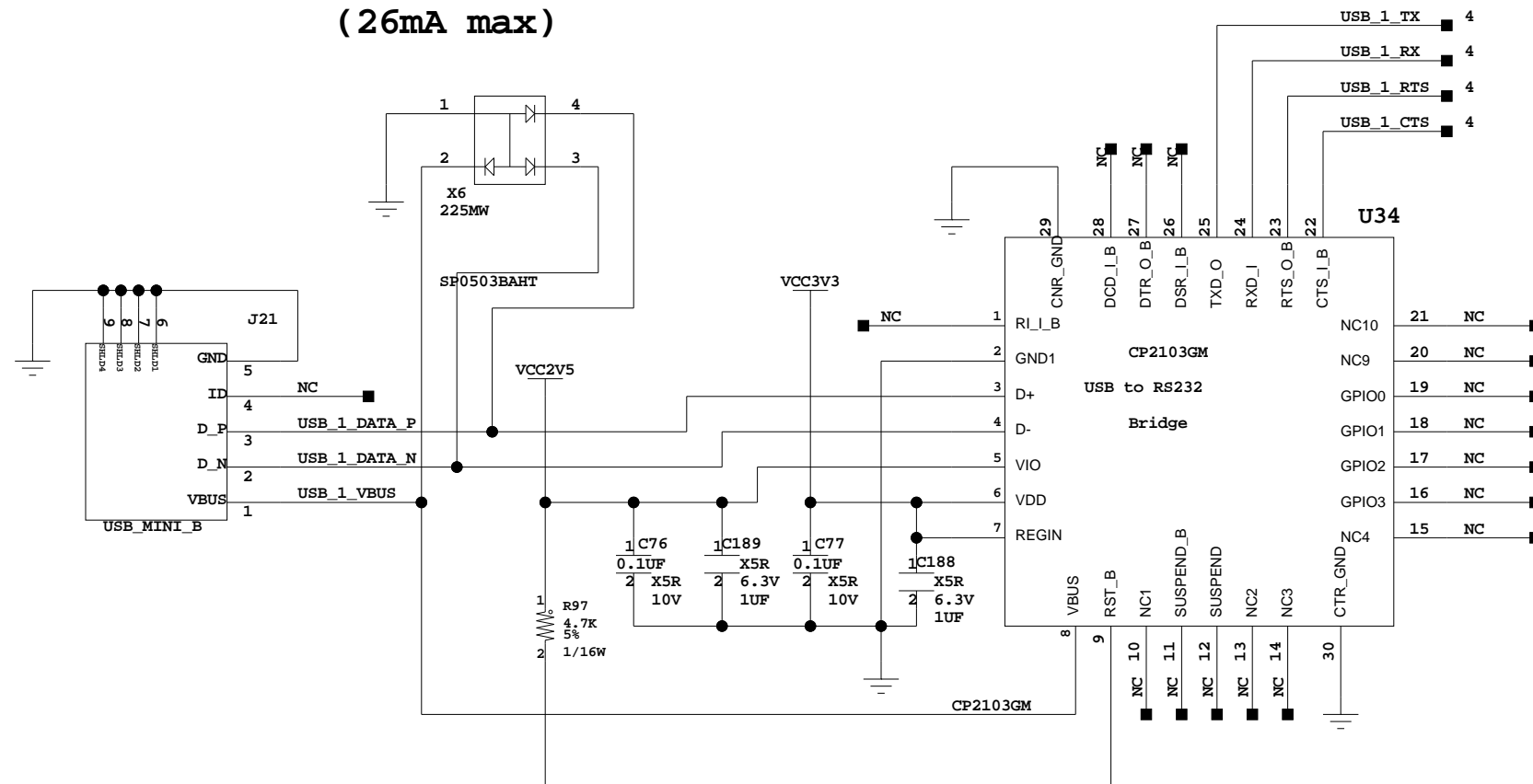


Misc - LCD, Level Shifters



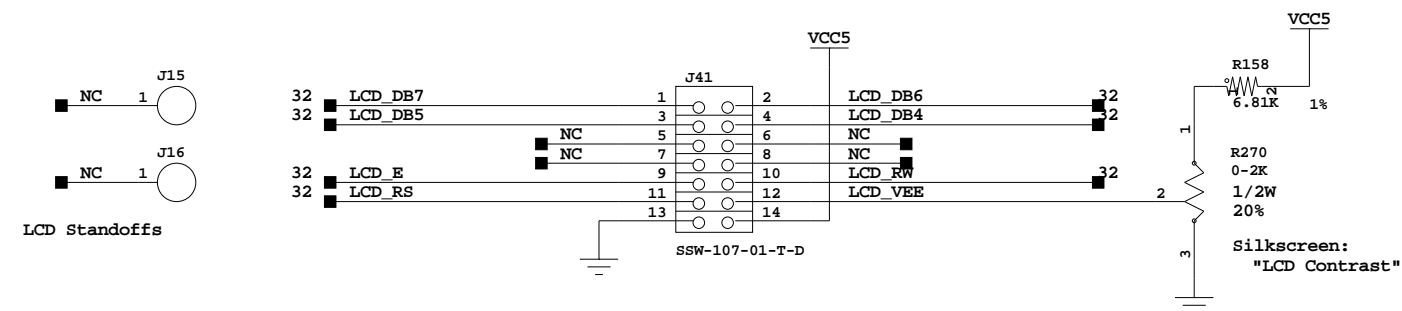
| | | |
|--|-------------|---|
| Title: LCD, Level Shifters SCHEM, ROHS COMPLIANT ML605 | | ASSY P/N: 0431540 PCB P/N: 1280479 SCH P/N: 0381311 |
| Date: 9-24-2009_11:19 | Ver: D | |
| Sheet Size: B | Rev: 04 | |
| Sheet 32 of 48 | Drawn By BF | |

CP2103 USB Self-Powered
(26mA max)



The VIO voltage must match the appropriate bank IO voltage

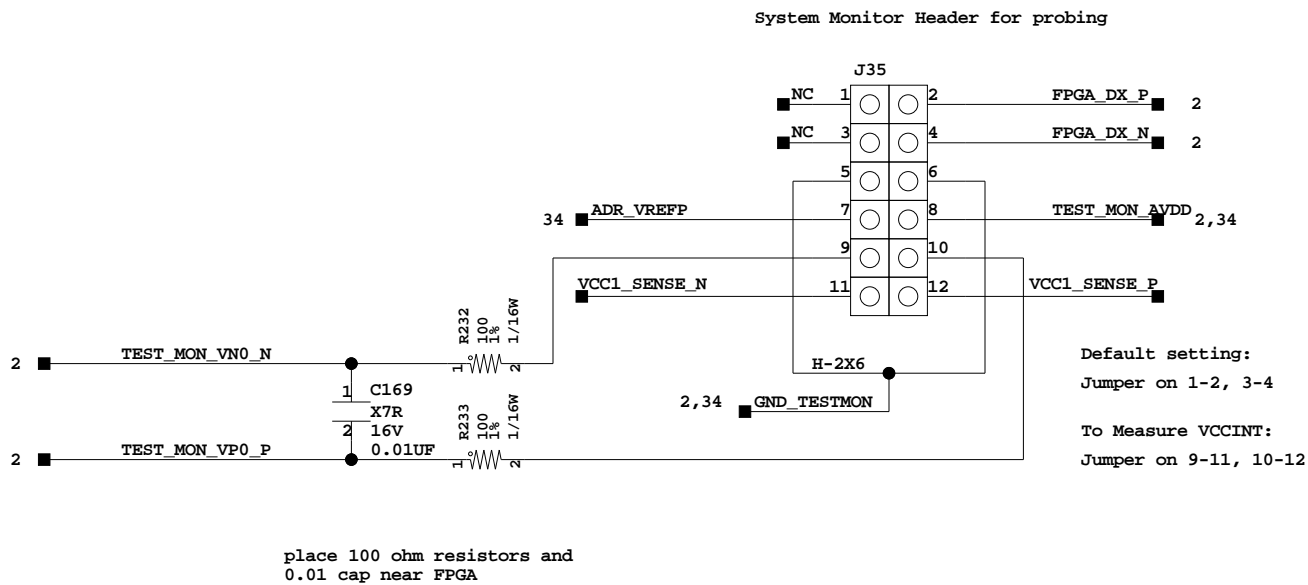
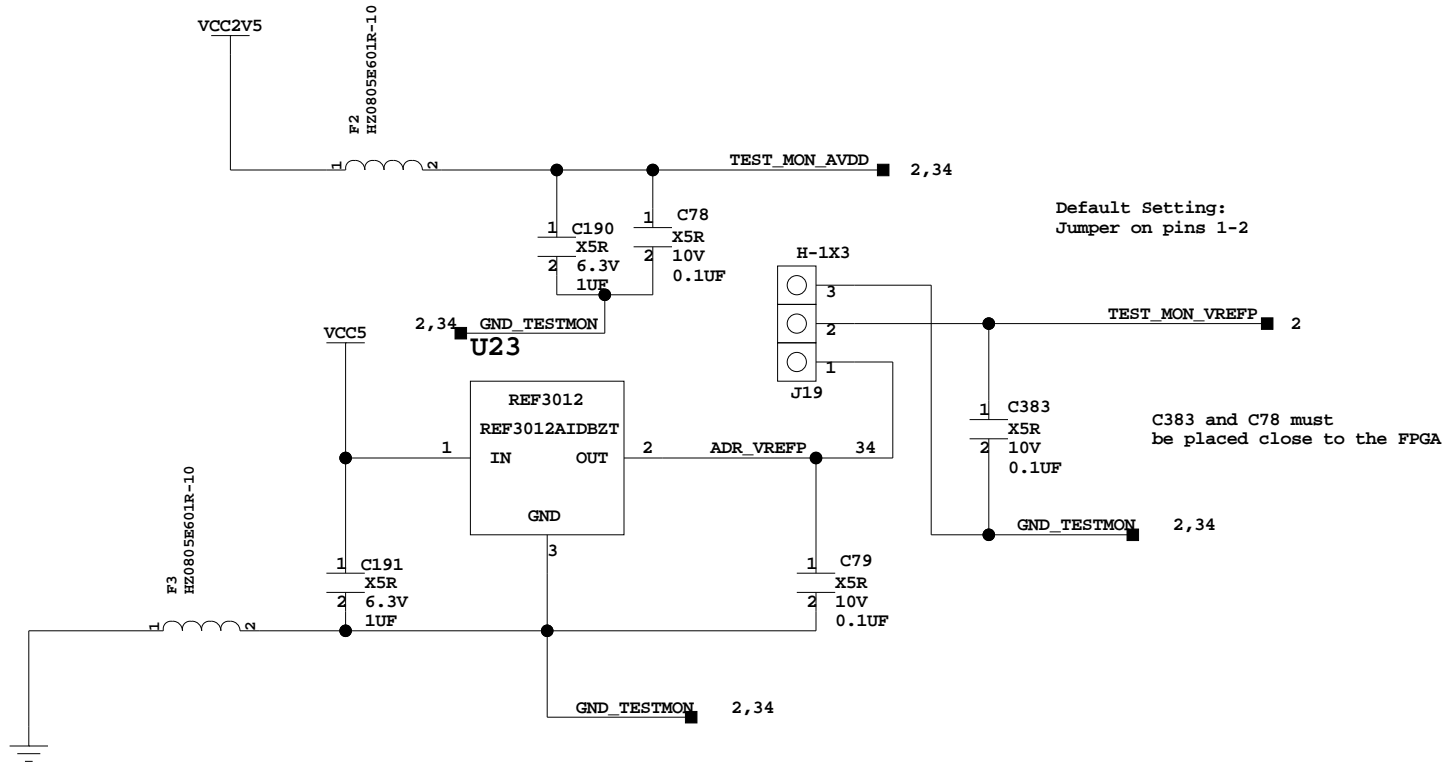
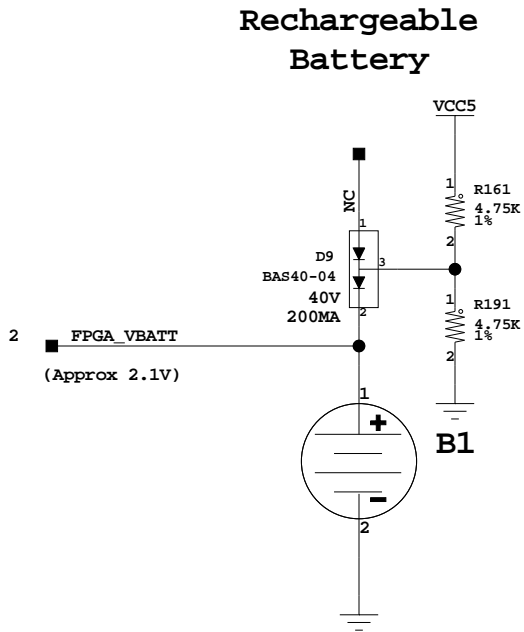
LCD Header



USB UART, LCD Header

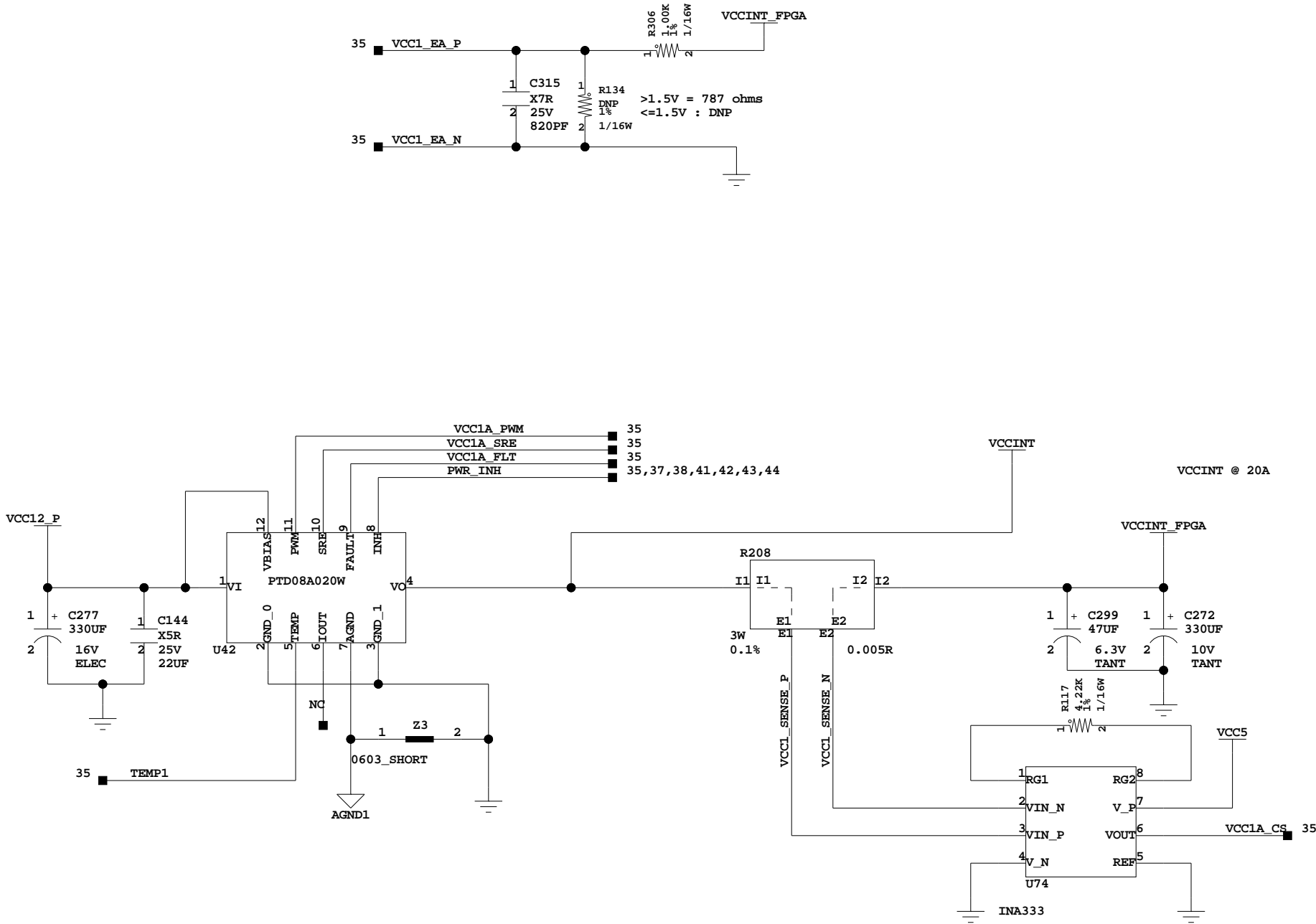


| | | |
|---|--|---|
| Title: SCHEM, ROHS COMPLIANT, USB UART, LCD HEADER | | ASSY P/N: 0431540 PCB P/N: 1280479 SCH P/N: 0381311 |
| Date: 9-17-2009_15:42 | | Ver: D |
| Sheet Size: B | | Rev: 04 |
| Sheet 33 of 48 | | Drawn By BF |




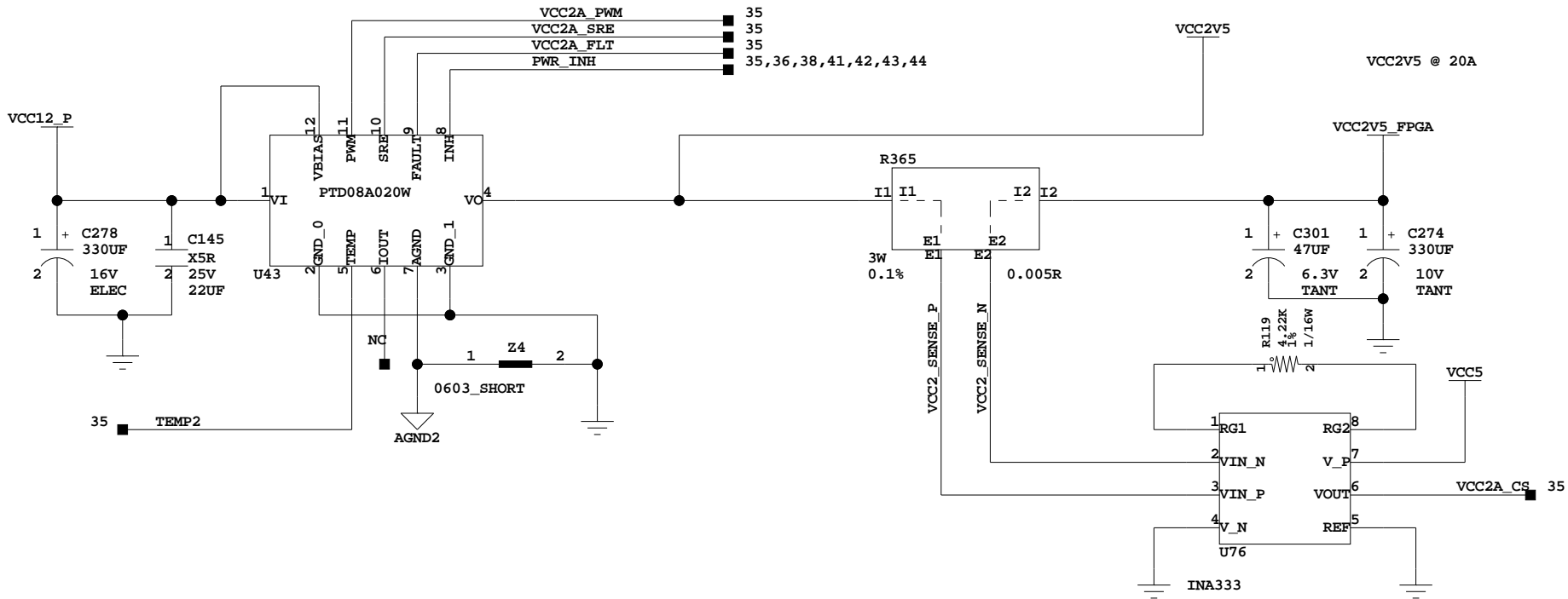
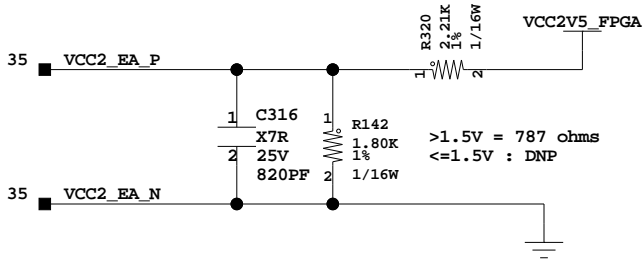
SYSMON HEADER / AVDD VREFP SUPPLY / Battery

| | | | |
|---|-----------------|-------------------|----|
| | | | |
| Title: SCHEM, ROHS COMPLIANT, | | ASSY P/N: 0431540 | |
| SYSMON HEADER / AVDD VREFP SUPPLY / BATTERY | | PCB P/N: 1280479 | |
| | | SCH P/N: 0381311 | |
| Date: | 9-17-2009_15:42 | Ver: | D |
| Sheet Size: | B | Rev: | 04 |
| Sheet | 34 of 48 | Drawn By | BF |



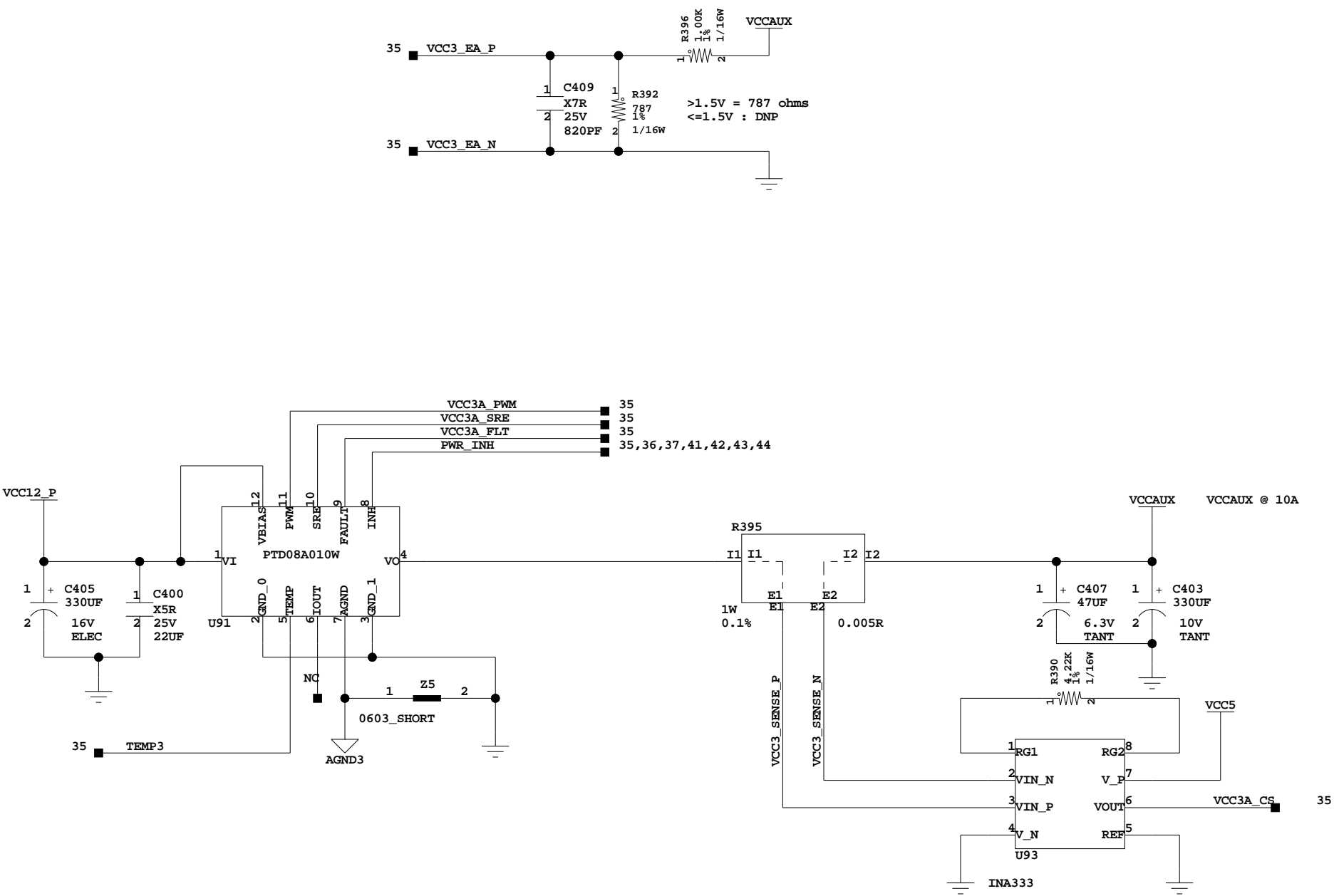
PTD08A020W 20A Max. Power Channel

| | | | |
|---|--|---|--|
|  | | | |
| Title: SCHEM, ROHS COMPLIANT PTD08A020W 20A Max. Power Channel | | ASSY P/N: 0431540 PCB P/N: 1280479 SCH P/N: 0381311 | |
| Date: 9-17-2009_15:42 | | Ver: D | |
| Sheet Size: B | | Rev: 04 | |
| Sheet 36 of 48 | | Drawn By BF | |




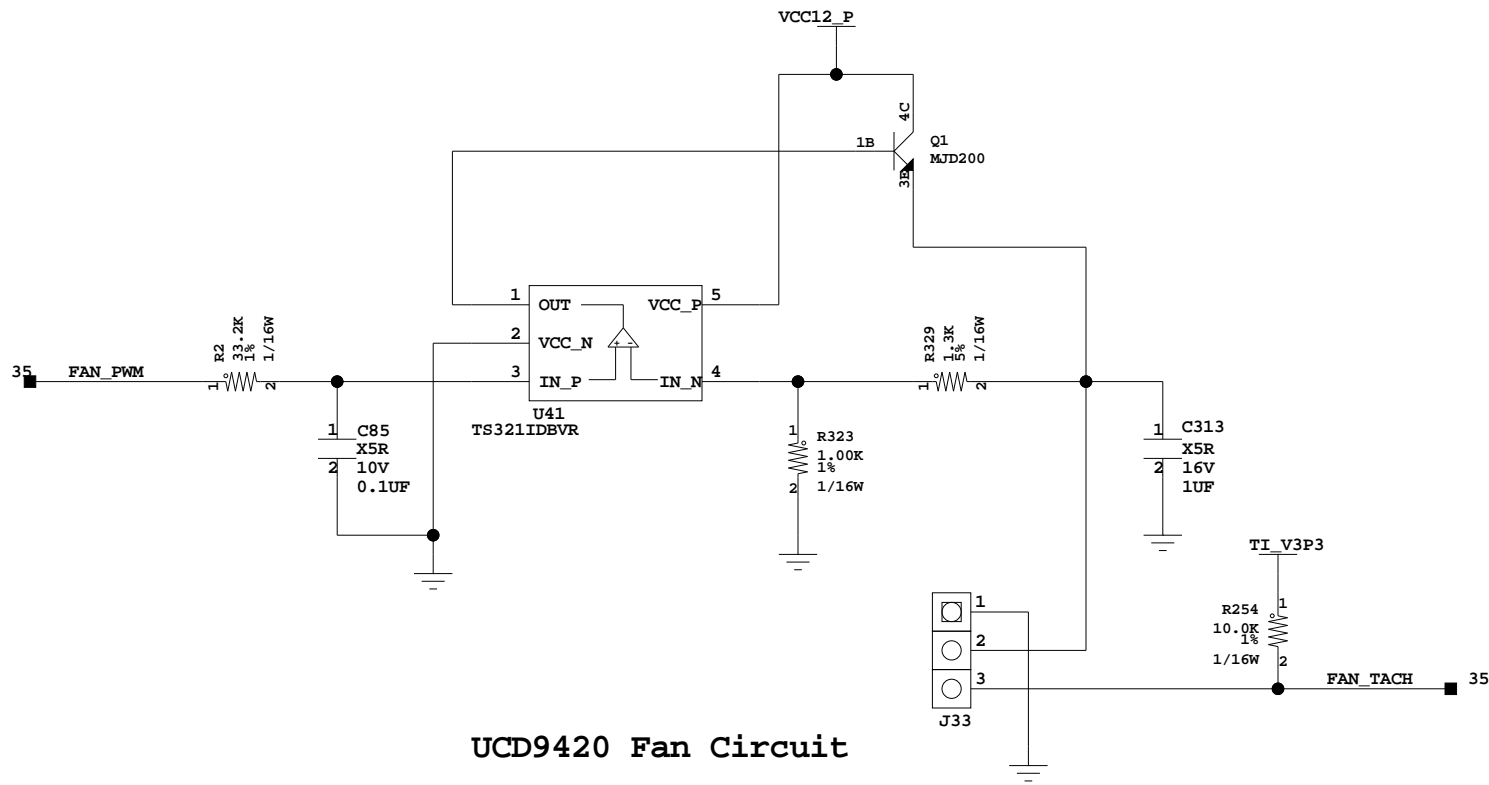
PTD08A020W 20A Max. Power Channel

| | | |
|---|-------------|---|
| Title: SCHEM, ROHS COMPLIANT PTD08A020W 20A Max. Power Channel | | ASSY P/N: 0431540 PCB P/N: 1280479 SCH P/N: 0381311 |
| Date: 9-17-2009_15:42 | Ver: D | |
| Sheet Size: B | Rev: 04 | |
| Sheet 37 of 48 | Drawn By BF | |

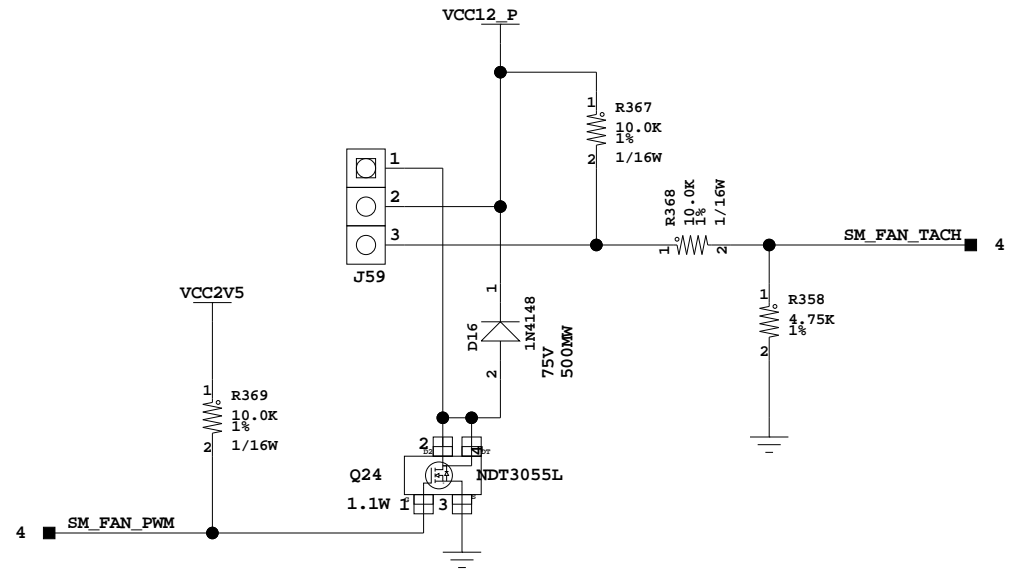


PTD08A010W 10A Max. Power Channel

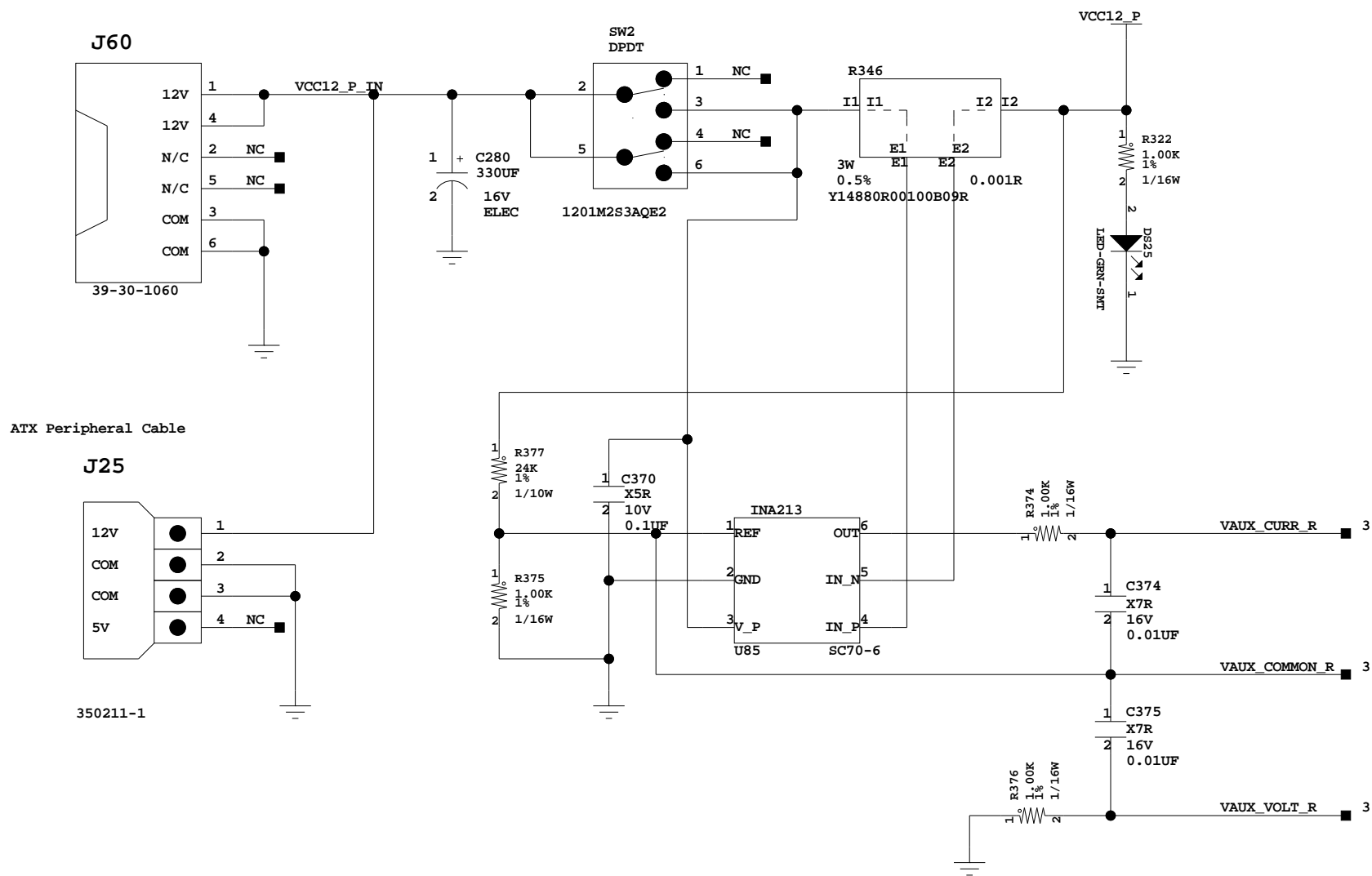
| | | | |
|---|--|---|--|
|  | | | |
| Title: SCHEM, ROHS COMPLIANT PTD08A010W 10A Max. Power Channel | | ASSY P/N: 0431540 PCB P/N: 1280479 SCH P/N: 0381311 | |
| Date: 9-17-2009_15:42 | | Ver: D | |
| Sheet Size: B | | Rev: 04 | |
| Sheet 38 of 48 | | Drawn By BF | |



UCD9420 Fan Circuit



System Monitor Fan Circuit



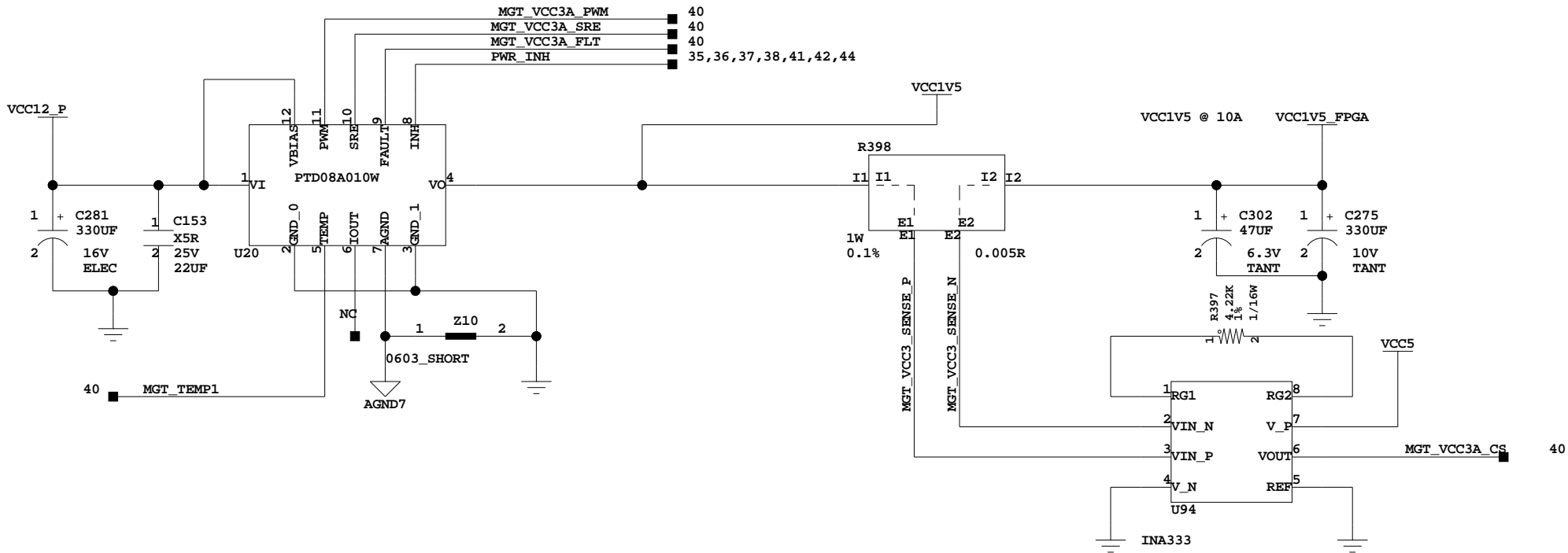
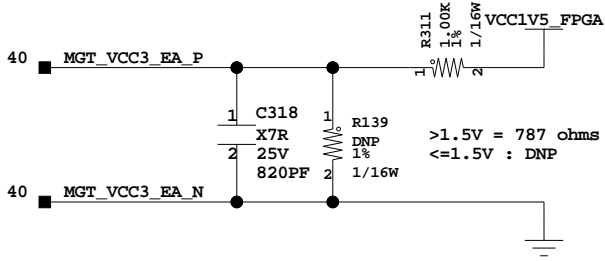
Route VAUX_CURR_R and VAUX_COMMON_R as a 100 ohm differential pair refer to the System Monitor User Guide

Route VAUX_VOLT_R and VAUX_COMMON_R as a 100 ohm differential pair refer to the System Monitor User Guide

12V Power Jacks, 12V Fan

| | | |
|---|-------------|---|
| | | |
| Title: SCHEM, ROHS COMPLIANT TI UCD9240 Power System | | ASSY P/N: 0431540 PCB P/N: 1280479 SCH P/N: 0381311 |
| Date: 10-14-2009_14:48 | Ver: D | |
| Sheet Size: B | Rev: 04 | |
| Sheet 39 of 48 | Drawn By BF | |

| | | | |
|--|--|--|----|
| Title: SCHEM, ROHS COMPLIANT TI UCD9240 Power System | | ASSY P/N: 0431540 PCB P/N: 1280479 SCH P/N: 0381311 | |
| Date: 9-24-2009_11:19 | | Ver: | D |
| Sheet Size: B | | Rev: | 04 |
| Sheet 40 of 48 | | Drawn By BF | |



PTD08A010W 10A Max. Power Channel



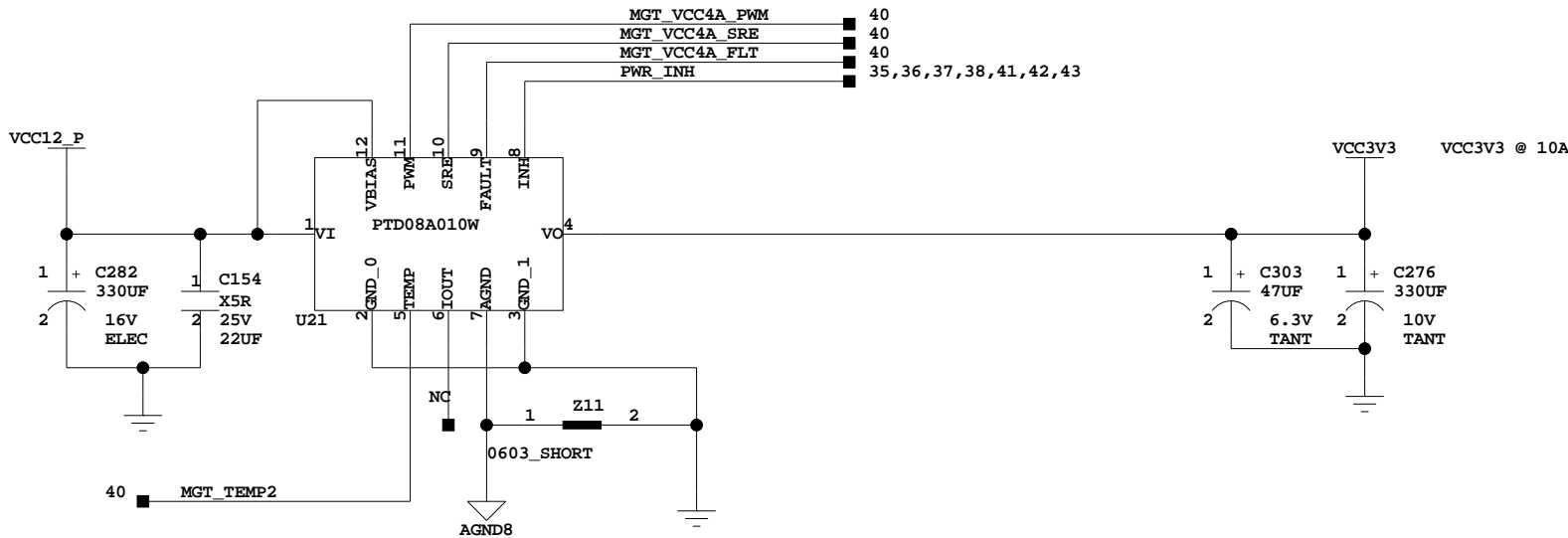
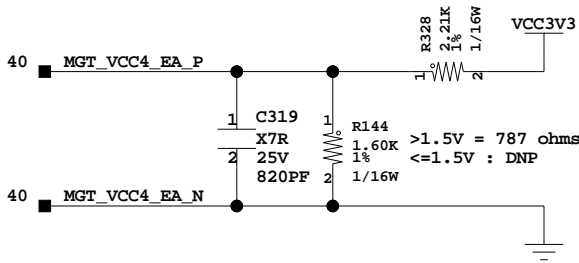
Title: SCHEM, ROHS COMPLIANT
PTD08A010W 10A Max. Power Channel

ASSY P/N: 0431540
PCB P/N: 1280479
SCH P/N: 0381311

Date: 9-17-2009_15:42 Ver: D

Sheet Size: B Rev: 04

Sheet 43 of 48 Drawn By BF



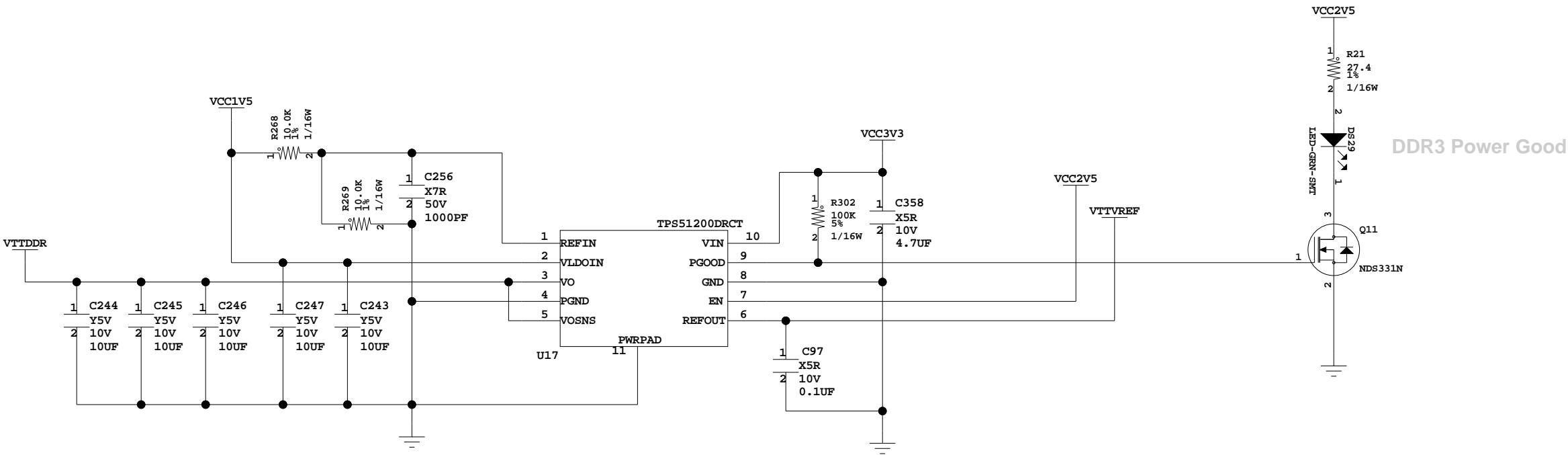
PTD08A010W 10A Max. Power Channel



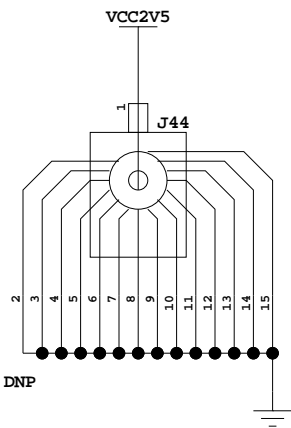
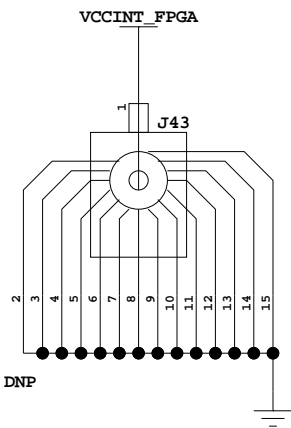
Title: SCHEM, ROHS COMPLIANT
PTD08A010W 10A Max. Power Channel

ASSY P/N: 0431540
PCB P/N: 1280479
SCH P/N: 0381311

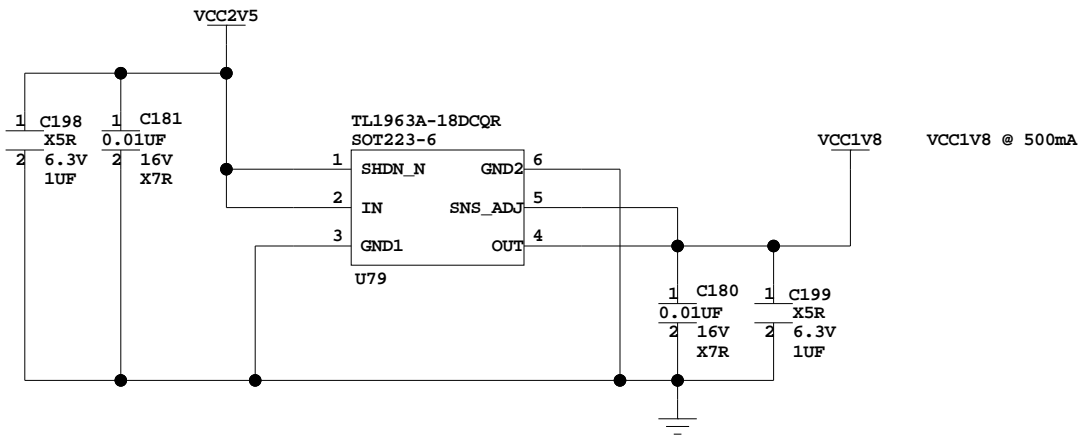
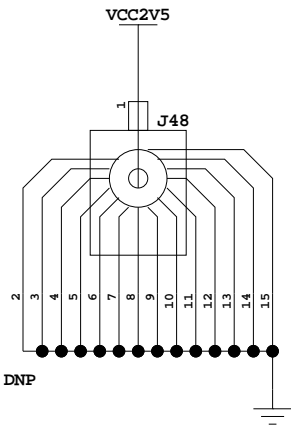
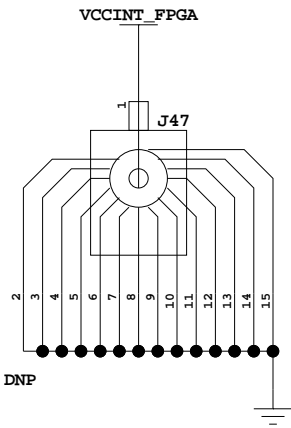
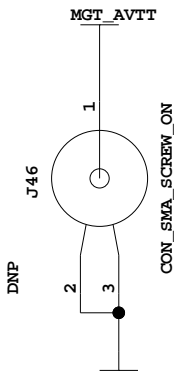
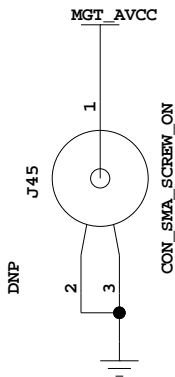
| | | | |
|-------------|-----------------|----------|----|
| Date: | 9-17-2009_15:42 | Ver: | D |
| Sheet Size: | B | Rev: | 04 |
| Sheet | 44 of 48 | Drawn By | BF |



VCCINT_FPGA, VCCAUX Power Probe Channels

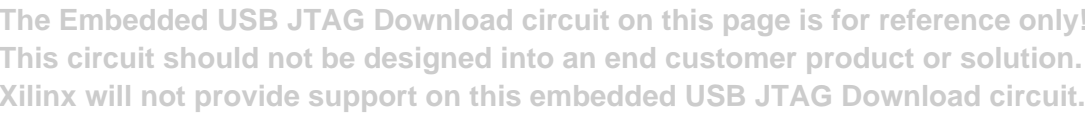


MGT Power Probe Channels



DDR3 Termination Regulator, power probes




| | | | |
|--|-----------------|---|----|
| | | | |
| Title: SCHEM, ROHS COMPLIANT DDR3 Termination Regulator | | ASSY P/N: 0431540 PCB P/N: 1280479 SCH P/N: 0381311 | |
| Date: | 9-17-2009_15:42 | Ver: | D |
| Sheet Size: | B | Rev: | 04 |
| Sheet | 45 of 48 | Drawn By | BF |



| TARGET INTERFACE CONNECTIONS | |
|------------------------------|------------------|
| FROM | TO JTAG |
| FPGA_TCK | TCK ALL DEVICES |
| FPGA_TMS | TMS ALL DEVICES |
| USB_HEADER_TDI | FIRST DEVICE TDI |
| JTAG_TDO | LAST DEVICE TDO |
| EMBEDDED_INIT | NO CONNECTION |

3.3V INTERFACE TO LOCAL JTAG OR SLAVE-SERIAL DEVICE CHAIN
FOR LONG CHAINS OR TRACES, DISTRIBUTE EMBEDDED_TCK
AND EMBEDDED_TMS WITH LVDS BUFFERS.

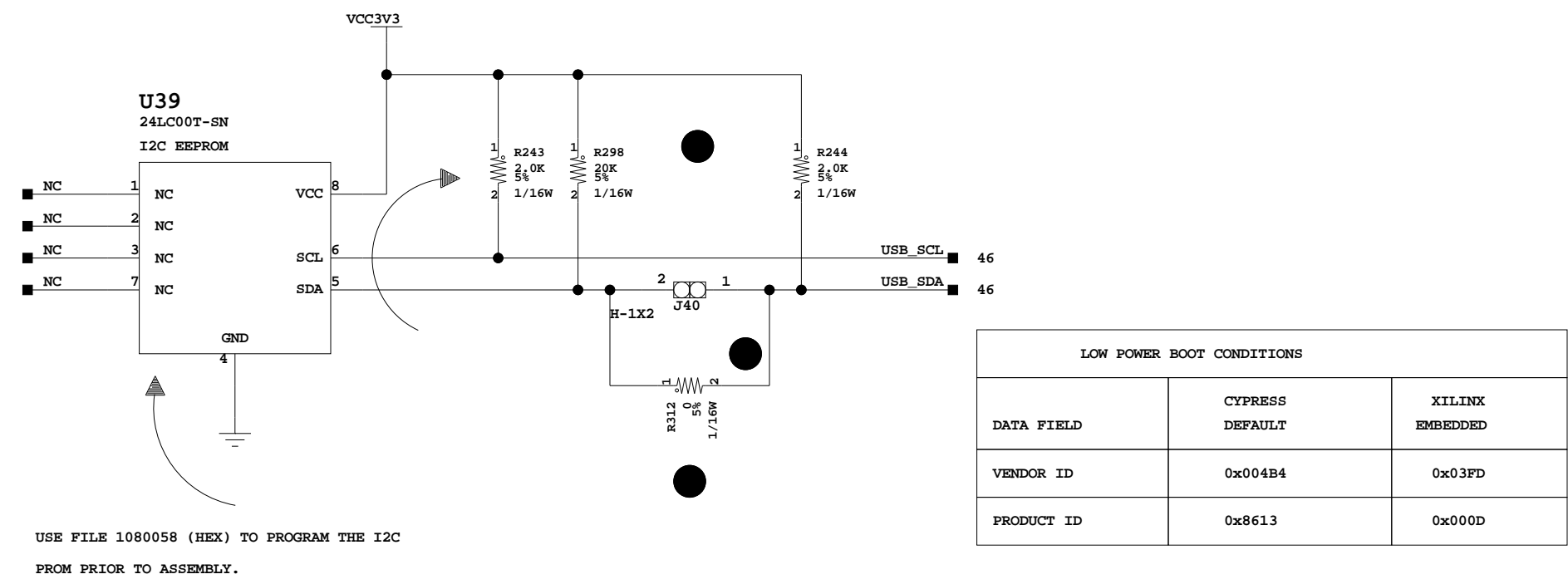
LEGEND:

| | |
|---|---|
|  | OPTIONAL NETS ROUTED IN PARALLEL TO LOCAL 28M CABLE CONNECTOR J1. |
|  | COMPONENTS TO BE LOADED FOR THE PRODUCTION ASSEMBLY VERSION ONLY. |
|  | OPTIONAL COMPONENTS THAT SUPPORT DEBUG AND/OR DIAGNOSTICS. |

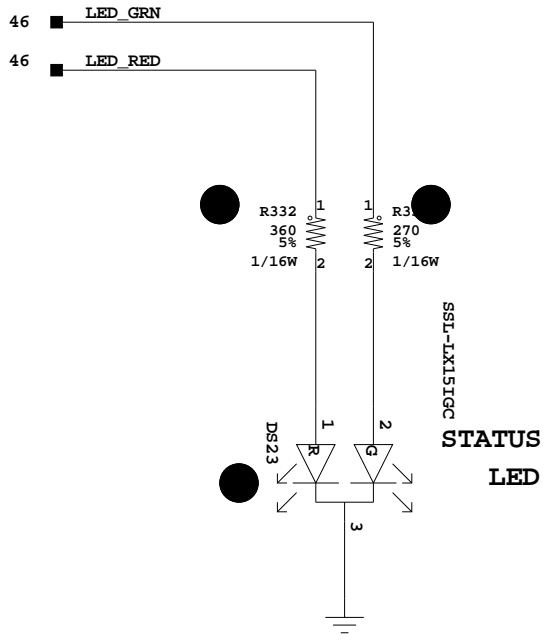
Embedded USB JTAG: USB Controller, CPLD

The Embedded USB JTAG Download circuit on this page is for reference only!
This circuit should not be designed into an end customer product or solution.
Xilinx will not provide support on this embedded USB JTAG Download circuit.

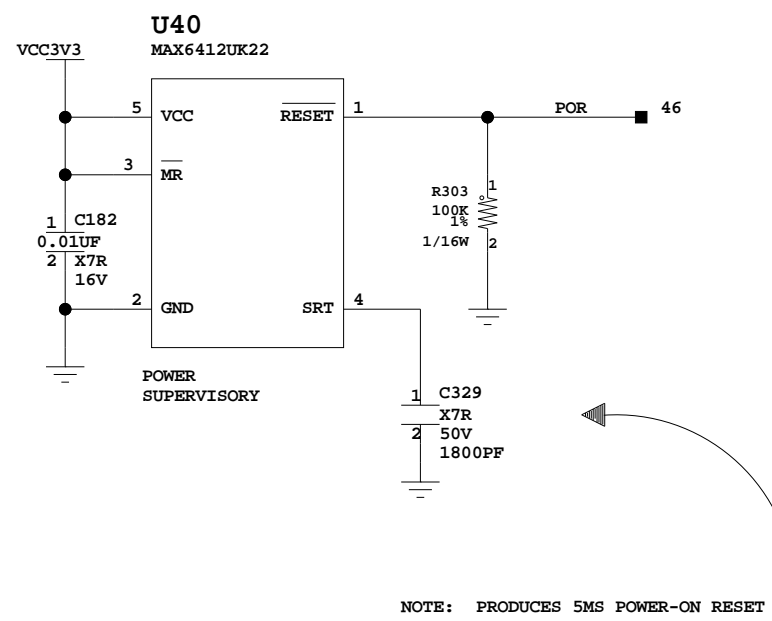
DEFAULT PID/VID EEPROM



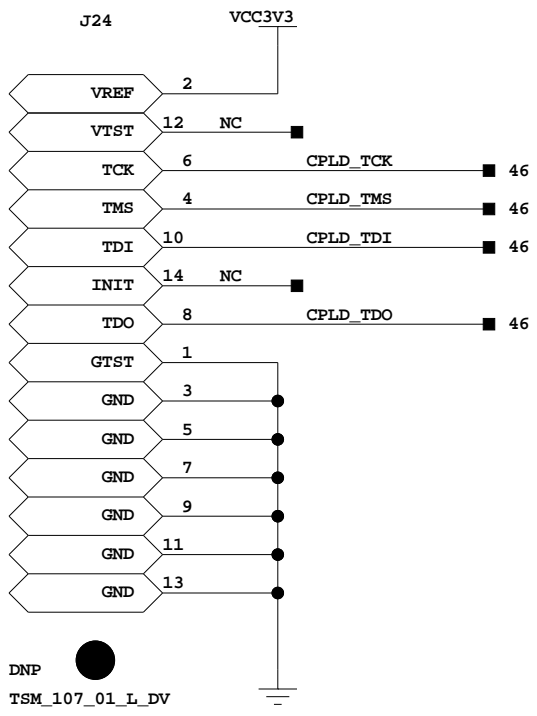
STATUS LEDS (OPTION A)



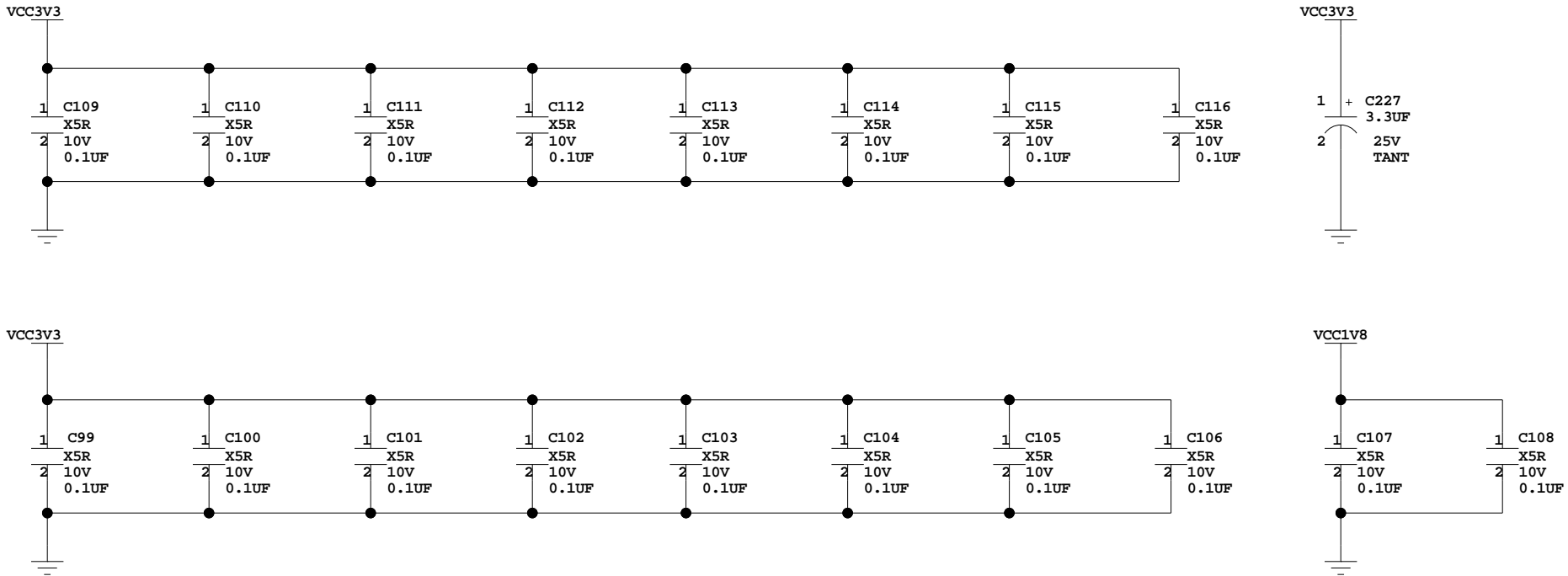
POWER-ON RESET



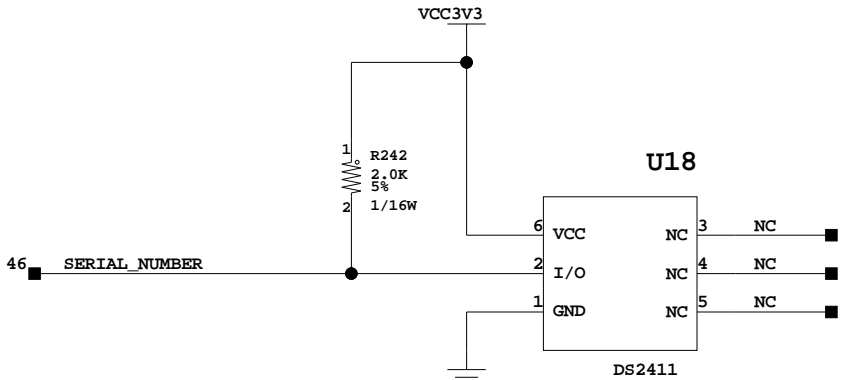
PC4 JTAG CONNECTOR (OPTION B)



BYPASS CAPACITORS



ELECTRONIC SERIAL NUMBER



Embedded USB JTAG: IIC, POR, Decoupling, LED, JTAG Header, Serial Number

ASSY P/N: 0431540
PCB P/N: 1280419
SCH P/N: 0381311

| | | | |
|-----------------|--------------|----------|------------|
| Drawing Number: | | 0381242 | |
| Date: | 14-JUNE-2006 | Ver: | B |
| Sheet Size: | D | Rev: | 04 |
| Sheet | 47 of 48 | Drawn BY | SCHWEIGLER |

LAST REVISION: 9-24-2009_11:19

