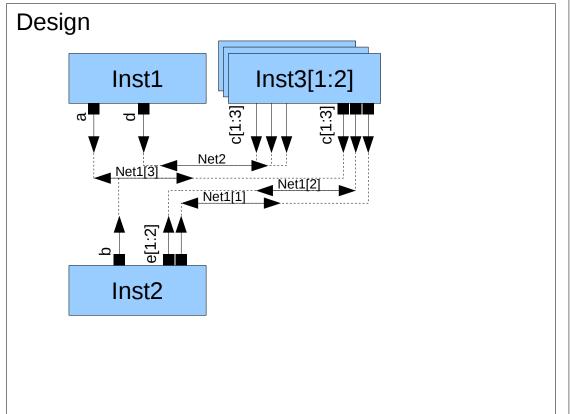
## NetListGenerator Test Case 02



## **Resulting Netlist**

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!PADS-POWERPCB-V9.0-MILS! NETLIST FILE FROM PADS LOGIC V9.3 \*PART\*

A1 DEVICE1@package1

B1 DEVICE2@package2

C1 DEVICE3@package3

C2 DEVICE3@package3

\*CONNECTION

\*SIGNAL\* NET2

A1.2 C1.8

C1.8 C1.9

C1.9 C1.10

\*SIGNAL\* NET1[3]

A1.1 B1.2

B1.2 C2.8

\*SIGNAL\* NET1[2]

B1.1 C2.9

\*SIGNAL\* NET1[1]

B1.3 C2.10

\*END\*

Reference Designations Inst1 A1 Inst2 B1 Inst3(1) C1 Inst3(2) C2	Package Assignments Inst1 package1 Inst2 package2 Inst3(1) package3 Inst3(2) package3	Pin Mappings Inst1.a 1 Inst2.b 2 Inst3(1).c[1] 8 Inst3(1).c[2] 9 Inst3(1).c[3] 10 Inst3(2).c[1] 8 Inst3(2).c[2] 9 Inst3(2).c[3] 10 Inst1.d 2 Inst2.e[1] 1 Inst2.e[2] 3		
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