NetListGenerator Test Case 01

DesignTop

Inst1

Pin1
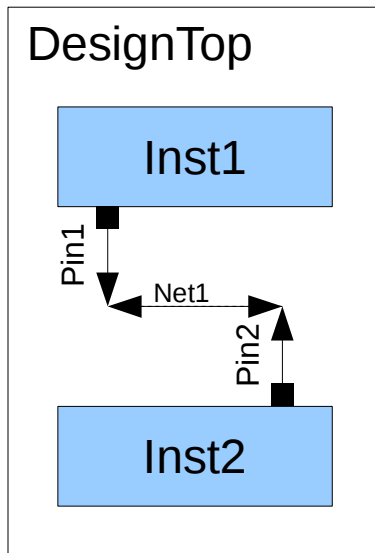
Net1

Pin2

Inst2

Resulting Netlist

!PADS-POWERPCB-V9.0-MILS! NETLIST FILE FROM PADS LOGIC V9.3
PART
  DEVICE1@package1
  DEVICE2@package2
*CONNECTION
SIGNAL NET1
  A1.1, B1.2

END

Reference Designations   Pin Mappings
  Inst1   A1   Inst1.Pin1   1
  Inst2   B1   Inst2.Pin2   2

Package Assignments
  Inst1   package1
  Inst2   package2

Device References
  Inst1   Device1
  Inst2   Device2