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Nios II Qsys microcontrollers

MANUAL

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List of Abbreviations

fifo first in, first out

FPGA Field Programmable Gate Array

Gbps Giga bits per second

H2P HIBI to PC

HDL Hardware Design Language

HIBI Heterogeneous IP Block Interconnect

HW Hardware

ID Identification

I/O Input / Output

IP Intellectual Property

IRQ Interrupt Request

P2H PC to HIBI

PC Personal Computer

SoC System-on-Chip

SW Software

tbd to be decided

TLP Transaction Layer Protocol

TUT Tampere University of Technology

VHDL VHSIC Hardware Description Language

VHSIC Very High Speed Integrated Circuit

# Identification

Vendor: TTY

Library: ip.hwp.cpu

Name: PCIe\_to\_HIBI

Version: 0.1

Author(s): Juha Arvio

Date created: 04.11.2011

Date last modified: 04.11.2011

# Version history

## Documentation

|  |  |  |  |
| --- | --- | --- | --- |
| Date | Version | Change description | Author |
| 04.11.2011 | 0.1 | Tutorial documentation started | Juha Arvio |

# Using Nios II microcontrollers

The Nios II Qsys microcontrollers must be generated with Altera’s Qsys editor prior to using them in Kactus 2 projects. To generate the necessary verilog files launch Qsys from Quartus by choosing “Tools/Qsys” on the toolbar. Now you can open the corresponding qsys file (for ex. funbase\_ip\_library\trunk\TUT\ip.hwp.cpu\nios\_ii\_a2gx\_onchip\1.0\gen\nios2\_a2gx\_onchip.qsys). The qsys project can be generated by pushing the “Generate” button on the Generate section as can be seen on figure .



Figure 3- Qsys generation

After you have successfully generated the source files you can now use the corresponding Nios II microcontroller in your Kactus 2 designs.

# Microcontroller variations

Various pre-made Nios II microcontrollers are available. Each different development board has to have it’s own microcontroller. Exception to this are the Nios II microcontrollers without board specific memory, interface, etc. controllers and use only the FPGA’s internal memory for programs and data. However these microcontrollers have to be created for each type of FPGA.

The Nios II microcontrollers without board specific controllers have the name standard as follows: nios\_ii\_[FPGA family]\_onchip\_[additional definition] (eg. nios\_ii\_a2gx\_onchip\_32kb). Nios II microcontrollers with board specific controllers have the name standard as follows: nios\_ii\_[FPGA board]\_[additional definition] (eg. nios\_ii\_a2gx\_ddr3).

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| FPGA family | name | onchip mem. | jtag |  |
| Arria II GX | a2gx\_onchip | 32kB | - |  |
| a2gx\_onchip\_debug | 32kB | x |  |
| Cyclone II | c2\_onchip | 8kB | - |  |
| c2\_onchip\_debug | 8kB | x |  |

Table 4- FPGA family specific Nios II microcontrollers

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| FPGA board | name | ext. mem. | jtag |  |
| Arria II GX | a2gx\_ddr3 | 128MB DDR3 | - |  |
| DE2 | de2\_dram | 16-bit 8MB DRAM | - |  |

Table - FPGA board specific Nios II microcontrollers