COMPARC **February 25, 2015**
Problem Set #3 **Prof. RLUy**

I. MIPS64 sequential execution tracing: Shown below is a snapshot of the memory and some registers. Show the contents of the internal registers after every cycle for all the instructions. The first cycle is already shown below. Assume: PC = 0000000000000000 and COND= 0

100F	55
100E	44
100D	33
100C	22
100B	11
100A	EF
1009	CD
1008	AB
1007	89
1006	67
1005	45
1004	23
1003	01
1002	EF
1001	CD
1000	AB

R1 :	0000 0000 0000 0002	R2	0000 0000 0000 0008	R3	0000 0000 0000 0004	R4	0000 0000 0000 0000

Instruction	Opcode (Hex)	$IR_{0..5}$	$IR_{6..10}$	$IR_{11..15}$	$IR_{16..31}$
LD R1, 1000(R2)	DC411000	110111	00010	00001	0001 0000 0000 0000
DADDIU R3, R0, #0002	64030002	011001	00000	00011	0000 0000 0000 00010
DADDU R5, R1, R3	0023282D	000000	00001	00011	00101 00000 101101
BNE R5, R0, L1	14A00001	000101	00101	00000	0000 0000 0000 0001
XOR R5, R1, R3	00232826	000000	00001	00011	00101 00000 100110
L1: SD R5, 1000(R4)	FC851000	111111	00100	00101	0001 0000 0000 0000

* Instruction: **LD R1, 1000(R2)**

Cycle:	1	IR =	DC41 1000
		NPC =	0000 0000 0000 0004
Cycle:	2	A =	
		B =	
		IMM =	
Cycle:	3	ALUOUTPUT =	
		COND =	
Cycle:	4	PC =	
		LMD =	
Cycle:	5	R1 =	

*Instruction: **DADDIU R3, R0, #0002**

Cycle:	1	IR =	
		NPC =	
Cycle:	2	A =	
		B =	
		IMM =	
Cycle:	3	ALUOUTPUT =	
		COND =	
Cycle:	4	PC =	
		LMD =	
Cycle:	5		

* Instruction: **DADDU R5, R1, R3**

Cycle:	1	IR =	
		NPC =	
Cycle:	2	A =	
		B =	
		IMM =	
Cycle:	3	ALUOUTPUT =	
		COND =	
Cycle:	4	PC =	
		LMD =	
Cycle:	5		

*Instruction: **BNEZ R5, L1**

Cycle:	1	IR =	
		NPC =	
Cycle:	2	A =	
		B =	
		IMM =	
Cycle:	3	ALUOUTPUT =	
		COND =	
Cycle:	4	PC =	
		LMD =	
Cycle:	5		

* Instruction: **XOR R5, R1, R3 (if needed)**

Cycle:	1	IR =	
		NPC =	
Cycle:	2	A =	
		B =	
		IMM =	
Cycle:	3	ALUOUTPUT =	
		COND =	
Cycle:	4	PC =	
		LMD =	
Cycle:	5		

*Instruction: **SD R5, 1000(R4)**

Cycle:	1	IR =	
		NPC =	
Cycle:	2	A =	
		B =	
		IMM =	
Cycle:	3	ALUOUTPUT =	
		COND =	
Cycle:	4	PC =	
		LMD =	
Cycle:	5		