COMPARC **February 25, 2015**
Problem Set #4 **Prof. RLUy**

I. MIPS pipeline execution tracing: Shown below is a snapshot of the memory and some registers. Show the contents of the internal **pipeline** registers after every cycle for all the instructions. The first cycle is already shown below. Assume: PC = 0000000000000000 and COND= 0

100F	55
100E	44
100D	33
100C	22
100B	11
100A	EF
1009	CD
1008	AB
1007	89
1006	67
1005	45
1004	23
1003	01
1002	EF
1001	CD
1000	AB

R1 :	0000 0000 0000 0002	R2	0000 0000 0000 0008	R3	0000 0000 0000 0004	R4	0000 0000 0000 0005
R5 :	0000 0000 0000 0008	R6	0000 0000 0000 0001	R7	0000 0000 0000 0000	R8	0000 0000 0000 0004

Instruction	Opcode (Hex)	$IR_{0..5}$	$IR_{6..10}$	$IR_{11..15}$	$IR_{16.31}$
LD R1, 1000(R2)	DC411000	110111	00010	00001	0001 0000 0000 0000
DADDU R5, R6, R8					
XOR R7, R3, R4					

Cycle 1		
IF	IF/ID.IR =	DC411000
	IF/ID.NPC =	00000004
	PC =	00000004
ID	ID/EX.A =	
	ID/EX.B =	
	ID/EX.IR =	
	ID/EX.IMM =	
	ID/EX.NPC=	
EX	EX/MEM.IR =	
	$EX/MEM.ALU_{Output}$ =	
	EX/MEM.B =	
	EX/MEM.COND =	
MEM	MEM/WB.IR =	
	MEM/WB.LMD =	
	$MEM/WB.ALU_{OUTPUT}$ =	
	$MEM[EX/MEM.ALU_{Output}]$ =	
WB	$REGS[MEM/WB.IR_{11..15}]$ =	
	$REGS[MEM/WB.IR_{16..20}]$ =	