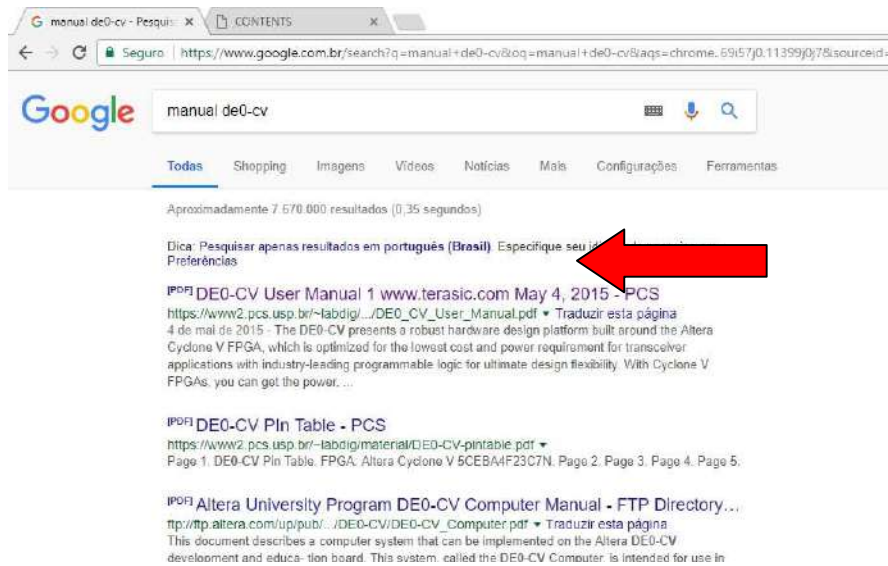
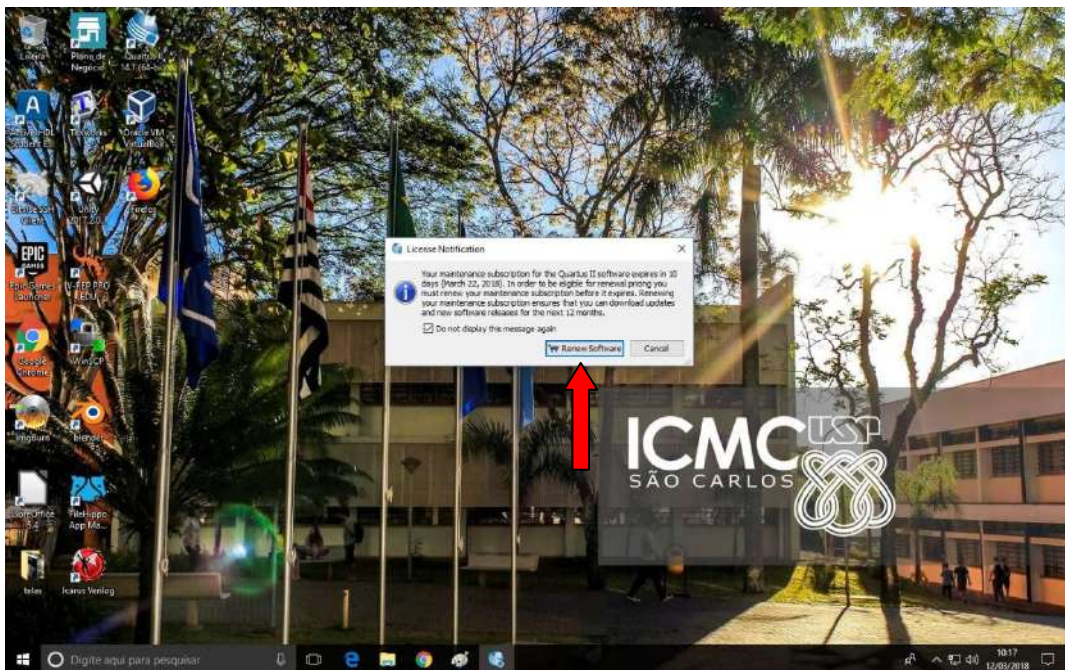


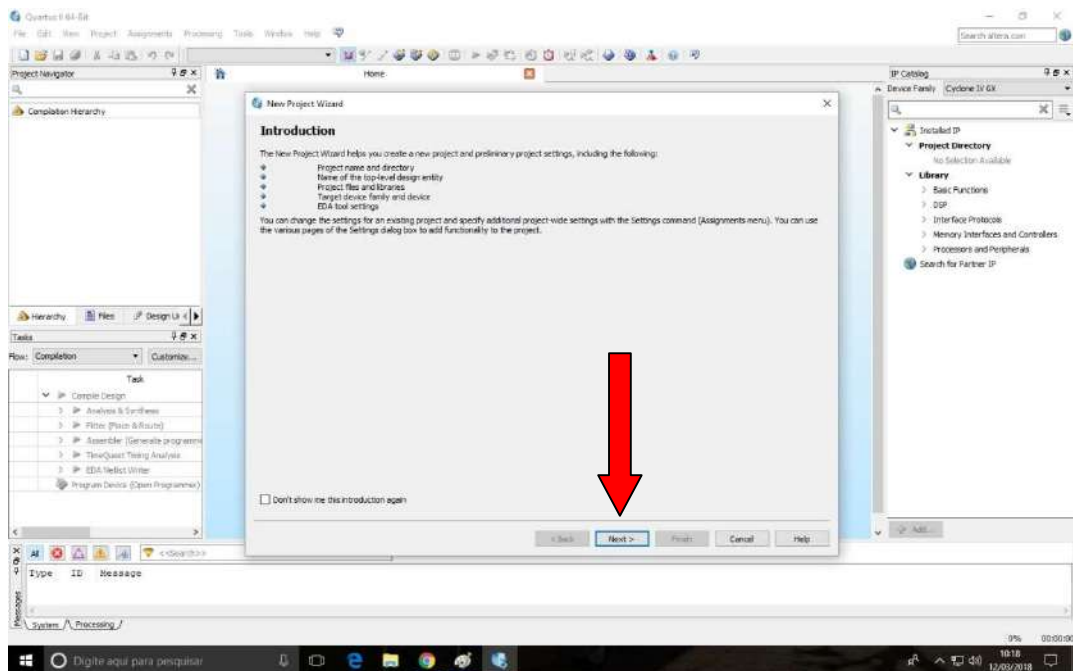
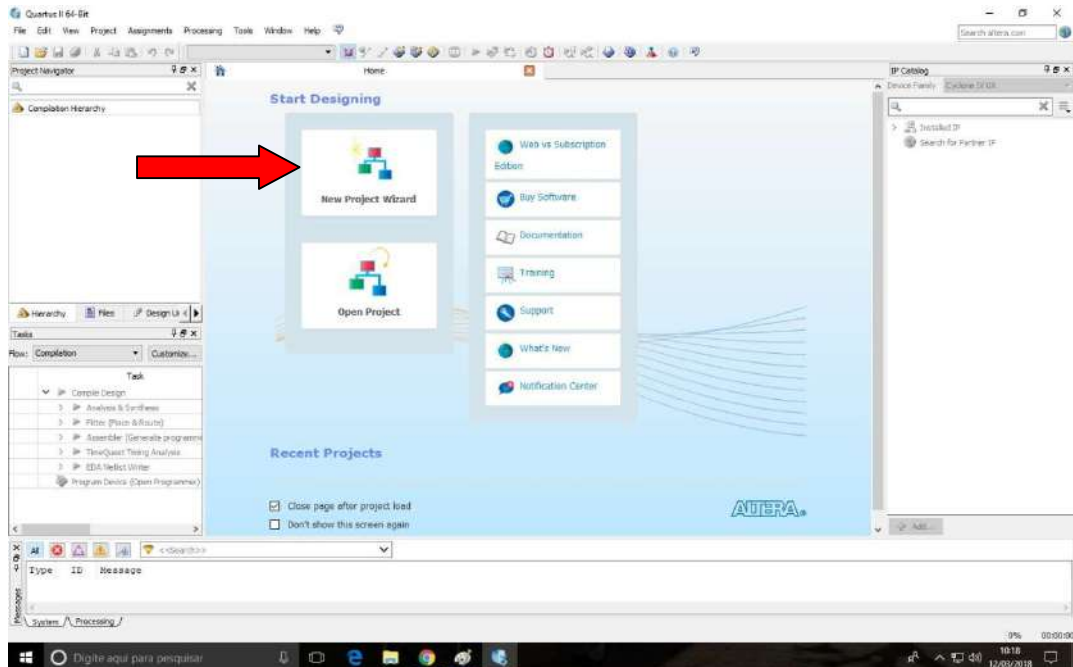
1) Baixar o manual da placa de FPGA usada no laboratório (DE0-CV ou DE2-70)



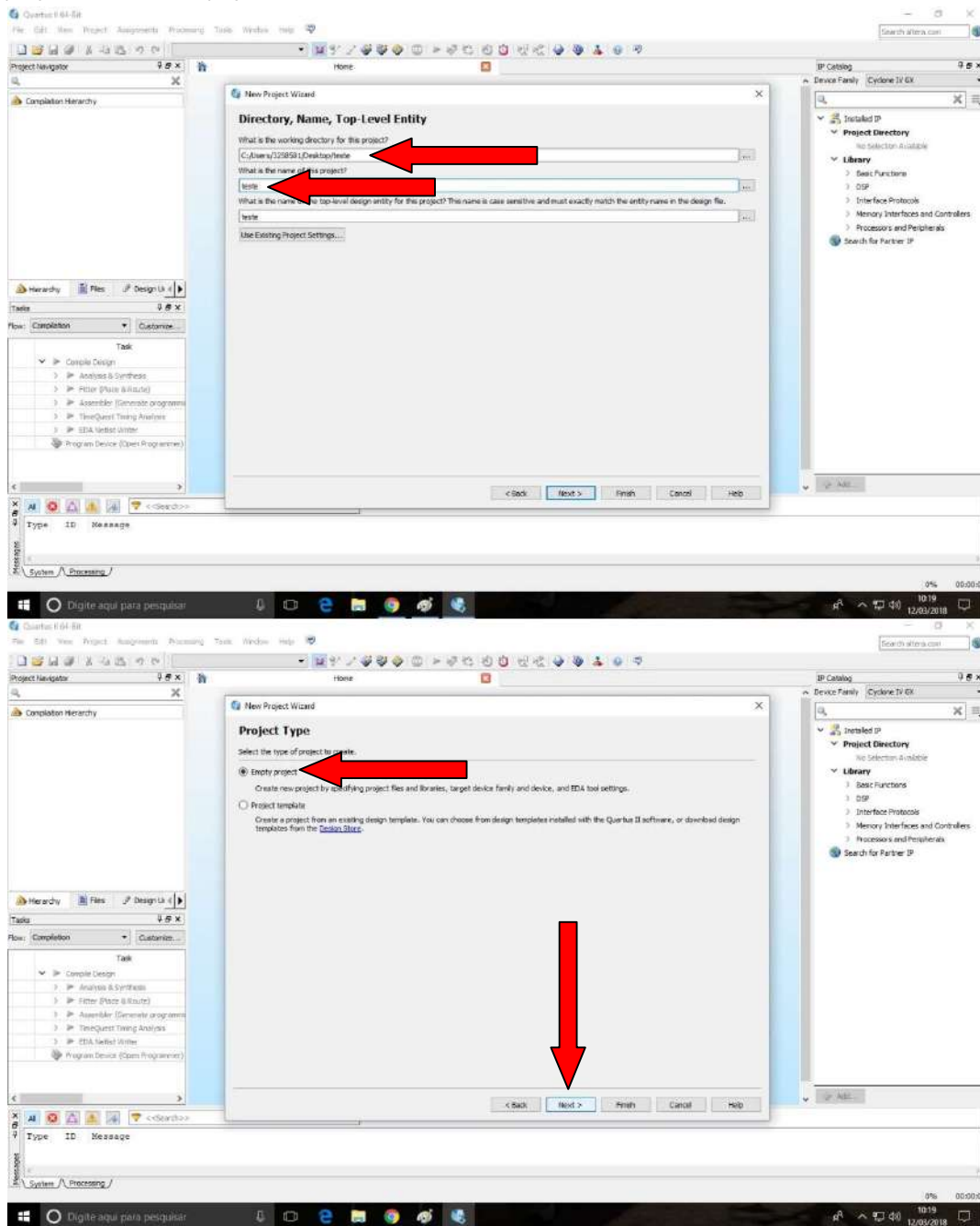
2) Executar o programa Quartus II (64 bits)

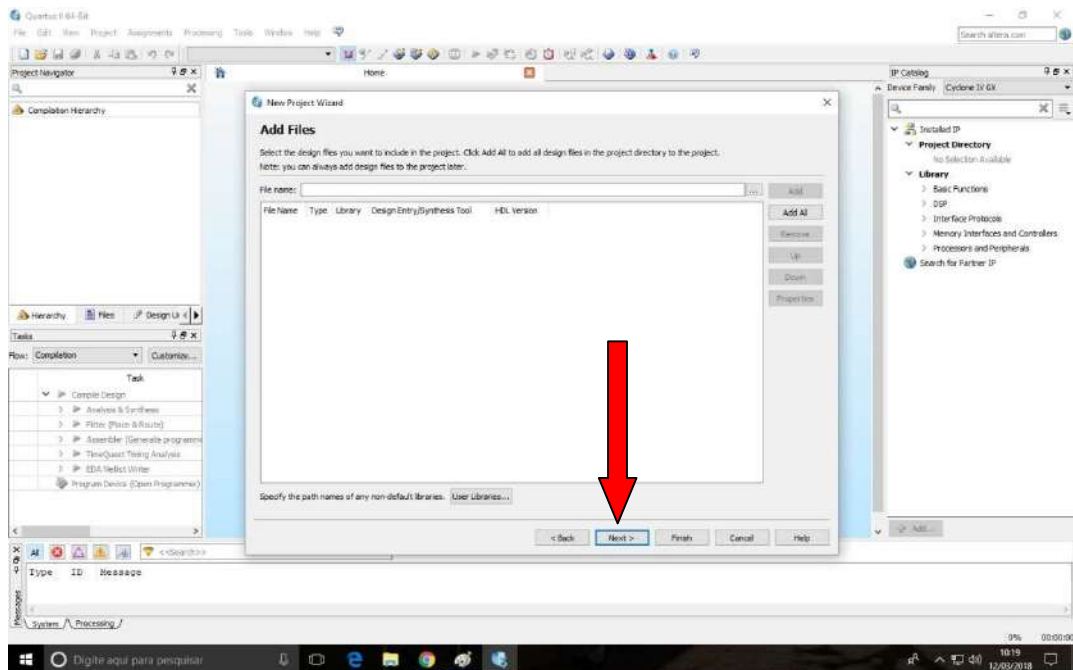


3) Após executar o Quartus II, usar a opção “New Project Wizard”

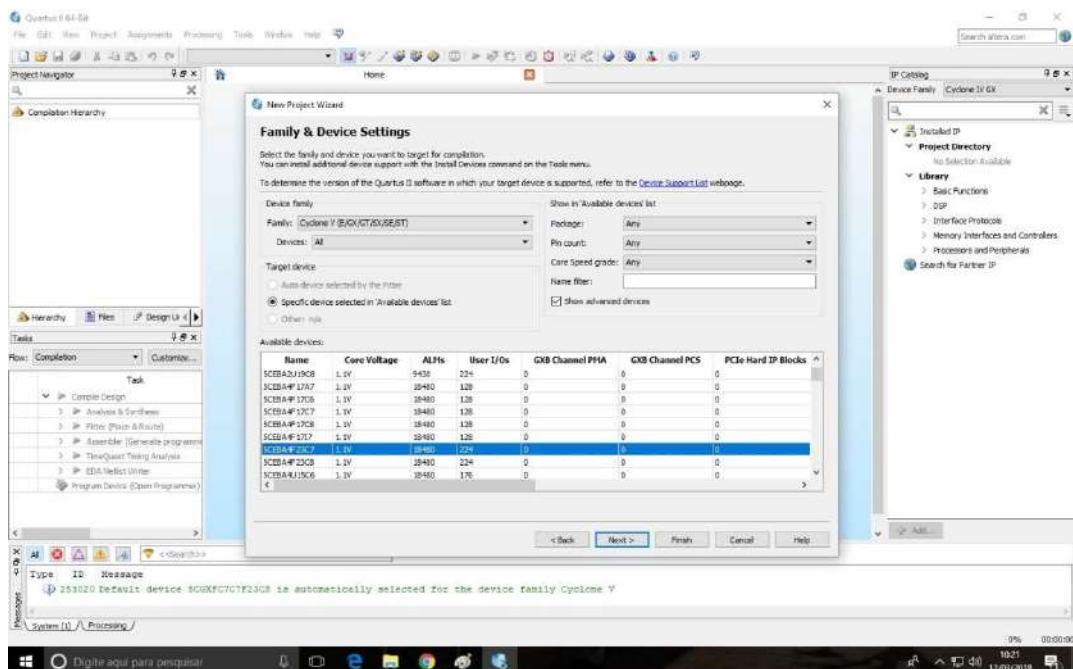


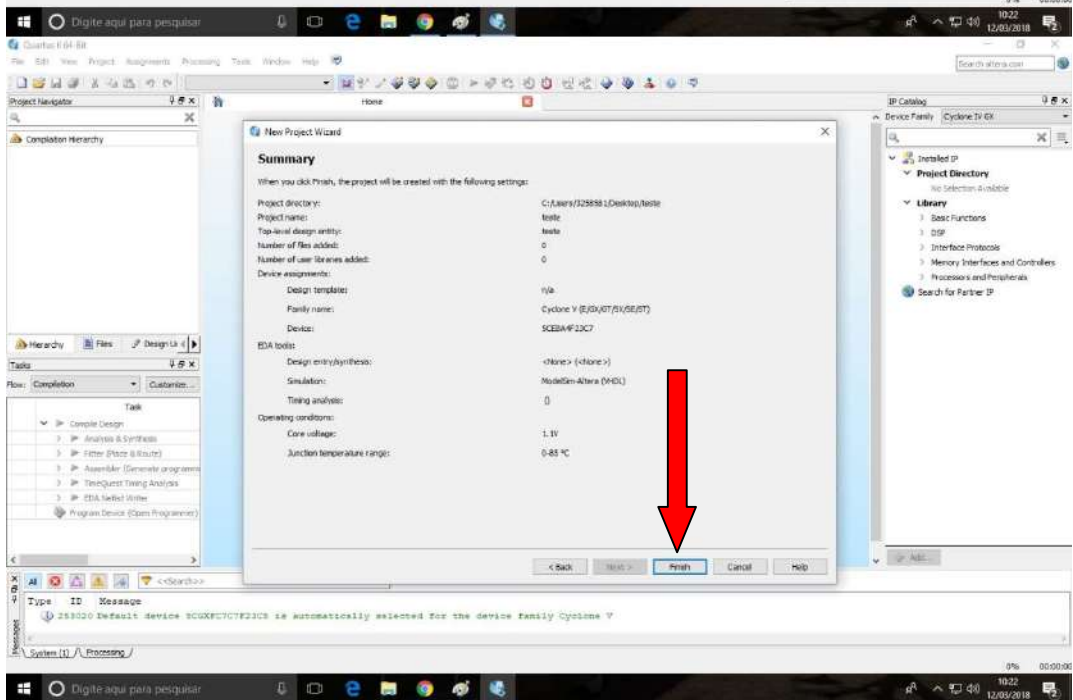
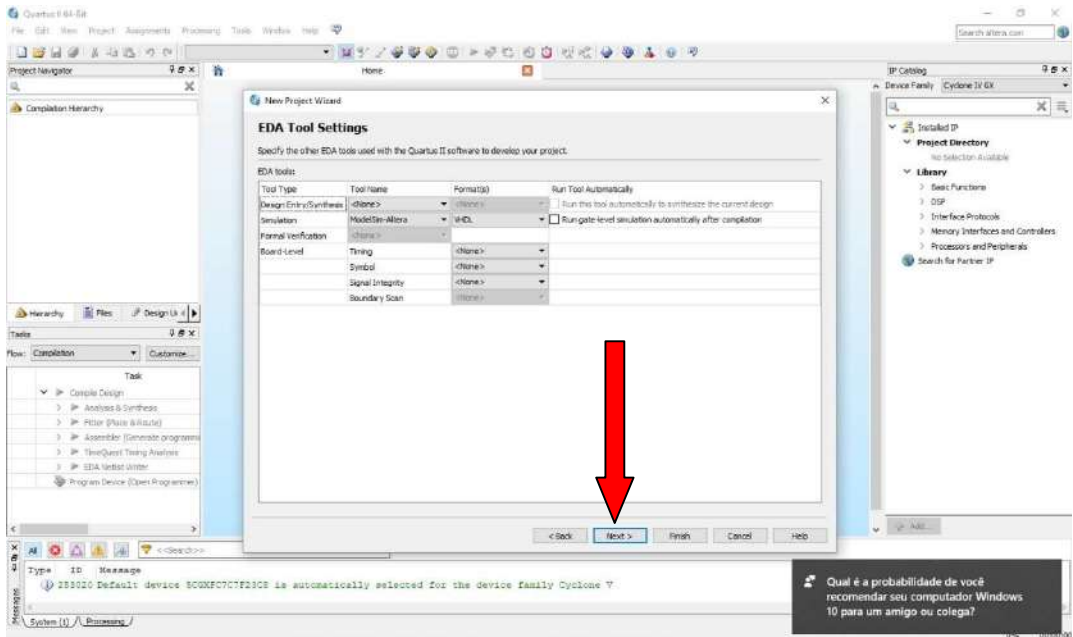
4) Escolha uma pasta na sua área de trabalho para salvar o projeto. Escolha um nome para o projeto usar sem espaços.



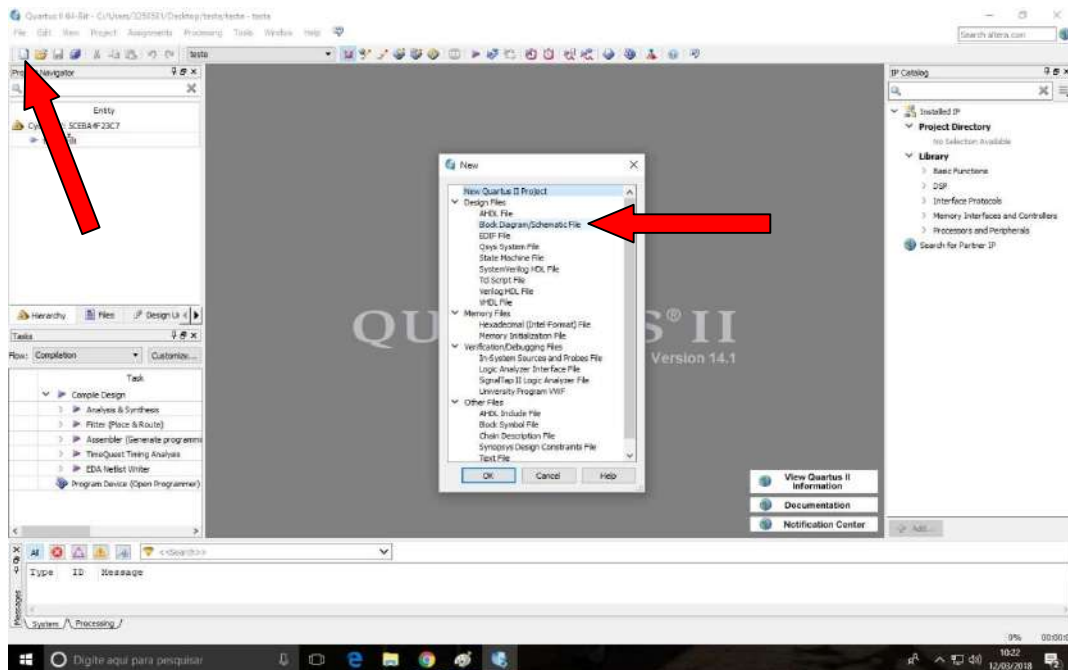


5) Escolha o modelo de FPGA que será utilizado. Nas placas DE0-CV, a família é a Cyclone V e o modelo: 5CEBA4F23C7

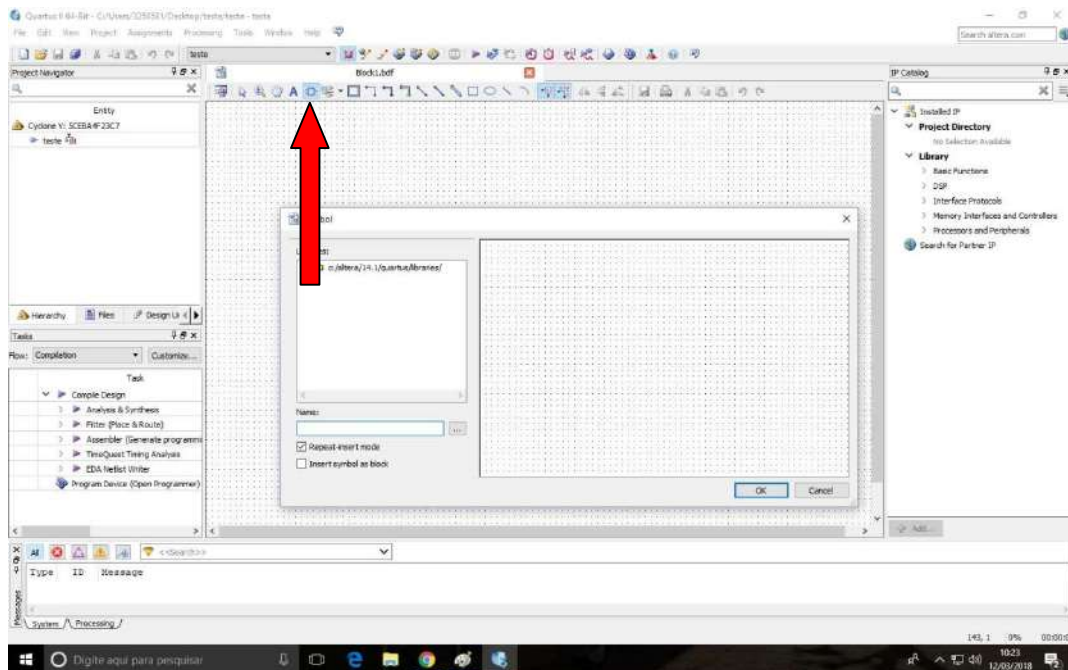




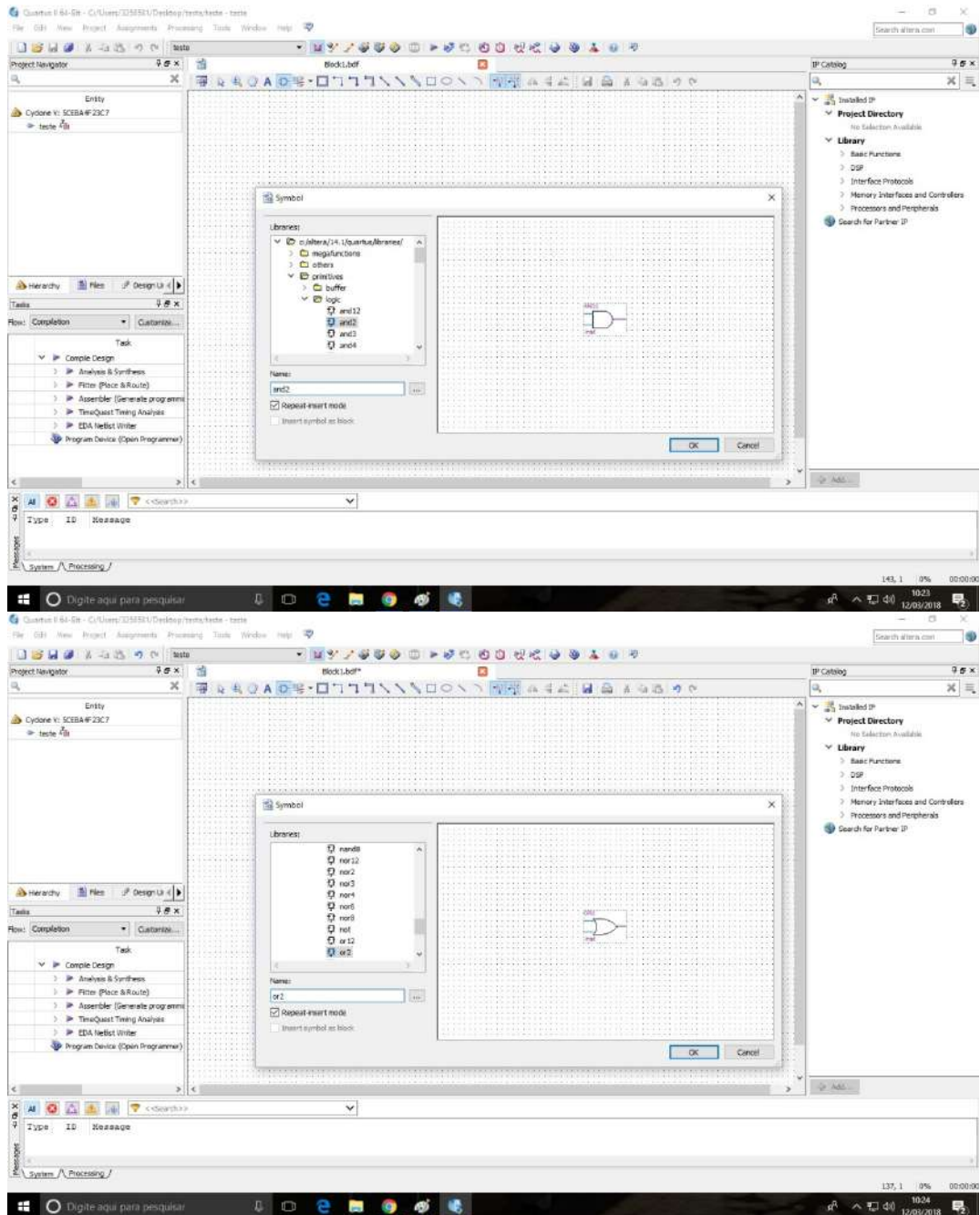
6) Após a criação do projeto use a opção “New File” e escolha “Block Diagram/Schematic File”



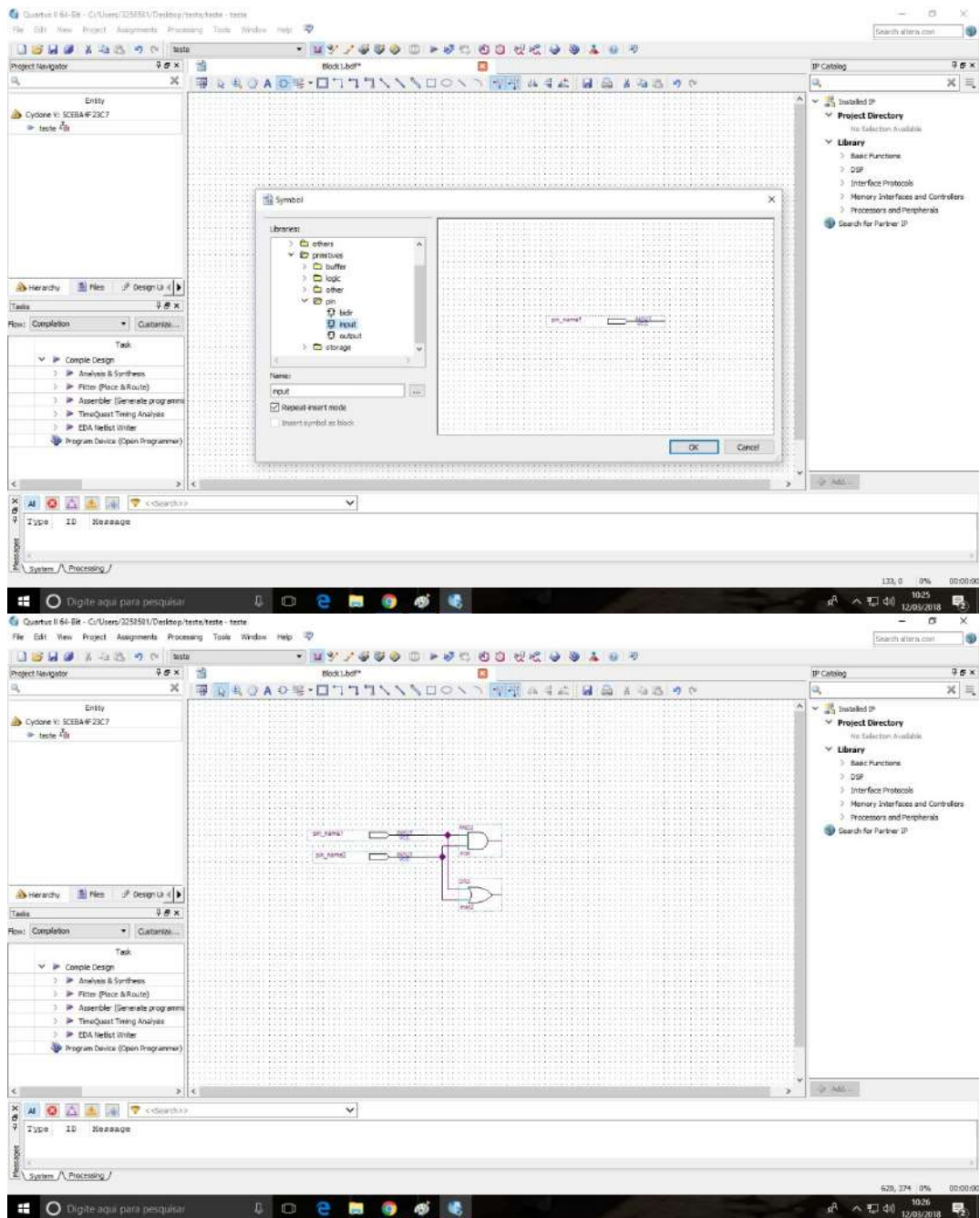
7) Clique na opção “Symbols” do menu.



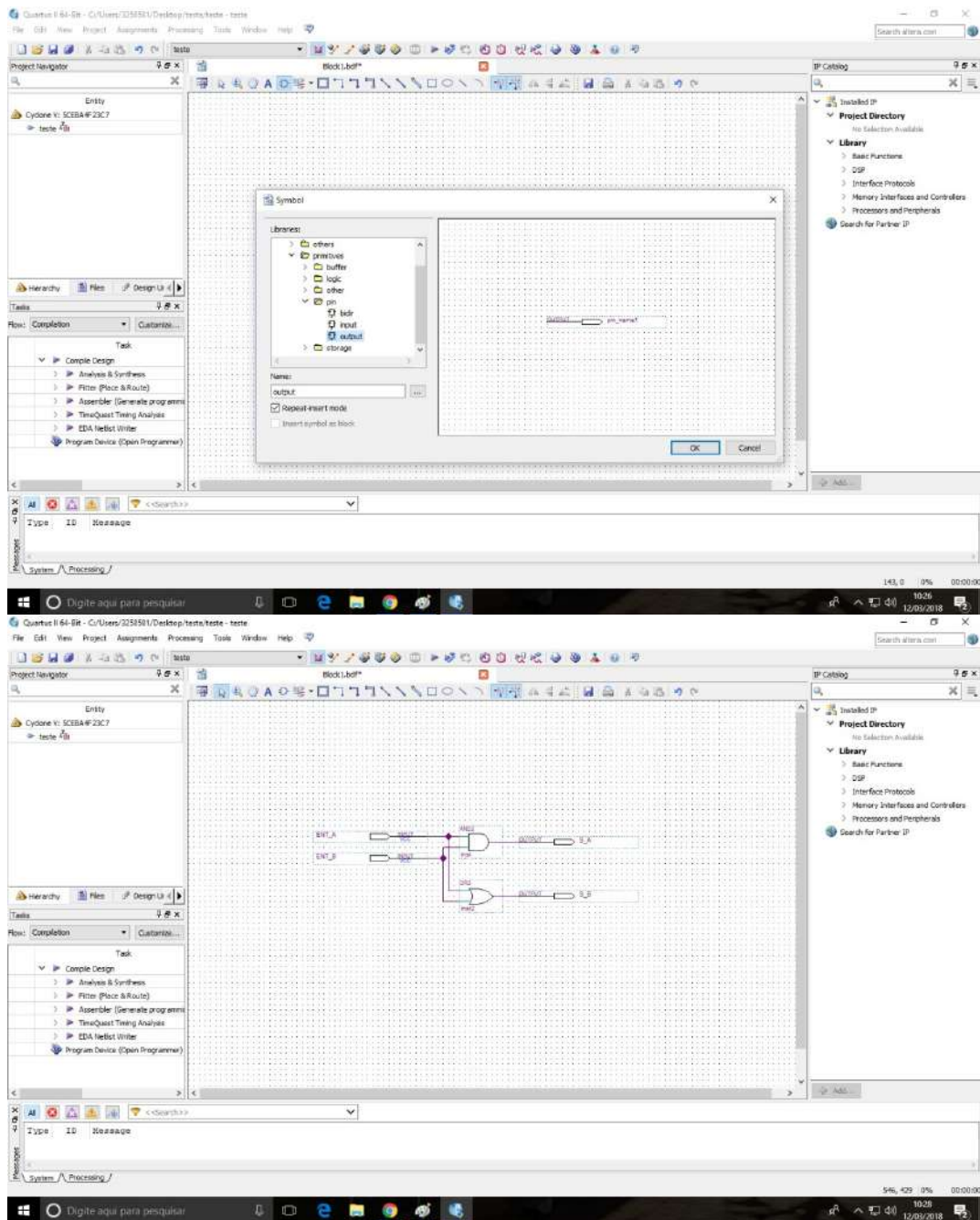
8) Escolha as portas AND2 e OR2, e insira essas portas no diagrama esquemático.



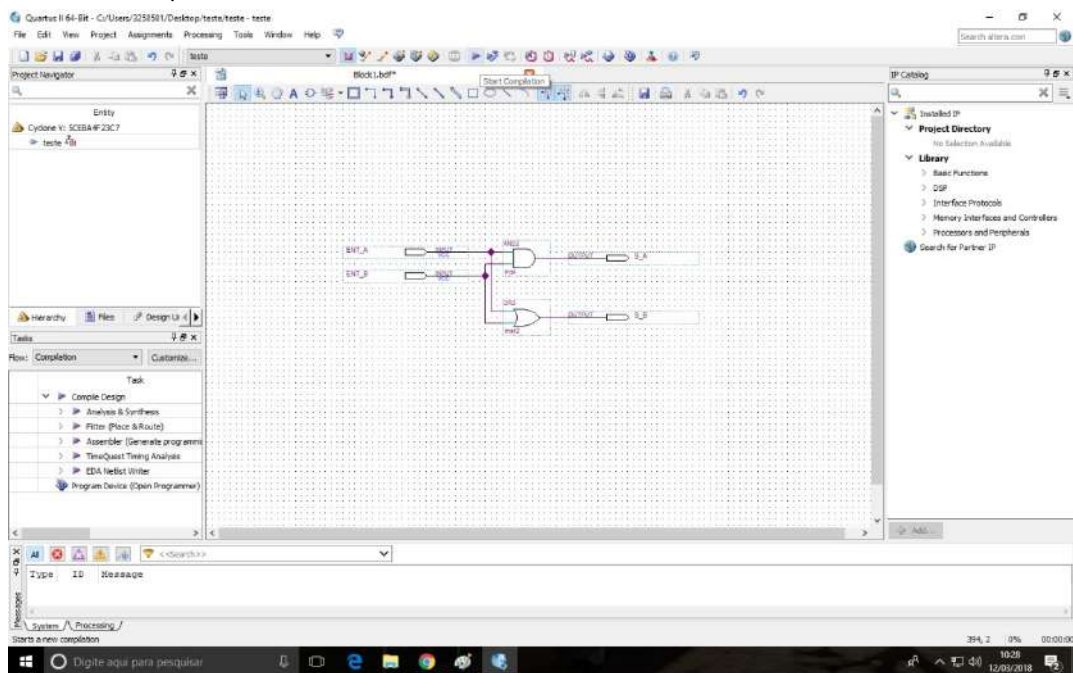
9) Insira 2 componentes do tipo “Input” no projeto e faça as conexões entre os 2 terminais “Input” e as entradas das 2 portas lógicas.



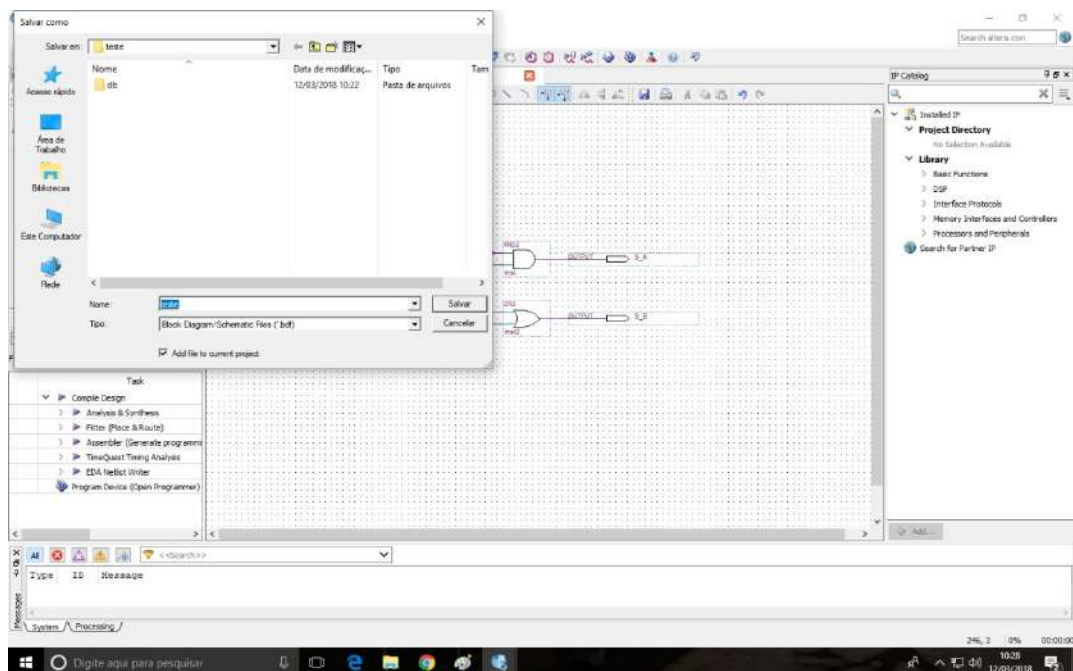
10) Selecione e insira 2 componentes do tipo “Output” no diagrama esquemático, conectando na saída de cada porta lógica.



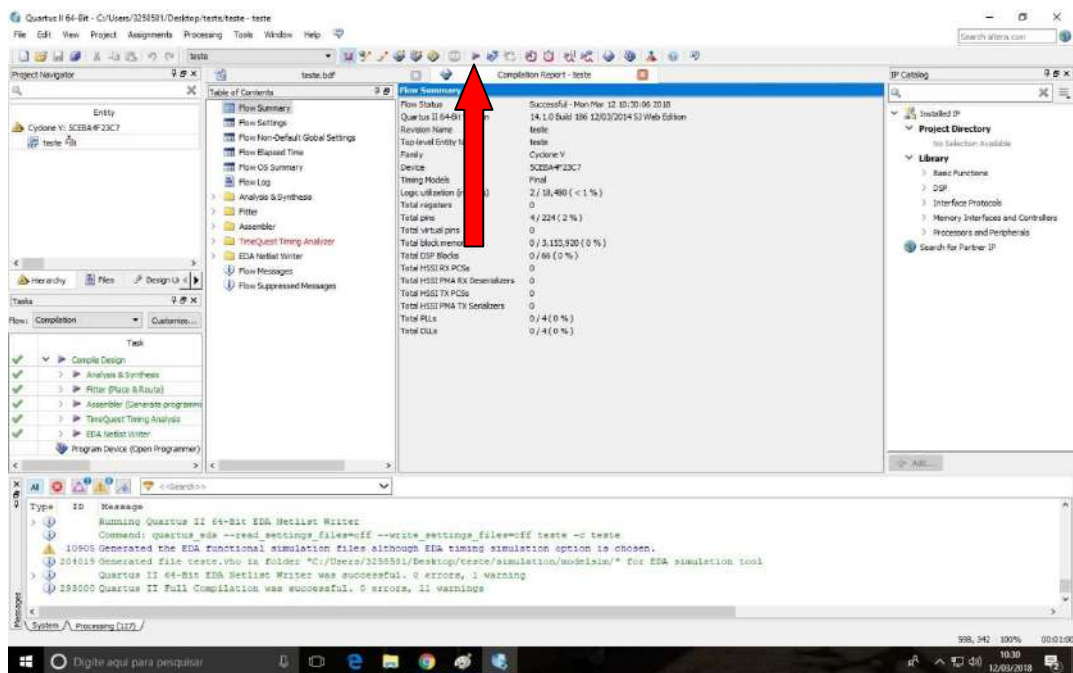
11) Altere os nomes das portas “Input” e “Output” clicando nas mesmas. Não usa espaços no nome dos componentes.



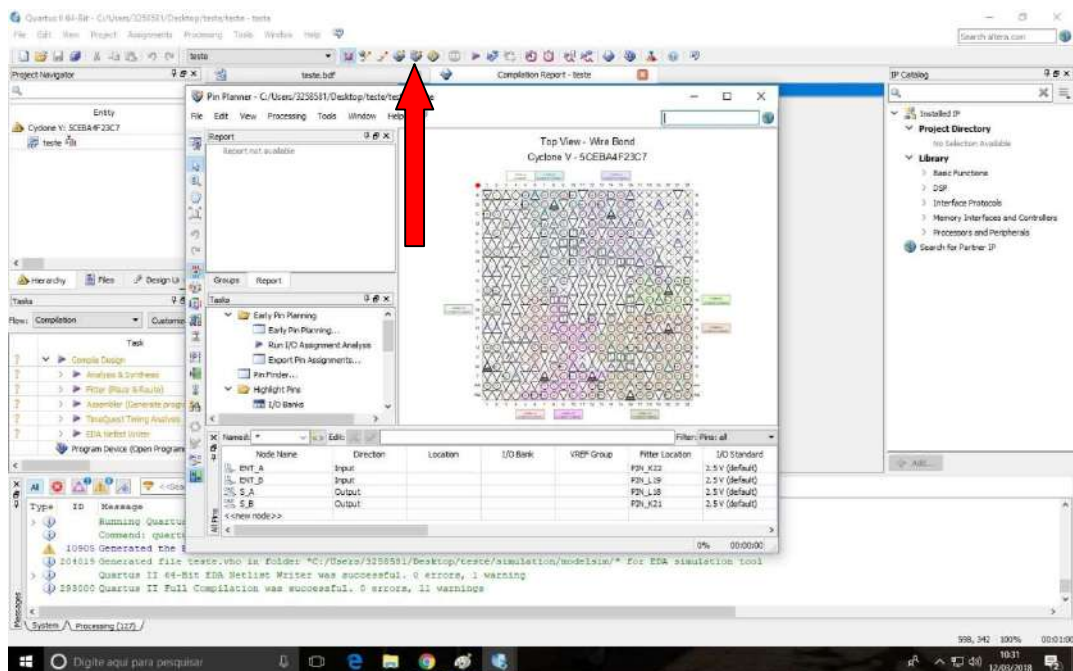
12) Salve o diagrama esquemático com o nome sugerido pelo Quartus, que deve ser o mesmo nome do projeto.



13) Execute a opção "Compile" do menu. O resultado da compilação deve ter apenas warnings e não erros.



14) Use a opção "Pin Planner" do menu.



15) Procure a tabela das chaves de entrada (“Slide switches”), escolha 2 chaves e anote os respectivos pinos.

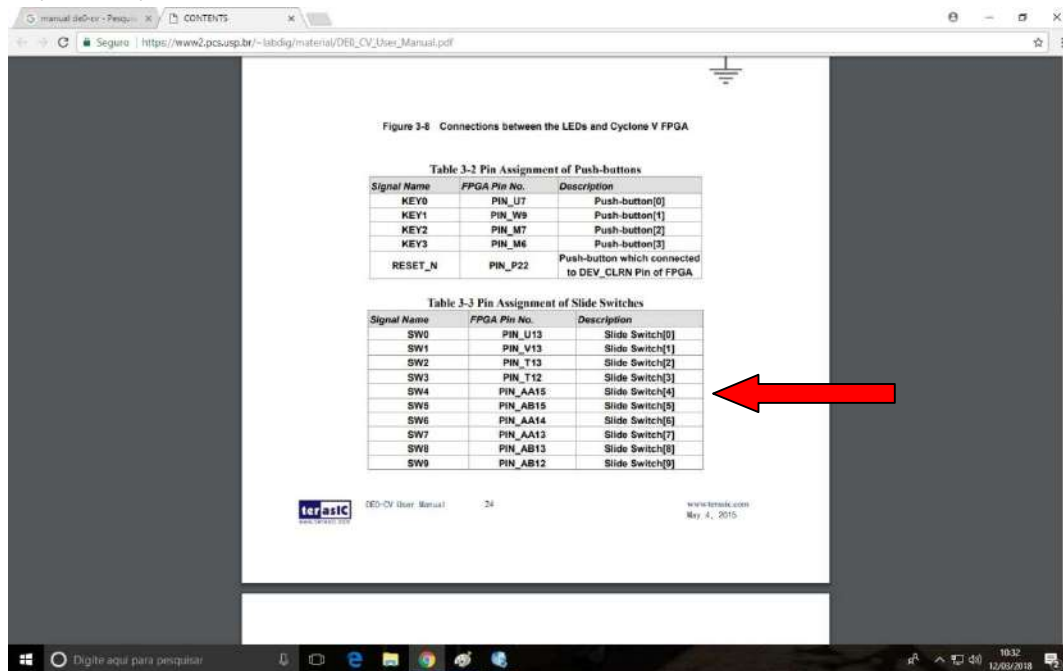


Figure 3-6 Connections between the LEDs and Cyclone V FPGA

Table 3-2 Pin Assignment of Push-buttons

Signal Name	FPGA Pin No.	Description
KEY0	PIN_U7	Push-button[0]
KEY1	PIN_W9	Push-button[1]
KEY2	PIN_M7	Push-button[2]
KEY3	PIN_M6	Push-button[3]
RESET_N	PIN_P22	Push-button which connected to DEV_CLRN Pin of FPGA

Table 3-3 Pin Assignment of Slide Switches

Signal Name	FPGA Pin No.	Description
SW0	PIN_U13	Slide Switch[0]
SW1	PIN_V13	Slide Switch[1]
SW2	PIN_T13	Slide Switch[2]
SW3	PIN_T12	Slide Switch[3]
SW4	PIN_AA15	Slide Switch[4]
SW5	PIN_AB15	Slide Switch[5]
SW6	PIN_AA14	Slide Switch[6]
SW7	PIN_AA13	Slide Switch[7]
SW8	PIN_AB13	Slide Switch[8]
SW9	PIN_AB12	Slide Switch[9]

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16) Procure a tabela dos LEDs, escolha 2 e anote os respectivos pinos.

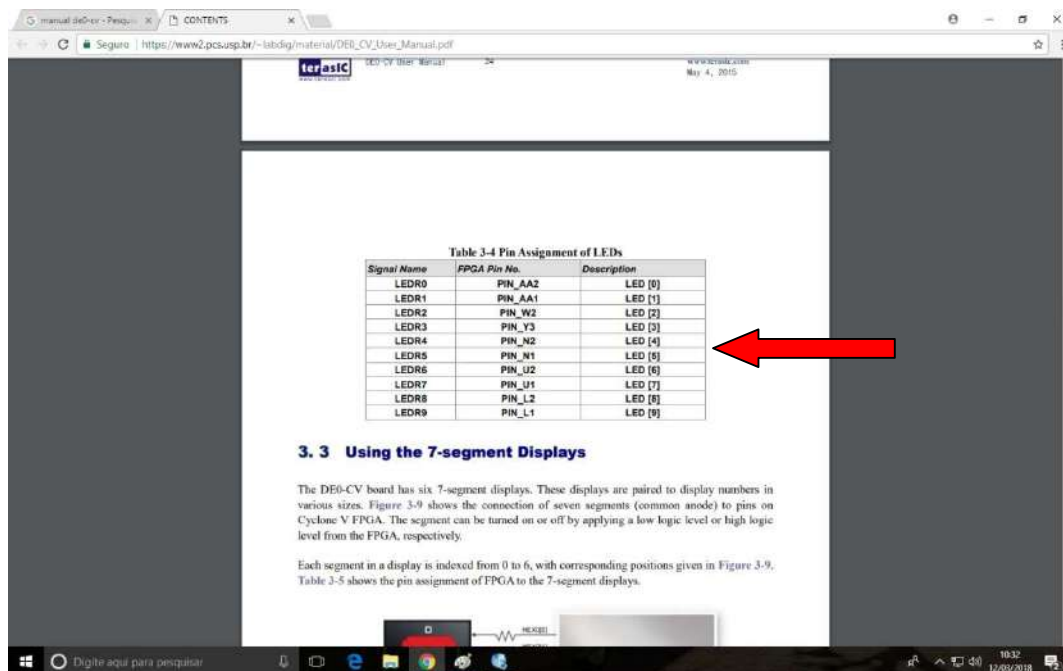


Table 3-4 Pin Assignment of LEDs

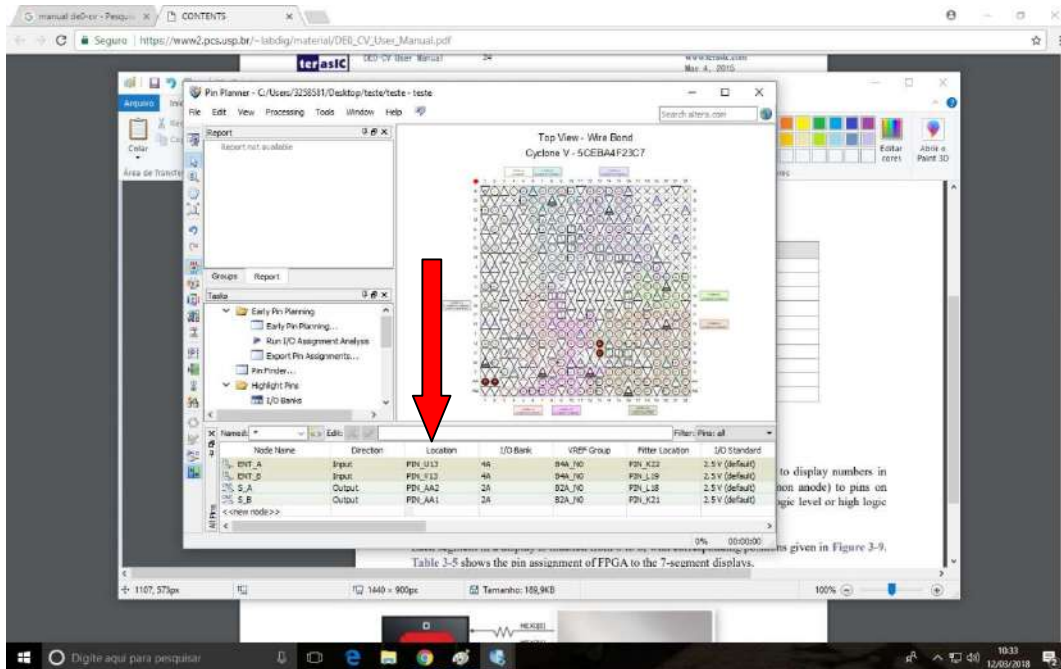
Signal Name	FPGA Pin No.	Description
LED0	PIN_AA2	LED [0]
LED1	PIN_AA1	LED [1]
LED2	PIN_W2	LED [2]
LED3	PIN_Y3	LED [3]
LED4	PIN_N2	LED [4]
LED5	PIN_N1	LED [5]
LED6	PIN_U2	LED [6]
LED7	PIN_U1	LED [7]
LED8	PIN_L2	LED [8]
LED9	PIN_L1	LED [9]

3.3 Using the 7-segment Displays

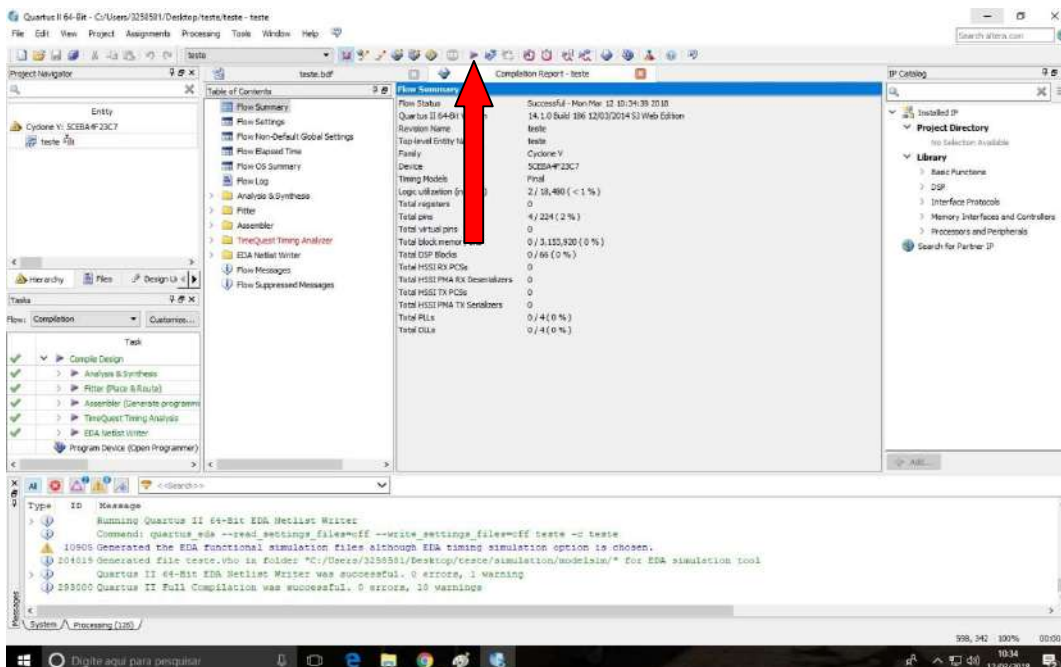
The DE0-CV board has six 7-segment displays. These displays are paired to display numbers in various sizes. Figure 3-9 shows the connection of seven segments (common anode) to pins on Cyclone V FPGA. The segment can be turned on or off by applying a low logic level or high logic level from the FPGA, respectively.

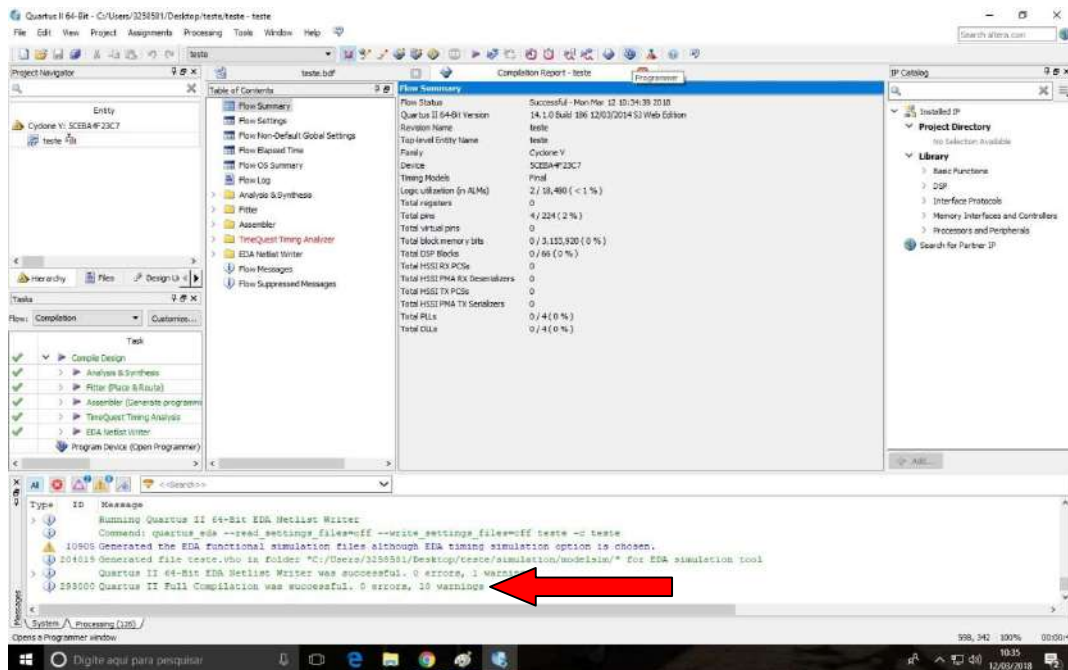
Each segment in a display is indexed from 0 to 6, with corresponding positions given in Figure 3-9. Table 3-5 shows the pin assignment of FPGA to the 7-segment displays.

17) Digite os pinos das chaves no campo “Location” dos terminais de entrada “Input” do circuito, e os pinos dos LEDs nos campos dos terminais de saída do circuito



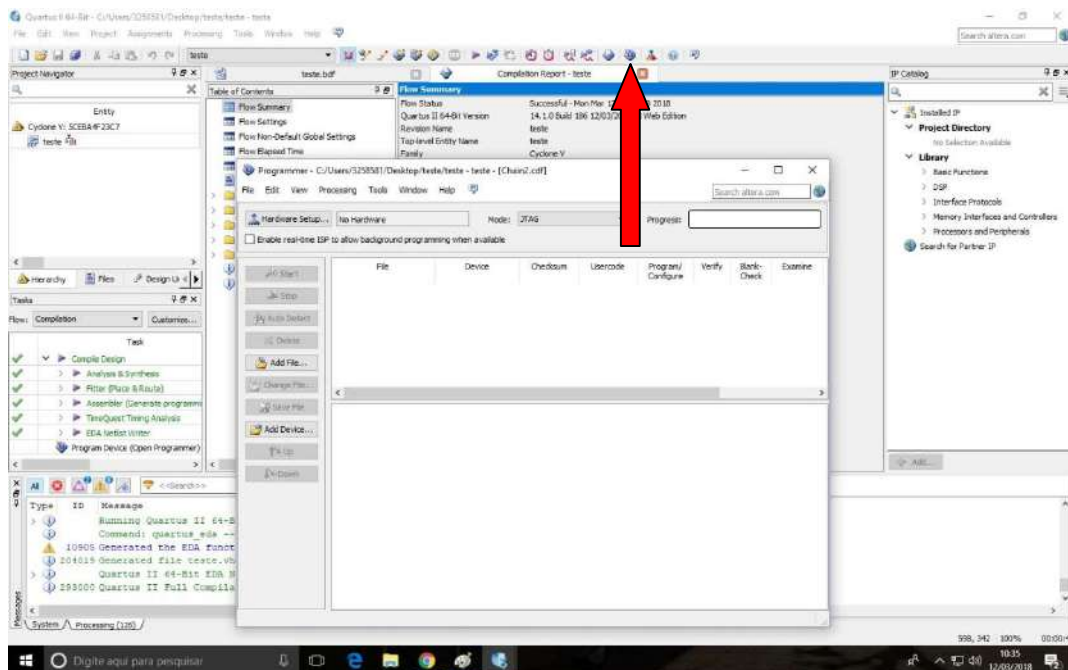
18) Feche o “Pin Planner” e clique novamente na opção “Compile” do menu. Não deve haver erros de compilação.



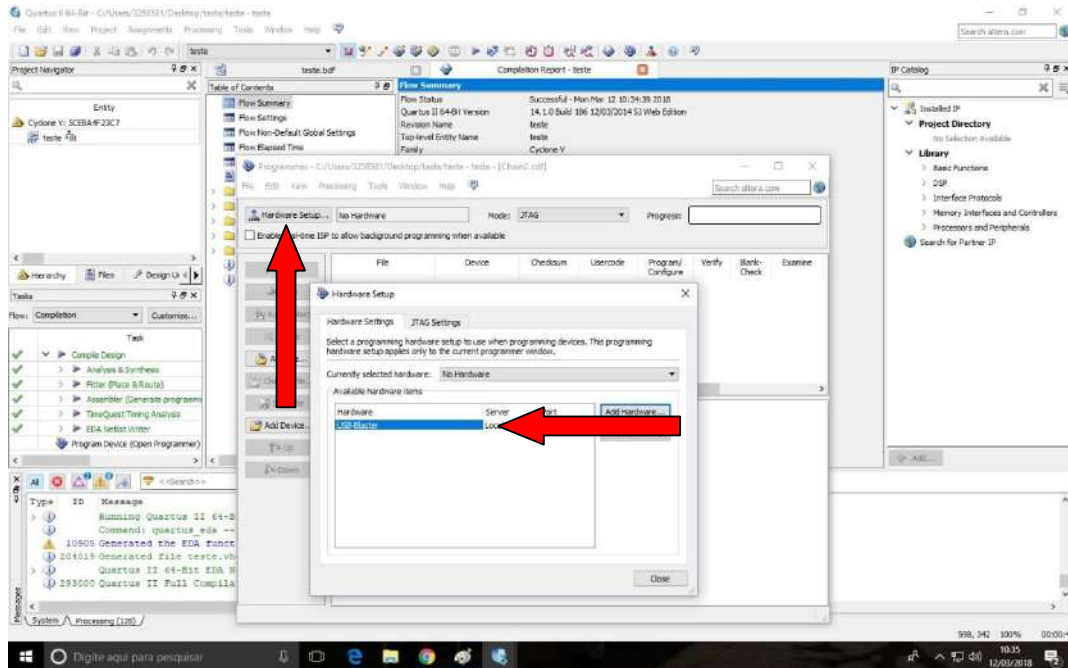


19) Clique a placa de FPGA

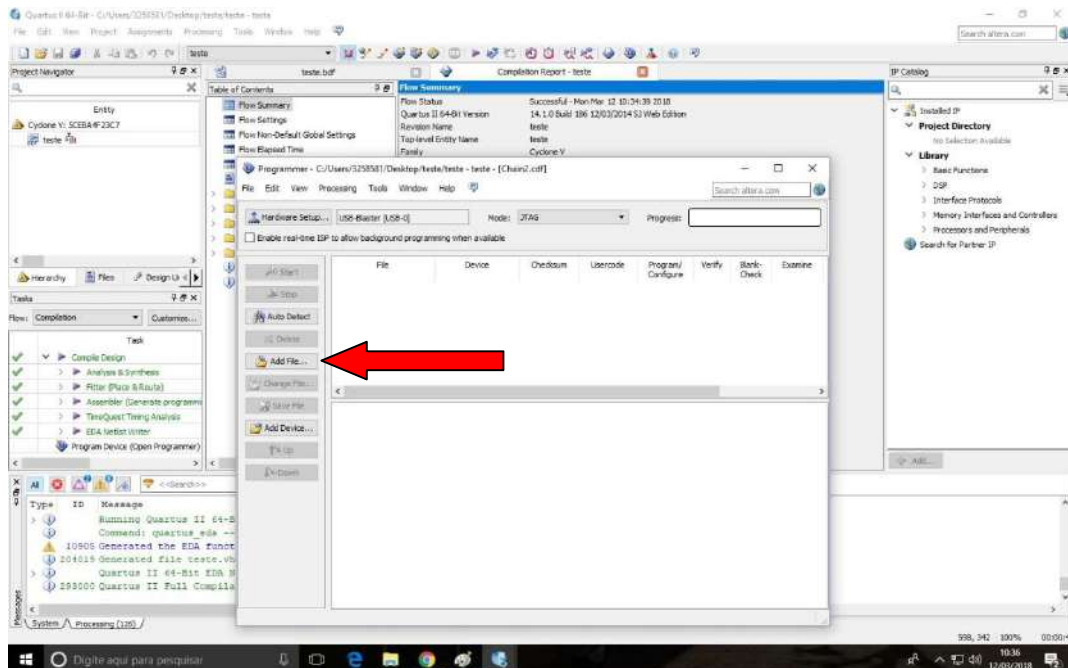
20) Clique na opção "Programmer" do menu



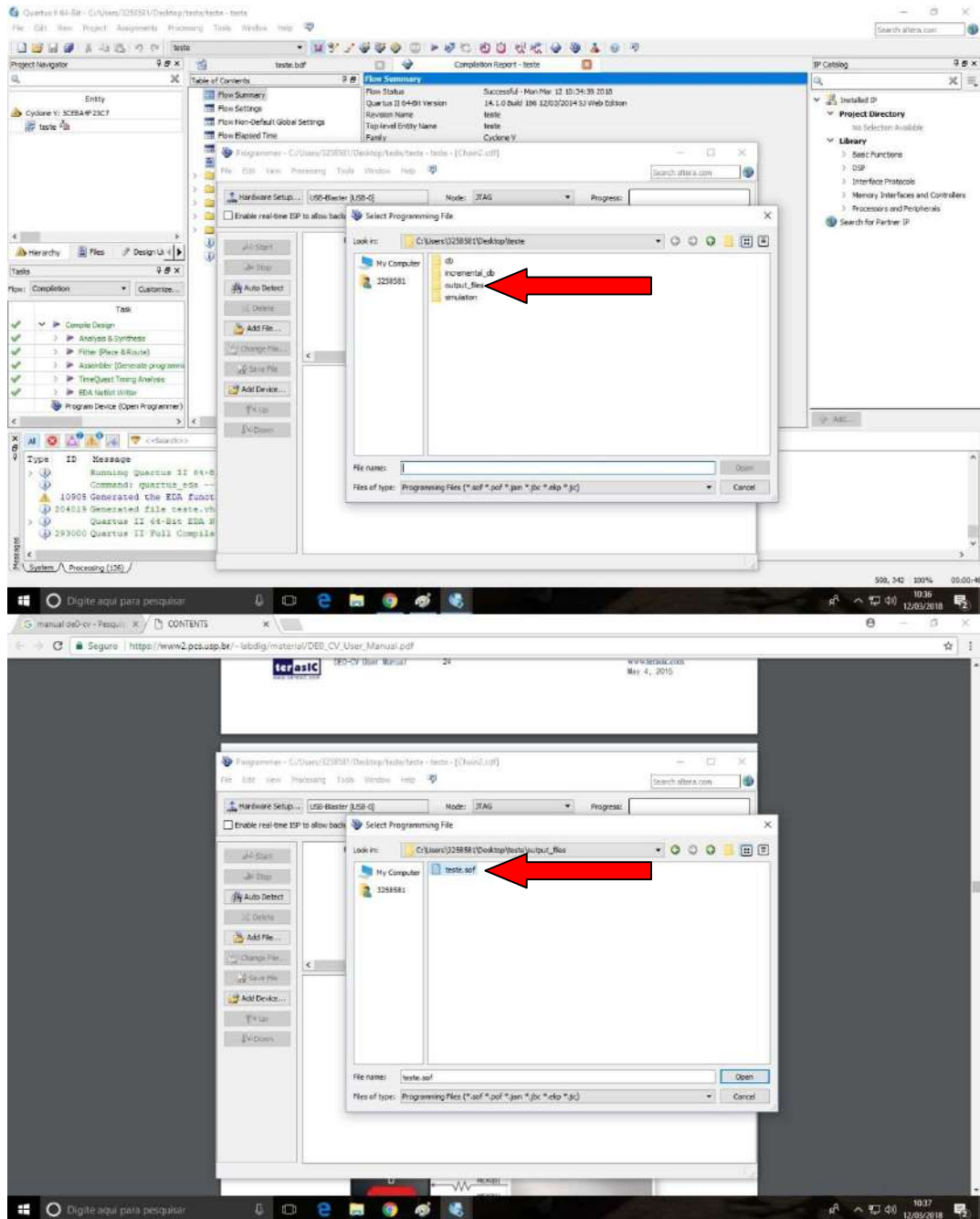
21) Clique no botão “Hardware Setup” e clique 2 vezes na opção “USB-Blaster”. Essa opção só aparece se a placa estiver ligada.



22) Feche o menu do “Hardware Setup” e clique no botão “Add File”.



23) Abra a pasta “output_files” e escolha o arquivo “.sof”



The screenshot shows the JTAG programmer software interface. A red arrow points to the 'Start' button in the left-hand menu. The main window displays the file 'test2.cdf' and the device 'XC6SLX160'. The 'Start' button is highlighted with a red arrow.

The screenshot shows the JTAG programmer interface with the following details:

- File:** output_hex/teste.asf
- Device:** XCE3A40F23
- Checksum:** 00400EA1
- Usercode:** 00400EA1
- Progress:** 100% (green bar)
- Verify:** (green box, highlighted by a red arrow)
- Program/Configure:** (checkbox checked)
- Verify:** (checkbox unchecked)
- Examine:** (checkbox unchecked)

The schematic diagram at the bottom shows the XCE3A40F23 device connected to a TDI pin and a TDO pin.