CprE 3810, Computer Organization and Assembly Level Programming

Team Contract – Project Part 1

Project Teams Group: F_03

Team Members: Austin Hunwardsen

Peter Knipper

Course Goals:

- *learn about computer architecture*
- *understand security risks posed by hardware primitives*
- *pass the course*
- *explain the workings of a computer from gates to C*

Team Expectations:

- **Conduct:** *Get assigned responsibilities done by the deadline.*
- **Communication:** Text communication will work best for the group. *Communication should occur weekly. A response should be expected within 24 hours.*
- **Group conventions:** *tb_ for test benches. i_ for inputs, o_ for outputs, s_for signals. Dataflow for simple components, structural for more technical. Waveform simulation. Follow the given tb file format that was given in labs 1 and 2. Do files will be used towards the end of the project. Github will be used for version control. Comment above block what the block is doing. In testbench, give desired output.*
- **Meetings:** *We will expect to work on the project on weekends. Times of availability would be 11:00am-2:00pm on Saturday and Sunday. Otherwise, we can meet virtually via Discord if major problems arise.*

- **Peer Evaluation Criteria:** *Effort will be determined by getting project work done on time and reaching out to the other if stuck or lost in they should be doing. Contribution has been decided by the role responsibilities table listed below. If confused, the other can help out.*

Role Responsibilities:

Lab Part	Estimated Time	Design		Test	
		Lead	**Deadline**	**Lead**	**Deadline**
High-level design	1 hr	Peter	10/09	Austin	10/09
Test programs	4 hr	Austin	10/16	Peter	10/16
Control logic	2 hr	Peter	10/09	Austin	10/09
Fetch logic	3 hr	Austin	10/09	Peter	10/09
Barrel shifter	2 hr	Peter	10/16	Austin	10/16
ALU integration + Misc updates	2 hr	Austin	10/16	Peter	10/16
High-level integration	4 hr	Peter	10/23	Austin	10/23
Synthesis (human effort)	1.5 hr	Austin	10/23	Peter	10/23

Integrity of Work: We agree that the work we provide to other team members and ultimately submit for a grade is a direct result of our own work as described in the course syllabus. Specifically, we will generate all VHDL code ourselves and not copy VHDL code from online sources, other groups, book companion material, or past student projects to which anyone outside of my team has contributed.

Student Signature Peter Knipper **Date** 10/02/25

Student Signature Austin Hunwardsen **Date** _10/02/25_____

Student Signature _____ **Date** _____