HELLO Project MOOC Edition - DE10-Lite Introductory Exercise

(Last updated June 12, 2019)

Version 1

Objectives:

- Verify the proper installation of the Quartus v16.1 Lite software
- Verify the DE10-Lite Board operates correctly.
- Update Default Demo to show "HELLO" on the seven segments.

Procedure:

1) Verify the Quartus tools are installed on your PC.

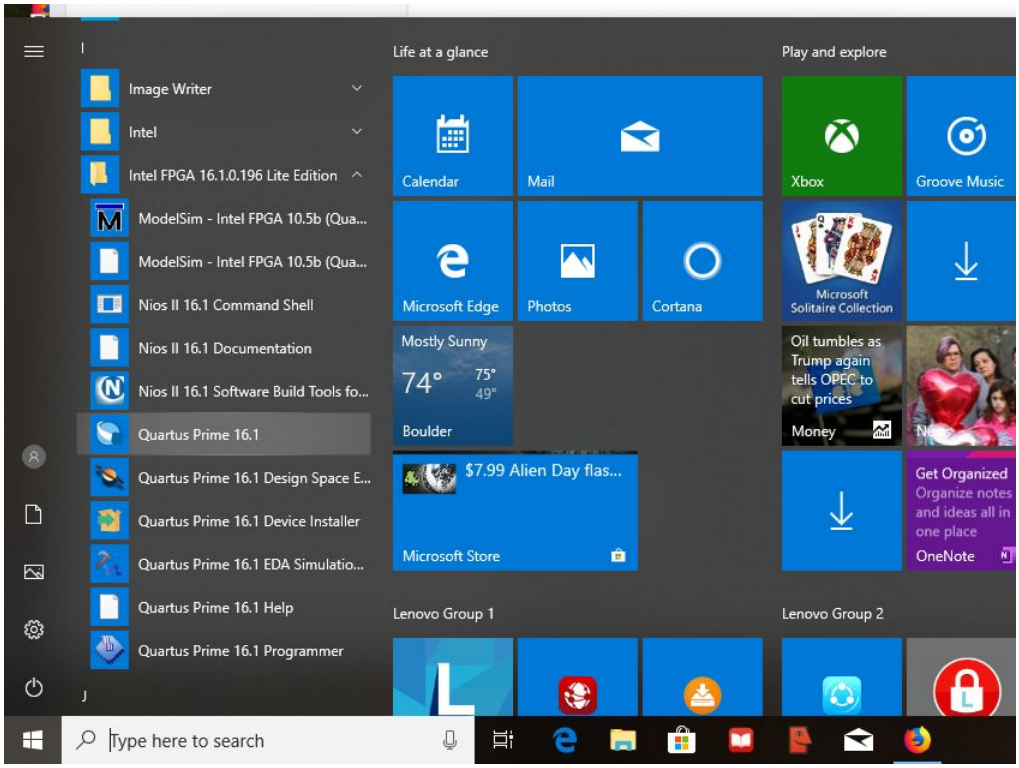
2) Create a Terasic account if you don't already have one and access the resources for the DE10-Lite board. The user manual is accessible directly from the website without logging in but the System CD will require an account.

http://download.terasic.com/downloads/cd-rom/de10-lite/DE10-Lite_v.2.0.2_SystemCD.zip

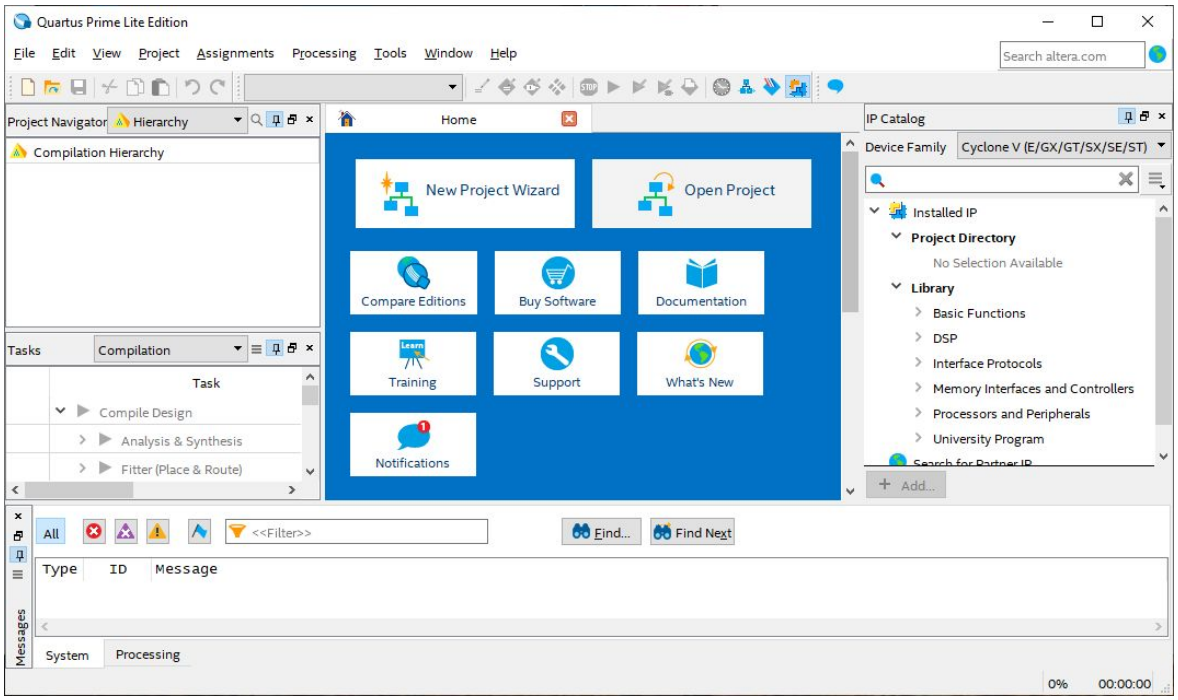
3) Install the files in a directory with no spaces in the path. A good example to use for the directory is \spd_sum_19_ex1_<team_name>_v<version#>\

4) Plug in the DE10-Lite board and verify it powers up through the USB cable.

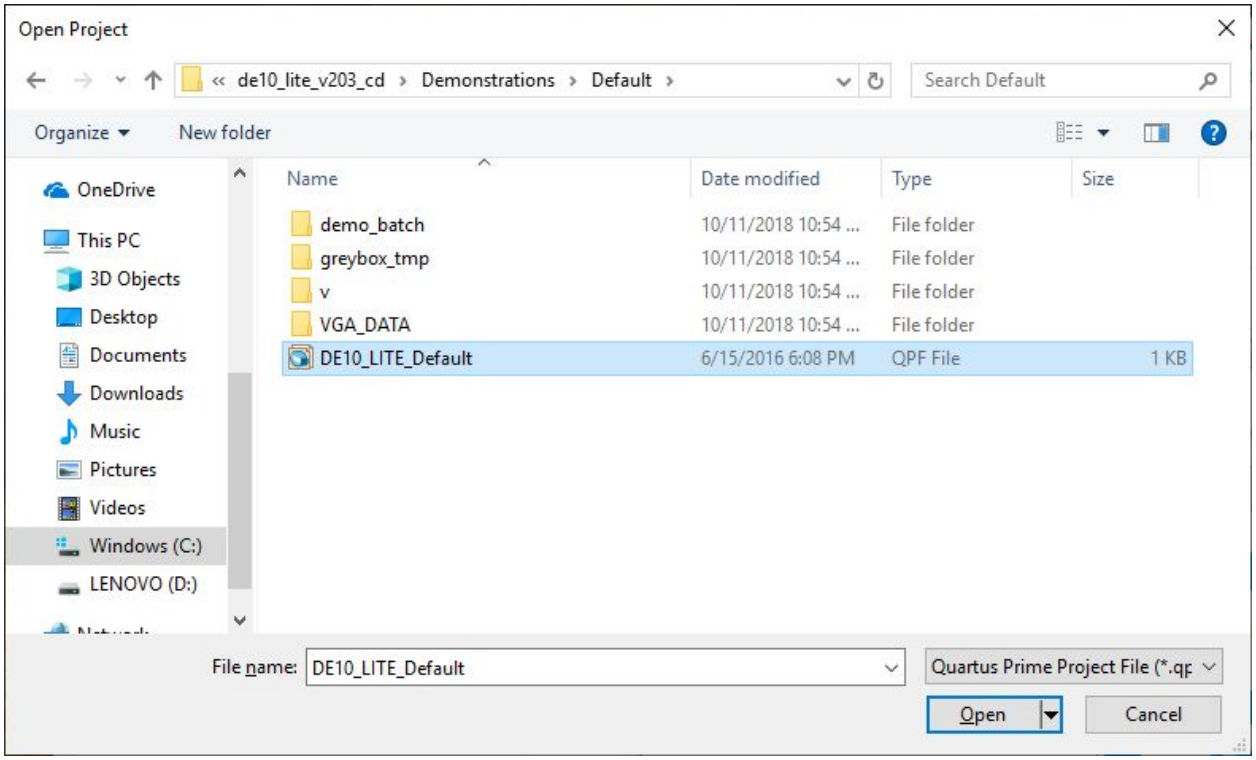
5) Open Quartus and launch the demonstration project DE10_LITE_Default. Be sure to select Quartus v16.1 Lite for the project. There may be other versions installed so be sure to pick this one.



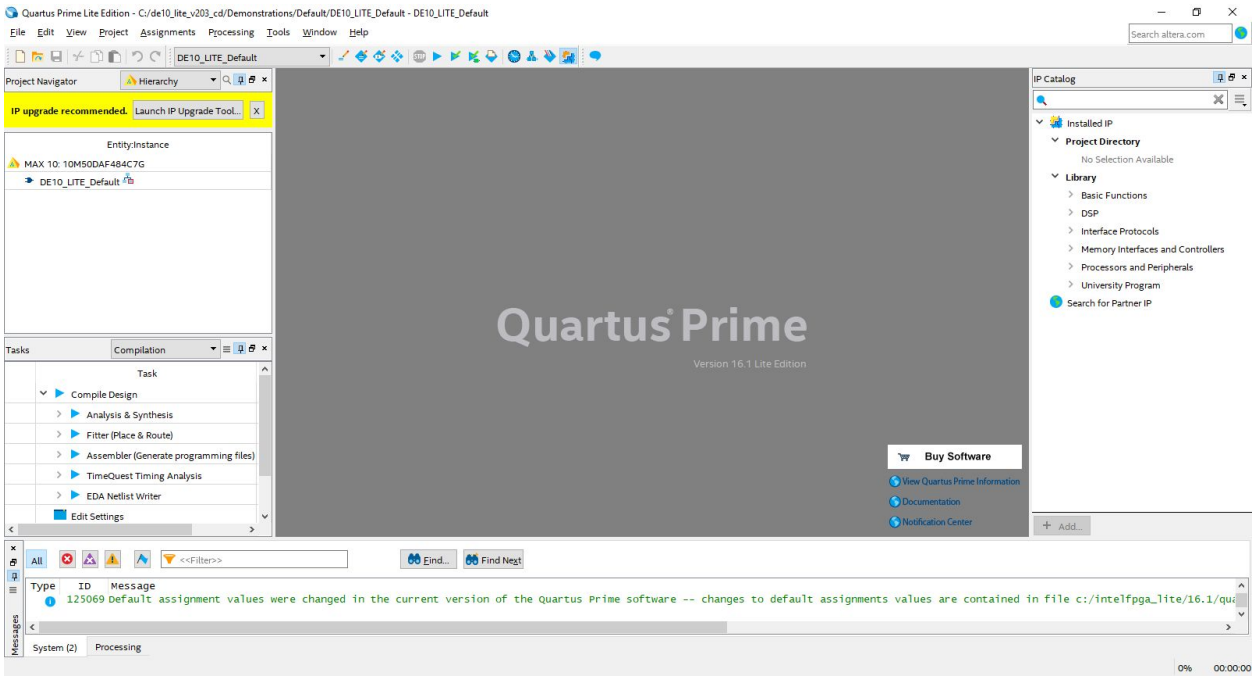
6) Once the IDE launches, select Open Project from the button in the middle of the screen.



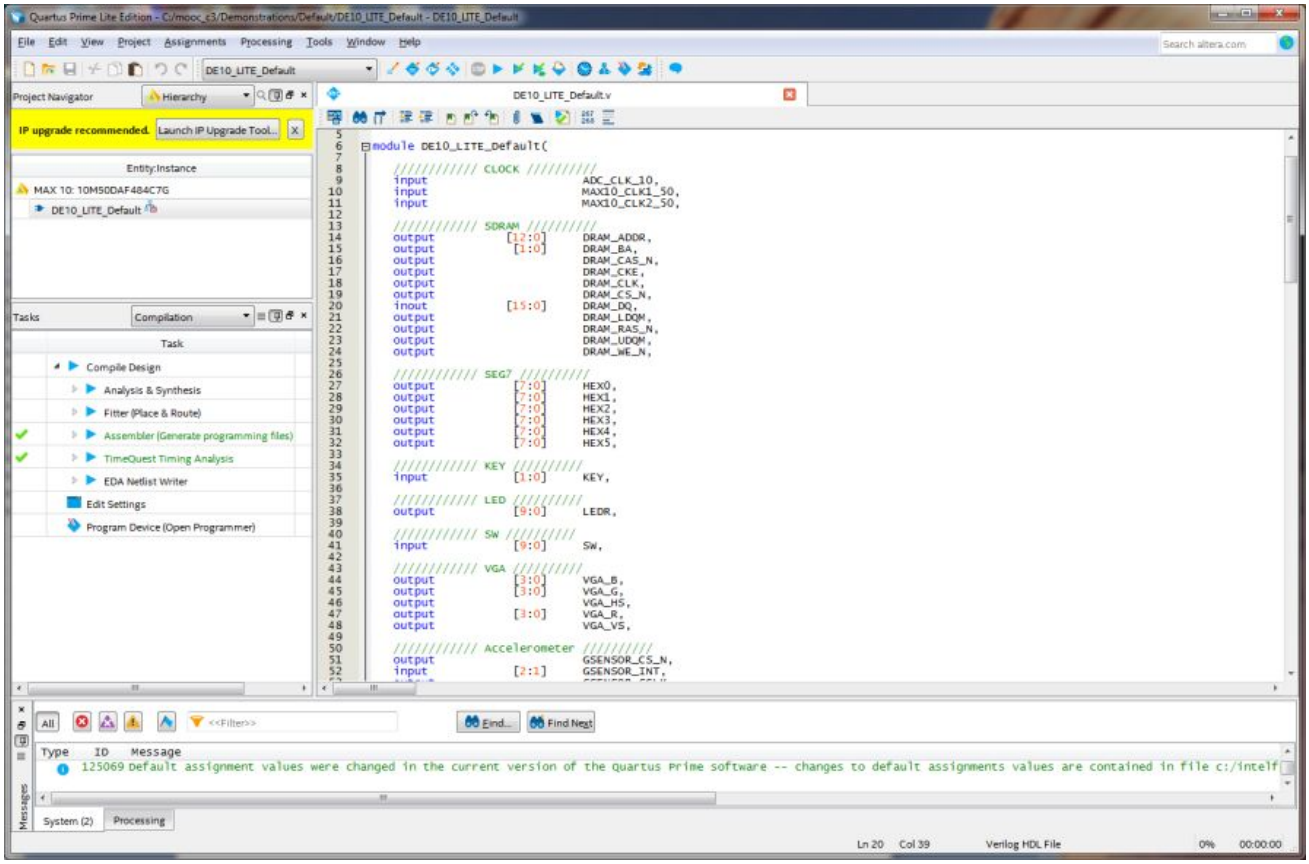
7) Navigate to the location of the system CD files and select the DE10_LITE_Default.QPF project file as shown in the screenshot below.



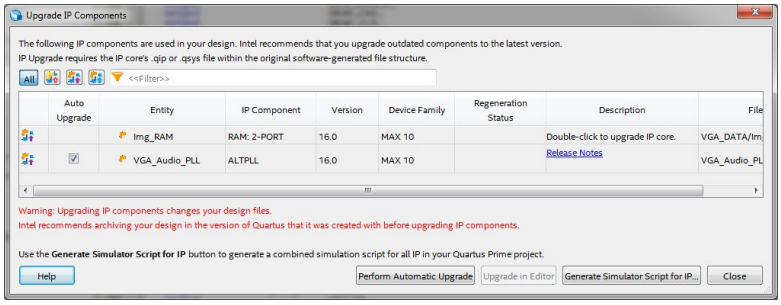
8) Once the project loads you will see the screen below.



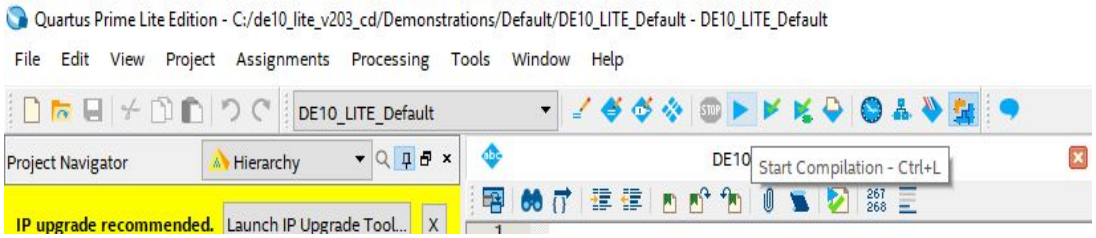
9) In order to see the HDL code you need to select the file on the left hands side under the Entity:Instance and definition of the MAX 10 device. Double click on the DE10_Lite_Default and the code will appear in the center of the screen.



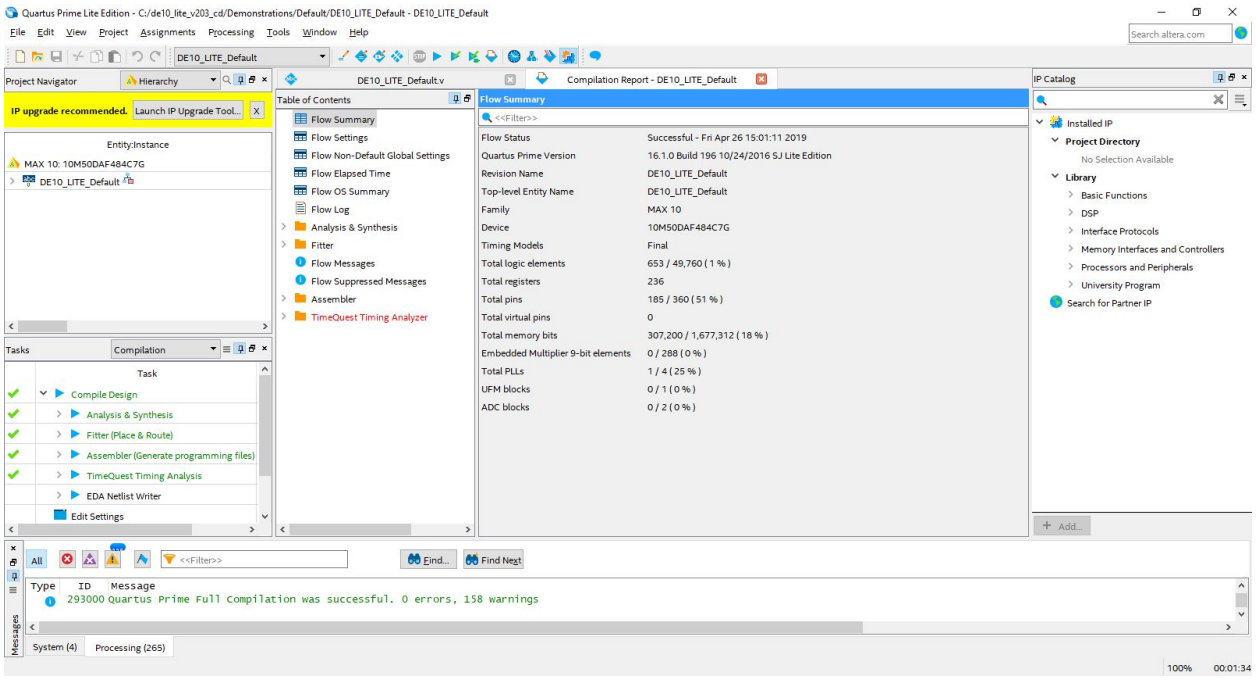
10) Next launch the IP upgrade tool and perform the recommended automatic upgrades. The VGA_Audio_PLL will take some time to regenerate. Select close once the process completes.



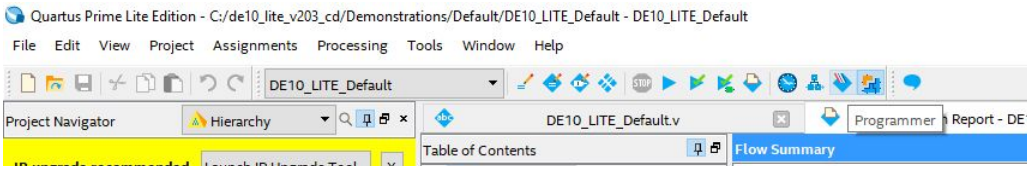
11) Next click the Blue button on the top row next to the STOP sign to Compile the design or use the CTRL-L key as a short cut. Depending on the speed of your computer it may take a little time for this to complete.



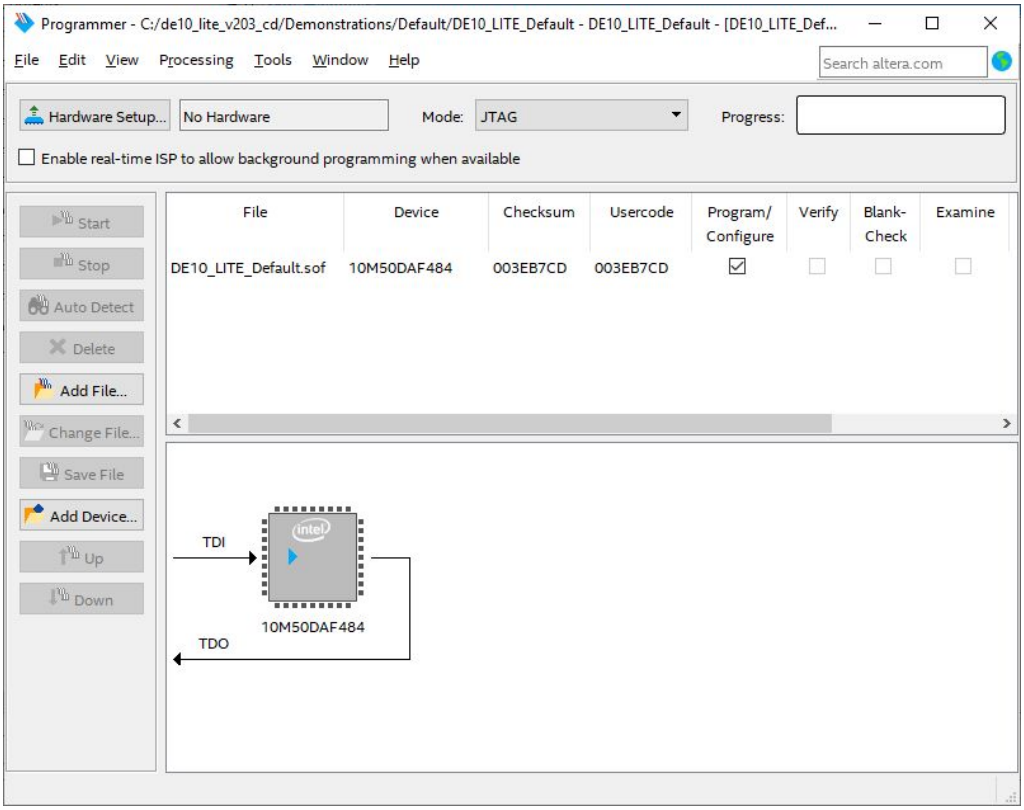
12) After the project compiles with no errors it should look like the screenshot below



13) The Icon for the programmer is highlighted in the screenshot below it is the third from the far right icon and next to the Qsys button.

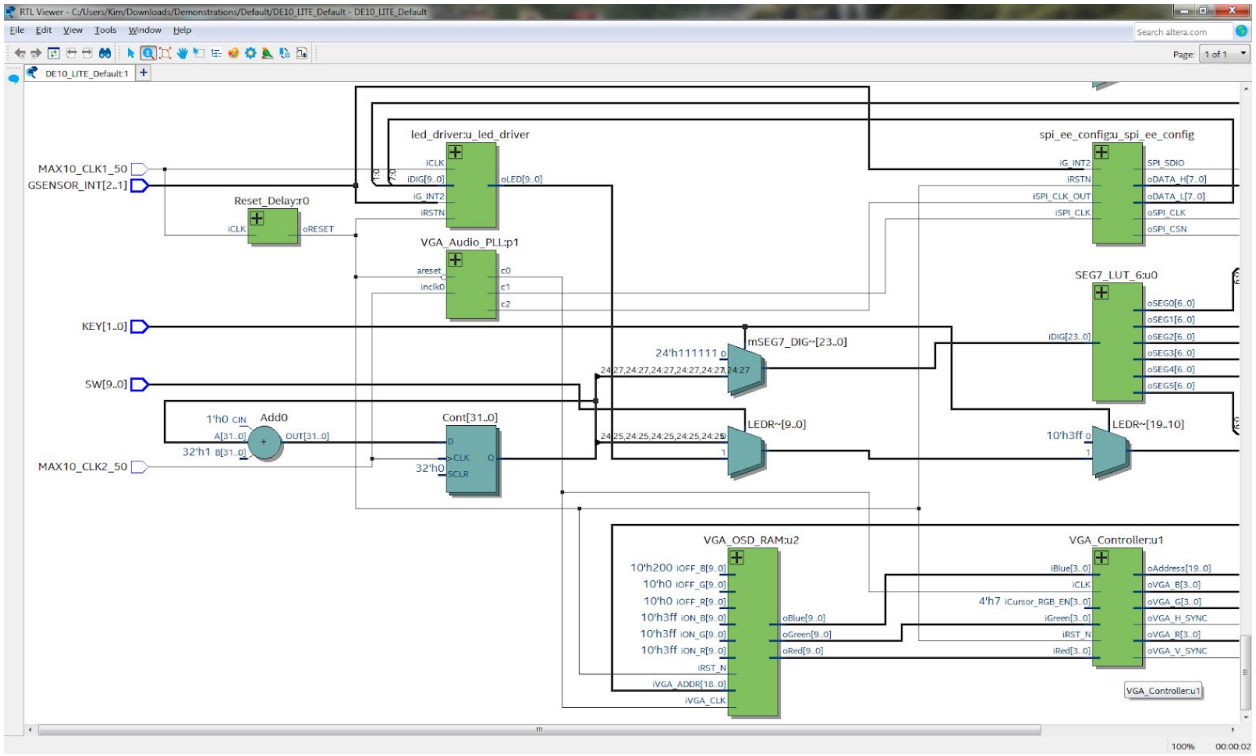


14) The default setup for the programmer is shown below. Once the DE10-Lite board is connected the hardware setup needs to be updated to connect to the USB-Blaster. There are detailed instructions in the DE10-Lite user manual that you can review for this step if you are not familiar with this tool flow.

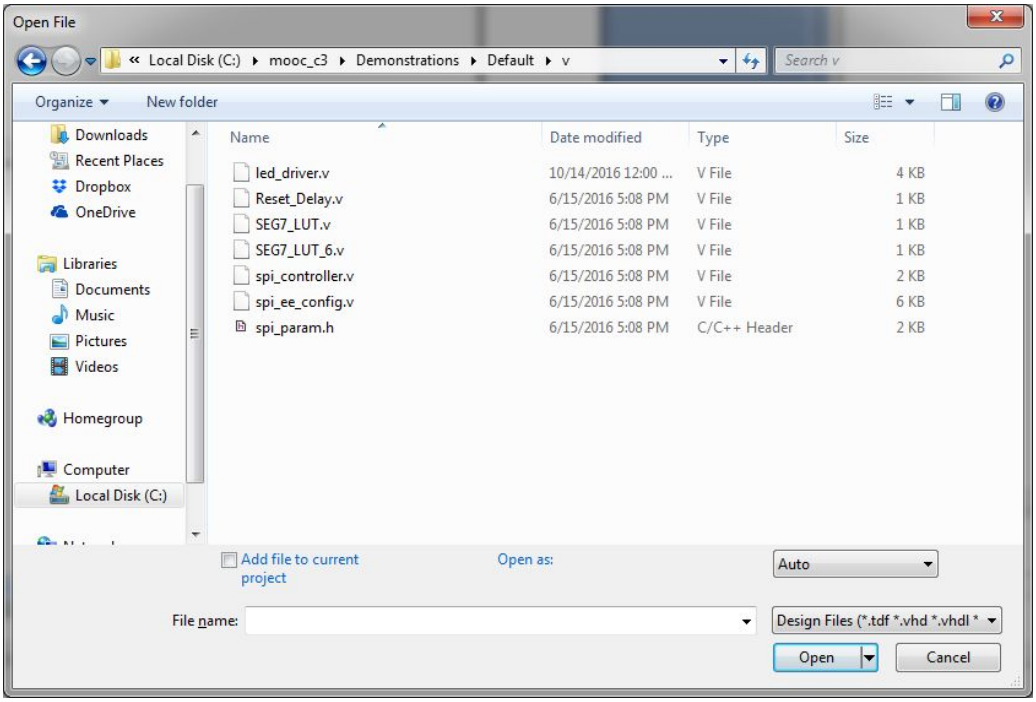


CHECK POINT 1: Post a screenshot of your progress to the forums.

15) To see how the project is implemented, use the netlist viewer after compiling the project.



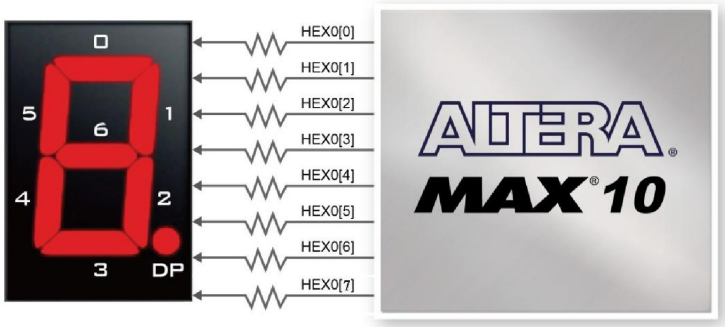
16) The next step is to update the project to show the letters on the displays. Navigate to the folder for the peripheral devices in the project.



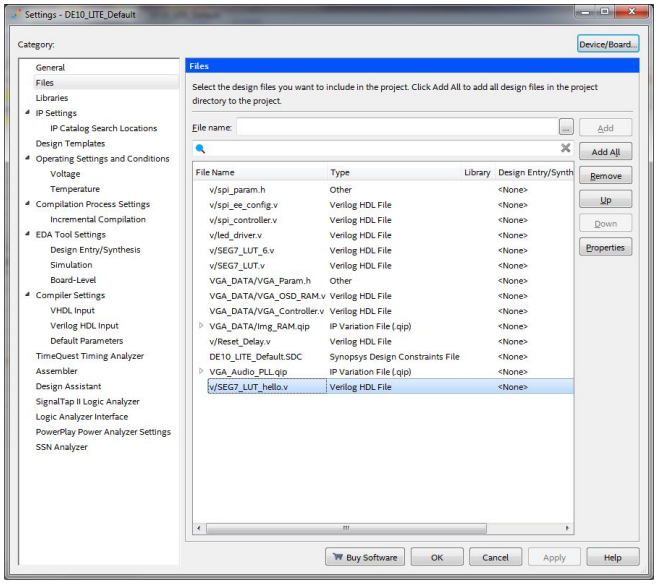
17) You can see here the module for the Seven segment display in the current form.

```
module SEG7_LUT   (  oSEG,iDIG   );
input [3:0] iDIG;
output   [6:0] oSEG;
reg      [6:0] oSEG;

always @(iDIG)
begin
      case(iDIG)
      4'h1: oSEG = 7'b1111001;   // ---t----
      4'h2: oSEG = 7'b0100100;   // |      |
      4'h3: oSEG = 7'b0110000;   // lt     rt
      4'h4: oSEG = 7'b0011001;   // |      |
      4'h5: oSEG = 7'b0010010;   // ---m----
      4'h6: oSEG = 7'b0000010;   // |      |
      4'h7: oSEG = 7'b1111000;   // lb     rb
      4'h8: oSEG = 7'b0000000;   // |      |
      4'h9: oSEG = 7'b0011000;   // ---b----
      4'ha: oSEG = 7'b0001000;
      4'hb: oSEG = 7'b0000011;
      4'hc: oSEG = 7'b1000110;
      4'hd: oSEG = 7'b0100001;
      4'he: oSEG = 7'b0000110;
      4'hf: oSEG = 7'b0001110;
      4'h0: oSEG = 7'b1000000;
      endcase
end

endmodule
```

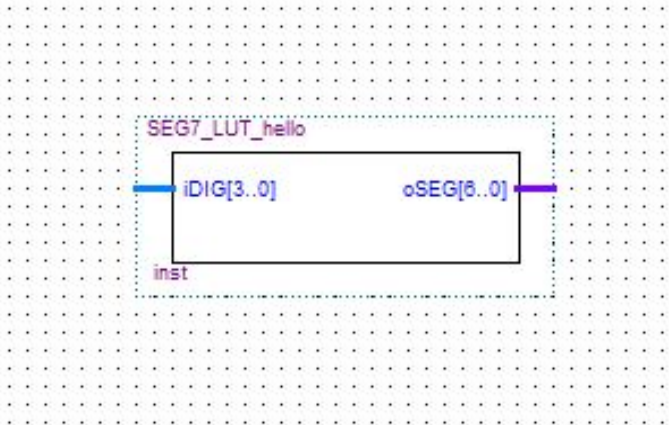
18) Make a new file called SEG7_LUT_hello.v by saving the SEG7_LUT.v as the new file name. Check the manual for the DE10-Lite and setup the output to display “HELO” for outputs 1-4 and remove the other settings. This is a good review if you have done this before and is a good skill check to make sure you can get through the tool flow.



19) Add the new file to the project.

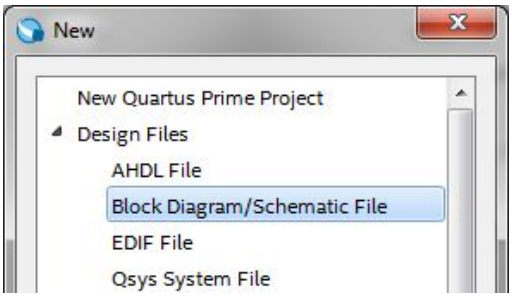


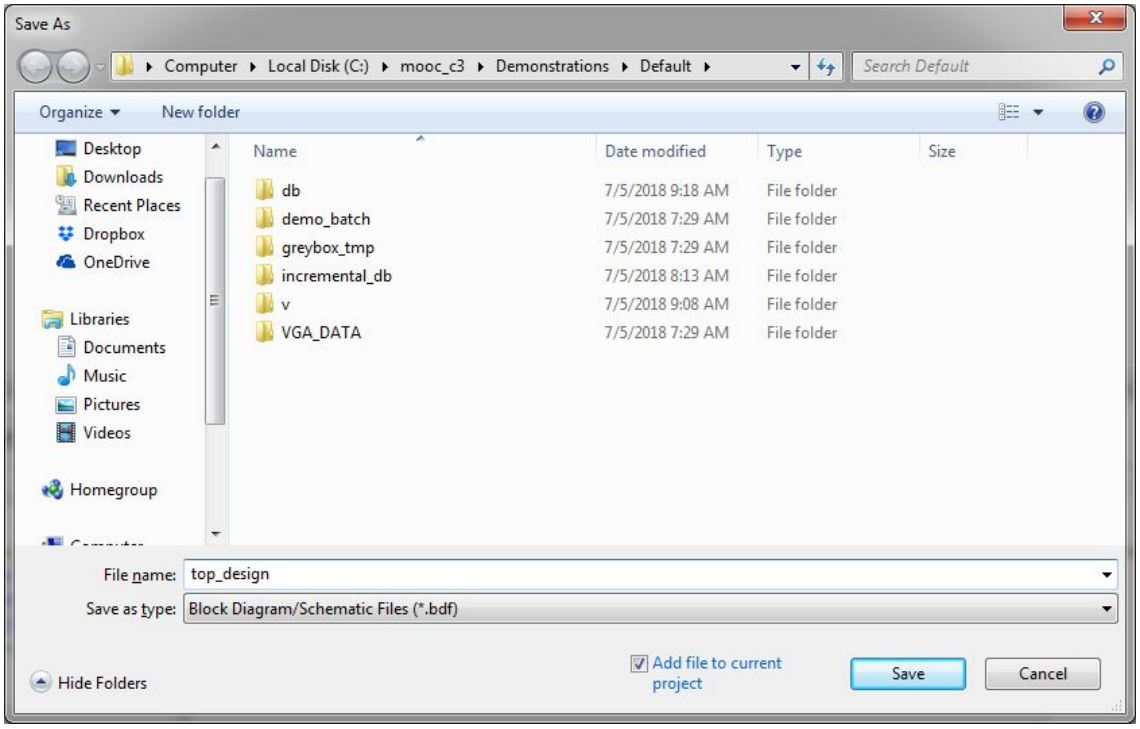
20) Generate a symbol file for the new SEG7_LUT_hello.v file. File > Create/Update > Create Symbol File for Current File. Ignore the warning message since they are only for my configuration and not pertinent to this project.



CHECK POINT 2: Post a screenshot of the symbol to the forums.

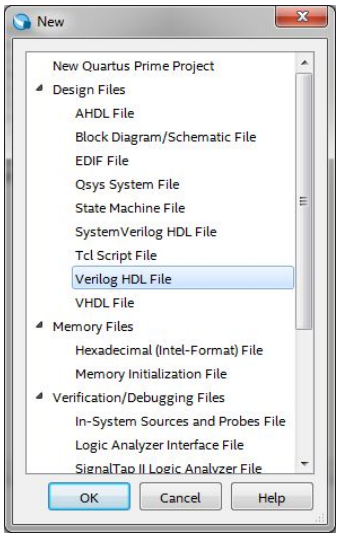
21) Create a new file for the project as shown below and save in the directory in the screen shot with the name top_design shown in the screenshot below.

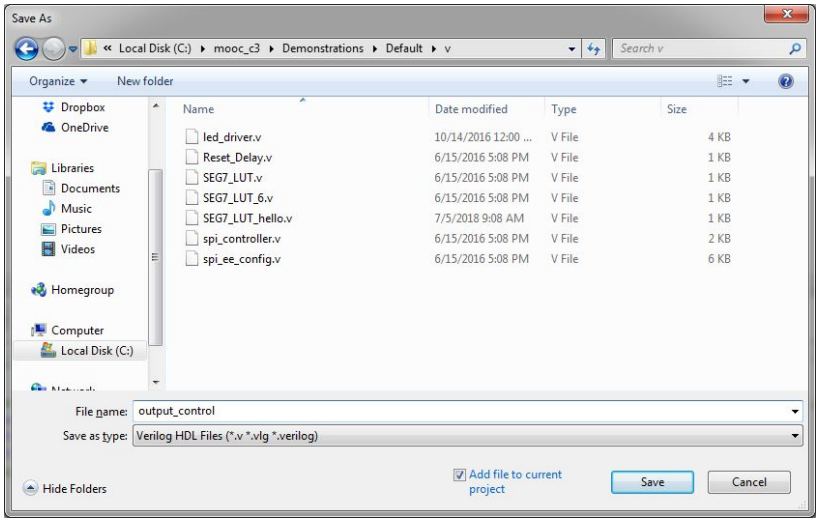




22) Open the project directory and set the BDF file as the top level entity. Add the new seven segment symbol that was generated in the previous step. Text comments can be added to the top level design to help with debugging.

23) Create a new Verilog file to control the output of the seven segment displays.

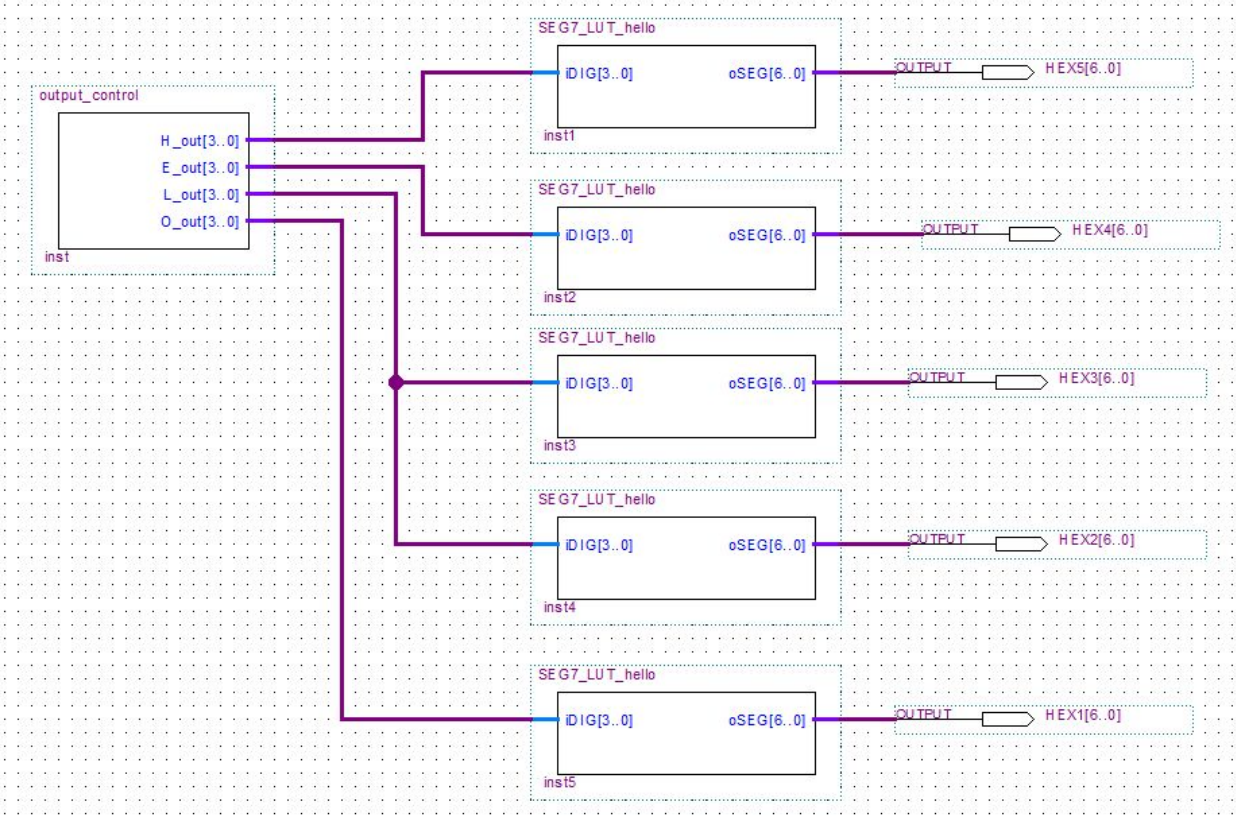




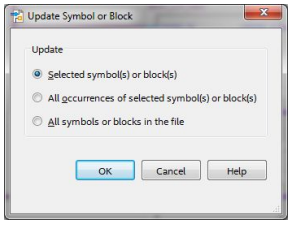
```
1   module SEG7_LUT_hello   (  oSEG,iDIG   );
2   input [3:0] iDIG;
3   output    [6:0] oSEG;
4   reg       [6:0] oSEG;
5
6   always @(iDIG)
7   begin
8         case(iDIG)
9         4'h0: oSEG = 7'b10001001; // Letter H
10        4'h1: oSEG = 7'b10000110; // Letter E
11        4'h2: oSEG = 7'b11000111; // Letter L
12        4'h3: oSEG = 7'b11000000; // Letter O
13        endcase
14  end
15
16  endmodule
17
```

(Verify the number of bits being entered - the variable is only 7 bits long but I specified 8 values)

24) Copy the Seven Segment output for each display and wire it as shown below. Use the Pin Planner to get the names of the output labels.



25) Compile the project and test the output. Each time the Verilog file is changed the symbol needs to be updated and replaced in the top level schematic. Right click on the symbol and select update.



Final Verification: Once the project is working, show it to the student assistant. Attached is a photo from my board when I was developing this exercise. The third seven segment display on my board doesn't work for the bottom output.