

EIE 211: Electronic Devices and Circuit Design II

Lecture 4x²(dx/dt): CMOS Cascode

Table 5.3 Small-Signal Equivalent-Circuit Models for the MOSFET

Small-Signal Parameters

NMOS transistors

■ Transconductance:

$$g_m = \mu_n C_{ox} \frac{W}{L} V_{OV} = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} = \frac{2I_D}{V_{OV}}$$

Output resistance:

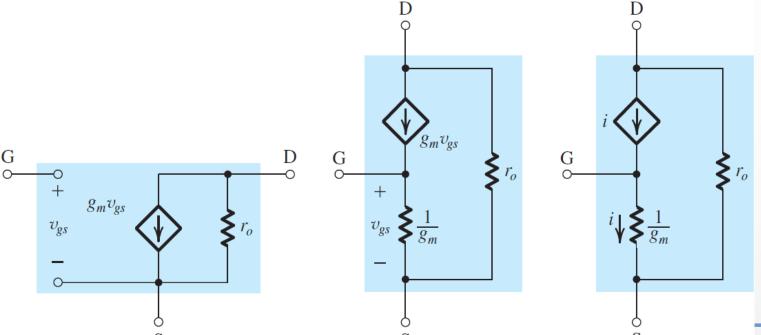
$$r_o = V_A/I_D = 1/\lambda I_D$$

PMOS transistors

Same formulas as for NMOS except using $|V_{OV}|$, $|V_A|$, and replacing μ_n with μ_p .

Small-Signal Equivalent Circuit Models

Hybrid- π model

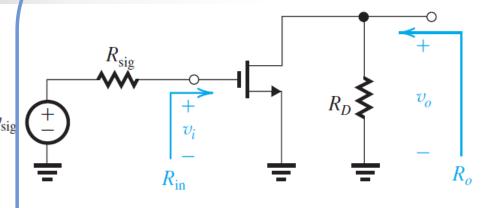


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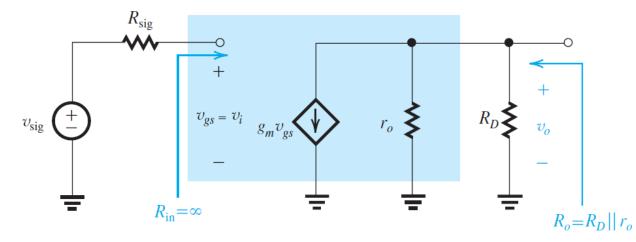
Common Source Amplifier



(a)

$$R_{\rm in} = \infty$$

$$R_o = R_D \parallel r_o$$

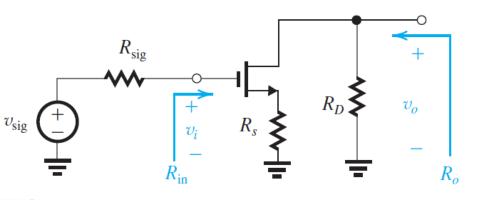


(b)

$$G_v = A_v = -g_m(R_D \parallel R_L \parallel r_o)$$



Common Source Amplifier w/ Degeneration Resistor



$$v_{gs} = v_i \frac{1/g_m}{1/g_m + R_s} = \frac{v_i}{1 + g_m R_s}$$

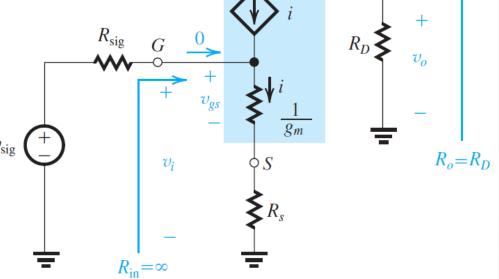
$$i = \frac{v_i}{1/g_m + R_s} = \left(\frac{g_m}{1 + g_m R_s}\right) v_i$$

$$v_o = -i R_D$$

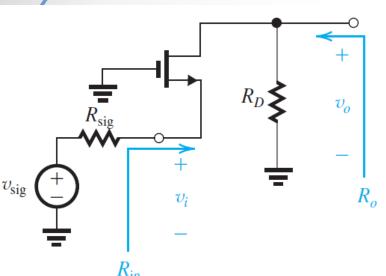
$$A_{vo} = \frac{v_o}{v_i} = -\frac{R_D}{1/g_m + R_s}$$

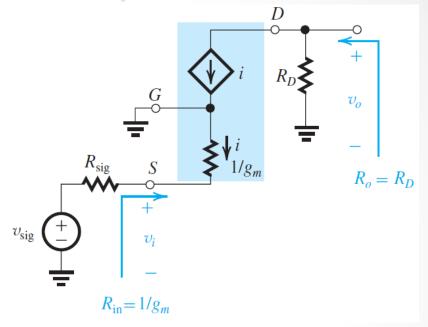
$$A_{vo} = -\frac{g_m R_D}{1 + g_m R_s}$$

Voltage gain from gate to drain = $-\frac{\text{Total resistance in drain}}{\text{Total resistance in source}}$



Common Gate Amplifier





$$R_{\rm in} = \frac{1}{g_m}$$

$$v_o = -iR_D$$

$$i = -\frac{v_i}{1/g_n}$$

$$A_{vo} \equiv \frac{v_o}{v_i} = g_m R_D$$

$$R_o = R_D$$

$$\frac{v_i}{v_{\text{sig}}} = \frac{R_{\text{in}}}{R_{\text{in}} + R_{\text{sig}}} = \frac{1/g_m}{1/g_m + R_{\text{sig}}}$$

$$G_v = \frac{1/g_m}{R_{\text{sig}} + 1/g_m} [g_m(R_D \parallel R_L)] = \frac{(R_D \parallel R_L)}{R_{\text{sig}} + 1/g_m}$$

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Table 5.4	Characteristics	of MOSFET	Amplifiers
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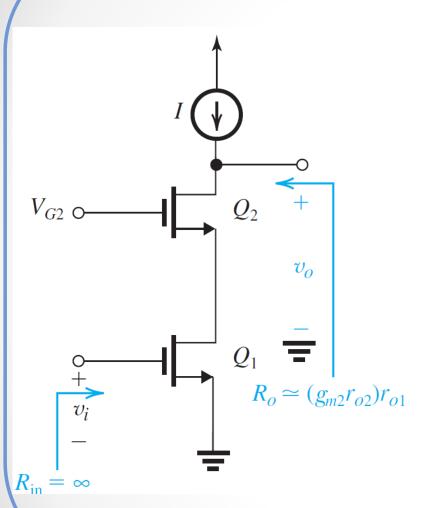
Characteristics ^{a, b}					
$R_{\rm in}$	A_{vo}	R_o	A_v	G_v	
∞	$-g_m R_D$	R_D	$-g_m(R_D \parallel R_L)$	$-g_m(R_D \parallel R_L)$	
∞	$-\frac{g_m R_D}{1 + g_m R_s}$	R_D	2	$-\frac{g_m(R_D \parallel R_L)}{1 + g_m R_s}$	
			$-\frac{R_D \parallel R_L}{1/g_m + R_s}$	$- \frac{R_D \parallel R_L}{1/g_m + R_s}$	
$\frac{1}{g_m}$	$g_m R_D$	R_D	$g_m(R_D \parallel R_L)$	$\frac{R_D \parallel R_L}{R_{\text{sig}} + 1/g_m}$	
∞	1	$\frac{1}{g_m}$	$\frac{R_L}{R_L + 1/g_m}$	$\frac{R_L}{R_L + 1/g_m}$	
	∞ ∞ $\frac{1}{g_m}$	$ \begin{array}{ccc} $	$R_{\rm in}$ A_{vo} R_o ∞ $-g_m R_D$ R_D ∞ $-\frac{g_m R_D}{1+g_m R_s}$ R_D $\frac{1}{g_m}$ $g_m R_D$ R_D	$R_{\rm in}$ A_{vo} R_o A_v R_o A_v R_D	

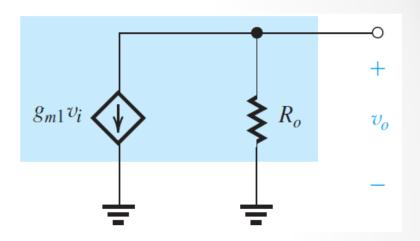


TABLE 6.5 Characteristics of BJT Amplifiers^{a, b, c}

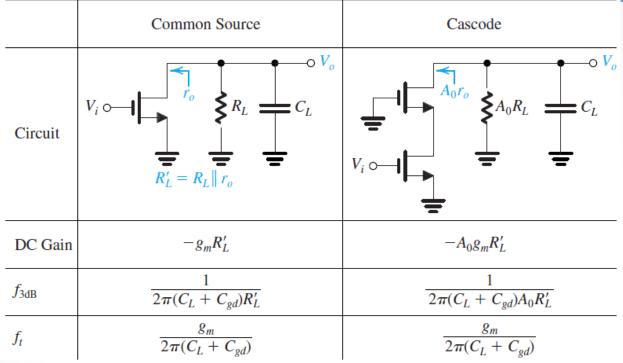
	$R_{ m in}$	A_{vo}	R_o	A_v	G_v
Common emitter (Fig. 6.50)	$(\beta+1)r_e$	$-g_mR_C$	R_C	$-g_m(R_C \parallel R_L) \\ -\alpha \frac{R_C \parallel R_L}{r_e}$	$-\beta \frac{R_C \parallel R_L}{R_{\text{sig}} + (\beta + 1)r_e}$
Common emitter with R_e (Fig. 6.52)	$(\beta+1)(r_e+R_e)$	$- \frac{g_m R_C}{1 + g_m R_e}$	R_C	$\frac{-g_m(R_C \parallel R_L)}{1 + g_m R_e}$ $-\alpha \frac{R_C \parallel R_L}{r_e + R_e}$	$-\beta \frac{R_C \parallel R_L}{R_{\text{sig}} + (\beta + 1)(r_e + R_e)}$
Common base (Fig. 6.53)	r _e	$g_m R_C$	R_C	$g_m(R_C \parallel R_L)$ $\alpha \frac{R_C \parallel R_L}{r_e}$	$\alpha \frac{R_C \parallel R_L}{R_{\text{sig}} + r_e}$
Emitter follower (Fig. 6.55)	$(\beta+1)(r_e+R_L)$	1	r_e	$\frac{R_L}{R_L + r_e}$	$\frac{R_L}{R_L + r_e + R_{\text{sig}}/(\beta + 1)}$ $G_{vo} = 1$ $R_{\text{out}} = r_e + \frac{R_{\text{sig}}}{\beta + 1}$
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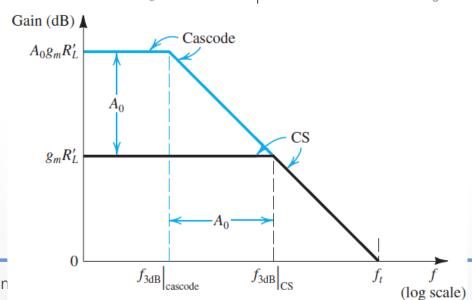
MOS Cascode



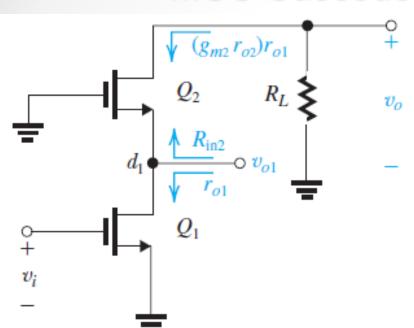


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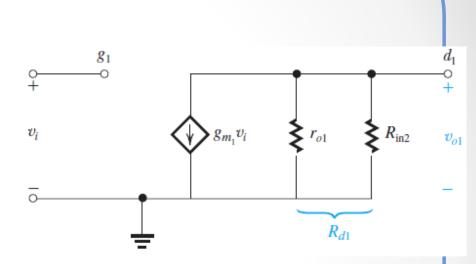
MOS Cascode: resistance

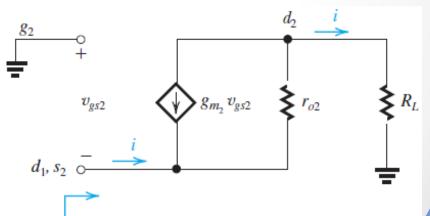


$$-v_{gs2} = (i + g_{m2}v_{gs2})r_{o2} + iR_L$$

$$R_{\rm in2} \equiv -v_{\rm gs2}/i$$

$$R_{\rm in2} = \frac{R_L + r_{o2}}{1 + g_{m2} r_{o2}}$$



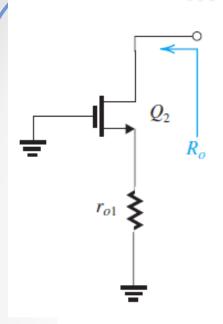


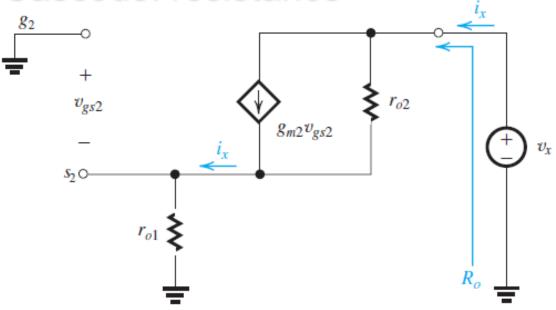


 $R_{\rm in2} \equiv \frac{-v_{\rm gs}}{2}$



MOS Cascode: resistance





$$R_o \equiv \frac{v_x}{i_x}$$

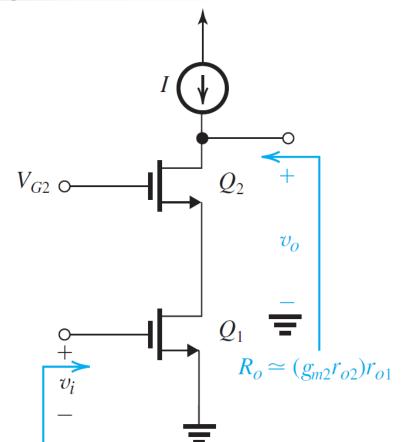
$$-v_{gs2} = i_x r_{o1}$$

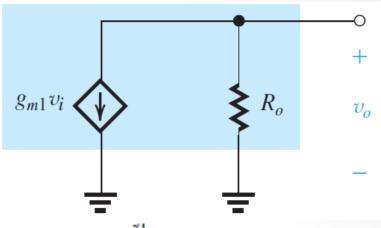
$$v_x = (i_x - g_{m2}v_{gs2}) r_{o2} + i_x r_{o1}$$

$$v_x = i_x(r_{o1} + r_{o2} + g_{m2}r_{o2}r_{o1})$$

$$R_o = r_{o1} + r_{o2} + g_{m2}r_{o2}r_{o1} \simeq (g_{m2}r_{o2})r_{o1}$$

MOS Cascode: voltage gain





$$A_{vo} = \frac{v_o}{v_i} = -g_{m1}R_o$$

$$A_{vo} = -g_{m1} x (g_{m2} r_{o2}) r_{o1}$$

$$A_{vo} = -(g_{m1}r_{o1}) (g_{m2}r_{o2})$$

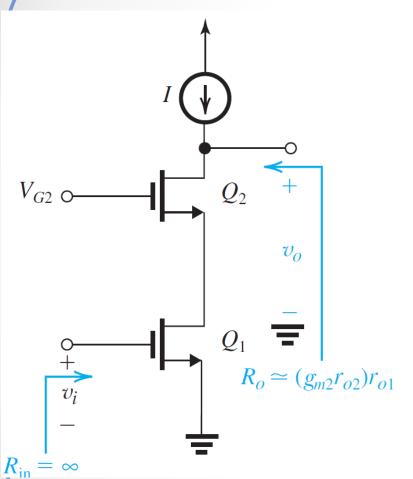
For the case $g_{m1} = g_{m2} = g_m$ and $r_{o1} = r_{o2} = r_o$,

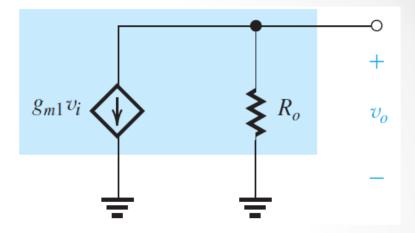
$$A_{vo} = -(g_m r_o)^2 = -A_0^2$$



 $R_{\rm in} = \infty$

MOS Cascode: voltage gain

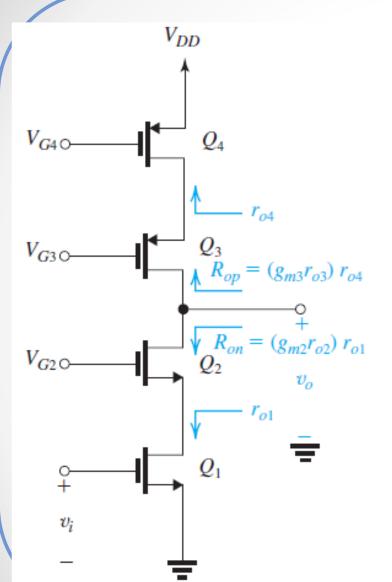


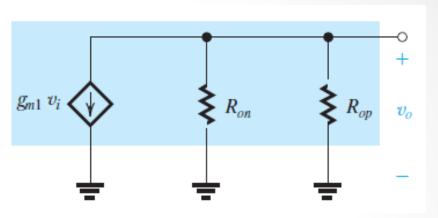


If there's a load resistance R_L connected to the output, the voltage gain will be

$$A_v = -g_{m1}(g_{m2}r_{o2}r_{o1} || R_L)$$

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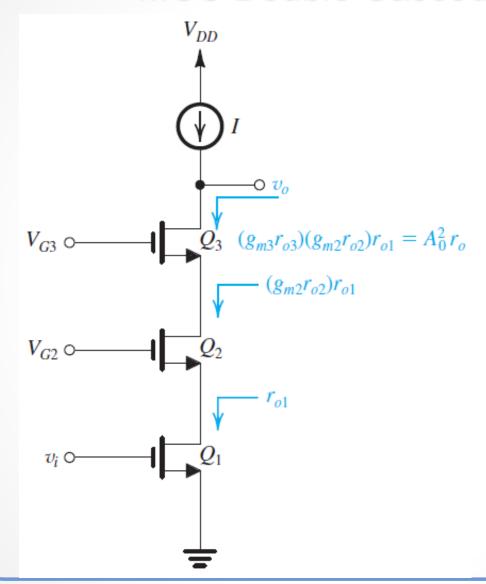




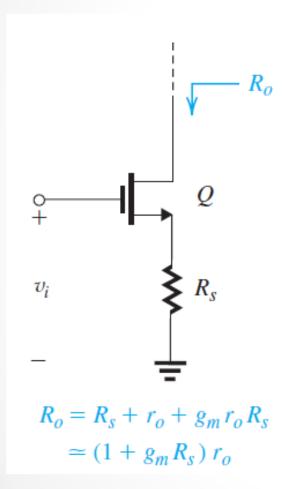
$$A_v = \frac{v_o}{v_i} = -g_{m1}[R_{on} || R_{op}]$$

$$A_v = -g_{m1}\{[(g_{m2}r_{o2})r_{o1}] \mid | [(g_{m3}r_{o3})r_{o4}]\}$$

MOS Double Cascode

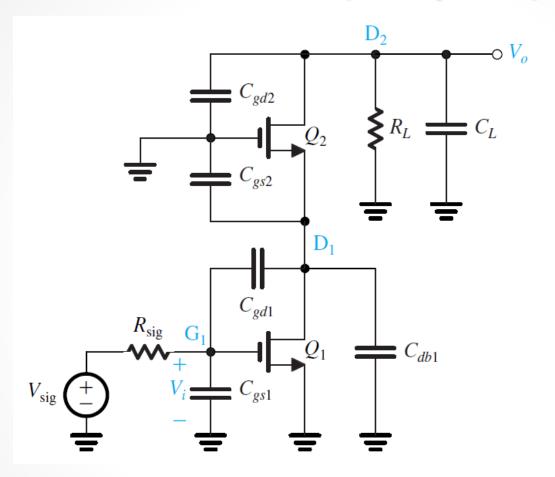


MOS Cascode: output resistance of a CS amplifier with degeneration resistor





MOS Cascode Frequency Response





MOS Cascode Frequency Response

We are going to use "open-ckt" time constant method to find f_H

- 1. Capacitance C_{gs1} sees a resistance R_{sig} .
- 2. Capacitance C_{gd1} sees a resistance R_{gd1} , which can be obtained by adapting the formula in Eq. (9.84) to

$$R_{gd1} = (1 + g_{m1}R_{d1})R_{sig} + R_{d1}$$
 (9.116)

where R_{d1} , the total resistance at D_1 , is given by

$$R_{d1} = r_{o1} \| R_{\text{in}2} = r_{o1} \| \frac{r_{o2} + R_L}{g_{m2} r_{o2}}$$
(9.117)

- **3.** Capacitance $(C_{db1} + C_{gs2})$ sees a resistance R_{d1} .
- **4.** Capacitance $(C_L + C_{gd2})$ sees a resistance $(R_L \parallel R_o)$ where R_o is given by

$$R_o = r_{o2} + r_{o1} + (g_{m2}r_{o2})r_{o1}$$

$$\begin{aligned} \tau_H &= \ C_{gs1} R_{\text{sig}} + C_{gd1} [(1 + g_{m1} R_{d1}) R_{\text{sig}} + R_{d1}] \\ &+ (C_{db1} + C_{gs2}) R_{d1} + (C_L + C_{gd2}) (R_L \parallel R_o) \end{aligned}$$

$$f_H \simeq \frac{1}{2\pi\tau_H} -$$









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References

Microelectronic Circuits by Adel S. Sedra & Kenneth C. Smith. Saunders College Publishing

"Chapter 7: Frequency Response", a lecture note by Prof. Yang Hua, Ph.D., Department of Electronic Engineering, Shanghai Jiao Tong University (SJTU), Shanghai, China