King Mongkut's University of Technology Thonburi
Midterm Exam of Second Semester, Academic Year 2007

CPE 311 Microprocessor Based System Design **Computer Eng. Department**

Friday 21st December 2007 **09.00-12.00 h.**

Instructions

1. Calculator, paper dictionary and ruler with mathematical formula are allowed in the examination room.
2. Books, documents, and notes are **allowed** in the examination room.
3. Do not take the examination sheets out of the examination room.
4. This examination has 8 pages (4 problems, 80 points).
5. If students find any problem from the problems, Write comments and solve the problem with the new assumptions.

Students will be punished if they violate any examination rules. The highest punishment is dismissal.

This examination is designed by

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1. **From the technical Datasheet of the ATMEGA 8 below, answer questions**
(Correct Answer: points, Incorrect Answer: -1 points, No answer: 0 point)

ATMEGA 8 FEATURES: --- DATASHEET !

• High-performance, Low-power AVR® 8-bit Microcontroller

• Advanced RISC Architecture

– 130 Powerful Instructions – Most Single-clock Cycle Execution

– 32 x 8 General Purpose Working Registers

– Fully Static Operation

– Up to 16 MIPS Throughput at 16 MHz

– On-chip 2-cycle Multiplier

• Nonvolatile Program and Data Memories

– 8K Bytes of In-System Self-Programmable Flash

Endurance: 10,000 Write/Erase Cycles

– Optional Boot Code Section with Independent Lock Bits

In-System Programming by On-chip Boot Program

True Read-While-Write Operation

– 512 Bytes EEPROM

Endurance: 100,000 Write/Erase Cycles

– 1K Byte Internal SRAM

– Programming Lock for Software Security

• Peripheral Features

– Two 8-bit Timer/Counters with Separate Prescaler, one Compare Mode

– One 16-bit Timer/Counter with Separate Prescaler, Compare Mode, and Capture Mode

– Real Time Counter with Separate Oscillator

– Three PWM Channels

– 8-channel ADC in TQFP and MLF package

Eight Channels 10-bit Accuracy

– 6-channel ADC in PDIP package

Eight Channels 10-bit Accuracy

– Byte-oriented Two-wire Serial Interface

– Programmable Serial USART

– Master/Slave SPI Serial Interface

– Programmable Watchdog Timer with Separate On-chip Oscillator

– On-chip Analog Comparator

1.1 Which information implied that "ATMEGA8 had high speed computing ability" (2 points)

1.2 What is the meaning of RISC Architecture? How different between RISC and other Architectures? (2 points)

1.3 How different between EEPROM and Self -Programmable Flash ? (2 points)

1.4 There are 32*8 General Purpose Register in ATMEGA8. Where and what type of memories are they? (2 points)

1.5 Give the initial and last address of the flash program memory (Hexadecimal number) (4 points)

1.6 How many bytes of the total memory does ATMEGA8 have? (4 points)

1.7 What is the meaning of "8" after the word "ATMEGA" (2 points)

1.8 Give the special fatures of ATMEGA8 that are different from other microprocessor (2 points)

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2. **Fill in the blank. (20 points)**

Define Data in every memory has the initial value as $FF and the initial value of all "General Purpose Registers" are $00.

2.1

Line No.	Program
1.	.dseg
2.	.org $60
3.	cpe18: .byte 2
4.	.cseg
5.	ldi r28, low(cpe18)
6.	ldi r29, high(cpe18)
7.	ld r16, Y+
8.	ldi r17, 27
9.	add r16, r17
10.	std Y+1, r16

Fill in the hexadecimal data in the memory.

2.1.1 After finishing the third line command.

Data Memory

Address	Data
$0060	
$0061	
$0062	

2.1.2 After finishing the sixth line command.

	High byte	Low Byte
Y- Register		

2..1.3 After finishing the seventh line command.

	High byte	Low Byte
Y- Register		

2.1.4 After finishing the eighth line command

Register	Data
R16	
R17	

2.1.5 After finishing the tenth line command.

Data Memory

Address	Data
$0060	
$0061	
$0062	
$0063	

2.2 The program below was a sine wave generator code from one of our lab. Answer the questions. (Students can write or draw on the code to refer the answer to the code)

```
 .INCLUDE "m8def.inc"

.DEF rmp = R16
        ldi rmp,0xFF
        out DDRB,rmp
        ldi ZH,HIGH(2*SineTable)
        ldi ZL,LOW(2*SineTable)
        clr rmp
loop1:
        nop
        nop
        nop
loop2:
        lpm
        out PORTB,R0
        adiw ZL,1
        dec rmp
        brne loop1
        ldi ZH,HIGH(2*SineTable)
        ldi ZL,LOW(2*SineTable)
        rjmp loop2

Sinetable:

.DB 64,65,67,68,70,72,73,75
.DB 76,78,79,81,82,84,85,87
.DB 88,90,91,92,94,95,97,98
.DB 99,100,102,103,104,105,107,108
.DB 109,110,111,112,113,114,115,116
.DB 117,118,118,119,120,121,121,122
.DB 123,123,124,124,125,125,126,126
.DB 126,127,127,127,127,127,127,127
.DB 128,127,127,127,127,127,127,127
.DB 126,126,126,125,125,124,124,123
.DB 123,122,121,121,120,119,118,118
.DB 117,116,115,114,113,112,111,110
.DB 109,108,107,105,104,103,102,100
.DB 99,98,97,95,94,92,91,90
.DB 88,87,85,84,82,81,79,78
.DB 76,75,73,72,70,68,67,65
.DB 64,62,61,59,58,56,54,53
.DB 51,50,48,47,45,44,42,41
.DB 39,38,36,35,34,32,31,30
.DB 28,27,26,25,23,22,21,20
.DB 19,18,17,15,14,13,13,12
.DB 11,10,9,8,8,7,6,5
.DB 5,4,4,3,3,2,2,2
.DB 1,1,1,0,0,0,0,0
.DB 0,0,0,0,0,0,1,1
.DB 1,2,2,2,3,3,4,4
.DB 5,5,6,7,8,8,9,10
.DB 11,12,13,13,14,15,17,18
.DB 19,20,21,22,23,25,26,27
.DB 28,30,31,32,34,35,36,38
.DB 39,41,42,44,45,47,48,50
.DB 51,53,54,56,58,59,61,62
```

2.2.4 Modify the code in order to generate full wave signal

2.2.5 How can adjust the code to define the frequency of the full wave signal from question 2.2.1

Hint : Full Wave is a Sine Wave that has only positive amplitude.

3. Write a delay subroutine for 1 second, using assembly, on an ATMEGA8 with 8 Megahertz of clock and show the calculation and program description. (20 points)

4. This program is for 16-bit unsigned number and 16-bit signed number multiplication. Debug the program and Fill the contents for related registers and Flag. (<u>all question and answer are hexadecimal number</u>) (20 points)

(HINT: Singed Number is negative number. Ex. 0x9C = - 2's compliment (0x9C) = - 0x64)

2's compliment (0101 1001) = (1010 0110 + 1) = (1010 0111) ----- *** Binary ***

OUTPUT (R19:R18:R17:R16) = R23:R22 x R21:R20

INITIAL DATA before execution:

R19	R18	R17	R16	R23	R22	R21	R20	R2	R1	R0	N	C	Z
00	00	00	00	**9C**	**6F**	**A5**	**40**	00	00	00	0	0	0

		Register after execution code									
Line	**CODE**	**R19**	**R18**	**R17**	**R16**	**R2**	**R1**	**R0**	**N**	**C**	**Z**
1	CLR R2					**00**					**1**
2	MULS R23,R21										
3	MOVW R19:R18, R1:R0										
4	MUL R22,R20										
5	MOVW R17:R16, R1:R0										
6	MULSU R23,R20										
7	SBC R19,R2										
8	ADD R17,R0										
9	ADC R18,R1										
10	ADC R19, R2										
11	MULSU R21,R22										
12	SBC R19,R2										
13	ADD R17,R0										
14	ADC R18,R1										
15	ADC R19,R2										