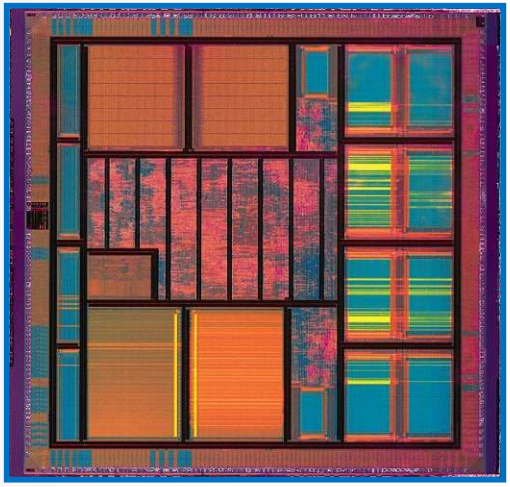
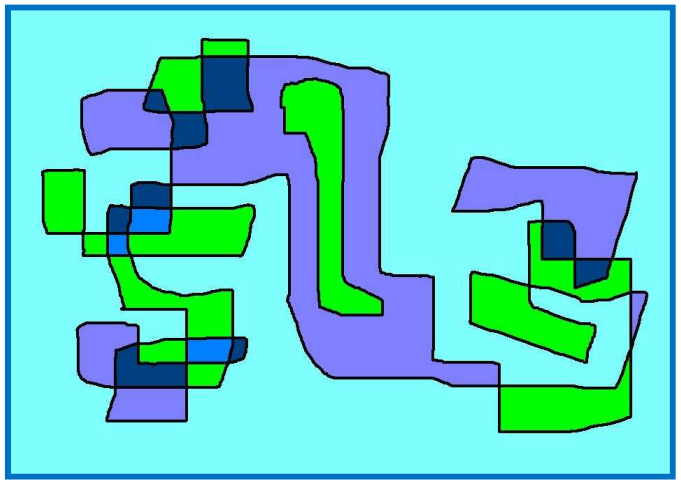
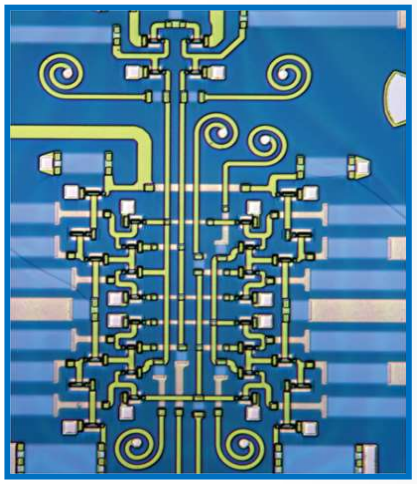




ENE/EIE 211 : Electronic Devices and Circuit Design II

Lecture13: Noise Reduction Techniques and PCB Design

- **Terminology**

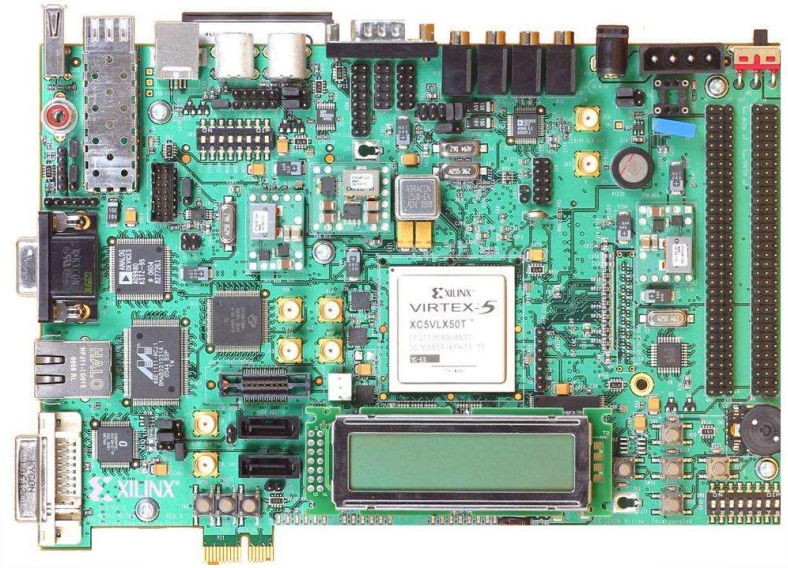
"PCB"= Printed Circuit Board (i.e., a "board")

"PWB"= Printed Wiring Board (same as PCB)

"PCA"= PCB Assembly, a PCB that is loaded with components

"Fab" = the process of creating the PCB

"Load"= the process of attaching the components to the PCB



- **Printed Circuit Board** is a structure that:
  1) mechanically support components
  2) provides electrical conduction paths between circuits

- **Construction**

- there are a variety of methods to create a PCB.
- the general approach is to start with a sheet of copper attached to an insulator and then remove copper leaving only your desired interconnect pattern.
- this is called a *subtractive* method and is the most common technique.

- we'll first go over all of the major process steps used in creating a PCB.

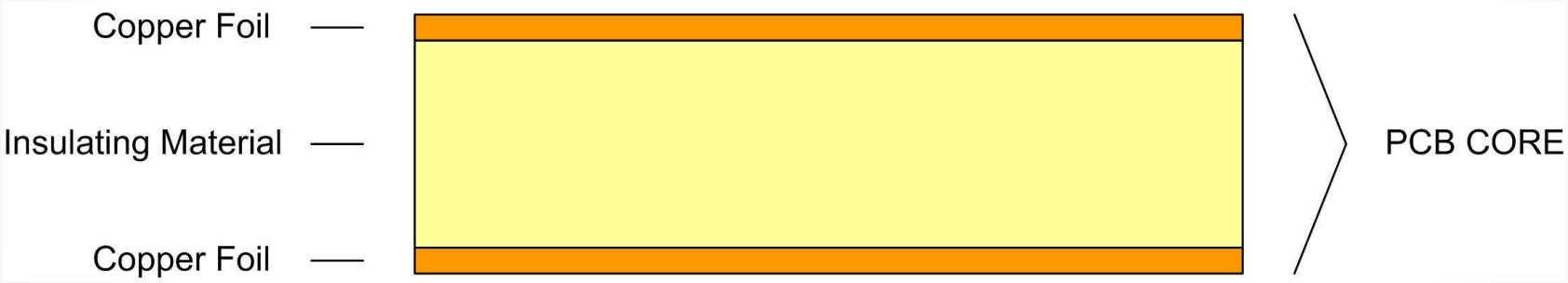
1) The CORE
2) Patterning
3) Vias
4) Pattern Plating
5) Solder Mask
6) Surface Finish
7) Silk Screening

- then we'll put them together in the appropriate sequence from start to finish.

PCB: Core

- **The CORE**

  - the base element to a PCB is called the “CORE”
  - this typically consists of two sheets of thin copper laminated (or glued) to an insulating material.



- the insulator is commonly call the “Substrate” or the “Laminate”

- this construction is also called a “Copper Clad” insulator

- COREs come in large sheets which are typically ~18” x 24” *(but can be as large as 24” x 48”)*

PCB: Core

- **The CORE**

CORE Conductors

- the most commonly used conducting material is *Copper (Cu)*

- the thickness of the copper sheet is specified in terms of its *weight*:

2oz	=	70 um	= 0.0024”	The term “weight” refers to the weight in
1oz	=	35 um	= 0.0012”	ounces per square foot”
0.5oz	=	17.5 um	= 0.0006”	
0.25oz	=	8.75 um	= 0.0003”	We sometimes call this sheet a “foil”

PCB: Core

- **The CORE**

CORE Insulators

- there are many different types of insulating material, each with varying degrees of:

  - Cost
  - Dielectric Constants
  - Electrical Performance (i.e,. Disipation factor = loss tangent)
  - Mechanical Robustness (rigidity, peel-strength, CTE)

- COREs are typically reinforced with a weave of fiber

- FR4 (Fire Retardant Epoxy #4) is the most common dielectric in use today.

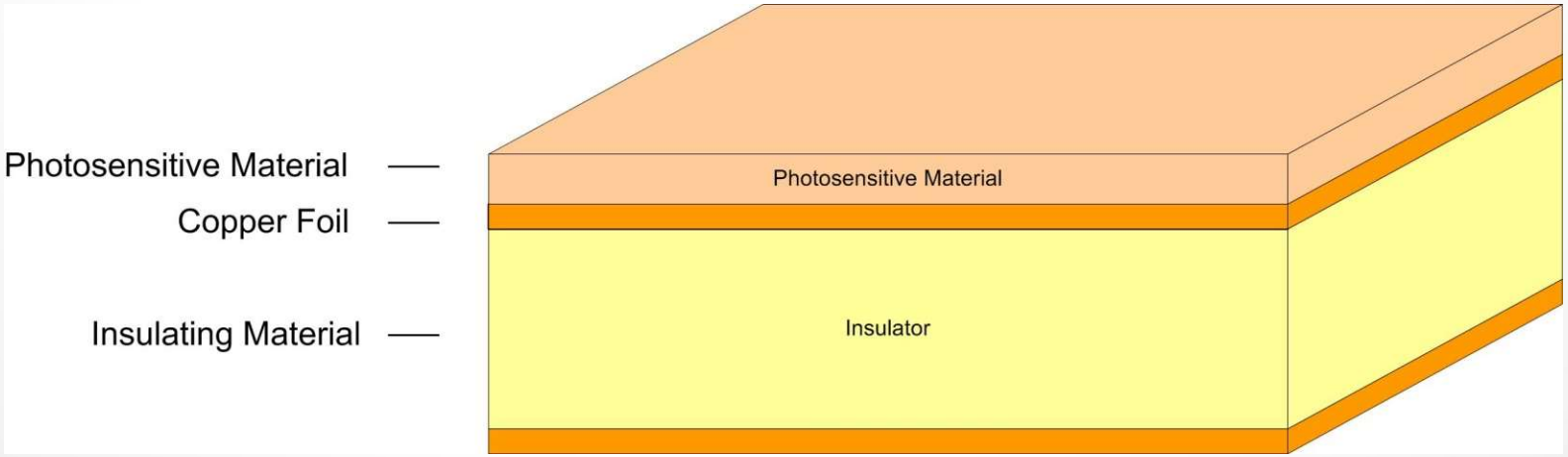
PCB: Patterning

Patterning

- there are 2 common techniques to remove material from the core to leave only the desired conduction paths.

1) Photoengraving / Photolithography

- a photomask is created by *printing* a design pattern onto a translucent material.
- this is very similar to printing an overhead transparency using a laser printer.
- the CORE is then covered in a photosensitive material (photosensitive dry film, or photoresist).
- when the photosensitive material is exposed to light, its properties change.

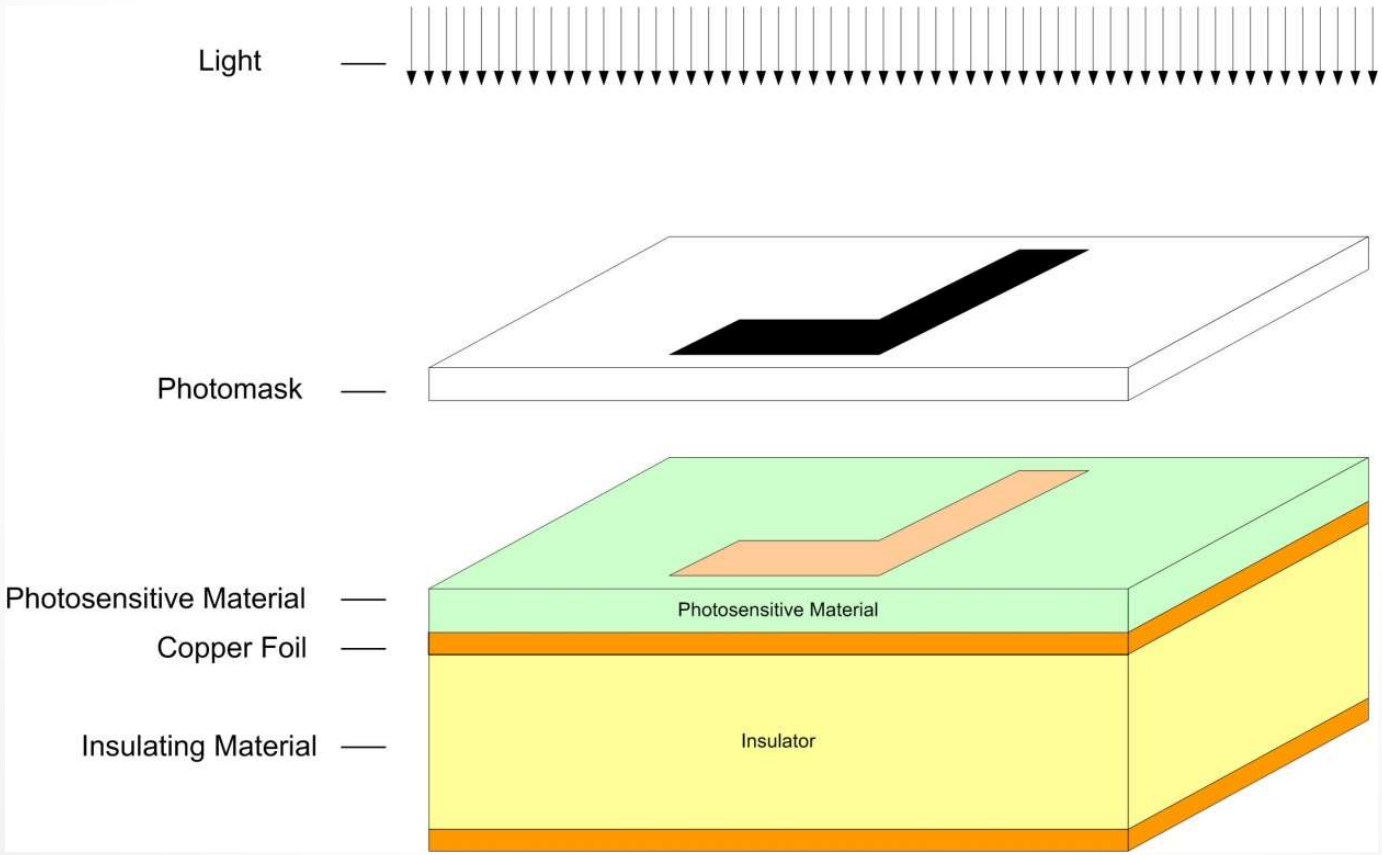


PCB: Patterning

- **Patterning**

1) Photoengraving / Photolithography cont…

- the CORE is ***exposed*** to a light source through the photomask
- a solution is then applied that ***develops*** the photosensitive material making is soluble.



PCB: Patterning

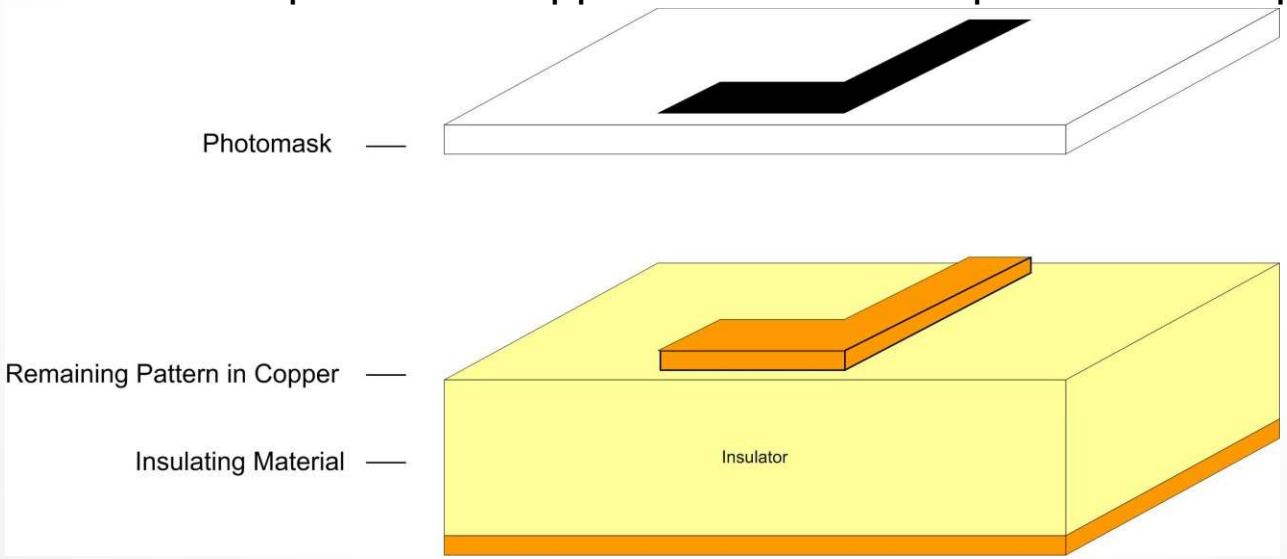
- **Patterning**

1) Photoengraving / Photolithography cont…

- an *etching* solution is then applied to the CORE which removes the "*now soluble*" photosensitive material in addition to the copper foil beneath it.

- this etching step removes any copper on the CORE that was exposed to light through the photomask, thus transferring the pattern.

- once the remaining photosensitive material is ***stripped*** using a cleaning solution, the CORE is left with a pattern of copper identical to the pattern on the photomask.

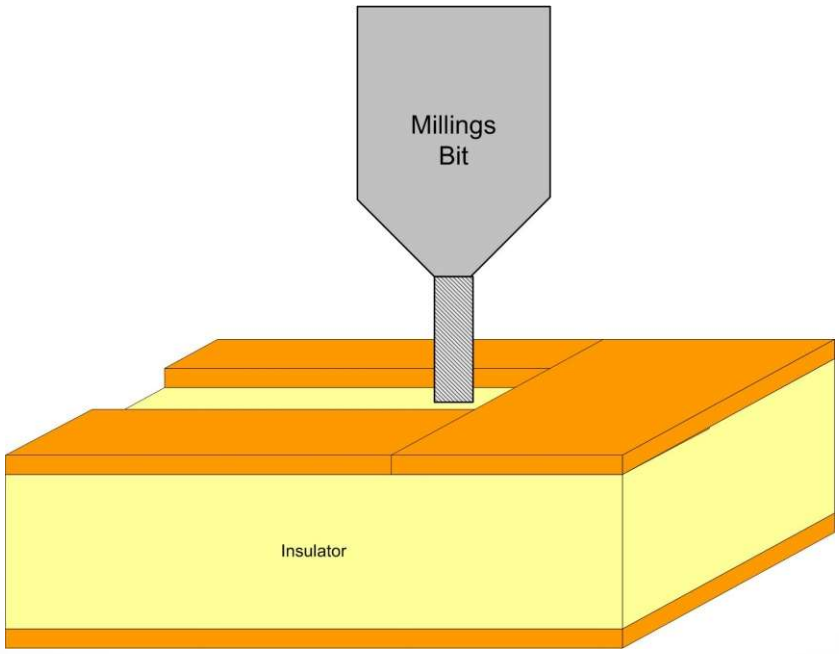


PCB: Patterning

- **Patterning**

2) PCB Milling

- another subtractive technique is to use a a milling bit (similar to a router or drill bit) to mechanically remove copper from the CORE leaving only the desired pattern.



PCB: Vias

- **Vias (Drilling)**

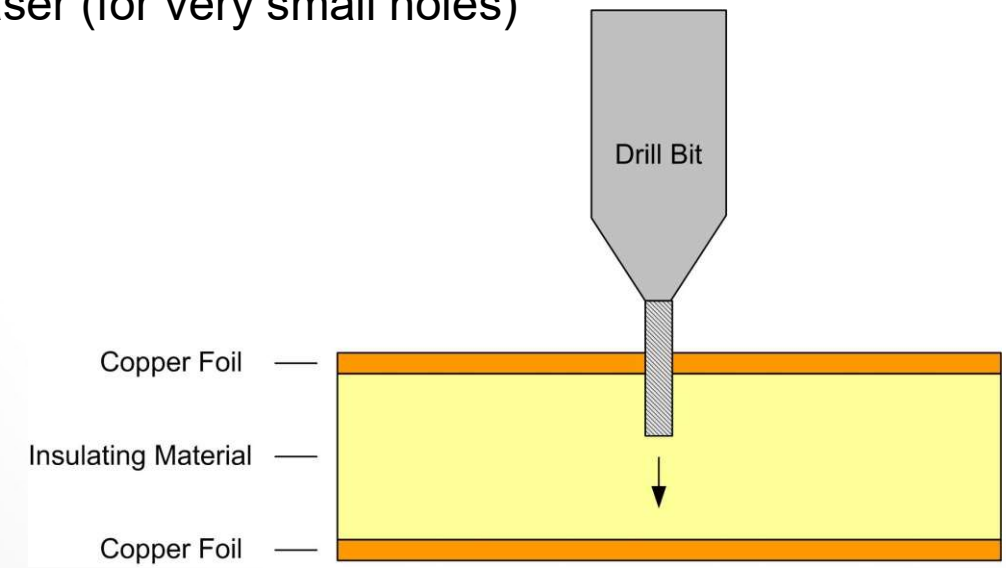
- A via is a structure that electrically connects two different layers of copper in a PCB.

- the first step in creating a via is to drill a hole where the contact will be made.

- this can be done using:

1) A mechanical process (i.e., a regular drill bit). This is currently the most common approach. or

2) A laser (for very small holes)

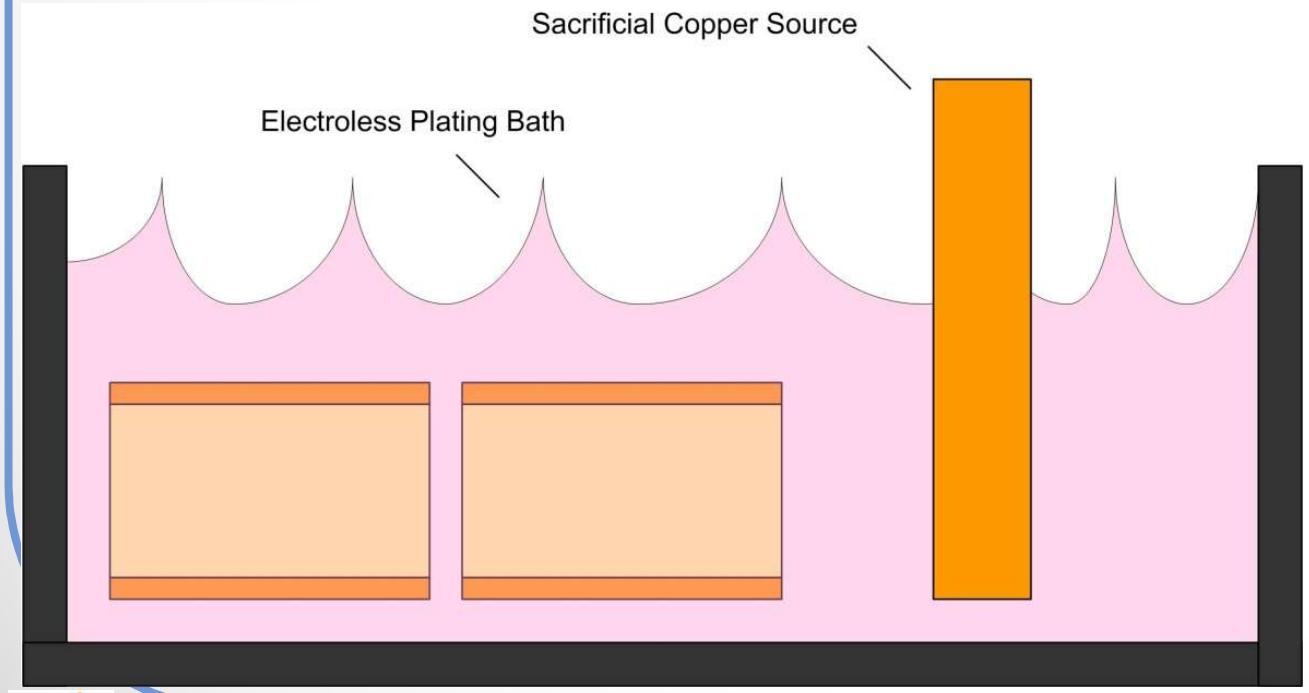


PCB: Vias

- **Vias (Electroless Plating)**

  - The next step in creating a via is to deposit Copper into the holes in order to **Plate** the inner diameter of the via with a conducting material.

  - PCB Via plating is accomplished by an *Electroless Plating Process* in which a series of chemical reactions are performed to transfer copper atoms from a *Sacrificial Copper Source* to the barrels of the via holes.



NOTE:

"Electroplating" is where the metal source is ionized and drawn to the target using an electric field.

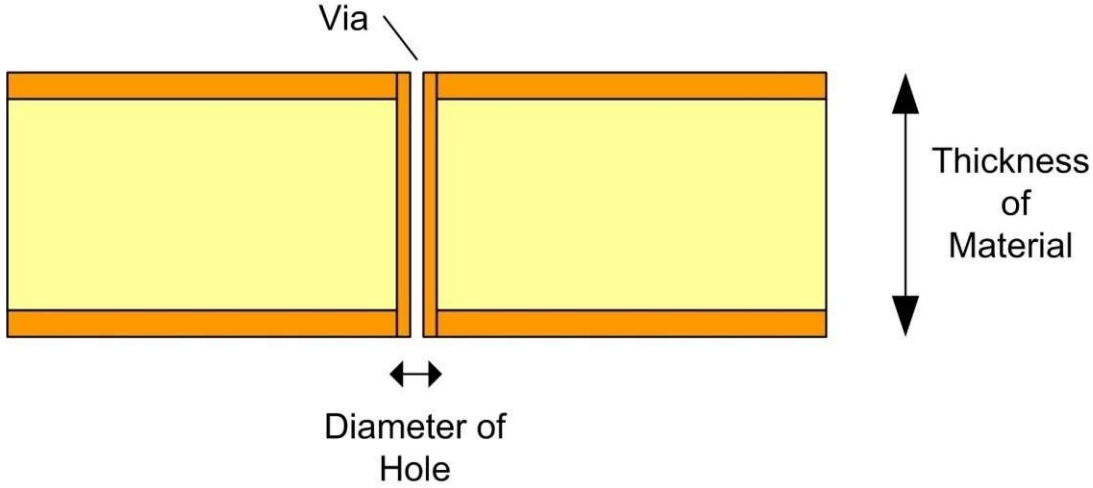
"Electroless Plating" uses a chemical reaction to release hydrogen from the target in order to create a negative charge and attract the plating metal to its surface.

PCB: Vias

- **Vias**

- The end result is a structure that connects different layers of a PCB.

- The “via” is also called a “Plated Through Hole”



NOTE: The **Aspect Ratio** is the ratio of the *Thickness of the Hole* (or Depth) to be plated to the *Diameter of the Hole*. If the aspect ratio is too large (i.e., deep & skinny holes), then the copper plating will not reach the center of the hole and result in an open circuit.

$$\text{Via Aspect Ratio} = \frac{Depth}{Diamter}$$

PCB fab shops will specify the maximum aspect ratio they can achieve (typically ~4-6)

PCB: Pattern Plating

- **Pattern Plating**

- the copper deposited from the *Electroless Plating* step applies a thin layer of copper on the entire surface of the CORE in addition to inside the drilled via holes.

- the plating in the via barrels is typically not thick enough (i.e., <0.001") to be reliable. To address this, a second *Electrochemical* plating is performed.

- *pattern plating* deposits a material over the copper circuitry that will protect it during a subsequent etch stage. A material such as *tin* can be used to cover the copper traces to protect them.

- the copper is first thickened using an additional *Electrochemical* plating process.

- once applied, the tin is deposited on the pattern.

- after the etch, the tin can be *stripped* off or left on depending on the manufacturer.

PCB: Solder Mask

- **Solder Mask**

- solder mask is a protective insulating layer that goes over the outer sides of the PCB.
NOTE: this is typically the *green* material you see on boards.

- copper is very susceptible to oxidation so if the pattern is going to be exposed to ambient air, they need to receive additional plating to protect against oxidation.

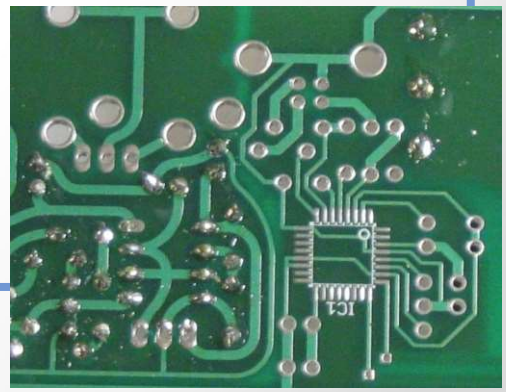
- oxidation is the reaction of oxygen with the copper. During this process, the copper is actually *consumed.* So a thin layer of copper can actually be completely oxidized into an insulator.

- solder mask is a layer of polymer that can be applied using either *silk screening* or a spray.

- the solder mask covers all conducting circuits on the board with the exception of any *pads* that components will connect to.

NOTE: The word "*pad*" has special meaning in PCBs. It indicates that a shape of metal:

1) will be used to connect to a component
2) will *not* be covered by solder mask
3) will receive a surface finish (next step)
4) will receive a layer of *solder paste* prior to component loading *(later)*



PCB: Surface Finish / Solder Coat

- **Surface Finish**

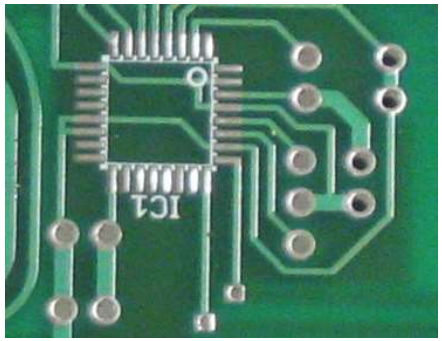
- also referred to as Solder Coat or Exposed Conductor Plating
- the *pads* of a board must receive a special surface finish to:

    1) resist oxidation from long periods of storage while waiting for loading
    2) prepare them for the application of solder

- to accomplish this, a layer of conducting material is applied to the pads after solder masking.

Ex)	Tin-Lead Solder	(industry is trying to move to “lead free” plating)
	Gold	
	Silver	(Lead-Free compliant, ROHS)

- this step is what gives the pads on the board the *shiny* look that you see



PCB: Silkscreen

- **Silk screening**

- silk screening is the process of adding documentation to the board.

- the term *silk screen* refers to the process of transferring a pattern using a special *stencil.*

- a *stencil* is a sheet of material that has physical openings in it that represent the pattern to be transferred.

- in a silk screen stencil, the openings are typically a set of small dots (i.e., a *screen*)

- the stencil is laid on top of the board and then a documentation material is applied to the entire board using a roller & *squeegee* or *spray.*

- when the stencil is removed, the documentation material remains in the pattern of the openings on the stencil.

- the board is then baked to harden the documentation material.

PCB: Silkscreen

- **Silk screening**

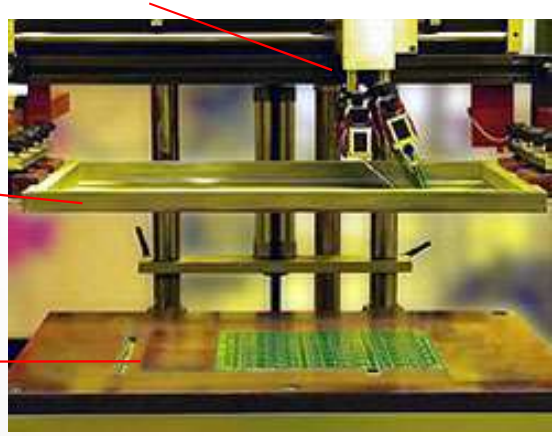
- you typically cannot draw silk screen lines that are smaller than the copper due to the resolution of the screening process.

- when looking at how small of a line can be drawn using a silk screen, manufacturers typically talk about LPI (lines per inch). In general, the smallest silk screen lines are ~0.008”

Applicator & squeegee

Silk screen stencil

Board to receive the silk screen



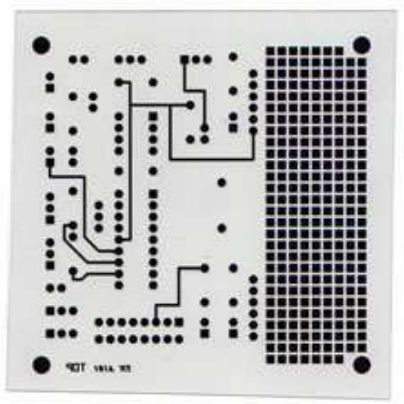
silk screen machine

patterns remaining after silk screen

2 Layer PCB Example

- **Step 1 – Photomask**

  - we create our design in a CAD tool (i.e., Mentor PADS) which generates files to create a photomask



- **Step 2 – Material Selection**

  - we now select a core that meets our application needs (Dk, loss tangent, copper weight, etc…)

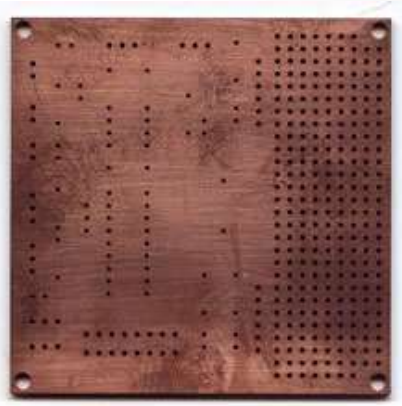
  - this core will be used to create our PCB.

NOTE: 2 Layer Example Images from *PCBexpress.com*

2 Layer PCB Example

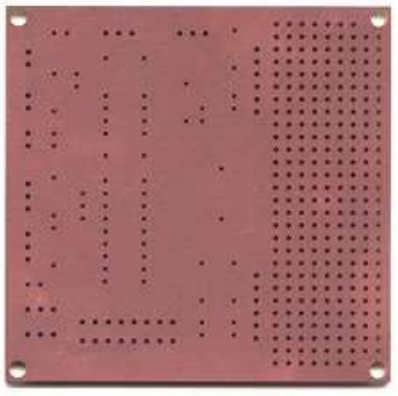
- **Step 3 – Drilling**

  - we now drill through holes where vias are going to be located.



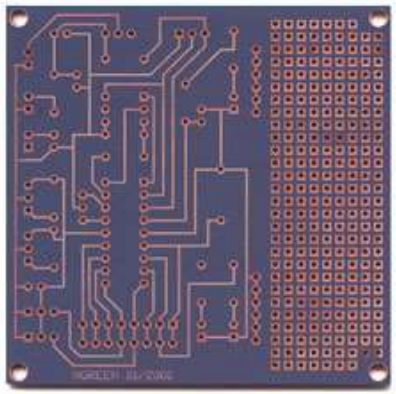
- **Step 4 – Electroless Plating of Vias**

  - we now put the board through an Electroless plating process which deposits copper inside of the via drill holes.



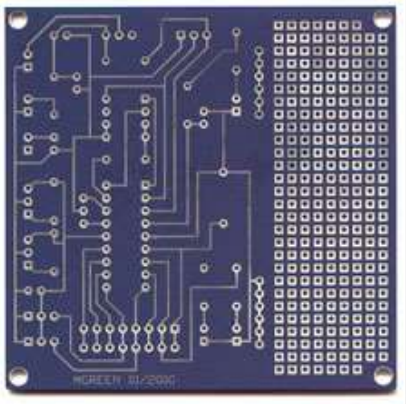
2 Layer PCB Example

- **Step 5 – Apply Pattern**



- we now transfer the pattern from our photomask to the core by:
  - applying photosensitive film (photo resist) to the CORE.
  - align photomask to the CORE
  - expose to UV light which changes the properties of the exposed photo resist
  - apply developing solution to make the exposed photoresist soluble

- **Step 6 – Pattern Plating**



- since the current copper patterns are going to be on the outer sides of the board, they require additional steps to ensure that oxidation doesn't completely consume the metal.
- the board undergoes an additional electrochemical plating step that adds additional copper to the existing copper traces and via barrels.

- a layer of tin is then added to the surface to protect the copper from the ensuing etch.

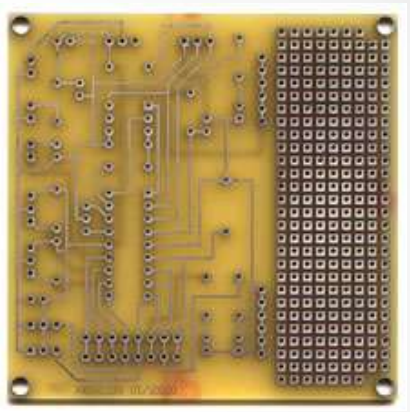
2 Layer PCB Example

- **Step 7 – Strip & Etch**

  - we now *strip* the photo resist layer off of the core exposing the unwanted copper.

  - an *etch* is performed which removes all of the unwanted copper.

  - the copper circuitry is protected by the tin and remains after the etch.

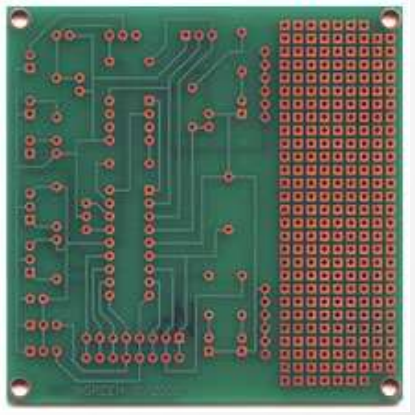


- **Step 8 – Solder mask**

  - an insulating layer of solder mask is applied to the core.

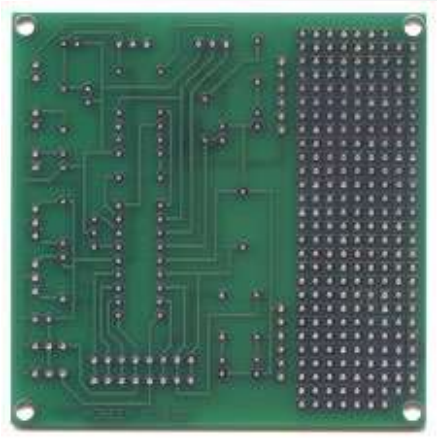
  - the solder mask covers all of the conductors with the exception of any *pads* that are to be used to connect to components.

  - this layer provides protection against inadvertent shorting of the conductors.



2 Layer PCB Example

- **Step 9 – Surface Finish**



- the pads that are visible through the solder mask will ultimately make contact to components using solder.

- In order to prepare the pads for the components, a layer of material is applied to the pads that:

    - is easily soldered to (i.e., Solder, Gold, or Silver)
    - that prevents any oxidation on the pads so that the board can be stored while waiting for load.

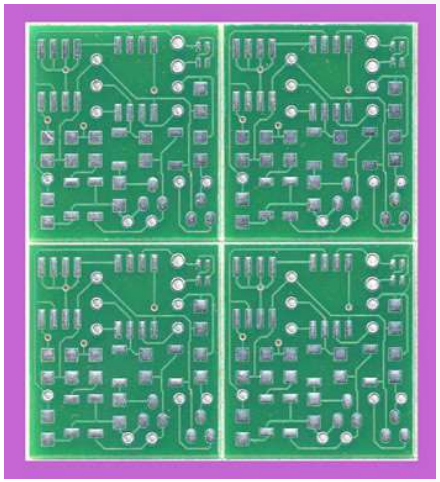
- **Step 10 – Silk Screen**

- documentation is now added to the board using a silk screen material.
- documentation is important for:

    - board identification
    - component locators
    - component orientations

2 Layer PCB Example

- **Step 11 – De-Panelization**



- typically, multiple images of the same PCB are put on one *panel* for processing.

- this allows the previously described process steps to create multiple boards in the same amount of time.

- the last step is to *de-panelize*, or route out the individual boards.

NOTE: Some automated loading processes can load the boards while still panelized.

Multi Layer PCBs

- **Multi Layer PCBs**

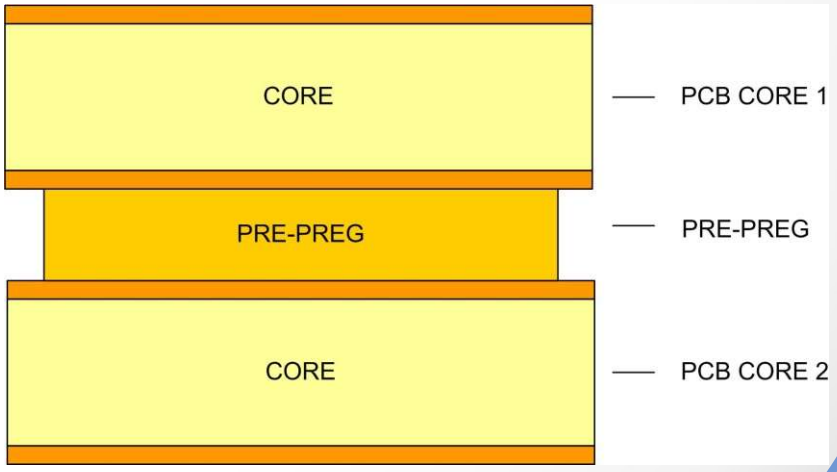
- the same set of steps can be used to create PCB's with more than 2 layers.

- in this case, multiple cores are patterned and then *laminated* together using an insulator material called a *pre-preg*

- the pre-preg serves as an insulator but has an adhesive property to it that *glues* the cores together.

- the pre-preg material can be the same insulating material as the core.

NOTE: this construction process is why boards always come with an EVEN number of layers (i.e., 2 layer, 4 layer, 6 layer, 8,…)



Multi Layer PCB

Multi Layer PCBs

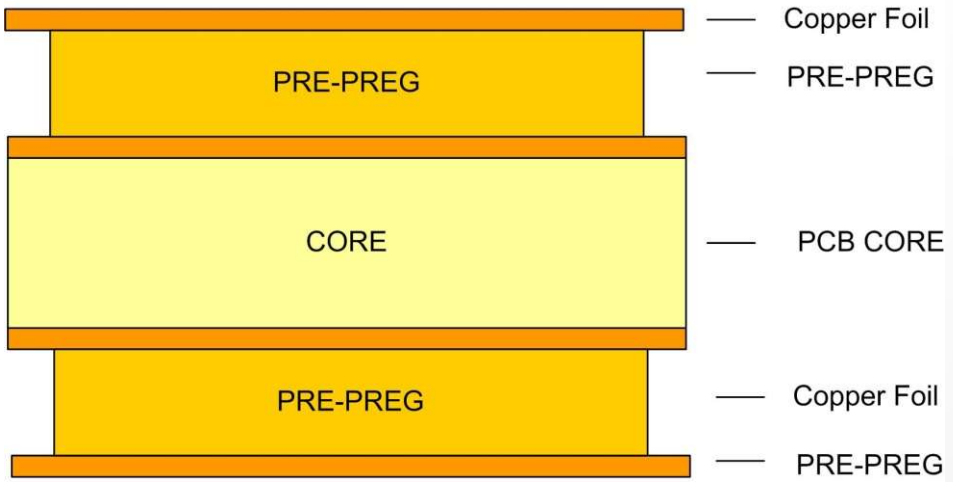
- **Multi Layer PCBs**

  - the resultant *stack* of layers is called a “stackup”

  - outer layers can be added to the stack by applying a pre-preg to the core and then laminating a copper foil on top of it.

  - the entire stack (core + pre-pregs) are put into a press.

  - the press applies pressure and temperature in order to bond the materials together into one rigid assembly.



4 Layer PCB

Multi Layer PCBs

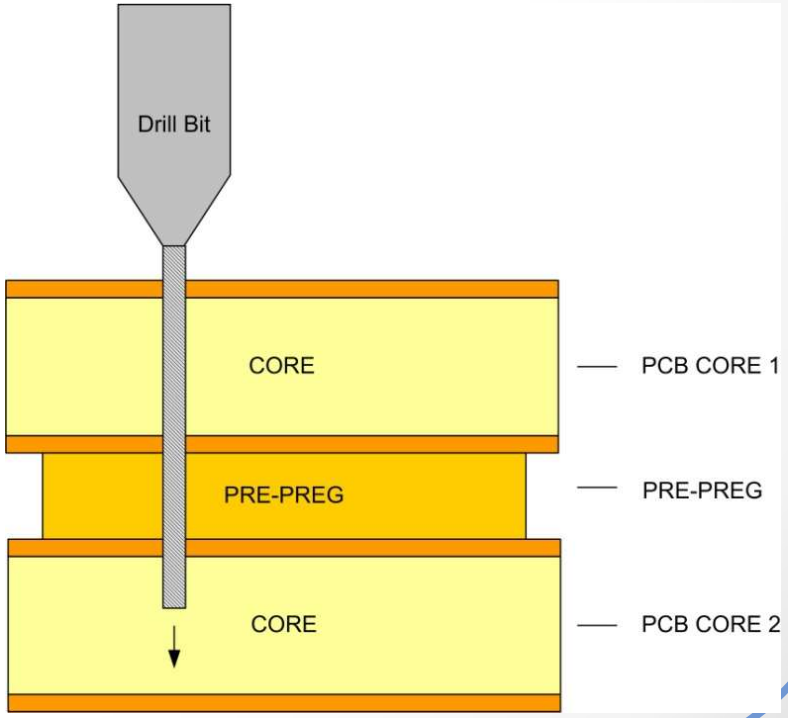
- **Multi Layer PCBs**

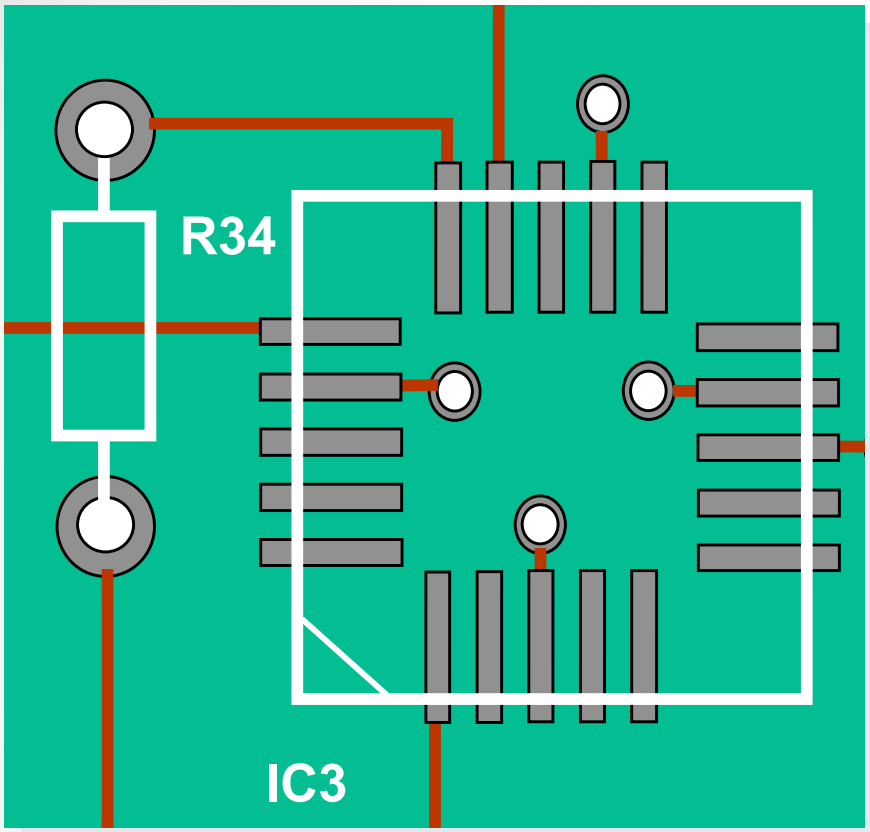
- creating multi-layer PCBs involves some changes to the fabrication process.

  1) Drilling occurs after the final lamination takes place.

  2) The inner layer traces are patterned prior to drilling and lamination and DO NOT need to undergo the pattern plating and surface finish step.

- notice that the through-hole vias will extend through the entire thickness of the board even if the desired connectivity is between the top two layers.





Noises in Electronic Systems

An IEEE Definition of Noise

- The IEEE standard dictionary of Electrical and Electronics Terms defines noise as unwanted disturbanaces superposed upon a useful signal that tend to obscure its information content.

- Applies both to intrinsic and extrinsic noise
  - Intrinsic noise is generated inside component themselves
  - Extrinsic noise designates noise originating elsewhere

Extrinsic Noise (interference)

- Due to:
  - Cross-talk between circuits
  - EM (Lightning)
  - Grounding issues
  - Unwanted coupling of AC power supply + harmonics

- Examples (symptoms of)
  - AM/FM radio (especially AM) during lightning storm
  - “Hum” or “buzz” of electric guitar (from lights, etc)
  - When using portable phone and hear unwanted third party conversation on the line

Intrinsic Noise

- Due to:
  - Resistor Thermal Noise
  - BJT/diode shot noise
  - MOS thermal (broadband) and flicker (low-freq) noise
- Examples (symptoms of)
  - The “shhhhh” sound of analog TV when signal lost
  - “snow” on the TV screen when signal lost
  - Tape “hiss” heard in old recordings

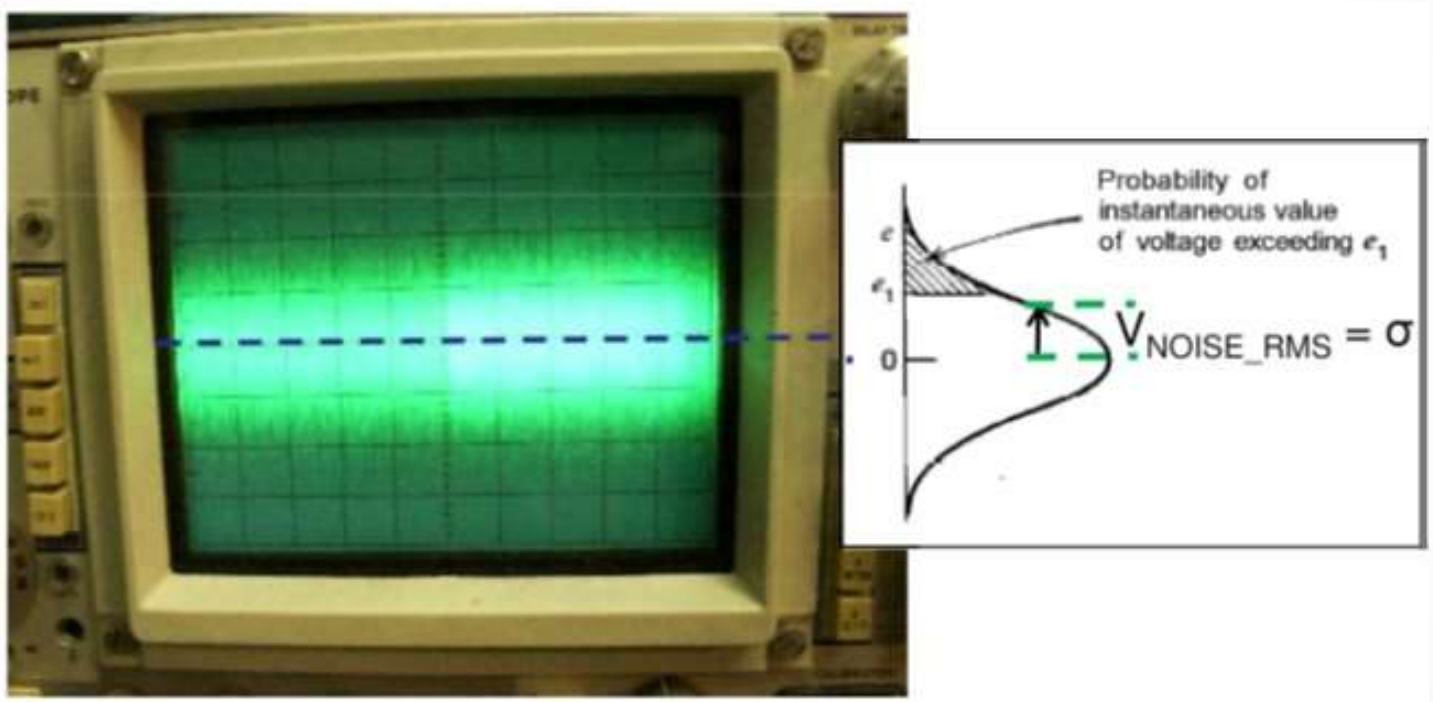
Two General Categories of Noise

- Extrinsic
  - "Interference", a better term
  - Unwanted signals coupled from sources outside, not due to circuit elements themselves
- Solutions: topology choice, grounding, shielding

- Intrinsic
  - "Fundamental noise"
  - Inherent to all active devices, resistors
  - Statistical in nature
- Solutions: careful design to minimize the effect

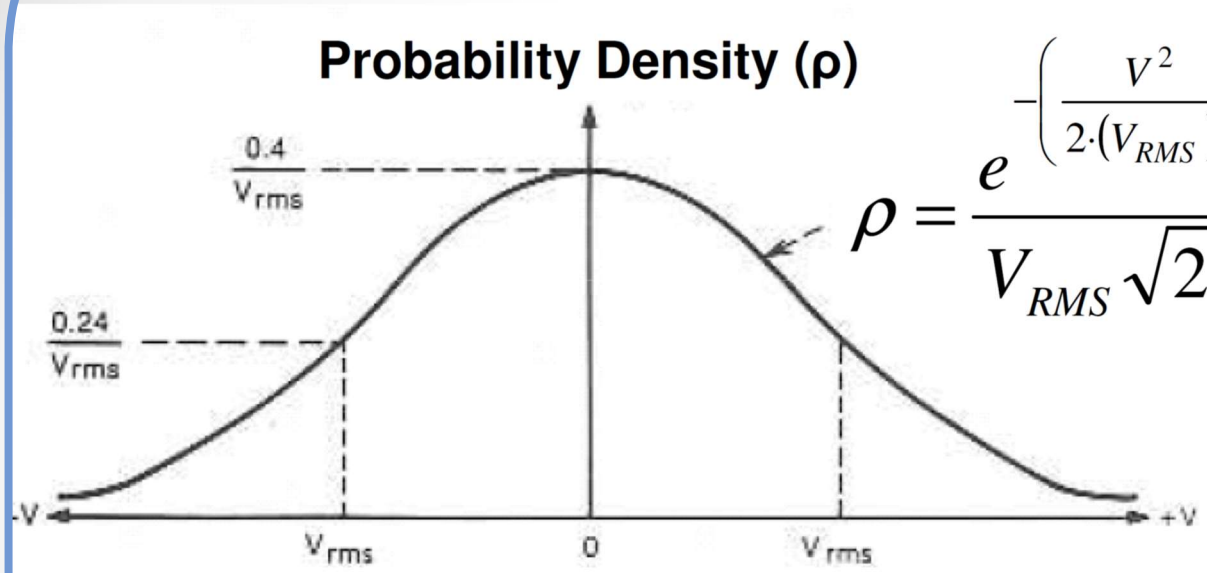
Noise

- is random in amplitude and phase
- possible to predict the “randomness” of noise
  - Mean (often zero)
  - Standard deviation is equal to RMS value of the noise



Noise waveform and Gaussian distribution of noise amplitude

Gaussian Noise Distribution



$$\rho = \frac{e^{-\left(\frac{V^2}{2\cdot(V_{RMS})^2}\right)}}{V_{RMS}\sqrt{2\pi}}$$

$$V_{RMS} = \sqrt{\frac{1}{T}\int_0^T v^2(t)dt}$$

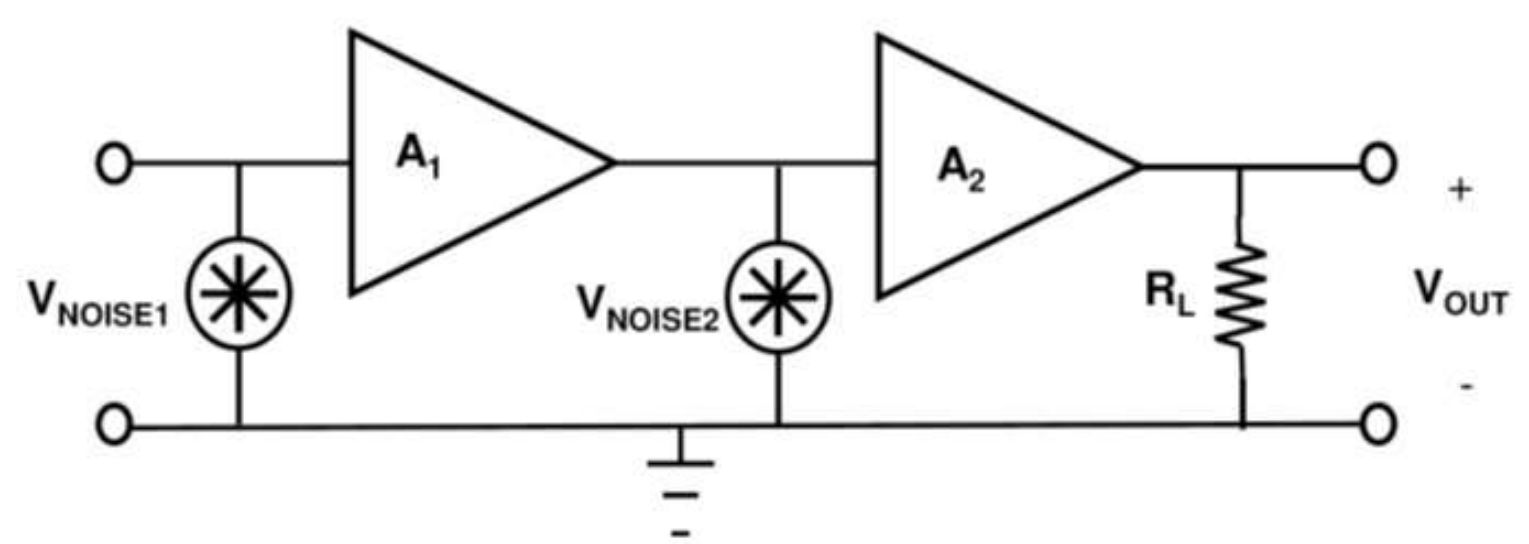
Instantaneous Noise Amplitude

- Recall that V_{RMS} is the same as the standard deviation, σ

Thus, the instantaneous noise amplitude is within +/- 3σ
($3 \times V_{RMS}$) ~ 99.7% of the time

Noise

- Examples mentioned show that problems due to noise are apparent at the output
- Sources of noise unique to low-level circuitry, typically input stage



$$V_{OUT} \cong V_{NOISE1} \cdot A_1 \cdot A_2$$

Assuming A_1 is much greater than 1, V_{NOISE1} dominates and we can ignore the output noise contribution of V_{NOISE2}

Thermal Noise

(aka Johnson noise, Nyquist noise)

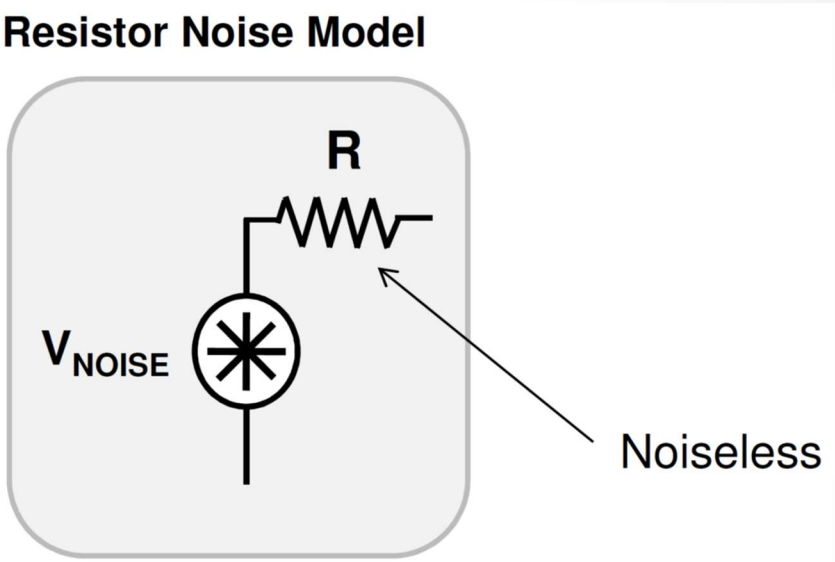
- Due to random motion of electrons in conductor when above absolute zero temp

From Nyquist:

Available Noise Power

$$P_{AVAIL} = kT\Delta f$$

k = 1.38 x10-23 J/K (Boltzmann's constant)
T is temperature in K
Δf is the noise bandwidth $\neq$ 3 dB bandwidth



V_{NOISE} = ?

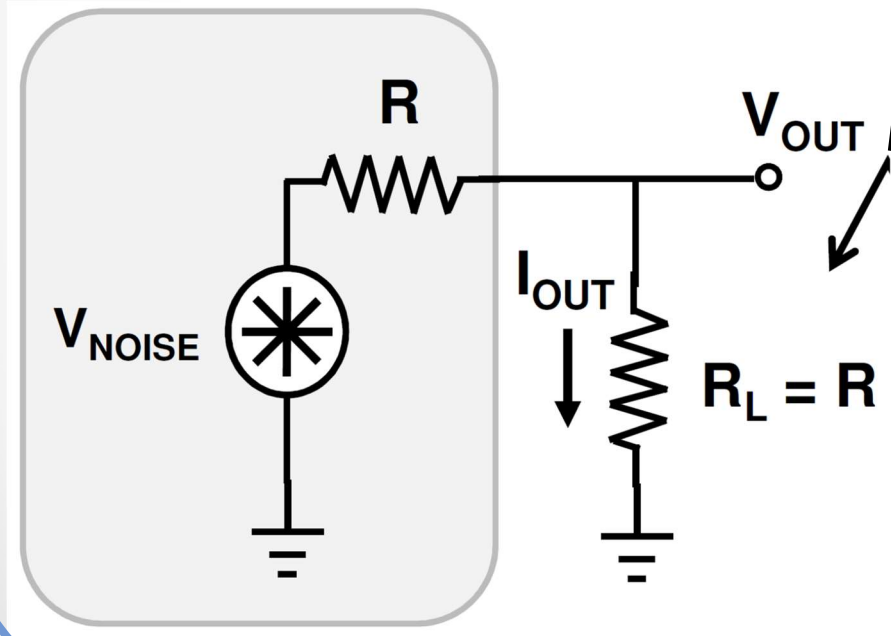
Thermal Noise

(Find V_{NOISE} from Available Noise Power)

Eqn 1.

$$P_{AVAIL} = kT\Delta f$$

Resistor Noise Model



Conjugately match for max power transfer; P_{OUT} under this condition is P_{AVAIL}. Find expression for P_{AVAIL} in terms of V_{NOISE}

$$V_{OUT} = V_{NOISE} \cdot \frac{R_L}{R_L + R} = \frac{V_{NOISE}}{2}$$

$$I_{OUT} = \frac{V_{NOISE}}{R_L + R} = \frac{V_{NOISE}}{2R}$$

$$P_{AVAIL} = P_{OUT} = V_{OUT} I_{OUT} = \frac{V_{NOISE}^2}{4R}$$

Eqn 2.

$$P_{AVAIL} = \frac{V_{NOISE}^2}{4R}$$

Thermal Noise

(Find V_{NOISE} from Available Noise Power)

Eqn 1.

$$P_{AVAIL} = kT\Delta f$$

Eqn 2.

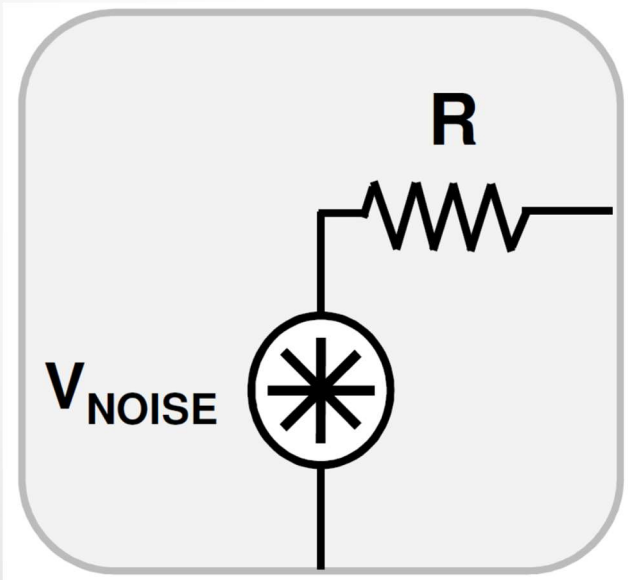
$$P_{AVAIL} = \frac{V_{NOISE}^2}{4R}$$

V_{NOISE} = ?

Set eqn 1 = eqn 2, find V_{NOISE}

$$kT\Delta f = \frac{V_{NOISE}^2}{4R}$$

Resistor Noise Model



$$V_{NOISE} = \sqrt{4kTR\Delta f}$$

Note: thermal noise applies only to true physical resistances, anything that represents energy loss from a system has thermal noise.

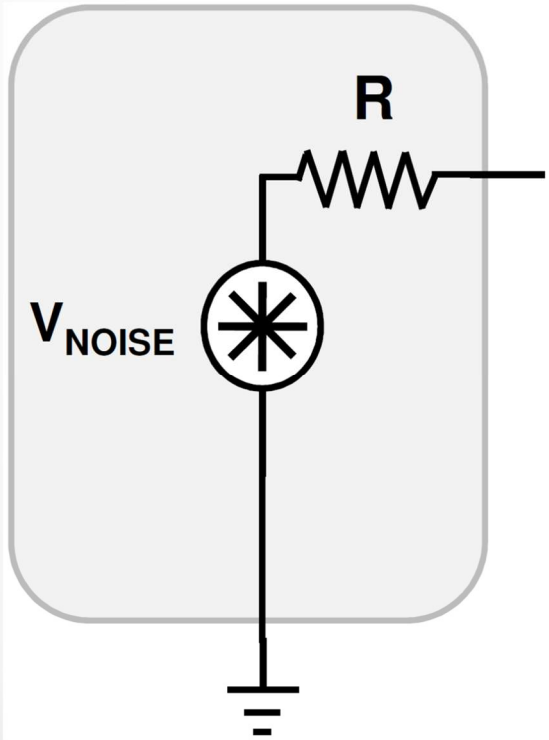
r_{π} from BJT model does NOT contribute thermal noise

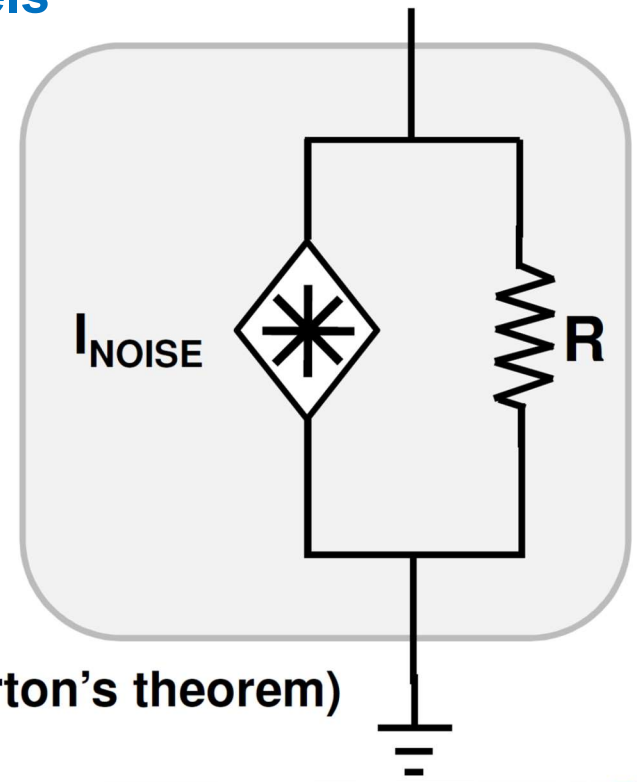
Thermal Noise

$$V_{NOISE} = \sqrt{4kTR\Delta f}$$

$$I_{NOISE} = \sqrt{\frac{4kT\Delta f}{R}}$$

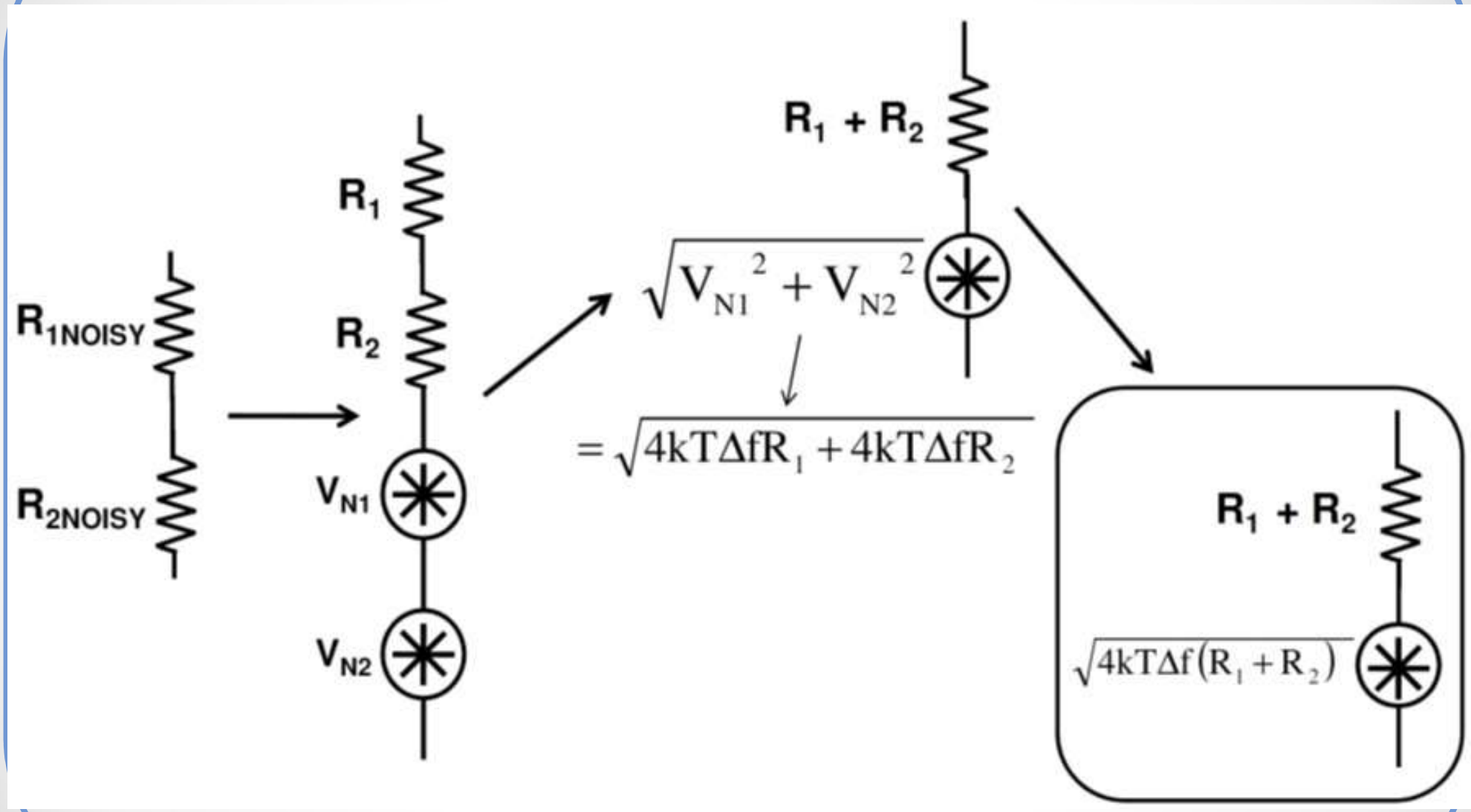
Resistor Noise Models





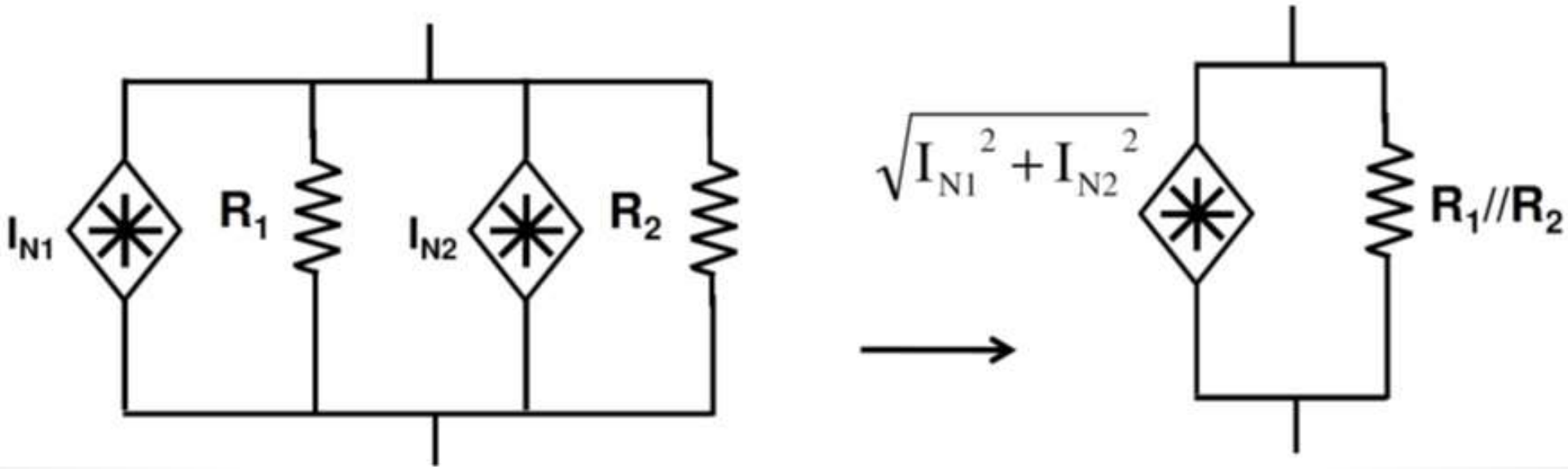
(From Norton's theorem)

Thermal Noise



Thermal Noise

What about R in parallel ?

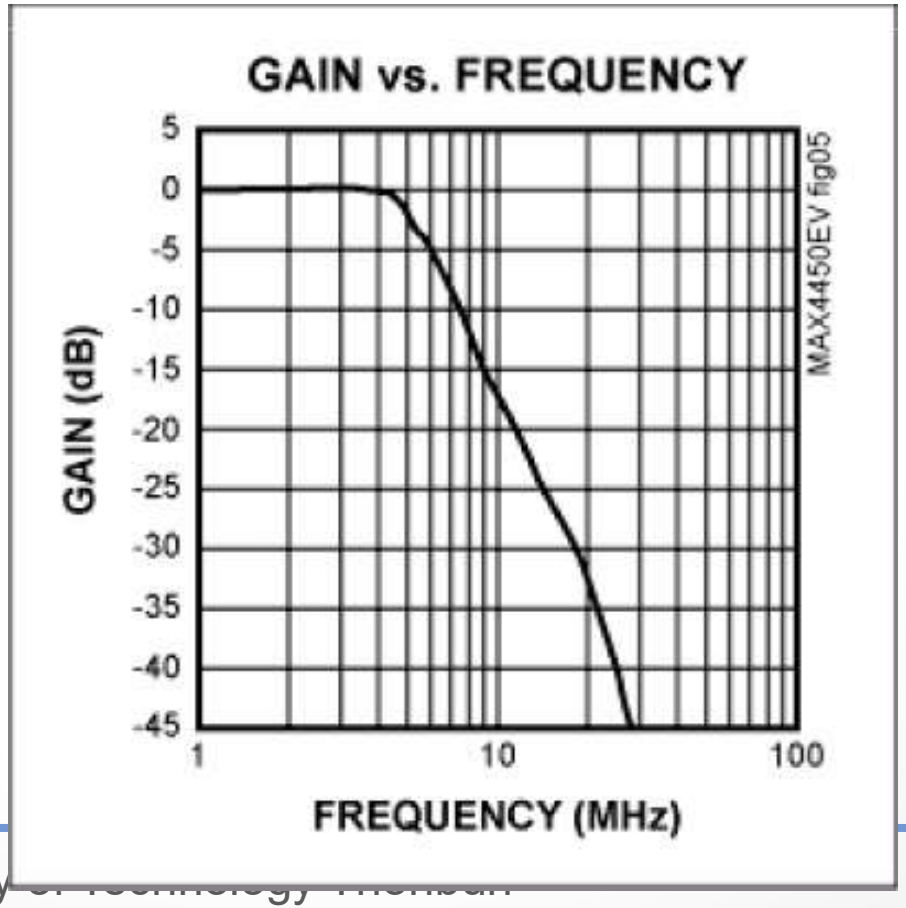


$$\sqrt{I_{N1}^2 + I_{N2}^2} = \sqrt{\frac{4kT\Delta f}{R_1} + \frac{4kT\Delta f}{R_2}} = \sqrt{\frac{4kT\Delta f \cdot R_2}{R_1 \cdot R_2} + \frac{4kT\Delta f \cdot R_1}{R_1 \cdot R_2}}$$

$$\sqrt{I_{N1}^2 + I_{N2}^2} = \sqrt{\frac{4kT\Delta f \cdot (R_1 + R_2)}{R_1 \cdot R_2}} = \sqrt{\frac{4kT\Delta f}{R_1 // R_2}}$$

3 dB Bandwidth

- Typically, the bandwidth of a filter is specified in terms of 3 dB (half-power) bandwidth
  - For a given transfer function, bandwidth spans the frequency range where the magnitude is greater than 3 dB down from maximum gain.
- Can be easily measured by driving the circuit with a sinusoidal source and monitoring output level

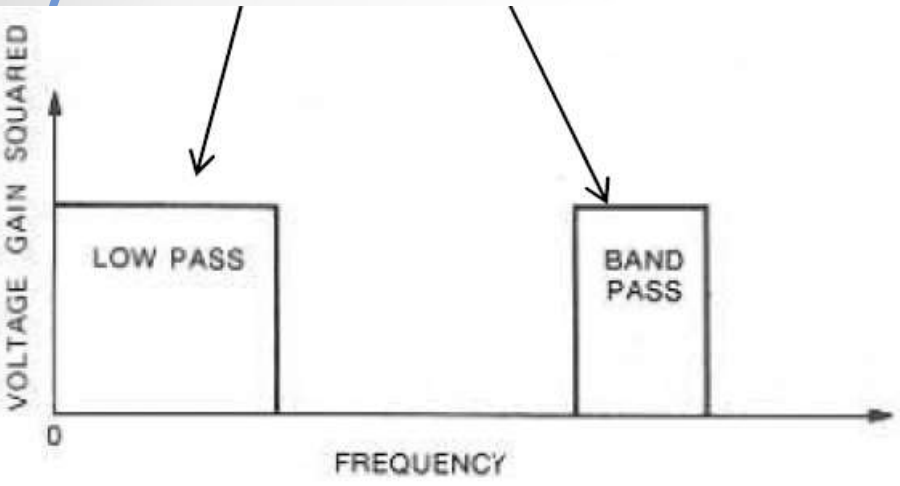


Noise Bandwidth

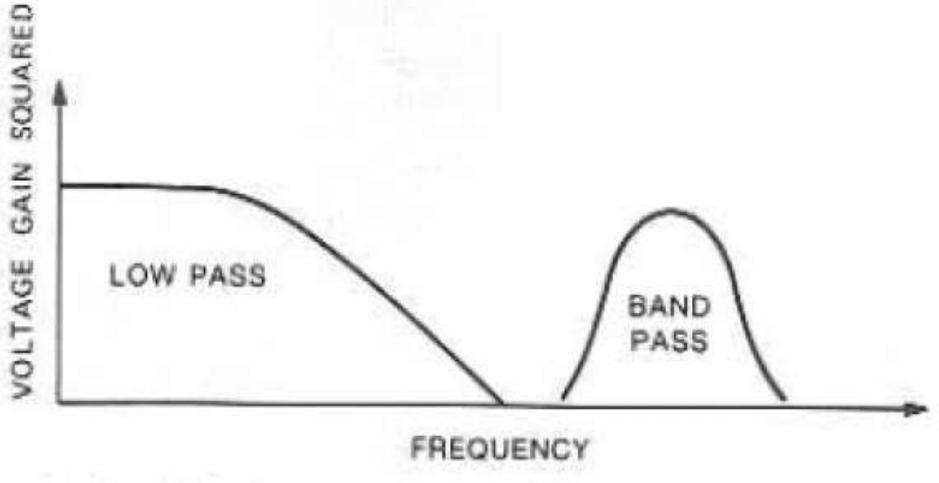
- Not the same as 3 dB (half-power) bandwidth
- Noise bandwidth – defined in terms of the voltage-gain squared (power gain)
  - Defined for a system with uniform gain throughout passband and zero gain outside
  - Shaped like ideal “brick-wall” filter
  - Since real system exhibit practical roll-offs, we need to define bandwidth in a manner consistent with the noise equations

Noise Bandwidth

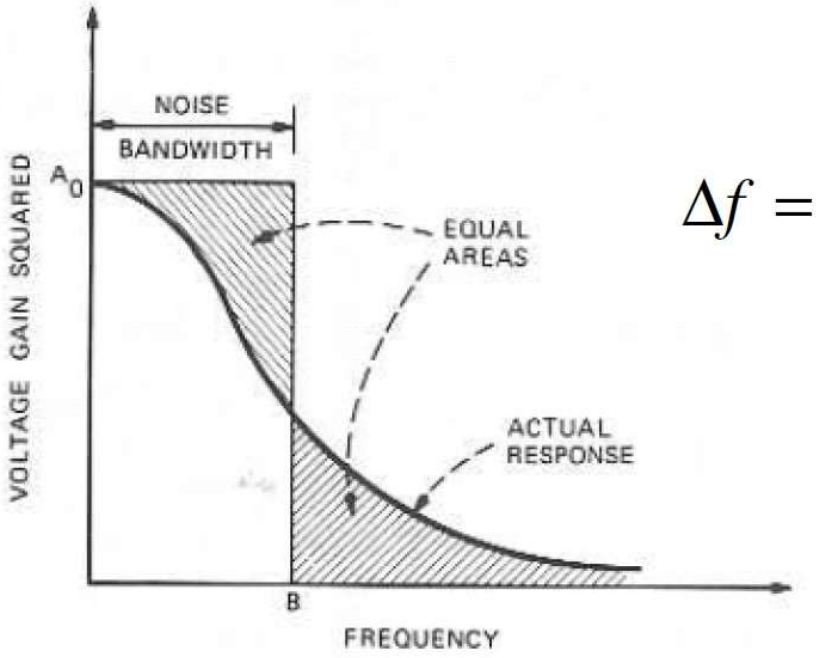
Uniform gain baseband



Ideal bandwidth of low-pass and band-pass circuit elements.



Actual bandwidth of low-pass and band-pass circuit elements.

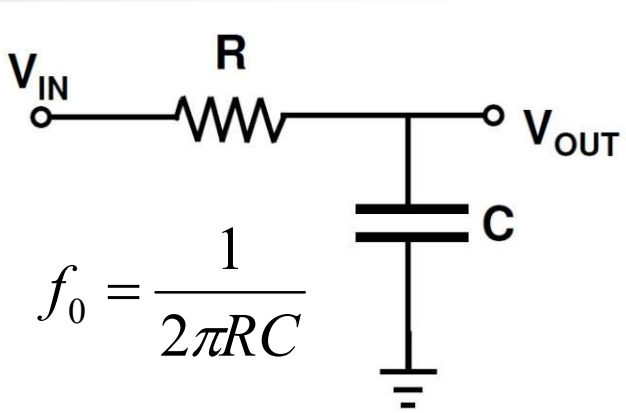


$$\Delta f = B = \frac{1}{|A_0|^2}\int_0^\infty |A(f)|^2\, df$$

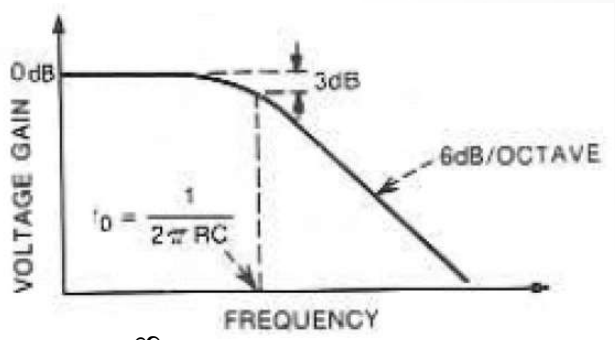
Actual response and equivalent noise bandwidth (low-pass).

Drawn in linear scale

Noise Bandwidth Example



$$f_0 = \frac{1}{2\pi RC}$$



$$|A(f)| = \frac{1}{\sqrt{1+\frac{f^2}{f_0^2}}}$$

$$\Delta f = \frac{1}{|A_0|^2}\int_0^\infty |A(f)|^2 df$$

$$\Delta f = \int_0^\infty \sqrt{1+\frac{f^2}{f_0^2}}\,df = \int_0^\infty \frac{f^2}{f_0^2+f^2}\,df$$

Using trigonometric substitution: let $f = f_0 \tan\theta$ so $df = f_0 \sec^2\theta \cdot d\theta$

$$\Delta f = f_0 \int_0^{\pi/2} d\theta$$

$$\boxed{\Delta f = \frac{\pi}{2} f_0}$$

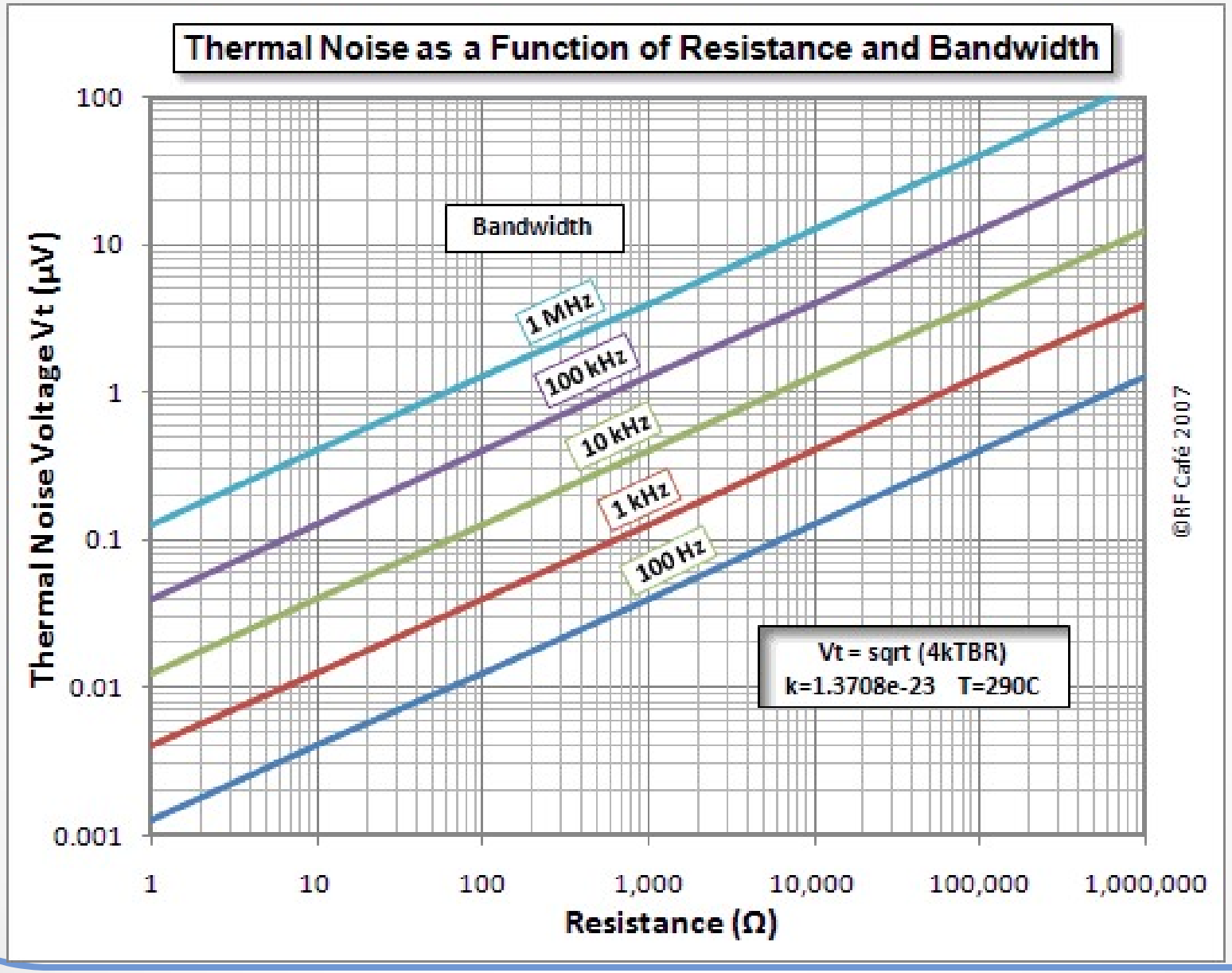
Noise bandwidth is $1.57 \times BW_{3dB}$ for circuits with 1st order roll-off

Relating Noise & 3 dB Bandwidth

- Using circuit roll-off behavior (based on number of poles) can convert 3 dB bandwidth to noise bandwidth
  - Use conversion factor

# of Poles	∆f/BW3dB	High frequency roll-off (dB/decade)
1	1.57	20
2	1.22	40
3	1.15	60
4	1.13	80
5	1.11	100

Thermal Noise vs. R and Δf



Noise Spectral Density

- Noise spectral density is the mean-squared value of the noise per unit bandwidth
  - Can be defined in terms of V or I
  - Noise spectral density of thermal noise is independent of frequency

$$S_v(f) = \frac{v_{noise}^2}{\Delta f} = 4kTR$$

$$S_i(f) = \frac{i_{noise}^2}{\Delta f} = \frac{4kT}{R}$$

Thermal noise is described as "white noise" because the energy is equal across all frequencies, an analogy to white light (equal light energy over all wavelength).

Spot Noise

- Spot noise – RMS value of the noise in a noise bandwidth of 1 Hz
- Unit of Volts/sqrt(Hz) or Amps/sqrt(Hz)

$$\frac{v_{noise}}{\sqrt{\Delta f}} = \sqrt{S_v(f)} = \sqrt{4kTR}$$

$$\frac{i_{noise}}{\sqrt{\Delta f}} = \sqrt{S_i(f)} = \sqrt{\frac{4kT}{R}}$$

Example: Thermal Noise

- What is "spot noise" of 1 kΩ resistor at 300K
- Use this to find V_{NOISE} for 100 kΩ in 1 MHz bandwidth
- 4kT is 1.6×10^{-20} at room temp (290K)

$$\frac{v_{noise}}{\sqrt{\Delta f}} = \sqrt{4kTR} = \sqrt{1.6\times10^{-20}\times1000} = 4.07\text{nV/sqrt(Hz)}$$

$$v_{noise} = \frac{v_{noise}}{\sqrt{\Delta f}}\cdot\sqrt{\Delta f}\cdot\sqrt{\Delta f} = 4\frac{\text{nV}}{\sqrt{\text{Hz}}}\cdot\sqrt{10^6}\cdot\sqrt{100\cdot10^3} = 1.27\text{mV}_{\text{rms}}$$

Noise Floor

- Going back to Nyquist's expression for P_{AVAIL} at room temperature (290K):

$$P_{AVAIL} = kT\Delta f = 4\times10^{-21} \quad \text{(watts)}$$

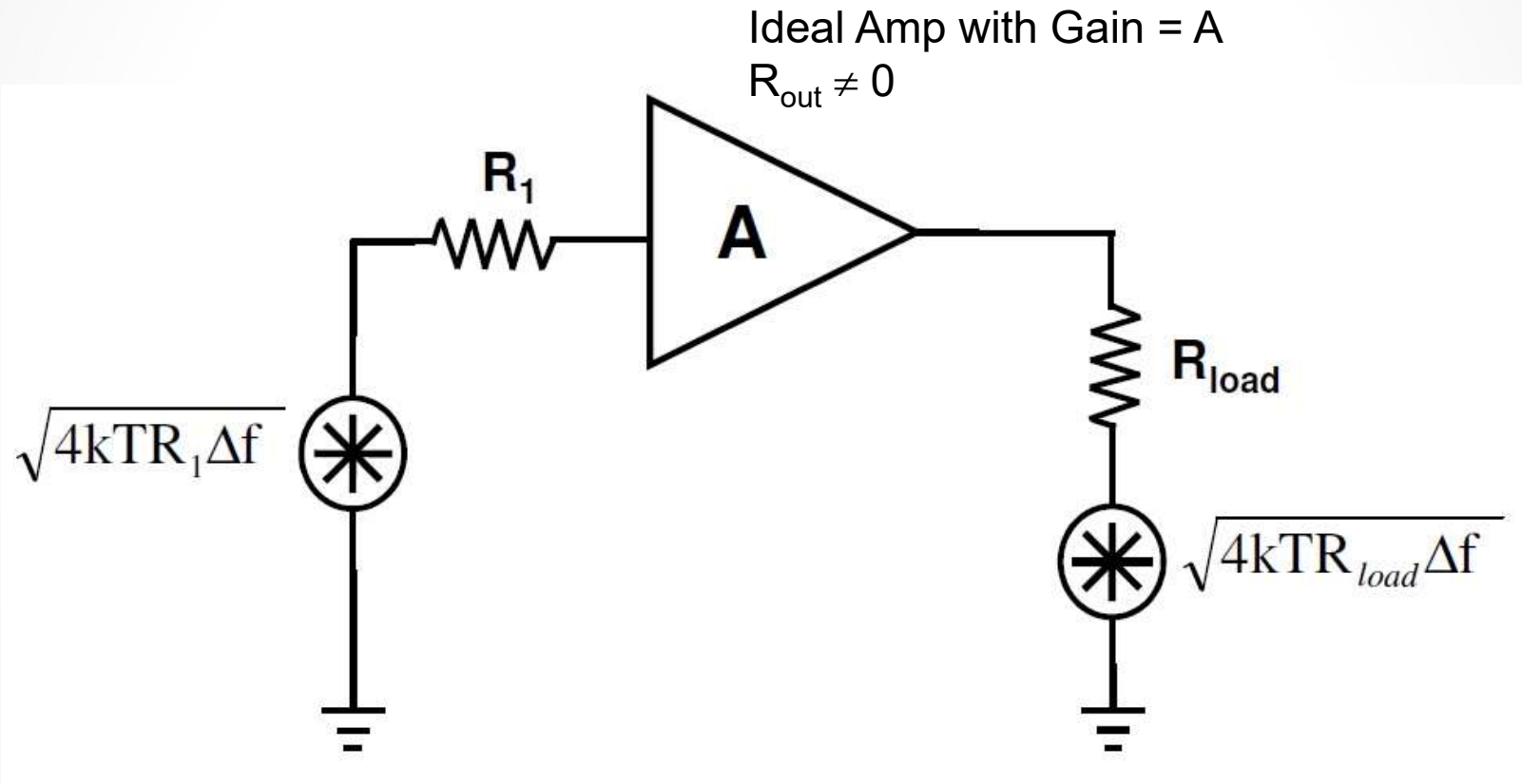
- Put in terms of dBm
- 4kT is $1.6\text{x}10^{-20}$ at room temp (290K)

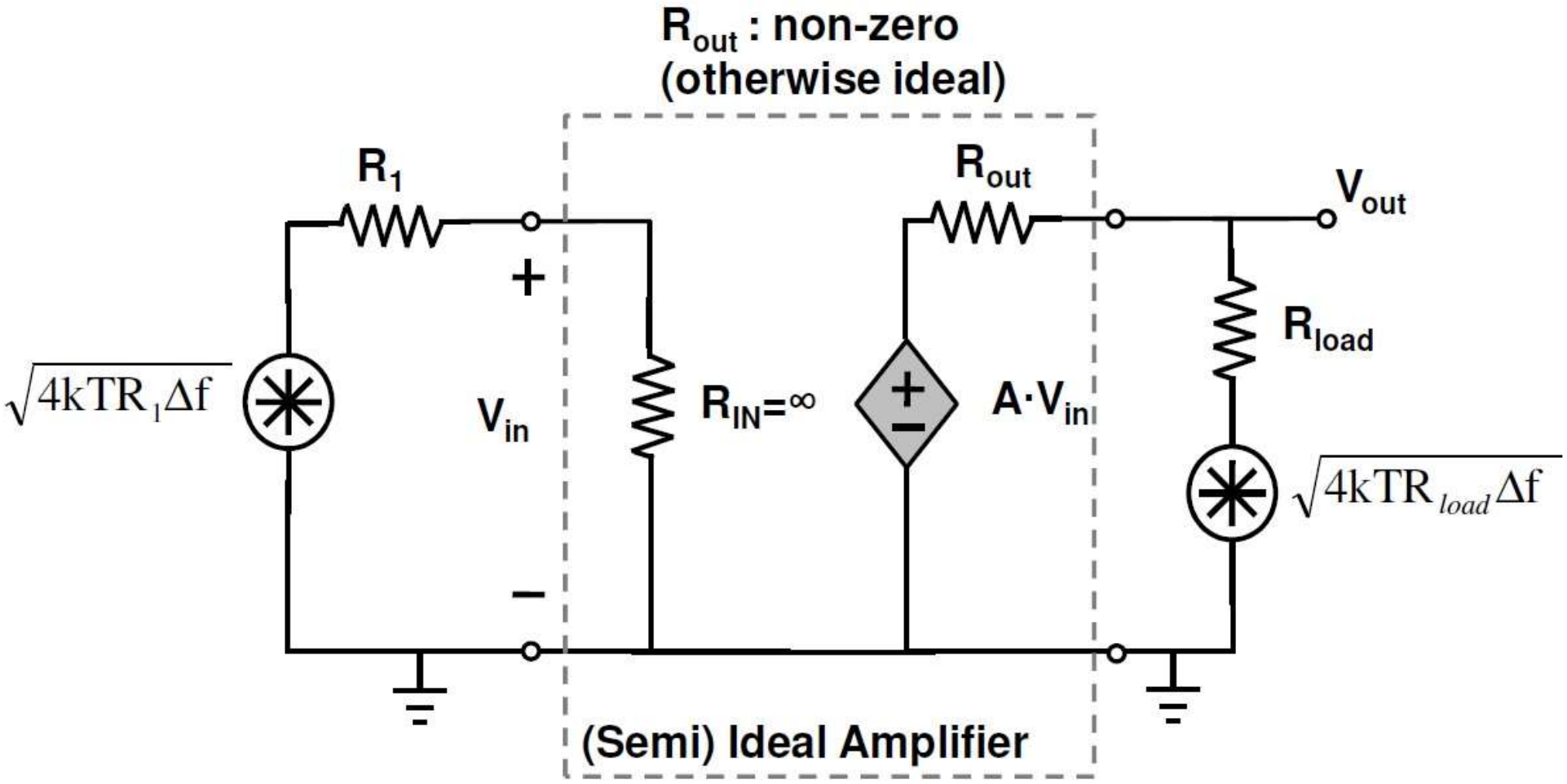
$$10\log\left(\frac{4\times10^{-21}}{10^{-3}}\right) = -174\text{dBm}$$

- Minimum noise level that is practically achievable in a system operating at room temperature.

- Thermal noise represents a minimum level of noise

R_{OUT} and Voltage Noise




R_{out} : non-zero
(otherwise ideal)
R_1
R_{out}
V_{out}
+
R_{load}
$\sqrt{4kTR_1\Delta f}$
V_{in}
$R_{IN}=\infty$
$A \cdot V_{in}$
$\sqrt{4kTR_{load}\Delta f}$
−
(Semi) Ideal Amplifier

Shot Noise

- Present in diodes, transistors
  - First observed in vacuum tubes
- Current flow across a potential barrier
  - DC current is actually the sum of many discrete events when a carrier crosses barrier

$$I_{SHOT} = \sqrt{2qI_{DC}\Delta f}$$

RMS noise current,
also “white”

q is the electronic charge: 1.6×10^{-19} Coulombs
IDC is bias current in Amps
Δf is the noise bandwidth

Avalanche Noise

- Due to Zener or avalanche breakdown in a PN junction
- When breakdown occurs EHPs created
- Results in noise produced that is much greater than that of same current
- Be cautious with zener based voltage references if noise is a concern

1/f Noise (Pink Noise)

- Low-frequency noise, NOT “white”
- AKA flicker noise
- Associated with contamination and crystal defect in all active devices
  - Also present in carbon resistors (consider metal film instead)
- Note inverse dependence on frequency: $$i_d^2 = K \cdot \frac{I_D^a}{f} \cdot \Delta f$$

where id is the drain bias current (this is for long channel MOSFETs)
K is a constant based on the device/technology
a is a constant between 0.5 and 2

1/f Noise

The general characteristic of op amp current or voltage noise is shown in Figure 1 below.

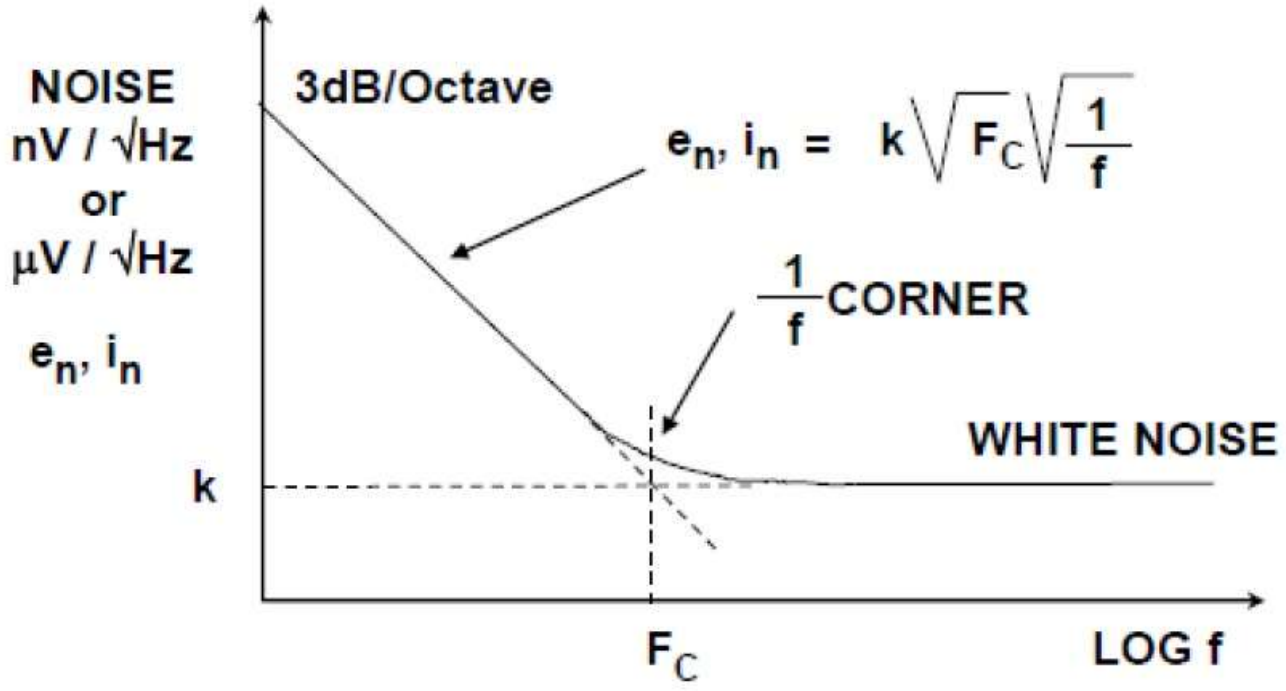
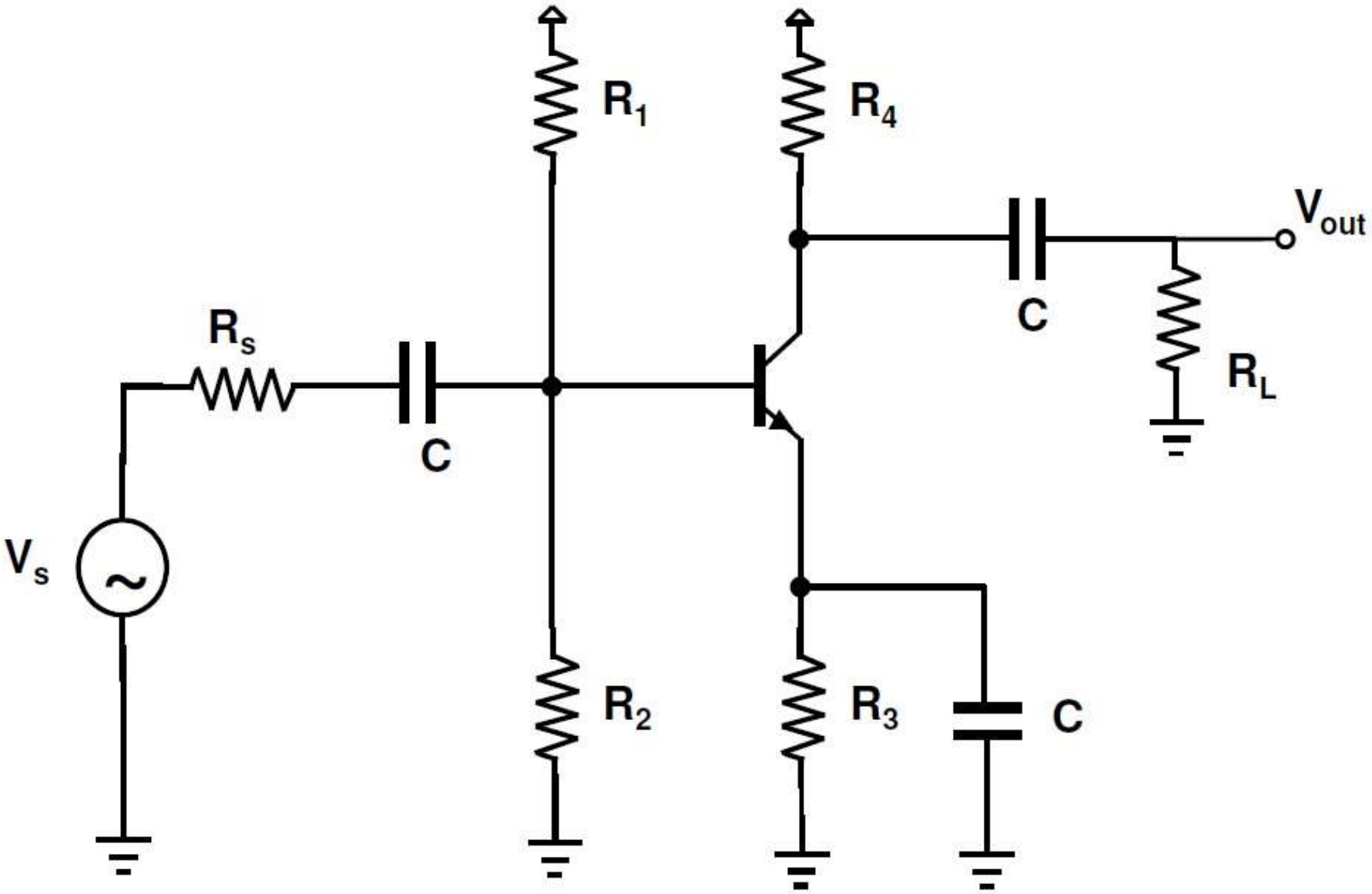


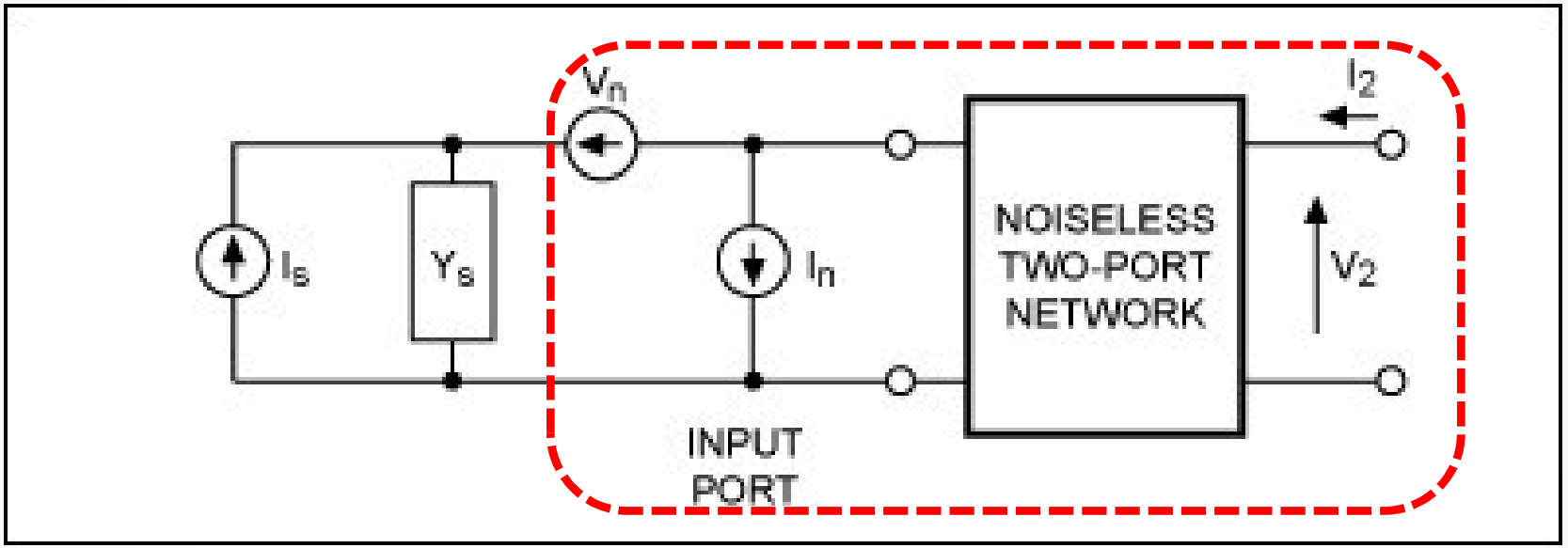
Figure 1: Frequency Characteristic of Op Amp Noise

Example



E.I.N Model

A noisy network can be modeled by addition of an input noise voltage and current source



noisy network

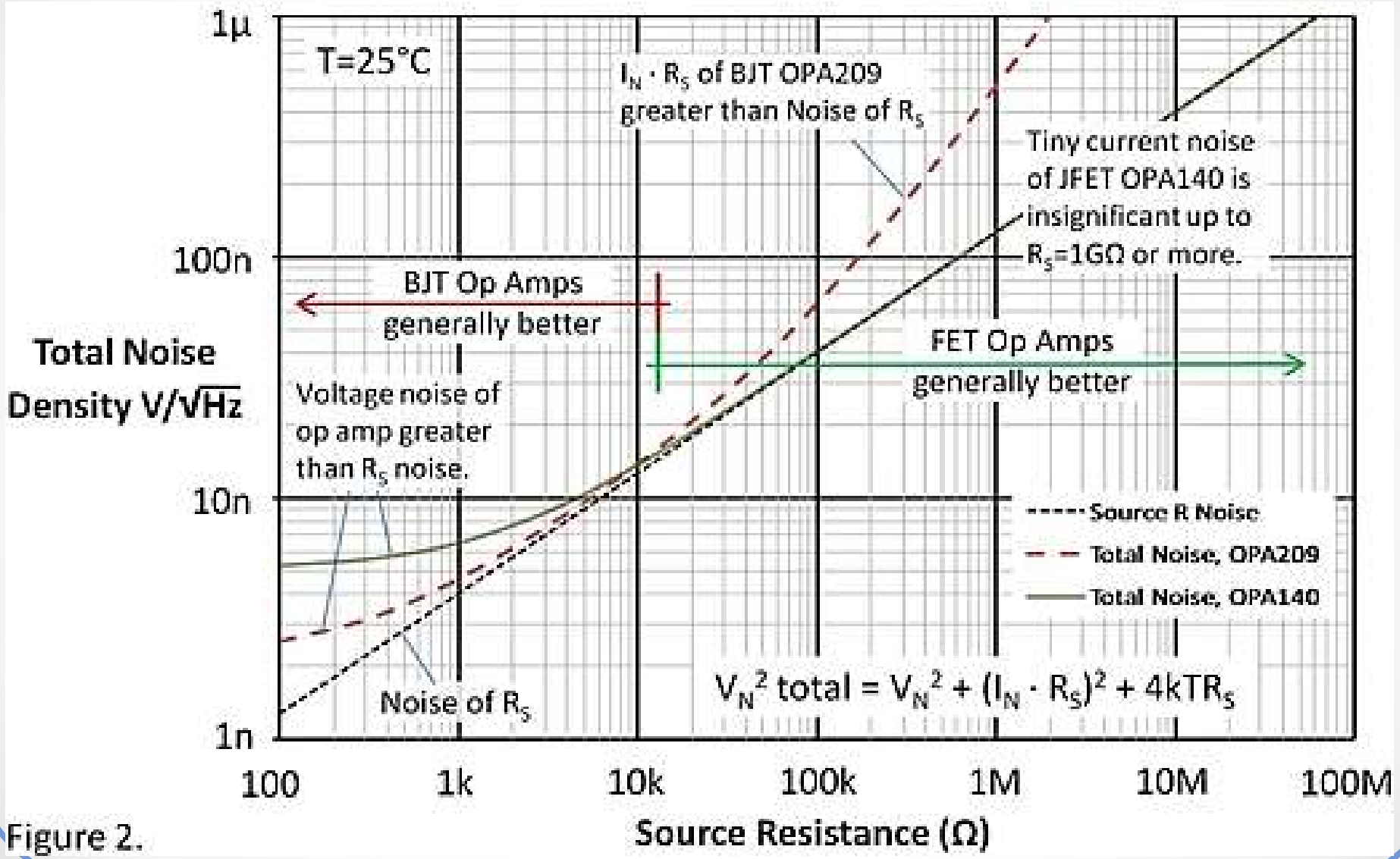

1µ
100n
10n
1n
T=25°C
$I_N \cdot R_S$ of BJT OPA209 greater than Noise of R_S
Tiny current noise of JFET OPA140 is insignificant up to R_S=1GΩ or more.
BJT Op Amps generally better
FET Op Amps generally better
Voltage noise of op amp greater than R_S noise.
Total Noise Density V/√Hz
Source R Noise
Total Noise, OPA209
Total Noise, OPA140
Noise of R_S
V_N^2 total = $V_N^2 + (I_N \cdot R_S)^2 + 4kTR_S$
100
1k
10k
100k
1M
10M
100M
Source Resistance (Ω)

Figure 2.

References

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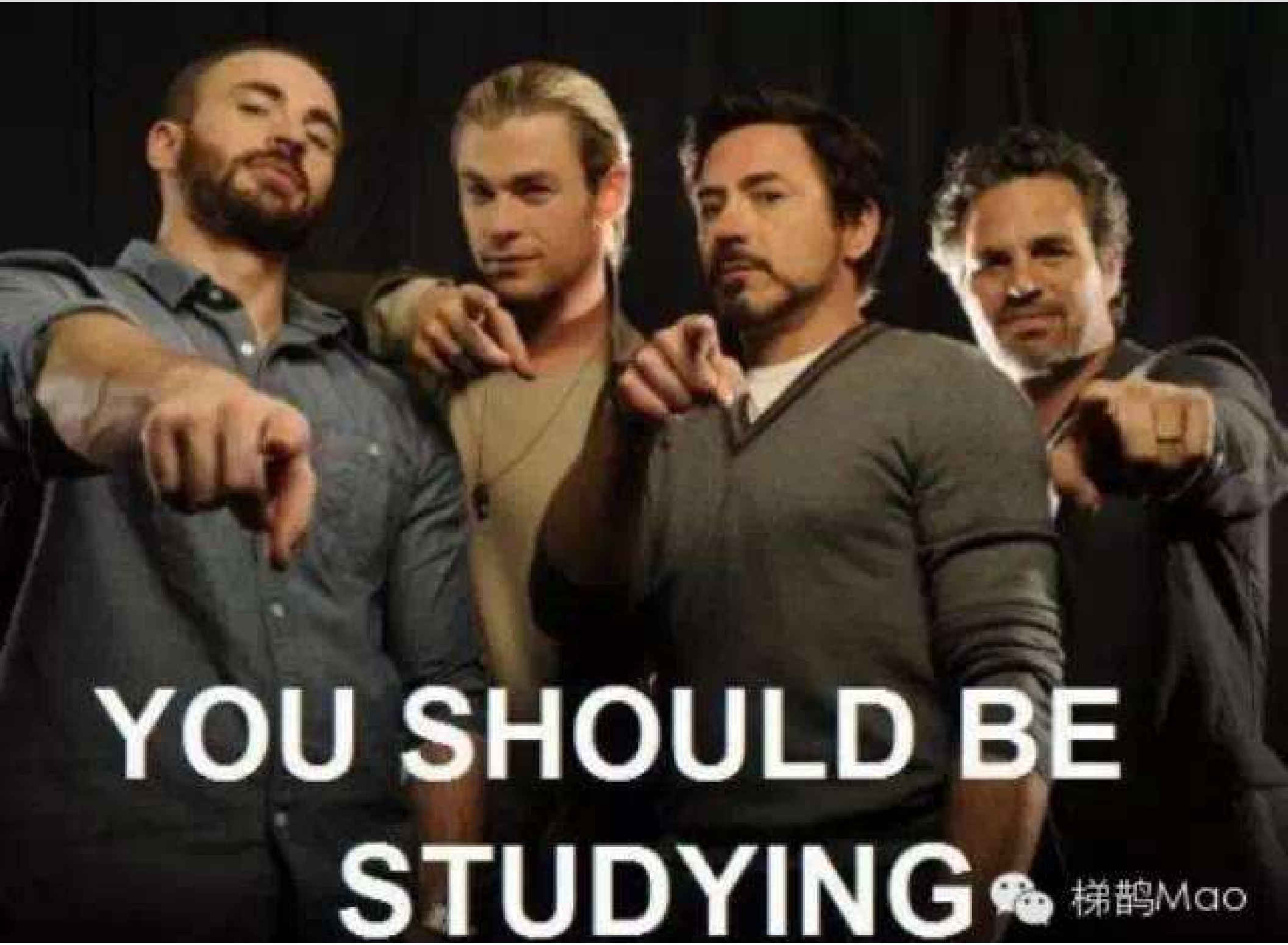
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