Seat No.:_____

King Mongkut's University of Technology Thonburi
Final Exam of Second Semester, Academic Year 2015

CPE 223 Digital System Design **CPE(Inter.) Students**

Tuesday 10 May 2016 **13.00-16.00**

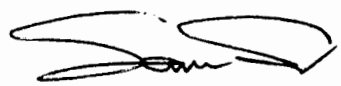
Instructions

1. This examination contains 7 problems, 9 pages (including this cover page), The total score is 40 points.
2. The answers must be written in the space provided.
3. Students are allowed to use **calculator.**
4. **Books**, **notes**, and **dictionary** are **NOT** allowed.

Students must raise their hand to inform to the proctor upon their completion of the examination, to ask for permission to leave the examination room.
Students must not take the examination and the answers out of the examination room.

Students will be punished if they violate any examination rules. The highest punishment is dismissal.

This examination is prepared by



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This examination paper is approved by Computer Engineering Department.

Problem	1	2	3	4	5	6	7	Total Points
Points Earned								
Points	5	5	5	5	5	5	10	40

Student Name: _____ I.D.: _____

1. In Figure 1, a 4-to-1 multiplexer circuit. (5 points)

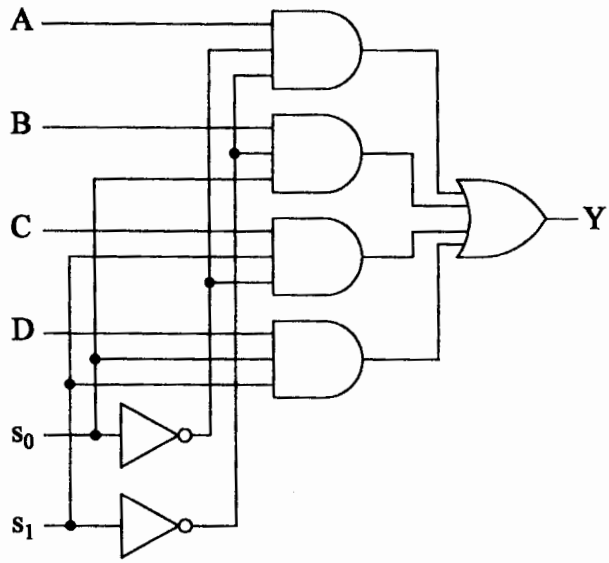

Figure 1: A 4-to-1 multiplexer circuit.

(a) Write a Verilog module using gate-level design(structural Verilog)

(b) Rewrite a Verilog module in (a) using behavioral model.

2. Given a half adder Verilog module

```
module half_adder((x, y, s, c);
input x,y;
output s,c;
        assign s = x ^ y;
        assign c = x & y;
endmodule
```

(5 points)

(a) Write a full adder Verilog module, namely **full_adder**, using half_adder.

(b) Write a 4-bit full adder Verilog module, namely **adder_4bit**, using **full_adder**.

3. Given a dataflow Verilog module below:

```
module fun(E,A,D);
input E;
input [1:0] A;
output [3:0] D;
        assign D[0] = ~(~E & ~A[1] & ~A[0]);
        assign D[1] = ~(~E & ~A[1] & A[0]);
        assign D[2] = ~(~E & A[1] & ~A[0]);
        assign D[3] = ~(~E & A[1] & A[0]);
endmodule
```

Draw a NAND-gate-only circuit to represent the Verilog module above. (5 points)

4. Write a Verilog code using **if... else** statement to implement an 8-bit 2-to-1 multiplexer as shown in Figure 2 below:

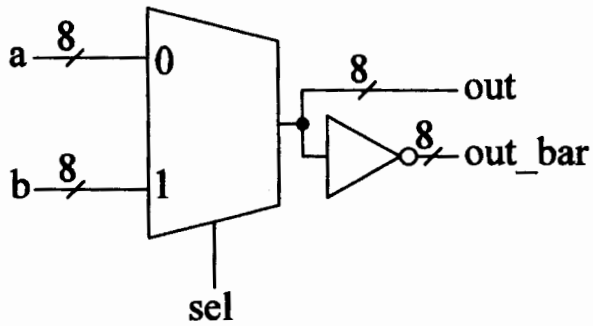

Figure 2: An 8-bit 2-to-1 multiplexer.

(5 points)

5. Given a 4-bit BCD counter circuit using JK flip-flops shown in Figure 3 below:

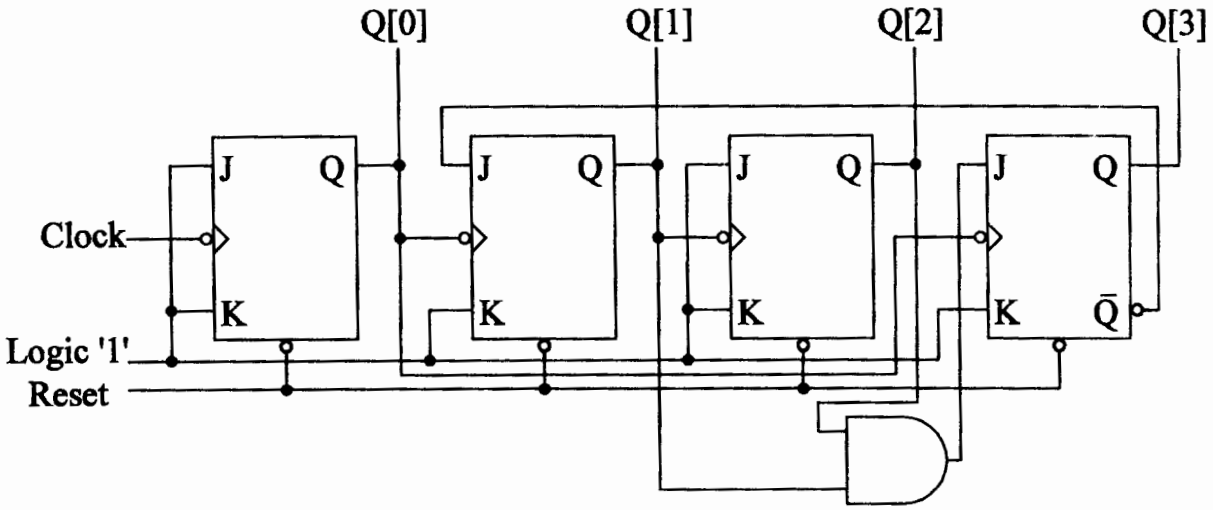

Figure 3: A 4-bit BCD counter using JK flip-flops.

```
module JKFF (input J, K, Clk, Reset, output reg Q);
  always @ (posedge Clk, negedge Reset)
    if (!Reset) Q <= 1'b0;
    else
      case ({J,K})
            2'b00: Q <= Q;
            2'b01: Q <= 1'b0;
            2'b10: Q <= 1'b1;
            2'b11: Q <= ~Q;
      endcase
endmodule
```

(5 points)

(a) Using JKFF module above, write a Verilog module to implement the 4-bit BCD counter of the circuit above.

(b) Rewrite the 4-bit BCD counter Verilog module using behavioral model.

6. From a simple CPU structure given in Figure 4 below:

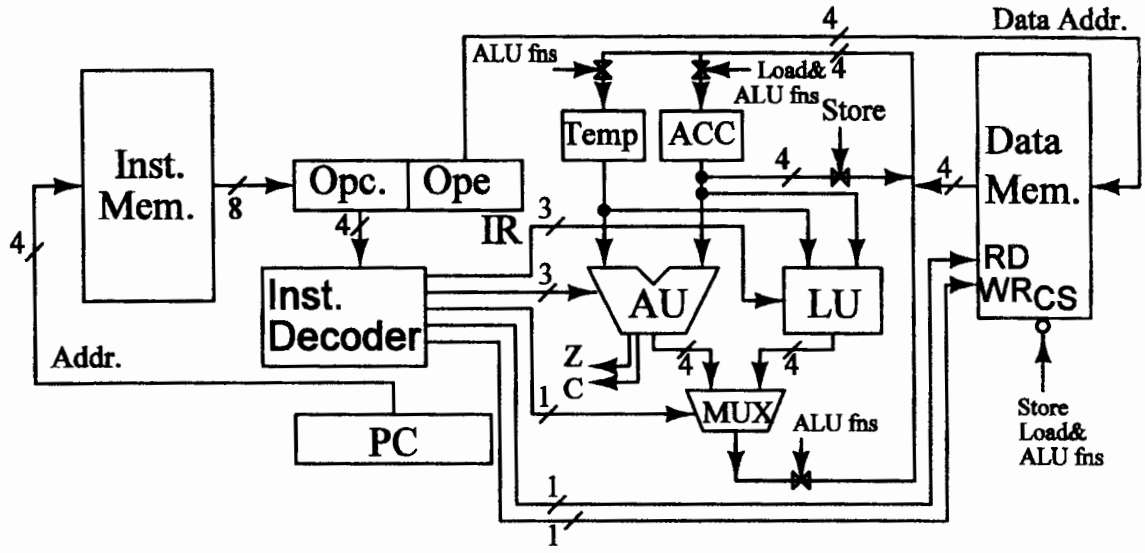

Figure 4. A simple CPU structure.

Write a Verilog code to implement a Data Memory module. (5 points)

7. What is your Final project name? Draw a block diagram of the top module of your Final project. Pick one module in the top module and write a Verilog code for that module. (10 points)