Seat
Number

King Mongkut's University of Technology Thonburi
Midterm Examination
Semester 1 -- Academic Year 2013

Subject: EIE 334 Microprocessors

For: Electrical Communication and Electronic Engineering, 3rd Yr. (Inter. Program)

Exam Date: Thursday September 26, 2013 **Time:** 9.00-12.00 pm.

Instructions:-

1. This exam consists of 4 problems with a total of 9 pages, including the cover.
2. This exam is open books.
3. Answer each problem on the exam itself.
4. A calculator compling with the university rule is allowed.
5. A dictionary is allowed.
6. **Do not** bring any exam papers and answer sheets outside the exam room.

Remarks:-

- **Raise your hand when you finish the exam to ask for a permission to leave the exam room.**
- **Students who fail to follow the exam instruction might eventually result in a failure of the class or may receive the highest punishment with university rules.**
- **Carefully read the entire exam before you start to solve problems. Before jumping into the mathematics, think about what the question is asking. Investing a few minutes of thought may allow you to avoid twenty minutes of needless calculation!**

Exam No.	1	2	3	4	TOTAL
Full Score	44	12	21	28	102
Graded Score					

Name ________________________________ **Student ID** ________________

Mr. Dejwoot Khawparisuth (tel: 9065,9070)
An examiner

A. Wudhichai

(Assoc. Prof. Wudhichai Assawinchaichote, Ph.D.)
Head of Electronic and Telecommunication Engineering Department

ชื่อ-สกุล ______________________________ รหัส__________ เลขที่นั่งสอบ_________

1.] Please answer the following questions and show your work in details.

1.1.) Consider two different processors P1 and P2 executing the same instruction set. There are three class of instructions. P1 has a clock rate of 90 MHz and P2 has a clock rate of 95 MHz. The average number of cycles for each instruction class and their frequencies of use (for a typical program) are given in the following table

Instruction Class	P1: Cycles/instruction class	P2: Cycles/instruction class	frequency
A	1	2	50%
B	4	3	30%
C	5	4	20%

1.1.1. Calculate the average CPI for each processor, P1 and P2. **(4 points)**

1.1.2. Calculate the average MIPS rating for each processor, P1 and P2. **(4 points)**

1.1.3. Which processor has a better performance? **(4 points)**

ชื่อ-สกุล ____ รหัส______________ เลขที่นั่งสอบ__________

1.2.) For the C statements below, what is the corresponding MIPS assembly code? Assume that the variable f, g, h and i are assigned to registers \$s0, \$s1, \$s2 and \$s3 respectively. Assume that the base address of the arrays A and B are in registers \$s6 and \$s7 respectively

1.2.1. C statement: f = g – h – A[5] **(6 points)**

1.2.2. C statement: f = g + B[A[3] – i] **(6 points)**

1.3.) For the binary entries below, what MIPS instruction do they represent?

1.3.1. Binary: 0000 0000 0001 1001 1000 0010 1000 0000 **(3 points)**

1.3.2. Binary: 0010 1010 1111 1000 1000 0000 0000 0001 **(3 points)**

ชื่อ-สกุล ______________________________ รหัส__________ เลขที่นั่งสอบ_________

1.4.) For the sequence of MIPS instructions below, show the hexadecimal representation. (MIPS machine code)

1.4.1. or $s7, $t7, $zero **(3 points)**

1.4.2. beq $s1, $a1, 40 **(3 points)**

1.5.) For the pseudoinstructions below, produce a minimal sequence of actual MIPS instructions to accomplish the same things. You may need to use **`$at`** for some of the sequences. Note: '**`big`**' refers to a specific number that requires 32 bits to represent and '**`small`**' requires 16 bits.

1.5.1. `addi $t0, $t2, big` # $t0 = $t2 + big **(4 points)**

1.5.2. `seq $t1, $t2, $t3` **(4 points)**

Set register rdest to 1 if register rsrc1 is equal to rsrc2, and to 0 otherwise.

ชื่อ-สกุล ______________________________ รหัส__________ เลขที่นั่งสอบ________

2.] Please answer the following questions and show your work in details.

2.1.) Encode the following number into their single precision floating point:

2.1.1. $-16.359375_{decimal}$ **(3 points)**

2.1.2. $3A1.4F_{hex}$ **(3 points)**

2.2.) Decode the following 64-bit floating point into their decimal value:

2.2.1. 0xFFE9 0000 0000 0000 **(3 points)**

2.2.2. 0x7FF2 437A 1B86 CDF8 **(3 points)**

ชื่อ-สกุล ______________________________ รหัส __________ เลขที่นั่งสอบ _________

3.] Complete the following tables

3.1.) Fill the values (in base 16 only) of any registers that effected by the following sequence. Note: initially \$t0 = -1_{ten}, \$t1 = -2_{ten}, \$t2 = 0x5781A, \$t3 = 0x80

(6 points)

Label	mnemonic	\$s0	\$s1	\$s2	\$s3	\$s4
start:	**subu \$s0,\$t0,\$t1**					
	sll \$s1,\$t3,4					
	andi \$s2,\$t2,0x0FF00					
	slt \$s3,\$t0,\$t1					
	or \$s4,\$s2,\$s3					
	srl \$s0,\$t1,28					

ชื่อ-สกุล ____ รหัส____________ เลขที่นั่งสอบ__________

3.2.) Use Division algorithm II (Optimized Divider) to find the Quotient and the Remainder of the 8-bit dividend = 177 and the 8-bit divisor = 18. (15 points)

Iteration	Step (Division: Algorithm II)	Divisor	Remainder
X	Initial Values	xxxx xxxx	xxxx xxxx xxxx xxxx
X	Initial Values		
0			

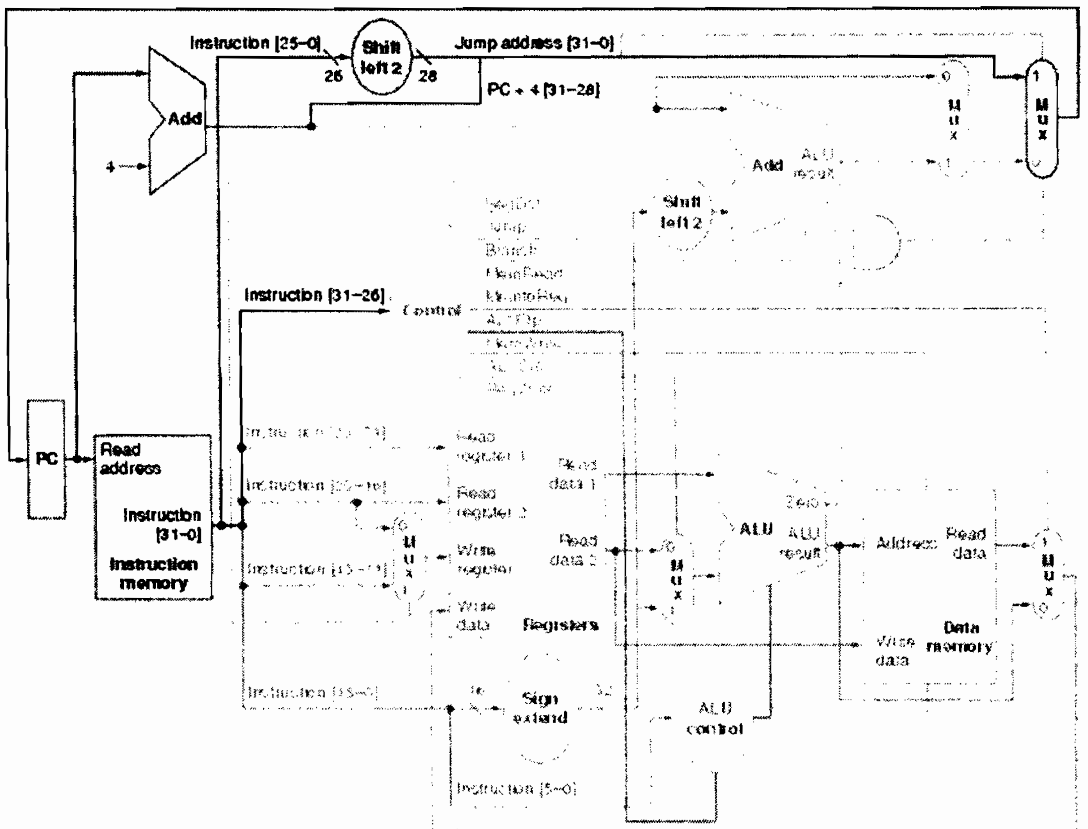
Quotient = ________ten

Remainder = ________ten

ชื่อ-สกุล ______________________________ รหัส__________ เลขที่นั่งสอบ_________

4.] Answer the following question in brief but accurate.

4.1.) From Datapath in figure 4.24 on page 329 (4^{th} ed.), (if you can't clearly see the figure, look at the book or lecture note)



4.1.1. Which is/are the instruction(s) that cause **RegDst** signal to reset to '1'?

(3 points)

4.1.2. Which is/are the instruction(s) that cause **RegDst** signal to reset to '1'?

(3 points)

4.1.3. How many bits are there for the **ALU** control output signal?

(3 points)

4.1.4. Can we use this Datapath for the 'jr' instruction? Why/why not?

(4 points)

ชื่อ-สกุล ______________________________________ รหัส__________ เลขที่นั่งสอบ_________

4.2.) With the following sequences of instructions, and assume that it is executed on a five-stage pipelined Datapath:

```
and $8, $9, $10
lw $9, 4($8)
lw $10, 8($8)
sub $9, $9, $8
sw $8, 8($10)
add $11,$8,$9
```

4.2.1. If there is no forwarding or hazard detection, insert '**nop**'s to ensure correct execution. **(8 points)**

4.2.2. If the processor has forwarding, but we forget to implement the hazard detection unit, what happen when this sequence executes? **(4 points)**