Seat Number

King Mongkut's University of Technology Thonburi
Final Examination
Semester 1 -- Academic Year 2015

Subject: EIE 210 Electronic Devices and Circuit Design I
For: Electrical Communication and Electronic Engineering, 2nd Yr (Inter. Program)
Exam Date: Friday November 27, 2015 **Time:** 13.00-16.00 pm.

Instructions:-

1. This exam consists of 5 problems with a total of 9 pages, including the cover.
2. This exam is closed books.
3. You are **not** allowed to use any written A4 note for this exam.
4. Answer each problem on the exam itself.
5. A calculator compiling with the university rule is allowed.
6. A dictionary is **not** allowed.
7. **Do not** bring any exam papers and answer sheets outside the exam room.
8. Open Minds … No Cheating! GOOD LUCK!!!

Remarks:-

- **Raise your hand when you finish the exam to ask for a permission to leave the exam room.**
- **Students who fail to follow the exam instruction might eventually result in a failure of the class or may receive the highest punishment with university rules.**
- **Carefully read the entire exam before you start to solve problems. Before jumping into the mathematics, think about what the question is asking. Investing a few minutes of thought may allow you to avoid twenty minutes of needless calculation!**

Exam No.	1	2	3	4	5	6	7	8	TOTAL
Full Score	10	10	20	20	20				80
Graded Score									

Name _____ **Student ID** _____

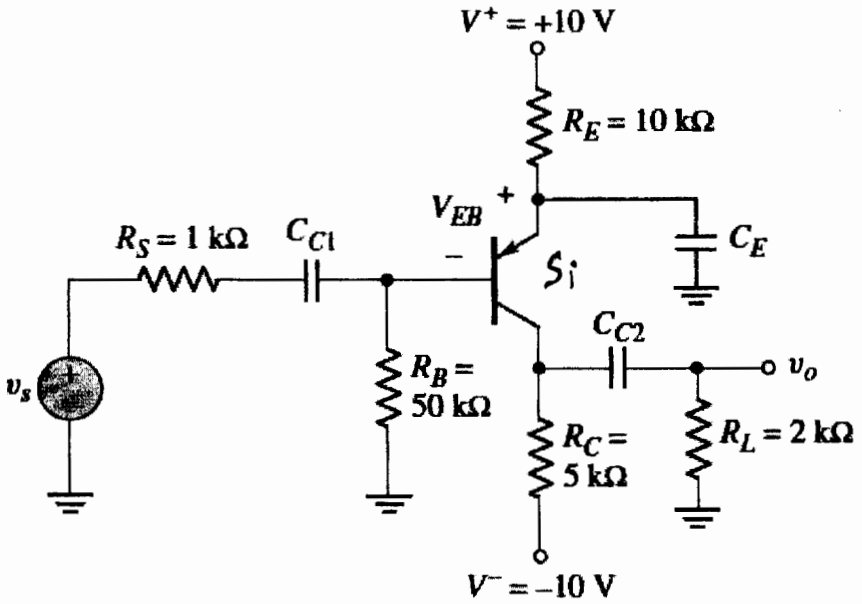
This examination is designed by
Asst. Prof. Kamon Jirasereeamornkul. Ph.D, & Prof. Peter Zeller. Ph.D.; Tel: 9067.

This examination has been approved by the committees of the ENE department.

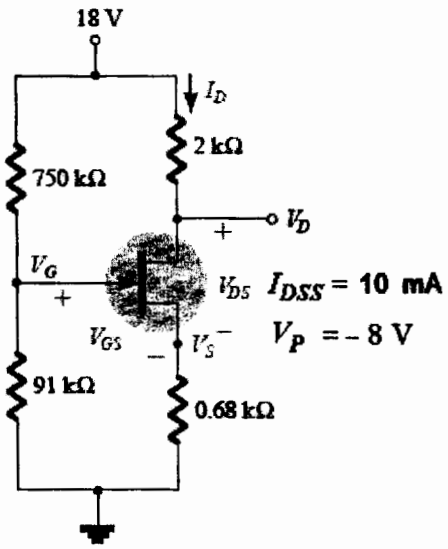
(Assoc. Prof. Rardchawadee Silapunt, Ph.D.)
Head of Electronic and Telecommunication Engineering Department

Part I:

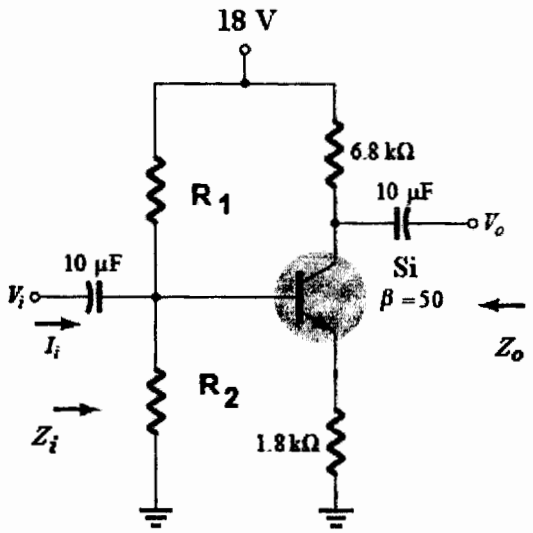
1. From the Fixed bias circuit, determine I_{BQ}, I_{CQ} and V_{CEQ}. (10 marks)



2. Consider the following circuit, determine V_{DQ} and I_{DQ}. (10 marks)

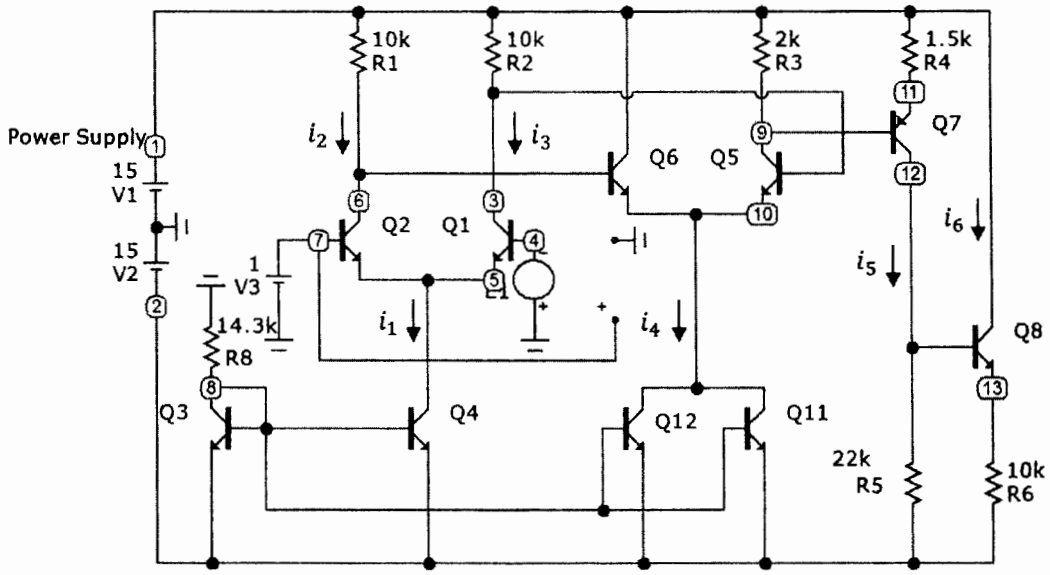


3. From the following amplifier circuit, determine R_1 and R_2 that give $V_{CEQ} = 8$ V and $Z_i = 10$ kOhm. Also, find the A_V by using r_e model. (20 marks)



Part II:

4. Given multiple amplifier stage: (β = 100, silicon transistors) (20 marks)



4.1 Name the type and explain the function of the transistors stages

Q1 / Q2:

Q3 / Q4

Q11 / Q12

Q6 / Q5

Q7

Q8

4.2 Calculate the potentials

3:

Formula:

Value:

6:
Formula:

Value:

8:
Formula:

Value:

9:
Formula:

Value:

11:
Formula:

Value:

12:
Formula:

Value:

13:
Formula:

Value:

4.3 Calculate the currents:
i_1:
Formula:

Value:

i_2:
Formula:

Value:

i_3:
Formula:

Value:

i_4:
Formula:

Value:

i_5:
Formula:

Value:

4.4 What will be the effect onto the potential 13 if resistor R8 is increased? Will potential 13 increase or decrease?

5. What type of current mirror circuits do you know? (20 marks)
5.1 Type 1:
Name:

Circuit and short description of the function:

5.2 Type 2:
Name:

Circuit and short description of the function:

5.3 Type 3:
Name:

Circuit and short description of the function:

5.4 Prove, that the collector current of the first transistor is mirrored to the other transistor by applying the following equation (for a circuit of your choice):

$$V_{BE} = V_T \ln\left(\frac{I_C}{I_S}\right)$$

5.5 Derive for one of the circuits the influence of the forward current ratio β onto the value of the mirrored current.

5.6 Why the transistor pairs should be coupled thermally perfect?

5.7 Should the desired output resistance of a constant current source high or low and why?