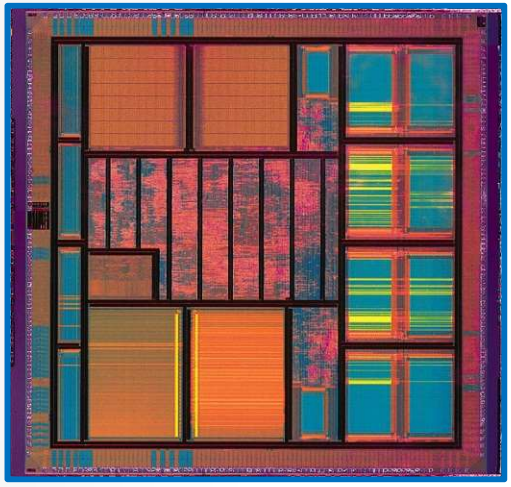
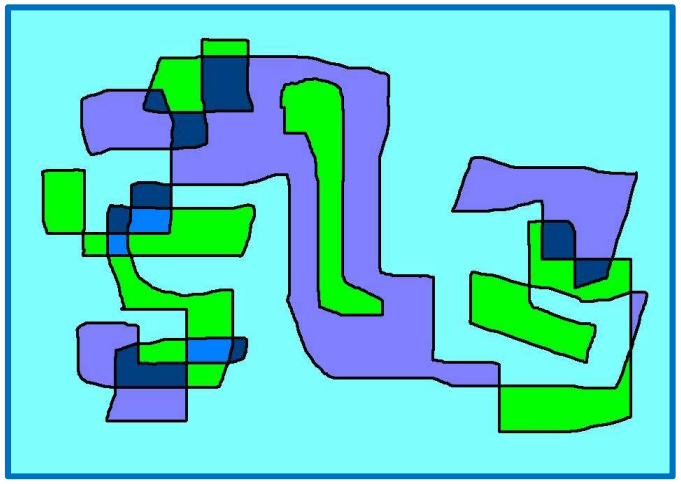
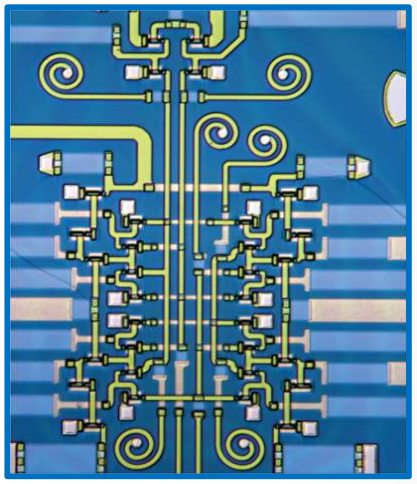
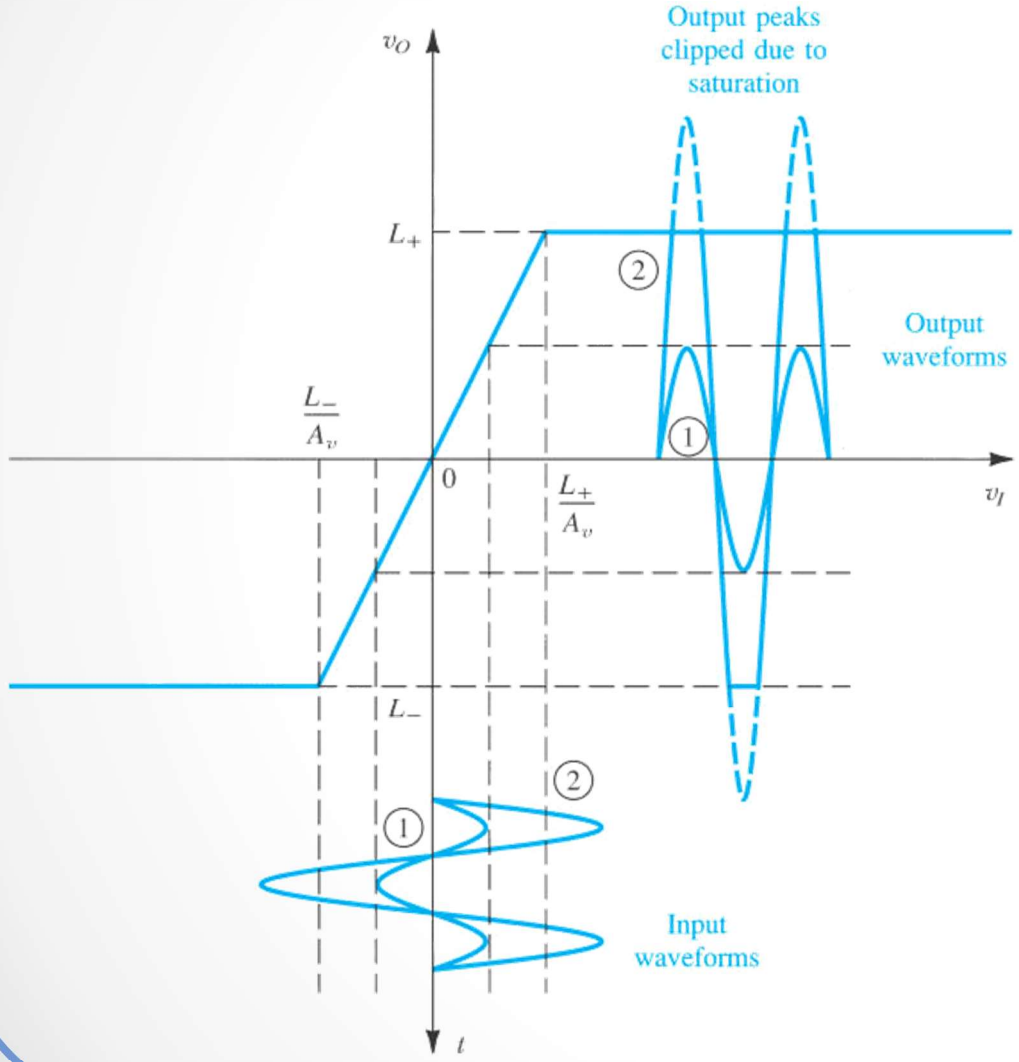




ENE/EIE 211 : Electronic Devices and Circuit Design II

Lecture 3

Large-signal operation of op amps

1. Output voltage saturation:



The op amp output saturates within 1 V of the positive and negative power supplies. Op amp that is operating from +/- 15 V supplies will saturate when the output voltage reaches about +/- 13 V.

2. Output current limit: the output current is limited to a specified max.

For example, the popular 741 op amp is specified to have max output current of +/- 20 mA.

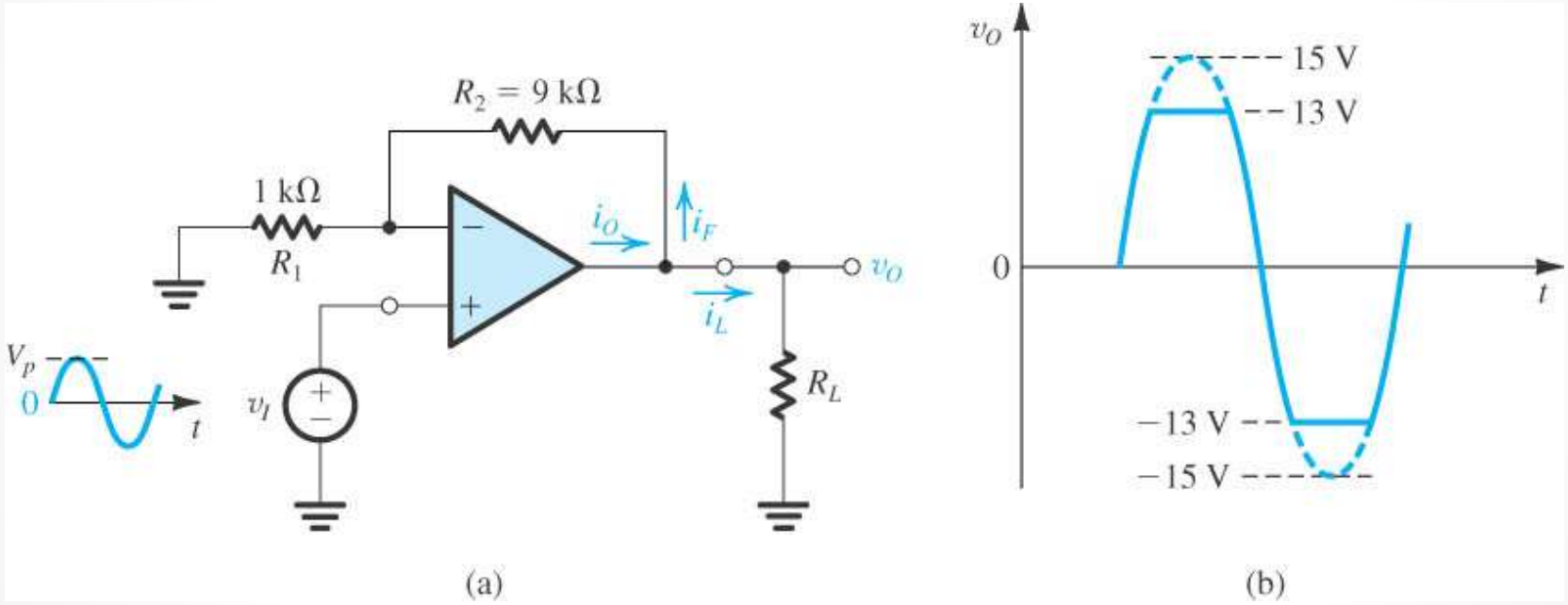
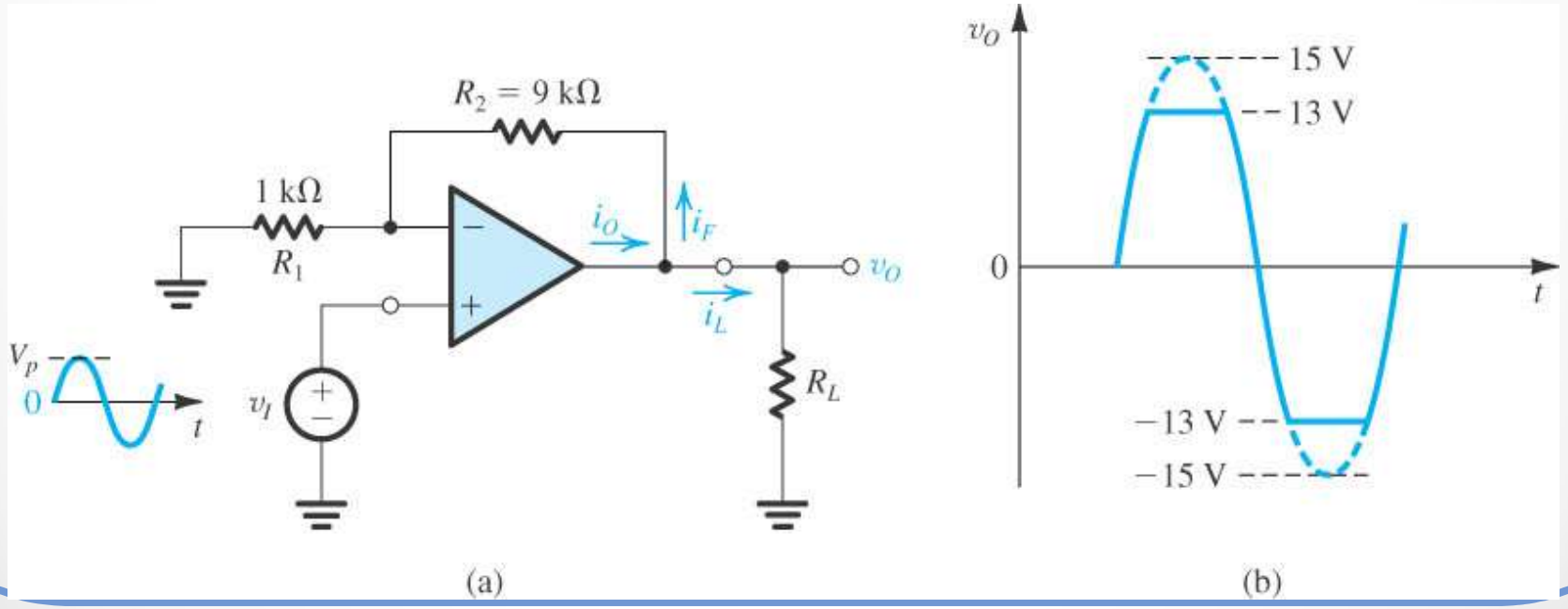


Figure (a) A noninverting amplifier with a nominal gain of 10 V/V designed using an op amp that saturates at ±13-V output voltage and has ±20-mA output current limits. **(b)** When the input sine wave has a peak of 1.5 V, the output is clipped off at ±13 V.

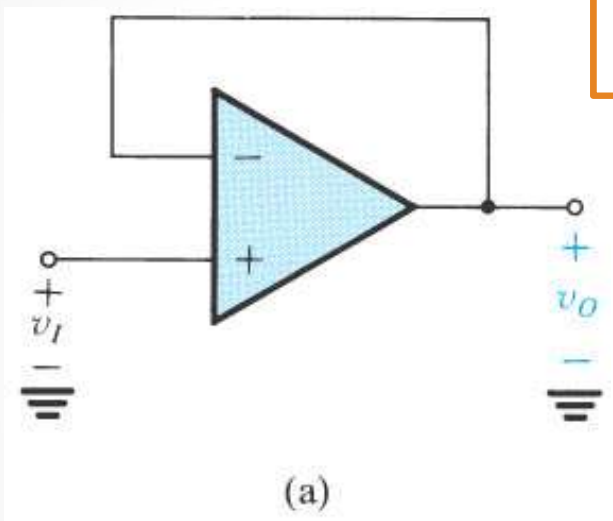
Example: consider the noninverting amp ckt as shown. The ckt is designed for A nominal gain (1 + R2/R1) = 10 V/V. It is fed with a low-freq sine-wave signal Of peak voltage Vp and is connected to a load resistor R_L. The op amp is Specified to have output sat. voltages of +/- 13 V and output current limits of +/- 20 mA.

(a) For Vp = 1V and R_L = 1kΩ, specify the resulting signal at the output.
(b) For Vp = 1.5 V and R_L = 1kΩ, specify the resulting signal at the output.
(c) For R_L = 1kΩ, specify the max value of Vp for which an undistorted sine-wave output is obtained.

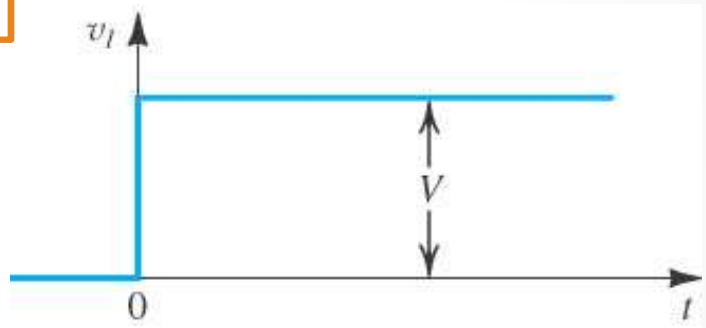


3. Slew rate limit: there is a specific maximum rate of change possible at the Output of a real op amp. This maximum is known as the slew rate (SR).
A nonlinear distortion can occur when large output signals are slew rate limited.

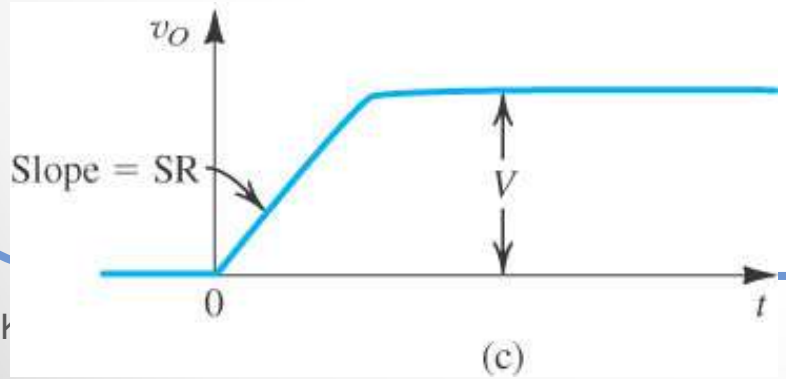
$$SR = \left.\frac{dv_O}{dt}\right|_{\max}$$



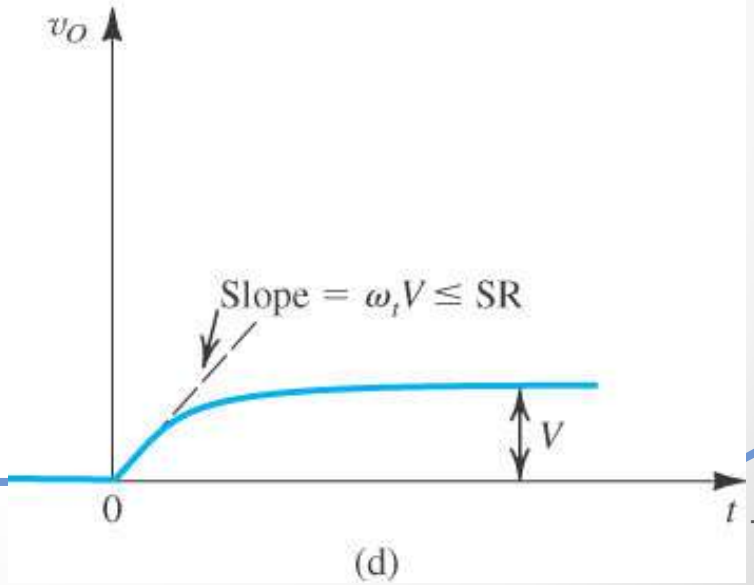
(a)



(b)



(c)



(d)

- SR is usually specified on the op amp data sheet in units of V/μs.

- It follows that if the input signal applied to an op amp circuit is such that it demands an output response that is faster than the specified value of SR, the op amp will not comply.

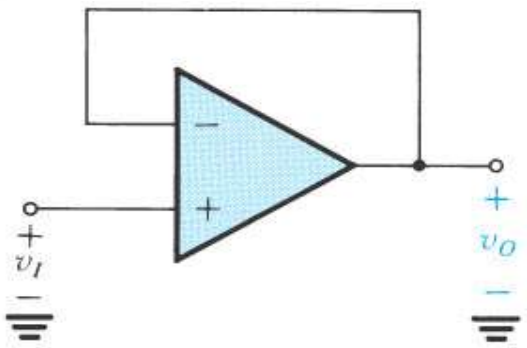
- The amplifier then said to be slewing and its output is slew-rate limited.

- This is distinct from the finite op amp bandwidth that limits the freq response of the closed-loop amplifiers. The limited bandwidth is a linear phenomenon and does not result in a change in the shape of an input sinusoid; that is, it does not lead to nonlinear distortion.

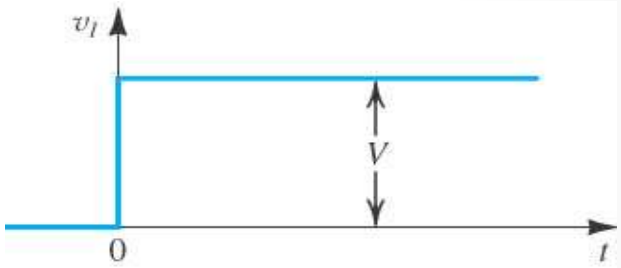
- The slew-rate limitation can cause nonlinear distortion to an input sinusoidal signal when its freq and amplitude are such that the corresponding ideal output would require v_O to change at a rate great than SR.

For the case of the follower, we have the transfer function of a low-pass STC

$$\frac{v_O(s)}{v_I(s)} = \frac{1 + R_2/R_1}{1 + \dfrac{s}{\omega_t/(1 + R_2/R_1)}}$$



(a)



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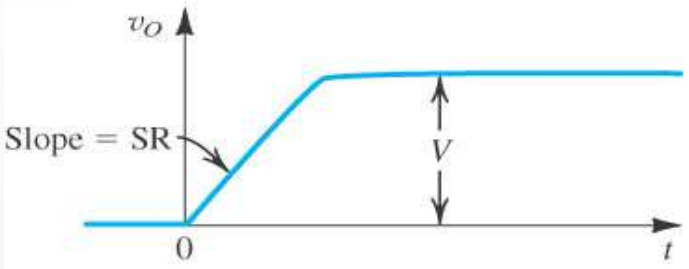

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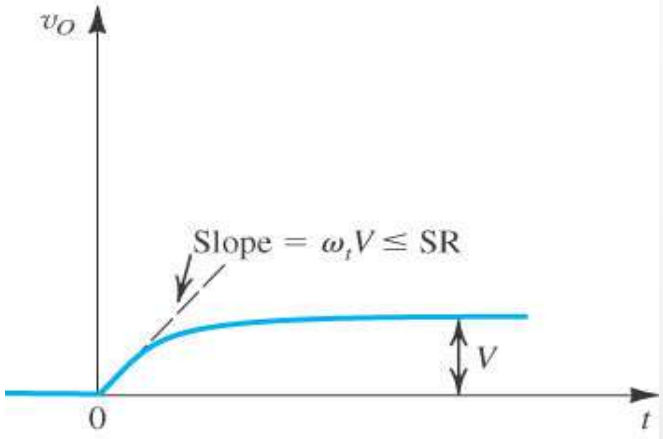
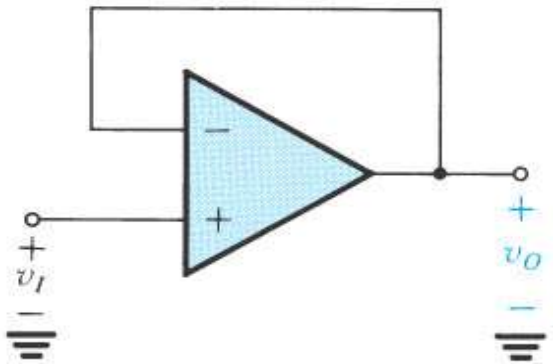


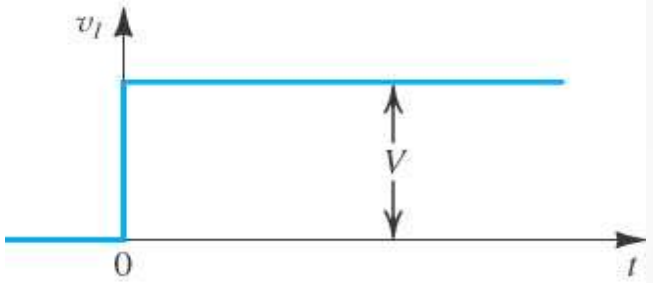
(d)

By substituting $R_1 = \infty$ and $R_2 = 0$, we'll get $$\frac{V_O}{V_i} = \frac{1}{1 + s/\omega_t}$$

Its step response would therefore be $$v_O(t) = V(1 - e^{-\omega_t t})$$



(a)



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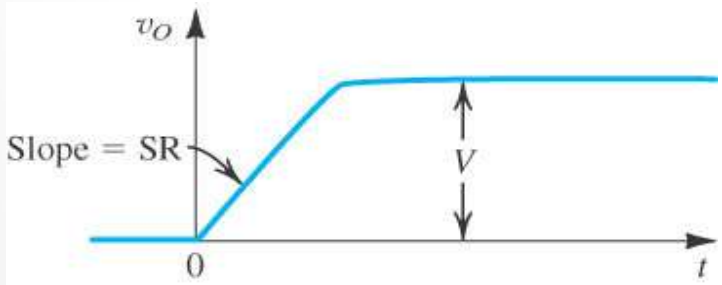

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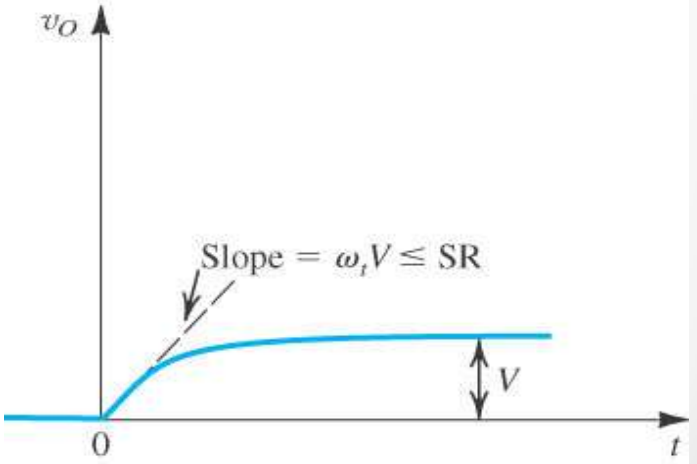


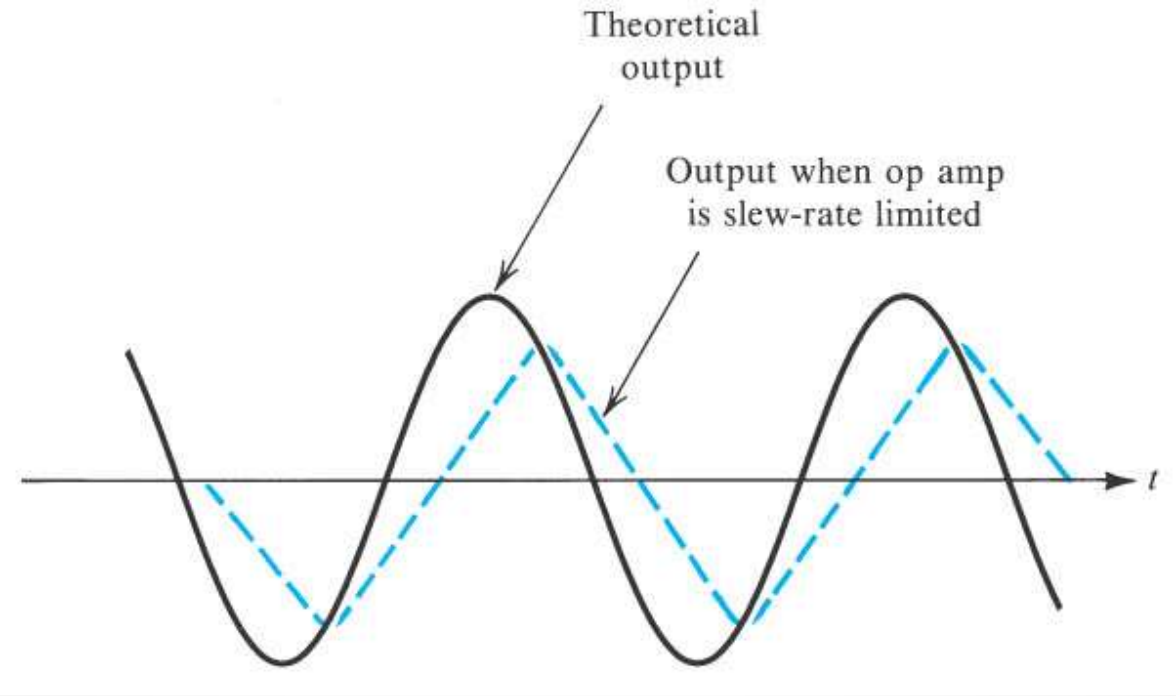
(d)

4. Full-Power Bandwidth: Op amp slew-rate limiting can cause nonlinear distortion in sinusoidal waveforms. Consider the unity-gain follower with an input given by

$$v_I = V_i \sin(\omega t)$$

The rate of change of this waveform is given by $\frac{dv_I}{dt} = \omega V_i \cos(\omega t)$

with a maximum value of ωVi, which occurs at the zero crossing of the input sinusoid. If ωVi exceeds the slew rate of the op amp, the output will be distorted as shown. The output cannot keep up with the large rate of change at its zero crossings, and the op amp slews.



The full-power bandwidth (f_M) is the freq at which an output sinusoid with amplitude equal to the rated output voltage of the op amp begins to show distortion due to slew-rate limiting.

$$\omega_M V_{OMax} = SR$$

Therefore,

$$f_M = \frac{SR}{2\pi V_{OMax}}$$

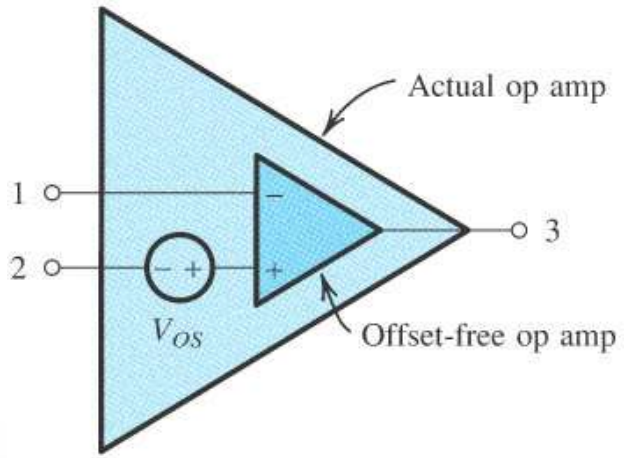
At a freq ω higher than ω_M, the max amplitude of the undistorted output sinusoid is given by

$$V_O = V_{OMax}\left(\frac{\omega_M}{\omega}\right)$$

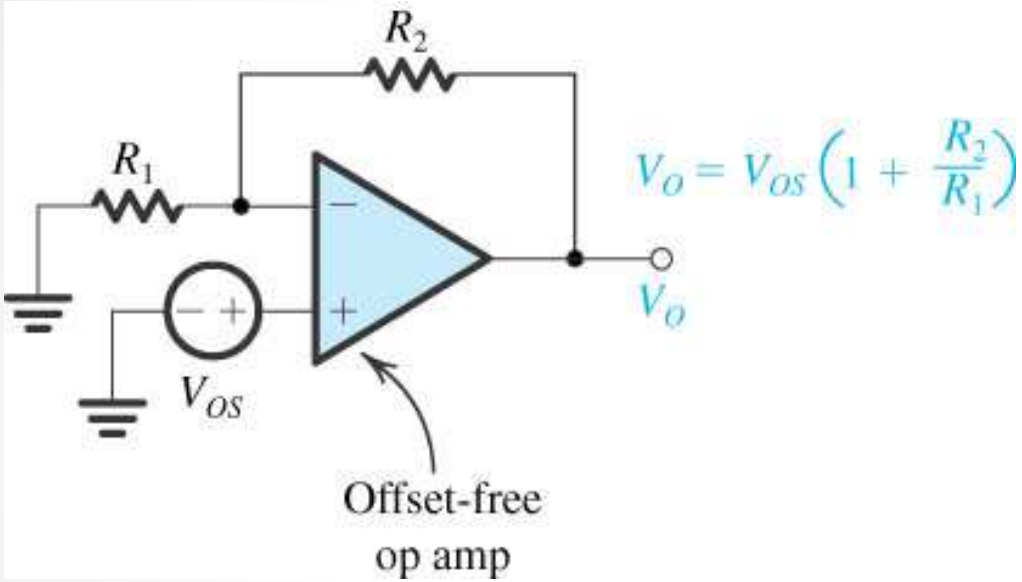
DC Imperfections

1. Offset Voltage: the input offset voltage (V_{OS}) arises as a result of the unavoidable mismatches present in the input differential stage inside the op amp. Its effect is to cause the output to be nonzero when the differential input is zero. The applied external source that brings the output back to zero will have an equal magnitude and opposite polarity to the V_{OS}.

- The op amp data sheet usually specify typical and max values for V_{OS} at room temp as well as the temp coeff of V_{OS} (usually in μV/°C). They do not specify the polarity of V_{OS} because the components mismatches are not known a priori; it may exhibit either a positive or a negative V_{OS}. The general purpose op amps exhibit V_{OS} in the range of 1 mV to 5 mV.

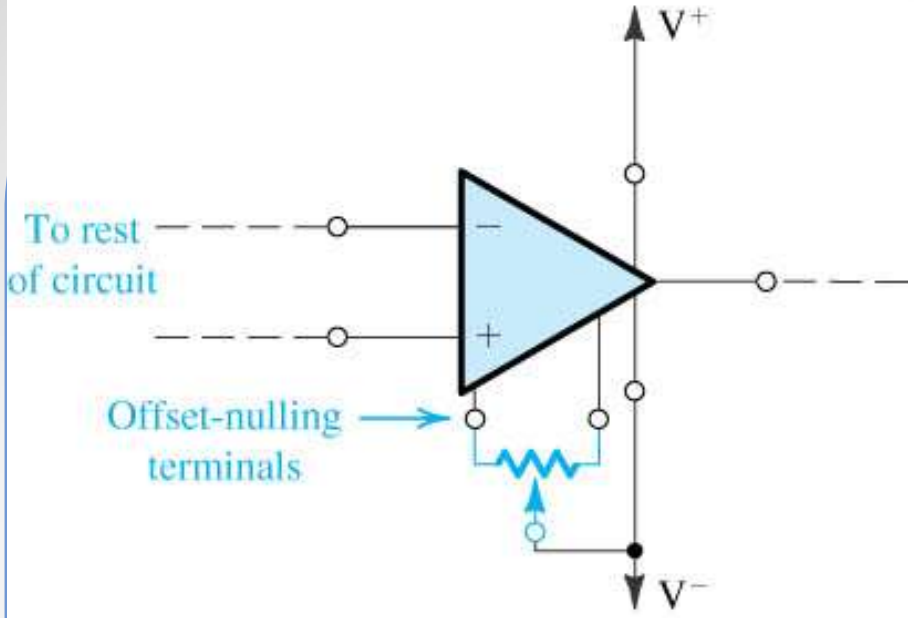


To analyze the circuit to determine the effect of the VOS, we replace voltage source with short circuited. Both inverting and noninverting amps would result in the same ckt as shown.



$$V_O = V_{OS}\left[1 + \frac{R_2}{R_1}\right]$$

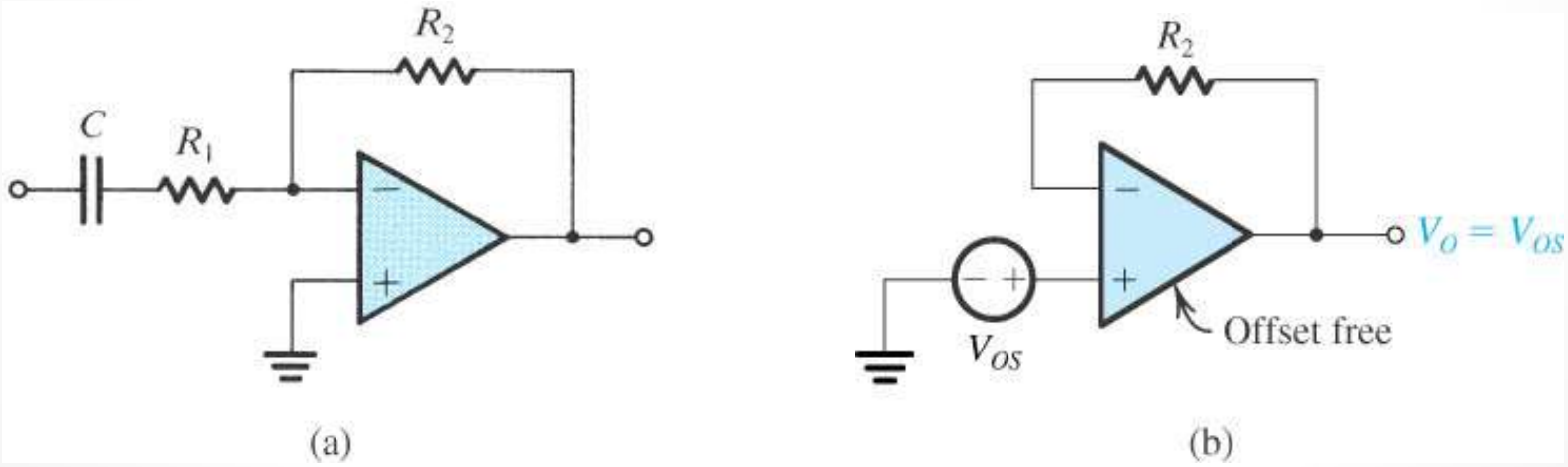
The output dc voltage can have large magnitude. For instance, a noninverting amp with a closed-loop gain of 1000, when constructed from an op amp with a 5-mV input offset voltage, will have a dc output of +5 V or -5V, rather than the ideal value of 0 V.



Some op amps are provided with 2 additional terminals to which a specified ckt can be connected to trim to zero the output dc voltage due to V_{OS}. A potentiometer is connected between the offset-nulling terminals with the wiper of the potentiometer connected to the op-amp negative supply. Moving the wiper would introduce imbalance that counteracts the asymmetry present in the internal op amp circuitry that gives rise to V_{OS}.

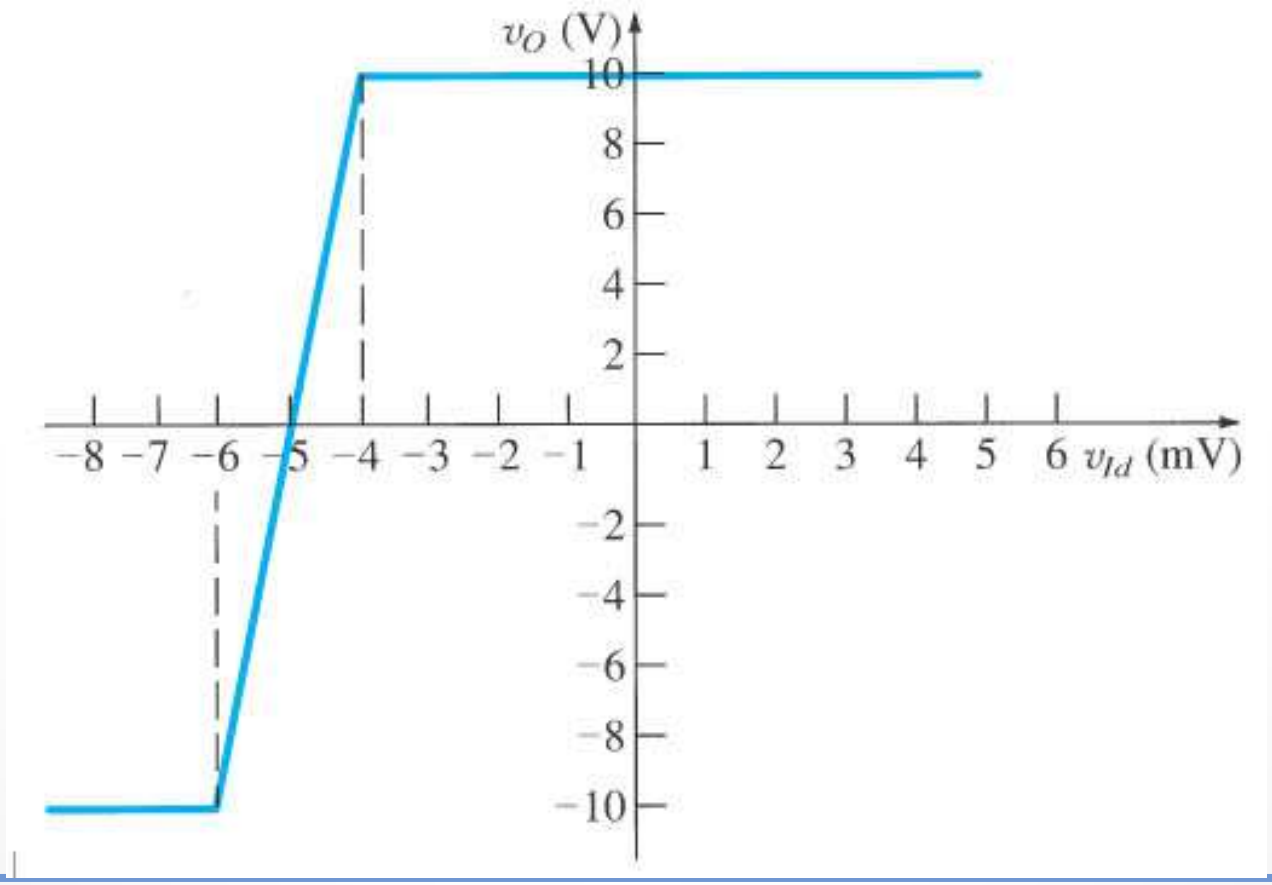
One way to overcome the dc offset problem is by capacitively coupling the amplifier. Because of its infinite impedance at dc, the coupling capacitor will cause the gain to be zero at dc. As result, V_{OS} sees in effect a unity-gain voltage follower, and the dc output voltage V_O will be equal to V_{OS} rather than $V_{OS}(1 + R_2/R_1)$.

The coupling cap C forms together with R1 an STC high-pass ckt w/ a corner freq of $\omega_o = 1/CR_1$.



(a) A capacitively coupled inverting amplifier, and **(b)** the equivalent circuit for determining its dc output offset voltage V_O.

Example: a sketch of the transfer characteristic v_O versus v_{Id} of an op amp having $A_O = 10^4$, output saturation levels of +/- 10 V, and V_{OS} of + 5 mV.

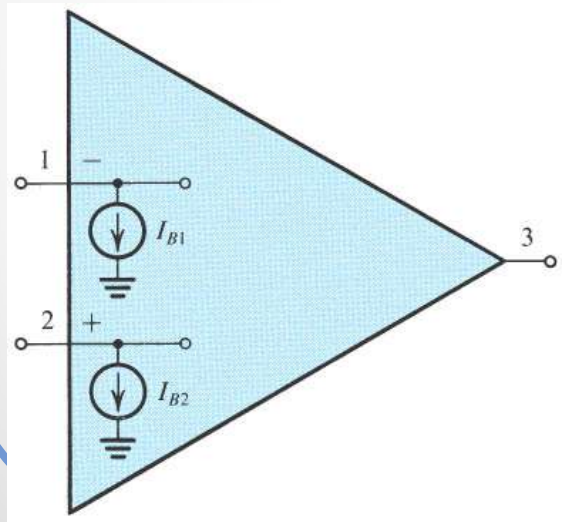


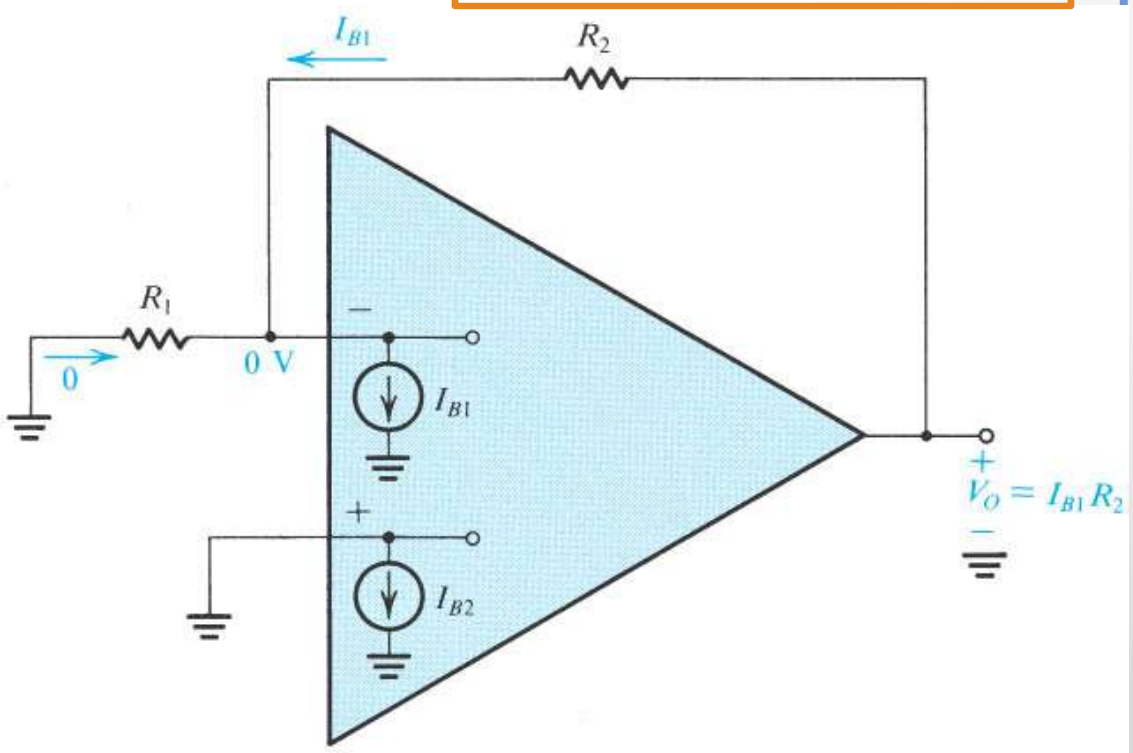
Input Bias and Offset Currents

In order for the op amp to operate, its 2 input terminals have to be supplied with dc current, termed the input biased currents. The op-omp manufacturer usually specifies the average value of I_{B1} and I_{B2}, as well as their expected difference. The average value I_B is called the input bias current and the difference is called the input offset current.

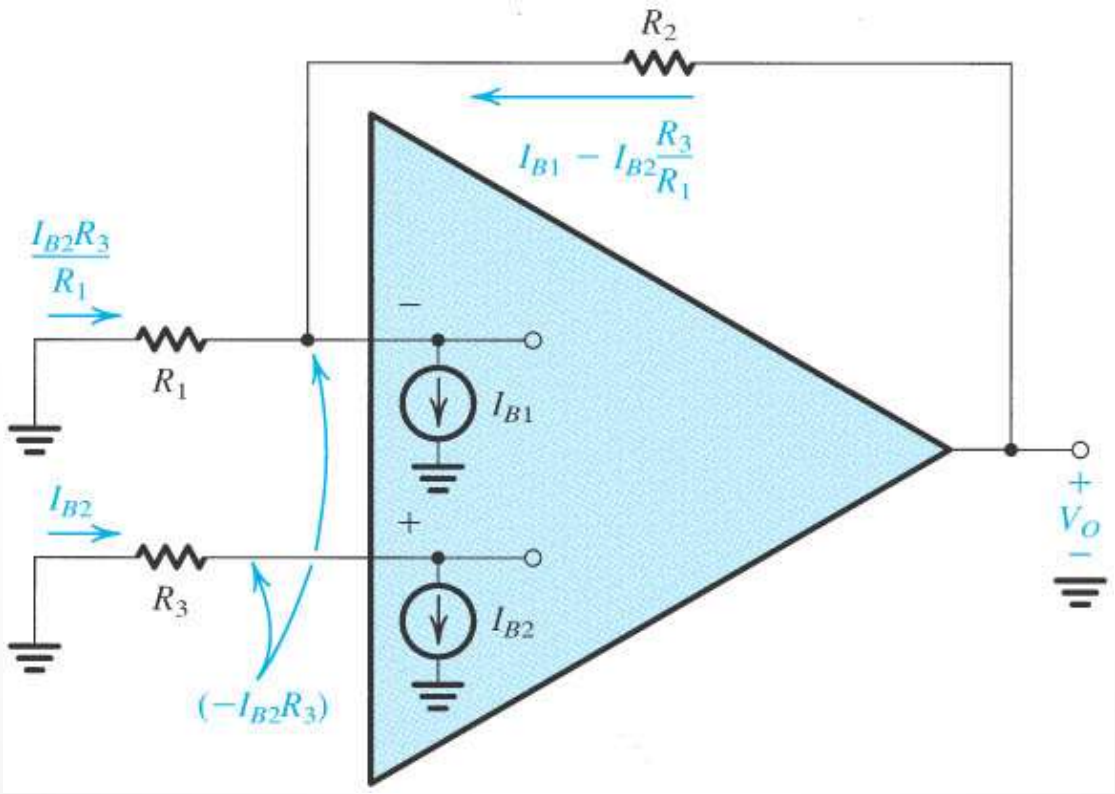
$$I_B = \frac{I_{B1} + I_{B2}}{2} \qquad I_{OS} = |I_{B1} - I_{B2}|$$

$$V_O = I_{B1}R_2 \approx I_B R_2$$





By introducing R_3 in series with the noninverting input lead, we can reduce the value of the output dc voltage due to the input bias currents. From a signal point of view, R_3 has negligible effect (ideally no effect).



$$V_O = -I_{B2}R_3 + R_2(I_{B1} - I_{B2}R_3 / R_1)$$

Consider the case $I_{B1} = I_{B2} = I_B$, which results in

$$V_O = I_B[R_2 - R_3(1 + R_2 / R_1)]$$

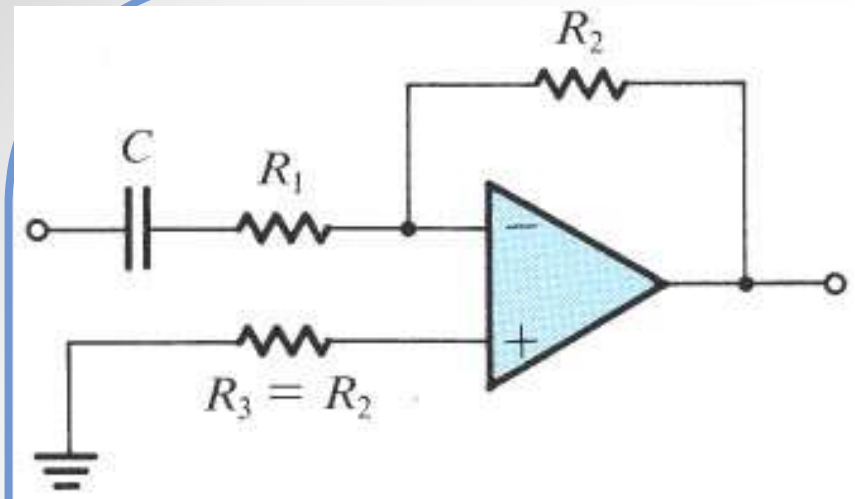
We can reduce V_O to zero by selecting R_3 such that

$$R_3 = \frac{R_2}{1 + R_2 / R_1} = \frac{R_1 R_2}{R_1 + R_2}$$

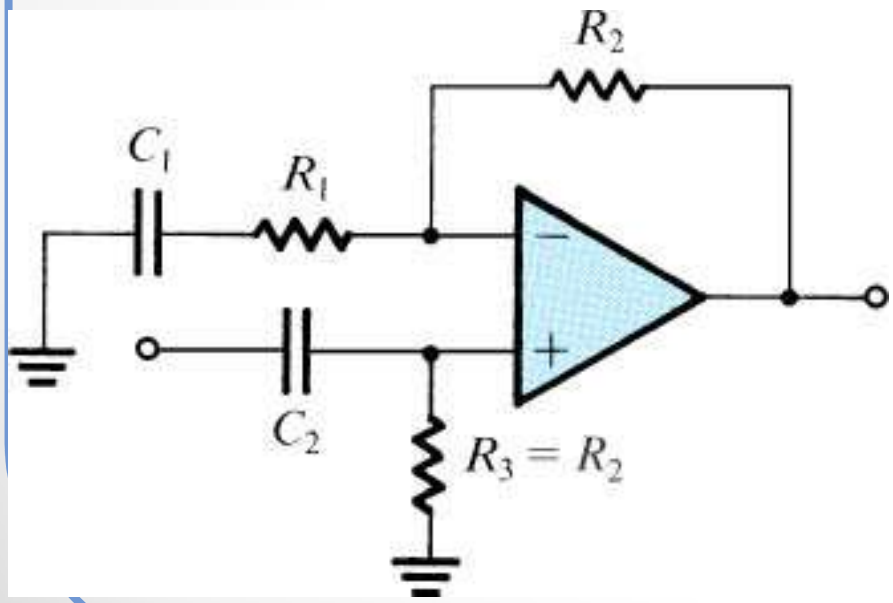
By using the above R_3 and $I_{B1} = I_B + I_{OS}/2$ and $I_{B2} = I_B - I_{OS}/2$, and substitute them in the topmost equation, we'll get

$$V_O = I_{OS}R_2$$

This Vo is usually about an order of magnitude smaller than the value obtained without R_3. Therefore, to minimize the effect of the input bias currents one should place in the positive lead a resistance equal to the dc resistance seen by the inverting terminal.



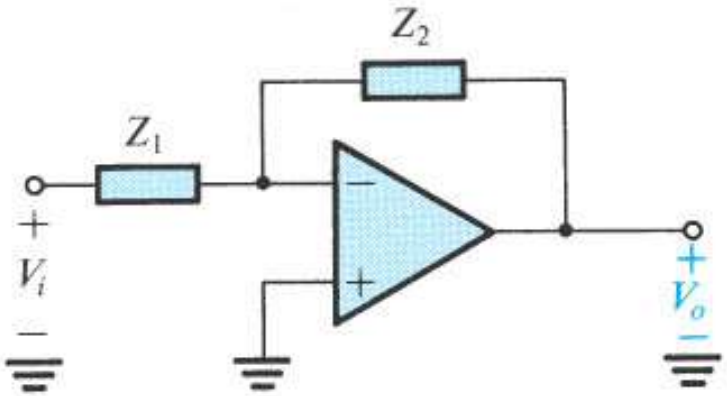
In an ac-coupled amplifier the dc resistance seen by the inverting terminal is R_2; hence R_3 is chosen equal to R_2.



Illustrating the need for a continuous dc path for each of the op-amp input terminals. Specifically, note that the amplifier will *not* work without resistor R_3.

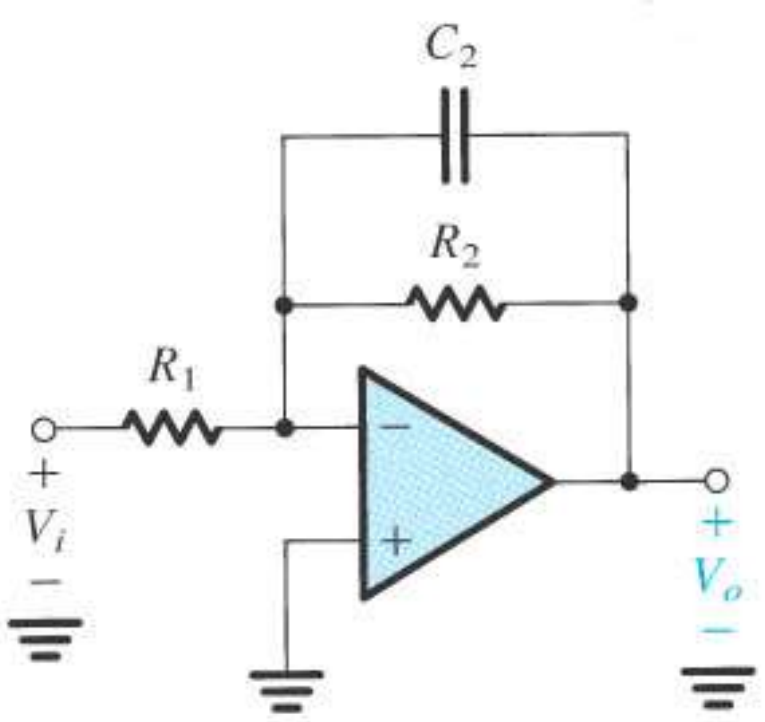
Integrators and Differentiators

The inverting config. w/ general impedances



$$\frac{V_o}{V_i} = -\frac{Z_2}{Z_1}$$

Example: for the ckt below, derive an expression for the transfer function $V_O(s)/V_i(s)$. Show that it is a low-pass STC ckt. Find the dc gain and the 3-dB freq.



$$\frac{V_O(s)}{V_i(s)} = -\frac{Z_2(s)}{Z_1(s)} = -\frac{1}{Z_1(s)Y_2(s)}$$

$$Z_1 = R_1 \quad \text{and} \quad Z_2 = R_2 \,||\, (1/sC_2)$$

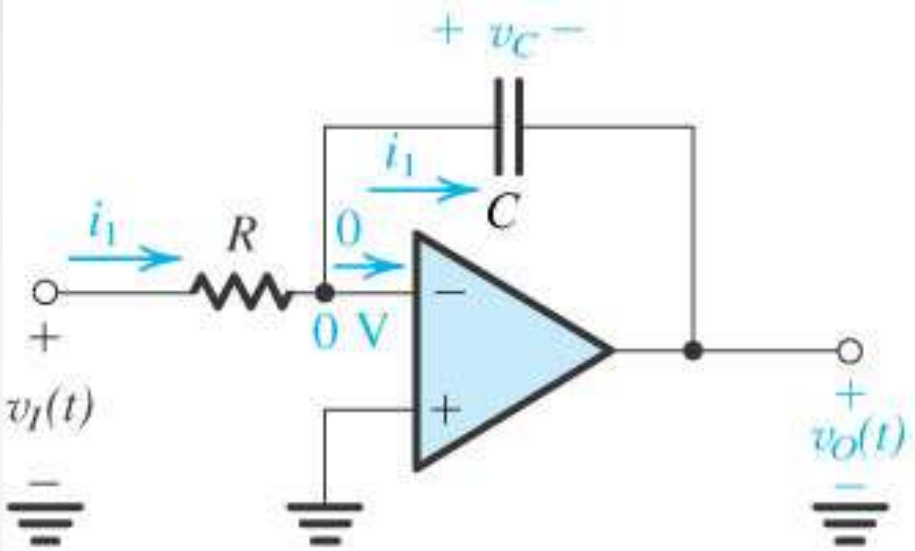
$$Y_2 = (1/R_2) + sC_2$$

$$\frac{V_O(s)}{V_i(s)} = -\frac{1}{\frac{R_1}{R_2} + sC_2R_1} = -\frac{R_2/R_1}{1+sC_2R_2}$$

DC gain is $K = -\dfrac{R_2}{R_1}$

3-dB freq is $\omega_O = \dfrac{1}{C_2R_2}$

The Inverting Integrator



(a)

$$v_O(t) = -\frac{1}{CR}\int_0^t v_I(t)\,dt$$

$$\frac{V_o}{V_i} = -\frac{1}{sCR}$$

Let the input be a time-varying function $v_I(t)$. The virtual ground at the inverting Op-amp input causes $v_I(t)$ to appear in effect across R, and thus the current $i_1(t)$ will be $v_I(t)/R$. This current flows thru the capacitor C, causing charge to accumulate on C.

$$v_C(t) = V_C + \frac{1}{C}\int_0^t i_1(t)dt$$

where V_C is the initial voltage on C at t = 0.

The output voltage $v_O(t) = -v_C(t)$ so $v_O(t) = -V_C - \frac{1}{RC}\int_0^t v_I(t)dt$

RC is called the integrator time-constant. Since there is a negative sign at the output voltage, this integrator ckt is said to be an inverting integrator or a Miller integrator.

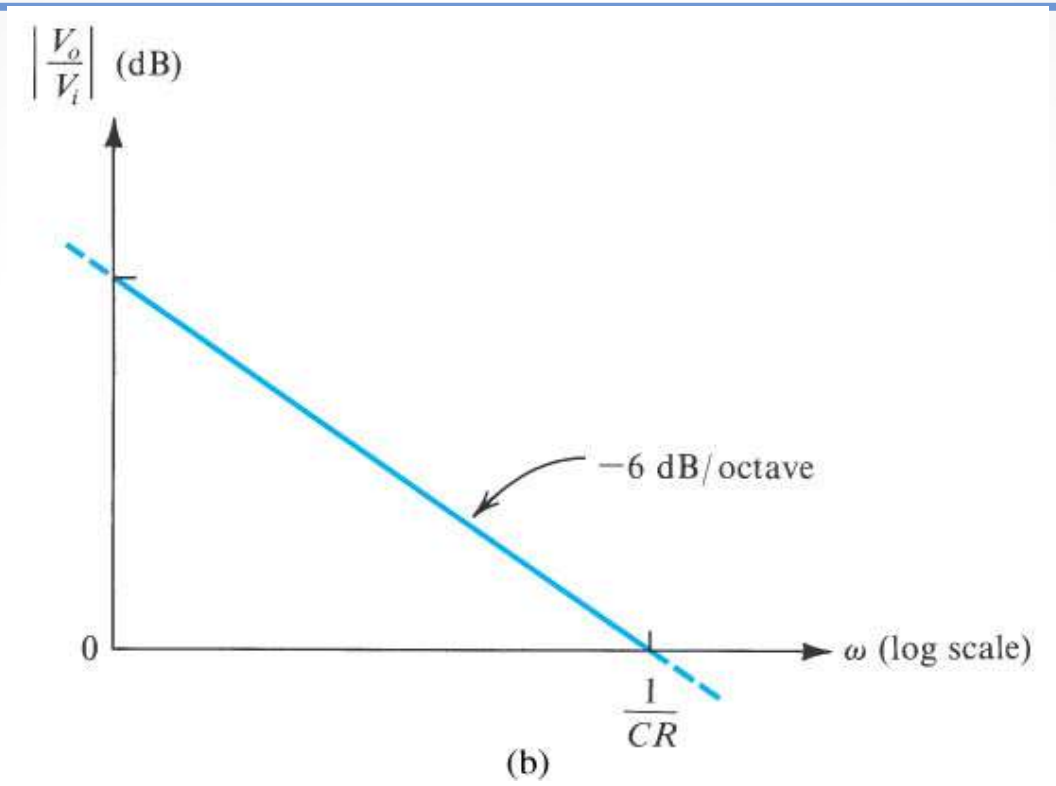
The operation can be described alternatively in the freq domain by substituting $Z_1(s) = R$ and $Z_2(s) = 1/sC$ to obtain the transfer funtion:

$$\frac{V_O(s)}{V_i(s)} = -\frac{1}{sCR}$$

$$\frac{V_O(j\omega)}{V_i(j\omega)} = -\frac{1}{j\omega CR}$$

Thus the integrator function has magnitude $\left|\frac{V_O(j\omega)}{V_i(j\omega)}\right| = \frac{1}{\omega CR}$

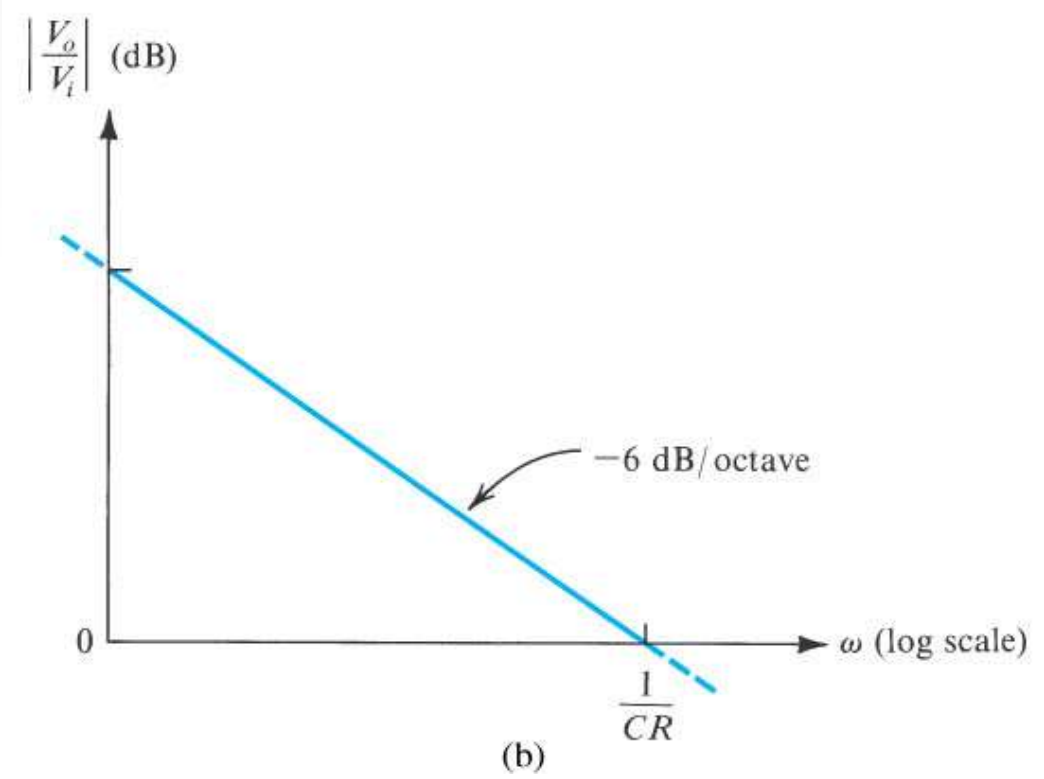
and phase $\phi = +90^O$



The Bode plot is straight line of slope -6 dB/octave. This line intercepts the 0-dB line at the freq that makes $|V_O/V_i|= 1$.

$$\omega_{\text{int}} = \frac{1}{RC}$$

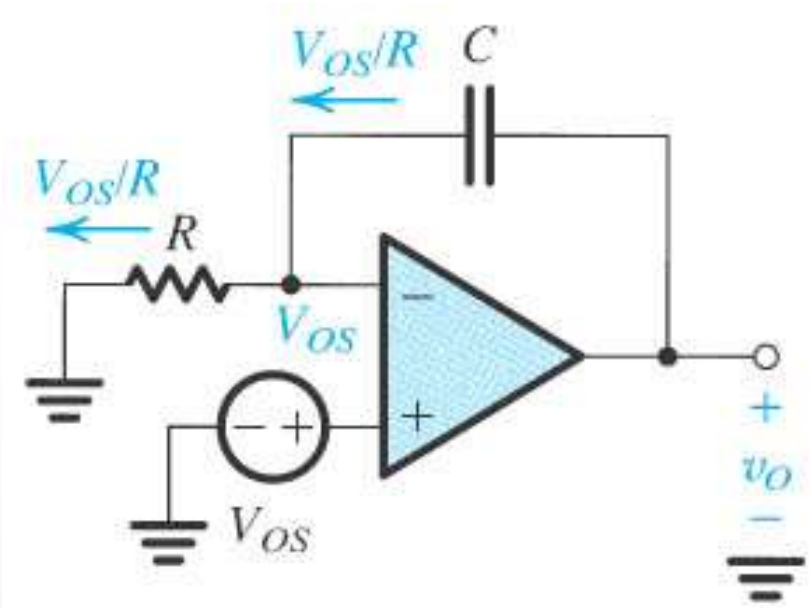
This is called the integrator frequency which is the inverse of the integrator time constant.



Comparison of the frequency response of the integrator to that of an STC low-pass network indicates that the integrator behaves as a low-pass filter with a corner freq of zero. Observe also that at ω = 0, the magnitude of the integrator transfer function is infinite. This indicates that at dc the op amp operates with an open loop.

The op amp will suffer deleterious effects from the presence of the op amp input dc offset voltage and current.

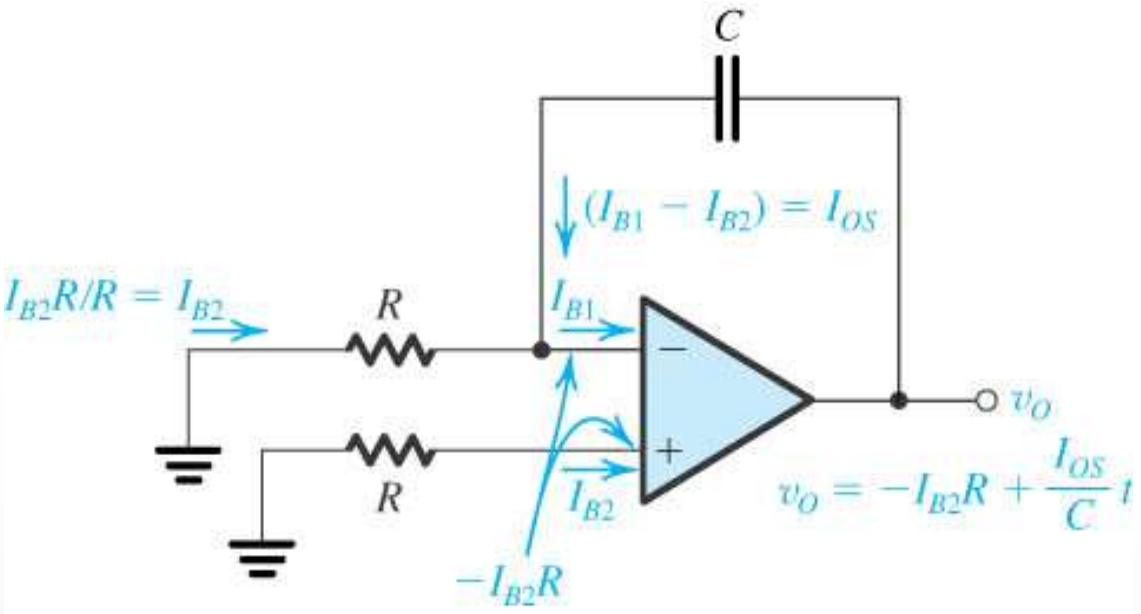
The offset voltage will drive v_O up linearly until op-amp saturates.



$$v_O = V_{OS} + \frac{1}{C}\int_0^t \frac{V_{OS}}{R}dt$$

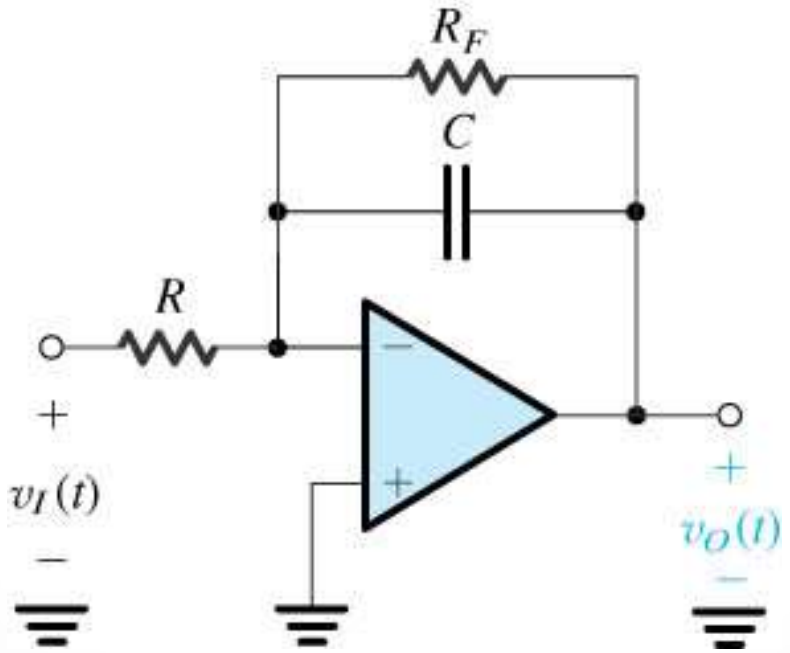
$$= V_{OS} + \frac{V_{OS}}{CR}t$$

Offset current will also cause v_O to ramp linearly with time unit op amp Saturates.



The dc problem of the integrator ckt can be alleviated by connecting R_F across the integrator capacitor C, as shown.

Such a resistor provides a dc path through which the dc current (V_{OS}/R) and I_{OS} can flow, with the result that v_O will now have a dc component $[V_{OS} (1 + R_F/R) + I_{OS}R_F]$ instead of rising linearly.

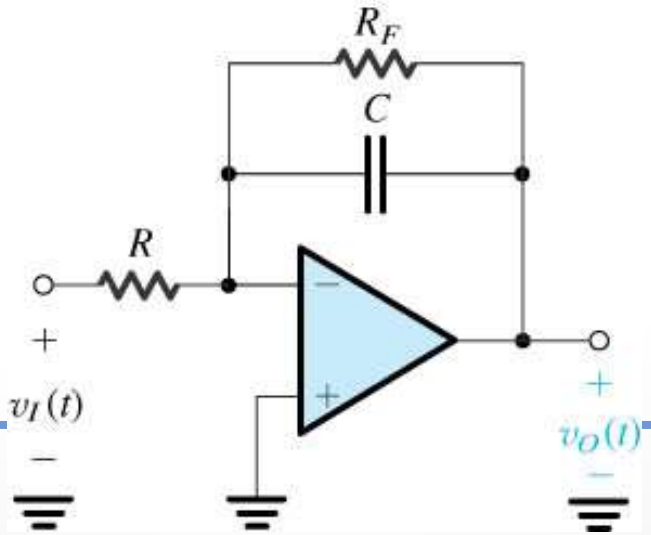


- To keep the dc offset at the output small, one would select a low value for R_F.
- Unfortunately, the lower the value of R_F, the less ideal the integrator ckt becomes. This is because R_F causes the freq of the integrator pole to move from its ideal location at ω = 0 to one determined by the corner freq of the STC network (R_F, C). Specifically, the integrator transfer function becomes

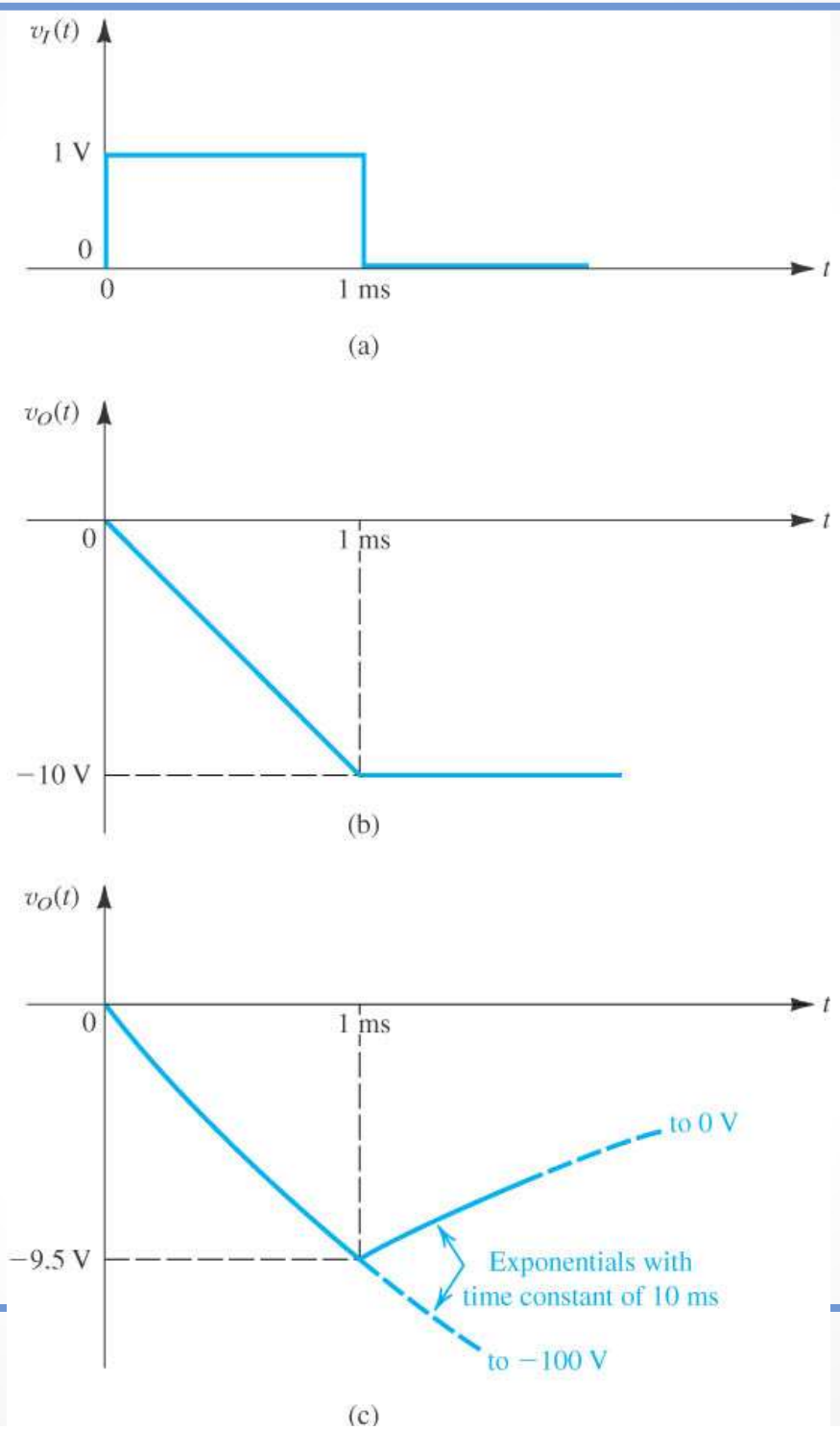
$$\frac{V_O(s)}{V_i(s)} = -\frac{R_F / R}{1 + sCR_F}$$

as opposed to the ideal function of -1/sCR.

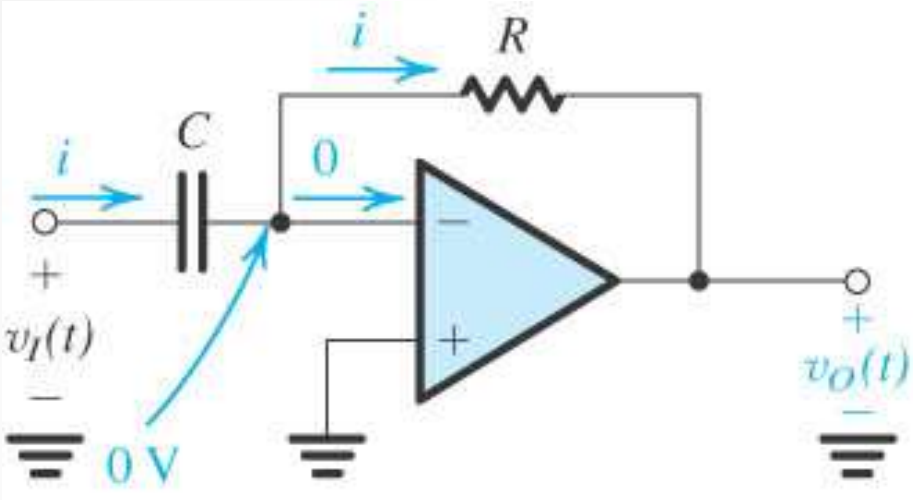
- The lower the value we select for R_F, the higher the corner freq ($1/CR_F$) will be and the more nonideal the integrator becomes.



Example: Find the output produced by a Miller integrator in response to an input pulse of 1-V height and 1-ms width. Let R = 10 kΩ and C = 10nF. If the integrator capacitor is shunted by a 1-MΩ resistor, how will the response be modified? The op-amp is specified to saturate at +/- 13 V.


$v_I(t)$
1 V
0
0
1 ms
t
(a)
$v_O(t)$
0
1 ms
t
−10 V
(b)
$v_O(t)$
0
1 ms
t
to 0 V
−9.5 V
Exponentials with
time constant of 10 ms
to −100 V
(c)

The op amp differentiator



(a)

$$i(t) = C\frac{dv_I(t)}{dt}$$

$$v_O(t) = -CR\frac{dv_I(t)}{dt}$$

$$\frac{V_o}{V_i} = -sCR$$

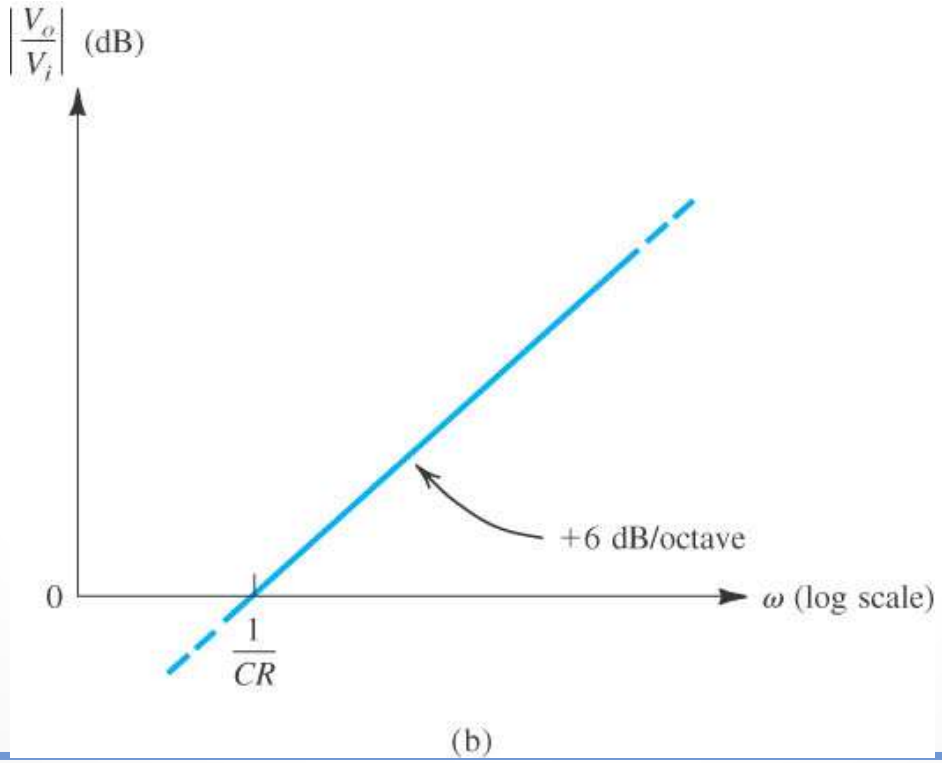
Interchange the location of the cap and the resist of the integrator ckt to get the differentiator. The freq-domain transfer function of the ckt can be found by substituting Z1(s) = 1/sC and Z2(s) = R:

$$\frac{V_O(s)}{V_i(s)} = -sCR$$

$$\frac{V_O(j\omega)}{V_i(j\omega)} = -j\omega CR$$

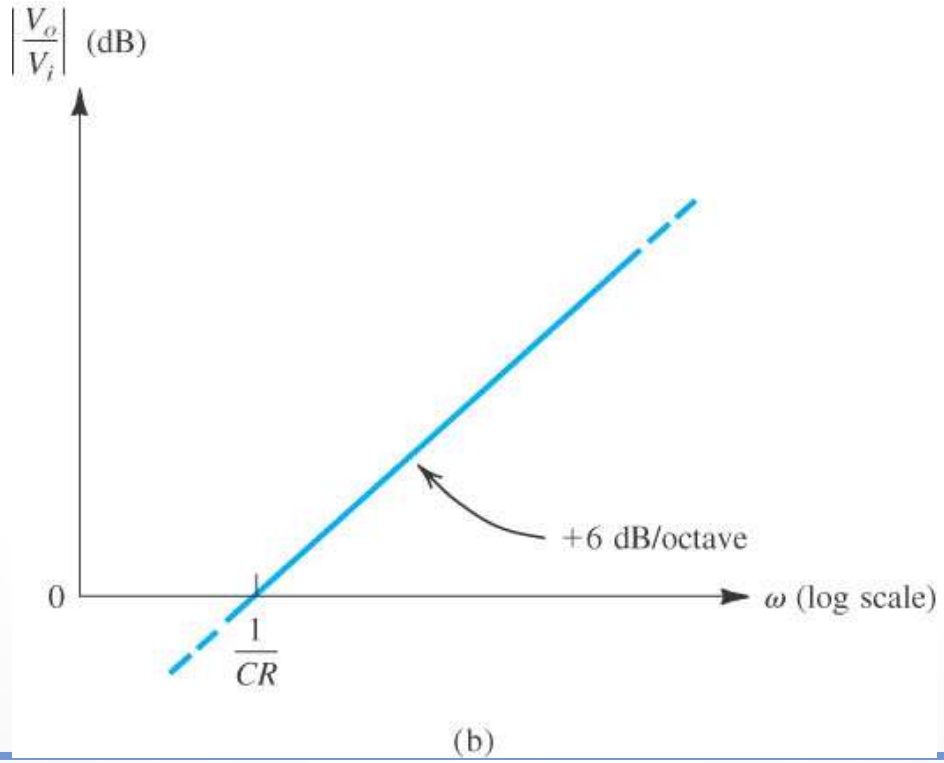
$$\left|\frac{V_O(j\omega)}{V_i(j\omega)}\right| = \omega CR \qquad \text{and} \qquad \phi = -90^O$$

The Bode-plot is a straight-line of slope +6 dB/octave (or +20 dB/decade) intersecting the 0-dB line (where || = 1) at ω = 1/RC, where RC is the differentiator time-constant.



(b)

- The freq response of the differentiator can be thought of as that of an STC high-pass filter with a corner freq at infinity.
- It is a “noise-magnifier” since spike introduced at the output every time there is a sharp change in $v_I(t)$.
- When the ckt is used, it is usually necessary to connect a small-valued resistor in series with the capacitor. This modification would make the ckt nonideal.



(b)

Reference

Microelectronic Circuits by Adel S. Sedra & Kenneth C. Smith. Saunders College Publishing

Wi-Fi passwords of airports around the world: goo.gl/8KBBWL

SAFETY AT WORK

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