Seat Number

**King Mongkut's University of Technology Thonburi**
**Final Examination**
**Semester 1 -- Academic Year 2015**

**Subject:** EIE 334 Microprocessors
**For:** Electrical Communication and Electronic Engineering, 3rd Yr. (Inter. Program)
**Exam Date:** Friday November 27th, 2015 **Time:** 9.00-12.00 pm.

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**Instructions:-**

1. This exam consists of 5 problems with a total of 9 pages, including the cover.
2. This exam is open books. (but electronics dictionary, smart watch, any communication devices are not allowed)
3. Answer each problem on the exam itself.
4. A calculator complying with the university rule is allowed.
5. **Do not take** any exam papers and answer sheets outside the exam room.

**Remarks:-**

- **Raise your hand when you finish the exam to ask for a permission to leave the exam room.**
- **Students who fail to follow the exam instruction might eventually result in a failure of the class or may receive the highest punishment with university rules.**
- **Carefully read the entire exam before you start to solve problems. Before jumping into the mathematics, think about what the question is asking. Investing a few minutes of thought may allow you to avoid twenty minutes of needless calculation!**

| Exam No. | 1 | 2 | 3 | 4 | 5 | TOTAL |
|---|---|---|---|---|---|---|
| Full Score | 14 | 15 | 24 | 35 | 31 | 119 |
| Graded Score | | | | | | |

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**Name** _____ **Student ID** _____

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Mr. Dejwoot KHAWPARISUTH (tel: 9065, 9070)
An examiner

R. Silapunt

**(Assoc. Prof. Rardchawadee Silapunt, Ph.D.)**
**Head of Electronic and Telecommunication Engineering Department**

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1.] Answer the following briefly but precise. (for the Cortex-M0 processor: NUC140)

**(14 points)**

1.1.) Which bit is set by hardware when PWM group input channel 3 has a falling transition?

ANS: _____ (2 points)

1.1.1. In which register? ANS: _____ (2 points)

1.2.) Which bit determines PWM timer 6 mode? ANS: _____ (2 points)

1.2.1. In which register? ANS: _____ (2 points)

1.3.) Which pin (Px.y) can we use for timer 2 event counting? ANS: _____

(2 points)

1.4.) The address of the **REGWRPROT** Register: ANS: _____ (2 points)

1.5.) Which register hold the current value in 16-bit counter of PWM1? ANS: _____

(2 points)

2.] The following multiple choice questions are for the Cortex-M0 processor :

(wrong answer = -2 pts, no answer = 0 pts and correct answer = 3 points)

**(15 points)**

2.1.) Which of the following is **incorrect**?

a. Handler mode is entered as a result of an exception.
b. 32-bit CISC processor
c. implements the ARMv6-M Thumb® instruction set
d. Thread mode is entered on Reset, and can be entered as a result of an exception return.

2.2.) Which of the following is **incorrect** (for Exception and Interrupt)?

a. The highest user-configurable priority is denoted as "0".
b. Software can set four levels of priority on some of exceptions as well as on all interrupts.
c. The default priority of all the user-configurable interrupts is "3".
d. Reset is the highest priority exception. It is permanently enabled and has a fixed priority of -3.

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2.3.) Which of the following is **incorrect**?

a. In Handler mode, the processor always uses the main stack.

b. On reset, the processor loads the MSP with the value from address 0x00000000.

c. On reset, the processor loads the PC with the value of the reset vector, at address 0x00000004.

d. The processor has a fixed memory map that provides up to 8GB of addressable memory.

2.4.) Which of the following is **incorrect** (Timer)?

a. When TDR_EN is set, TDR (Timer Data Register) will be updated continuously with the 24-bit up-timer value as the timer is counting.

b. If timer interrupt is enabled, the timer asserts its interrupt signal when the associated up-timer value is equal to TCMPR.

c. While TEXEN = 1, and TEX_EDGE = 01, a 1 to 0 transition on the TEX pin causes the TEXIF to be set.

d. While TEXIEN = 1, TEXEN = 1, and TEX_EDGE = 10, a 0 to 1 transition on the TEX pin will cause the TEXIF(TEXISR[0]) interrupt flag to be set then the interrupt signal is generated and sent to NVIC to inform CPU.

2.5.) Which of the following is **incorrect** (PWM0)?

a. When re-start next one-shot operation, the PWMA->CNR0 should be written first.

b. As PWM0 operate at auto-reload mode, CMR0 and CNR0 should be written first and then set CH0EN bit to 1 to enable PWM0 counter start running.

c. As PWM0 operate at auto-reload mode, the value of CNR0 will reload to PWM0 counter when it down count reaches zero.

d. If PWMA->CNR0 is set to zero, PWM0 counter will be held.

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3.] Using the following values (or if not provided, use value(s) after RESET) in the registers to answer the following questions: (show how to get the answer) **(24 points)**

```
PWMA->CNR2 = 0x0000_C274
PWMB->CNR2 = 0x0000_7AB8
PWMA->CMR2 = 0x0000_63AE
PWMB->CMR2 = 0x0000_1CD2
PWMA->CNR3 = 0x0000_9D92
PWMB->CNR3 = 0x0000_EC7B
PWMA->CMR3 = 0x0000_3126
PWMB->CMR3 = 0x0000_2E35
PWMA->PPR = 0xCCDD_FAEB
PWMB->PPR = 0x0000_EF01
PWMA->CSR = 0x0000_3402
PWMB->CSR = 0x0000_3214
WTCR = 0x8000_0682
CLKSEL0 = 0x0000_003F
CLKSEL1 = 0xD200_003D
CLKSEL2 = 0x0000_21FF
CLKDIV = 0x0008_3EFF
```

3.1.) What is the **CPUCLK** frequency? (6 points)

3.2.) What is the Maximum $T_{WTR}$ in seconds (WDT)? (5 points)

3.3.) What is the frequency of **PWM3**? (7 points)

3.4.) What is the **PWM6 low width** in seconds? (6 points)

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4.] Write programs for each of the following tasks using as **few lines of code** as you can using Cortex-M0 instruction set. **(35 points)**

4.1.) To count the number of ones in R1 and R2 (64 bits) (10 points)

```
;
; Input: R1, R2
; Output: R0 = the number of ones
;
countOne
```

4.2.) To calculate the product: [R1:R0] = R3 * 1020 (10 points)

(Not allowed to use MULS, **MUST** use Shift Operations)

```
;
; Input: R3
; Output: [R1:R0] = R3 * 1020

mul1020
```

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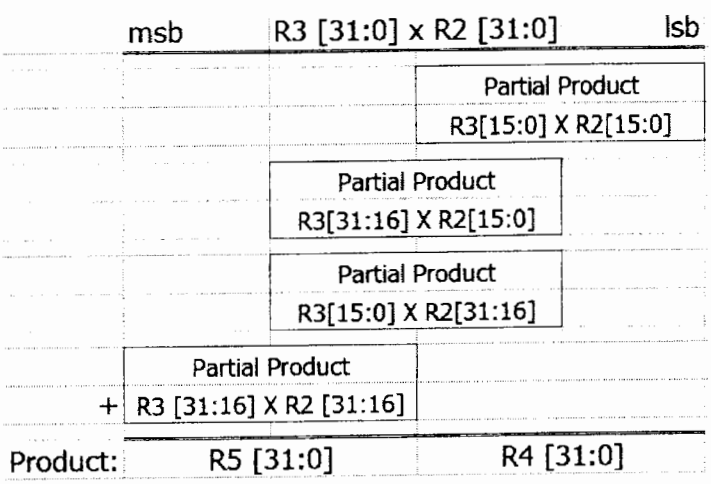
4.3.) 32-Bit Unsigned Multiplication: To multiply two unsigned 32-bit integers passed in R2 and R3 and return the product in [R5:R4] (64 bits) (15 points)

```
;
; Input: R2,R3
; Output: [R5:R4] = R3 * R2
mul32
    LSLS R6,R2,#16
    LSRS R6,R6,#16    ; R6 = R2[15:0]
    MOV R4,R6
    LSLS R7,R3,#16
    LSRS R7,R7,#16    ; R7 = R3[15:0]
    MULS R4,R7,R4     ; Partial Product: R3[15:0]*R2[15:0]
```



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5.] From the following program (from start: till stop :) (31 points)

Fill the table using only a number in base 16, show the results of the execution.

```
start

      ORRS R0,R0,R1
      EORS R1,R1,R2
      ASRS R2,#05
      ADCS R0,R1
      REV16 R1,R5
      BHI SKIP_NOP
      NOP
SKIP_NOP
      STM R3!,{R4}
      PUSH {R5}
      LDRB R1,[R3,#3]
      SXTH R0,R4
      MULS R4,R5,R4
      CMN R0,R1
      BHS SKIP_NOP2
      NOP
SKIP_NOP2
      POP {R0,R2,R4}

stop
```

| | | | | flag | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Step# | PC | | SP | N | Z | C | V | Branch taken? (Yes/No) | R0 | R1 | R2 | R3 | R4 | R5 |
| | | | 0x2000 04D4 | 0 | 0 | 0 | 0 | | 0xF479 3626 | 0xF0F0 FF00 | 0x283D 8032 | 0x2000 04D8 | 0xD0B8 CE69 | 0xB8F8 3DA2 |
| 1 | 0x00000178 | ORRS R0,R0,R1 | | | | | | | | | | | | |
| 2 | | EORS R1,R1,R2 | | | | | | | | | | | | |
| 3 | | ASRS R2,#05 | | | | | | | | | | | | |
| 4 | | ADCS R0,R1 | | | | | | | | | | | | |
| 5 | | REV16 R1,R5 | | | | | | | | | | | | |
| 6 | | BHI SKIP_NOP | | | | | | | | | | | | |
| 7 | | STM R3!,{R4} | | | | | | | | | | | | |
| 8 | | PUSH {R5} | | | | | | | | | | | | |
| 9 | | LDRB R1,[R3,#3] | | | | | | | | | | | | |
| 10 | | SXTH R0,R4 | | | | | | | | | | | | |
| 11 | | MULS R4,R5,R4 | | | | | | | | | | | | |
| 12 | | CMN R0,R1 | | | | | | | | | | | | |
| 13 | | BHS SKIP_NOP2 | | | | | | | | | | | | |
| 14 | | NOP | | | | | | | | | | | | |
| 15 | | POP {R0,R2,R4} | | | | | | | | | | | | |
| 16 | | | | | | | | | | | | | | |
| 17 | | | | | | | | | | | | | | |
| 18 | | | | | | | | | | | | | | |
| 19 | | | | | | | | | | | | | | |

| PC | | 0x200004D0 | 0x200004D1 | 0x200004D2 | 0x200004D3 | 0x200004D4 | 0x200004D5 | 0x200004D6 | 0x200004D7 | 0x200004D8 | 0x200004D9 | 0x200004DA | 0x200004DB | 0x200004DC | 0x200004DD | 0x200004DE | 0x200004DF | 0x200004E0 | 0x200004E1 | 0x200004E2 | 0x200004E3 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 0x00 | 0x01 | 0x02 | 0x03 | 0x04 | 0x05 | 0x06 | 0x07 | 0x08 | 0x09 | 0x0A | 0x0B | 0x0C | 0x0D | 0x0E | 0x0F | 0x10 | 0x11 | 0x12 | 0x13 |
| 0x00000178 | ORRS R0,R0,R1 | | | | | | | | | | | | | | | | | | | | |
| | EORS R1,R1,R2 | | | | | | | | | | | | | | | | | | | | |
| | ASRS R2,#05 | | | | | | | | | | | | | | | | | | | | |
| | ADCS R0,R1 | | | | | | | | | | | | | | | | | | | | |
| | REV16 R1,R5 | | | | | | | | | | | | | | | | | | | | |
| | BHI SKIP_NOP | | | | | | | | | | | | | | | | | | | | |
| | STM R3!,{R4} | | | | | | | | | | | | | | | | | | | | |
| | PUSH {R5} | | | | | | | | | | | | | | | | | | | | |
| | LDRB R1,[R3,#3] | | | | | | | | | | | | | | | | | | | | |
| | SXTH R0,R4 | | | | | | | | | | | | | | | | | | | | |
| | MULS R4,R5,R4 | | | | | | | | | | | | | | | | | | | | |
| | CMN R0,R1 | | | | | | | | | | | | | | | | | | | | |
| | BHS SKIP_NOP2 | | | | | | | | | | | | | | | | | | | | |
| | NOP | | | | | | | | | | | | | | | | | | | | |
| | POP {R0,R2,R4} | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | |
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