Seat
Number

King Mongkut's University of Technology Thonburi
Midterm Examination
Semester 1 -- Academic Year 2016

Subject: EIE 334 Microprocessors

For: Electrical Communication and Electronic Engineering, 3rd Yr. (Inter. Program)

Exam Date: Thursday September 22, 2016 **Time:** 9.00-12.00 pm.

Instructions:-

1. This exam consists of 4 problems with a total of 9 pages, including the cover.
2. This exam is open books. (but electronics dictionary, smart watch, any communication devices are not allowed)
3. Answer each problem on the exam itself.
4. A calculator complying with the university rule is allowed.
5. **Do not** bring any exam papers and answer sheets outside the exam room.

Remarks:-

- **Raise your hand when you finish the exam to ask for a permission to leave the exam room.**
- **Students who fail to follow the exam instruction might eventually result in a failure of the class or may receive the highest punishment with university rules.**
- **Carefully read the entire exam before you start to solve problems. Before jumping into the mathematics, think about what the question is asking. Investing a few minutes of thought may allow you to avoid twenty minutes of needless calculation!**

Exam No.	1	2	3	4	TOTAL
Full Score	15	46	20	23	104
Graded Score					

Name ______________________________ **Student ID** ________________

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An examiner

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Head of Electronic and Telecommunication Engineering Department

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1.] Please answer the following questions and show your work in details,

1.1.) use the information in the following table.

Processor	Clock rate	No.Instructions	Time
P1	2.5 GHz.	25×10^9	6 s.
P2	1.75 GHz.	40×10^9	12 s.
P3	4 GHz.	80×10^9	10 s.

1.1.1. Find the IPC (instructions per cycle) for each processor. **(4 points)**

1.1.2. Find the clock rate for P2 that reduces its execution time to that of P1. **(2 points)**

1.1.3. Find the number of instruction for P2 that reduces its execution time to that of P3. **(2 points)**

1.2.) Consider two different implementations of the same instruction set architecture. There are four classes of instructions A,B,C, and D. The clock rate and CPI of each implementation are given in the following table.

Processor	Clock rate	CPI Class A	CPI Class B	CPI Class C	CPI Class D
P1	3 GHz.	1	2	3	4
P2	4 GHz.	2	2	3	3

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1.2.1. Given a program with 10^9 instructions divided into classes as follows: 25% Class A, 45% Class B, 20% Class C and 10% Class D, which implementation is faster? (4 points)

1.2.2. What is the global CPI for each implementation? (3 points)

2.] Please answer the following questions and show your work in details.

2.1.) For the binary entries below, what MIPS instruction do they represent?

2.1.1. Hex: `0x000763c0` (3 points)

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2.1.2. Hex: `0x33620fa0` (3 points)

2.1.3. Hex: `0x7398c020` (3 points)

2.2.) Translate MIPS instructions into machine code (use number only in base 16, and program start at 0x400024) (9 points)

Label	Mnemonic	Opcode	rs	rt	rd	Shamt	funct
					Immediate		
			Address				
main:	**`addu $t7,$s6,$a2`**						
loop:	**`nop`**	0	0	0	0	0	0
	`bgez $k0,main`						
	`nop`	0	0	0	0		
	`nop`	0	0	0	0		
	`j loop`						
exit:							

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2.3.) Fill the values (in base 16 only) of any registers that effected by the following sequence. Note: initially `$t0 = 0x789ABCDE, $t1 = 0x89ABCDEF, $t2 = 0x0FEDCBA98`

(8 points)

Label	Mnemonic	$s0	$s1	$s2	Overflow (Yes/No)
begin:	**add $s0,$t1,$t0**				
	srl $s1,$t2,8				
	clo $s2,$t2				

2.4.) Translate the following C code to MIPS assembly code. Use a minimum number of instructions. Assume that the value a, b, and i are in register $s0, $s1, $t0, respectively. Also, assume that register $s2 holds the base address of the array D.

(10 points)

```
for (i = 0: i < 10: i++) {
     D[i] = a + b:
     a += 1;
}
```

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2.5.) Translate function funcA into MIPS assembly code using calling convention.

(10 points)

Note: a function funcA calls another function funcB. The function declaration for funcB is "int funcB(int a, int b)"

```
int funcA(int a, int b, int c) {
     return funcB(funcB(a,b),c)
}
```

3.] Please answer the following questions and show your work in details.

3.1.) Show the IEEE 754 binary representation of the number

$-2.46588869082304000000 \times 10^{148}$ in double precision: (answer in hex.) (3 points)

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3.2.) What decimal number is represented by this double precision float?

4	0	3	8	4	C	1	0

63 62 52 51 32

D	0	0	0	0	8	8	0

31 28 27 24 23 20 19 16 15 12 11 8 7 4 3 0

(2 points)

3.3.) Use Booth algorithm (4-bits) to calculate the product. (15 points)

(assume there are enough bits so no overflow ever occurs)

Iteration	Step (Booth algorithm: 4-bits)	Multiplicand	Product
X	Initial Values	XXXX XXXX	xxxx xxxx xxxx xxxxx
0	Initial Values (126:8 bits)x(-224: 9 bits)=	0111 1110	0000 0000 1001 00000 0

Product = ____________________ten

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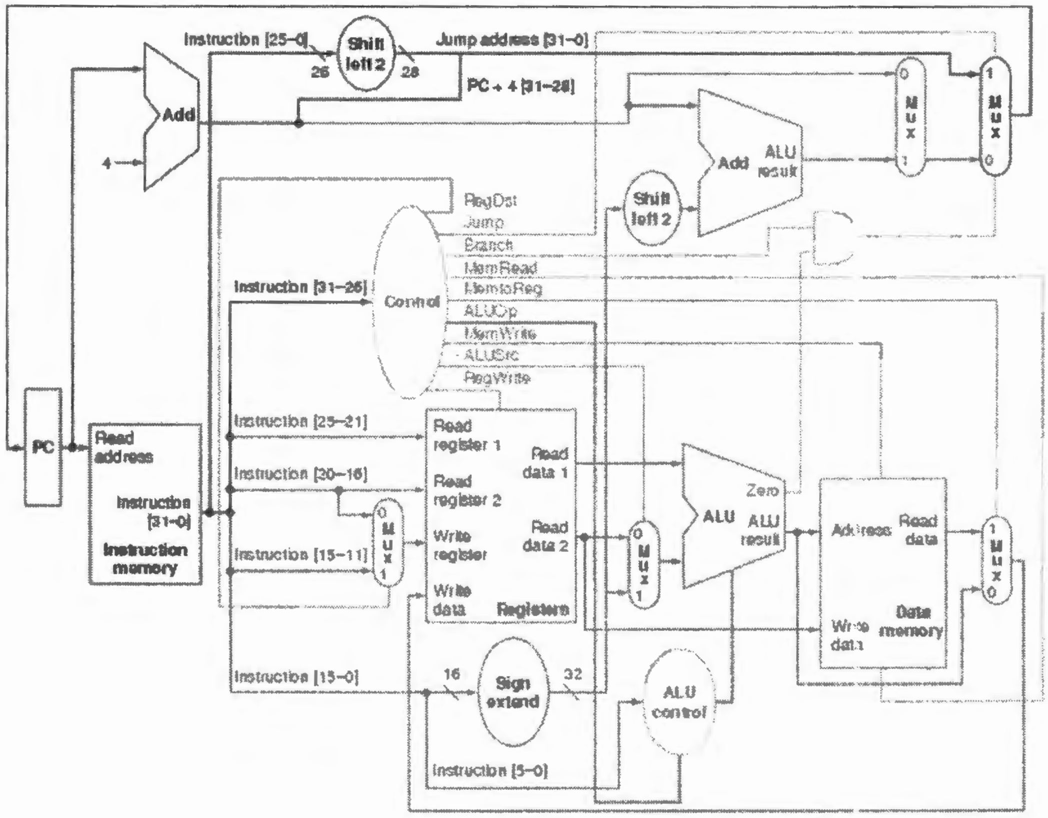
4.] Answer the following question in brief but accurate.

4.1.) From Datapath in figure 4.24 on page 329 (4th ed.), (if you can't clearly see the figure, look at the book or lecture note) (8 points)



4.1.1. Which is/are the instruction(s) that cause **MemtoReg** signal to reset to '0'?

(2 points)

4.1.2. Which is/are the instruction(s) that cause **ALUOp** signal to set to '0'?

(2 points)

4.1.3. How to modify this Datapath and control to execute jr(Jump Register) ? you may draw on the figure. (4 points)

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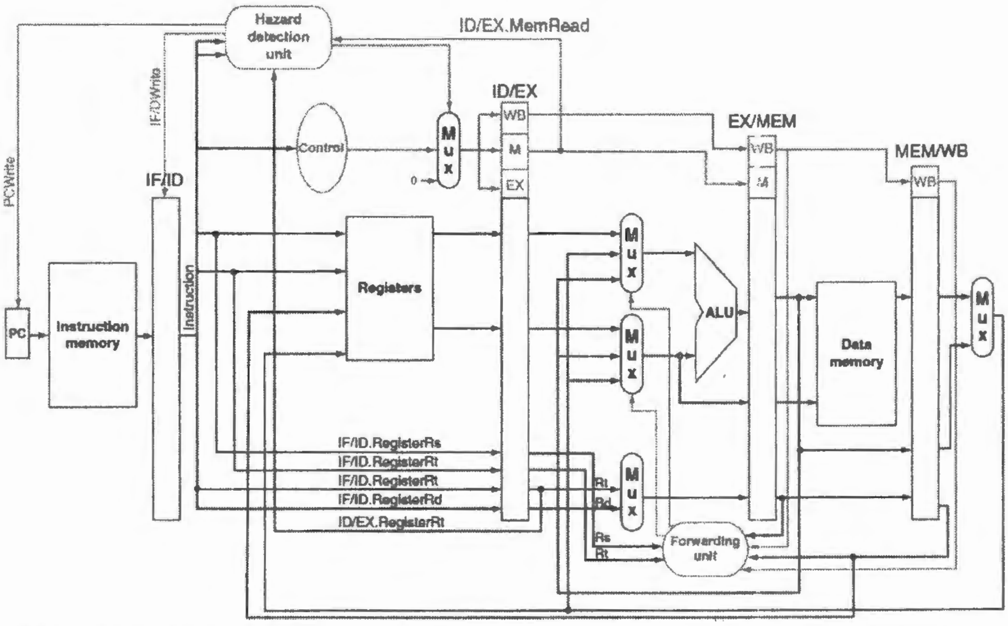
4.2.) With the following sequences of instructions, and assume that it is executed on a five-stage pipelined Datapath as in figure 4.60 on page 375 (4th ed.), (if you can't clearly see the figure, look at the book or lecture note): (15 points)




```
slt $11,$12,$13
lw $14,4($15)
or $17,$16,$11
sw $14,16($17)
and $14,$14,100
```

What is the values of control signal?

4.2.1. Clock cycle 3, ALU control input = _______ (1 points)

4.2.2. Clock cycle 3, ID/EX.RegDst = _______ (1 points)

4.2.3. Clock cycle 4, ALUop = _______ (1 points)

4.2.4. Clock cycle 4, ForwardB = _______ (1 points)

4.2.5. Clock cycle 4, ID/EX.MenRead = _______ (1 points)

4.2.6. Clock cycle 5, IF/ID. RegisterRs = _______ (1 points)

4.2.7. Clock cycle 5, ForwardA = _______ (1 points)

4.2.8. Clock cycle 6, MEM/WB.RegisterRd = _______ (1 points)

4.2.9. Clock cycle 6, EX/MEM.RegisterRd = _______ (1 points)

4.2.10. Clock cycle 7, ALU control input = _______ (2 points)

4.2.11. Clock cycle 7, ForwardA = _______ (2 points)

4.2.12. Clock cycle 8, ForwardB = _______ (2 points)