Seat No.:_____

King Mongkut's University of Technology Thonburi
Final Exam of Second Semester, Academic Year 2016

CPE 223 Digital System Design — CPE(Inter.) Students

Monday 8 May 2017 — 13.00-16.00

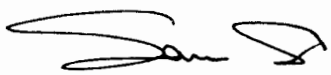
Instructions

1. This examination contains 7 problems, 8 pages (including this cover page), The total score is 40 points.
2. The answers must be written in the space provided.
3. **No calculator, book**, **note**, and **dictionary** allowed in the exam room.

Students must raise their hand to inform to the proctor upon their completion of the examination, to ask for permission to leave the examination room.
Students must not take the examination and the answers out of the examination room.

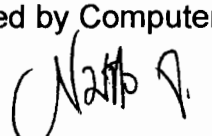
Students will be punished if they violate any examination rules. The highest punishment is dismissal.

This examination is prepared by



Asst. Prof. Sanan Srakaew
Tel. 0-2470-9083

This examination paper is approved by Computer Engineering Department.



Assoc. Prof. Dr. Natasha Dejdumrong
Head of Curriculum

Problem	1	2	3	4	5	6	7	Total
Points	4	5	3	6	6	6	10	40
Earned Points								

Student Name: _____ I.D.: _____

1. In Figure 1, a 4-to-1-line multiplexer circuit.

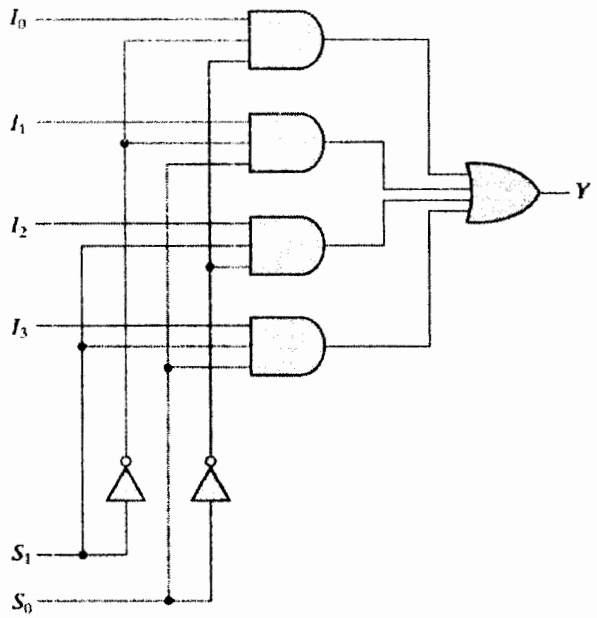


Figure 1: A 4-to-1-line multiplexer circuit.

(a) Write a Verilog module using gate-level design(structural Verilog) (2 points)

(b) Rewrite a Verilog module in (a) using behavioral model. (2 points)

2.

(a) Sketch a full adder circuit using AND, OR, and XOR gates. (1 point)

(b) Write a full adder gate-level Verilog module, namely **full_adder**. (2 points)

(c) Write a 4-bit full adder Verilog module, namely **adder_4bit**, using **full_adder**. (2 points)

3. Given a dataflow Verilog module below:

```
module fun(A,B,D, En);

        input A, B;
        output [3:0] D;
        input En;


        assign  D[0] = !((!A) && (!B) && (!En)),
                D[1] = !(!A) && B && (!En)),
                D[2] = !(A && (!B) && (!En)
                D[3] = !(A && B && (!En));
endmodule
```

Draw a NAND-gate-only circuit to represent the Verilog module above. (3 points)

4. Write a Verilog code to implement an 8-bit 4-to-1 multiplexer. (6 points)

module mux_4_to_1 (a, b, c, d, out, out_bar, sel);

input [7:0] _____

output _____

input [1:0] sel;

endmodule

5. Given a 4-bit binary ripple counter circuit using D flip-flops shown in Figure 2 below:

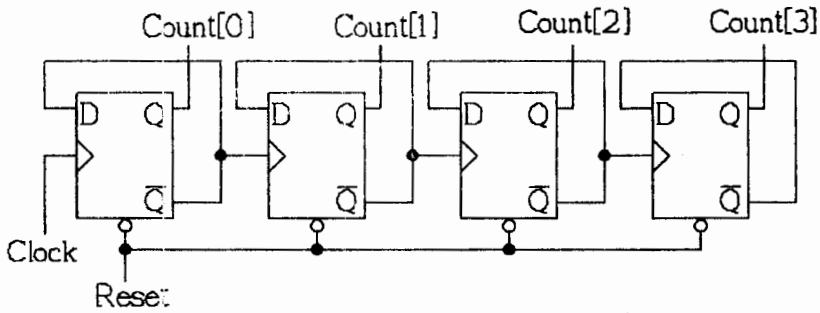


Figure 2: A 4-bit binary ripple counter using D flip-flops.

(a) Write a Verilog module of D flip-flop. (2 points)

```
module DFF (D, Clock, clear, q, qbar);
    input  D,Clock, clear;
    output reg q;
    output qbar;

endmodule
```

(b) Using DFF module above, write a Verilog module to implement the 4-bit binary ripple counter. (2 points)

(c) Rewrite the 4-bit binary ripple counter Verilog module using behavioral model. (2 points)

6. From a simple BCD counter given in Figure 3 below:

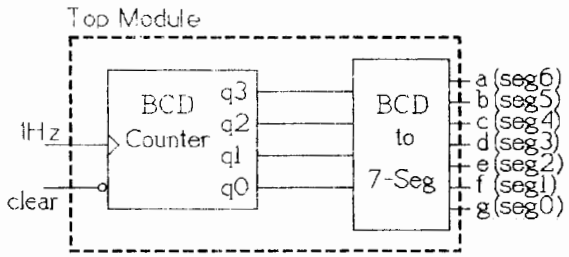


Figure 3. A simple BCD counter.

Write BCD counter and BCD to 7-segment Verilog behavioral modules. Assume the common anode 7-segment display is used. (6 points)

7. What is your Final project name? Draw a block diagram of the top module of your Final project. Pick one module in the top module and write a Verilog code for that module. (10 points)