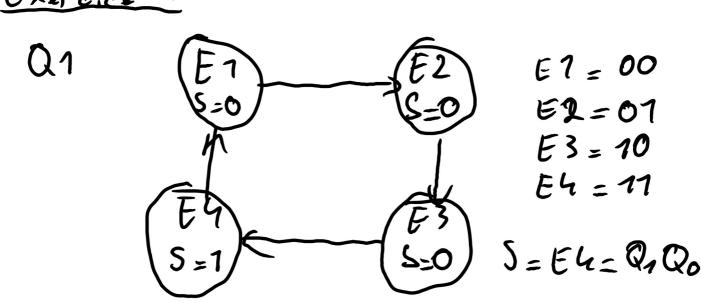
Architecture d'une FSN



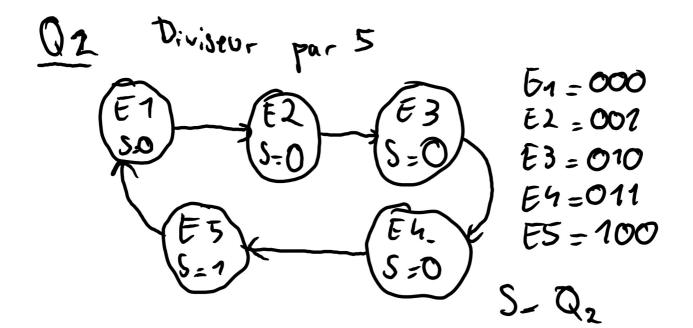
Nombre de bascule D nécessaire

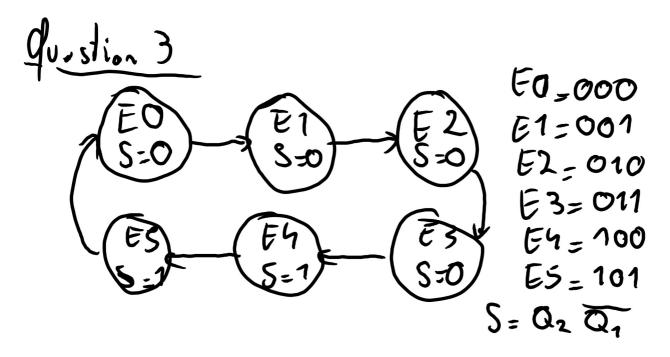
$$N_b = \frac{\ln(\text{etat})}{\ln(2)}$$

Exercice 1

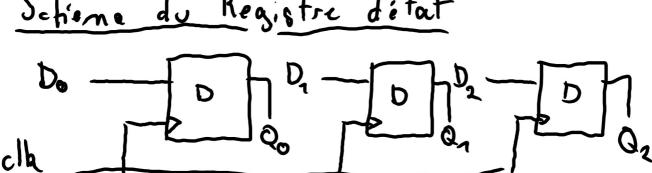


On convertit chaque état on nombre (ici 2 bits sufficent) Puis en fonction de l'état on calcul fa sorlie S





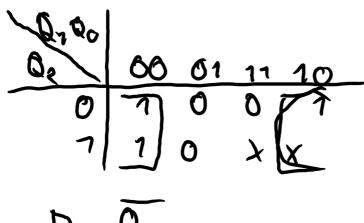
Overtion 4 Clear Asynctrone Les Indépendent de l'horloge Les force la sortie à 0 Schieme du Registre détat

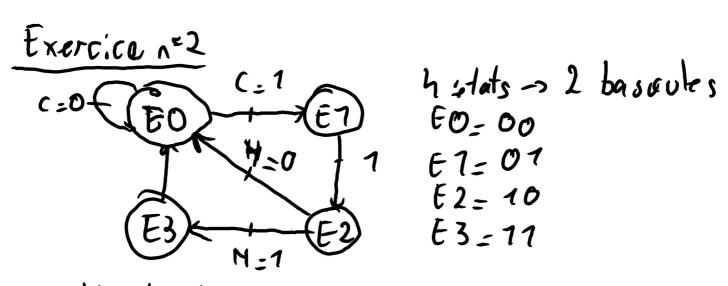


Schema du circuit Next State

Q	Q	O°	Ds	D	D_{o}	Reset
0	0	0	0	0	1	0
0	0	1	0	1	0	0
0	7	B	0	1	1/	0
0	1	1	1	0	0	0
1	0	O	1	0	1	Ò
7	O	1	1	1	0	Ó
7	7.	0	X	X	X	7
		,		7		

Marrivera Jamais donc don't care





	Eta	Loctuel	1 Ent	ries	Etat	suivent	LSortie
Ftat	Q,	Qo	C	M	Da	D _o	S
EO	0	0	0	X	0	0	6
FO	0	0	1	×	0	1	0
E1	0	1	X	X	7	B	clk
62	1	0	X	0	0	ð	clk
E2	1	0	×	1	7	0	clk
E3	1	7 1	\checkmark	X	0	0 1	clk