UNIVERSITÉ DE LIÈGE

[GBIO0029] BIOELECTRONICS

Electrocardiogram (ECG) Monitor Design

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Contents

1 Introduction

In our bodies, electrical pulses are used by the nervous system to carry information from one cell to another and to stimulate cells into performing an action. An example of this is the sino-atrial(SA) node in our hearts. This region periodically generates action potentials that trigger the heart muscles' contraction. By measuring the electrical activity of the heart we can monitor the cardiac health of a patient.

Electrocardiograms(ECGs) are systems that are made to measure and process the electrical activity of the heart. The signal is acquired through electrodes placed on the body. In this report, we will explain the design and the choices that were made in order to build a custom ECG monitor. To motivate our choices, both simulations and experimental data from our final build will be presented.

2 System requirements

In order to measure the electrical activity of a heart, several factors had to be taken into account. First, is the signal acquisition method. In this project, we were provided electrodes to make a 3-lead ECG.

The second is the normal activity of the human heart. At rest, a human heart rate is typically between 40 and 100 beats per minute(bpm). However, higher frequencies are required to accurately capture the different characteristic parts of an ECG complex. It has been shown [1] that the frequency content of the ECG lies between 0.05 Hz to at least 330 Hz. Higher frequencies are useful up to 700Hz to capture cardiac abnormalities.

The last requirement is to have a qualitatively clear signal. The magnitude of the acquired signal compared to the noise is important. The signal that will be recorded will be of the order of $10^{-}3$V in a noisy environment. The prevalent noise frequency that needs to be eliminated is due to the electrical distribution system that surrounds us. This noise is stable and around 50Hz.

3 Simulated circuit schematics

In order to design the circuit and perform simulations, LTspice was used. The simulated circuit schematic can be found in figure 1. As can be seen in the LTspice schematic, several sources of noise along with the models of the electrodes were used in order to get realistic simulations. These simulations were used as the first test to verify the correct fulfillment of the afford mentioned system's requirements

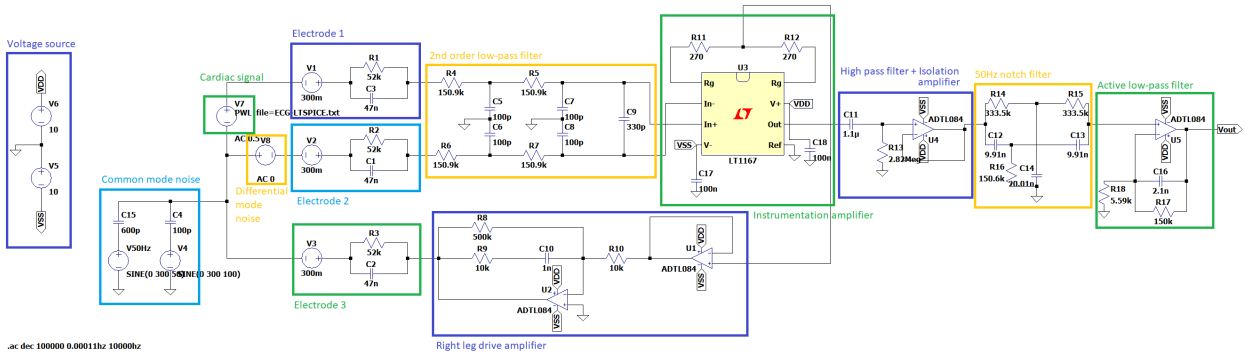


Figure 1: ECG schematic

4 Modules

The circuit can be divided into modules as shown in figure 1. These modules are centered around the instrumentation amplifier whose goal is to amplify the voltage difference created by the heart's electrical activity. The first stages of the circuit consist of the acquisition through the electrodes and a first denoising phase through a low pass filter. Also, a Driven Right Leg (DRL) compensator is used to sense, invert, and amplify the common mode noise captured by the body. This voltage is then applied to the patient through the third electrode to compensate for the voltage induced by the noise. The last stages of the circuit are a set of filters to further reduce noise and amplify the signal to improve the readability of the signal at the output.

4.1 Low-pass filter

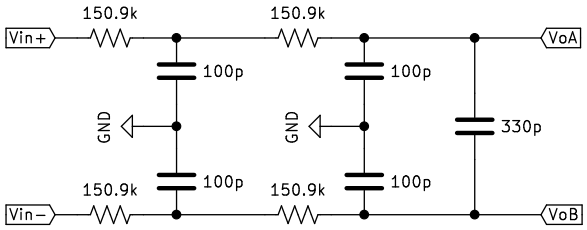


Figure 2: Second order low-pass filter schematic.

As the first step, it was decided to use a second-order low-pass filter on the acquired signal to reduce noise before amplification. The filter design can be seen in figure 2. It is composed of 2 vertically symmetric low-pass filters in series to filter the common-mode signal. The last capacitor on the right does not affect the common mode signal. Therefore, when added to the two previous filters it acts as a low-pass filter for the differential mode component of the signal. As a result, we get two different cut-off frequencies. One for the common mode signal by taking only the two first filters into account, and one for the differential mode by taking also the last capacitor into account.

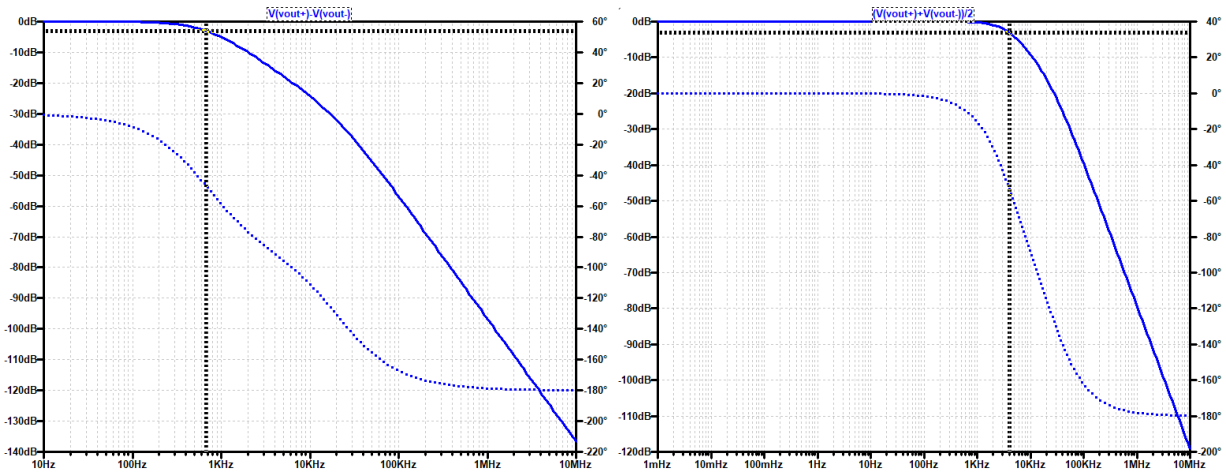
$$f_C = \frac{1}{2\pi\sqrt{R_1 C_1 R_2 C_2}} \tag{1}$$

$$f_{(-3\text{ dB})} = f_C\sqrt{2^{\left(\frac{1}{n}\right)} - 1} \tag{2}$$

The cutoff frequency of a low pass filter is given in equation 1. By replacing $R_1 = R_2 = 150.9k$ and $C_1 = C_2 = 100p$ in the equation we get the common mode cutoff frequency at $f_c = 10.55kHz$. However, cascading filters have an effect on each other that further reduce the cut-off frequency. To compensate for this we use equation 2 with f_c the previously computed cutoff frequency and $n = 2$ the order of the filter to get a more realistic cutoff frequency $f_{(-3\text{ dB})} = 6.78kHz$.

For the differential mode filter, we apply the same process but replace with $R_1 = R_2 = 150.9k$, $C_1 = 100p$, and $C_2 = 100p + 330p = 430p$ to get $f_c = 5.08kHz$ and $f_{(-3\text{ dB})} = 3.27kHz$.

Figure 3 shows the LT spice simulation of the bode plots of the second-order filter. These simulations show that the calculation for the common mode filter was accurate. However, we can see that the used equation was not accurate in the differential mode case and failed to capture the coupled dynamics of the two stages. The simulated cutoff frequency for the differential mode is close to $700Hz$ which is acceptable for our application as it is at the top of the frequency range of interest.



(a) Differential mode noise bode plot.

(b) Common mode noise bode plot.

Figure 3: Bode plots of the used passive second-order low-pass filter to reduce noise before amplification.The cursor is placed at the -3db point.

4.2 Instrumentation amplifier (INA128)

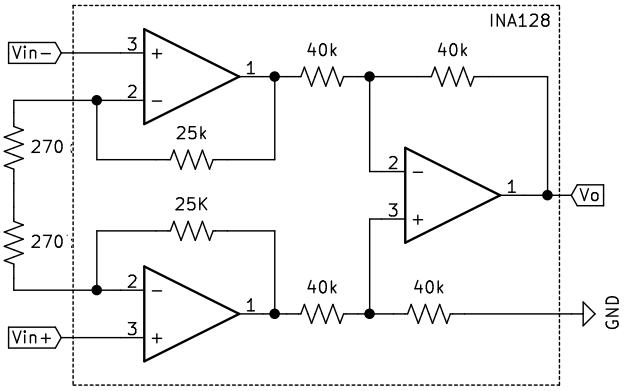


Figure 4: Intrumentation amplifier schematic.

The amplification of the weak ECG signal is made possible by an INA128 instrumentation amplifier. This type of amplifier has a variety of characteristics that make it highly suitable for this task. Starting with a gain that is tunable through a resistor as shown in equation 3. The gain can therefore set to be high by using a low resistor. Then, thanks to the differential amplifier stage, instrumentation amplifiers have a very high common-mode rejection ratio. This is highly desirable as common-mode noise is the main noise present in the ECG signal. Finally, it has a high input impedance and low output impedance that reduces the effects of measurement on the signal.

$$A = 1 + \frac{50k\Omega}{R_G} \tag{3}$$

For our simulation, the LTspice equivalent(LT1167) of the INA128 was used as the latter is not available. The differences between the two components' gain formulas are negligible.

By using a resistor of 540Ω for the R_G resistor our gain is therefore 93.5. This amplification ratio was chosen as a compromise between wanting to amplify the signal (higher is better) and not wanting to amplify the noise(lower is better). For example, amplifying the 50Hz noise that is highly present in the body is not desired as the goal is to suppress it.

R_G is divided into two 270Ω resistors in order to have the common-mode noise voltage on the body at the junction between the two resistors. This voltage is then used as the input of the RLD compensator module.

4.3 Right Leg Drive (RLD) Compensator

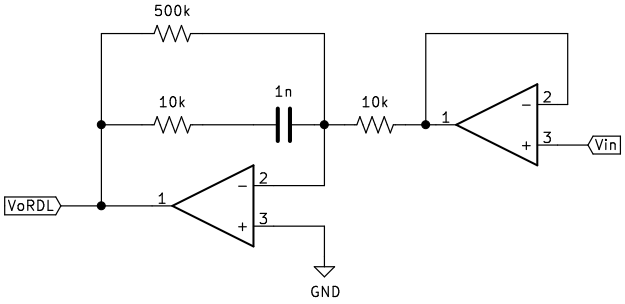


Figure 5: Right leg drive compensator schematic.

The Driven Right Leg (DRL) compensator circuit shown in figure 5 is in essence an inverting amplifier. By giving the common mode voltage at its input as stated in the previous section, the goal is to invert and amplify the noise. Then, the inverted noise is sent to the body of the patient through the right leg electrode to cancel the common mode noise.

However, as this is a feedback system with the body and the previous parts of the circuit being the plant and the DRL being the controller, there has to be a concern with the stability of the system. Indeed, the gain of an inverting operational amplifier is given by $A_v = -\frac{R_{in}}{R_f}$, with the input resistance $R_{in} = 10k$ in our case, and the feedback resistance R_f being an impedance given by the parallel branch. The gain of the amplifier cannot be too high or it would make the system unstable and introduce more noise than it cancels, but if it is too small, it would have no effect on the noise. The parallel branch that can be seen in the DRL is designed to obtain a good compromise. We can have a high gain at low frequencies where it is the most important and lower the gain at high frequencies to attain stability.

To verify stability, the bode plot of the open loop gain for our DRL system was simulated in LTspice. As it can be seen in figure 6, the open loop gain has a positive phase margin of 86°. The system is therefore stable and has a high gain of $A_v = -\frac{500k}{10k} = 50$ for low frequencies. At higher frequencies, the gain drops to $A_v = -\frac{10k}{10k} = 1$.

Finally, the unit gain amplifier at the input of the DRL is used to reduce the current driven by the amplifiers in the instrumentation amplifier as these currents can be considerable if R_G is small as it is in our case.

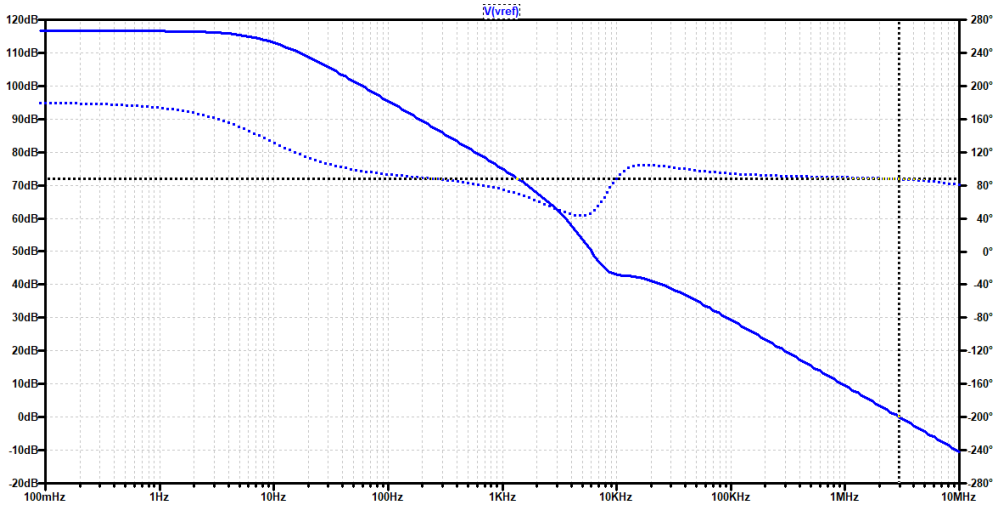
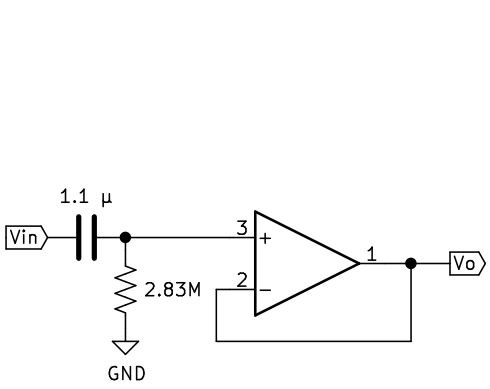
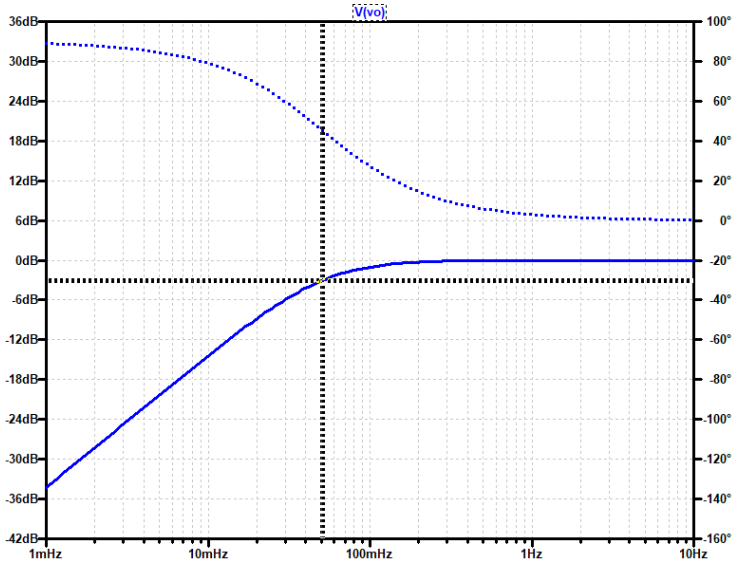


Figure 6: Right leg drive compensator open loop gain bode plot.

4.4 High-pass filter



(a) High-pass filter and isolation amplifier schematic.

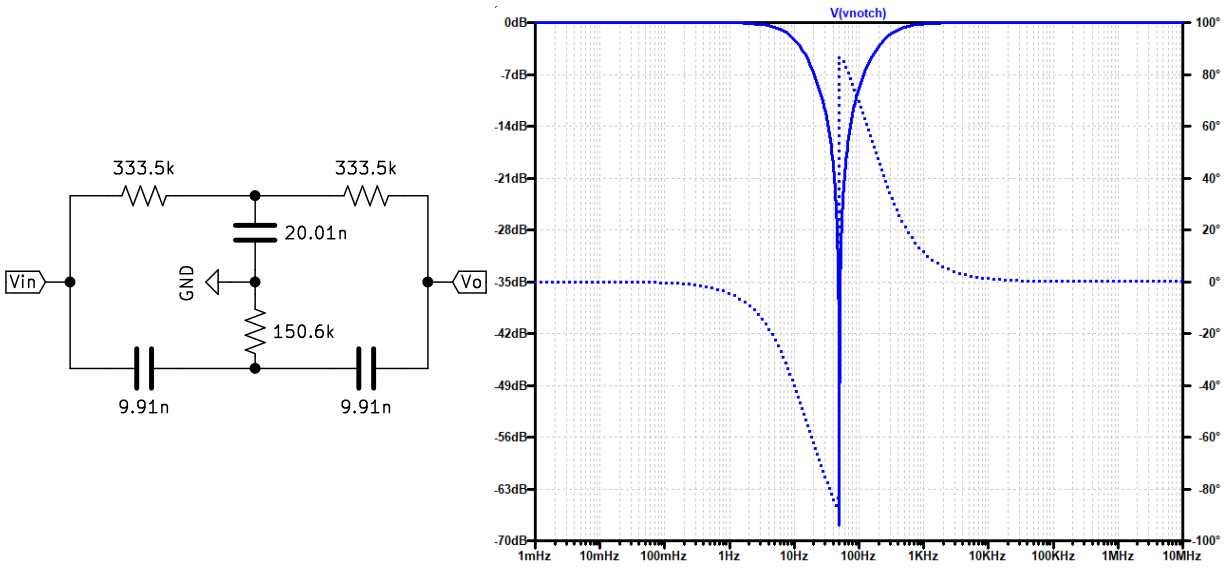


(b) High-pass filter bode plot. The cursor is placed at the -3db point.

Figure 7: High-pass filter schematic and its simulated bode plot.

In order to remove the DC component at the output of our circuit, we used a passive first-order high-pass filter. The cutoff frequency had to be small in order to not attenuate useful frequency components of the signal. Using a 1.1µ F capacitor and $2.82M\Omega$ resistor as shown in figure 7 obtained a cut-off frequency at $f_c = 0.051Hz$. Which is at the lower limit of the useful frequency components described in section 2.

4.5 Notch filter



(a) Notch filter schematic

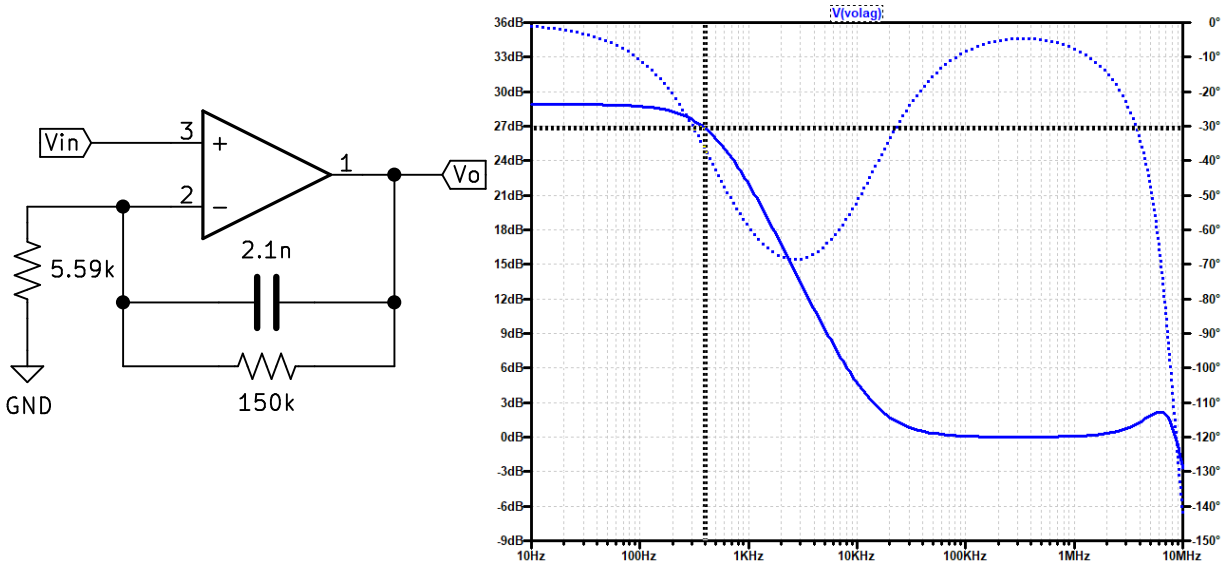
(b) Notch filter bode plot.

Figure 8: Notch filter schematic and its simulated bode plot showing the notch close to 50Hz.

In order to suppress the main component of the noise at 50Hz, the notch filter shown in fire 8a was designed. The center frequency of this filter can be obtained from the following equation: $f_N = \frac{1}{4RC} = 48.15Hz$. This frequency is close to 50Hz, and in tests, it successfully suppressed the 50Hz component of the noise. Figure 8b shows the shape of the simulated bode plot of the notch filter and its center frequency close to 50Hz.

The main challenge of this filter is its sensitivity to mismatched components. Indeed, it was necessary to take care and measure each of the components to be able to get the closest possible values. Otherwise, the shape and center frequency of the notch would have been greatly affected.

4.6 Lag compensator



(a) Lag compensator schematic

(b) Lag compensator bode plot. The cursor is placed at the -3db point.

Figure 9: Notch filter schematic and its simulated bode plot showing the notch close to 50Hz.

Figure 9a shows the schematic of the last filter used in the ECG circuit. It is a lag compensator. This last stage was used to obtain one last amplification before the signal is output to be read at the oscilloscope. In addition, it is also an active low-pass filter. It amplifies the bandwidth we are interested in and reduces the gain after its cutoff frequency. The feedback branch of this non-inverting amplifier is a simple low-pass filter. Therefore, we can use equation 1 again to compute its cutoff frequency. The obtained cutoff frequency is $f_c = 505.3Hz$. Figure 9b shows the simulated bode plot to confirm our calculations.

With this cutoff frequency, we do attenuate some of the frequency range of interest as the range goes up to 700Hz. However, it will later be shown in the results section that this attenuation did not have a severe impact on the shape of the ECG signal in practice.

At frequencies below the cutoff, the gain of the active filter was tuned using the non-inverting amplifier equation 4. A final amplification of 27.8 was found to be sufficient experimentally and yield an output signal at the volt scale that is easy to read at the oscilloscope.

$$A_v = 1 + \frac{R_{17}}{R_{18}} = 1 + \frac{150k}{5.6k} = 27.8 \tag{4}$$

5 Results

The simulated bode plot of the full electrocardiogram circuit is shown in figure 10. There are 3 distinctive elements that characterize this plot. The first element is the low-frequency cutoff created by the high pass filter at 0.05Hz. Then, at 50Hz we can appreciate the notch filter attenuating the frequencies close to 50Hz as desired. Finally, the second cutoff for high frequencies is close to 1Khz. We can therefore conclude that the initially required frequency range of [0.05Hz 700Hz] was respected in the design of the circuit.

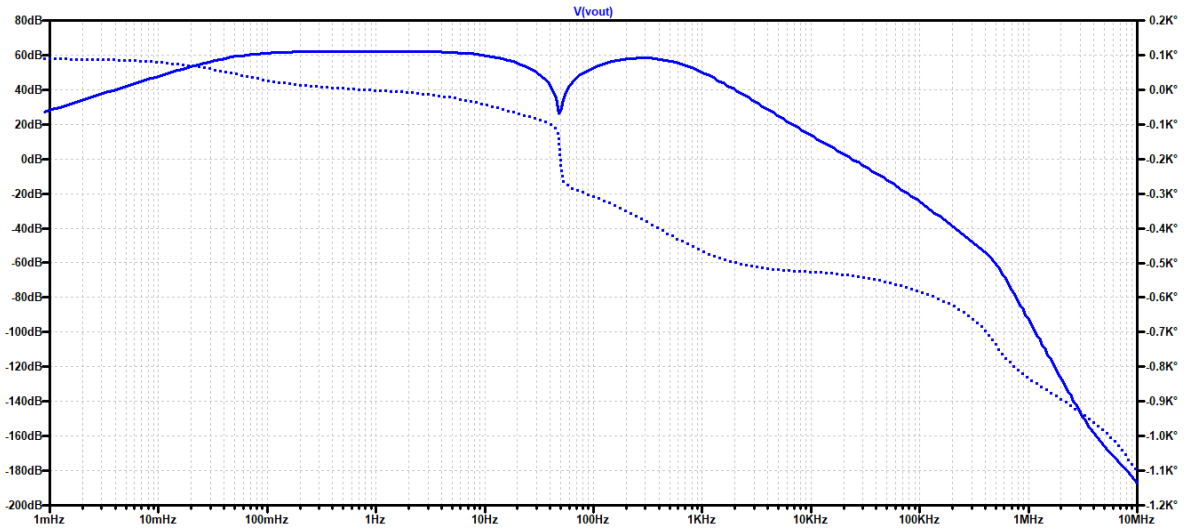


Figure 10: Simulated bode plot of the full electrocardiogram circuit

The bode plot was also plotted experimentally in order to obtain a more realistic plot. With an experimental plot, parasitic capacitances and inductances that were not modeled in the LTspice simulation would also be taken into account. The bode plot shown in figure 11 is very similar for the plotted range to its simulated counterpart. However, its high-frequency cutoff seems to be higher than the calculated cutoff which is unexpected but beneficial as it preserves more of the frequency range of interest.

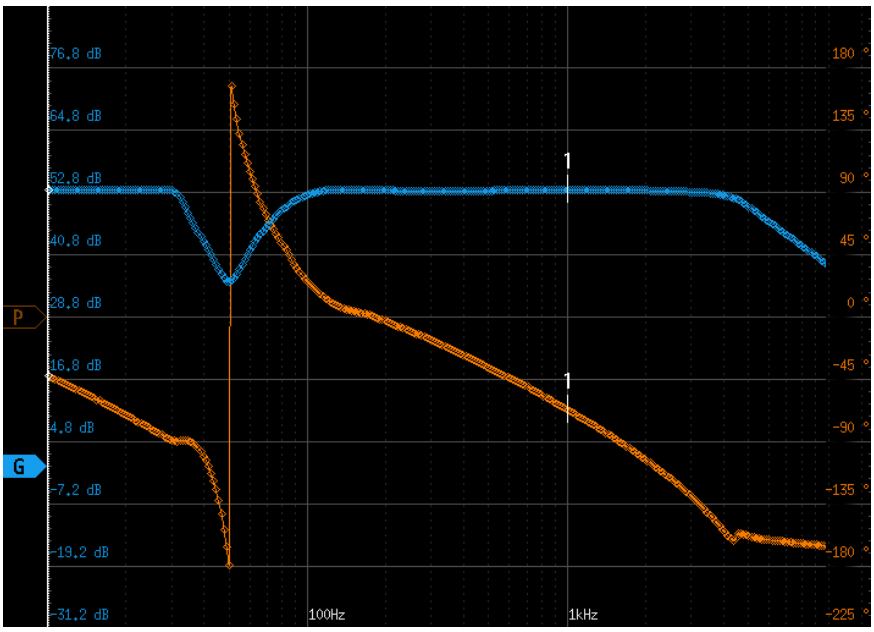


Figure 11: Experimental bode plot of the full electrocardiogram circuit

The circuit was also tested on one of the members of the group and figure 12 shows the obtained electrocardiogram. Every expected component of the ECG signal can be easily identified in the signal as shown in the figure. We can see the small P wave, the QRS complex, and finally the small T wave.

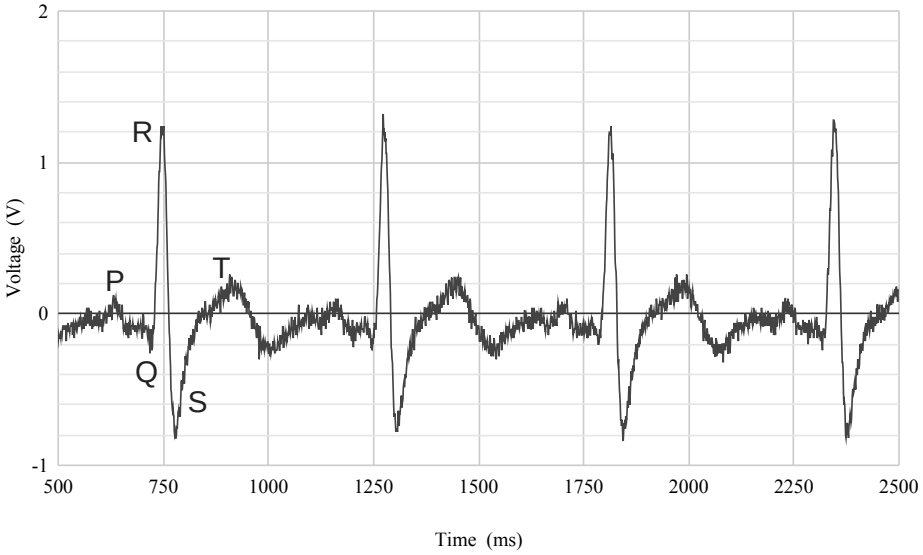


Figure 12: Recorded ECG signal with annotations of the different parts of an ECG signal

6 Circuit Assembly

The final circuit is shown in figure 13. The circuit was assembled on a breadboard to facilitate the testing of different components. However, on breadboards, circuits are prone to have higher parasitic capacitors between tracks. There are higher resistances in the circuit due to contact resistances and they are also prone to contact errors. Fortunately, the results obtained seem not to be subject to such issues.

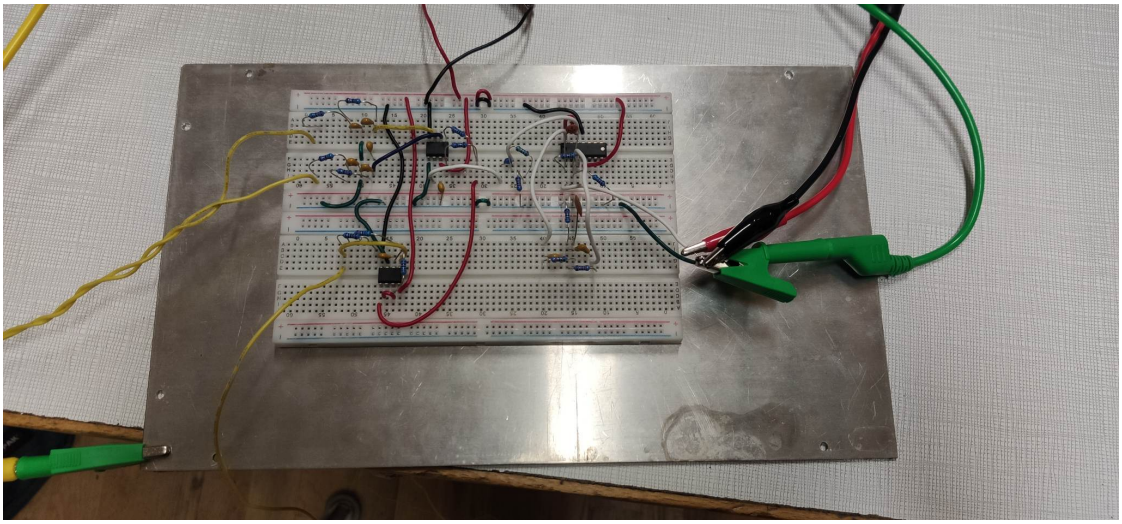
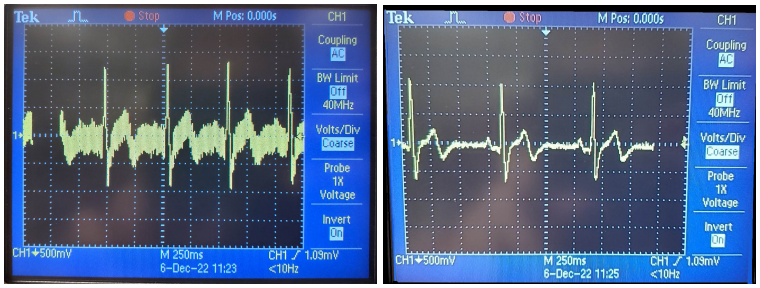


Figure 13: Picture of the built circuit with the grounded plate used as electromagnetic shielding.

6.1 Shielding

After building the circuit and testing every module we found that everything was functional and working as expected. However, during testing, it was found that noise at 50Hz was still present at the output despite

the notch filter. This was due to a 220V power line running too close to the circuit. To solve this issue, a grounded metal plate was used as shown in figure 13. Placing the metal plate between the main noise source an,d the circuit shields it from induced currents and considerably reduces the noise in the circuit as can be seen in figure 14.



(a) Without shielding (b) With shielding

Figure 14: Recorded ECG signals that show the noise reducing the effect of our shielding method

7 Improvements

Our Electrocardiogram already shows good results. However, 3 main steps could be taken to further improve the circuit and the quality of the obtained signal:

- Build the circuit on PCB to improve robustness and reduce parasitic effects.
- Using shielded cables for the leads to reduce noise;
- Using smaller tolerance components to design the circuits more finely.

8 Conclusion

Throughout this report, we have explained our design process and motivated the decisions it involved. The final circuit can be decomposed sequentially into a low-pass filter, an instrumentation amplifier, a high-pass filter, a notch filter, and an active low-pass filter. An RDL compensator was also used to reduce common mode noise. The open loop gain bode plot showed an 80° frequency margin and high gain at low frequencies which indicates that the designed RDL is stable and rejects noise effectively.

To motivate those decisions, calculations supported by simulations were given. The final bode plot of the system shows that we keep and amplify the frequencies within the [0.05Hz 700Hz] range of interest and suppress the other frequencies.

We have shown the built and functional ECG. The circuit is built on a breadboard and a grounded metal plate is used as shielding to reduce noise.

Furthermore, we proposed areas where improvements could be made to the circuit. These improvements mainly concern the circuit build quality and the quality of the used components.

Finally, the obtained experimental results support our frequency domain simulations. In the temporal domain, experiments show a clear output signal where the characteristic PQRST pattern of a heartbeat can be easily distinguished. These results indicate that we successfully fulfilled the purpose of this project by designing a working 3-lead ECG.

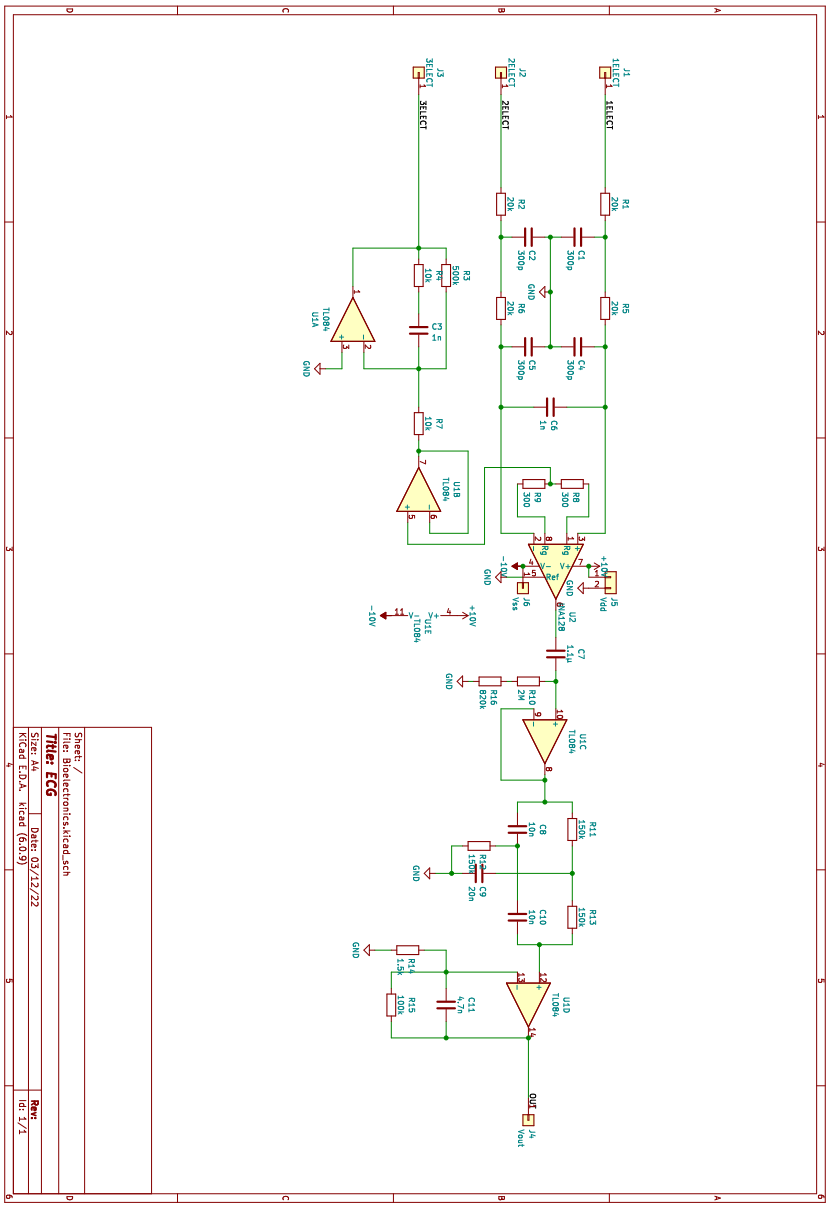


Figure 15: Kicad schematic of the circuit

References

[1] Josephson ME Tereshchenko LG. Frequency content and characteristics of ventricular conduction. 2015.