| Instruction streams that are present in instruction generator to generate different kinds of instructions | | | | | | | |
|---|---|---|---|---|---|---|---|
| S No. | Streams | Description | Status of using | Error from assembler that it is generating illegal instructions | Stream working fine with floating point instrunctions enabled | | |
| 1 | riscv_rand_instr_stream | Generate a random instruction stream | x | | ✅ | | |
| 2 | riscv_directed_instr_stream | Base class for directed instruction stream | x | | | | |
| 3 | riscv_mem_access_stream | Base class for memory access stream | x | | | | |
| 4 | riscv_jump_instr | Jump instruction (JAL, JALR)<br>For JAL, restore the stack before doing the jump | x | | | | |
| 5 | riscv_jal_instr | Stress back to back jump instruction | ✅ | | | | |
| 6 | riscv_push_stack_instr | Push stack instruction stream | x | | | | |
| 7 | riscv_pop_stack_instr | Pop stack instruction stream | x | | | | |
| 8 | riscv_int_numeric_corner_stream | Stress the numeric corner cases of integer arithmetic operations | x | | | | |
| 9 | riscv_load_store_base_instr_stream | All load/store instruction stream | x | | | | |
| 10 | riscv_single_load_store_instr_stream | A single load/store instruction | x | | ✅ | | |
| 11 | riscv_load_store_stress_instr_stream | Back to back load/store instructions | x | | ✅ | | |
| 12 | riscv_load_store_shared_mem_stream | Back to back load/store instructions | | | x | | |
| 13 | riscv_load_store_rand_instr_stream | A random mix of load/store instructions and other instructions | ✅ | Yes | x | | |
| 14 | riscv_hazard_instr_stream | Use a small set of GPR to create various WAW, RAW, WAR hazard scenario | x | | | | |
| 15 | riscv_load_store_hazard_instr_stream | This instruction stream focus more on hazard handling of load store unit. | ✅ | | | | |
| 16 | riscv_multi_page_load_store_instr_stream | Back to back access to multiple data pages<br>This is useful to test data TLB switch and replacement | ✅ | Yes | | | |
| 17 | riscv_mem_region_stress_test | Access the different locations of the same memory regions | ✅ | On some seed | | | |
| 18 | riscv_load_store_rand_addr_instr_stream | Random load/store sequence to full address range | ✅ | | | | |
| 19 | riscv_amo_base_instr_stream | AMO instruction stream | x | | | | Will not use |
| 20 | riscv_lr_sc_instr_stream | A pair of LR/SC instruction | x | | | | Will not use |
| 21 | riscv_amo_instr_stream | | ✅ | | | | Will not use |
| 22 | riscv_vector_amo_instr_stream | | ✅ | | | | Will not use |