Note: This sheet contain the important signals in different stages of Azadi Core

	STAGE	IMPORTANT SIGNALS
Important signals in Azadi core	**INTRUCTION FETCH**	clk_i rst_ni rdata_q[2:0] instr_addr_o[31:0] instr_rdata_i[31:0] instr_rdata_alu_id_o[31:0] instr_rdata_c_id_o[15:0] instr_rdata_id_o[31:0]
	DECOD	instr_rdata_alu_i[31:0] alu_op_a_mux_sel_o[1:0] alu_op_b_mux_sel_o alu_operand_a_ex_o[31:0] alu_operand_b_ex_o[31:0] alu_operator_ex_o[5:0] rf_waddr_id_o[4:0] rf_wdata_id_o[31:0] instr_valid_i ex_valid_i
	DECOD MUL/DIV	multdiv_operand_a_ex_o[31:0] multdiv_operand_b_ex_o[31:0] multdiv_operator_ex_o[1:0] div_en_ex_o div_sel_ex_o mult_en_ex_o mult_sel_ex_o multdiv_ready_id_o instr_valid_i ex_valid_i multdiv_signed_mode_ex_o[1:0]
	DECOD FPU OUT	other dec_o fpu signals fp_src_fmt_o[2:0] fp_rounding_mode_o[2:0] fp_rf_wdata_id_o[31:0] fp_rf_waddr_o[4:0] fp_rf_raddr_c_o[4:0] fp_rf_raddr_b_o[4:0] fp_rf_raddr_a_o[4:0] fp_operands_o[2:0] fp_alu_operator_o[3:0] fp_alu_op_mod_o
	EXE ADD	operand_a_i[31:0] operand_b_i[31:0] operator_i[5:0] alu_adder_result_ex_o[31:0] ex_valid_o
	EXE MULT DIV	clk_i rst_ni ex_valid_o multdiv_valid mult_en_i mult_sel_i div_en_i div_sel_i multdiv_operand_a_i[31:0] multdiv_operand_b_i[31:0] multdiv_operator_i[1:0] multdiv_result[31:0] multdiv_operator[1:0] waddr_a_i[4:0] multdiv_signed_mode_i[1:0] multdiv_operator_i[1:0]
	RF	rf_reg_q[31:1]
	FPU RF	rf_reg_q[31:0]
	FPU TOP	clk_i rst_ni result_o[31:0] operands_i[2:0] out_valid_o busy_o in_valid_i

	LOAD STORE	clk_i
		data_addr_o[31:0]
		// STORE
		data_we_o
		data_be_o[3:0]
		data_wdata_o[31:0]
		data_gnt_i
		// LOAD
		data_rvalid_i
		data_rdata_i[31:0]
		data_err_i