8.1.8 Size Field

This field specifies the size of the operation. The encoding is as follows:

00 — Byte Operation

01 — Word Operation

10 — Long Operation

8.1.9 Opmode Field

Refer to the applicable instruction descriptions for the encoding of this field in **Section 4 Integer Instructions**, **Section 5 Floating Point Instructions**, **Section 6 Supervisor (Privaleged) Instructions**, and **Section 7 CPU32 Instructions**.

8.1.10 Address/Data Field

This field specifies the type of general register. The encoding is:

0 — Data Register

1 — Address Register

8.2 OPERATION CODE MAP

Table 8-2 lists the encoding for bits 15 – 12 and the operation performed.

Table 8-2. Operation Code Map

Bits 15 – 12 Operation

Bits 15 – 12	Operation
0000	Bit Manipulation/MOVEP/Immed iate
0001	Move Byte
0010	Move Long
0011	Move Word
0100	Miscellaneous
0101	ADDQ/SUBQ/Scc/DBcc/TRAPc c
0110	Bcc/BSR/BRA
0111	MOVEQ
1000	OR/DIV/SBCD
1001	SUB/SUBX
1010	(Unassigned, Reserved)
1011	CMP/EOR
1100	AND/MUL/ABCD/EXG
1101	ADD/ADDX
1110	Shift/Rotate/Bit Field
1111	Coprocessor Interface/MC68040 and CPU32 Extensions

ORI to CCR

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0
0	0	0	0	0	0	0	0				3-BIT BY	TE DATA	4	-	

ORI to SR

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ſ	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0
							10	6-BIT W	ORD DA	ΓA						

ORI

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		0	0	0	_	0	0	91	ZE	EFFECTIVE ADDRESS MODE REGIS				SS	
"	"	0	"	"	"	"	"	31.	ZE					R	
	·	10	6-BIT W	ORD DA	ΓA						8-BIT BY	TE DATA	A		
						3	2-BIT LC	NG DAT	ГА						

ANDI to CCR

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	0	0	0	1	1	1	1	0	0
0	0	0	0	0	0	0	0				8-BIT BY	TE DATA	4	-	

ANDI to SR

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	0	0	1	1	1	1	1	0	0
						16	6-BIT W	ORD DA	ΤA						

ANDI

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	_	0	_	_	_	GI.	SIZE EFFECTIVE ADDRESS MODE REGISTER						
"	0	0	"	U	"	"	"	31.	<u> </u>		MODE		R	EGISTE	:R
	•	10	6-BIT WO	ORD DAT	ΓA					:	3-BIT BY	TE DATA	Ä		
						3	2-BIT LC	NG DAT	Ā						

Instruction Format Summary

SUBI

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	0	SI	75	EFFECTIVE ADDRESS MODE REGISTER					
"	"	"	"	"	!	"	"	31,	4 L					R	
	•	16	6-BIT WO	ORD DA	ΓA	•	•				3-BIT BY	TE DATA	4		
						3	2-BIT LC	NG DAT	A						

RTM

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ſ	0	0	0	0	0	1	1	0	1	1	0	0	D/A	R	EGISTE	₹

CALLM

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	0	0	0	-1	1	0	1	1		EFF	ECTIVE	ADDRE	ESS	
"	"	"	0	"	'	'	"	'	'	EFFECTIVE ADDRESS MODE REGISTER				R	
0	0	0	0	0	0	0	0			Α	RGUMEN	IT COU	NT		

ADDI

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	0	0	0	1	1	0	Q1	ZE	EFFECTIVE ADDRESS MODE REGISTER					
			0	U	'	'	U	31.	Z L						
	•	16	6-BIT WO	ORD DAT	ΓA	•					8-BIT BY	TE DATA	4		
						3	2-BIT LC	NG DAT	Ā						

CMP2

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ſ	0	0	0	0	0	SI	ZE	0	1	1		EFI	FECTIVE	ADDRE	SS	
	U	"	"	"	"	31	ZL.	"	'	'		MODE		R	EGISTE	R
	D/A	R	EGISTE	R	0	0	0	0	0	0	0	0	0	0	0	0

CHK2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	QI	ZE	0	1	1		EFI	FECTIVE	ADDRE	SS	
U					31		0	'	'		MODE		R	EGISTE	R
D/A	R	EGISTE	R	1	0	0	0	0	0	0	0	0	0	0	0

EORI to CCR

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	0	1	0	0	0	1	1	1	1	0	0
0	0	0	0	0	0	0	0			B,	YTE DAT	A (8 BIT	S)	-	

EORI to SR

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	0	1	0	0	1	1	1	1	1	0	0
						16	6-BIT W	ORD DA	ГА	•		•	•	•	

EORI

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	_	0	_	1	_	1	0	QI	ZE		EFF	ECTIVE	ADDRE	SS	
"	"	0	"	'	"	'	"	31.	ZL		MODE		R	EGISTE	R
		16	6-BIT WO	ORD DA	ΓA	•	•			1	6-BIT BY	TE DAT	A		
						3	2-BIT LC	NG DAT	ΓΑ						

CMPI

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	1	0	0	SI	70		EFF	ECTIVE	ADDRE	ESS	
	"	"	"	'	'	0	0	31.	<u> </u>		MODE		R	REGISTE	R
	•	16	6-BIT WO	ORD DAT	ГА					-	3-BIT BY	TE DATA	Ä		
						3	2-BIT LC	NG DAT	A						

BTST

BIT NUMBER STATIC, SPECIFIED AS IMMEDIATE DATA

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	_	0		1		_	0	_	0		EFF	ECTIVE	ADDRE	ESS	
U	"	"	"	'	"	"	U	"			MODE		F	REGISTE	:R
0	0	0	0	0	0	0	0				BIT NU	MBER			

BCHG

BIT NUMBER STATIC, SPECIFIED AS IMMEDIATE DATA

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	_	0		1		_	0	_	1		EFF	ECTIVE	ADDRE	ESS	
U	"	"	"	'	"	"	U	"	'		MODE		F	REGISTE	:R
0	0	0	0	0	0	0	0				BIT NU	IMBER			

BCLR

BIT NUMBER STATIC, SPECIFIED AS IMMEDIATE DATA

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	0	_	_	1	_	_	_	1	0		EFF	ECTIVE	ADDRE	SS	
	U	0	"	"	'	"	"	"	'	0		MODE		R	EGISTE	R
Ī	0	0	0	0	0	0	0	0				BIT NU	MBER			

BSET

BIT NUMBER STATIC, SPECIFIED AS IMMEDIATE DATA

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	0		0	4	4		EFF	ECTIVE	ADDRE	SS	
"	0	U	U	'	U	"	U	'	'		MODE		R	EGISTE	R
0	0	0	0	0	0	0	BIT NUMBER								

MOVES

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	1	1	0	QI.	ZE	EFFECTIVE ADDRESS					
U				'	'	'	U	OI.	4		MODE		R	EGISTE	R
A/D	R	EGISTE	R	dr	0	0	0	0	0	0	0	0	0	0	0

CAS₂

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	SI	ZE	0	1	1	1	1	1	1	0	0
D/A1		Rn1		0	0	0		Du1		0	0	0		Dc1	
D/A2		Rn2		0	0	0		Du2		0	0	0		Dc2	

CAS

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0		_	1	Q1	ZE	_	4	4		EF	FECTIVE	ADDRE	SS	
	0	0	U		SI.	<u> </u>	U	'			MODE		R	EGISTE	R
0	0	0	0	0	0	0		Du		0	0	0		Dc	

BTST

BIT NUMBER DYNAMIC, SPECIFIED IN A REGISTER

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0		DECISTES	,	1	0	0		EFI	ECTIVE	ADDRE	SS	
"	0	"	"	'	(LGISTEI	`	'	"	"		MODE		R	EGISTE	R.

BCHG

BIT NUMBER DYNAMIC	. SPECIFIED IN A REGISTER

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	_	ECISTE	.	1	0	1		EFI	ECTIVE	ADDRE	SS	
U	U	"	"		EGISTER	`	'	"	'		MODE		R	EGISTE	R

BCLR

BIT NUMBER DYNAMIC, SPECIFIED IN A REGISTER

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0		DECISTED		1	1	0		EF	ECTIVE	ADDRE	SS	
U	"	"	"	'	KEGISTEK		'	'	"		MODE		R	EGISTE	R

BSET

BIT NUMBER DYNAMIC, SPECIFIED IN A REGISTER

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	_	0	0		REGISTER		1	4	1		EFI	FECTIVE	E ADDRE	SS	
U	0	0	0		REGISTER		'		'		MODE		R	EGISTE	R

MOVEP

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	DATA REGISTER			OPMODE		0	0	1		ADDRES: REGISTE		
						16-1	BIT DISF	PLACEME	ENT						

MOVEA

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	SIZ	7=	DE	STINATIO	NC	_	_	1			SOU	RCE		
0		312		R	REGISTER	₹	"	0	!		MODE		R	REGISTER	₹

MOVE

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	61.	7E			DESTI	NATION					SOU	IRCE		
		312		R	REGISTE	₹		MODE			MODE		F	REGISTE	R

MOVE from SR

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	0	0	0	0	1	1		MODE	SOU	IRCE	REGISTER	₹

Instruction Format Summary

-															
MOVE	E fron	n CCF	2												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	0	0	1	0	1	1		EF MODE	FECTIVE	ADDRE R	ESS EGISTE	R
NEG	(
15	14	13	12	11	10	9	8	7	6		4				
0	1	0	0	0	0	0	0	SIZ	ZE1		EF				
											MODE		R	EGISTE	R
CLR															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	0	0	1	0	SI	ZE			FECTIVE			
											MODE		R	EGISTE	R
MOVE	E to C	CR													
15	14	13	12	11	10	9	8	7	6	5	4				0
0	1	0	0	0	1	0	0	1	1		EF MODE	FECTIVE		ESS EGISTE	D
											MODE			EGISTE	<u> </u>
NEG															
15	14	13	12	11	10	9	8	7	6		4				
0	1	0	0	0	1	0	0	SI	7F		EF				
	•	Ů	Ů	Ů	·		Ů				MODE		R	EGISTE	R
NOT															
15	14	13	12	11	10	9	8	7	6	5	4 EF MODE	3	2	1	0
0	1	0	0	0	1	1	0	SI	ZE		EF	FECTIVE	ADDRE	ESS	_
											MODE		l R	EGISTE	K
MOVE	E to S	R													

MODE

EFFECTIVE ADDRESS

2 1

REGISTER

EXT	•	_ \	(1	۲R
	•	_/	•	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	1	0	0		OPMODE		0	0	0	R	EGISTE	K I

LINK

LONG

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	1	0	0	0	0	0	0	0	1	R	EGISTE	R
						HIGH-C	RDER [DISPLAC	EMENT						
						LOW-O	RDER D	ISPLAC	EMENT						

NBCD

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ſ	0	1	0	0	1	0	0	0	0	0		EF	ECTIVE	E ADDRE	SS	
	U	1	"	"	'	"	"	"	"	"		MODE		R	EGISTE	R

SWAP

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	1	0	0	0	0	1	0	0	0	I K	EGISTE	R

BKPT

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	1	0	0	0	0	1	0	0	1		VECTOR	

PEA

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0	1	0	0	1	0	0	0	0	1	EFFECTIVE ADDRESS						
	'	"	"	'	"	"	"	"	'		MODE		F	EGISTE	R	

BGND

1	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	1	0	1	0	1	1	1	1	1	0	1	0

ILLEGAL

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	1	0	1	0	1	1	1	1	1	1	0	0

TAS

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	1	0	0	1	0	1	0	1	1	EFFECTIVE ADDRESS					
"	'	"	"	'	"	'	"	!	'		MODE		R	EGISTE	R

TST

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	_	1	_	1		e i	70		EF	ECTIVE	ADDRE	SS	
U	'	U	"	'	"	·	"	31.	ZE		MODE		R	EGISTE	:R

MULU

LONG 15 13 12 10 9 6 5 3 2 1 14 11 EFFECTIVE ADDRESS 0 0 1 1 0 0 0 0 MODE REGISTER REGISTER DI SIZE 0 REGISTER Dh 0 0 0 0 0 0 0

MULS

							LO	NG								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	1	0	0	1	1	0	0	0	0	EFFECTIVE ADDRESS						
"	'	"	"	'	'	0	"	"	0	MODE			F	REGISTE	:R	
0	RE	GISTER	DI	1	SIZE	0	0	0	0	0	0	0	RE	GISTER	Dh	

DIVU, DIVUL

							LO	NG									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
0	1	0	0	1	1	0	0	0	0	EFFECTIVE ADDRESS							
"	'	U	U	'	'	U	U	"	0	MODE			R	EGISTE	R		
0	RE	GISTER	Dq	0	SIZE	0	0	0	0	0	0	0	RE	GISTER	Dr		

DIVS, DIVSL

							LO	NG									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
0	1	0	0	1	1	0	0	0	1	EFFECTIVE ADDRESS							
U	'	0	"	'	'	"	"	"	'		MODE		F	REGISTE	.R		
0	RE	GISTER	Da	1	SIZE	0	0	0	0	0	0	RE	GISTER	Dr			

TRAP

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	1	1	1	0	0	1	0	0		VEC	TOR	

LINK

							WC	RD							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0 1 0 0 1 1 0 0 1 0 REGISTER														
						WO	RD DISF	PLACEM	ENT						

UNLK

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	1	1	1	0	0	1	0	1	1	R	EGISTE	R

MOVE USP

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	1	1	1	0	0	1	1	0	dr	R	EGISTE	K I

RESET

															0
0	1	0	0	1	1	1	0	0	1	1	1	0	0	0	0

NOP

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	1	1	1	0	0	1	1	1	0	0	0	1

Instruction Format Summary

STOP

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	1	1	1	0	0	1	1	1	0	0	1	0
						ı	MMEDIA	TE DAT	A	-	-	-	-	-	

RTE

															0
0	1	0	0	1	1	1	0	0	1	1	1	0	0	1	1

RTD

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	1	1	1	0	0	1	1	1	0	1	0	0
						16-l	BIT DISF	LACEM	ENT			-			

RTS

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0	1	0	0	1	1	1	0	0	1	1	1	0	1	0	1	Ì

TRAPV

15															
0	1	0	0	1	1	1	0	0	1	1	1	0	1	1	0

RTR

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	1	1	1	0	0	1	1	1	0	1	1	1

MOVEC

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	1	1	1	0	0	1	1	1	1	0	1	dr
A/D	F	REGISTE	R	O 1 1 1 1 0 0 1 1 CONTR							ER	-		-	

J	S	R

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	1	1	1	_	1	0		EFI	ECTIVE	ADDRE	SS	
U	Į.	U	U	ı	Į.	Į.	U	'	U		MODE		R	EGISTE	R

JMP

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	1	1	1	0	1	1		EFI	ECTIVE	ADDRE	SS	
U	!	"	"	'	'	'	"	'	'		MODE		R	EGISTE	11

MOVEM

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	1	dr	0	0	1	SIZE		EFI MODE	ECTIVE	ADDRE	SS EGISTE	P
						RE	L GISTER	LIST MA	ASK		WODE			LOIOTL	

LEA

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	_	_		REGISTER		1	1	4		EF	ECTIVE	ADDRE	SS	
"	'	"	"	'	KEGISTER		'	'	'		MODE		R	EGISTE	:R

CHK

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	1	0	0	Б	REGISTER		SI.	70	0		EF	ECTIVE	ADDRE	SS	
	ļ.	U	U	יו	LGISTEIN		512		"		MODE		R	EGISTE	R

ADDQ

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	_	1		DATA		0	CI.	ZE		EFI	ECTIVE	ADDRE	SS	
U	'	"	'		DAIA		0	31	Z E		MODE		R	EGISTE	.R

SUBQ

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	_	1		DATA		1	e i	ZE		EFI	ECTIVE	ADDRE	SS	
U	ı	U	ı		DATA		ı	31.	ZE		MODE		R	EGISTE	R

DBcc

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	1		COND	ITION		1	1	0	0	1	R	EGISTE	R
						16-E	BIT DISF	LACEM	ENT						

TRAPcc

	15	14						8	7	6	5	4	3	2	1	0
ſ	0	1	0	1		COND	ITION		1	1	1	1	1	(PMODE	
Γ							C	OPTIONA	AL WORE)						
							(OR LON	G WORD)						

Scc

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	1		COND	ITION		1	1		EFI	FECTIVE	ADDRE	SS	
"	'	"	'		COND	ITION		'	'		MODE		R	EGISTE	R

BRA

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
0	1	1	0	0	0	0	0 8-BIT DISPLACEMENT										
				16-	BIT DISF	PLACEM	ENT IF 8	B-BIT DIS	SPLACE	MENT =	\$00						
				32-	BIT DISF	PLACEM	ENT IF 8	B-BIT DIS	PLACE	MENT =	\$FF						

BSR

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	0	0	0	0	1			8-B	IT DISPI	LACEME	NT		
	16-BIT DISPLACEMENT IF 8-BIT DISPLACEMENT = \$00														
	•		•	32-	BIT DISF	PLACEM	ENT IF 8	-BIT DIS	PLACE	ΛΕΝΤ = S	\$FF		•	•	

Bcc

15	14	13	12	11	10	9	8	/	6	5	4	3	2	1	0
0	1	1	0		COND	ITION				8-B	IT DISPI	ACEME	NT		
				16-	16-BIT DISPLACEMENT IF 8-BIT DISPLACEMENT = \$00										
				32-	BIT DISP	LACEM	ENT IF 8	B-BIT DIS	PLACE	/IENT =	\$FF				

N/I	\sim	/	_	<u> </u>
IVI	U	•	ᆮ	u

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	1	R	REGISTE	R	0				DA	λTΑ			

DIVU, DIVUL

							WC)RD							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	0		REGISTE	D	0	1	1		EFF	ECTIVE	ADDRE	SS	
'	0	"	"	'	(LGISTL	11	0	'	'		MODE		R	EGISTE	R

SBCD

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	0	REG	SISTER D)y/Ay	1	0	0	0	0	R/M	REG	ISTER D)x/Ax

PACK

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	0	REG	ISTER D	у/Ау	1	0	1	0	0	R/M	REG	ISTER D	Dx/Ax
	-				10	6-BIT EX	KTENSIC	N: ADJU	JSTMEN	Т			-		

UNPK

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	0	REG	ISTER D	у/Ау	1	1	0	0	0	R/M	REG	ISTER	Dx/Ax
	16-BIT EXTENSION: ADJUSTMENT														

DIVS, DIVSL

							WC)RD							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	0	_	REGISTE	D	1	1	4		EFF	ECTIVE	ADDRE	SS	
'	0	"	"		CEGISTE	I.	'	'	'		MODE		R	EGISTE	R

OR

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ſ	1	0	0	0	ь	EGISTE	Ь		OPMODI	=		EFI	ECTIVE	ADDRE	SS	
	I	U	U	U	, r	EGISTE	K		OPINIODI	=		MODE		R	EGISTE	R

Instruction Format Summary

SUBX

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	1	I KEG	SISTER D	Dy/Ay	1	SI	ZE	0	0	R/M	REG	ISTER [

SUB

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Γ	1	_	0	1		REGISTER	-		OPMODI	=		EFI	ECTIVE	ADDRE	SS	
	'	"	"	'		KEGISTEI	`		OFIVIODI	=		MODE		R	EGISTE	R

SUBA

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	_	1		REGISTE	D		OPMODI	=		EFI	ECTIVE	ADDRE	SS	
1	U	"	'	r	KEGISTEI	N.	'	OFIVIODI			MODE		R	EGISTE	:R

CMPM

15	5	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1		0	1	1	RE	GISTER	Ax	1	I 51	ZE	0	0	1	I KE	GISTER	X AV

CMP

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	1		REGISTER	<u> </u>		OPMODI	=		EF	ECTIVE	ADDRE	SS	
'	U	!	Į.	l i	KEGI31EI	`	'	OFWODI			MODE		R	EGISTE	R

CMPA

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	1		REGISTER)	l ,	OPMODI	_		EFF	ECTIVE	ADDRE	SS	
!		'	!	_ r	ALGISTER	`	,		<u> </u>		MODE		R	REGISTE	R

EOR

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	4	4	_	REGISTER			OPMODE	_		EFI	ECTIVE	ADDRE	SS	
'		Į.	Į.		EGISTER	<u> </u>		JPIVIODE	=		MODE		R	EGISTE	:R

EFFECTIVE ADDRESS

REGISTER

MODE

I\/I			
IVI	u	_	··

							WC	ORD							
15	14	13	12	11	10	9	8	7	6	5		3			
1	1	0	0	R	EGISTE	R	0	1	1			FECTIVE			
											MODE		R	EGISTE	R
ABCI)														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	0	RE	GISTER	Rx	1	0	0	0	0	R/M	RE	GISTER	Ry
MULS	6														
45	4.4	40	40	44	40	•)RD	•	_		0		_	
15	14	13	12	11	10	9	8	7	6	5		3 FECTIVE			
1	1	0	0	R	EGISTE	R	1	1	1			LECTIVE			
EXG	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	0	RE	GISTER	Rx	1			OPMOD			RE	GISTER	Ry
AND		40	40		40			_		_	,				
15	14	13	12	11	10	9	8	7	6	5		3 FECTIVE			
1	1	0	0	R	EGISTE	R		OPMODE	Ē		MODE			EGISTE	
ADD	K														
15	14	13	12		10			7	6	5	4	3		1	
1	1	0	1	RE	GISTER	Rx	1	SIZE		0	0	R/M	RE	GISTER	Ry
ADDA		42	40	44	10	0	0	7	6	E	4	2	2	4	0
15	14	13	12	11	10	9	8	7	О	5	4	3	2	1	0

0

REGISTER

OPMODE

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ſ	1	1	0	1		REGISTER	D		OPMODE	=		EFI	ECTIVE	ADDRE	ESS	
	'	'		'		KLGI3 I EI	TER C		OF WIODI			MODE		R	REGISTE	R

ASL, ASR

MEMORY SHIFT

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	0	0	0	0	dr	1	1		EFI	FECTIVE	E ADDRE	ESS	
'	'	'	U		U	U	dr	!	'		MODE		F	REGISTE	R

LSL, LSR

MEMORY SHIFT

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
1	1	1	0	0	0	1	dr	1	1	EFFECTIVE ADDRESS						
'	'	'	U	U	U		dr	'	!		MODE		R	EGISTE	R	

ROXL, ROXR

MEMORY ROTATE

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	0	0	1	0	dr	1	1		EFI	ECTIVE	E ADDRE	SS	
'	'	'	0	0	'	0	dr	'	'		MODE		R	EGISTE	:R

$\mathsf{ROL}, \mathsf{ROR}$

MEMORY ROTATE

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	0	0	1	1	dr	1	1		EFI	ECTIVE	ADDRE	SS	
'	'	'	"	"	'	'	dr	'	!		MODE		R	EGISTE	R

BFTST

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	0	4	0	0	0	4	1		EFF	ECTIVE	ADDRE	SS	
'	'	'	0	'	U	"	"	'	'		MODE		R	EGISTE	:R
0	0	0	0	Do			OFFSET			Dw			WIDTH		

BFEXTU

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	0	1	0	0	1	1	1		EFF	ECTIVE	ADDRE	ESS	
1			U		U	U	1	1	'		MODE		R	REGISTE	R
0	R	EGISTE	R	Do			OFFSET	-		Dw WIDTH					

BFCHG

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ſ	1	1	1	0	1	0	1	0	1	1		EFI	ECTIVE	ADDRE	SS	
		'	'	"	'	0	'	"	'	'		MODE		R	EGISTE	R
Ī	0	0	0	0	Do			OFFSET			Dw			WIDTH		

BFEXTS

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	0	1	0	1	1	1	-1	EFFECTIVE ADDRESS					
'	'	1	U	!	U	'	1	'		MODE REGISTER				R	
0	R	EGISTE	R	Do			OFFSET	•		Dw WIDTH					

BFCLR

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	_	1	1	0	_	1	1	EFFECTIVE ADDRESS					
'	'	'	"	'	'	"	"	'	'	MODE REGISTER				R	
0	0	0	0	Do			OFFSE1	-		Dw WIDTH					

BFFFO

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	0	1	1	0	1	1	1		EFF	ECTIVE	ADDRE	SS	
'	'	'	0	'	'	"	'	'	'		MODE		R	REGISTE	R
0	R	EGISTE	R	Do		OFF	SET			Dw	Dw WIDTH				

BFSET

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	1	1	1	_	1	1	1		1	4		EF	ECTIVE	ADDRE	ESS	
	1	'	'	"	'	'	'	"	'	'		MODE		F	REGISTE	R
ĺ	0	0	0	0	Do	OFFSET DW WIDTH										

Instruction Format Summary

BFINS

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	_	1	1	1	1	1	1	EFFECTIVE ADDRESS					
1	'	'	"	'	'	'	'	'	'	MODE REGISTER				R	
0	R	EGISTE	R	Do			OFFSE1	-		Dw WIDTH					

ASL, ASR

REGISTER SHIFT

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	0		COUNT/ REGISTER		dr	SIZ	ZE	i/r	0	0	R	EGISTE	٦

LSL, LSR

REGISTER SHIFT

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	0	F	COUNT/ REGISTE	R	dr	SI	ZE	i/r	0	1	R	EGISTE	R

ROXL, ROXR

REGISTER ROTATE

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	0	F	COUNT/ REGISTER		dr	SI	ZE	i/r	1	0	R	EGISTE	

ROL, ROR

REGISTER ROTATE

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	0	F	COUNT/ REGISTEI	R	dr	SI	ZE	i/r	1	1	R	EGISTE	R

PMOVE

MC68EC030, ACX REGISTERS

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	0	0	0	0	0	0		EF	FECTIVE	E ADDRE	ESS	
'	'	'	'	"	"	"	"	"	"		MODE		R	REGISTE	R
0	0	0	Р	REGIST	ER	R/W	0	0	0	0	0	0	0	0	0

PMOVE

MC68030 ONLY, TT REGISTERS

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	4	4	4	_	0	0	_	_			EF	FECTIVE	E ADDRE	ESS	
1	'	'	'	"	"	"	"	"	"		MODE		R	REGISTE	.R
0	0	0	Р	REGIST	ER	R/W	FD	0	0	0	0	0	0	0	0

PLOAD

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	1	1	1	1	0	0	_	_	0	0		EFF	ECTIVE	E ADDRE	SS	
	1	'	'	'	0	0	"	"	U	U		MODE		F	REGISTE	R
Ī	0	0	1	0	0	0	R/W	0	0	0	0			FC		

PVALID

VAL CONTAINS ACCESS LEVEL TO TEST AGAINST

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	0	0	0	0	0	0		EFI	FECTIVE	ADDRE	SS	
'	'	!	'	U	U	U		U	U		MODE		R	EGISTE	R
0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0

PVALID

MAIN PROCESSOR REGISTER CONTAINS ACCESS LEVEL TO TEST AGAINST

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	0	0	0	0	0	0		EF	FECTIVE	ADDR	ESS	
'	'	'	'			0		U	U		MODE		F	REGISTE	R
0	0	1	0	1	0	0	0	0	0	0	0	0	F	REGISTE	R

PFLUSH

MC68030 ONLY

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	4	4				_	_	_		EFF	ECTIVE	ADDRE	SS	
ı	'	'	'	"	"	"	"	"	"		MODE		R	EGISTE	R
0	0	1		MODE		0	0	MA	SK				FC		

PFLUSHA PFLUSHS

R /	C	^	0	റ	E /	1
IV		n	റ	ಗ	ລ	ı

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	1	1	1	1	0	0	0	0	0	0		EFF MODE	ECTIVE	ADDRE	ESS REGISTE	R
Ī	0	0	1		MODE	•	0		MA	SK						

PMOVE

MC68851, TO/FROM TC, CRP, DRP, SRP, CAL, VAL, SCC, AND AC REGISTERS

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Г	1	1	1	1	0	0	0	0	0	0		EF	FECTIVE	ADDRE	SS	
	ı	'	'	'								MODE		R	EGISTE	R
Г	0	1	0	Р	REGIST	ER	R/W	0	0	0	0	0	0	0	0	0

PMOVE

MC68030 ONLY, SRP, CRP, AND TC REGISTERS

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	0	0	0	0	_	0		EFI	FECTIVE	E ADDRE	ESS	
ı	'	'	'				U	0	U		MODE		R	EGISTE	R
0	1	0	Р	REGIST	ER	R/W	FD	0	0	0	0	0	0	0	0

PMOVE

MC68030 ONLY, MMUSR

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	0	0	0	0	0	0		EF	FECTIVE	ADDRE	SS	
'	'	'	'	U	U	0	U	U			MODE		R	EGISTE	R
0	1	1	0	0	0	R/W	0	0	0	0	0	0	0	0	0

PMOVE

MC68EC030, ACUSR

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	0	0	_	_	_	0		EFI	ECTIVE	ADDRE	SS	
ı	!			0	"	"	0	U	U		MODE		R	REGISTE	R
0	1	1	0	0	0	R/W	0	0	0	0	0	0	0	0	0

PMOVE

MC68851, TO/FROM PSR AND PCSR REGISTERS

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ſ	1	1	1	1	0	0	0	0	0	0		EF	FECTIVE	ADDRE	SS	
	'	'	'	'	"	"	"	"	"	"		MODE		R	REGISTE	R
Ī	0	1	1	Р	REGIST	ER	R/W	0	0	0	0	0	0	0	0	0

PMOVE

MC68851, TO/FROM BADX AND BACX REGISTERS

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	0	0	_	0	_	_		EFF	ECTIVE	E ADDRE	ESS	
'	'	'	'	0	0	"	0	"	"	MODE REGISTER				R	
0	1	1	Р	REGISTI	ER	R/W	0	0	0	0 NUM				0	0

PTEST

MC68EC030

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	0	0	0	0	0	0		EFF MODE	ECTIVE	ADDRE	ESS REGISTE	:R
1	0	0	0	0	0	R/W	0	R	EGISTE	R			FC		

PTEST

MC68030 ONLY

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ſ	1	1	1	1	0	0	_	0	0	0		EFF	ECTIVE	ADDRE	SS	
	ı	'	'	'	0	0	"	0	"	"		MODE		F	REGISTE	R
Ī	1	0	0		LEVEL		R/W	Α	REGI	STER			F	С		

PTEST

MC68851

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	4	4	0	0	_	0	_	_		EFF	ECTIVE	ADDRE	SS	
1	'	'	'	U	"	"	"	"	"		MODE		R	EGISTE	R
1	0	0		LEVEL		R/W	Α	REGIST	ER			F	С		

PFLUSHR

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	0	0	0	0	0	0		EFI	FECTIVE	E ADDRE	ESS	
'	'	'	'								MODE		R	EGISTE	R
1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

PScc

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ſ	1	1	-1	1	0	0	0	0	0	1		EFF	ECTIVE	ADDRE	ESS	
	1	'	'	'	"	"	"	"	"	'		MODE		F	REGISTE	:R
Ī	0	0	0	0	0	0	0	0	0	0		MC	68851	CONDITI	ON	

PDBcc

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	0	0	0	0	0	1	0	0	1	COU	NT REG	ISTER
0 0 0 0 0 0 0 0 0 0 MC68851 CONDITION															
	16-BIT DISPLACEMENT														

PTRAPcc

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
1	1	1	1	0	0	0	0	0	1	1	1	1	(OPMODE					
0	0	0	0	0	0	0	0	0	0		MC	68851	CONDITI	ONDITION					
	16-BIT OPERAND OR MOST SIGNIFICANT WORD OF 32-BIT OPERAND (IF NEEDED)																		
	LEAST SIGNIFICANT WORD OF 32-BIT OPERAND (IF NEEDED)																		

PBcc

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1 1 0 0 0 1 SIZE MC68851 CONDITION													
	16-BIT DISPLACEMENT OR MOST SIGNIFICANT WORD OF 32-BIT DISPLACEMENT														
	LEAST SIGNIFICANT WORD OF 32-BIT DISPLACEMENT (IF NEEDED)														

PSAVE

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	0	0	0	1	0	0		EF	ECTIVE	ADDRE	SS	
'	'	'	'	"	"	"	'	"	U		MODE		R	EGISTE	R

PRESTORE

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Γ	1	1	1	1	_	_	_	1	_	1		EFI	ECTIVE	ADDRE	SS	
	1	'	'	'	"	"	"	'	"	!		MODE		R	EGISTE	R

PFLUSH

MC68EC040, POSTINCREMENT SOURCE AND DESTINATION

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	0	1	0	1	0	0	0	I OPM	ODE	I 1	EGISTE	Г (

PFLUSH

MC68040/MC68LC040

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	0	1	0	1	0	0	0	I OPM	ODE	I 1	EGISTE	Г (

PTEST

MC68040/MC68LC040

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	0	1	0	1	0	1	R/W	0	1		EGISTE	R

PTEST

MC68EC040

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	0	1	0	1	0	1	R/W	0	1	R	EGISTE	K I

CINV

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	0	1	0	0	CAC	CHE	0		DPE	I K	EGISTE	1.

CPUSH

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	0	1	0	0	CAC	HE	1	500	PE		EGISTE	

MOVE16

ABSOLUTE LONG ADDRESS SOURCE OR DESTINATION

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	0	1	1	0	0	0	0	OPM	ODE	RE	GISTER	R Ay
	HIGH-ORDER ADDRESS														
	LOW-ORDER ADDRESS														

MOVE16

POSTINCREMENT SOURCE AND DESTINATION

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	0	1	1	0	0	0	1	0	0	RE	GISTER	Ax
1	RE	GISTER	RAy	0	0	0	0	0	0	0	0	0	0	0	0

TBLU, TBLUN

TABLE LOOKUP AND INTERPOLATE

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	1	0	0	0	0	0		EF	FECTIVE	ADDRE	SS	
'	'	'	'	'	0	0	"	0	0		MODE		F	REGISTE	R
0	RE	GISTER	Dx	0	R	0	1	SIZE	0	0	0	0	0	0	0

TBLS, TBLSN

TABLE LOOKUP AND INTERPOLATE

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ſ	1	1	1	1	1	0	0	0	0	0		EFI	FECTIVE	ADDRE	SS	
	'	'	'	'	'	"	"	0	U	"		MODE		R	REGISTE	R
	0	RE	GISTER	Dx	1	R	0	1	SI	ZE	0	0	0	0	0	0

TBLU, TBLUN

DATA REGISTER INTERPOLATE

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ſ	1	1	1	1	1	0	0	0	0	0	0	0	0	REC	SISTER	Dym
ſ	0	RE	GISTER	Dx	0	R	0	0		ZE	0	0	0	REC	SISTER	Dyn

TBLS, TBLSN

DATA REGISTER INTERPOLATE

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	1	0	0	0	0	0	0	0	0	REG	SISTER	Dym
0	RE	GISTER	Dx	1	R	0	0	SI	ZE	0	0	0	REC	SISTER	Dyn

LPSTOP

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0
						ı	MMEDIA	TE DAT	A						

FMOVECR

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	COF	ROCES ID	SOR	0	0	0	0	0	0	0	0	0
0	1	0	1	1	1			ON R				ROM OFFSET	-		

FINT

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	COP	ROCES	SOR	0	0	0		EFI	FECTIVE	ADDRE	ESS	
'	'	'	'		ID			"	0		MODE		F	REGISTE	:R
0	R/M	0		SOURCE	OURCE DES		STINATI		0	0	0	0	0	0	1

FSINH

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	COP	COPROCESSOR			0	0		EFI	FECTIVE	ADDRE	ESS	
1	'				ID		U	U	U		MODE		F	REGISTE	R
0	R/M	0			OURCE DES		STINATI EGISTE		0	0	0	0	0	1	0

FINTRZ

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	COP	COPROCESSOR			0	0		EF	FECTIVE	E ADDRE	ESS	
'	!	'	'		ID		"	"	0		MODE		R	REGISTE	R
0	R/M	0		SOURCE PECIFIE			STINATI REGISTE		0	0	0	0	0	1	1

FLOGNP1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	COF	PROCES	SOR	0	0	0		EFI	FECTIVE	E ADDRE	ESS	
'	'	'	'		ID		0	U	U		MODE		R	EGISTE	R
0	R/M	0		SOURCE PECIFIE			STINATI EGISTE		0	0	0	0	1	1	0

FETOXM1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	COF	PROCES	SOR	0	0	0		EFI	FECTIVE	E ADDRE	ESS	
'	'	'	'		ID		U	U	U		MODE		R	EGISTE	R
0	R/M	0		SOURCE PECIFIE			STINATI EGISTE		0	0	0	1	0	0	0

FTANH

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ſ	1	1	1	1	COP	COPROCESSOR			_	_		EF	FECTIVE	ADDRE	SS	
	ı	1		1		ID		0	0	0		MODE		R	EGISTE	R
	0	R/M	0		SOURCE PECIFIE			STINATI EGISTE		0	0	0	1	0	0	1

FATAN

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	COF	PROCES	SOR	_	0	_		EF	FECTIVE	E ADDRE	SS	
'	'	'	'		ID			"	"		MODE		F	REGISTE	R
0	R/M	0		SOURCE			STINATI REGISTE		0	0	0	1	0	1	0

FASIN

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	COP	ROCES	SOR	_	0	_		EF	FECTIVE	ADDRE	SS	
'	'	'	'		ID			0	"		MODE		F	REGISTE	R
0	R/M	0		SOURCE PECIFIE			STINATI EGISTE		0	0	0	1	1	0	0

FATANH

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	COP	COPROCESSOR			_	_		EF	FECTIVE	ADDRE	SS	
'	'	'	'		ID		"	"	"		MODE		F	EGISTE	R
0	R/M	0		SOURCE PECIFIE	OURCE DES		STINATI		0	0	0	1	1	0	1

FSIN

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	COP	ROCES	SOR	_	_	0		EF	FECTIVE	ADDRE	SS	
'	'		1		ID			U	U		MODE		R	REGISTE	R
0	R/M	0		SOURCE PECIFIE	DURCE DES		STINATI REGISTE		0	0	0	1	1	1	0

FTAN

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	COF	ROCES	SOR	0	_	_		EFI	FECTIVE	ADDRE	SS	
'	1	'	'		ID			0	0		MODE		R	EGISTE	R
0	R/M	0		SOURCE PECIFIE	DURCE DES		STINATI REGISTE		0	0	0	1	1	1	1

FETOX

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	COF	COPROCESSOR			0	_		EF	FECTIVE	ADDRE	SS	
'	'	'	'		ID		"	"	"		MODE		F	REGISTE	R
0	R/M	0		SOURCE PECIFIE	DURCE D		STINATI REGISTE		0	0	1	0	0	0	0

FTWOTOX

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	COF	COPROCESSOR			0	_		EF	FECTIVE	ADDRE	SS	
'	'	'	'		ID			"	"		MODE		F	REGISTE	R
0	R/M	0			OURCE DES		STINATI EGISTE		0	0	1	0	0	0	1

FTENTOX

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	COF	PROCES	SOR	_	0	_		EF	FECTIVE	ADDRE	SS	
1	'	'	'		ID		"	0	"		MODE		F	REGISTE	R
0	R/M	0			OURCE DES		STINATI EGISTE		0	0	1	0	0	1	0

FLOGN

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ſ	1	1	1	1	COF	COPROCESSOR			0	0		EF	FECTIVE	ADDRE	SS	
	'	'	'	'		ID				U		MODE		R	EGISTE	R
	0	R/M	0		SOURCE	OURCE DES		STINATI REGISTE		0	0	1	0	1	0	0

FLOG10

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Г	1	1	1	1	COP	COPROCESSOR			_	_		EF	FECTIVE	ADDRE	SS	
	'	'	'	'		ID		"	"	"		MODE		F	EGISTE	R
	0	R/M	0		SOURCE PECIFIE	OURCE DES		STINATI		0	0	1	0	1	0	1

FLOG2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	COF	COPROCESSOR			0	_		EF	FECTIVE	ADDRE	SS	
'	'	'	'		ID			"	"		MODE		F	EGISTE	R
0	R/M	0		SOURCE	OURCE DES		STINATI REGISTE		0	0	1	0	1	1	0

FCOSH

 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	COF	COPROCESSOR			0	0		EF	FECTIVE	E ADDRE	SS	
'	'	'	'		ID			"	"		MODE		F	REGISTE	R
0	R/M	0		SOURCE	OURCE DES		STINATI REGISTE		0	0	1	1	0	0	1

FACOS

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	COF	COPROCESSOR			0	_		EF	FECTIVE	E ADDRE	SS	
'	'	'	'		ID			"	"		MODE		F	REGISTE	R
0	R/M	0			OURCE DES		STINATI REGISTE		0	0	1	1	1	0	0

FCOS

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	COF	ROCES	SOR	_	_	0		EF	FECTIVE	ADDRE	SS	
	'	'	'		ID		"	"	0		MODE		R	REGISTE	R
0	R/M	0		SOURCE PECIFIE	OURCE DES		STINATI EGISTE		0	0	1	1	1	0	1

FGETEXP

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	COF	COPROCESSOR			_	0		EF	FECTIVE	ADDRE	SS	
'	'	'	'		ID		"	"	0		MODE		F	EGISTE	R
0	R/M	0		SOURCE	OURCE DES		STINATI REGISTE		0	0	1	1	1	1	0

FGETMAN

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	COP	ROCES	SOR	_	_	0		EFI	FECTIVE	ADDRE	ESS	
'	'	'	'		ID			"	0		MODE		F	REGISTE	R
0	R/M	0		SOURCE			STINATI		0	0	1	1	1	1	1

FMOD

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	COF	ROCES	SOR	0	0	0		EFI	FECTIVE	ADDRE	ESS	
'	1	'	'		ID		"	"	0		MODE		R	EGISTE	R
0	R/M	0		SOURCE PECIFIE	DURCE DES		STINATI REGISTE		0	1	0	0	0	0	1

FSGLDIV

1	5	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	1	1	1	1	COF	COPROCESSOR			0	0		EF	FECTIVE	E ADDRE	SS	
	1	'	'	'		ID			"	"		MODE		F	REGISTE	R
()	R/M	0		SOURCE	OURCE DES		STINATI REGISTE		0	1	0	0	1	0	0

FREM

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	COF	COPROCESSOR			0	_		EF	FECTIVE	ADDRE	SS	
'	'	'	'		ID			"	"		MODE		F	REGISTE	R
0	R/M	0		SOURCE	OURCE DES		STINATI EGISTE		0	1	0	0	1	0	1

FSCALE

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	COF	COPROCESSOR			0	_		EF	FECTIVE	ADDRE	SS	
1	'	'	'		ID			"	"		MODE		F	REGISTE	R
0	R/M	0		SOURCE	OURCE DES		STINATI EGISTE		0	1	0	0	1	1	0

FSGLMUL

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	COF	ROCES	SOR	_	_	0		EFI	FECTIVE	ADDRE	SS	
'		'	'		ID			0	U		MODE		R	REGISTE	R
0	R/M	0		SOURCE PECIFIE	DURCE DEST		STINATI EGISTE		0	1	0	0	1	1	1

FSINCOS

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ſ	1	1	1	1	COF	COPROCESSOR ID			_	0		EF	FECTIVE	ADDRE	SS	
	Į.	'	'	'					"	0		MODE		F	REGISTE	R
Γ	0	R/M	0	;	SOURCE D		DE	STINATI	ON	0	1	1	0	DE	STINATI	ION
	0	I IX/IVI		S	PECIFIE	R	R	REGISTE	R		'	'	"	REG	SISTER,	FPc

FCMP

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	COF	COPROCESSOR			0	0		EF	FECTIVE	ADDRE	ESS	
'	'	'	'		ID				U		MODE		R	EGISTE	R
0	R/M	0		SOURCE PECIFIE	DURCE DES		STINATI EGISTE		0	1	1	1	0	0	0

FTST

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Г	1	1	1	1	COP	COPROCESSOR			0	0		EF	FECTIVE	ADDRE	SS	
	ı	'	'	'		ID			0	0		MODE		F	REGISTE	R
	0	R/M	0			OURCE DES		STINATI REGISTE		0	1	1	1	0	1	0

FABS

 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	COF	PROCES	SOR	_	_	0		EF	ECTIVE	E ADDRE	ESS	
'	'	'	'		ID			"	"		MODE		F	REGISTE	:R
0	R/M	0			SOURCE PECIFIER		STINATI				(OPMODI	E		

FADD

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	4	1	4	COP	ROCES	SOR	_	_	0		EF	ECTIVE	ADDRE	ESS	
1	'	'	'		ID			"			MODE		F	REGISTE	R
0	R/M	0			SOURCE PECIFIER		STINATI EGISTE				(PMODI			

FDIV

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	COP	ROCES	SOR	0	_	0		EFF	ECTIVE	E ADDRE	SS	
'	'	'	'		ID		"	"			MODE		F	EGISTE	R
0	R/M	0		SOURCE			STINATI				(PMODI	E		
			S	PECIFIE	:K		REGISTE	:K							

FMOVE

DATA REGISTER, EFFECTIVE ADDRESS TO REGISTER

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ſ	1	1	1	1	COP	ROCES	SOR	0	0	0		EF	ECTIVE	ADDRE	SS	
	'	!	'	'		ID		"	"	"		MODE		R	EGISTE	R
	0	R/M	0		SOURCE PECIFIE			STINATI REGISTE				(PMODI	E		

FMUL

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	COP	ROCES	SOR	0	0	0		EFF	ECTIVE	ADDRE	SS	
!	1	'	'		ID		"	0	0		MODE		R	EGISTE	R
0	R/M	0		SOURCE PECIFIE			STINATI REGISTE				(PMODI	E		

FNEG

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ſ	1	1	1	1	COF	PROCES	SOR	_	_	0		EFF	ECTIVE	ADDRE	ESS	
	ı	'	'	'		ID		"	"	"		MODE		F	REGISTE	:R
	0	R/M	0	1	SOURCI PECIFIE		I	STINATI EGISTE				(OPMODI	Ξ		

FSQRT

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	COF	PROCES	SOR	_	0	0		EF	ECTIVE	ADDRE	ESS	
1	'	'	'		ID		"	"	"		MODE		F	REGISTE	R
0	R/M	0	l	SOURCE PECIFIE		l	STINATI REGISTE				(OPMODI	E		

FSUB

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ſ	1	1	1	1	COF	PROCES	SOR	_		0		EFF	ECTIVE	E ADDRE	ESS	
	'	'	'	'		ID		"	"	"		MODE		F	REGISTE	:R
	0	R/M	0	1	SOURCI PECIFIE		I	STINATI EGISTE				(DPMOD	E		

FMOVE

DATA REGISTER, REGISTER TO MEMORY

_	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	4	1	1	1	0	_	1	0				EFI	ECTIVE	E ADDRI	ESS		
	'	'	'	'	"	"	1	U	"	0		MODE		F	REGISTE	R	
	0	1	1		SOURCE			STINAT				K-FACTOR (IF REQUIRED)					

FMOVE

SYSTEM CONTROL REGISTER

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	COP	ROCES	SOR	_	0	0		EF	FECTIVE	ADDRE	SS	
ı		'			ID		U	U	U		MODE		R	EGISTE	R
1	0	dr		EGISTE SELECT		0	0	0	0	0	0	0	0	0	0

FMOVEM

CONTROL REGISTERS

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	COP	ROCES ID	SOR	0	0	0		EF MODE	FECTIVE	ADDRE	SS EGISTE	.R
1	0	dr	F	EGISTE SELECT		0	0	0	0	0	0	0	0	0	0

FMOVEM

DATA REGISTERS

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	1	1	1	1	COF	ROCES ID	SOR	0	0	0		EFF MODE	ECTIVE	ADDRE R	SS EGISTE	R
Ī	1	1	dr	MC	DE	0	0	0		•		REGIST	ER LIST	•		

cpGEN

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
1	1	1	1	COF	ROCES	SOR	0	0	0		EFF	EFFECTIVE ADDRESS DE REGISTER						
'	'	'	'		ID		"	0			MODE	1						
	•	•	•	C	OPROCE	SSOR I	D-DEPE	NDENT	COMMAI	ND WO	RD		•					
		OPT	IONAL E	FFECTI	VE ADDF	RESS O	R COPR	OCESSO	OR ID-DE	FINED	EXTENS	ION WC	RDS					

FScc

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ſ	1	1	1	1	COF	ROCES	SOR	0	0	1		EF	ECTIVE	ADDRE	SS	
	•					ID						MODE		R	EGISTE	R
ſ	0	0	0	0	0	0	0	0	0	0	CON	ANOITIC	L PRED	ICATE		

cpScc

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Г	1	1	1	1	COF	ROCES	SOR	0	0	1		EF	ECTIVE	ADDRE	SS	
	ı	'	'	'		ID		"	"	'		MODE		R	EGISTE	R
	0	0	0	0	0	0	0	0	0	0		COPRO	CESSO	R ID CON	NOITION	
			OPT	IONAL E	FFECTI	VE ADDI	RESS OF	R COPR	OCESSO	OR ID-DE	FINED	EXTENS	ION WC	RDS		

FBcc

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	COP	ROCES:	SOR	0	1	SIZE	(CONDITIO	ONAL PF	REDICAT	Έ	
	16-BIT DISPLACEMENT OR MOST SIGNIFICANT WORD OF 32-BIT DISPLACEMENT														
	LEAST SIGNIFICANT WORD OF 32-BIT DISPLACEMENT (IF NEEDED)														

срВсс

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	COP	COPROCESSOR ID OPTIONAL COPROCES			1	SIZE		COPRO	CESSOF	R ID COI	NDITION	
				OPTION	NAL COF	PROCES	SSOR ID	-DEFINE	D EXTE	NSION	WORDS				
							WOR	D OR							
						LONG-	WORD D	DISPLAC	EMENT						

cpSAVE

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	COF	PROCES	SOR	1	_	_		EF	ECTIVE	ADDRE	SS	
'	'	'	'		ID		'	"	"		MODE		R	EGISTE	R

FSAVE

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ſ	1	1	1	1	COF	ROCES	SOR	1	0	0		EFI	ECTIVE	ADDRE	SS	
		'	'	'		ID		'	"	"		MODE		R	EGISTE	R

cpRESTORE

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ſ	1	1	1	1	COF	PROCES	SOR	1	_	1		EF	ECTIVE	ADDRE	ESS	
	'	'	'	'		ID		'	"	'		MODE		F	REGISTE	R

FRESTORE

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	COF	ROCES	SOR	1	0	1		EFI	ECTIVE	ADDRE	SS	
'	'	'	'		ID		'	"	'		MODE		R	EGISTE	R

FDBcc

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	COF	ROCES ID	SOR	0	0	1	0	0	1	F	COUNT REGISTE	R
0	0	0	0	0	0	0	0	0	0		CONI	DITIONA	L PRED	ICATE	
	•	•		•		16-l	BIT DISF	LACEMI	ENT			•		•	

cpDBcc

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	COF	ROCES ID	SOR	0	0	1	0	0	1	F	REGISTE	R
0	0	0	0	0	0	0	0	0	0		COPRO	CESSOI	R ID COI	NDITION	
				OPTION	VAL CO	ROCES	SOR ID	DEFINE	D EXTE	NSION \	NORDS				
16-BIT DISPLACEMENT															

FTRAPcc

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
1	1	1	1	COF	ROCES ID	SOR	0	0	1	1	1	1		MODE					
0	0	0	0	0	0	0	0	0	0		CONI	NDITIONAL PREDICATE							
	16-BIT OPERAND OR MOST SIGNIFICANT WORD OF 32-BIT OPERAND (IF NEEDED)																		
				LEAST:	SIGNIFI	CANT W	ORD OF	32-BIT	OPERAI	ND (IF N	EEDED)								

cpTRAPcc

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	COF	ROCES ID	SOR	0	0	1	1	1	1		OPMODE	
0 0 0 0 0 0 0 0 0 0 COPROCESSOR ID CONDITION												NDITION			
	•			OPTIO	VAL CO	PROCES	SOR ID	-DEFINE	D EXTE	NSION \	WORDS				
						(OPTIONA	AL WOR	D						
						OR LC	NG-WO	RD OPE	RAND						

FNOP

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	COF	ROCES ID	SOR	0	1	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0