Carleton University

Course : ELEC3509 *Lab :* 3 L1

The 741 Op-Amp

July 7, 2017

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1 Introduction

In this lab, a simple op-amp was analysed by hand. Then it was modelled in SPICE and the results were compared to hand calculations.

The DC operation point, slew rate, gain, common mode range, common mode gain, frequency response and unity gain were modeled and compared.

2 Theory & Design

2.1 DC Bias

2.1.1 Q_{14} and Q_{20}

Starting at V_2 a voltage loop is found where the emitter currents can be solved. Note that here the V_{BE} cannot be assumed to be 0.6V, it will be approximated to $V_{BE} = V_T ln(\frac{I_C}{I_S})$.

$$1.4V = V_{BE14} + V_{BE20} + I_{E14}(30\Omega) + I_{E20}(30\Omega) \tag{1}$$

$$1.4V = V_T ln(\frac{I_{C14}}{I_S}) + V_T ln(\frac{I_{C20}}{I_S}) + I_{E14}(30\Omega) + I_{E20}(30\Omega) \tag{2}$$

$$1.4V = V_T ln(\frac{\alpha I_{E14}}{I_S}) + V_T ln(\frac{\alpha I_{E20}}{I_S}) + I_{E14}(30\Omega) + I_{E20}(30\Omega) \tag{3}$$

Solving Equation 3, assuming $I_{E14} = I_{E20}$, then $I_E = 1.14mA$.

Next we can solve for the base voltage and currents in these two transistor.

$$V_{BE14} = V_T ln(\frac{\alpha I_{E14}}{I_S}) = 0.65V \tag{4}$$

$$V_{BE20} = V_T ln(\frac{\alpha I_{E20}}{I_S}) = 0.69V \tag{5}$$

$$I_{B14} = I_{B20} = \frac{I_E}{\beta + 1} = 11.3\mu A \tag{6}$$

2.1.2 Q_{23}

To solve for the current of Q_{23} lets start by getting the voltage at the base of V_{B14}.

$$2.5V + (1.14mA)(30\Omega) + 0.65V = 3.18V \tag{7}$$

Now the current across R_{13} can be found in order to get the total current going into the emitter of Q_{23}.

$$I_{R13} = \frac{5V - 3.18V}{90k\Omega} = 20.3\mu A \tag{8}$$

The base current of the two transistors Q_{14} and Q_{20} can be ignored since they will cancel each other out.

$$I_{C23} = 180\mu A + 20.2\mu A = 200.2\mu A \tag{9}$$

2.1.3 Q_{17}

To find the collector current at Q_{17} we can work out way from V_{B14}

$$V_{C17} = 3.18V - 1.4V - 0.6V = 1.18V \tag{10}$$

Next the current from R_{12} can be found, after which the rest of the voltages and currents can be found.

$$I_{R12} = \frac{5V - 1.18V}{30k\Omega} = 76.4\mu A \tag{11}$$

$$I_{C17} = 550\mu A + 76.4\mu A = 626.4\mu A \tag{12}$$

$$\begin{aligned} V_{E17} &= (R8)(I_{E17}) && (13)\\ &= 100\Omega\frac{\beta+1}{\beta}626.4\mu A && (14)\\ &= 63mV && (15) \end{aligned}$$

$$V_{B17} = 0.6V + 0.06V = 0.66V \tag{16}$$

2.1.4 Q_{16}

$$I_{E16} = I_{R9} = \frac{0.66V}{50k\Omega} = 13.2\mu A \tag{17}$$

2.1.5 Q_1, Q_2, Q_5, Q_6, Q_7

Assume $V_{common} = V_{B1} = V_{B2}$.

$$V_{E1} = V_{E2} = 2.5V + 0.6V = 3.1V \tag{18}$$

$$I_{R11} = \frac{5V - 3.1V}{1M\Omega} = 1.9\mu A \tag{19}$$

Since the collectors of Q_1 and Q_2 are connected to a current mirror, it can be assumed that their collector currents are the same.

$$I_{C1} = I_{C2} = \frac{1.9\mu A + 19\mu A}{2} = 10.5\mu A \tag{20}$$

$$\begin{aligned} I_{C6} &= I_{C2} - I_{B16} && (21)\\ &= 10.5\mu A - \frac{13.4\mu A}{100} && (22)\\ &= 10.3\mu A && (23) \end{aligned}$$

$$I_{C5} = I_{C6} \tag{24}$$

$$I_{C7} = I_{B16} \tag{25}$$

Transistor	I_C (μA)	R_o (MΩ)	g_m (mS)	r_π (kΩ)
1	10.5	1.9	0.42	238
2	10.5	1.90	0.42	238
5	10.3	7.77	0.41	244
6	10.3	7.77	0.41	244
7	13.4	5.97	0.54	185
14	1140	0.070	45.6	2.19
16	13.2	6.06	0.53	189
17	626	0.13	25.0	4.0
20	1140	0.018	45.6	2.19
23	200.2	0.10	8.00	12.5

Table 1: Summary of calculated theoretical DC values

2.2 First Stage

2.2.1 Gain

To calculate the gain, the small signal model was draw and simplified in the following Figure.

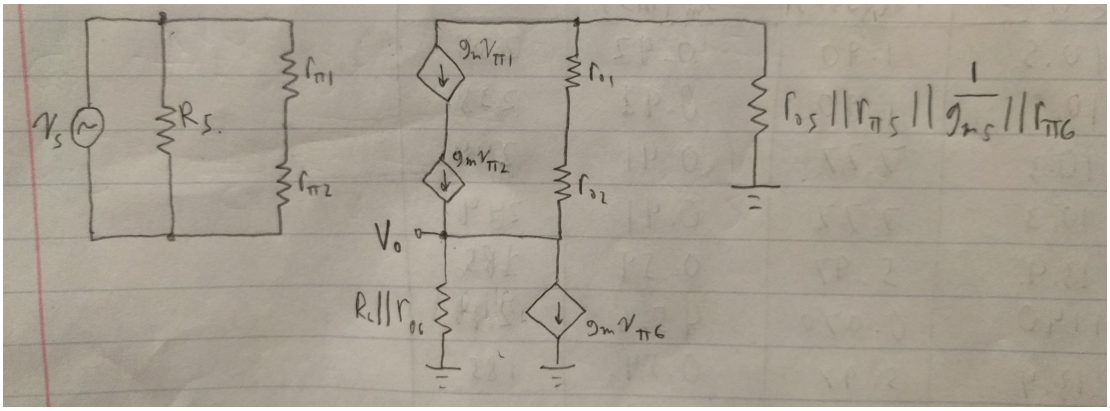

Figure 1: Small signal model for the first stage of the opamp

v_o can be determined by multiplying the output current and equivalent load resistance

$$v_o = R_L^{'} I_{out} = (R_L \parallel r_{o6} \parallel r_{o2})(g_{m2} v_{\pi 2} - g_{m6} v_{\pi 6}) \tag{26}$$

Next $v_{\pi 6}$ can be related to $v_{\pi 2}$

$$v_{\pi 6} = -g_{m2} v_{\pi 2} (r_{o5} \parallel r_{\pi 5} \parallel r_{e5}) \tag{27}$$

Now $v_{\pi 2}$ in terms of v_s, note that since $r_{\pi 1} = r_{\pi 2}$ the divider ratio is roughly 2.

$$v_{\pi 2} = v_s \frac{r_{\pi 1}}{r_{\pi 1} + r_{\pi 2}} \tag{28}$$

$$= \frac{v_s}{2} \tag{29}$$

Now some work can be done to find the gain. Subbing 29 into 27 yields the following.

$$v_{\pi 6} = -g_{m2} \frac{v_s}{2} (r_{o5} \parallel r_{\pi 5} \parallel r_{e5}) \tag{30}$$

And now sub that into 31. To simplify this nasty expression the following assumptions are made, $r_{e5} << r_{\pi 5} << r_{o5}$ and $g_{m6} = g_{m5}$.

$$v_o = R_L^{'} I_{out} = (R_L \parallel r_{o6} \parallel r_{o2})(g_{m2} \frac{v_s}{2} + g_{m6} g_{m2} \frac{v_s}{2} (r_{o5} \parallel r_{\pi 5} \parallel r_{e5})) \tag{31}$$

$$v_o = (R_L \parallel r_{o6} \parallel r_{o2})(g_{m2} \frac{v_s}{2} + g_{m6} g_{m2} \frac{v_s}{2} r_{e5}) \tag{32}$$

$$v_o = (R_L \parallel r_{o6} \parallel r_{o2}) g_{m2} v_s \tag{33}$$

The gain of the first stage of the amplifier is as follows.

$$A_{v1} = \frac{v_o}{v_s} = (R_L \parallel r_{o6} \parallel r_{o2}) g_{m2} \tag{34}$$

$$= (643k\Omega \parallel 7.77M\Omega \parallel 1.90M\Omega) 0.42mS \tag{35}$$

$$= 283 \frac{V}{V} \tag{36}$$

2.2.2 Output Resistance

The output resistance of this amplifier can be found where r_{o6} is reflected by $g_{m6} v_{\pi 6}$.

$$R_{out} = r_{o6}(1 + g_{m6}(R_2 \parallel r_{\pi 6})) \tag{37}$$

$$= 11.6M\Omega \tag{38}$$

2.3 Second Stage

2.3.1 Input Resistance

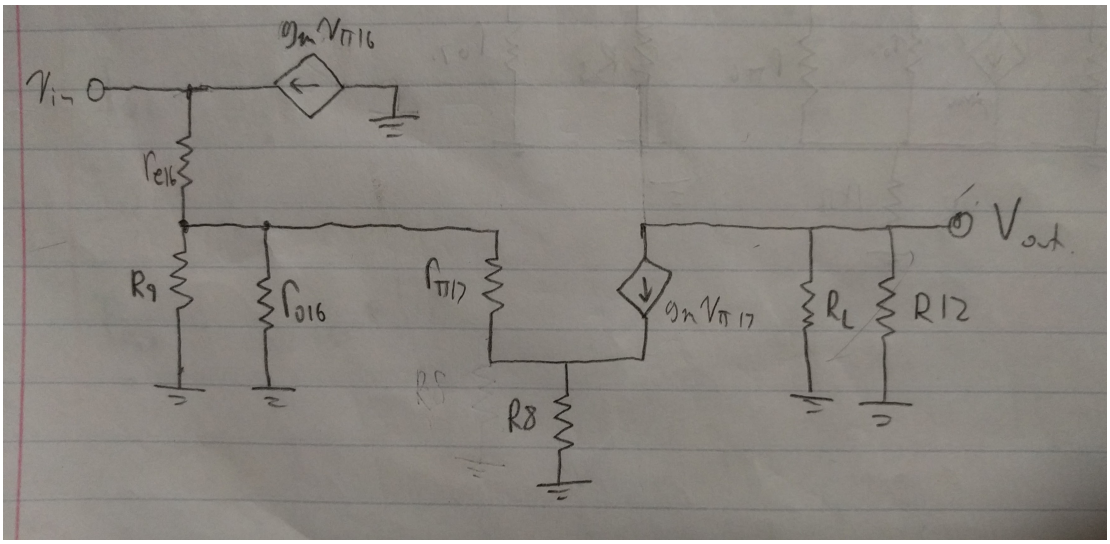

Figure 2: Small signal model for the second stage of the opamp

The small signal model for the second stage of the amplifier can be seen in the Figure above. We will start by finding the input resistance of the amplifier. It is noteworthy that the input of this stage is a common collector amplifier. The gain of the second stage is large if its load resistance is large, the common collector amplifier acts to multiply the input resistance of this stage by β as we will see below.

$$R_{in} = \beta(r_{e16} + r_{o16} \parallel R_9 \parallel (r_{\pi 17} + (1+\beta)R_8)) \tag{39}$$
$$= 100(1.89k\Omega + 6.06M\Omega \parallel 50k\Omega \parallel (4.0k\Omega + (101)100\Omega)) \tag{40}$$
$$= 643k\Omega \tag{41}$$

2.3.2 Gain

To find the gain we will start at the input of the amplifier. First let us find the voltage V_A from the voltage v_{in}.

$$\frac{V_A}{V_{in}} = \frac{r_{o16} \parallel R_9 \parallel (r_{\pi 17} + (1+\beta)R_8)}{r_{e17} + r_{o16} \parallel R_9 \parallel (r_{\pi 17} + (1+\beta)R_8)} = 1 \tag{42}$$

It was found that when subbing in values, the above was very close to one, therefore let $v_{in} = V_A$. Now we can easily find $v_{\pi 17}$ from v_s.

$$\frac{r_{\pi 17}}{v_{in}} = \frac{(1+\beta)R_8}{r_{\pi 17} + (1+\beta)R_8} \tag{43}$$

And now v_{out} in terms of $v_{\pi 17}$.

$$\frac{v_{out}}{v_{\pi 17}} = -g_{m17}(R_L \parallel R_{12}) \tag{44}$$

$$A_{v2} = -g_{m17}(R_L \parallel R_{12})\frac{(1+\beta)R_8}{r_{\pi 17} + (1+\beta)R_8} \tag{45}$$

$$= 169\frac{V}{V} \tag{46}$$

2.4 Third Stage

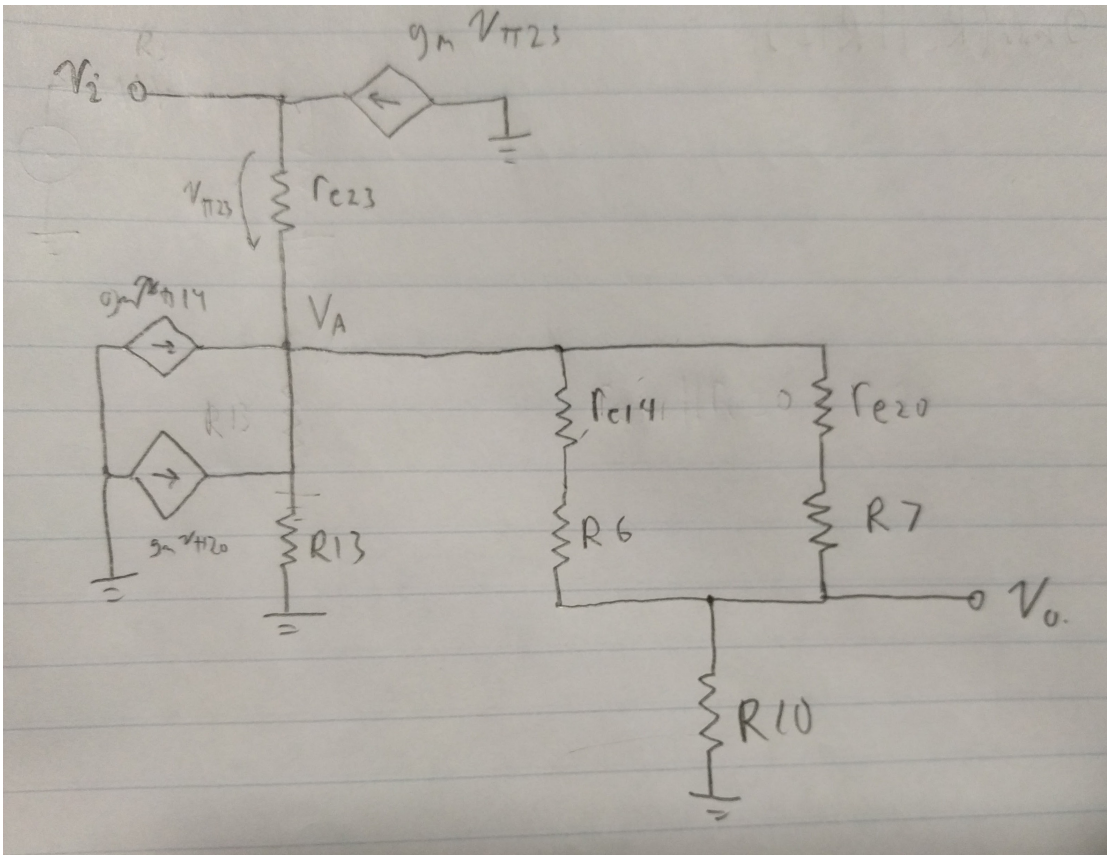

Figure 3: Small signal model for the third stage of the opamp

2.4.1 Input Resistance

As this is entirely a buffer stage it will have a very high input resistance. We can find the expression for the input resistance by looking at the small signal model.

$$R_{in} = (\beta+1)r_{e23} + (\beta+1)^2(R_{13} \parallel ((r_{e14} + R_6) \parallel (r_{e20} + R_7) + R_{10})) \tag{47}$$

In this case R_{10} is so massive it will dominate all the other resistances, we are then left with $R_{in} = (101)^2 1M\Omega = \infty$.

2.4.2 Gain

The gain of this amplifier can be found a series of voltage dividers. Since this is a cascade of 2 common collector amplifiers, the fain should be found to be very close to 1. We will start by finding V_A from v_{in}.

$$\frac{V_A}{v_{in}} = \frac{R_{in}}{R_{in} + (1+\beta)r_{e23}} \tag{48}$$

Now v_{out} from V_A.

$$\frac{v_{out}}{V_A} = \frac{R_{10}}{R_{10} + (r_{e14} + R_6) \parallel (r_{e20} + R_7)} \tag{49}$$

The total gain can now be found and expanded. It is very close to 1.

$$A_{v3} = \frac{R_{10}}{R_{10} + (r_{e14} + R_6) \parallel (r_{e20} + R_7)} \frac{R_{in}}{R_{in} + (1+\beta)r_{e23}} \tag{50}$$

$$= \frac{R_{10}}{R_{10} + (r_{e14} + R_6) \parallel (r_{e20} + R_7)} \times \tag{51}$$

$$\frac{(\beta+1)r_{e23} + (\beta+1)^2(R_{13} \parallel ((r_{e14} + R_6) \parallel (r_{e20} + R_7) + R_{10}))}{(\beta+1)r_{e23} + (\beta+1)^2(R_{13} \parallel ((r_{e14} + R_6) \parallel (r_{e20} + R_7) + R_{10})) + (1+\beta)r_{e23}}) \tag{52}$$

$$= 1 \tag{53}$$

2.5 Complete Gain

The complete gain for this amplifier can simply be found by multiplying hte gain of the first and second stages since the last stage of the amplifer is a buffer with gain very close to one.

$$A_v = A_{v1}A_{v2} = 169\frac{V}{V}283\frac{V}{V} = 47\frac{kV}{V} \tag{54}$$

3 Output Swing and Common Mode Range

To find the output swing and common mode range of this amplifier we first note that the supply voltage of the op amp is at 5V. Next we note that there is 0.6V lost on each of the transistors. The maximum swing can then be calculated as follows provided the output is in the range from 1.2V to 5V.

$$v_{swing} = \frac{5V - 1.2V}{2} = 1.9V \tag{55}$$

Therefore a 1.9V swing centered around the middle of the opamp range would be possible.

Using the same logic as the output range except the input stage was primarily considered, the common mode range was determined to be from 1.2V to 4.4V.

3.1 Design for C_1

3.1.1 f_u

The purpose of C_1 in this amplifier is to avoid positive feedback at high frequencies. C_1 achieves this by bringing the gain to unity at a designed frequency where we don't need it to go. In this lab the desired frequency is f_u =1MHz.

To determine this value we can start to split C_1 into two with the Miller effect to ease calculation. Since this is a high gain stage, the second capacitance can be ignored, the important capacitor is placed at the output of the first stage and the input of the second stage.

$$C_M = C_1(1 + A_{v2}) \tag{56}$$

Due to this capacitors location its parallel resistance to ground can be expressed as $R_{out1} \parallel R_{in2}$. The pole of this capacitor can therefore be expressed as follows.

$$\omega_p = \frac{1}{C_M(R_{out1} \parallel R_{in2})} \tag{57}$$

The total frequency can be found from the following.

$$\omega_T = A_0\omega_p \tag{58}$$

$$\frac{1}{\omega_p} = \frac{A_0}{\omega_T} \tag{59}$$

$$C_M(R_{out1} \parallel R_{in2}) = \frac{A_0}{\omega_T} \tag{60}$$

$$C_M = \frac{A_0}{\omega_T(R_{out1} \parallel R_{in2})} \tag{61}$$

$$= 63pF \tag{62}$$

3.1.2 Slew Rate

The slew rate of this amplifier can now be simply calculated that we have the value for C_1.

$$S_r = \frac{I_1}{C_1} \tag{63}$$

$$= \frac{19\mu A}{63pF} \tag{64}$$

$$= 310\frac{V}{s} \tag{65}$$

3.2 Pre-lab Questions

1. V_5 is the common mode voltage applied on both of the input of the opamp. V_{10} is the DC offset of the inputs of the opamp. The main difference is that in the ideal case V_5 should not be amplified at all, and V_{10} should be amplified to infinity.

2. Q_7 is a helper transistor for the base current of the current mirror. It supplies the current that is lost from the base so it is mirrored exactly on each side.

3. The purpose of C_1 is to set the low frequency pole of the circuit. This prevents the opamp from producing positive feedback.

4. The ideal current sources could be implemented with current mirrors. This may impact the amplifiers frequency response since all of the additional transistors will add more high frequency poles.

5. The purpose of V_2 is to eliminate the 1.4V dead zone in the push pull output stage generated from the diode drops of the output stage. This voltage source could be made from 2 diodes in series.

6. Each stage of the opamp has a different job. The first stage is the one that produces the differential gain, The second is a high gain amplifier to greatly increase the gain, and finally the last stage is a buffer. The last stage of the opamp is important even if it has little gain since it is necessary to decrease the output resistance of the amplifier. The amplifier is more useful and universal if it provides the lowest possible output resistance.

7. The DC power of this opamp can be found by summing all of the collector currents and multiplying by the supply current since all of the transistors are in parallel with the supply.

4 Simulation

4.1 Vo-Vd plot

To determine the required offset to ensure the correct offset for later, the differential is swept from -10 mV to 10 mV. The following figures show the sweep and zoom in to find the exact location of the midpoint.

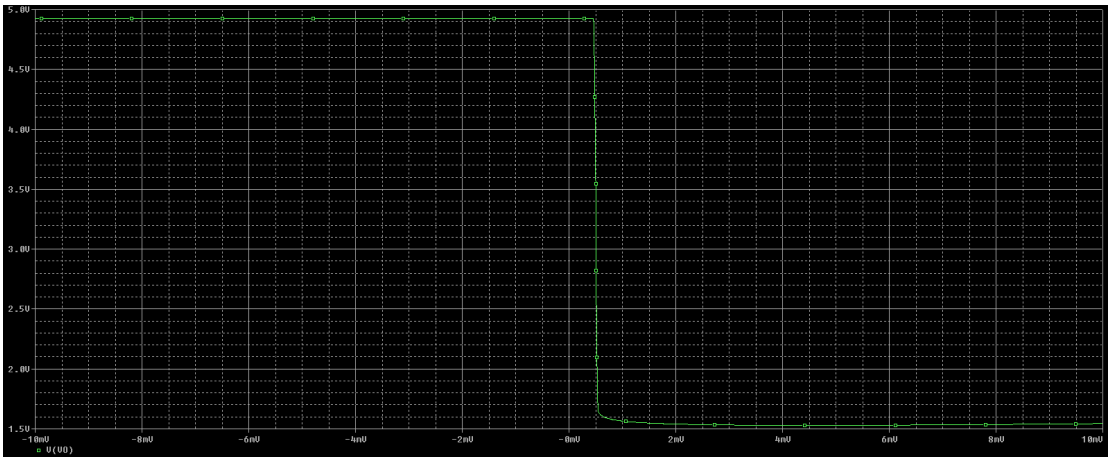

Figure 4: Full sweep from a differential of -10 mV to 10 mV, note that the voltage is held to either the positive or negative rails for most of the sweep. Also note that the transition is very sharp and looks almost instant.

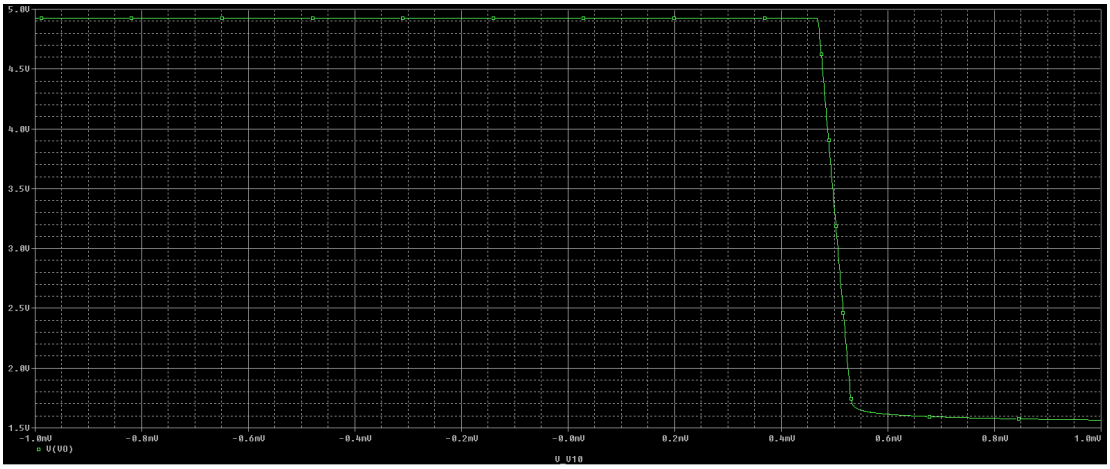

Figure 5: A zoomed in portion of the previous plot from a differential of -1 mV to 1 mV. Now the transition shows some linearity in the

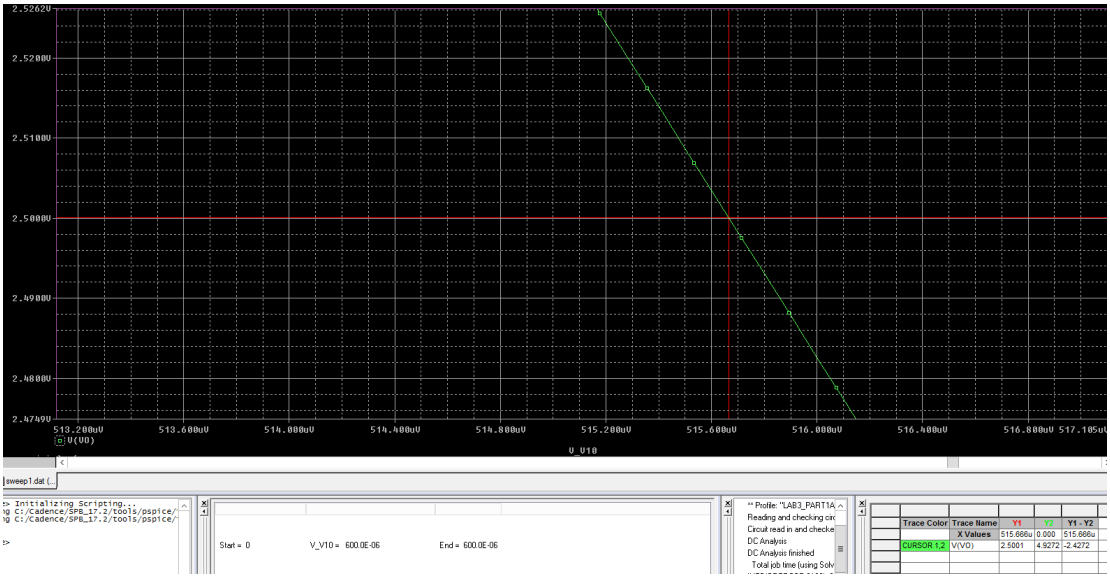

Figure 6: Zoomed in on the point where the output is half the supply range (2.5V) to find the required offset of V_d.

As seen in figure 6 the offset voltage for equal input voltages to give a midpoint output is 515.67μV, this is very close to the assumed calculated midpoint value of 0V.

A possible reason for the discrepancy would be that if the value of V_{BE} on the current mirror is not 0.6V, the reference current would be different and therefore the base current would be different as well.

Also from the above figures, the output swing can be observed to go almost up to the positive rail at 4.8V and down to 1.5V above the negative supply which in this case is ground.

The gain of the opamp can be found from the slope of the line in the transition region. In the third figure, a run of $0.7\mu V$ was found to correlate with a rise of $36mV$, this correlates to a slope, and therefore gain, of $51.4\frac{kV}{V}$.

The range calculated in the prelab is from 1.2V to 5V. The actual range is close to this value.

A possible reason for the difference is some transistors are transitioning from saturation to active mode, making predictions assuming all transistors are in the active mode incorrect. Also the gain and frequency response is likely quite different than expected on the edge of the range due to significantly due to being on the edge of saturation.

4.2 Common mode range

sing the voltage offset found earlier, the inputs were kept at a constant differential and their values were swept from 0V to 5V to find the common mode gain. The output is plotted in the following figure:

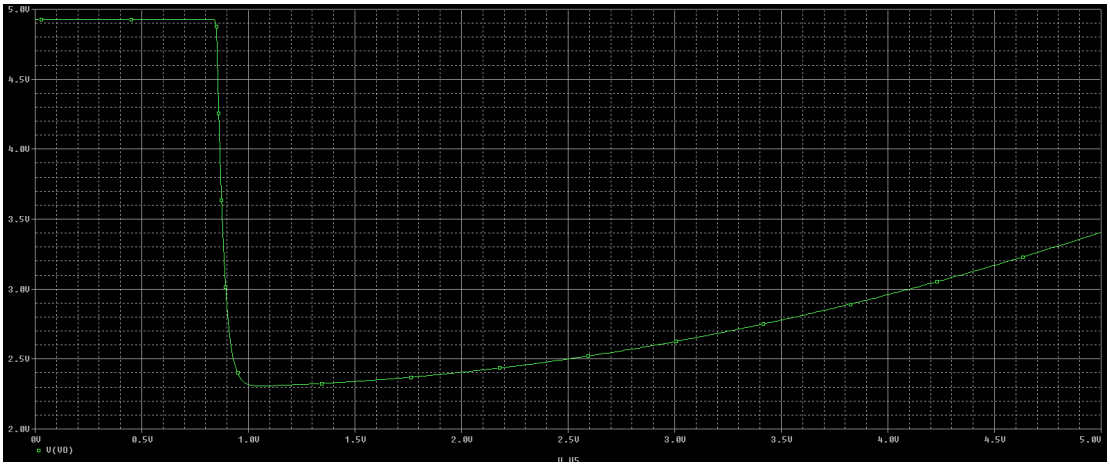

Figure 7: Output voltage vs common input voltage.

From figure above, the common-mode range is from 1V to 5V. Over the range, the output changes from 2.3V to 3.4V. It's likely that the effective range ends a little below 5V (probably by 0.6V to 0.5V) and it's not shown on the output, this would be as the transistors in the input stage, Q_1 and Q_2, transitioning from active mode to saturation mode. A better way to test this would be to sweep the offset of a differential sine wave though the amplifier and plot the gain over the range.

The asymmetry in both the common-mode range and the output swing comes from the circuit. There are more transistor drops between the input and ground than between the input and power. In particular, the transistors Q_7, Q_{23} and the secondary stage transistors Q_{16} and Q_{17} cause this asymmetry.

The common mode range from the simulations was determined to be from 1V to 5V compared to the range of 1.2V to 4.4V. The likely cause of the difference is that some transistors continued to work close to as expected into their saturation range. This would however greatly change the performance parameters of the opamp for signals in this range.

4.3 DC Operating Point

A DC operating point of the circuit was done and the complete results are tabulated in appendix A. A summary of the values calculated for the prelab and the difference to the simulated value are tabulated in the following table :

Q	I_C Exp. (μA)	I_C Theo. (μA)	% Error	R_o Exp. (MΩ)	R_o Theo. (MΩ)	g_m Exp. (mS)	g_m Theo. (mS)	r_π Exp. (kΩ)	r_π Theo. (kΩ)
1	10.40	10.50	0.95	1.92	1.90	0.42	0.42	240.38	238.10
2	10.40	10.50	0.95	1.92	1.90	0.42	0.42	240.38	238.10
5	10.20	10.30	0.97	7.84	7.77	0.41	0.41	245.10	242.72
6	10.20	10.30	0.97	7.84	7.77	0.41	0.41	245.10	242.72
7	11.30	13.40	15.67	7.08	5.97	0.45	0.54	221.24	186.57
14	559.00	1140.00	50.96	0.14	0.07	22.36	45.60	4.47	2.19
16	11.20	13.20	15.15	7.14	6.06	0.45	0.53	223.21	189.39
17	19.00	626.00	96.96	4.21	0.13	0.76	25.04	131.58	3.99
20	720.00	1170.00	38.46	0.03	0.02	28.80	46.80	3.47	2.14
23	0.01	200.20	99.99	1526.72	0.10	0.00	8.01	∞	12.49

Table 2: Summary of calculated theoretical compared to experimental DC values

Most of the obtained DC values were very close to the calculated as seen in the percent error column. Q_{17} had a very large error compared to the theoretical as it was observed to be much smaller than expected, This seems to be a cascaded effect from Q_{16} providing a slightly different bias voltage, as well as Q_{23} outputting a much different base current. Q_{23} was found to be nearly cut-off, as the current was nearly zero. This is caused from the fact that it had a much different V_{BE} than expected.

4.4 Revised Gain Calculations

Using the obtained DC operating point data, a revised value for the gain of the opamp can be found. We can start by calculating the value R_{in2} such that A_{v1} can be found.

$$R_{in} = \beta(r_{e16} + r_{o16} \parallel R_9 \parallel (r_{\pi 17} + (1+\beta)R_8)) \tag{66}$$
$$= 3.68M\Omega \tag{67}$$

$$A_{v1} = (R_L \parallel r_{o6} \parallel r_{o2})g_{m2} \tag{68}$$
$$= 456\frac{V}{V} \tag{69}$$

Next the value for the second stage, The R_L will be assumed to be infinity due to the misbehaviour of Q_{23}.

$$A_{v2} = -g_{m17}(R_L \parallel R_{12})\frac{(1+\beta)R_8}{r_{\pi 17} + (1+\beta)R_8} \tag{70}$$
$$= 214\frac{V}{V} \tag{71}$$

$$A_v = A_{v1}A_{v2} = 214\frac{V}{V}456\frac{V}{V} = 98\frac{kV}{V} \tag{72}$$

This gain is much higher than was expected. This may actually be the case and the output buffer could have a lower than unity gain. From the DC op point, the buffer did seem to have significantly different parameters than expected.

5 Results & Analysis

5.1 Frequency Response

The gain and phase response of the opamp was swept from 1 Hz to 10 MHz and the results are shown in the following figure:

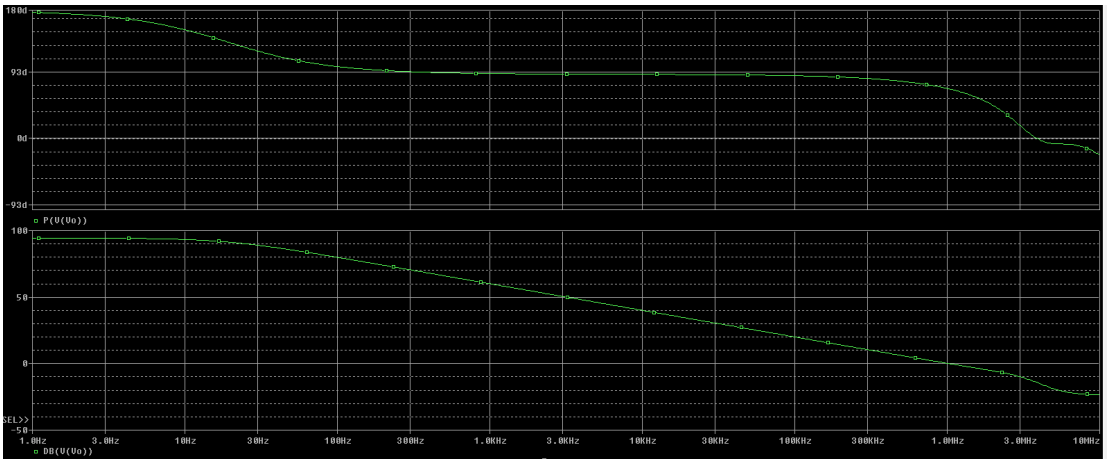

Figure 8: Gain and phase response of the opamp.

The gain starts out around 94 dB, then it starts to go down at a rate of 20 dB/decade starting around 10 Hz. The unity gain point is accurately measure in the next figure:

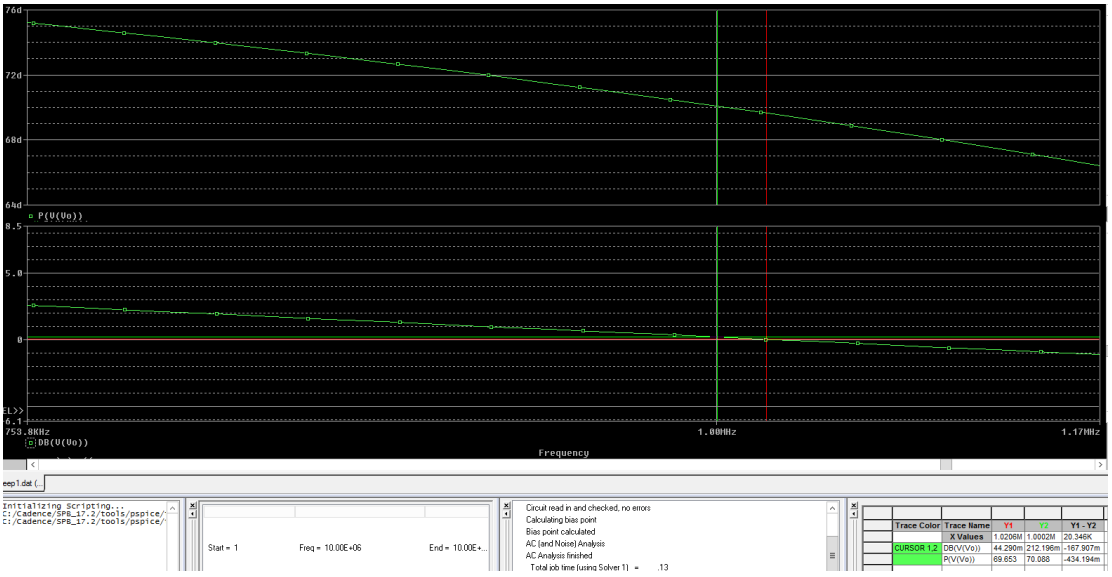

Figure 9: Measurement of unity gain of the opamp.

The unity gain point was measure to be 1.02 MHz At exactly 1 MHz, the gain is 0.21 dB. This will be discussed further in subsection 5.3.

5.2 Slew Rate

Using the differential offset found the part one, a square wave was put through the opamp configured as a buffer to measure the slew rate. The following plots show the results:

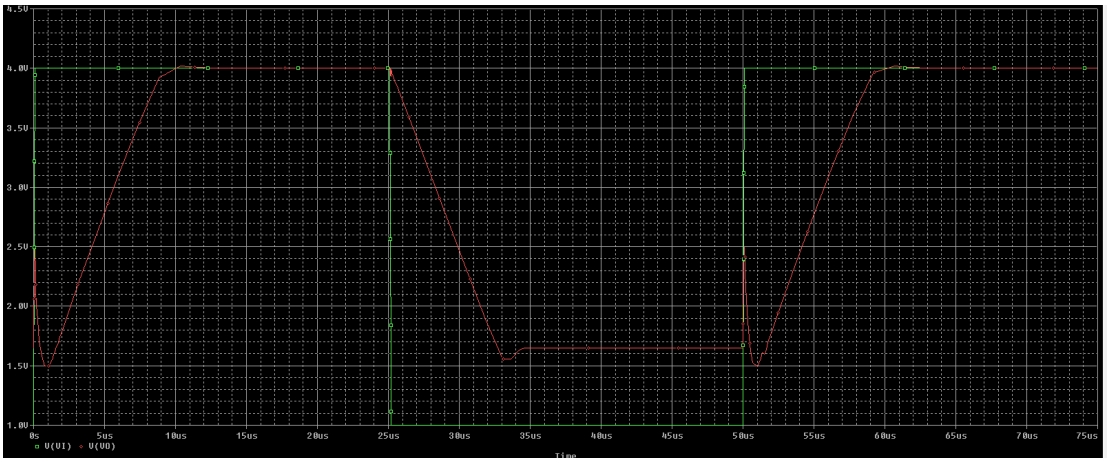

Figure 10: Plot of the input square wave (green) and the output square wave (red) through the opamp in a buffer configuration.

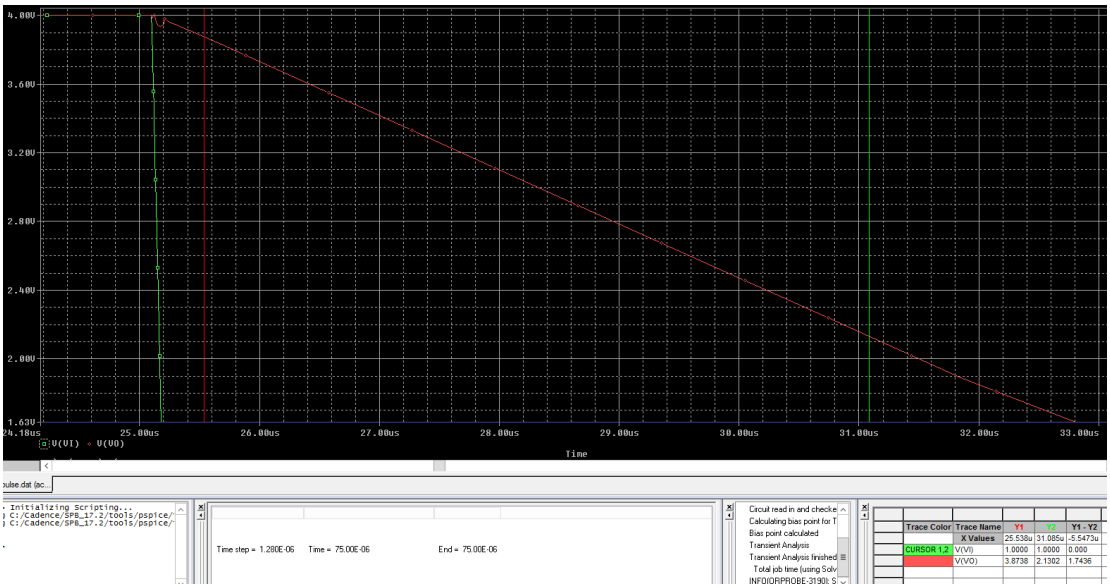

Figure 11: Zoomed in on the falling edge of the square wave with raw measurements shown.

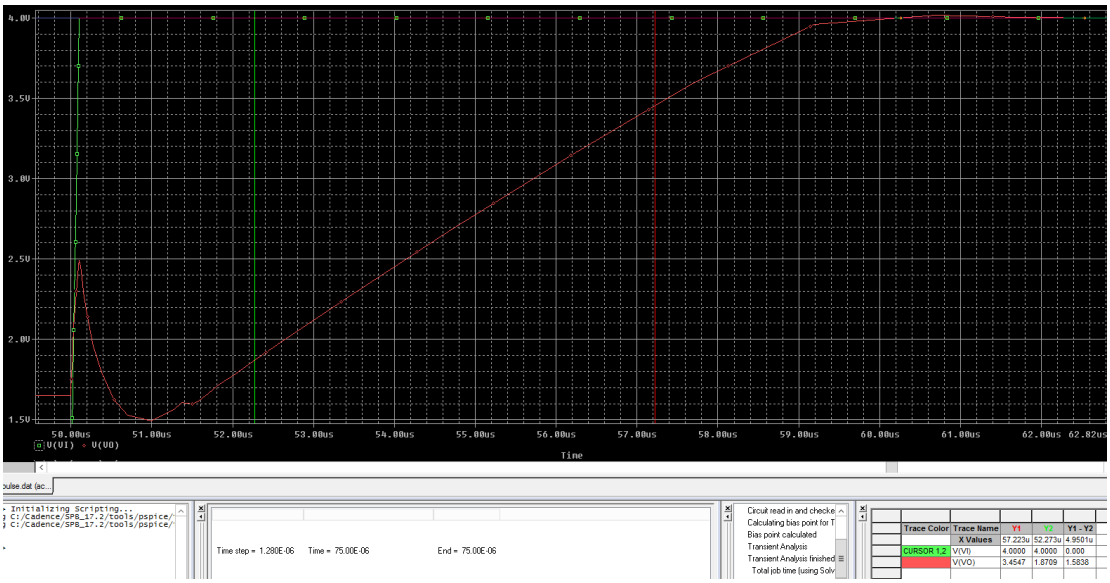

Figure 12: Zoomed in on the rising edge of the square wave with raw measurements shown.

From figure 11, the output falls by -1.7436V in $5.5473\mu s$. This gives a slew rate of $-314.3\frac{kV}{s}$.

From figure 12, the output rises by 1.5838V in $4.9501\mu s$. This gives a slew rate of $320.0\frac{kV}{s}$.

This is because the series resistance of the transistor that charge the internal capacitor are smaller on the charging side than on the discharge side.

To charge the capacitor, current must flow through Q_2 which has a series resistance of 1.90Ω from the prelab calculations.

To discharge the capacitor, current flows through Q_6 and Q_{16}. Q_6 has a series resistance of 7.77Ω. Q_{16} is affected by the miller effect, this would affect the RC time constant therefore rather than changing the capacitor values, for the purposes of this comparison, the resistor value can be multiplied by the gain. The revised gain of the second stage is 214 so the effective resistance is 24Ω. In parallel this works out to roughly 5.4Ω.

While this comparison is very loose and inaccurate, it does show that the magnitude of the resistance on the high driving side is lower than the low side. To properly do this comparison, the DC operating points would have to be taken for both the high state and the low state and the effective resistance on the capacitor to ground would have to be derived in full.

We decided to reduce the capacitor to $1pF$ to see what would happen, both in terms of stability and the slew rate. We expected the slew rate to increase but it may make the output unstable due to the high frequency components of the square wave that it was being fed. The following figure shows the results.

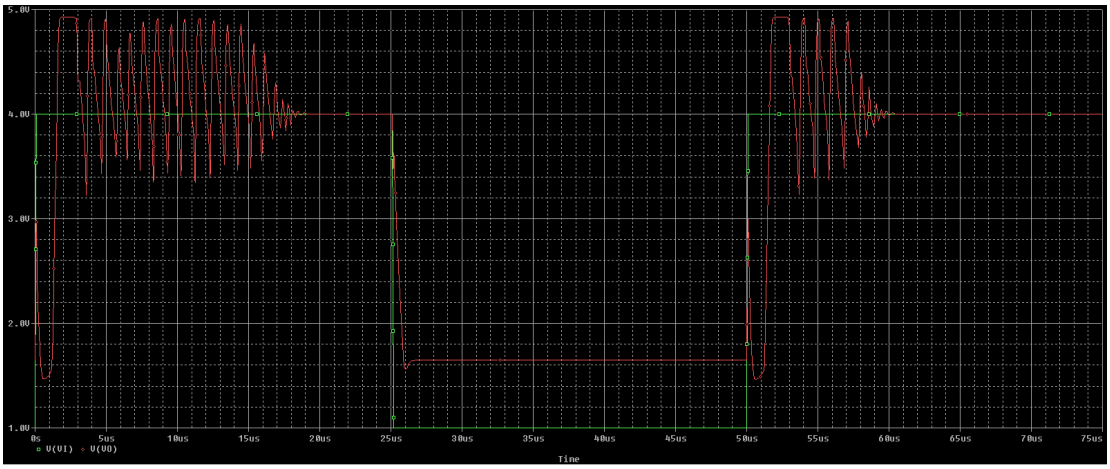

Figure 13: Slew rate test with the capacitor set to $1pF$.

As seen in figure 13, the slew rate has increased with a reduction of the capacitor size. There is also significant ringing on the high side but not on the low side. This could be due to the uneven resistances for the charge and discharge making the charging side unstable but leaving the low side just on the edge of being stable. Another possibility is that the transistors are too far into the saturation mode on the low side for the assumed parameter to be true and the ringing is eliminated.

The next figure shows what happens when the capacitor value is made to be $1fF$, at this point it's probably less than the parasitic capacitance from the transistors.

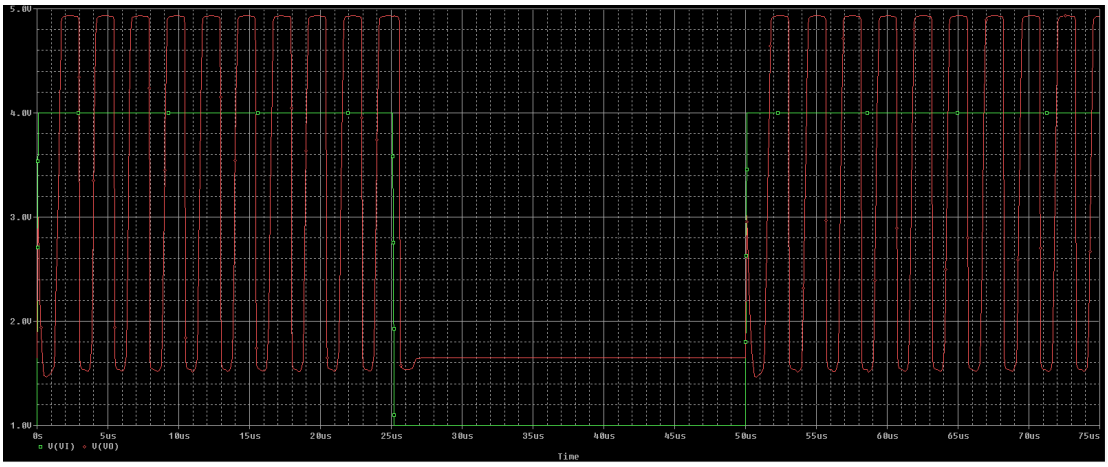

Figure 14: Slew rate test with the capacitor set to $1fF$.

As seen in the figure above, the slew rate increased again but the output is now completely useless. On the high side there is only oscillation and on the low side it's still flat. This indicates that the later of the two theories for the asymmetric ringing is true, where the transistor are too far into saturation and it dampens the system.

5.3 Comparison of unity gain as measured to theoretical

The unity gain point was only 20 kHz away from the theoretical value of 1 MHz. This is just a 2% difference.

6 Conclusion

The hand calculations were in a reasonable approximation of the simulated results. The main cause of error was the assumption that all the transistors are in active mode with a V_{BE} of 0.6V.

From simulations, the output swing was determined to be from 1.0V to 4.8V, the theoretical range was 1.2V to 5V.

The common mode range from the simulations was determined to be from 1V to 5V compared to the range of 1.2V to 4.4V.

The DC operating parameters were quite close to the theoretical values when the assumption of active mode with $V_{BE} = 0.6V$. For the transistors were this is not the case, there was a large discrepancy between the theoretical values and the actual values.

The theoretical gain was found to be $46\frac{kV}{V}$ and the experimental value was found to be $51\frac{kV}{V}$.

The frequency response was as expected. Large gain initially with a large pole at around 10 Hz dropping the gain at 20 dB/decade until 1 MHz. The unity gain point was only 20 kHz away from the theoretical value of 1 MHz.

The slew rate was found to be $-314\frac{kV}{V}$ for the falling edge and $320\frac{kV}{V}$ for the rising edge. This is close to the calculated value of $310\frac{kV}{V}$. Interestingly, the rising and falling edges were not the same due to asymmetry in the charge and discharge circuits.

Using a small capacitor value affected the stability of the opamp, $1pF$ caused a lot of ringing and $1fF$ caused oscillation. This only occurred on the high side, on the low side the output remained flat likely due to the saturating transistors causing a damping effect.

A DC Operating Point

```
**** 11/10/16 15:46:32 ******* PSpice Lite (March 2016) ******* ID#
    10813 ****

 ** Profile: "LAB3_PART1AND3-sweep1"  [ H:\3A\Elec 2\Lab 3\
     ELEC3509_Lab3_Fall2011\ELEC3509_Lab3_Fall2011\Part1&3\
     LAB3_PART1AND3-PSpic


 ****      CIRCUIT DESCRIPTION


*******************************************************************************




** Creating circuit file "sweep1.cir"
** WARNING: THIS AUTOMATICALLY GENERATED FILE MAY BE OVERWRITTEN BY
    SUBSEQUENT SIMULATIONS

*Libraries:
* Profile Libraries :
* Local Libraries :
* From [PSPICE NETLIST] section of C:\SPB_Data\cdssetup\OrCAD_PSpice
    \17.2.0\PSpice.ini file:
.lib "nomd.lib"

*Analysis directives:
.OP
.OPTIONS ADVCONV
.PROBE64 V(alias(*)) I(alias(*)) W(alias(*)) D(alias(*)) NOISE(alias
    (*))
.INC "..\LAB3_PART1AND3.net"



**** INCLUDING LAB3_PART1AND3.net ****
* source LAB3_PART1AND3
R_R1            0 N00455  1k
R_R10            0 VO  1MEG
R_R2            0 N00443  1k
R_R6            VO N00539  30
E_E1            N00379 N00371 N00463 0 0.5
R_R7            N001372 VO  30
V_V2            N00413 N00419 1.4V
E_E2            N00371 N00381 N00463 0 0.5
```

```
R_R13           N00413 N00387  90k
V_V5            N00371 0 2.5V
R_R8            0 N00435  100
I_I1            N00387 N00425 DC 19uA
R_R9            0 N00437  50k
I_I2            N00387 N00527 DC 550uA
V_V1            N00387 0 5V
I_I3            N00387 N00413 DC 180uA
R_R11           N00425 N00387  1MEG
R_R3            0 N00445  50k
V_V9            N00463 N000951 DC 0V AC 0V
R_R5            0 N00463  1k
V_V10           N000951 0 0
R_R12           N00527 N00387  30k
C_C1            N00515 N00527  100p
Q_Q14           N00387 N00413 N00539 Q2N3904
Q_Q20           0 N00419 N001372 Q2N3906
Q_Q23           0 N00527 N00419 Q2N3906
Q_Q17           N00527 N00437 N00435 Q2N3904
Q_Q16           N00387 N00515 N00437 Q2N3904
Q_Q1            N00457 N00379 N00425 Q2N3906
Q_Q2            N00515 N00381 N00425 Q2N3906
Q_Q7            N00387 N00457 N00445 Q2N3904
Q_Q5            N00457 N00445 N00455 Q2N3904
Q_Q6            N00515 N00445 N00443 Q2N3904

**** RESUMING sweep1.cir ****
.END


**** 11/10/16 15:46:32 ******* PSpice Lite (March 2016) ******* ID#
    10813 ****

 ** Profile: "LAB3_PART1AND3-sweep1"  [ H:\3A\Elec 2\Lab 3\
    ELEC3509_Lab3_Fall2011\ELEC3509_Lab3_Fall2011\Part1&3\
    LAB3_PART1AND3-PSpic


 ****       BJT MODEL PARAMETERS


********************************************************************************



                Q2N3904           Q2N3906
                NPN               PNP
       LEVEL    1                 1
          IS    6.734000E-15      1.410000E-15
```

BF	416.4	180.7
NF	1	1
VAF	74.03	18.7
IKF	.06678	.08
ISE	6.734000E-15	
NE	1.259	
BR	.7371	4.977
NR	1	1
ISS	0	0
RB	10	10
RE	0	0
RC	1	2.5
CJE	4.493000E-12	8.063000E-12
VJE	.75	.75
MJE	.2593	.3677
CJC	3.638000E-12	9.728000E-12
VJC	.75	.75
MJC	.3085	.5776
XCJC	1	1
CJS	0	0
VJS	.75	.75
TF	301.200000E-12	179.300000E-12
XTF	2	6
VTF	4	4
ITF	.4	.4
TR	239.500000E-09	33.420000E-09
XTB	1.5	1.5
KF	0	0
AF	1	1
CN	2.42	2.2
D	.87	.52

**** 11/10/16 15:46:32 ******* PSpice Lite (March 2016) ******* ID# 10813 ****

** Profile: "LAB3_PART1AND3-sweep1" [H:\3A\Elec 2\Lab 3\ ELEC3509_Lab3_Fall2011\ELEC3509_Lab3_Fall2011\Part1&3\ LAB3_PART1AND3-PSpic

**** SMALL SIGNAL BIAS SOLUTION TEMPERATURE = 27.000 DEG C

****

```
 NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE
    VOLTAGE

(   VO)    4.9272  (N00371)    2.5000 (N00379)    2.5000 (N00381)
    2.5000

(N00387)    5.0000 (N00413)    5.6128 (N00419)    4.2128 (N00425)
    3.0858

(N00435)     .0019 (N00437)     .5585 (N00443)     .0104 (N00445)
     .5570

(N00455)     .0104 (N00457)    1.1051 (N00463)    0.0000 (N00515)
    1.1064

(N00527)   20.9290 (N00539)    4.9493 (N000951)    0.0000

(N001372)    4.9053



    VOLTAGE SOURCE CURRENTS
    NAME            CURRENT

    V_V2          -3.311E-06
    V_V5           1.072E-07
    V_V1          -7.949E-04
    V_V9           0.000E+00
    V_V10          0.000E+00

    TOTAL POWER DISSIPATION    3.98E-03  WATTS


**** 11/10/16 15:46:32 ******* PSpice Lite (March 2016) ******* ID#
    10813 ****

 ** Profile: "LAB3_PART1AND3-sweep1"  [ H:\3A\Elec 2\Lab 3\
    ELEC3509_Lab3_Fall2011\ELEC3509_Lab3_Fall2011\Part1&3\
    LAB3_PART1AND3-PSpic


 ****     OPERATING POINT INFORMATION      TEMPERATURE =   27.000 DEG
     C

**********************************************************************
```

**** VOLTAGE-CONTROLLED VOLTAGE SOURCES

NAME	E_E1	E_E2
V-SOURCE	0.000E+00	0.000E+00
I-SOURCE	5.358E-08	-5.358E-08

**** BIPOLAR JUNCTION TRANSISTORS

NAME	Q_Q14	Q_Q20	Q_Q23	Q_Q17	Q_Q16
MODEL	Q2N3904	Q2N3906	Q2N3906	Q2N3904	Q2N3904
IB	1.77E-04	-3.31E-06	4.30E-12	2.14E-07	1.62E-07
IC	5.59E-04	-7.28E-04	-1.31E-11	1.90E-05	1.12E-05
VBE	6.63E-01	-6.93E-01	1.67E+01	5.57E-01	5.48E-01
VBC	6.13E-01	4.21E+00	2.09E+01	-2.04E+01	-3.89E+00
VCE	5.07E-02	-4.91E+00	-4.21E+00	2.09E+01	4.44E+00
BETADC	3.17E+00	2.20E+02	-3.06E+00	8.88E+01	6.92E+01
GM	2.78E-02	2.79E-02	-2.25E-13	7.35E-04	4.34E-04
RPI	4.56E+03	7.81E+03	1.81E+14	1.46E+05	1.93E+05
RX	1.00E+01	1.00E+01	1.00E+01	1.00E+01	1.00E+01
RO	2.10E+02	3.15E+04	4.27E+11	4.96E+06	6.94E+06
CBE	1.62E-11	1.86E-11	2.53E-12	6.27E-12	6.15E-12
CBC	1.17E-09	3.27E-12	1.39E-12	1.30E-12	2.07E-12
CJS	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
BETAAC	1.27E+02	2.18E+02	-4.07E+01	1.07E+02	8.37E+01
CBX/CBX2	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
FT/FT2	3.75E+06	2.03E+08	-9.13E-03	1.55E+07	8.39E+06

NAME	Q_Q1	Q_Q2	Q_Q7	Q_Q5	Q_Q6
MODEL	Q2N3906	Q2N3906	Q2N3904	Q2N3904	Q2N3904
IB	-5.36E-08	-5.36E-08	1.63E-07	1.56E-07	1.56E-07
IC	-1.04E-05	-1.04E-05	1.13E-05	1.02E-05	1.02E-05
VBE	-5.86E-01	-5.86E-01	5.48E-01	5.47E-01	5.47E-01
VBC	1.39E+00	1.39E+00	-3.89E+00	-5.48E-01	-5.49E-01
VCE	-1.98E+00	-1.98E+00	4.44E+00	1.09E+00	1.10E+00
BETADC	1.94E+02	1.94E+02	6.93E+01	6.57E+01	6.57E+01
GM	4.02E-04	4.02E-04	4.36E-04	3.96E-04	3.96E-04
RPI	4.83E+05	4.83E+05	1.92E+05	2.01E+05	2.01E+05
RX	1.00E+01	1.00E+01	1.00E+01	1.00E+01	1.00E+01
RO	1.93E+06	1.93E+06	6.90E+06	7.28E+06	7.28E+06
CBE	1.26E-11	1.26E-11	6.15E-12	6.14E-12	6.14E-12
CBC	5.30E-12	5.30E-12	2.07E-12	3.07E-12	3.07E-12

CJS	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
BETAAC	1.94E+02	1.94E+02	8.37E+01	7.94E+01	7.94E+01
CBX/CBX2	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
FT/FT2	3.57E+06	3.57E+06	8.44E+06	6.84E+06	6.84E+06

JOB CONCLUDED

**** 11/10/16 15:46:32 ******* PSpice Lite (March 2016) ******* ID# 10813 ****

** Profile: "LAB3_PART1AND3-sweep1" [H:\3A\Elec 2\Lab 3\ ELEC3509_Lab3_Fall2011\ELEC3509_Lab3_Fall2011\Part1&3\ LAB3_PART1AND3-PSpic

**** JOB STATISTICS SUMMARY

****

Total job time (using Solver 1) = .06