数字电路与数字系统实验

实验四

触发器和锁存器

计算机科学与技术系

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一、实验目的

本次实验的目的是复习锁存器和触发器的工作原理，复习时序电路中电路时序图的分析和阅读。学习如何对时序电路进行仿真，了解 Verilog 语言中阻塞赋值语句和非阻塞赋值语句的区别。

（一）分析阻塞和非阻塞 RTL 视图和仿真结果

请建立两个工程，分别研究阻塞赋值和非阻塞赋值的 RTL 级视图和仿真结果，步骤如下：

1. 新建工程，用阻塞赋值语句设计两个触发器；保存 Verilog 语言文件。
2. 在 Tools 栏，点击 Netlist Viewers 栏下的 RTL Viewer 查看生成的 RTL Schematic，看看在用阻塞赋值语句生成两个触发器的实际电路原理。
3. 新建另一个工程，用非阻塞赋值语句实现两个触发器，重复上述步骤，比较两种触发器实现方式在硬件电路实现上的异同。

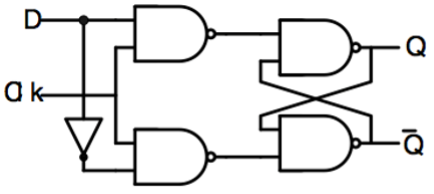
（二）设计一个同步清零和一个异步清零的 D 触发器

查阅资料，分析同步清零和异步清零的不同，并请在一个工程中设计两个触发器，一个是带有异步清零端的 D 触发器，而另一个是带有同步清零端的 D 触发器。

二、实验原理（知识背景）

1、D 锁存器：

RS 锁存器中有一个 Q 和 Q 同时为 1 的无效状态，这是 R 和 S 同时为 1 的缘故，如果强制 R 和 S 总是相反的逻辑，就可以避免这一现象产生。如图所示，这个电路就是 D 锁存器电路，当时钟触发信号为 0 时，输出保持不变，当时钟触发信号为 1 时，Q 输出 D 的值，即 Q 随着 D 值的改变而改变。

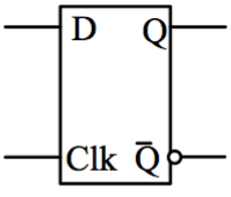


(a) 电路原理图

Clk	D	Q	Q̄
0	×	q_0	$\bar{q}_0$
1	0	0	1
1	1	1	0

保持
D
D

(b) 真值表

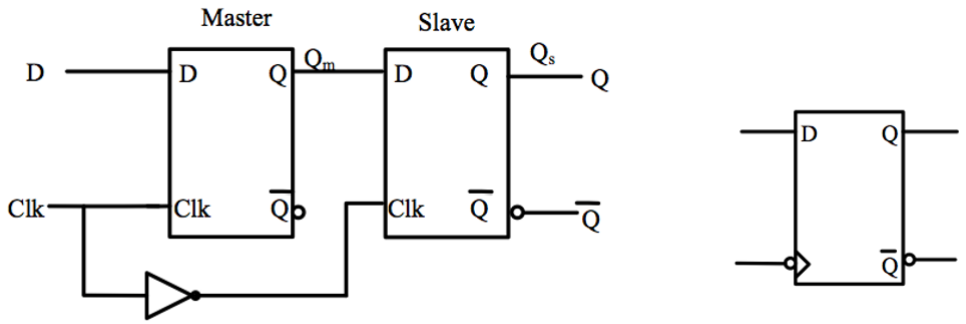


(c) 模块框图

2、时钟边沿触发的 D 触发器

前面讨论的锁存器都是在时钟为高电平（也可以设计为低电平）时触发的，如果我们希望锁存器只在时钟的特定时刻（如上升沿或者下降沿）触发，锁存此时刻 D 的值，这样的锁存器通常称为时钟边沿触发的触发器

用两个锁存器可以构成触发器，如图所示。图中的两个 D 锁存器，前者为主锁存器，后者为从锁存器，当 Clk 信号为 1 时，主锁存器的 Qm 随着 D 的变化而变化，从锁存器的状态保持不变。当时钟信号变为 0 后，主锁存器的状态不再变化，从锁存器 Qs 的状态则跟随 Qm 状态的变化而变化，由于当 Clk=0 时，Qm 不会发生变化，因此对于外部的观察者而言，在一个时钟周期内 Q 只在 Clk 从 1 变为 0（即时钟的负跳变沿或下降沿）的时候发生一次变化。因此，我们也可以说输出信号 Q 是在时钟下降沿采集到的输入信号 D 的瞬间值。



(a) 电路原理图　　(b) 模块框图

3、模块实例化

一个模块能够在另外一个模块中被引用， 这样就建立了描述的层次。模块实例化语句形式如下：

module_name instance_name(port_associations) ;

连接信号到模块端口：

有两种常用的方法将信号连接到端口上：位置和名称。

位置

通过位置将信号连到端口上的语法应该比较熟悉，因为这是类 c 语言的语法。当实例化一个模块时，根据这个模块声明时的端口顺序从左到右写下来。举个例子：

mod_a instance1 (wa, wb, wc);

这实例化了一个模块 mod_a 并且起了一个实例名 instance1。这种语法有一个缺点，如果模块端口列表发生改变，所有这个模块的实例也必须被找到并且改成和新的相匹配。

名称

通过名称将信号连接到模块的端口，即使端口列表发生更改，也可以保持正确连接。但是这个语法更冗长。

mod_a instance2 (.out(wc), .in1(wa), .in2(wb));

注意端口的顺序在这里是不相关的，无论它在子模块的端口列表中的位置如何，都将连接到正确的名称。还请注意此语法中紧靠端口名称前面的英文句号“.”。

根据名称连接是最常用也是最方便的，在给实例起名时推荐用原端口名_u0，多次调用数字增长。例如：

```
mod_a mod_a_u0 ( .out(wc), .in1(wa), .in2(wb) );
mod_a mod_a_u1 ( .out(wc), .in1(wa), .in2(wb) );etc
```

三、实验环境/器材等

1) 软件环境：

Quartus (Quartus Prime 17.1) Lite Edition

2) 硬件环境：

DE10-Standard 开发板

FPGA 部分：

Intel Cyclone V SE 5CSXFC6D6 F31C6N

- 110K 逻辑单元
- 5,761Kbit RAM

HPS 部分：

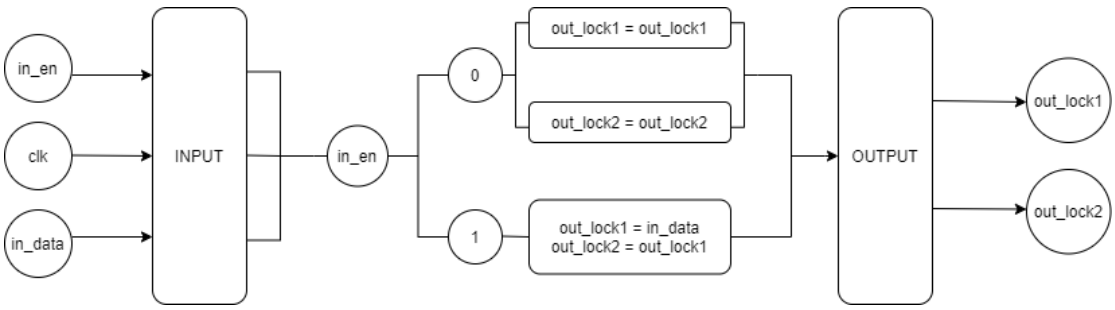
Dual-core ARM Cortex A9

- 925MHz
- 1GB DDR

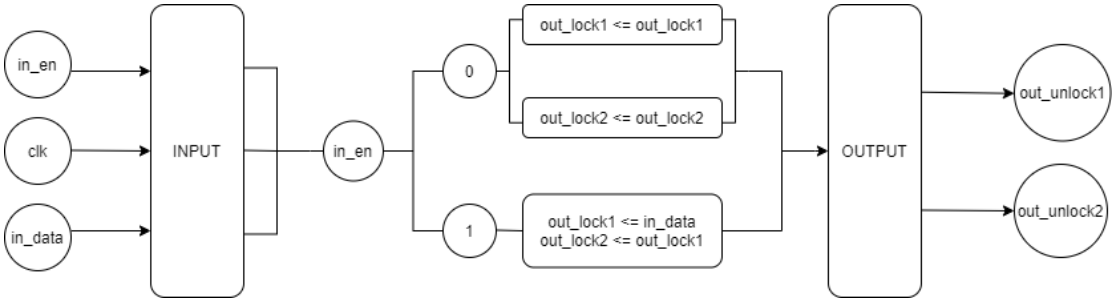
四、程序代码或流程图

（一）

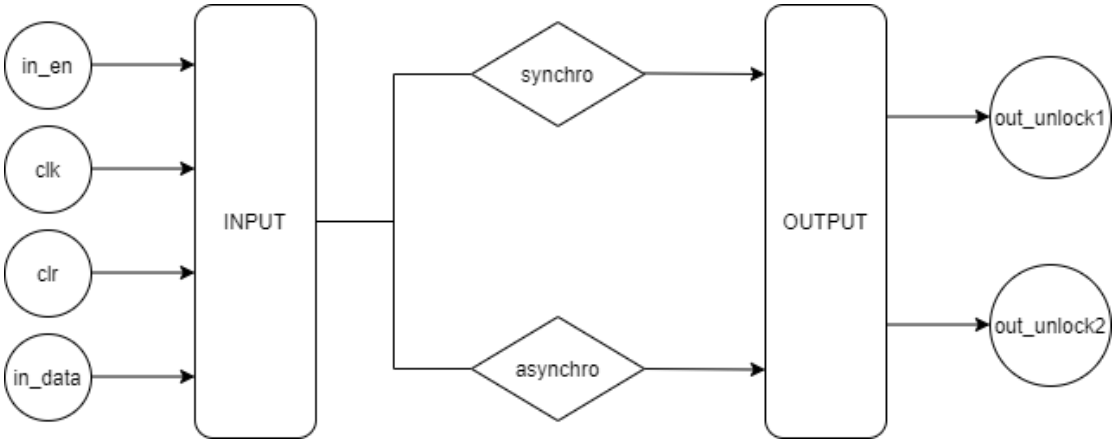
阻塞：



非阻塞:

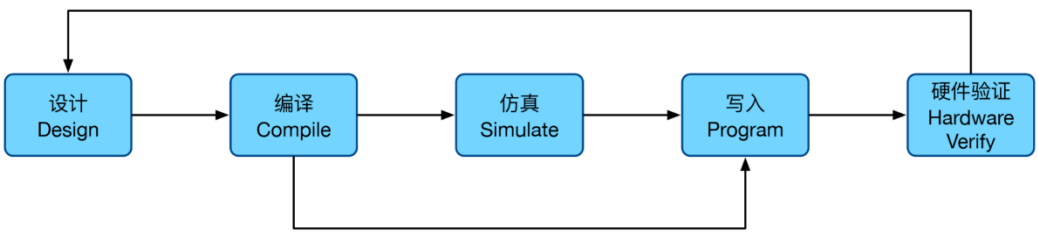


（二）



五、实验步骤/过程

（一）



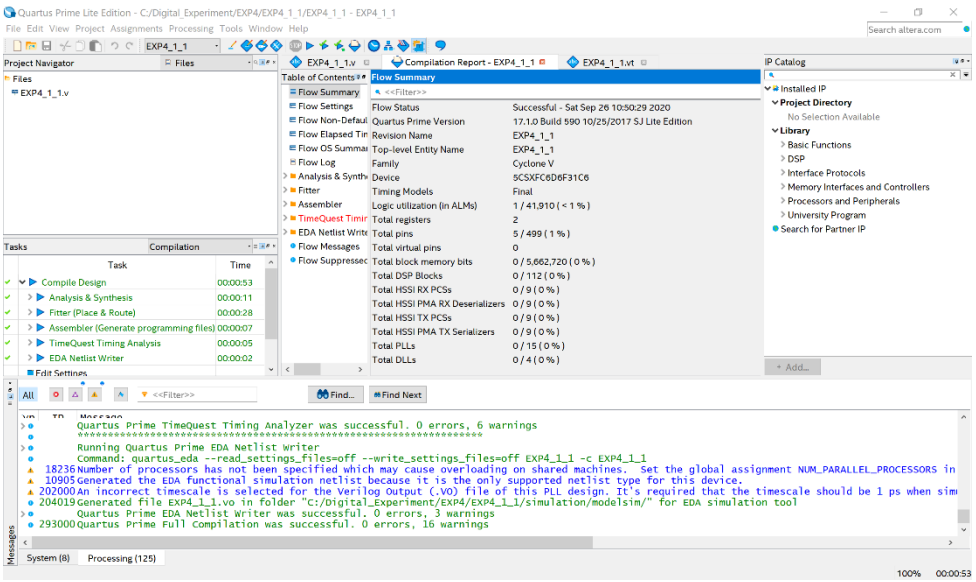
设计：

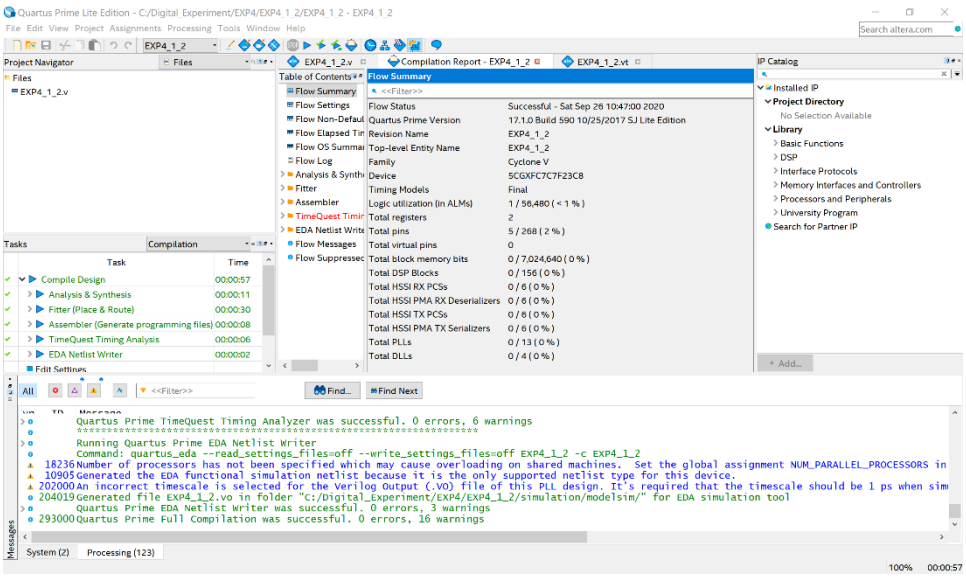
```
module EXP4_1_1(in_data, clk, in_en, out_lock1, out_lock2);
    input in_data;
    input clk;
    input in_en;

    output reg out_lock1;
    output reg out_lock2;

    always @ (posedge clk)

      if(in_en)
        begin
          out_lock1 = in_data;
          out_lock2 = out_lock1;
        end
      else
        begin
          out_lock1 = out_lock1;
          out_lock2 = out_lock2;
        end

endmodule

module EXP4_1_2(in_data, clk, in_en, out_unlock1, out_unlock2);
    input in_data;
    input clk;
    input in_en;

    output reg out_unlock1;
    output reg out_unlock2;

    always @ (posedge clk)

      if(in_en)
        begin
          out_unlock1 <= in_data;
          out_unlock2 <= out_unlock1;
        end
      else
        begin
          out_unlock1 <= out_unlock1;
          out_unlock2 <= out_unlock2;
        end

endmodule
```

测试：

```
initial
begin
// code that executes only once
// insert code here --> begin
      clk = 0; in_data = 0; in_en = 0; #7;
               in_data = 0; #7;
               in_data = 1; #7;
               in_data = 0; #7;
               in_data = 1; #7;
      in_en = 1; #7;
               in_data = 0; #7;
               in_data = 1; #7;
               in_data = 0; #7;
               in_data = 1; #7;
      $stop;
end

always
begin
#5 clk = ~clk;
// --> end
//$display("Running testbench");
end
```

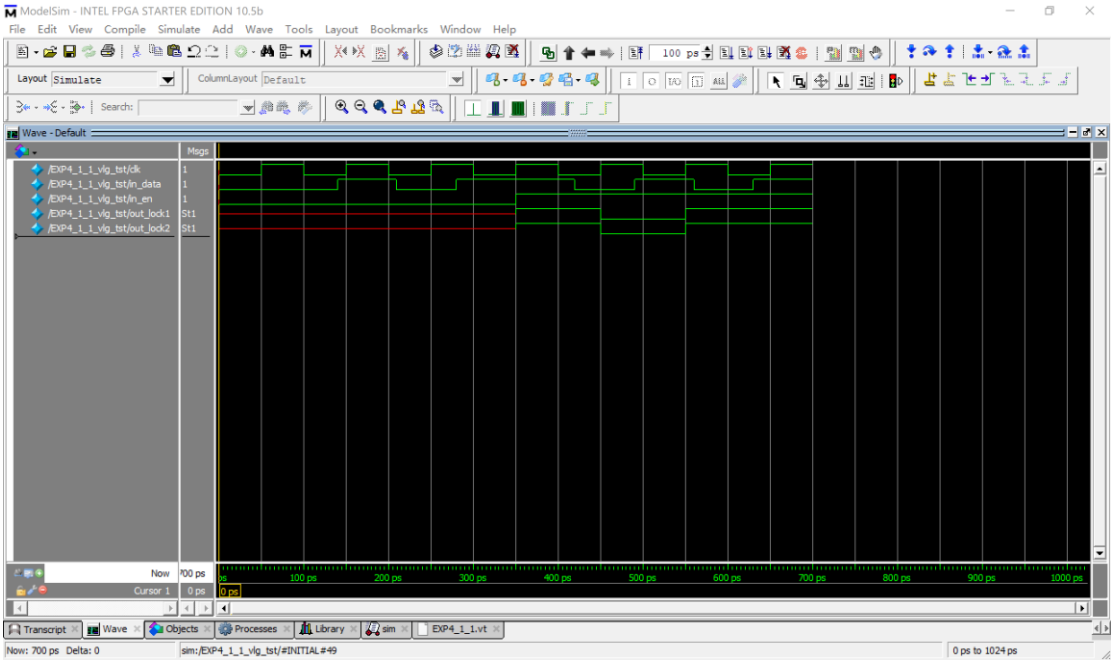
编译：

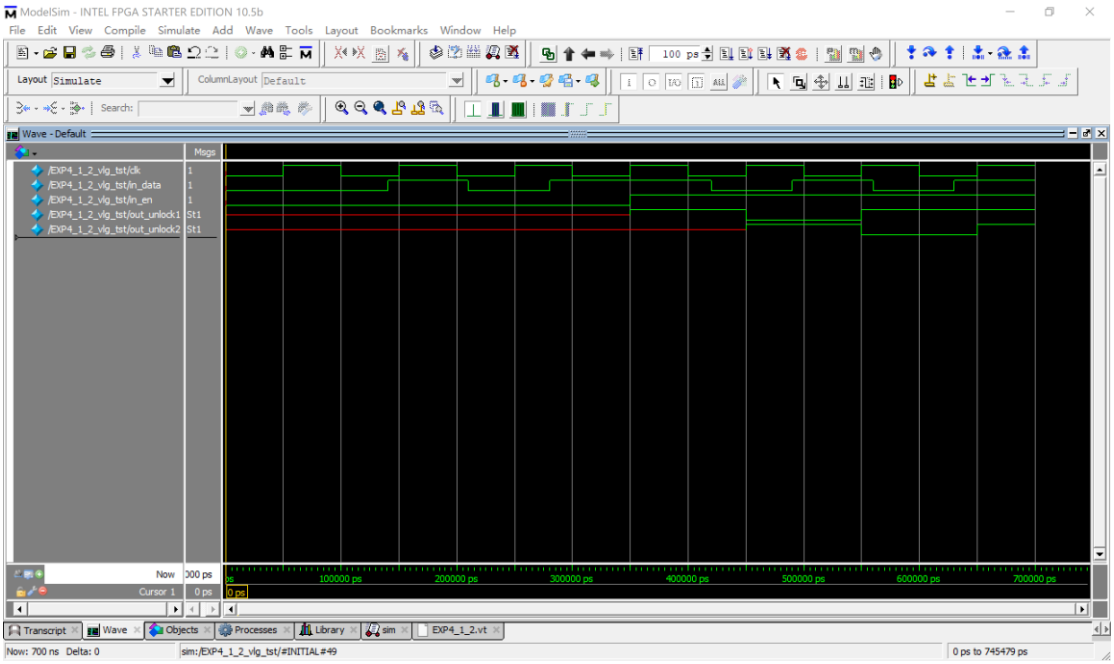

Quartus Prime Lite Edition - C:/Digital_Experiment/EXP4/EXP4_1_1/EXP4_1_1 - EXP4_1_1
Flow Summary
Flow Status Successful - Sat Sep 26 10:50:29 2020
Quartus Prime Version 17.1.0 Build 590 10/25/2017 SJ Lite Edition
Revision Name EXP4_1_1
Top-level Entity Name EXP4_1_1
Family Cyclone V
Device 5CSXFC6D6F31C6
Timing Models Final
Logic utilization (in ALMs) 1 / 41,910 (< 1 %)
Total registers 2
Total pins 5 / 499 (1 %)
Total virtual pins 0
Total block memory bits 0 / 5,662,720 (0 %)
Total DSP Blocks 0 / 112 (0 %)
Total HSSI RX PCSs 0 / 9 (0 %)
Total HSSI PMA RX Deserializers 0 / 9 (0 %)
Total HSSI TX PCSs 0 / 9 (0 %)
Total HSSI PMA TX Serializers 0 / 9 (0 %)
Total PLLs 0 / 15 (0 %)
Total DLLs 0 / 4 (0 %)
Compile Design 00:00:53
Analysis & Synthesis 00:00:11
Fitter (Place & Route) 00:00:28
Assembler (Generate programming files) 00:00:07
TimeQuest Timing Analysis 00:00:05
EDA Netlist Writer 00:00:02
Quartus Prime TimeQuest Timing Analyzer was successful. 0 errors, 6 warnings
Running Quartus Prime EDA Netlist Writer
Command: quartus_eda --read_settings_files=off --write_settings_files=off EXP4_1_1 -c EXP4_1_1
18236 Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM_PARALLEL_PROCESSORS in
10905 Generated the EDA functional simulation netlist because it is the only supported netlist type for this device.
202000 An incorrect timescale is selected for the Verilog Output (.VO) file of this PLL design. It's required that the timescale should be 1 ps when sim
204019 Generated file EXP4_1_1.vo in folder "C:/Digital_Experiment/EXP4/EXP4_1_1/simulation/modelsim/" for EDA simulation tool
Quartus Prime EDA Netlist Writer was successful. 0 errors, 3 warnings
293000 Quartus Prime Full Compilation was successful. 0 errors, 16 warnings
System (8)
Processing (125)
100%
00:00:53


Quartus Prime Lite Edition - C:/Digital_Experiment/EXP4/EXP4_1_2/EXP4_1_2 - EXP4_1_2
Flow Summary
Flow Status Successful - Sat Sep 26 10:47:00 2020
Quartus Prime Version 17.1.0 Build 590 10/25/2017 SJ Lite Edition
Revision Name EXP4_1_2
Top-level Entity Name EXP4_1_2
Family Cyclone V
Device 5CGXFC7C7F23C8
Timing Models Final
Logic utilization (in ALMs) 1 / 56,480 (< 1 %)
Total registers 2
Total pins 5 / 268 (2 %)
Total virtual pins 0
Total block memory bits 0 / 7,024,640 (0 %)
Total DSP Blocks 0 / 156 (0 %)
Total HSSI RX PCSs 0 / 6 (0 %)
Total HSSI PMA RX Deserializers 0 / 6 (0 %)
Total HSSI TX PCSs 0 / 6 (0 %)
Total HSSI PMA TX Serializers 0 / 6 (0 %)
Total PLLs 0 / 13 (0 %)
Total DLLs 0 / 4 (0 %)
Compile Design 00:00:57
Analysis & Synthesis 00:00:11
Fitter (Place & Route) 00:00:30
Assembler (Generate programming files) 00:00:08
TimeQuest Timing Analysis 00:00:06
EDA Netlist Writer 00:00:02
Quartus Prime TimeQuest Timing Analyzer was successful. 0 errors, 6 warnings
Running Quartus Prime EDA Netlist Writer
Command: quartus_eda --read_settings_files=off --write_settings_files=off EXP4_1_2 -c EXP4_1_2
18236 Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM_PARALLEL_PROCESSORS in
10905 Generated the EDA functional simulation netlist because it is the only supported netlist type for this device.
202000 An incorrect timescale is selected for the Verilog Output (.VO) file of this PLL design. It's required that the timescale should be 1 ps when sim
204019 Generated file EXP4_1_2.vo in folder "C:/Digital_Experiment/EXP4/EXP4_1_2/simulation/modelsim/" for EDA simulation tool
Quartus Prime EDA Netlist Writer was successful. 0 errors, 3 warnings
293000 Quartus Prime Full Compilation was successful. 0 errors, 16 warnings
System (2)
Processing (123)
100%
00:00:57

引脚分配：无

仿真：


ModelSim - INTEL FPGA STARTER EDITION 10.5b
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
Wave - Default
/EXP4_1_1_vlg_tst/clk
/EXP4_1_1_vlg_tst/in_data
/EXP4_1_1_vlg_tst/in_en
/EXP4_1_1_vlg_tst/out_lock1
/EXP4_1_1_vlg_tst/out_lock2
Now
Cursor 1
100 ps
200 ps
300 ps
400 ps
500 ps
600 ps
700 ps
800 ps
900 ps
1000 ps
Transcript
Wave
Objects
Processes
Library
sim
EXP4_1_1.vt
Now: 700 ps Delta: 0
sim:/EXP4_1_1_vlg_tst/#INITIAL#49
0 ps to 1024 ps


ModelSim - INTEL FPGA STARTER EDITION 10.5b
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
Wave - Default
/EXP4_1_2_vlg_tst/clk
/EXP4_1_2_vlg_tst/in_data
/EXP4_1_2_vlg_tst/in_en
/EXP4_1_2_vlg_tst/out_unlock1
/EXP4_1_2_vlg_tst/out_unlock2
Now
Cursor 1
100000 ps
200000 ps
300000 ps
400000 ps
500000 ps
600000 ps
700000 ps
Transcript
Wave
Objects
Processes
Library
sim
EXP4_1_2.vt
Now: 700 ns Delta: 0
sim:/EXP4_1_2_vlg_tst/#INITIAL#49
0 ps to 745479 ps

写入：无

硬件验证：无

（二）

设计：

```
module synchro(in_data, clk, clr, in_en, out_unlock);
    input in_data;
    input clk;
    input clr;
    input in_en;

    output reg out_unlock;

    always @ (posedge clk)

      if(!in_en)
        out_unlock <= out_unlock;
      else
        begin
          if(clr)
            out_unlock = 0;
          else
            out_unlock <= in_data;
        end

endmodule
```

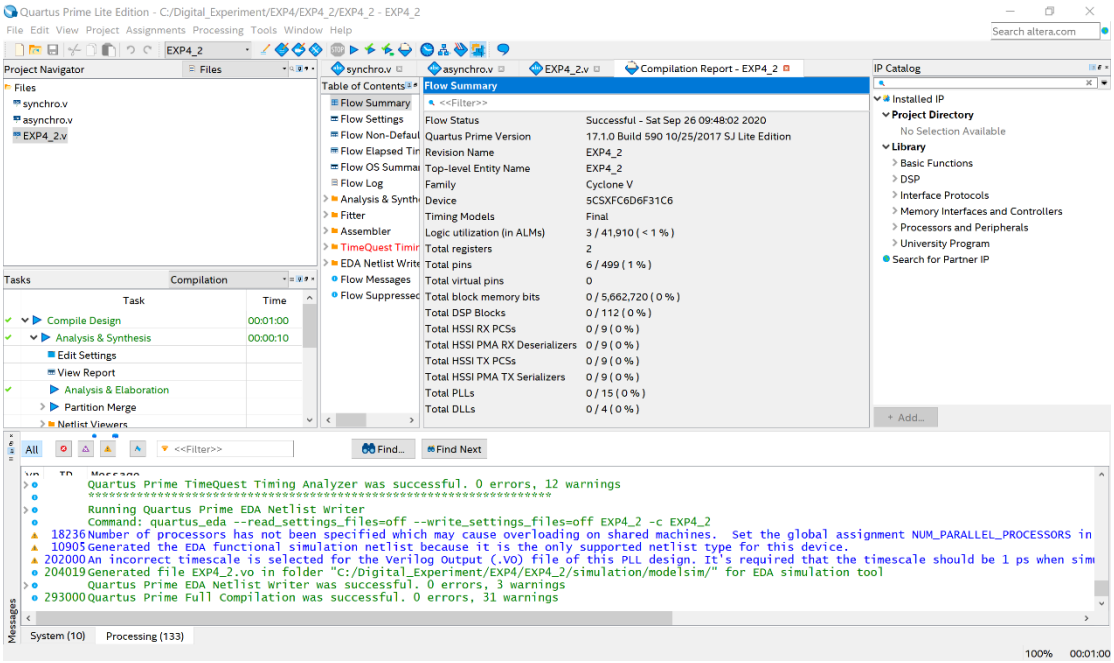
```
module asynchro(in_data, clk, clr, in_en, out_unlock);
    input in_data;
    input clk;
    input clr;
    input in_en;

    output reg out_unlock;

    always @ (posedge clk or posedge clr)

      if(clr)
        begin
          if(in_en)
            out_unlock = 0;
          else
            out_unlock <= out_unlock;
        end
      else
        begin
          if(in_en)
            out_unlock <= in_data;
          else
            out_unlock <= out_unlock;
        end

endmodule
```

```
module EXP4_2(in_data, clk, clr, in_en, out_unlock1, out_unlock2);
    input in_data;
    input clk;
    input clr;
    input in_en;

    output out_unlock1;
    output out_unlock2;

    synchro a (in_data, clk, clr, in_en, out_unlock1);
    asynchro b (in_data, clk, clr, in_en, out_unlock2);


endmodule
```

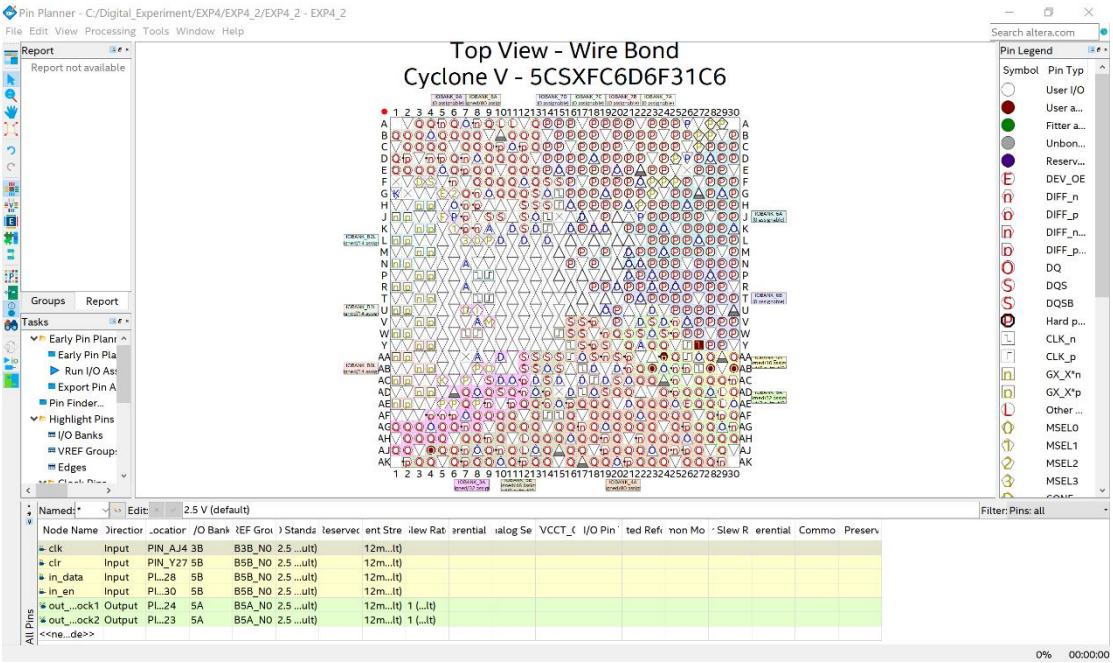
测试：

```
clk = 0; in_data = 0; in_en = 1; clr = 0; #7;
    in_data = 0; #7;
    in_data = 1; #7;
    clr = 1; #3;
    in_data = 0; #7;
    in_data = 1; #7;
    clr = 0; #3;
    in_data = 0; #7;
    clr = 1; #3;
    in_data = 1; #7;
    in_data = 0; #7;
    in_data = 1; #7;
    clr = 0; #3;
    in_data = 0; #7;
    in_data = 1; #7;
    clr = 1; #3;
    in_data = 0; #7;
    clr = 0; #3;
    in_data = 1; #7;
in_en = 0; #7;
    in_data = 0; #7;
    in_data = 1; #7;
    clr = 1; #3;
```

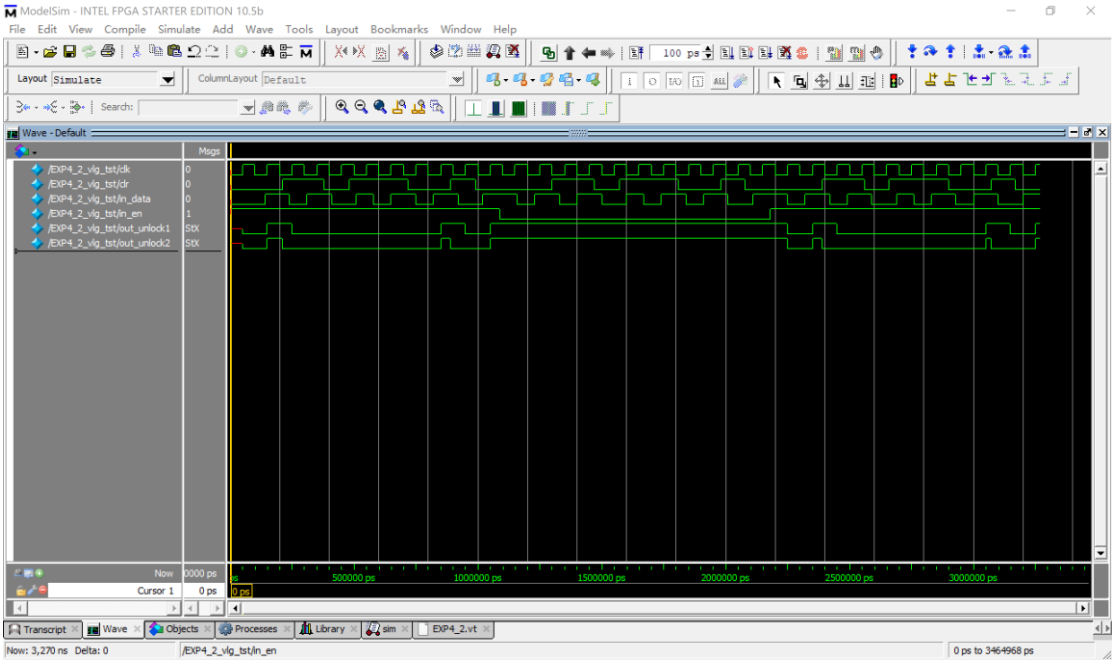
编译：


Quartus Prime Lite Edition - C:/Digital_Experiment/EXP4/EXP4_2/EXP4_2 - EXP4_2
Flow Summary
Flow Status Successful - Sat Sep 26 09:48:02 2020
Quartus Prime Version 17.1.0 Build 590 10/25/2017 SJ Lite Edition
Revision Name EXP4_2
Top-level Entity Name EXP4_2
Family Cyclone V
Device 5CSXFC6D6F31C6
Timing Models Final
Logic utilization (in ALMs) 3 / 41,910 (< 1 %)
Total registers 2
Total pins 6 / 499 (1 %)
Total virtual pins 0
Total block memory bits 0 / 5,662,720 (0 %)
Total DSP Blocks 0 / 112 (0 %)
Total HSSI RX PCSs 0 / 9 (0 %)
Total HSSI PMA RX Deserializers 0 / 9 (0 %)
Total HSSI TX PCSs 0 / 9 (0 %)
Total HSSI PMA TX Serializers 0 / 9 (0 %)
Total PLLs 0 / 15 (0 %)
Total DLLs 0 / 4 (0 %)
Quartus Prime TimeQuest Timing Analyzer was successful. 0 errors, 12 warnings
Running Quartus Prime EDA Netlist Writer
Command: quartus_eda --read_settings_files=off --write_settings_files=off EXP4_2 -c EXP4_2
18236 Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM_PARALLEL_PROCESSORS in
10905 Generated the EDA functional simulation netlist because it is the only supported netlist type for this device.
202000 An incorrect timescale is selected for the Verilog Output (.VO) file of this PLL design. It's required that the timescale should be 1 ps when simu
204019 Generated file EXP4_2.vo in folder "C:/Digital_Experiment/EXP4/EXP4_2/simulation/modelsim/" for EDA simulation tool
Quartus Prime EDA Netlist Writer was successful. 0 errors, 3 warnings
293000 Quartus Prime Full Compilation was successful. 0 errors, 31 warnings

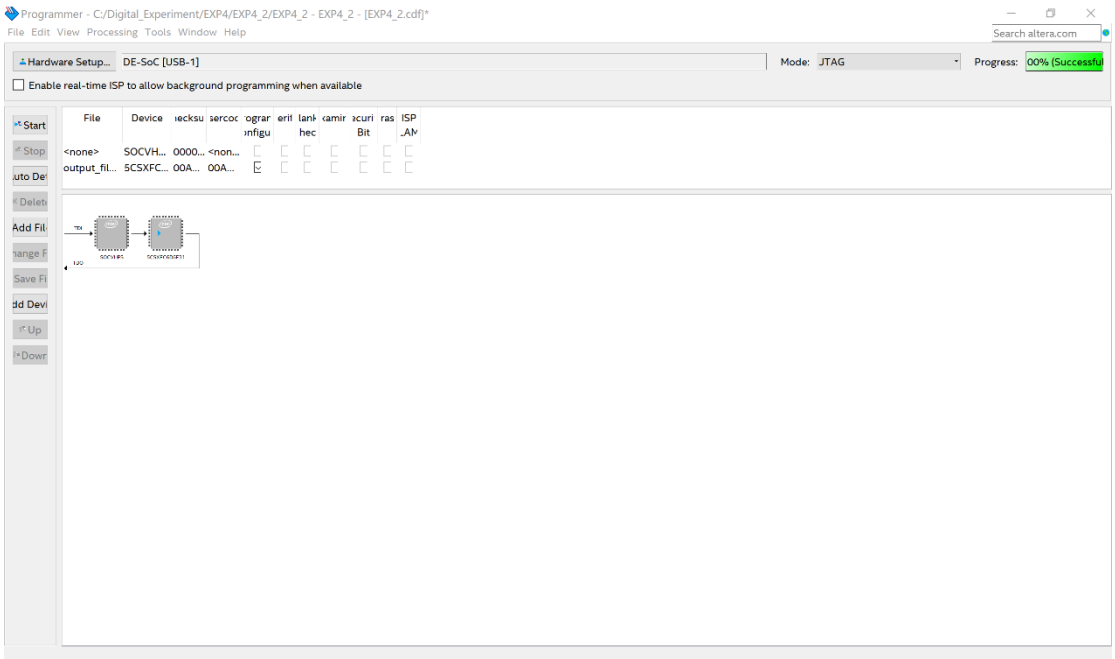
引脚分配：


Pin Planner - C:/Digital_Experiment/EXP4/EXP4_2/EXP4_2 - EXP4_2
Top View - Wire Bond
Cyclone V - 5CSXFC6D6F31C6
clk Input PIN_AJ4 3B B3B_N0 2.5 ...ult) 12m...lt)
clr Input PIN_Y27 5B B5B_N0 2.5 ...ult) 12m...lt)
in_data Input PI...28 5B B5B_N0 2.5 ...ult) 12m...lt)
in_en Input PI...30 5B B5B_N0 2.5 ...ult) 12m...lt)
out_...ock1 Output PI...24 5A B5A_N0 2.5 ...ult) 12m...lt) 1 (...lt)
out_...ock2 Output PI...23 5A B5A_N0 2.5 ...ult) 12m...lt) 1 (...lt)

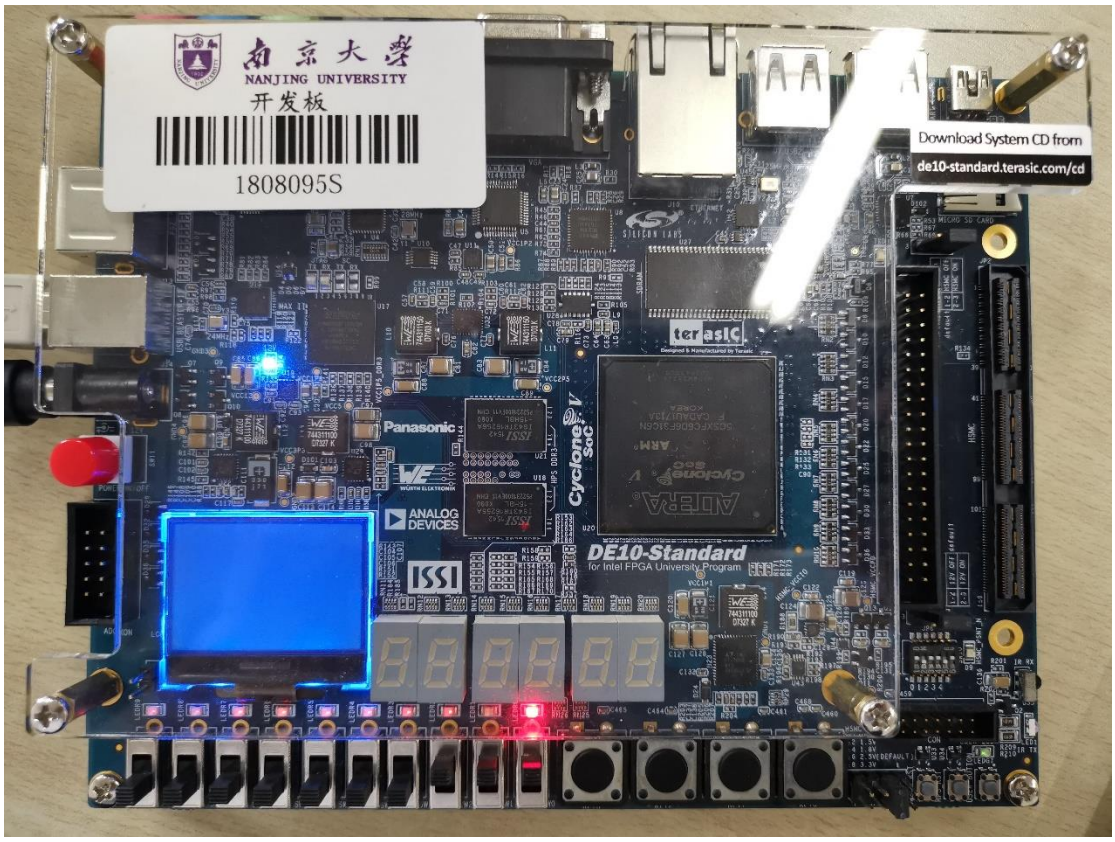
仿真：


ModelSim - INTEL FPGA STARTER EDITION 10.5b
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
Wave - Default
/EXP4_2_vlg_tst/clk
/EXP4_2_vlg_tst/clr
/EXP4_2_vlg_tst/in_data
/EXP4_2_vlg_tst/in_en
/EXP4_2_vlg_tst/out_unlock1
/EXP4_2_vlg_tst/out_unlock2
Cursor 1
500000 ps
1000000 ps
1500000 ps
2000000 ps
2500000 ps
3000000 ps
Transcript
Wave
Objects
Processes
Library
sim
EXP4_2.vt
Now: 3,270 ns Delta: 0
/EXP4_2_vlg_tst/in_en
0 ps to 3464968 ps

写入：


Programmer - C:/Digital_Experiment/EXP4/EXP4_2/EXP4_2 - EXP4_2 - [EXP4_2.cdf]*
File Edit View Processing Tools Window Help
Search altera.com
Hardware Setup...
DE-SoC [USB-1]
Mode: JTAG
Progress:
00% (Successful
Enable real-time ISP to allow background programming when available
Start
Stop
Add Fil
Save Fi
Up
Down
File
Device
<none>
SOCVH...
output_fil...
5CSXFC...

硬件验证：



SW[0] —— in_en
SW[1] —— clr
SW[2] —— in_data
KEY[0] —— clk
LEDR[0] —— out_unlock1
LEDR[1] —— out_unlock2

六、测试方法

Test Bench

任意给 in_data 和 clr 赋值，观察在 in_en 时，in_data 随 clk（和 clr）的变化

七、实验结果

仿真结果与实际结果完全一致

In_data 随 clk（和 clr）的变化符合触发器规律和同步异步清零规律

八、实验中遇到的问题及解决办法

1、不知道模块实例化的方法

上网查阅了模块的相关概念和实例化的方法

2、仿真图出现粗线，且一直没有变化

猜测是仿真无法停止，结果发现测试代码里未加“$stop”

九、实验得到的启示

关于同步异步，阻塞非阻塞的理解：

同步:

A 调用 B，B 处理直到获得结果，才返回给 A。

需要调用者一直等待和确认调用结果是否返回， 然后继续往下执行。

异步:

A 调用 B，B 直接返回。无需等待结果，B 通过状态，通知等来通知 A 或回调函数来处理。

调用结果返回时， 会以消息或回调的方式通知调用者。

阻塞：

A 调用 B，A 被挂起直到 B 返回结果给 A，A 继续执行。

调用结果返回前，当前进程挂起不能够处理其他任务，一直等待调用结果返回。

非阻塞：

A 调用 B，A 不会被挂起，A 可以执行其他操作。

调用结果返回前，当前进程不挂起， 可以去处理其他任务。

所以要区分开同步异步阻塞非阻塞，同步异步说的是被调用者结果返回时通知进程的一种通知机制，阻塞非阻塞说的是调用结果返回前进程的状态，是挂起还是继续处理其他任务。

十、意见和建议

可以将模块实例化的方法讲得更清楚一些，或者推荐一篇讲的比较好的文章。