数字电路与数字系统实验

实验五

计数器和时钟

计算机科学与技术系

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2020.10.1

一、实验目的

在数字系统中，常用计数器来记录系统的工作状态，本实验复习了计数器的工作原理，通过介绍几种简单计数器的工作过程和设计方法、以及开发板系统时钟的使用，学习计数器的设计和定时器的工作原理。

（一）基础实验：计时器

请在 DE10-Standard 开发板上实现一个计时器，在七段数码管上直接以十进制显示。

利用开发板上的频率为 50MHz 的时钟，请先设计一个分频器，其输入为 50MHz 的时钟，输出为一个频率为 1Hz，周期为 1 秒的时钟信号。再用这个新的频率为 1Hz 的时钟信号作为你设计的时钟信号，进行计数。

要求此计时器有开始、暂停和清零功能，要求从 00 计数到 99，计数值到 99 后重新从零开始计数。在数码管上用两位数字显示。

可以在计时结束的时候让某一个发光二极管闪烁，提示计时结束，类似数电教材 8.4.3 节 74x163 计数器中的 RCO 信号高电平一个周期。

（二）拓展实验：时钟、闹钟、秒表

在 DE-10 Standard 开发板上实现一个电子时钟，时钟要求能够显示时、分、秒；还可以有以下功能：调整时间；闹铃（在特定时间 LED 闪烁）；秒表；等。

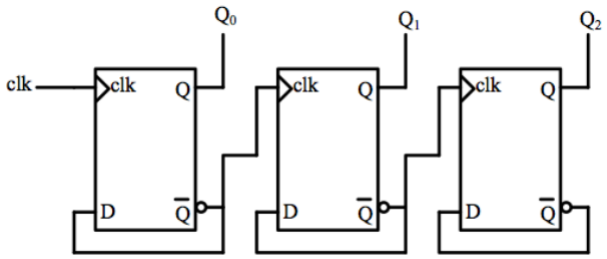
二、实验原理（知识背景）

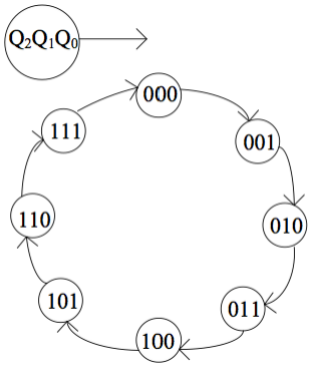
1、加法计数器

利用触发器可以构成简单的计数器。图 1 是由 3 个上升沿触发的 D 触发器组成的 3 位二进制异步加法计数器，即在每个 Clock 的上升沿，计数器输出 Q2Q1Q0 加 1。

图 2 是此 3 位二进制异步加法计数器的状态转移图。

也可以给 D 触发器加上“清零”和“置数”端，构成一个可以清零和置数的二进制异步加法计数器。

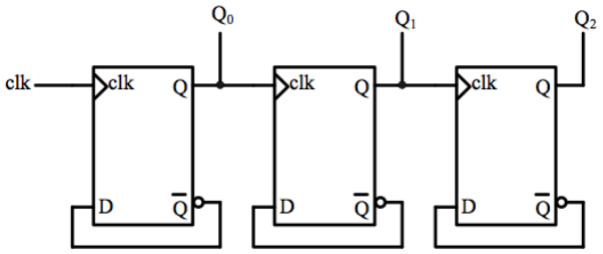


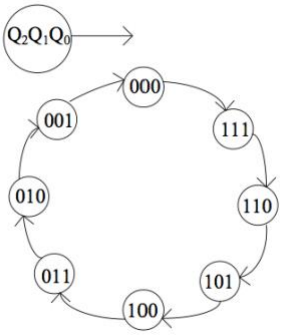


2、减法计数器

利用 D 触发器同样可以构成减法计数器，图 3 是由 3 个上升沿触发的 D 触发器组成的 3 位二进制异步减法计数器。

图 4 是此 3 位二进制异步减法计数器的状态转移图。

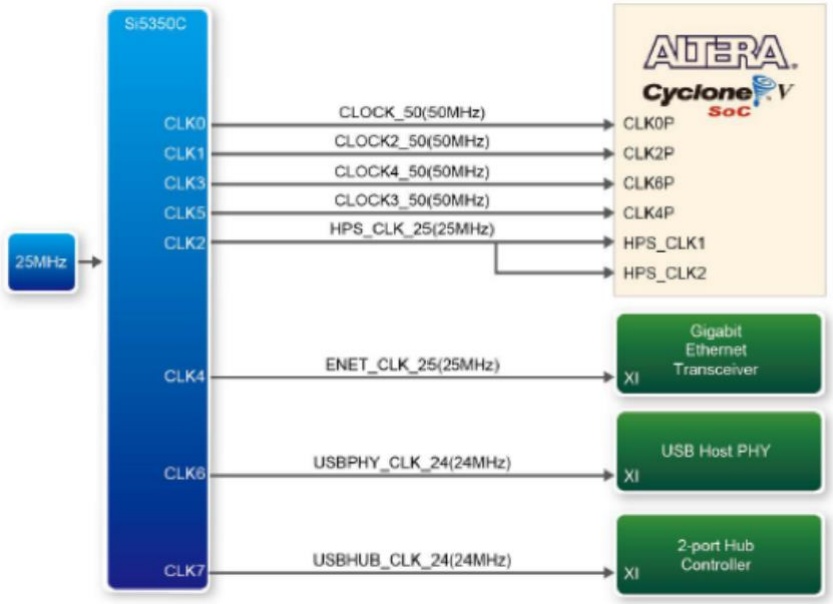




3、定时器

如果在计数器的时钟输入端输入一个固定周期的时钟，那么计数器就变成了定时器。

DE-10 Standard 开发板为 Cyclone V SOC FPGA 提供了四个频率为 50MHz 的外部输入时钟，这些时钟均可供用户使用。另外还给开放平台上的 HPS 提供了一个 25MHz 的时钟。



三、实验环境/器材等

1) 软件环境:

Quartus (Quartus Prime 17.1) Lite Edition

2) 硬件环境:

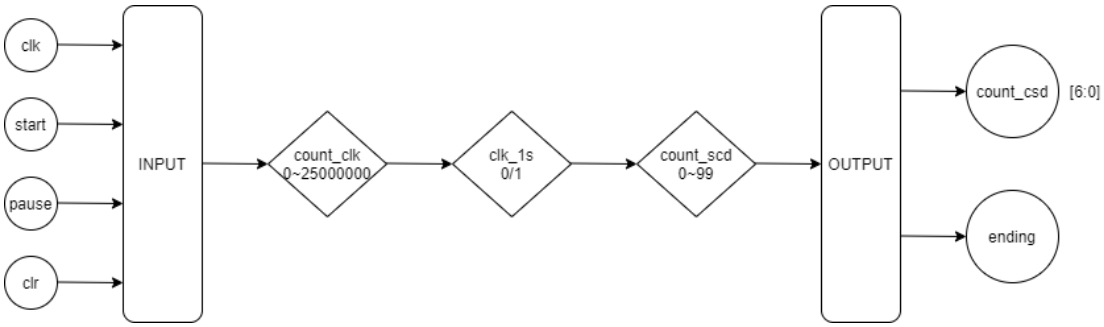
DE10-Standard 开发板
FPGA 部分:
Intel Cyclone V SE 5CSXFC6D6 F31C6N

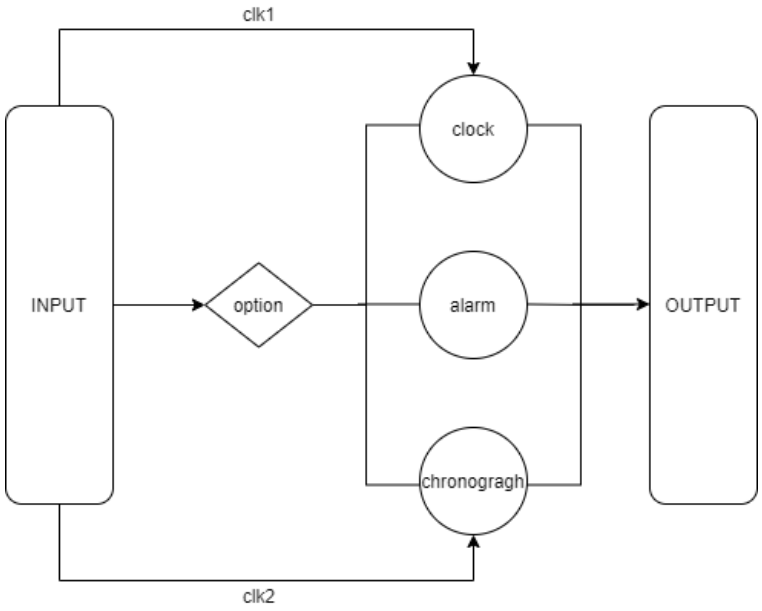
- 110K 逻辑单元
- 5,761Kbit RAM

HPS 部分:
Dual-core ARM Cortex A9

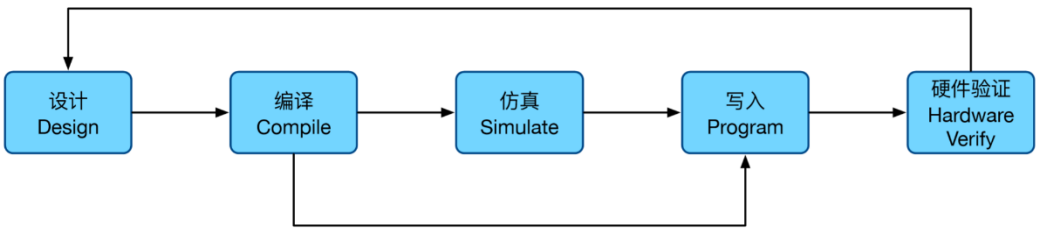
- 925MHz
- 1GB DDR

四、程序代码或流程图


clk
start
pause
clr
INPUT
count_clk
0~25000000
clk_1s
0/1
count_scd
0~99
OUTPUT
count_csd
[6:0]
ending


clk1
INPUT
option
clock
alarm
chronogragh
OUTPUT
clk2

五、实验步骤/过程


设计
Design
编译
Compile
仿真
Simulate
写入
Program
硬件验证
Hardware
Verify

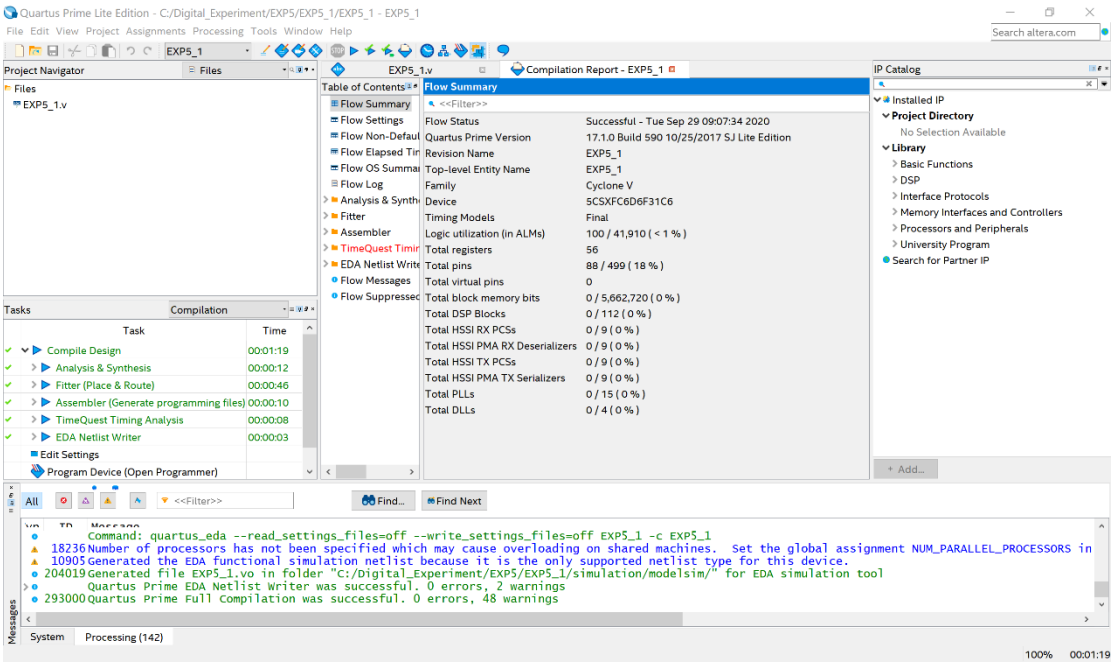
1、基础实验：

设计：

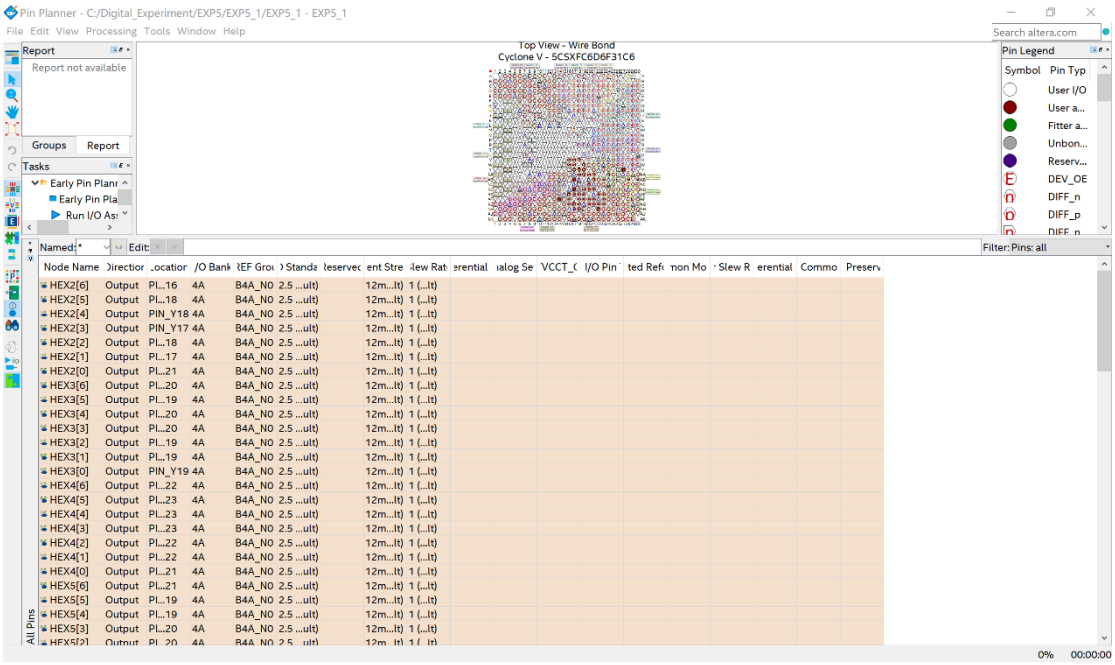
```
module EXP5_1(clk, start, pause, clr, count_clk, clk_1s, count_scd, ending, units_digi
    input clk;
    input start;
    input pause;
    input clr;

    output reg [24:0]count_clk = 0;
    output reg clk_1s = 0;
    output reg [6:0] count_scd = 0;
    output reg ending = 0;
    output reg [3:0] units_digit = 0;
    output reg [3:0] tens_digit = 0;
    output reg [6:0] units_HEX = 64;
    output reg [6:0] tens_HEX = 64;
    output reg [6:0] HEX2 = 127;
    output reg [6:0] HEX3 = 127;
    output reg [6:0] HEX4 = 127;
    output reg [6:0] HEX5 = 127;

    always @(posedge clk)
      if (clr == 1 || start == 0)
      begin
        count_clk = 0;
        count_scd = 0;
        units_HEX = 64;
        tens_HEX = 64;
      end
```

测试：无

编译：

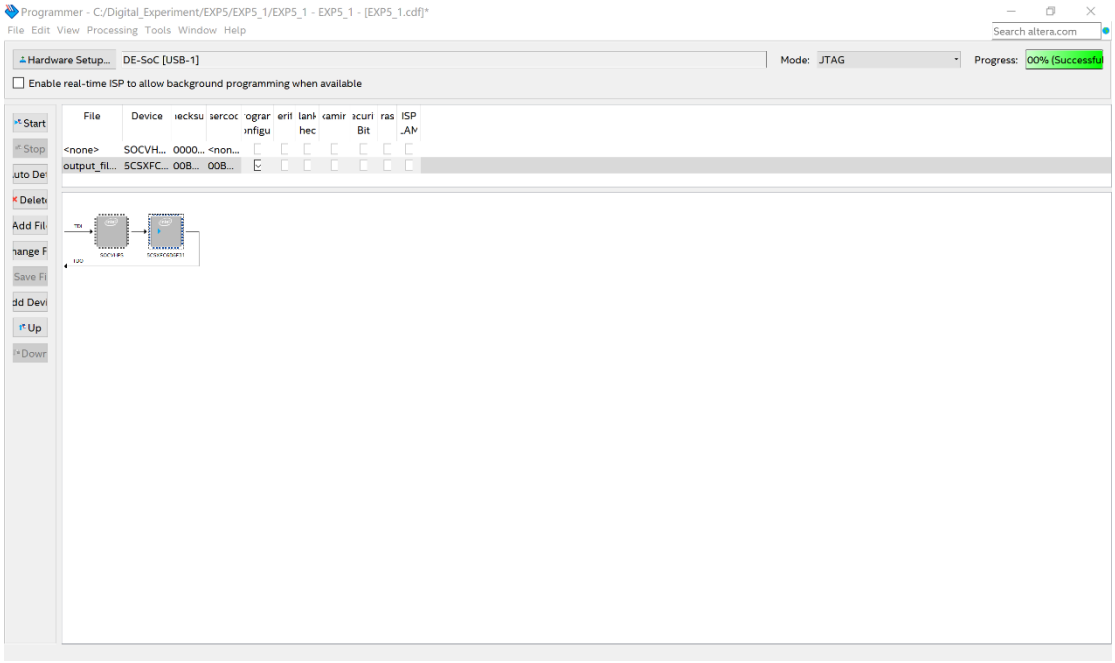


引脚分配：

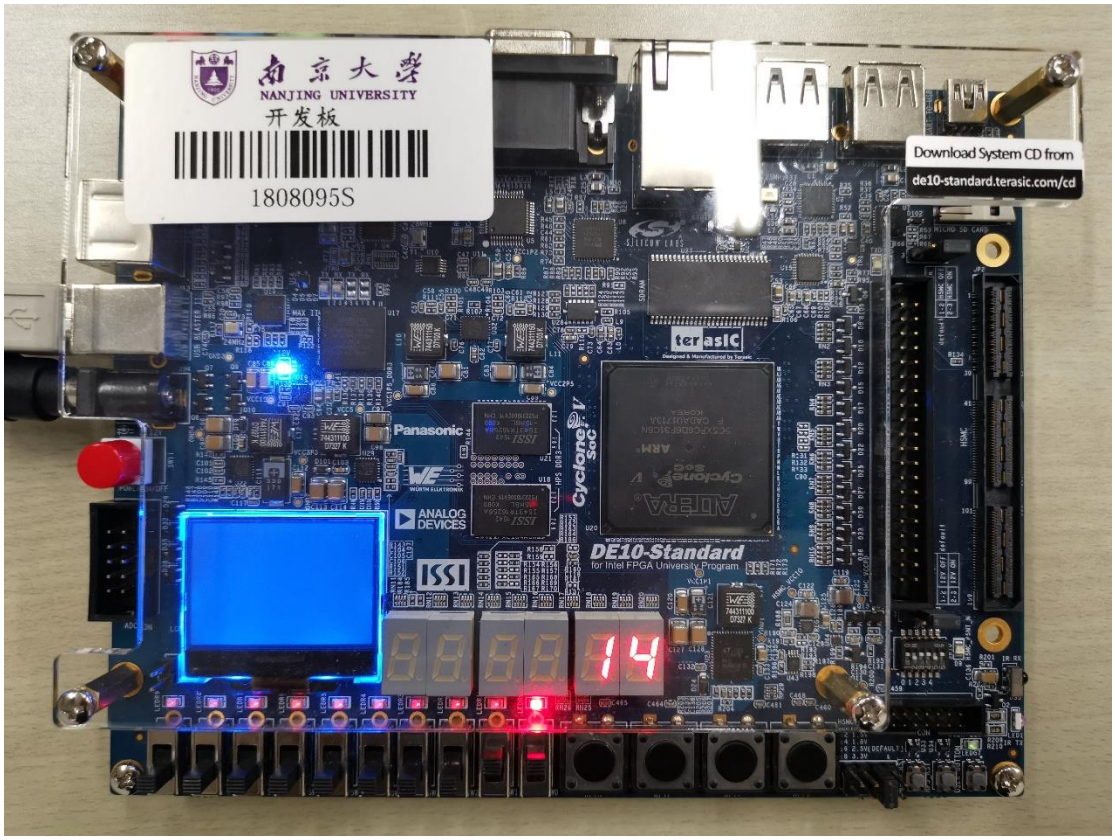

Pin Planner - C:/Digital_Experiment/EXP5/EXP5_1/EXP5_1 - EXP5_1
File Edit View Processing Tools Window Help
Search altera.com
Report
Report not available
Groups Report
Tasks
Early Pin Plann
Early Pin Pla
Run I/O As
Top View - Wire Bond
Cyclone V - 5CSXFC6D6F31C6
Pin Legend
Symbol Pin Typ
User I/O
User a...
Fitter a...
Unbon...
Reserv...
DEV_OE
DIFF_n
DIFF_p
Named: *
Edit:
Filter: Pins: all
Node Name
HEX2[6] Output PI...16 4A B4A_NO 2.5 ...ult) 12m...lt) 1 (...lt)
HEX2[5] Output PI...18 4A B4A_NO 2.5 ...ult) 12m...lt) 1 (...lt)
HEX2[4] Output PIN_Y18 4A B4A_NO 2.5 ...ult) 12m...lt) 1 (...lt)
HEX2[3] Output PIN_Y17 4A B4A_NO 2.5 ...ult) 12m...lt) 1 (...lt)
HEX2[2] Output PI...18 4A B4A_NO 2.5 ...ult) 12m...lt) 1 (...lt)
HEX2[1] Output PI...17 4A B4A_NO 2.5 ...ult) 12m...lt) 1 (...lt)
HEX2[0] Output PI...21 4A B4A_NO 2.5 ...ult) 12m...lt) 1 (...lt)
HEX3[6] Output PI...20 4A B4A_NO 2.5 ...ult) 12m...lt) 1 (...lt)
HEX3[5] Output PI...19 4A B4A_NO 2.5 ...ult) 12m...lt) 1 (...lt)
HEX3[4] Output PI...20 4A B4A_NO 2.5 ...ult) 12m...lt) 1 (...lt)
HEX3[3] Output PI...20 4A B4A_NO 2.5 ...ult) 12m...lt) 1 (...lt)
HEX3[2] Output PI...19 4A B4A_NO 2.5 ...ult) 12m...lt) 1 (...lt)
HEX3[1] Output PI...19 4A B4A_NO 2.5 ...ult) 12m...lt) 1 (...lt)
HEX3[0] Output PIN_Y19 4A B4A_NO 2.5 ...ult) 12m...lt) 1 (...lt)
HEX4[6] Output PI...22 4A B4A_NO 2.5 ...ult) 12m...lt) 1 (...lt)
HEX4[5] Output PI...23 4A B4A_NO 2.5 ...ult) 12m...lt) 1 (...lt)
HEX4[4] Output PI...23 4A B4A_NO 2.5 ...ult) 12m...lt) 1 (...lt)
HEX4[3] Output PI...23 4A B4A_NO 2.5 ...ult) 12m...lt) 1 (...lt)
HEX4[2] Output PI...22 4A B4A_NO 2.5 ...ult) 12m...lt) 1 (...lt)
HEX4[1] Output PI...22 4A B4A_NO 2.5 ...ult) 12m...lt) 1 (...lt)
HEX4[0] Output PI...21 4A B4A_NO 2.5 ...ult) 12m...lt) 1 (...lt)
HEX5[6] Output PI...21 4A B4A_NO 2.5 ...ult) 12m...lt) 1 (...lt)
HEX5[5] Output PI...19 4A B4A_NO 2.5 ...ult) 12m...lt) 1 (...lt)
HEX5[4] Output PI...19 4A B4A_NO 2.5 ...ult) 12m...lt) 1 (...lt)
HEX5[3] Output PI...20 4A B4A_NO 2.5 ...ult) 12m...lt) 1 (...lt)
All Pins
0%
00:00:00

仿真：无

写入：


Programmer - C:/Digital_Experiment/EXP5/EXP5_1/EXP5_1 - EXP5_1 - [EXP5_1.cdf]*
File Edit View Processing Tools Window Help
Search altera.com
Hardware Setup...
DE-SoC [USB-1]
Mode: JTAG
Progress:
00% (Successful
Enable real-time ISP to allow background programming when available
Start
Stop
Add Fil
Up
File
Device
<none>
SOCVH...
output_fil...
5CSXFC...
Bit

硬件验证:



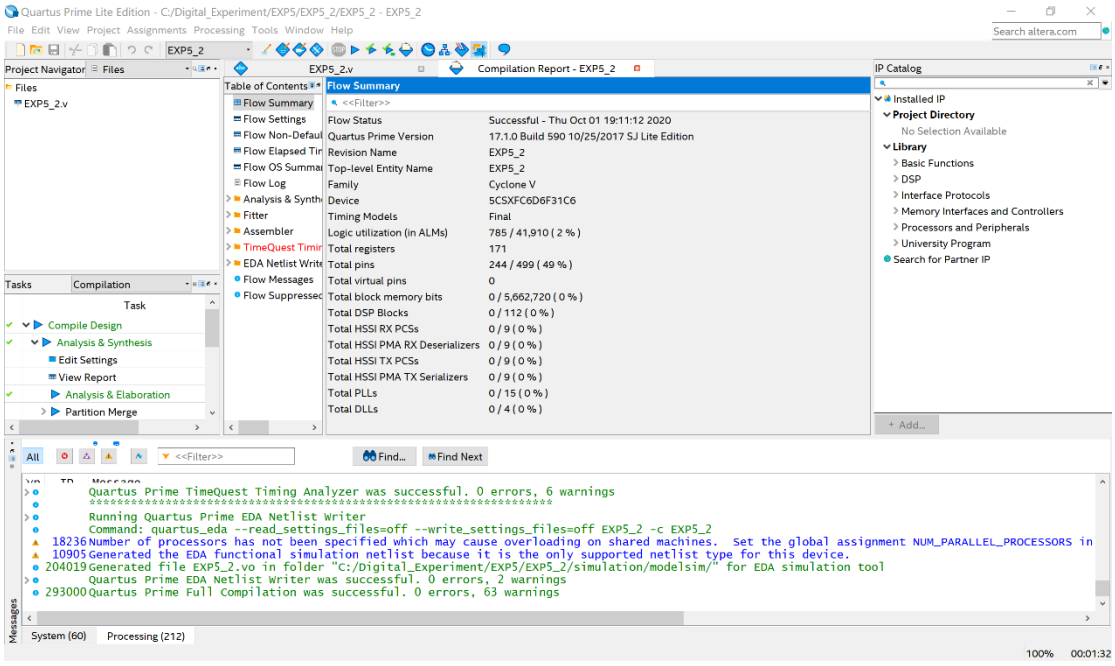
2、拓展实验：

设计:

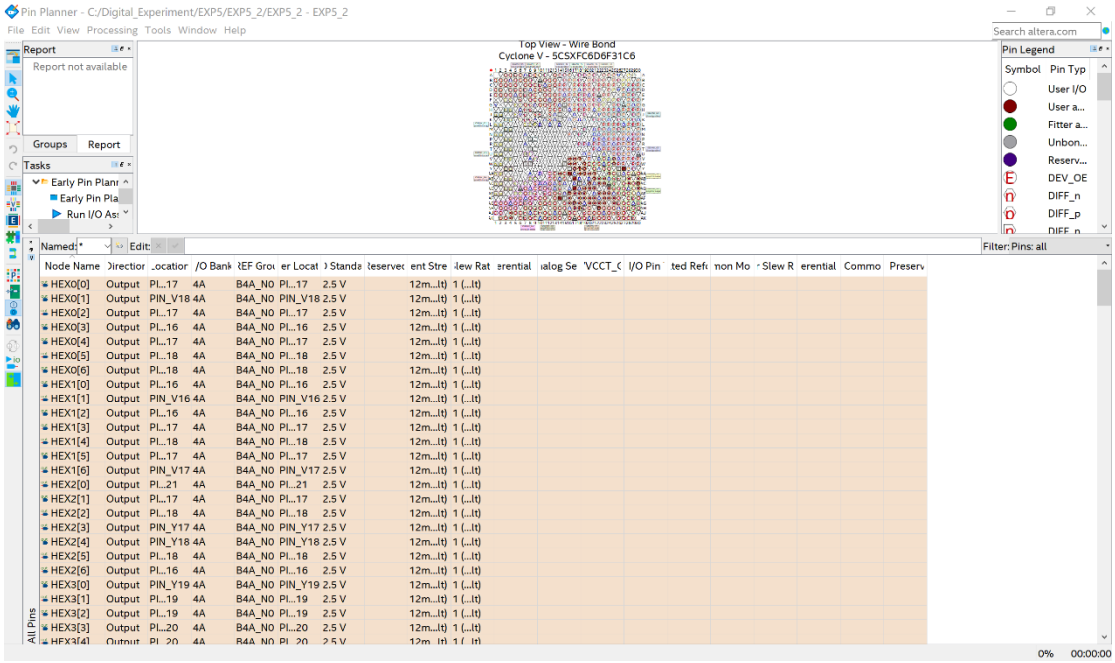
```
module EXP5_2(
clk, count_clk, clk_1s, count_scd, count_min, count_hour,
digit0, digit1, digit2, digit3, digit4, digit5,
HEX0, HEX1, HEX2, HEX3, HEX4, HEX5,
pause, shift_scd, shift_min, shift_hour,
alarm, alarm_set, alarm_shift_min, alarm_shift_hour,
alarm_min, alarm_hour, alarm_digit2, alarm_digit3, alarm_digit4, alarm_digit5,
alarm_min_set, alarm_hour_set, alarm_flag, alarm_remind,
clk2, count_clk2, clk2_1s, clk2_1ms, count_mscd2, count_scd2, count_min2,
chrono, chrono_start_and_pause, chrono_clear,
chrono_digit0, chrono_digit1, chrono_digit2, chrono_digit3, chrono_digit4, chrono_d
);

    input clk;
    input pause;
    input shift_scd;
    input shift_min;
    input shift_hour;
    input alarm;
    input alarm_set;
    input alarm_shift_min;
    input alarm_shift_hour;
    input clk2;
    input chrono;
    input chrono_start_and_pause;
    input chrono_clear;
```

测试：无

编译：

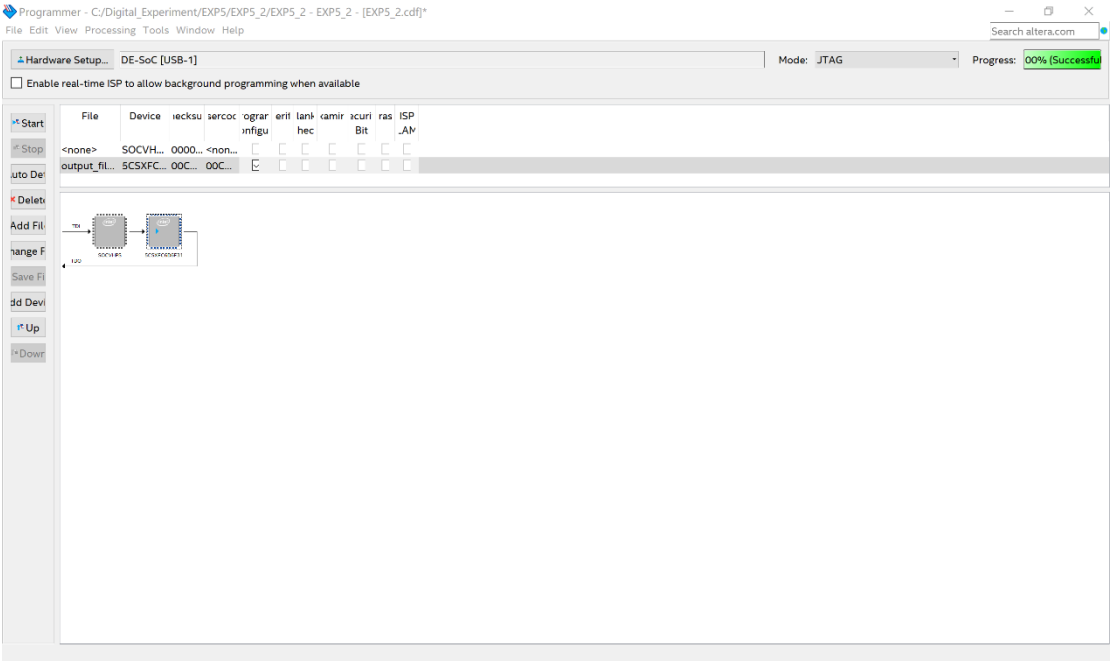

Quartus Prime Lite Edition - C:/Digital_Experiment/EXP5/EXP5_2/EXP5_2 - EXP5_2
Flow Summary
Flow Status Successful - Thu Oct 01 19:11:12 2020
Quartus Prime Version 17.1.0 Build 590 10/25/2017 SJ Lite Edition
Revision Name EXP5_2
Top-level Entity Name EXP5_2
Family Cyclone V
Device 5CSXFC6D6F31C6
Timing Models Final
Logic utilization (in ALMs) 785 / 41,910 (2 %)
Total registers 171
Total pins 244 / 499 (49 %)
Total virtual pins 0
Total block memory bits 0 / 5,662,720 (0 %)
Total DSP Blocks 0 / 112 (0 %)
Total HSSI RX PCSs 0 / 9 (0 %)
Total HSSI PMA RX Deserializers 0 / 9 (0 %)
Total HSSI TX PCSs 0 / 9 (0 %)
Total HSSI PMA TX Serializers 0 / 9 (0 %)
Total PLLs 0 / 15 (0 %)
Total DLLs 0 / 4 (0 %)
Quartus Prime TimeQuest Timing Analyzer was successful. 0 errors, 6 warnings
Running Quartus Prime EDA Netlist Writer
Command: quartus_eda --read_settings_files=off --write_settings_files=off EXP5_2 -c EXP5_2
18236 Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM_PARALLEL_PROCESSORS in
10905 Generated the EDA functional simulation netlist because it is the only supported netlist type for this device.
204019 Generated file EXP5_2.vo in folder "C:/Digital_Experiment/EXP5/EXP5_2/simulation/modelsim/" for EDA simulation tool
Quartus Prime EDA Netlist Writer was successful. 0 errors, 2 warnings
293000 Quartus Prime Full Compilation was successful. 0 errors, 63 warnings

引脚分配：

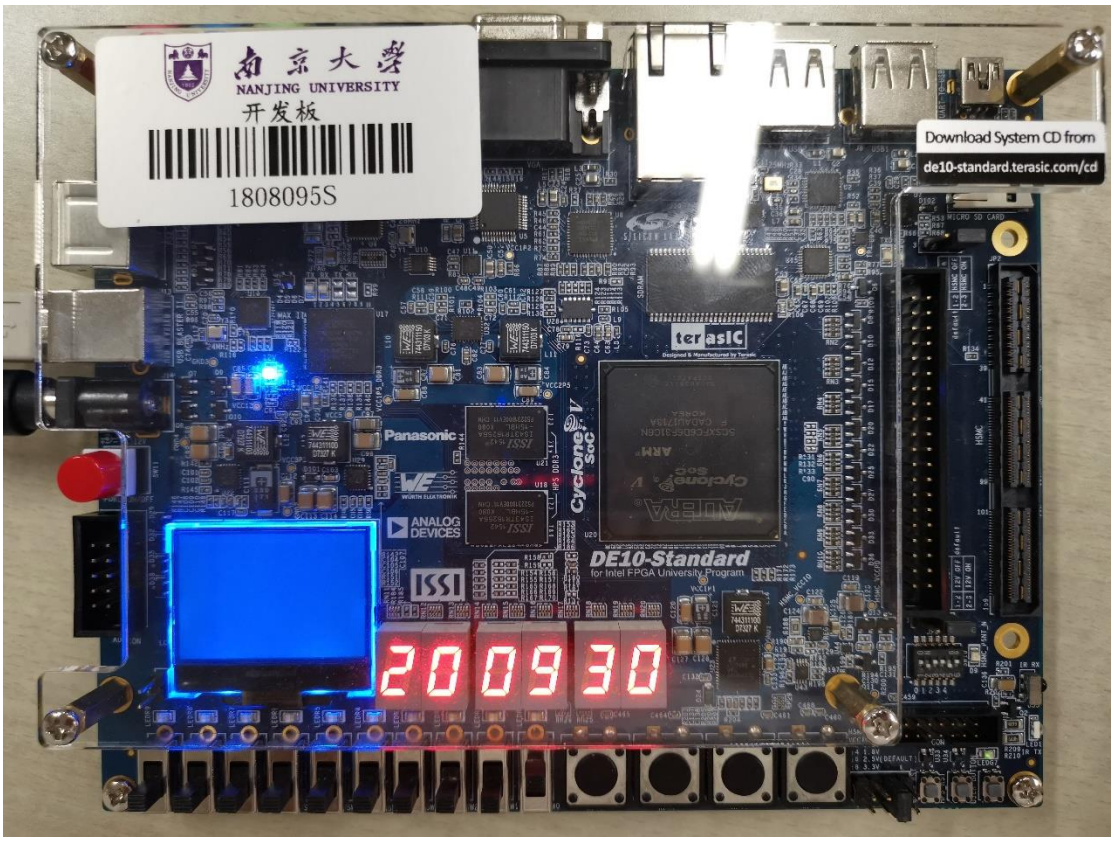

Pin Planner - C:/Digital_Experiment/EXP5/EXP5_2/EXP5_2 - EXP5_2
Top View - Wire Bond
Cyclone V - 5CSXFC6D6F31C6
HEX0[0] Output PL...17 4A B4A_N0 PI...17 2.5 V
HEX0[1] Output PIN_V18 4A B4A_N0 PIN_V18 2.5 V
HEX0[2] Output PL...17 4A B4A_N0 PI...17 2.5 V
HEX0[3] Output PL...16 4A B4A_N0 PI...16 2.5 V
HEX0[4] Output PL...17 4A B4A_N0 PI...17 2.5 V
HEX0[5] Output PL...18 4A B4A_N0 PI...18 2.5 V
HEX0[6] Output PL...18 4A B4A_N0 PI...18 2.5 V
HEX1[0] Output PL...16 4A B4A_N0 PI...16 2.5 V
HEX1[1] Output PIN_V16 4A B4A_N0 PIN_V16 2.5 V
HEX1[2] Output PL...16 4A B4A_N0 PI...16 2.5 V
HEX1[3] Output PL...17 4A B4A_N0 PI...17 2.5 V
HEX1[4] Output PL...18 4A B4A_N0 PI...18 2.5 V
HEX1[5] Output PL...17 4A B4A_N0 PI...17 2.5 V
HEX1[6] Output PIN_V17 4A B4A_N0 PIN_V17 2.5 V
HEX2[0] Output PL...21 4A B4A_N0 PI...21 2.5 V
HEX2[1] Output PL...17 4A B4A_N0 PI...17 2.5 V
HEX2[2] Output PL...18 4A B4A_N0 PI...18 2.5 V
HEX2[3] Output PIN_Y17 4A B4A_N0 PIN_Y17 2.5 V
HEX2[4] Output PIN_Y18 4A B4A_N0 PIN_Y18 2.5 V
HEX2[5] Output PL...18 4A B4A_N0 PI...18 2.5 V
HEX2[6] Output PL...16 4A B4A_N0 PI...16 2.5 V
HEX3[0] Output PIN_Y19 4A B4A_N0 PIN_Y19 2.5 V
HEX3[1] Output PL...19 4A B4A_N0 PI...19 2.5 V
HEX3[2] Output PL...19 4A B4A_N0 PI...19 2.5 V
HEX3[3] Output PL...20 4A B4A_N0 PI...20 2.5 V

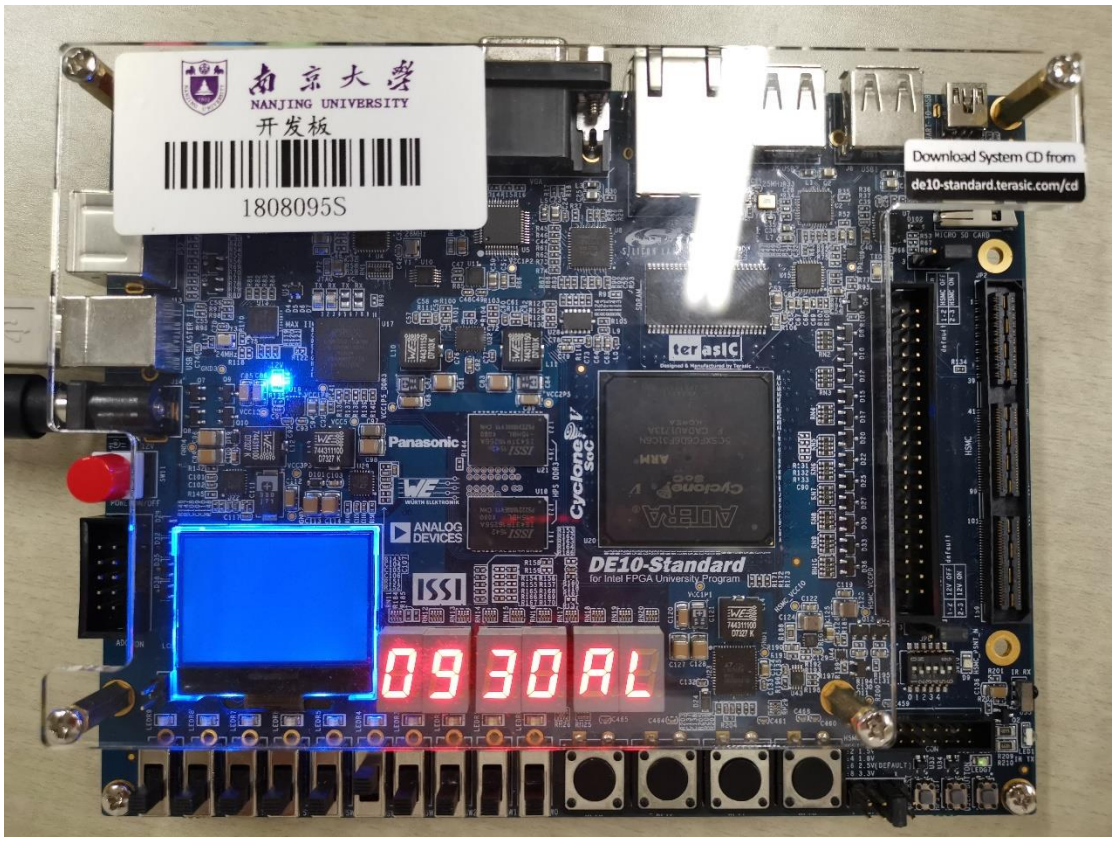
仿真：无

写入：


Programmer - C:/Digital_Experiment/EXP5/EXP5_2/EXP5_2 - EXP5_2 - [EXP5_2.cdf]*
File Edit View Processing Tools Window Help
Search altera.com
Hardware Setup...
DE-SoC [USB-1]
Mode: JTAG
Progress: 00% (Successful
Enable real-time ISP to allow background programming when available
Start
Stop
Add Fil
Save Fi
Up
File
Device
<none>
SOCVH...
output_fil...
5CSXFC...

硬件验证：


南京大学
NANJING UNIVERSITY
开发板
1808095S
Download System CD from
de10-standard.terasic.com/cd
terasIC
Panasonic
ANALOG DEVICES
ISSI
DE10-Standard
for Intel FPGA University Program
200930



六、测试方法

该实验不易通过 Test Bench 进行且测试效率过低，故选择直接在实验板上验证，更为直观方便

七、实验结果

实验板上的实际结果与预期结果一致

八、实验中遇到的问题及解决办法

本实验产生的问题太多，现只列举部分问题

1、时钟和秒表无法在同一个时钟信号 clk 下同时实现

解决办法：增加另一个时钟信号 clk2，使得两个功能的 clk 相互独立，互不干扰。

2、难以在同一个 always 模块内实现所有功能

解决办法：分析各个功能的调用情况，将其分为多个 always 模块，最后再加上一个专门用于输出到数码管的 always 模块，使得代码结构清晰，不易出错。但需避免同一个变量再不同模块内赋值，不然会编译不通过。

3、赋值语句太多，阻塞和非阻塞常常容易用反

解决办法：可以画一个简单的局部时序图，来展示不同变量的变化顺序和时刻，进来理清什么时候用阻塞，什么时候用非阻塞。

九、实验得到的启示

当遇到一个较为庞大的功能时，应当先设计出一个初步的流程图，然后划分功能模块，分别实现每个模块的细节。

十、意见和建议

拓展功能太麻烦了，与分数占比严重不符合，虽然花了大精力做完了，用的时间远超基本功能，但最后的分数与不做拓展功能却并无太大区别，对用心做拓展功能的同学不太公平，希望能够适当提高拓展功能的分数占比。