AutoMOS

CMOS 180nm VCO and LDO Design with Open-Source EDA and GLayout

Chipathon 2025
GLayout track

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Agenda

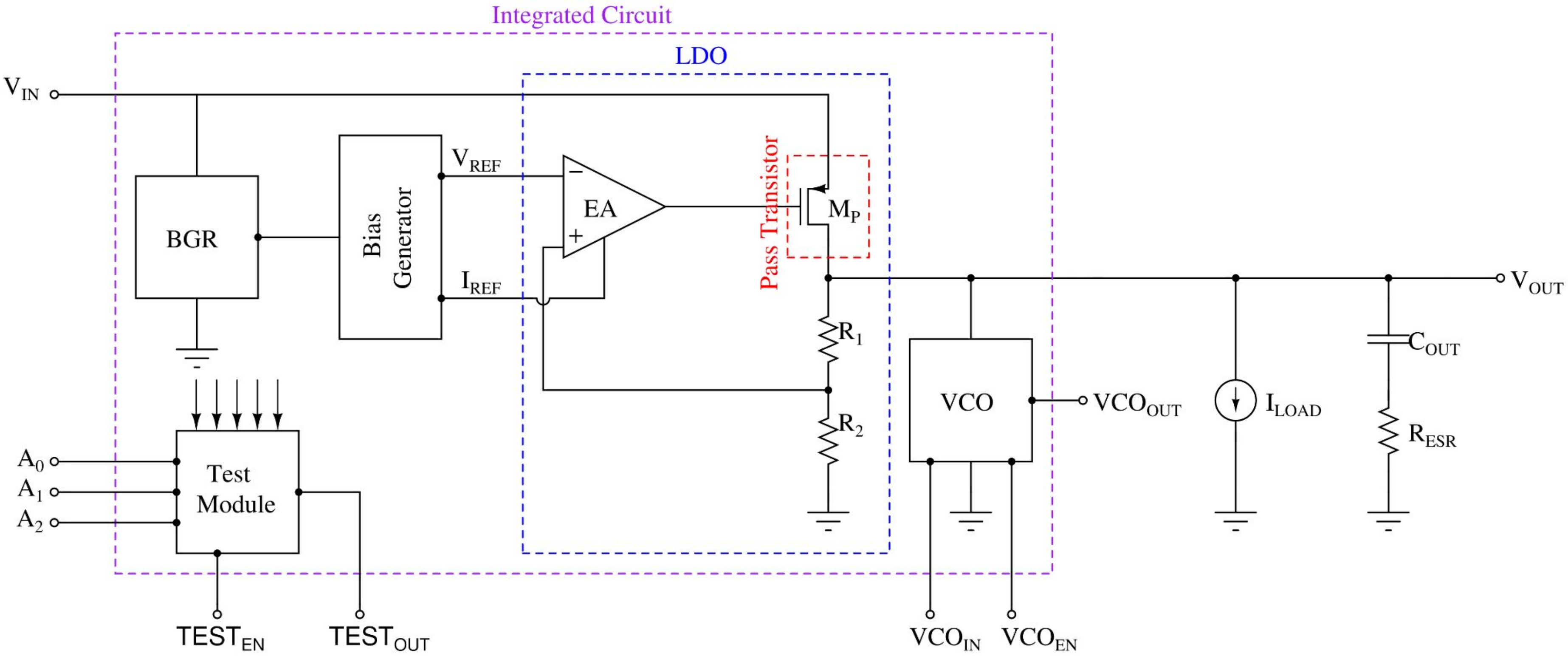
1. Chip Overview
2. Top level block diagram
    a. Functionality of building blocks
    b. Schematics and design complexity
3. Pin-out
4. Application diagrams
5. Work distribution
6. Schedule

Overview

We are proposing a design of some common power management blocks (LDO, bangap and bias generator) used to supply a controlled voltage for other internal/external blocks, and use as an sample load a simple VCO which can provide a carrier signal to an RF module.

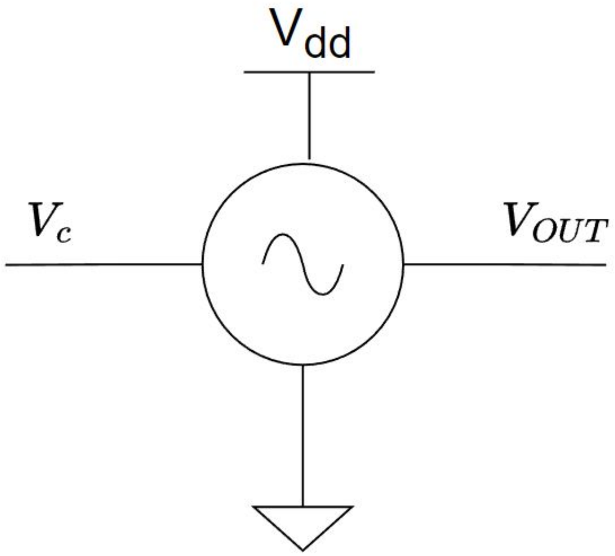
We are planning to use the GLayout tool to generate the layouts of the structures required for each of the subblocks in our proposal.

Top level block diagram



Main subblocks - VCO

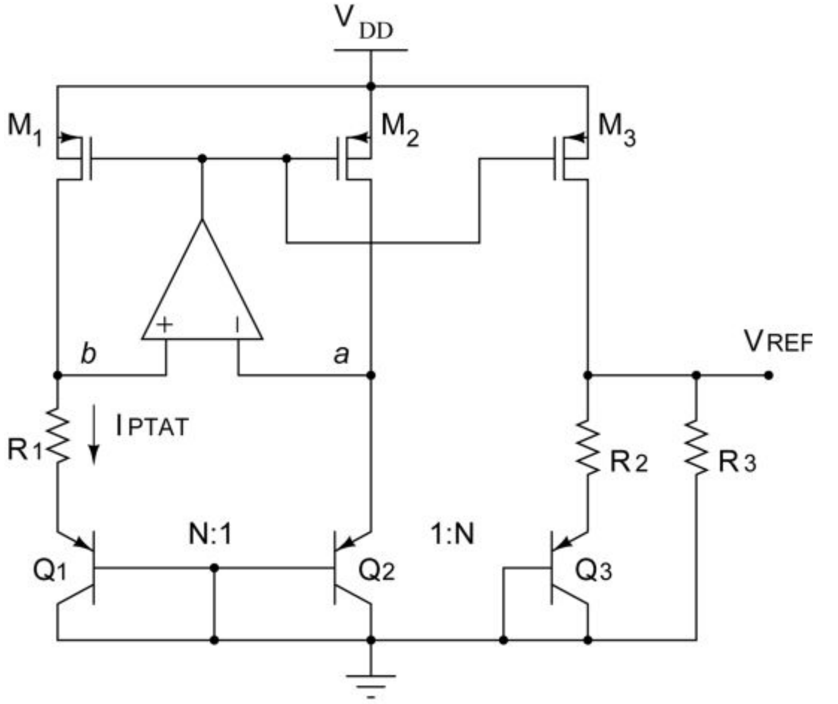
- A VCO is an oscillator whose output frequency is controlled by an input voltage (Vcl). By varying Vctrl, the frequency changes accordingly. In Phase-Locked Loops (PLLs), the VCO generates a signal that is compared to a reference, and the PLL adjusts Vctrl to lock the VCO frequency and phase to the reference, enabling stable frequency generation, clock recovery, and frequency synthesis in communication and digital systems.



Main subblocks - Bandgap voltage reference circuit

This block is responsible to generate a voltage reference used across the chip and tolerant to PVT variations.

We use a classical topology based on 2BJTs that generates a PTAT current, which, when summed with a CTAT current, results in a ZTC voltage.

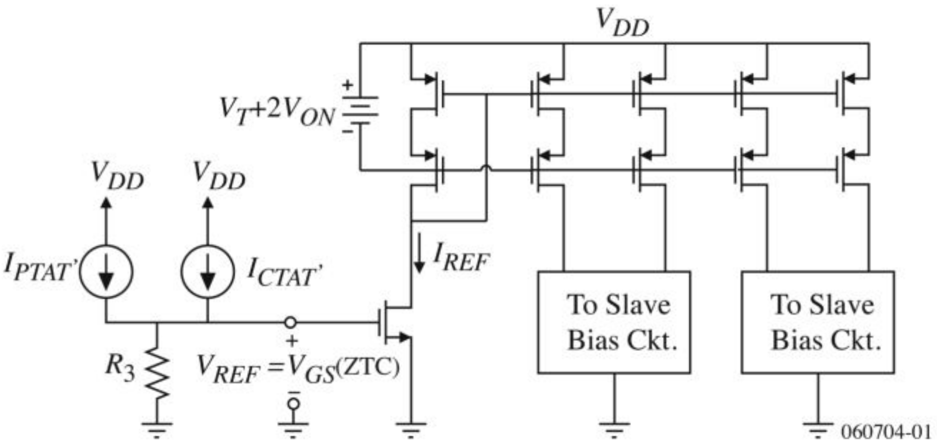


https://scientiairanica.sharif.edu/article_3994_662e80335f901210ed94ab381405fac2.pdf

Main subblocks - Bias generator

Once a voltage reference and a current reference is generated by the Bandgap we need to distribute them for the different subblocks inside the chip.

We will use an opamp based current generator and voltage split on an resistive array to generate the required current bias and voltage references.

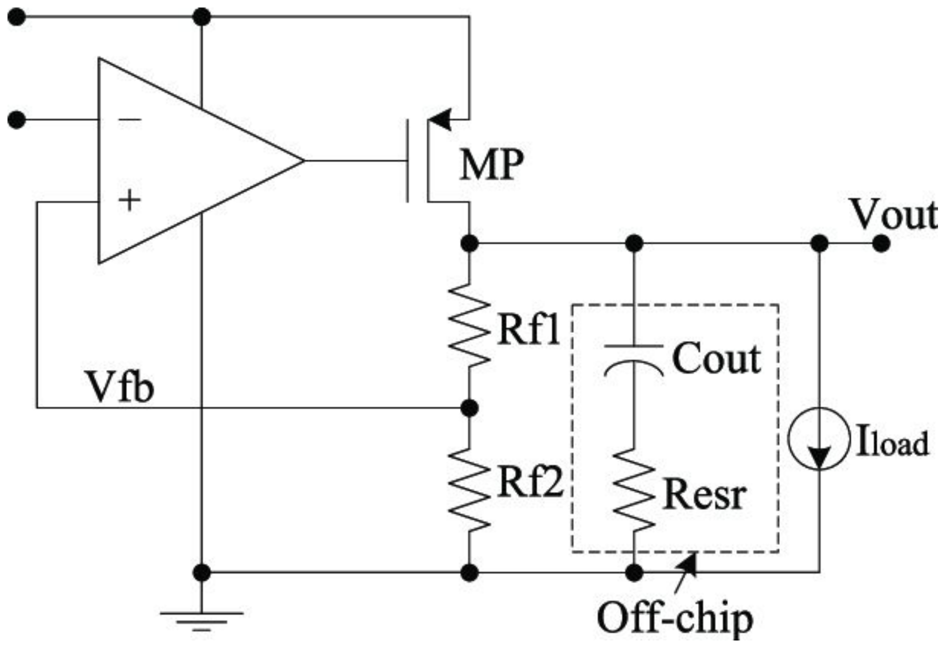


https://aicdesign.org/wp-content/uploads/2018/08/lecture17-180515.pdf

Main subblocks - Low-dropout (LDO) voltage regulator

This is our main block required to generate the stable voltage that will supply the VCO and other external loads.

We will use a classical topology using an external capacitor (order of 0.1n) with and internal error amplifier that controls the pass transistor between the power supply and the LDO output.

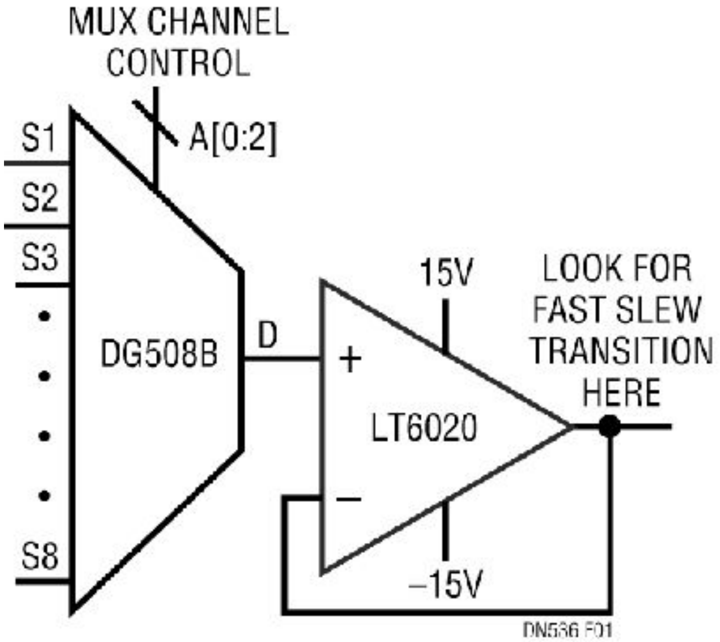


https://www.researchgate.net/publication/316733865_A_300-mA_load_CMOS_low-dropout_regulator_without_an_external_capacitor_for_SoC_and_embedded_applications_A_300-MA_REGULATOR_WITHOUT_AN_EXTERNAL_CAPACITOR

Main subblocks - Test module

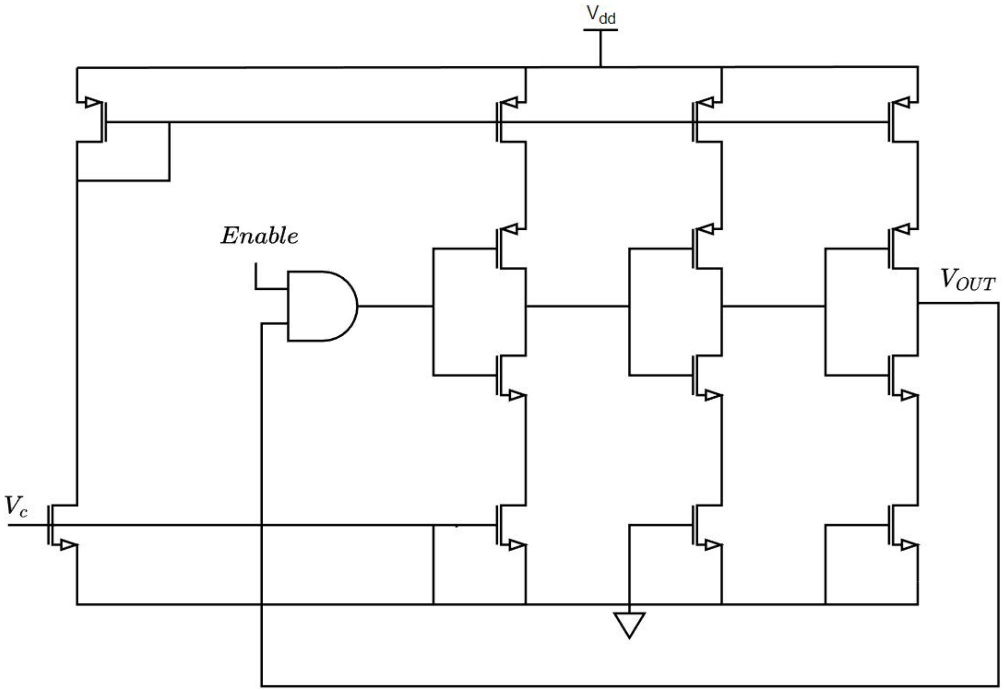
In order to check that internal voltages and currents are in the expected ranges according to specifications, we include a test module to expose those signals.

We will use an analog mux controlled externally followed by a buffer to forward the internal signals to the pin test.

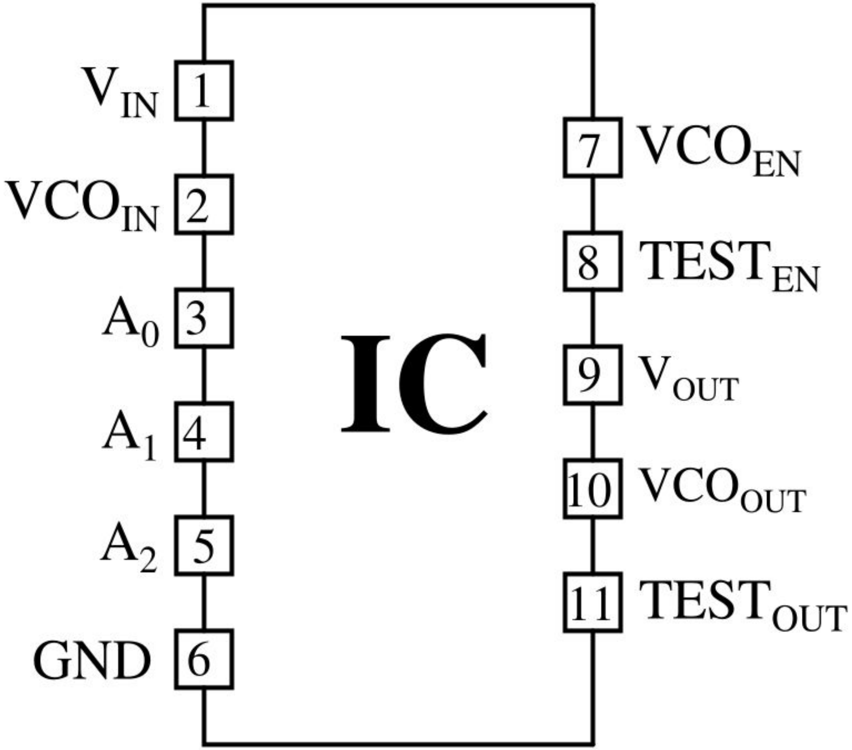


Current-Starved Ring Oscillator

To generate an oscillation at a specific frequency, we use a ring oscillator, and in this case, we implemented a three-stage current-starved ring oscillator. This topology allows us to limit the charge and discharge current using transistors controlled by a bias voltage, which gives us the advantage of efficiently modulating and controlling the oscillation frequency.

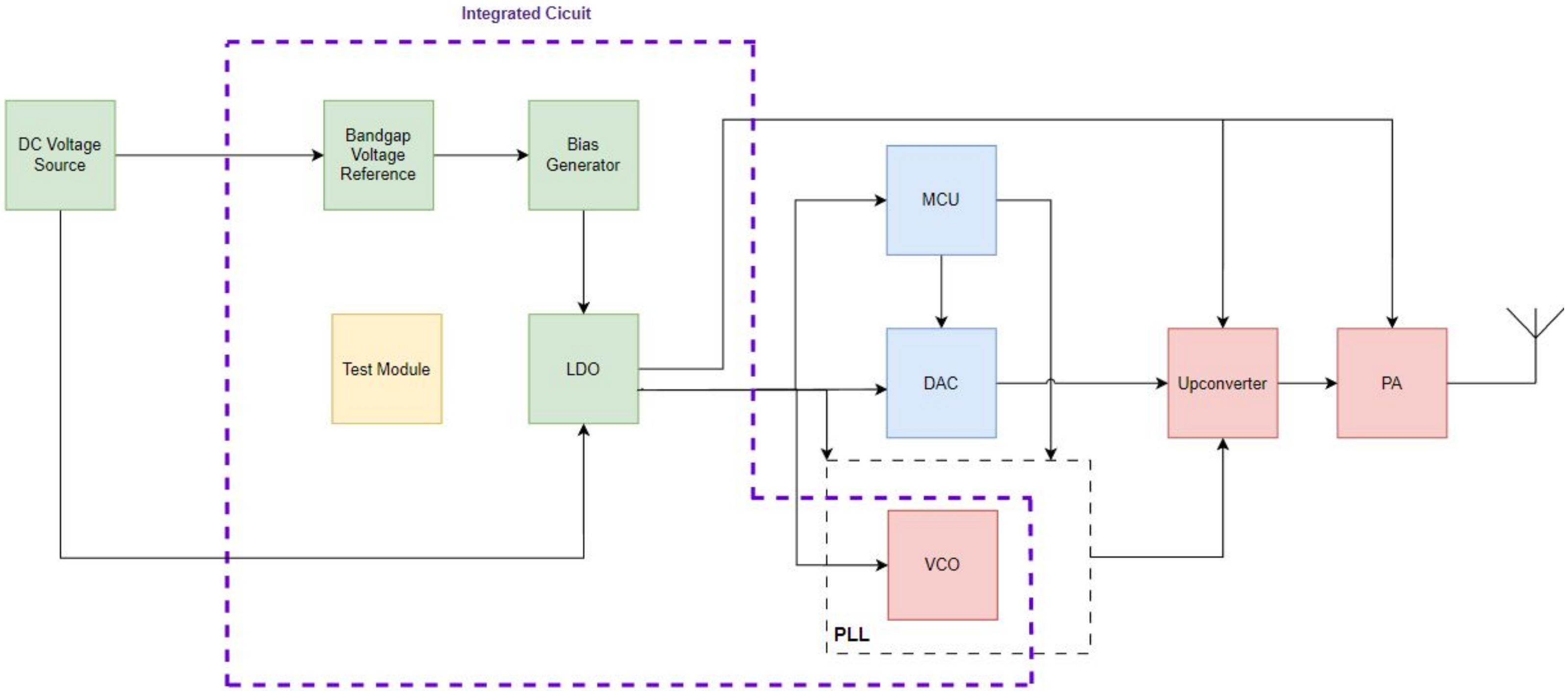


Pinout



Pin	Label	Description
1	V_{IN}	LDO input voltage
2	VCO_{IN}	VCO control voltage
3	A_0	MUX select bit 0 for Test module
4	A_1	MUX select bit 1 for Test module
5	A_2	MUX select bit 2 for Test module
6	GND	Ground connection
7	VCO_{EN}	Enable input for VCO
8	$TEST_{EN}$	MUX enable input for Test module
9	V_{OUT}	LDO output voltage
10	VCO_{OUT}	VCO output signal
11	$TEST_{OUT}$	Test output for internal signal monitoring

Application diagram



Work distribution

Circuit	Responsible	Main Tasks	Comments
Bandgap Voltage Reference	Luighi Viton	- Schematic Design - Functional Simulation - Parameter Optimization - Layout	Critical for voltage stability; requires precision and temperature compensation
Bias Generator	Luighi Viton	- Schematic Design - Current simulation - Noise and Stability Analysis - Layout	Essential for correct biasing; focus on low variability and noise
Low Dropout Regulator (LDO)	Julio Vilca	- Schematic Design - Voltage and ripple simulation - Load testing - Layout	Important for efficient and low-noise regulation; verify stability under load
Test Module	Rodrigo Marin	- Schematic Design - Test signal simulation - Interference with other modules - Layout	Facilitates full functionality verification and post-fab testing
Voltage Controlled Oscillator	Rodrigo Marin	- Schematic Design - Oscillation frequency simulation - Phase noise and tuning range analysis - Layout	Key for frequency generation; focus on phase noise and linearity

Schedule

Chipathon Schedule	Date	Luighi	Julio	Rodrigo
Week 28	July 11, 2025	Project definition	Project definition	Project definition
Week 29	July 18, 2025	Bandgap schematic + functional simulation	LDO error amplifier schematic + functional simulation	VCO schematic + functional simulation
Week 30	July 25, 2025	Bias schematic + functional simulation	LDO top level schematic + functional simulation	VCO schematic + parameter optimization
DESIGN AND SIMULATION				
Week 31	Aug 01, 2025 Schematic review	Bandgap parameter optimization	LDO parameter optimization	Test MUX and buffer schematic + functional simulation
Week 32	Aug 08, 2025 Simulation review blocks	Bias parameter optimization	LDO parameter optimization	Test module parameter optimization
Week 33	Aug 15, 2025 Simulation review top	Top level integration + functional simulation	Top level integration + functional simulation	Top level integration + functional simulation

Schedule

Chipathon Schedule	**Date**	**Luighi**	**Julio**	**Rodrigo**
LAYOUT AND VERIFICATION				
Week 34	Aug 22, 2025	Bandgap layout - glayout	Error amplifier layout - glayout	VCO layout - glayout
Week 35	Aug 29, 2025	Bias layout - glayout	LDO layout - glayout	Test layout - glayout
Week 36	Sept 05, 2025 Layout review blocks	Layout adjustments for subblocks	Layout adjustments for subblocks	Layout adjustments for subblocks
Week 37	Sept 12, 2025 Layout review top - DRC	Top layout	Top layout	Top layout
Week 38	Sept 19, 2025 Verification	Bandgap, ibias PEX extraction and simulation	LDO PEX extraction and simulation	VCO and test PEX extraction and simulation
Week 39	Sept 26, 2025 Final submission	Top level PEX simulation	Top level PEX simulation	Top level PEX simulation
Week 40				