ALMA MATER STUDIORUM
UNIVERSITÀ DI BOLOGNA

Automation Engineering

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Power Electronic Circuits M

Report topic:

Cascaded H-bridge three-level three-phase inverter

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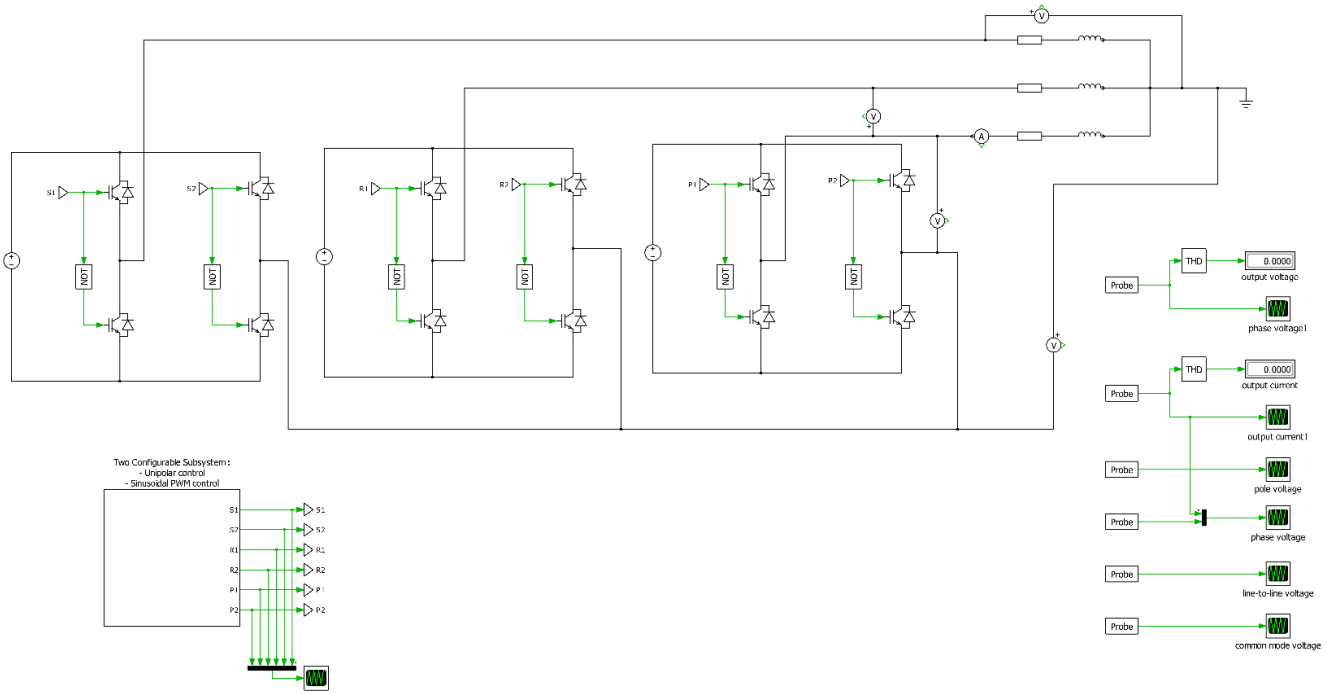
I. Introduction:

The Cascaded H-bridge three-level three-phase inverter is a power electronic circuit widely used for converting direct current (DC) into alternating current (AC) with a three-level output voltage waveform. This inverter topology is employed in various applications, including renewable energy systems, motor drives, and grid-connected power systems. It offers advantages such as improved power quality, reduced harmonic distortion, increased efficiency, and enhanced control capabilities.

II. Description of the chosen topology

1. Schematic of Cascaded H-bridge three-level three-phase inverter:

A Cascaded H-bridge three-level three-phase inverter consists of multiple H-bridge units in general connected in series and in this case, three H-bridge units connected in series for each phase of the three-phase output. Each H-bridge unit provides the input DC voltage for the inverter, several power semiconductor devices, such as insulated gate bipolar transistors (IGBTs) or MOSFETs in general in our case we work with IGBTs, together with control circuits.



CHB : Cascaded H-bridge three-level three-phase inverter

2. Working principle

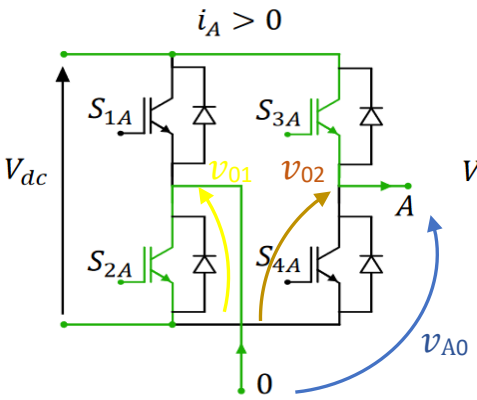
As a normal DC-AC converter, the cascaded H-bridge three-level three-phase inverter involves the combination of multiple **H-bridge units** (well known as **Full-bridge** inverter) to generate a three-phase AC output with three voltage levels. To performs this, Each H-bridge unit is responsible for generating one phase of the three-phase output waveform, since the DC voltage input is divided among the H-bridge units to generate the desired output voltage levels.

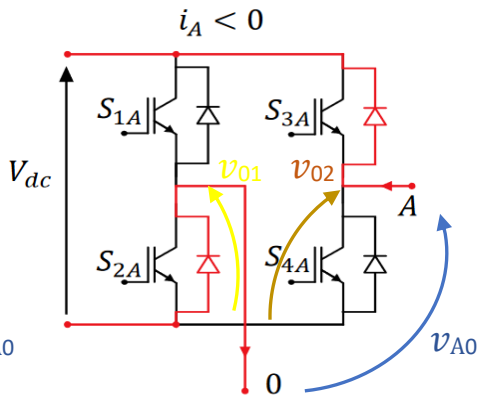
Let us now analyze the sequence of activation of each H-bridge, considering that the output voltage is for both cases the direction of the output current. Kirchhoff's Law: $v_{A0} = v_{02} - v_{01}$

Switch pattern:

- S_{1A} OFF and S_{2A} ON
- S_{3A} ON and S_{4A} OFF

$v_{A0} = v_{02} - v_{01} = V_{dc} - 0 = V_{dc}$

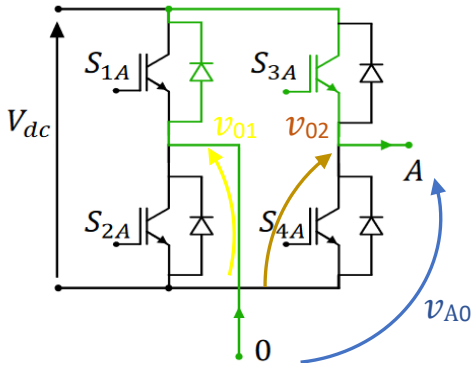


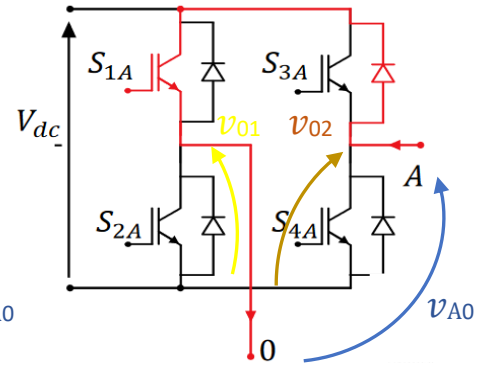


Switch pattern:

- S_{1A} ON and S_{2A} OFF
- S_{3A} ON and S_{4A} OFF

$v_{A0} = v_{02} - v_{01} = V_{dc} - V_{dc} = 0$

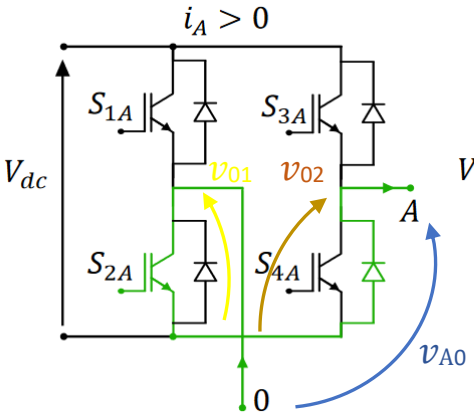


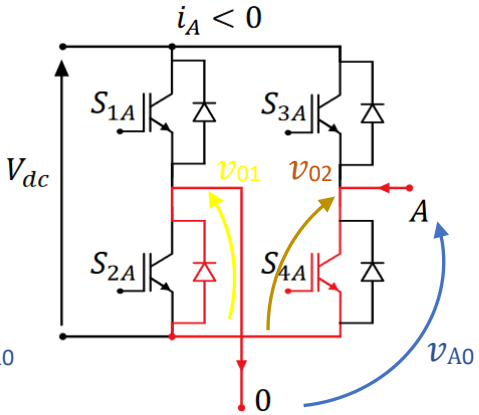


Switch pattern:

- S_{1A} OFF and S_{2A} ON
- S_{3A} OFF and S_{4A} ON

$v_{A0} = v_{02} - v_{01} = 0 - 0 = 0$

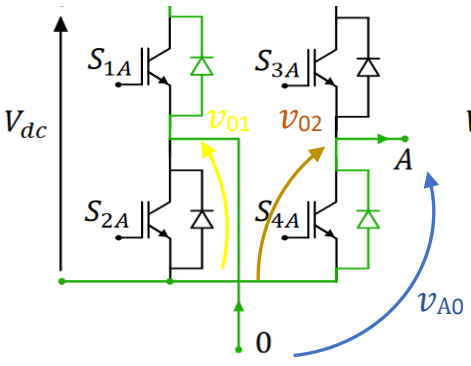


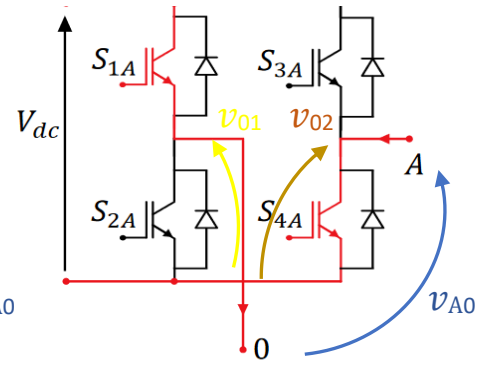


Switch pattern:

- S_{1A} ON and S_{2A} OFF
- S_{3A} OFF and S_{4A} ON

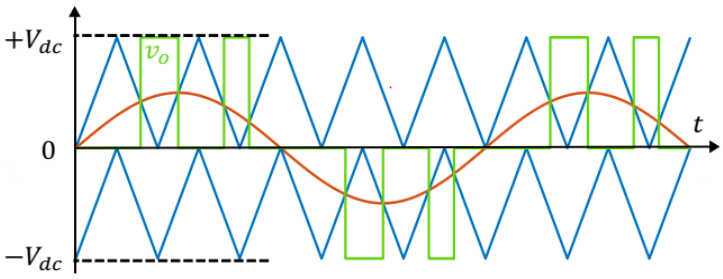
$v_{A0} = v_{02} - v_{01} = 0 - V_{dc} = -V_{dc}$





III. Description of the adopted modulation technique

To achieve the desired voltage levels and waveform shape, based on the **Pulse Width Modulation** that typically uses a reference waveform, that is a **modulating signal**, compared to a **carrier signal** usually a **triangular**, with a fixed frequency, which determines the output voltage and current characteristics. we choose to implement the **Unipolar Modulation technique (three levels)** where four states are used to generate the AC voltage in this approach: $v_{A0} \in [-v_{dc}, 0, +v_{dc}]$.



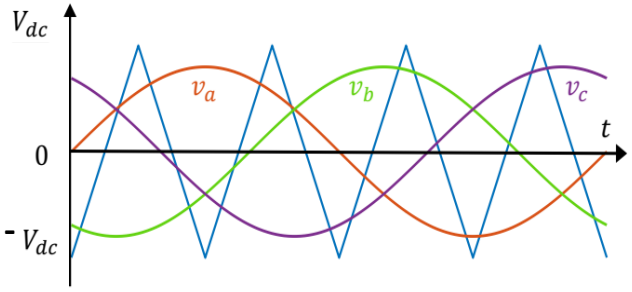
(Two carriers and one modulating signal)

Compared with ***Sinusoidal PWM (SPWM)*** **(two levels),** we would like to experiment the effect of:

- ✓ Output current Quality with respect to number of voltage levels
- ✓ Voltage Balancing
- ✓ Reduction of switching Losses (in terms of commutation)

Can also be implement a ***Sinusoidal PWM*** **(three levels) by implementing a specific modulation strategy known as Zero Voltage Space Vector Modulation (ZVSM) or Zero Voltage Vector Modulation that allows the inverter to generate a zero-voltage level during certain intervals of the modulation period.**

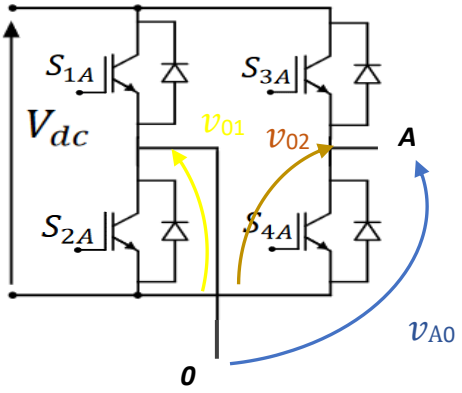
Now we focus on how we can keep the same circuit and implement the ***sinusoidal PWM (SPWM)*** that has three sinusoidal modulating signals a, b, c phase shifted by 120° and these are compared with triangular carrier signal. Modulation index ranges from $0 \leq m \leq 1$. We can make the analysis by simplicity consider ***bipolar modulation technique*** where two states of switches are used to generate the AC versus four in the unipolar modulation. In this approach, shifting the modulating signal waveform by 120° that is ***sinusoidal PWM***, we ensure that the switching signals provided to the **H-bridge units** to have appropriate voltage levels for proper operation. So, in this case, we will focus on describing the single H-bridge units controlled by our **bipolar modulation (only one modulating signal).**

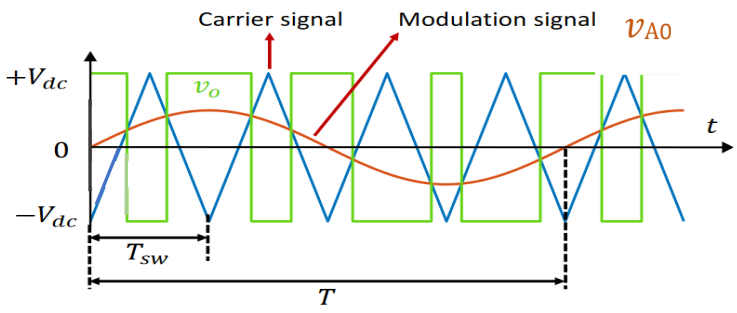


1. Carrier signal, modulating signals, gate signals

One carrier and **one** modulating signal for driving the diagonal switches of the H-bridge: **Diagonal switching configuration.**

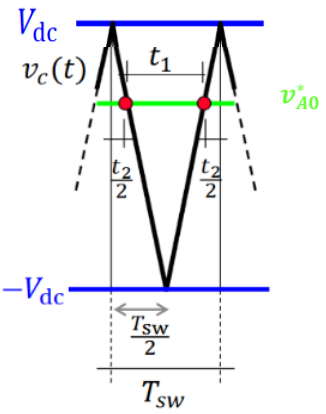
When the modulating signal becomes higher than the carrier, this switch ON the diagonal switches corresponding and switch off when it becomes lower.





Notice that during the implementation we use an opposite signal (Not) to commutate the two power switches on the leg and to avoid **the shoot-through** that is the overlapping conduction of power switches present in the leg, we introduce a **safety time**, called **dead time** ***td*** in which both power switches are in OFF state.

2. description of the working principle



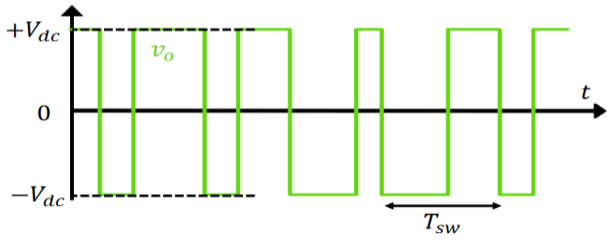
$$\rightarrow \begin{cases} \boldsymbol{v^*_{A0}} \geq \text{carrier} \\ \boldsymbol{v^*_{A0}} \leq \text{carrier} \end{cases} \begin{cases} S_{2A} \text{ ON and } S_{3A} \text{ ON} \\ S_{1A} \text{ ON and } S_{4A} \text{ ON} \end{cases} \rightarrow \begin{cases} \boldsymbol{v}_{A0} = V_{dc} \\ \boldsymbol{v}_{A0} = -V_{dc} \end{cases}$$

a) Duty cycle evaluation:

$$\begin{cases} \boldsymbol{v^*_{A0}} \geq \text{carrier} \\ \boldsymbol{v^*_{A0}} \leq \text{carrier} \end{cases} \rightarrow \begin{cases} S_{2A} \text{ ON and } S_{3A} \text{ ON}: \ t_{on} = t_1 \\ S_{1A} \text{ ON and } S_{4A} \text{ ON}: \ t_{on} = t_2 \\ t_1 + t_2 = T_{sw} \end{cases} \qquad \frac{\boldsymbol{t_2}}{\boldsymbol{2}} = \frac{\boldsymbol{T_{sw}}}{\boldsymbol{2}}\left[\frac{\boldsymbol{V_{dc} - v^*_{A0}}}{\boldsymbol{2V_{dc}}}\right]$$

$$\Rightarrow \begin{cases} \boldsymbol{v^*_{A0}} \geq \text{carrier} \rightarrow \frac{\boldsymbol{t_1}}{\boldsymbol{T_{sw}}} = \delta_1 = \frac{\boldsymbol{1}}{\boldsymbol{2}} + \frac{\boldsymbol{v^*_{A0}}}{\boldsymbol{2V_{dc}}} \\ \boldsymbol{v^*_{A0}} \leq \text{carrier} \rightarrow \frac{\boldsymbol{t_2}}{\boldsymbol{T_{sw}}} = \delta_2 = \frac{\boldsymbol{1}}{\boldsymbol{2}} - \frac{\boldsymbol{v^*_{A0}}}{\boldsymbol{2V_{dc}}} \end{cases}$$

b) THD Evaluation – Bipolar Control:



THD of the output voltage $v_{AO}(t)$:

$$V_{tot} = \sqrt{V_1^2 + V_{dist}^2} \rightarrow V_{dist} = \sqrt{V_{tot}^2 - V_1^2}$$

$$THD = \frac{V_{dist}}{V_1} = \frac{\sqrt{V_{tot}^2 - V_1^2}}{V_1} = \sqrt{\frac{V_{tot}^2}{{V_1}^2} - 1}$$

Reference modulating signal: $v^*_{A0} = v_1 = mV_{dc}\sin(\omega t + \varphi)$ $\qquad \varphi = 0 \ for \ semplicity$

$$\boldsymbol{V_{tot}^2} = \frac{1}{T}\int_0^T \boldsymbol{v_{A0}^2}(\alpha)\boldsymbol{dt} = \frac{1}{T}\int_0^T \boldsymbol{V_{dc}^2}\,\boldsymbol{dt} = {V_{dc}}^2$$

$$\boldsymbol{V_1^2} = \frac{1}{T}\int_0^T \boldsymbol{v_1^2}(\alpha)\boldsymbol{dt} = \frac{1}{T}\int_0^T [mV_{dc}\sin(\omega t)]^2\,\boldsymbol{dt} = \frac{(mV_{dc})^2}{T}\int_0^T \frac{1 - \cos(2\omega t)}{\boldsymbol{2}}\boldsymbol{dt}$$

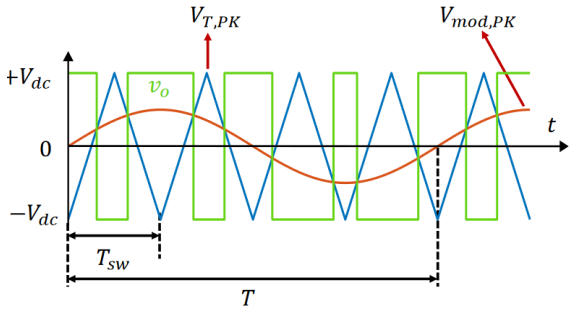
$$\boldsymbol{V_1^2} = \frac{(mV_{dc})^2}{2T}\left[\boldsymbol{t} - \frac{\sin(2\omega t)}{\boldsymbol{2\omega}}\right]_0^T = \frac{(mV_{dc})^2}{2T}T = \frac{(mV_{dc})^2}{2}$$

$$\Rightarrow \quad THD = \sqrt{\frac{V_{tot}^2}{{V_1}^2} - 1} = \sqrt{\frac{{V_{dc}}^2}{\frac{(mV_{dc})^2}{2}} - 1} = \sqrt{\frac{2}{m^2} - 1}$$

In this case of Bipolar modulation is it important to define the **amplitude modulation index** as:

$m = \frac{V_{\text{mod,PK}}}{V_{\text{T,PK}}}$ and we obtain for

- $0 \leq m \leq 1$ is the linear region of the modulating techniques, where the AC output voltage varies linearly as a function of the modulation index, and the harmonics are at well-defined frequencies and amplitudes.
- $m > 1$ is the overmodulation region, where low-order harmonics appear in the AC output voltage : complicates the filter design



And frequency modulation index: $m_f = \frac{f_{sw}}{f}$ $\begin{cases} f_{sw} \text{ is the carrier frequency or switching frequency} \\ f \text{ is the modulating frequency} \end{cases}$

$fsw > f \rightarrow mf > 1$ (m_f = 20 at least)

IV. PLECS simulation 1:

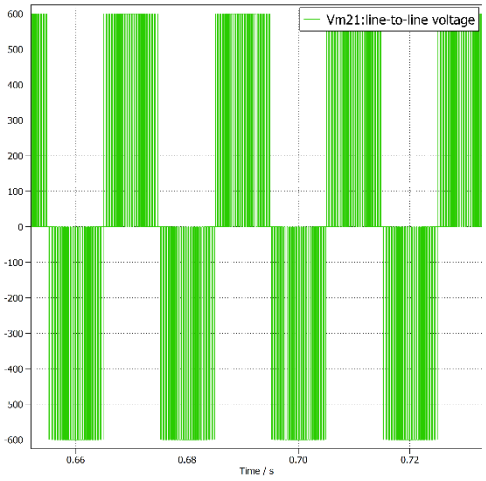
Let us find a real simulation problem given in this image from the website: https://www.semanticscholar.org/paper/An-improved-phase-shifted-PWM-method-for-a-cascaded-Lee-Lee/40eb6c9b4ab47e6cf12729e6fdc45daf991ae9b8.

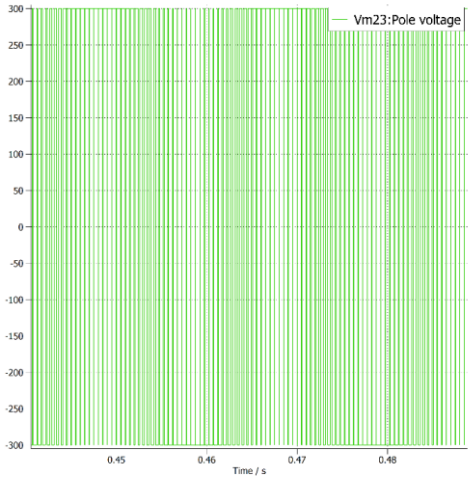
Where the given specification can be tested in our model by only used the specifics parameters.

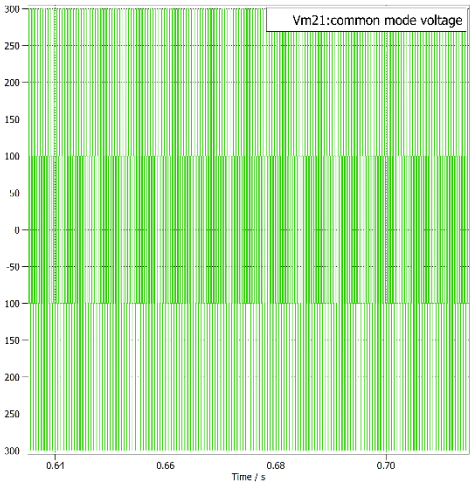
First, we check the frequency modulation index: $m_f = \frac{2kHz}{50Hz} = 40$ since $(m_f \geq 20)$ **it** indicates how much the modulated variable varies around its unmodulated level.

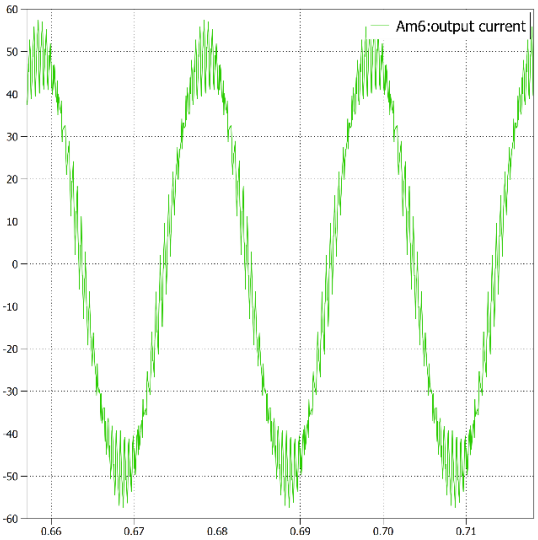
TABLE I. SIMULATION PARAMETERS

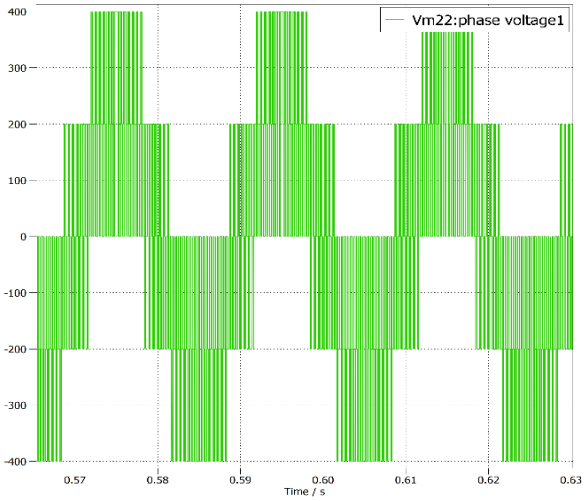
Premasters	Value
~~N (the number of HBC)~~	~~2~~
dc-link voltage for each HBC (V_{dc})	300 V
dc-link capacitor (C_{dc})	1000 uF
Fundamental frequency of the output voltage	50 Hz
Switching frequency	2 kHz
RL-load	6 Ω/ 2 mH

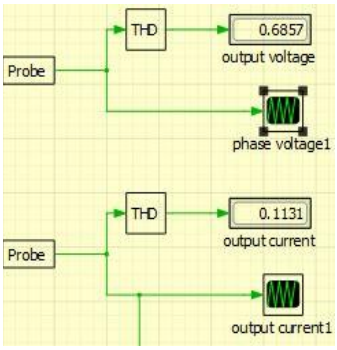


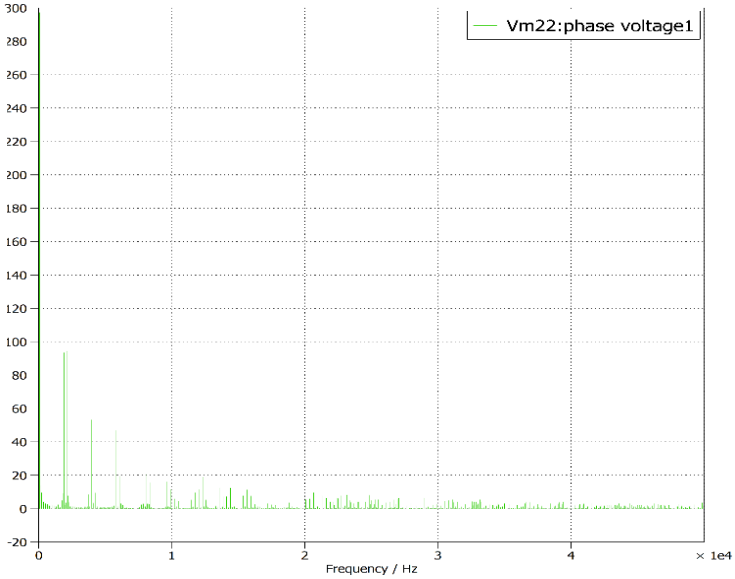




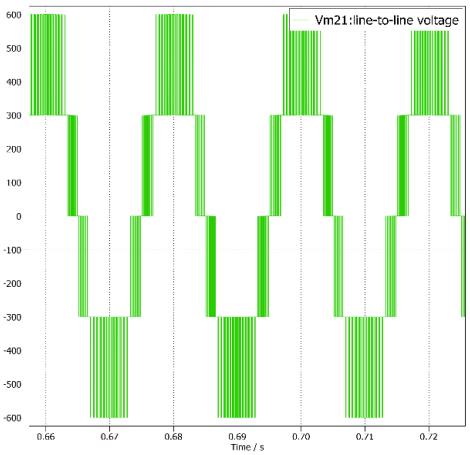


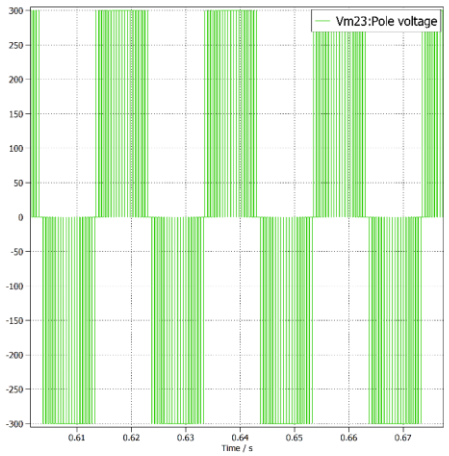


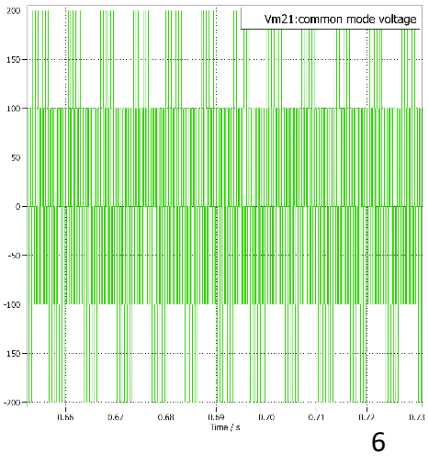


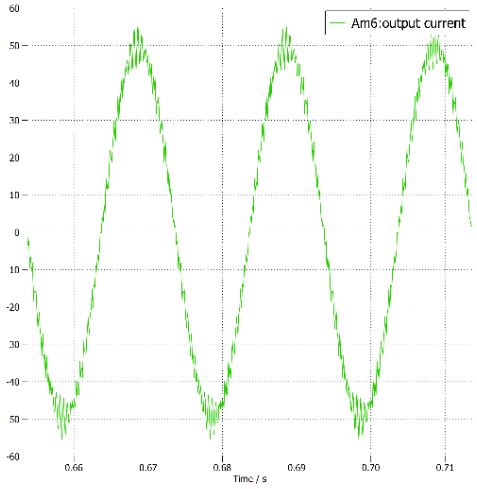


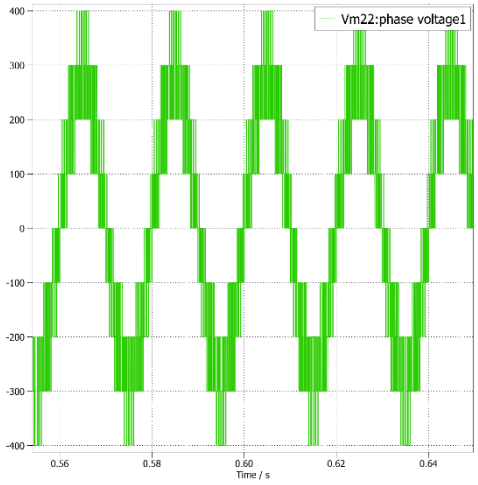
Following the required implementation, ***sinusoidal PWM* technique** helps in reducing total harmonic distortion in the output waveform, which is crucial in applications sensitive to harmonic content. It enables bidirectional power flow and allows the inverter to handle different load. For this first simulation, we can observe that the output **phase voltage has five levels**, the **line-to-line voltage has three levels** and the **pole voltage two levels**. The harmonic contents are around 2kHz either for the current and voltage, and as we observe, the output current has an AC shape but since the harmonic content are not enough shifted at higher frequencies this affects the output filter. The THD of the voltage is 0.6857 and the THD of the current is 0.1131.

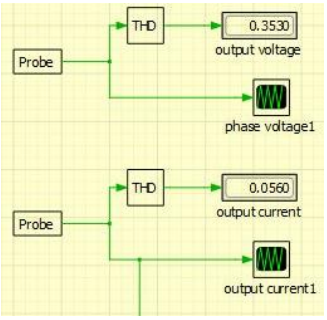




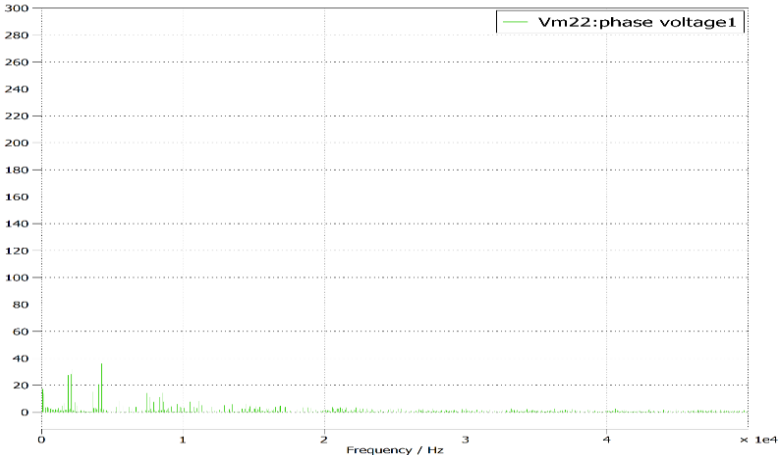








Compared to the **unipolar modulation** that is three levels, we can observe these differences: the **line-to-line voltage has five levels**, the **phase voltage has night levels,** and the **phase voltage has three levels**, also the filter of our output current is affected by the low frequencies of the harmonic contents where we have these oscillations and compared to the sinusoidal PWM these **are small: reduced harmonic content and lower distortion.**



The THD of the output voltage is 0.3530 and the current is 0.0560 that is half with respect to the SPWM case: **The output voltage oscillation in the bipolar/SPWM case is double than in the unipolar case. It therefore has a double ripple also in the load current**.

And the unipolar control allows practically to reduce the amplitude of the switching harmonic by half.

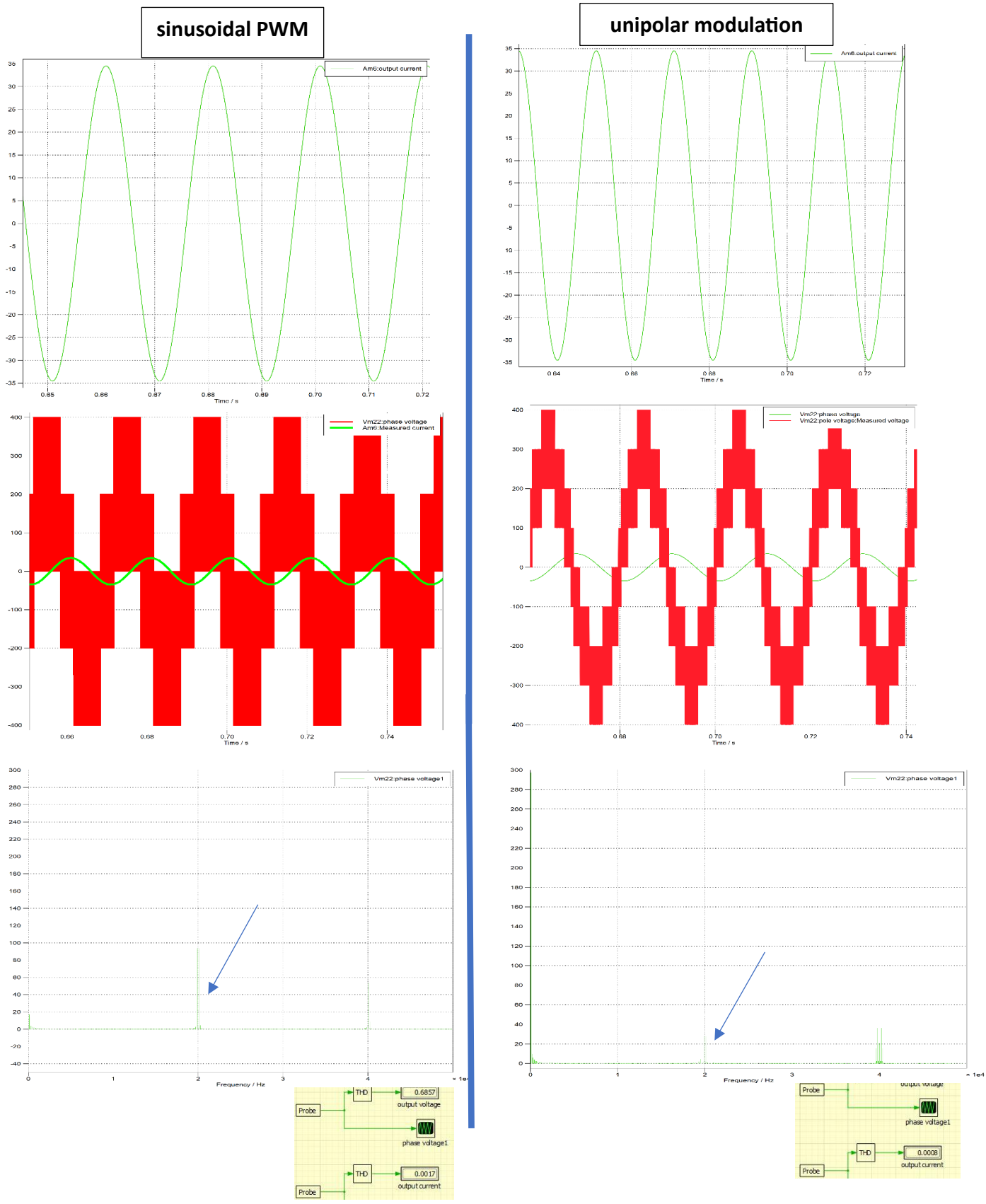
V. PLECS simulation 2: Variations

Considering some variations to optimize our solution, we choose to modify some parameters and check if these can help to obtain the best solution using these modulation techniques.

As indicated in the front figure, we choose to find a **tradeoff** between the **switching frequency** and the **output filter** to get the next simulation.

Model initialization commands

```
Vdc=300;              % DC voltage (V)

fsw=20e3; %2000;      % Switching frequency (Hz)

f=50;                 % grid frequency (Hz)

phase=120*[0 -1 1];% Ideal balanced three-phase angles (Rads)

Vac=230;              %grid voltage RMS%

P=10e3;               %rate power%

m=0.5;                %duty cycling

R=6;                  % Grid connecting resistance (Ohm)

L=2e-2;   %2e-3;      % Grid connecting reactance (H)

Iref= P/(3*Vac);      % Reference current (Irms)
```



As shown in the figure above, we get a better AC output current and the THD of the harmonic content is reduced significantly, this implies that we have shifted to high frequency the harmonic content and our output filter can now filter these out better (better reduced in the unipolar with THD =0.0008). This means that the three-level technique can achieve the same output voltage with reduced switching losses compared to the two-level. By utilizing the additional voltage levels, the switching frequency of the power switches can be

reduced, leading to lower switching losses. This can contribute to improved overall efficiency and reduced heat dissipation in the inverter.

Note:

- the THD of the voltage has not changed since it depends only on the amplitude modulation index that we keep fix. $m_f \neq m$
- in all these simulations, we are observing a phase shift between the output current and the output voltage in your simulation because of an inductive load. This is due to the inherent nature of inductive elements to cause a delay in the current response relative to the voltage.
- Mainly, the **tradeoff** that we used in this last simulation is linked to the fact that:
  - only increasing the output filter generate more delay of the output current, cost and not well for micro application.
  - In the other hand increasing only the frequency imply to gives less time to the commutation of the switches: limited switching speed, increased switching losses and cost.
- *Sinusoidal PWM* (three levels) can be implemented using a specific modulation strategy known as Zero Voltage Space Vector Modulation (ZVSM).

VI. Conclusion

In summary, we have seen the **unipolar modulation technique** used to drive the **Cascaded H-Bridge Three-Level Three-Phase Inverter** in the optimal way over the ***Sinusoidal PWM technique*** **(two levels)**. Where the presence of more voltage levels helps in reducing the high-frequency harmonics in the output.
In general, the three-level inverter typically requires more power electronic components and more complex control strategies compared to the two-level inverter. This can result in higher initial costs and increased complexity in system design and implementation.
These techniques allow precise control over the inverter output voltage waveform and help reduce harmonics and distortion, resulting in a cleaner, higher quality output voltage. They optimize the switching pattern of the inverter, minimizing power losses and maximizing overall efficiency. They help reduce switching losses and improve the overall energy conversion efficiency of the inverter. They allow precise control over positive and negative voltage levels and ensure that the inverter generates a cleaner, more sinusoidal output voltage, while minimizing the effects of distortion on connected loads.
These advantages make the cascade H-bridge three-level three-phase inverter with **unipolar modulation** a preferred choice in many applications where high-quality voltage, efficiency, and precise control are crucial factors. We indicate the application in electric vehicles/drives, motor drives, power supplies and more generally in all' industrial applications that need DC-AC inverters.