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NVIDIA Jetson TX2 J21 Header Pinout

JETSON TX2 HEADER PINOUT

This is the Jetson TX2 J21 GPIO Header Layout. Last updated July 18, 2018
The GPIO numbering is different than the [Jetson TX1 table](#).

Jetson TX2 J21 Header					
Sysfs GPIO	Connector Label	Pin	Pin	Connector Label	Sys GP
	3.3 VDC Power	1	2	5.0 VDC Power	
	SDA1 <i>General I2C Data 3.3.V, I2C Bus 1</i>	3	4	5.0 VDC Power	
	SCL1 <i>General I2C Clock 3.3.V, I2C Bus 1</i>	5	6	GND	

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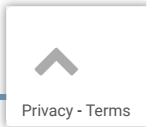
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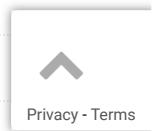
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gpio396	GPIO_GCLK			TXDO <i>UART #0 Transmit</i>	Android Caffe Camera CUDA
	<i>Audio Master Clock (1.8/3.3.V)</i>				
	GND			RXDO <i>UART #0 Receive</i>	Deep Learning Featured GPIO/I2C
	<i>UART #0 Request to Send</i>				
gpio466	GPIO_GEN0 <i>UART #0 Request to Send</i>			GPIO_GEN1 <i>Audio I2S #0 Clock</i>	gpio: Grinch Gstreamer GTC
gpio397	GPIO_GEN2 <i>Audio Code Interrupt</i>			GND	GTC 2015 GTC 2016 Hardware
gpio255	GPIO_GEN3 <i>From GPIO Expander (P17)</i>			GPIO_GEN4 <i>Unused</i>	gpio: Information JetPack Jetson Drone
	3.3 VDC Power			GPIO_GEN5 <i>Modem Wake AP GPIO</i>	gpio: Jetson Nano Jetson RACECAR Jetson Rover Jetson TX1
gpio429	SPI_MOSI <i>SPI #1 Master Out/Slave In</i>			GND	gpio: Jetson TX2 Jetson Xavier JetsonBot
gpio428	SPI1_MISO <i>SPI #1 Master In/Slave Out</i>			GPIO_GEN6 <i>From GPIO Expander (P16)</i>	gpio: News OpenCV Operating System Programming
gpio427	SPI_SCLK <i>SPI #1 Shift Clock</i>			SPI_CE0_N <i>SPI Chip Select #0</i>	gpio: Qt RACECAR/J Robotics



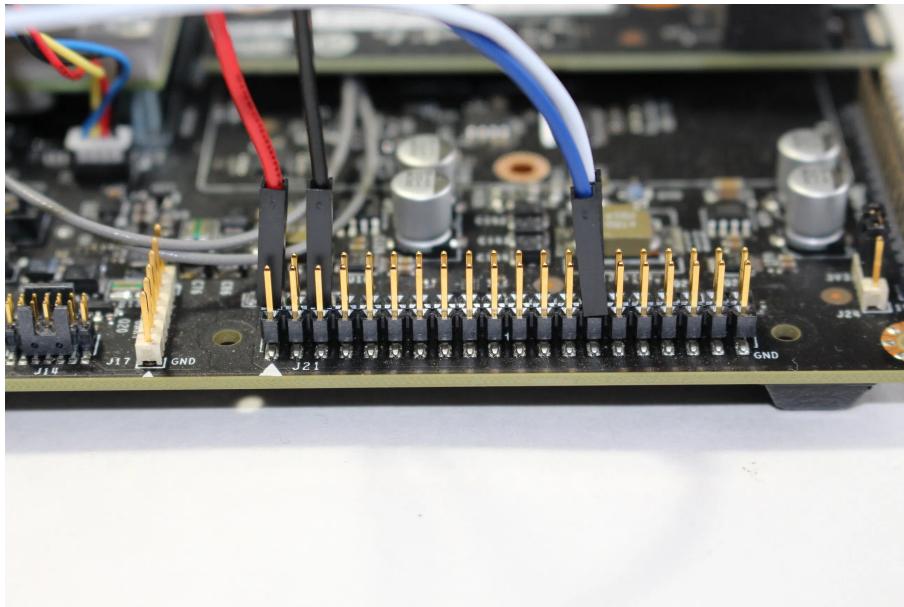
	GND	25	26	SPI_CE1_N SPI #1 Chip Select #1	ROS SDK Manager
	ID_SD <i>General I2C</i>	27	28	ID_SC <i>General I2C</i>	Software TensorFlow
	#1 Data (3.3V), I2C Bus 0			#1 Clock (3.3V), I2C Bus 0	Torch Tutorial
gpio398	GPIO5 <i>Audio Reset</i> (1.8/3.3V)	29	30	GND	UPenn ARC Vision Wireless
gpio298	GPIO6 <i>Motion Interrupt</i> (3.3V)	31	32	GPIO12 <i>Unused</i>	gpio: TAGS
gpio389	GPIO13 <i>AP Wake Bt</i> <i>GPIO</i>	33	34	GND	ANDROID BATTERY CAMERA CASE CUDA CUDNN DEEP LEARNING
gpio395	GPIO19 <i>AUDIO I2S #0</i> <i>Left/Right Clock</i>	35	36	GPIO16 <i>UART #0</i> <i>Clear to Send</i>	gpio: DEMONSTRATION ENCLOSURE GPS GSTREAMER GTC 2015 HACKING IMU
gpio388	GPIO26 (3.3V)	37	38	GPIO20 <i>Audio I2S #0</i> <i>Data in</i>	gpio: INFORMATION IROBOT CREATE 2 JETPACK
	GND	39	40	GPIO21 <i>Audio I2S #0</i> <i>Data in</i>	gpio: JETSON TK1 JETSONTK1 QUADCOPTER KINECT L4T 21.1 L4T 21.3 L4T 21.4 L4T 23.1

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NVIDIA Jetson TX1/TX2 J21 Header

Note: The arrow on the circuit board points to pin 1. Pin 2 is behind pin 1 in the picture.

The I2C bus numbers are swapped in comparison to the Jetson TX1.

I2C Bus 0 address 0x0040-0x0043 are the INA3221x power monitors.

Here is a spreadsheet which maps the J21 signals back through the carrier board, to the module, and to the Tegra chip itself:

[Google Doc Spreadsheet](#)

[Jetson TX2 GPIO mapping \(link to .xlsx spreadsheet\)](#)

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