

FPGA GPIO Control with Device Driver

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본인의 Home 계정에서 시작하도록 한다.

파일명은 마음대로 지정해도 상관없다만 hardware 라고 되어 있는 부분을 기억해야 한다.

```
root@sdr-Samsung-DeskTop-System:/home/sdr# cd lab6
root@sdr-Samsung-DeskTop-System:/home/sdr/lab6# mkdir hardware
root@sdr-Samsung-DeskTop-System:/home/sdr/lab6# cd hardware
root@sdr-Samsung-DeskTop-System:/home/sdr/lab6/hardware#
```

이후에 아래의 작업들을 하게 될텐데 우선은 Vivado 를 구동시키도록 한다.

```
sdr@sdr-Samsung-DeskTop-System: ~/zynq_zybo/lab6
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6$ petalinux-create -t project -n
software --template zynq
INFO: Create project: software
INFO: New project successfully created in /home/sdr/zynq_zybo/lab6/software
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6$
```

```
sdr@sdr-Samsung-DeskTop-System: ~/zynq_zybo/lab6/hardware/driver_lab.sdk
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6$ clear
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6$ petalinux-create -t project -n softwar
e --template zynq
INFO: Create project: software
INFO: New project successfully created in /home/sdr/zynq_zybo/lab6/software
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6$ cd hardware/driver_lab.sdk/
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/hardware/driver_lab.sdk$ petalinux-conf
ig --get-hw-description -p ~/zynq_zybo/lab6/software
INFO: Checking component...
INFO: Getting hardware description...
INFO: Rename system_wrapper.hdf to system.hdf
```



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Quick Start



Create New Project



Open Project



Open Example Project

Tasks



Manage IP



Open Hardware Manager



Xilinx Tcl Store

Information Center



Documentation and Tutorials



Quick Take Videos



Release Notes Guide



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XILINX
PROGRAMMABLE**New Project****Quick Start**

Create Ne

Tasks

Mana

Information

Documentation

Create a New Vivado Project

This wizard will guide you through the creation of a new project.

To create a Vivado project you will need to provide a name and a location for your project files. Next, you will specify the type of flow you'll be working with. Finally, you will specify your project sources and choose a default part.

To continue, click Next.

< Back

Next >

Finish

Cancel



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PRO

New Project

Project Name

Enter a name for your project and specify a directory where the project data files will be stored.

Project name:

Project location:

Create project subdirectory

Project will be created at: /home/sdr/lab6/hardware

Quick Start



Create New

Tasks



Manage

Information



Documentation



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Next >

Finish

Cancel



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PRO

New Project

Project Type

Specify the type of project to create.

RTL Project

You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.

Do not specify sources at this time

Post-synthesis Project: You will be able to add sources, view device resources, run design analysis, planning and implementation.

Do not specify sources at this time

I/O Planning Project

Do not specify design sources. You will be able to view part/package resources.

Imported Project

Create a Vivado project from a Synplify, XST or ISE Project File.

Example Project

Create a new Vivado project from a predefined template.

Quick Start



Create New

Tasks



Manage

Information



Documentation

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Next >

Finish

Cancel



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XILINX PRO

New Project

Default Part

Choose a default Xilinx part or board for your project. This can be changed later.

Select: Parts Boards

Filter

Vendor:

All

Display Name:

All

Board Rev:

Latest

Reset All Filters

Search:

Display Name	Vendor	Board Rev	Part	I/O Pin Count	File Ve
Zybo	digilentinc.com	B.3	xc7z010clg400-1	400	1.0
ZedBoard Zynq Evaluation and Development Kit	ern.avnet.com	d	xc7z020clg484-1	484	1.3
Artix-7 AC701 Evaluation Platform	xilinx.com	1.1	xc7a200tfbg676-2	676	1.2
ZYNQ-7 ZC702 Evaluation Board	xilinx.com	1.0	xc7z020clg484-1	484	1.2

◀ ▶

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Next >

Finish

Cancel



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New Project

Quick Start



Create New

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XILINX
ALL PROGRAMMABLE™

New Project Summary

ⓘ A new RTL project named 'driver_lab' will be created.

ⓘ The default part and product family for the new project:

Default Board: Zynq

Default Part: xc7z010clg400-1

Product: Zynq-7000

Family: Zynq-7000

Package: clg400

Speed Grade: -1

To create the project, click Finish

< Back

Next >

Finish

Cancel

driver_lab - [/home/sdr/lab6/hardware/driver_lab.xpr] - Vivado 2015.4

File Edit Flow Tools Window Layout View Help

Search commands Ready

Flow Navigator

Project Manager - driver_lab

Sources

- Design Sources
- Constraints
- Simulation Sources
 - sim_1

Hierarchy Libraries Compile Order

Sources Templates

Properties

Select an object to see properties

Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Failed R
synth_1	constrs_1	Not started						
impl_1	constrs_1	Not started						

Tcl Console Messages Log Reports Design Runs

Project Summary

- bo (xc7z010clg400-1)
- it defined
- rilog
- zed

Diligentinc.com:zybo:part0:1.0
Xilinx/Vivado/2015.4/data/boards/board_files
www.digilentinc.com

Implementation

Status:	Not
Messages:	No e
Part:	xc7z01
Strategy:	Viva
Incremental compile:	None

Project Manager

- Project Settings
- Add Sources
- Language Templates
- IP Catalog

IP Integrator

- Create Block Design
- Open Block Design
- Generate Block Design

Simulation

- Simulation Settings
- Run Simulation

RTL Analysis

- Elaboration Settings
- Open Elaborated Design

Synthesis

- Synthesis Settings
- Run Synthesis
- Open Synthesized Design

Implementation

- Implementation Settings
- Run Implementation
- Open Implemented Design

Program and Debug

- Bitstream Settings
- Generate Bitstream

Navigator



Project Manager

Project Settings

Add Sources

Language Templates

IP Catalog

Integrator

Create Block Design

Open Block Design

Generate Block Design

Simulation

Simulation Settings

Run Simulation

Analysis

Elaboration Settings

Open Elaborated Design

Synthesis

Synthesis Settings

Run Synthesis

Open Synthesized Design

Implementation

Implementation Settings

Run Implementation

Open Implemented Design

Program and Debug

Bitstream Settings

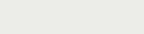


Project Manager - driver_lab

Sources



- Design Sources
- Constraints
- Simulation Sources
 - sim_1



Project Summary

- bo (xc7z010clg400-1)
- it_defined
- rilog
- xed

intinc.com:zybo:part0:1.0

do/2015.4/data/boards/board_files
intinc.com

Hierarchy



Create Block Design



Please specify name of block design.



Design name:

system

Directory:

<Local to Project>

Specify source set:

Design Sources

OK

Cancel

Design



synthesis_1	Not started
impl_1	Not started
constraints_1	Not started



Implementation

Status:

Messages:

Part:

Strategy:

Incremental compile:

NS	WHS	THS	TPWS



Navigator

Project Manager

- Project Settings
- Add Sources
- Language Templates
- IP Catalog

IP Integrator

- Create Block Design
- Open Block Design
- Generate Block Design

Simulation

- Simulation Settings
- Run Simulation

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- Elaboration Settings
- Open Elaborated Design

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- Synthesis Settings
- Run Synthesis
- Open Synthesized Design

Implementation

- Implementation Settings
- Run Implementation
- Open Implemented Design

Program and Debug

- Bitstream Settings
- Generate Bitstream

Block Design - system

Design



system

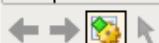
Sources

Design

Signals

Board

Properties



Select an object to see properties

Tcl Console

```
start_gui
create_project driver_lab . -part xc7z010clg400-1
INFO: [IP_Flow 19-234] Refreshing IP repositories
INFO: [IP_Flow 19-1704] No user IP repositories specified
INFO: [IP_Flow 19-2313] Loaded Vivado IP repository '/opt/Xilinx/Vivado/2015.4/data/ip'.
set_property board_part digilentinc.com:zybo:part0:1.0 [current_project]
create_bd_design "system"
Wrote : </home/sdr/lab6/hardware/driver_lab.srcc/sources_1/bd/system/system.bd>
```

Type a Tcl command here

Tcl Console

Messages

Log

Reports

Design Runs

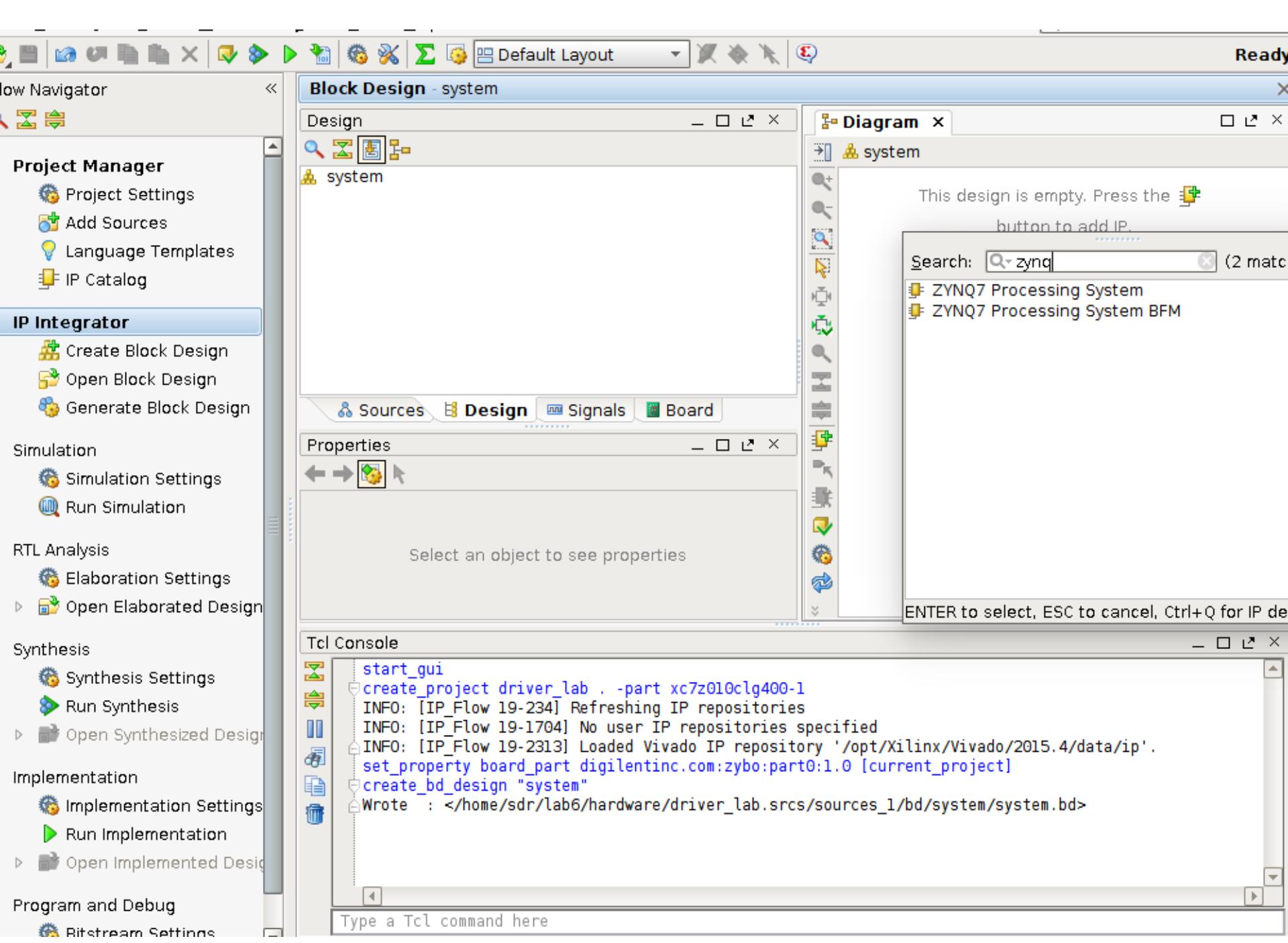
Diagram x

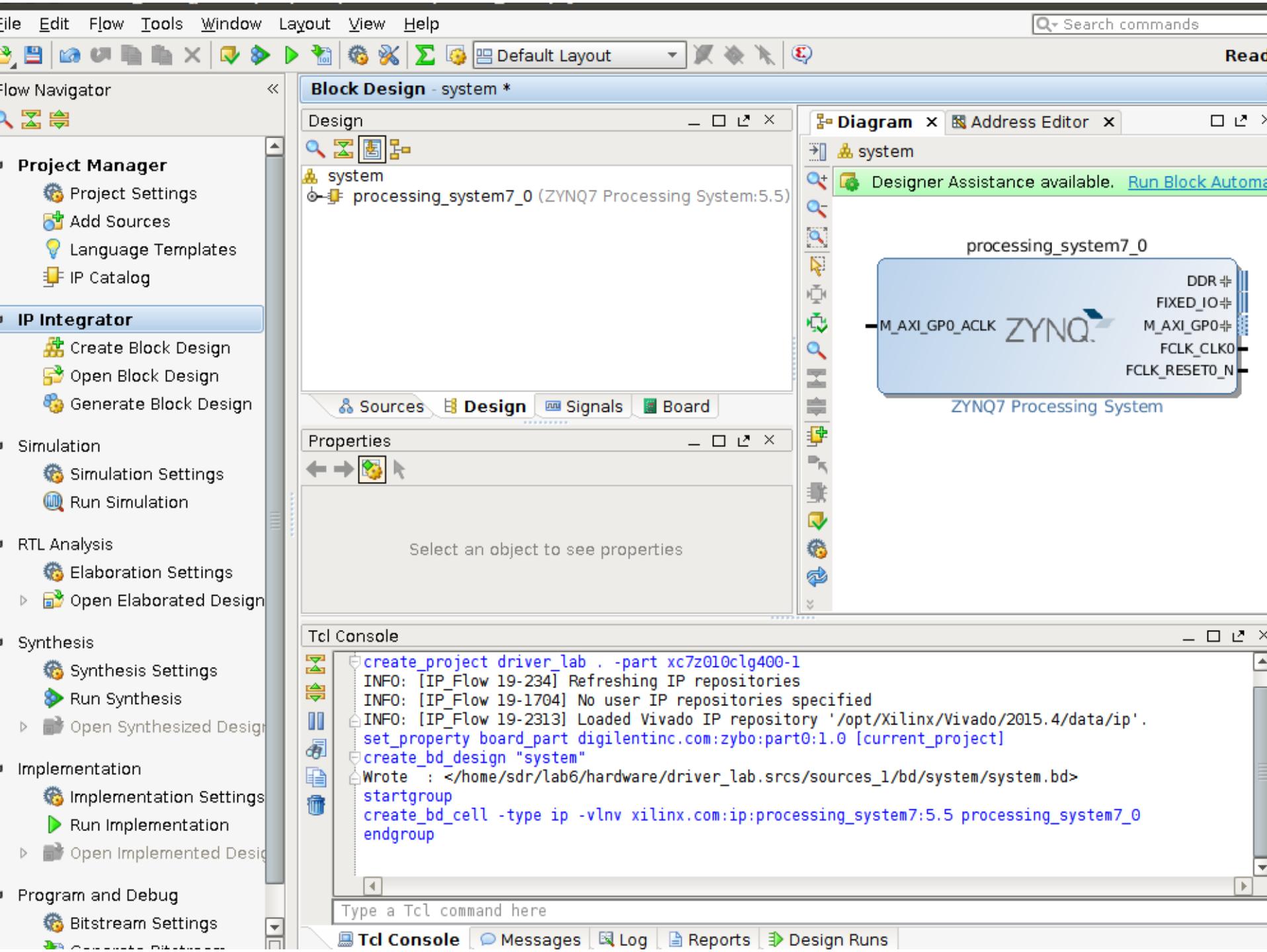
system

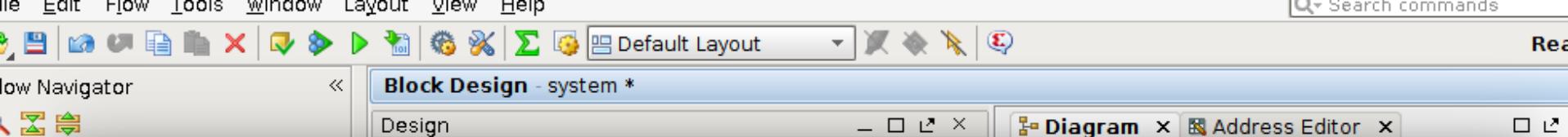


This design is empty. Press the button to add IP.

Add IP







Proj

IP In

Simu

RTL

Synt

Impl

Prog

Bitstream Settings

Generate Bitstream

Type a Tcl command here

Tcl Console

Messages

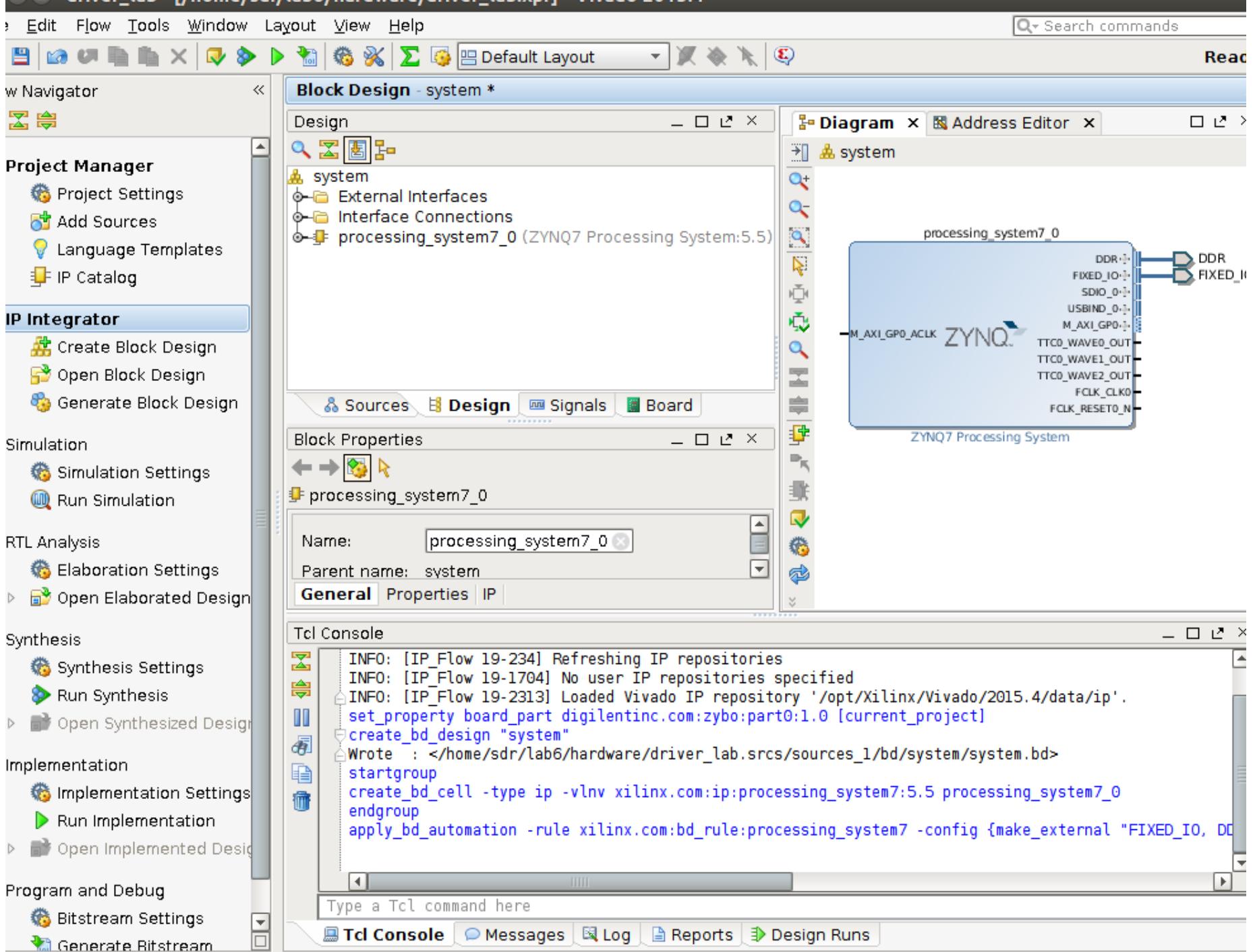
Log

Reports

Design Runs

OK

Cancel



Re-customize IP



ZYNQ7 Processing System (5.5)

Documentation Presets IP Location Import XPS Settings

Page Navigator

Zynq Block Design

PS-PL Configuration

Peripheral I/O Pins

MIO Configuration

Clock Configuration

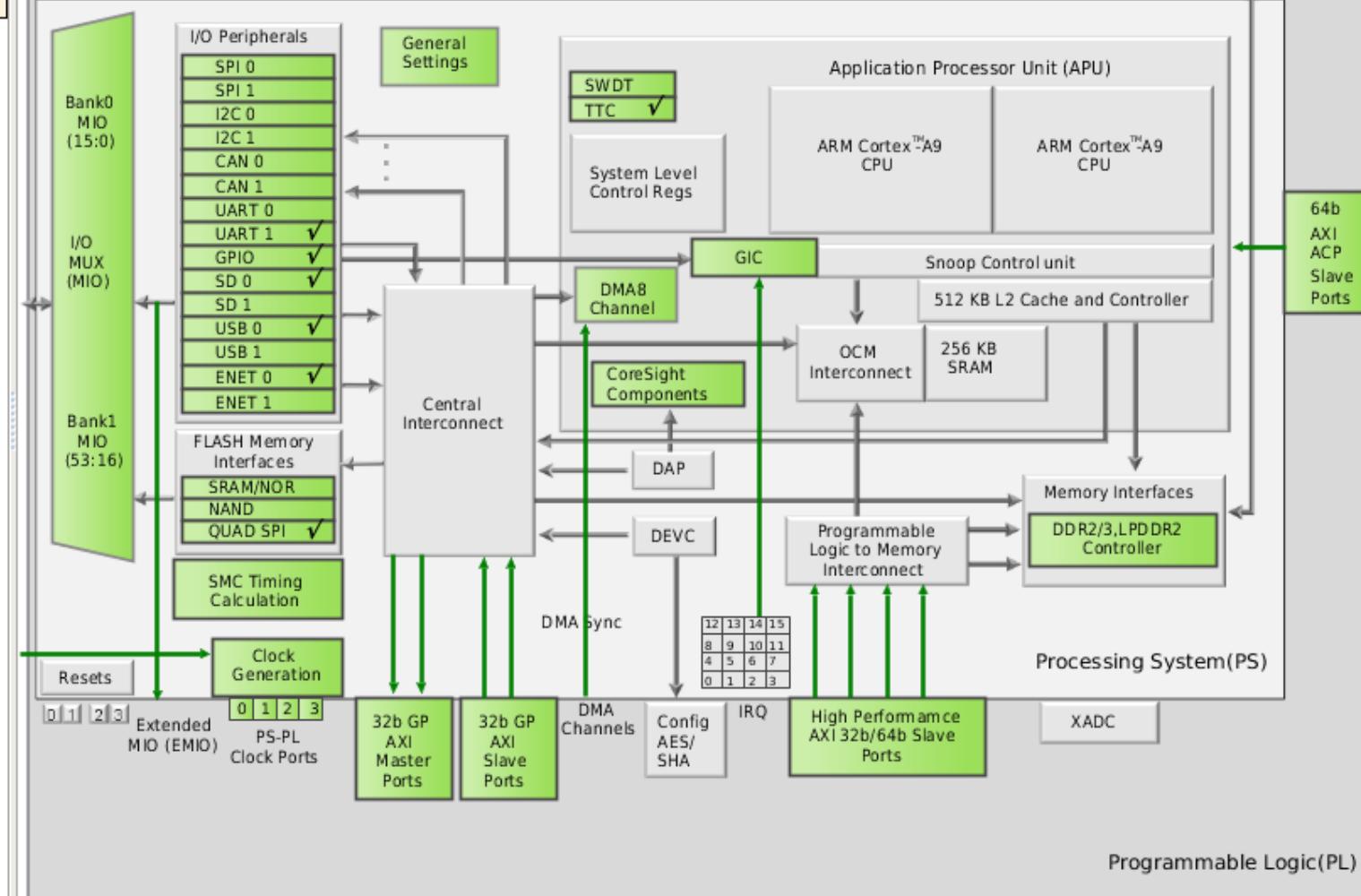
DDR Configuration

SMC Timing Calculation

Interrupts

Summary Report

Zynq Block Design



OK

Cancel

Re-customize IP

ZYNQ7 Processing System (5.5)



Documentation Presets IP Location Import XPS Settings

Page Navigator <<

Zynq Block Design

PS-PL Configuration

Peripheral I/O Pins

MIO Configuration

Clock Configuration

DDR Configuration

SMC Timing Calculation

Interrupts

Summary Report

MIO Configuration

Bank 0 I/O Voltage LVCMS 3.3V Bank 1 I/O Voltage LVCMS 1.8V



Search:

Peripheral	IO	Signal	IO Type	Speed	Pullup	Dir
Memory Interfaces						
I/O Peripherals						
ENET 0	MIO 16 .. 27					
ENET 1						
USB 0						
USB 1						
SD 0	MIO 40 .. 45					
SD 1						
UART 0						
UART 1	MIO 48 .. 49					
I2C 0						
I2C 1						
SPI 0						
SPI 1						
CAN 0						
CAN 1						
GPIO						
GPIO MIO						
EMIO GPIO (Width)						
ENET Reset						



OK

Cancel

[Documentation](#) [Presets](#) [IP Location](#) [Import XPS Settings](#)

Page Navigator <>

Zynq Block Design

PS-PL Configuration

Peripheral I/O Pins

MIO Configuration

Clock Configuration

DDR Configuration

SMC Timing Calculation

Interrupts

Clock Configuration

[Basic Clocking](#) [Advanced Clocking](#)Input Frequency (MHz) CPU Clock Ratio Search:

Component	Clock Source	Requested Freq...	Actual Frequency...	Range(MHz)
Processor/Memory Clocks				
IO Peripheral Clocks				
PL Fabric Clocks				
FCLK_CLK0	IO PLL	100	100.000000	0.100000 : 250.00000...
FCLK_CLK1	IO PLL	50	50.000000	0.100000 : 250.00000...
FCLK_CLK2	IO PLL	50	50.000000	0.100000 : 250.00000...
FCLK_CLK3	IO PLL	50	50.000000	0.100000 : 250.00000...
System Debug Clocks				
Timers				

OK

Cancel

Edit Flow Tools Window Layout View Help Search commands

Navigator

Object Manager

- Project Settings
- Add Sources
- Language Templates
- IP Catalog

Integrator

- Create Block Design
- Open Block Design
- Generate Block Design

Simulation

- Simulation Settings
- Run Simulation

Analysis

- Elaboration Settings
- Open Elaborated Design

Synthesis

- Synthesis Settings
- Run Synthesis
- Open Synthesized Design

Implementation

- Implementation Settings
- Run Implementation
- Open Implemented Design

Program and Debug

- Bitstream Settings
- Generate Bitstream

processing_system7_0

Block Design - system *

Design

system

- External Interfaces
- Interface Connections
- processing_system7_0 (ZYNQ7 Processing System:5.5)

Sources Design Signals Board

Block Properties

processing_system7_0

Name: processing_system7_0

Parent name: system

General Properties IP

Tcl Console

```
set_property board_part digilentinc.com:zybo:part0:1.0 [current_project]
create_bd_design "system"
Wrote : </home/sdr/lab6/hardware/driver_lab.srsc/sources_1/bd/system/system.bd>
startgroup
create_bd_cell -type ip -vlnv xilinx.com:ip:processing_system7:5.5 processing_system7_0
endgroup
apply_bd_automation -rule xilinx.com:bd_rule:processing_system7 -config {make_external "FIXED_IO, DD
startgroup
set_property -dict [list CONFIG.POW_QSPI_GRP_SINGLE_SS_ENABLE {1} CONFIG.POW_USB0_PERIPHERAL_ENABLE
endgroup
```

Type a Tcl command here

Tcl Console Messages Log Reports Design Runs

Diagram Address Editor

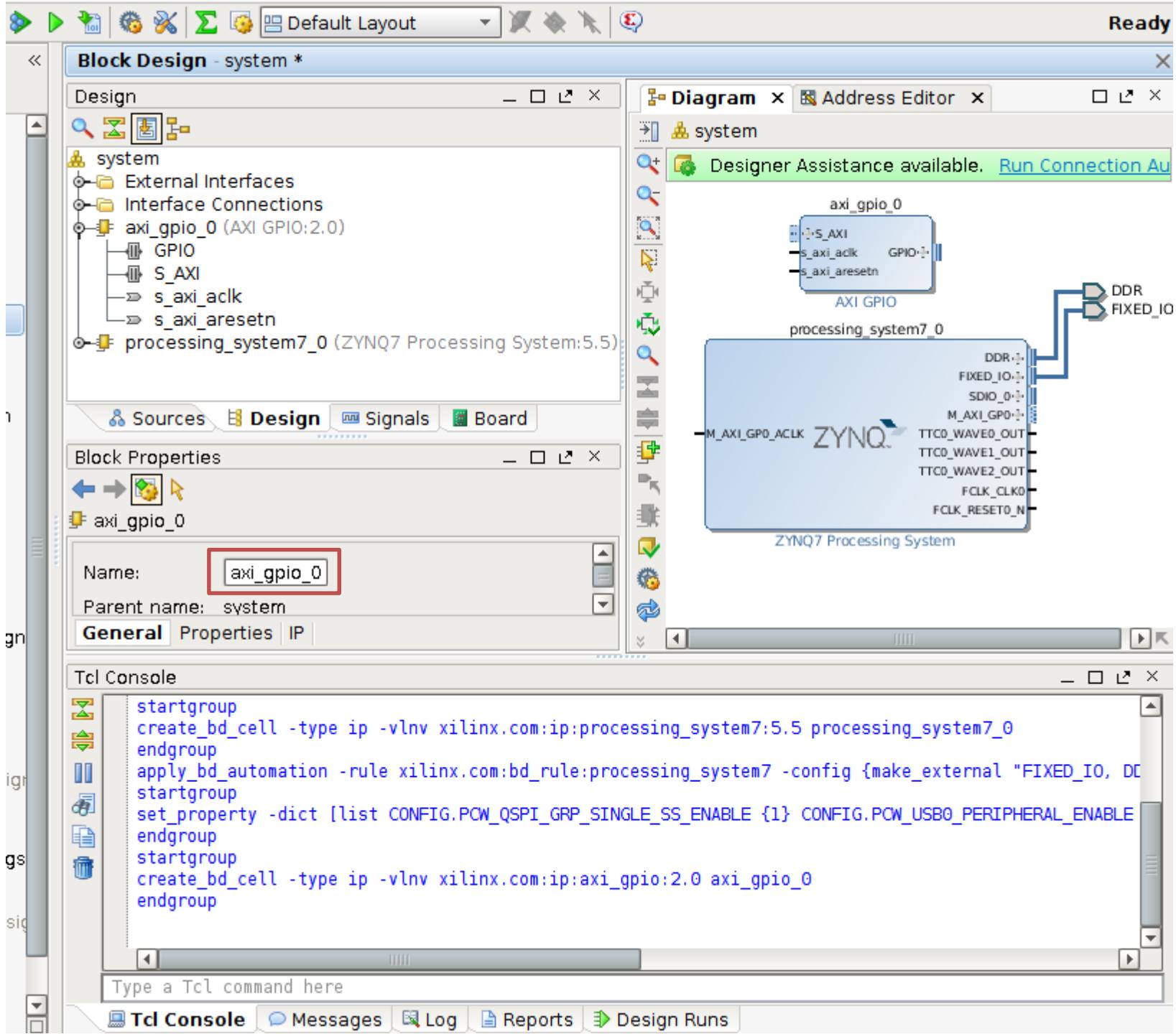
system

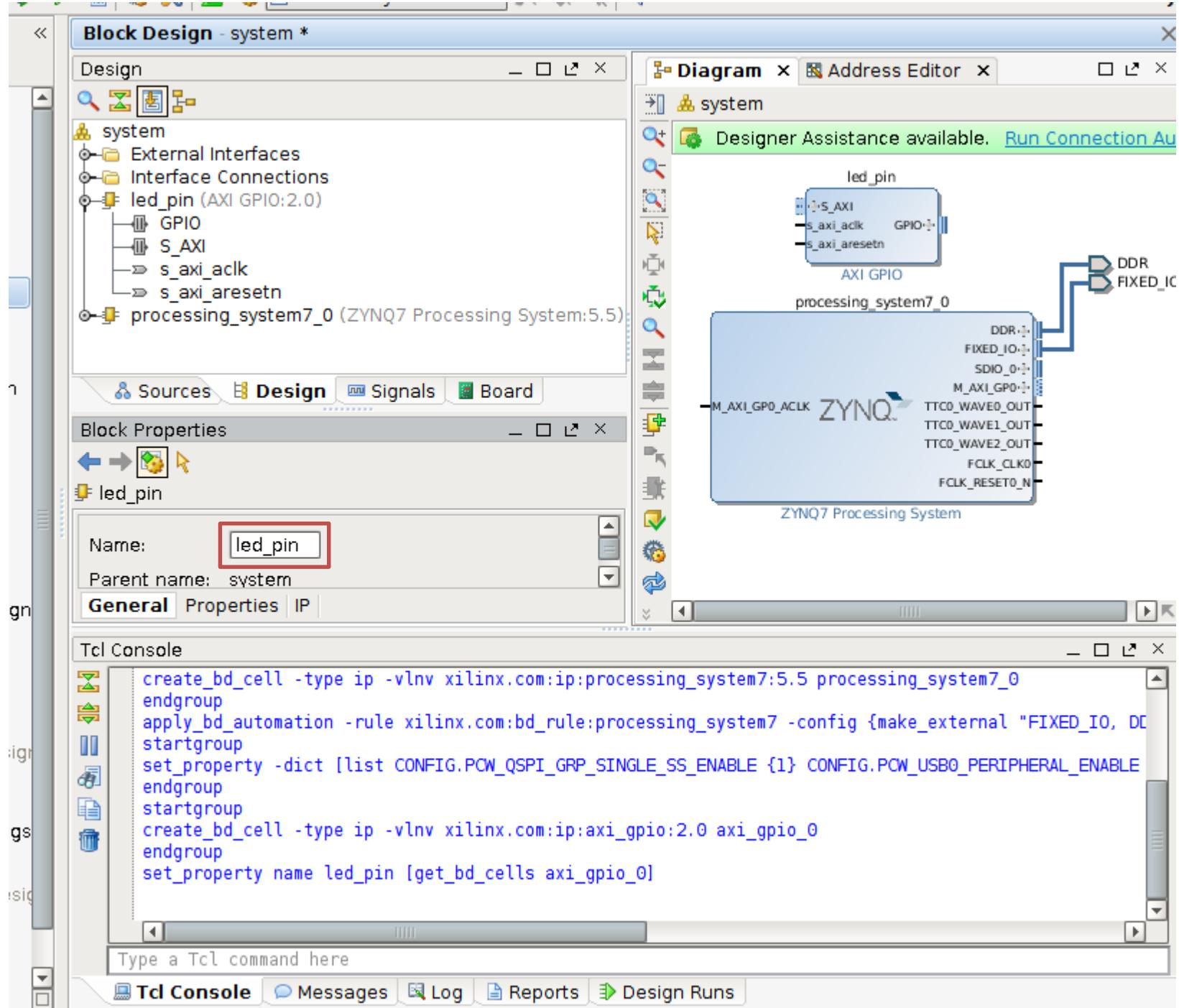
Search: gpio (1)

AXI GPIO

M_AX

ENTER to select, ESC to cancel, Ctrl+Q for IP





Re-customize IP

AXI GPIO (2.0)

Documentation IP Location

Show disabled ports

Component Name: system_axi_gpio_0_0

Board **IP Configuration**

GPIO

All Inputs
 All Outputs

GPIO Width: 1 [1 - 32]
Default Output Value: 0x00000000 [0x00000000, 0xFFFFFFFF]
Default Tri State Value: 0xFFFFFFFF [0x00000000, 0xFFFFFFFF]

Enable Dual Channel

GPIO 2

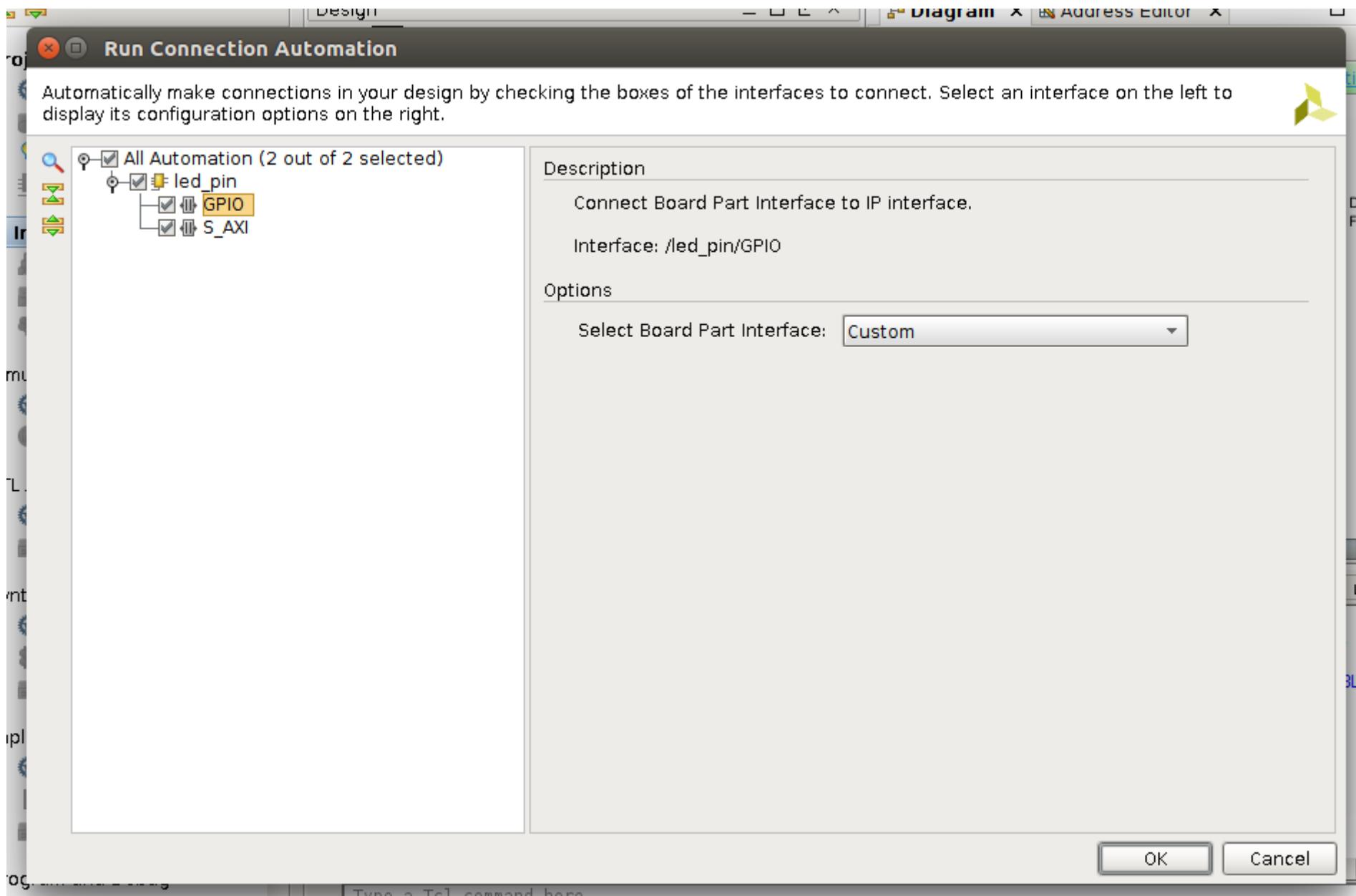
All Inputs
 All Outputs

GPIO Width: 32 [1 - 32]
Default Output Value: 0x00000000 [0x00000000, 0xFFFFFFFF]
Default Tri State Value: 0xFFFFFFFF [0x00000000, 0xFFFFFFFF]

Enable Interrupt

S_AXI
- s_axi_aclk GPIO+
- s_axi_aresetn

OK Cancel



Block Design - system *

Design

- system
 - External Interfaces
 - Interface Connections
 - Nets
 - led_pin (AXI GPIO:2.0)
 - GPIO
 - S_AXI
 - s_axi_aclk
 - s_axi_aresetn
 - processing_system7_0 (ZYNQ7 Processing System:5.5)

Sources Design Signals Board

Address Segment Properties

- SEG_led_pin_Reg

Name: SEG_led_pin_Reg

Full name: processing_system7_0/Data/SEG_led_pi

Diagram

Address Editor

Base Name	Offset Address	Range	High Address
	0x4120_0000	64K	0x4120_FFFF

Tcl Console

```
INFO: [Ipptcl 7-1463] No Compatible Board Interface found. Board Tab not created in customize GUI
</led_pin/S_AXI/Reg> is being mapped into </processing_system7_0/Data> at <0x41200000 [ 64K ]>
apply_bd_automation -rule xilinx.com:bd_rule:board -config {Board_Interface "Custom" } [get_bd_intf_pins /led_pin]
INFO: [board_rule:/led_pin-100] set_property CONFIG.USE_BOARD_FLOW true [get_bd_cells /led_pin]
INFO: [board_rule:/led_pin-100] set_property CONFIG.GPIO_BOARD_INTERFACE Custom [get_bd_cells /led_pin]
INFO: [board_rule:/led_pin-100] create_bd_intf_port -mode Master -vlnv xilinx.com:interface:gpio_rtl
INFO: [board_rule:/led_pin-100] connect_bd_intf_net /gpio_rtl /led_pin/GPIO
WARNING: [board_rule:/led_pin-100] Board automation did not generate location constraint for /led_pin
endgroup
regenerate_bd_layout
```

Block Design - system *

Design

system

- External Interfaces
- Interface Connections
- Nets
- led_pin (AXI GPIO:2.0)
 - GPIO
 - S_AXI
 - s_axi_aclk
 - s_axi_aresetn
- processing_system7_0 (ZYNQ7 Processing System:5)

Sources Design Signals Board

Diagram

system

Validate Design

Validation successful. There are no errors or critical warnings in this design.

OK

Tcl Console

```
INFO: [board_rule:/led_pin-100] set_property CONFIG.USE_BOARD_FLOW true [get_bd_cells /led_pin]
INFO: [board_rule:/led_pin-100] set_property CONFIG.GPIO_BOARD_INTERFACE Custom [get_bd_cells /led_p
INFO: [board_rule:/led_pin-100] create_bd_intf_port -mode Master -vlnv xilinx.com:interface:gpio_rtl
INFO: [board_rule:/led_pin-100] connect_bd_intf_net /gpio_rtl /led_pin/GPIO
WARNING: [board_rule:/led_pin-100] Board automation did not generate location constraint for /led_pi
endgroup
regenerate_bd_layout
save_bd_design
Wrote : </home/sdr/lab6/hardware/driver_lab.srcts/sources_1/bd/system/system.bd>
validate_bd_design
```

Block Design - system *

Sources Diagram Address Editor

Generate Output Products

The following output products will be generated.

Preview

- system.bd (Global)
 - Synthesis
 - Implementation
 - Simulation

Synthesis Options

Location:
 Global
 Out of context per IP
 Out of context per Block Design

Tcl Console

INFO INFO INFO INFO
WARNING: end reg save Wrote validate

Run Settings

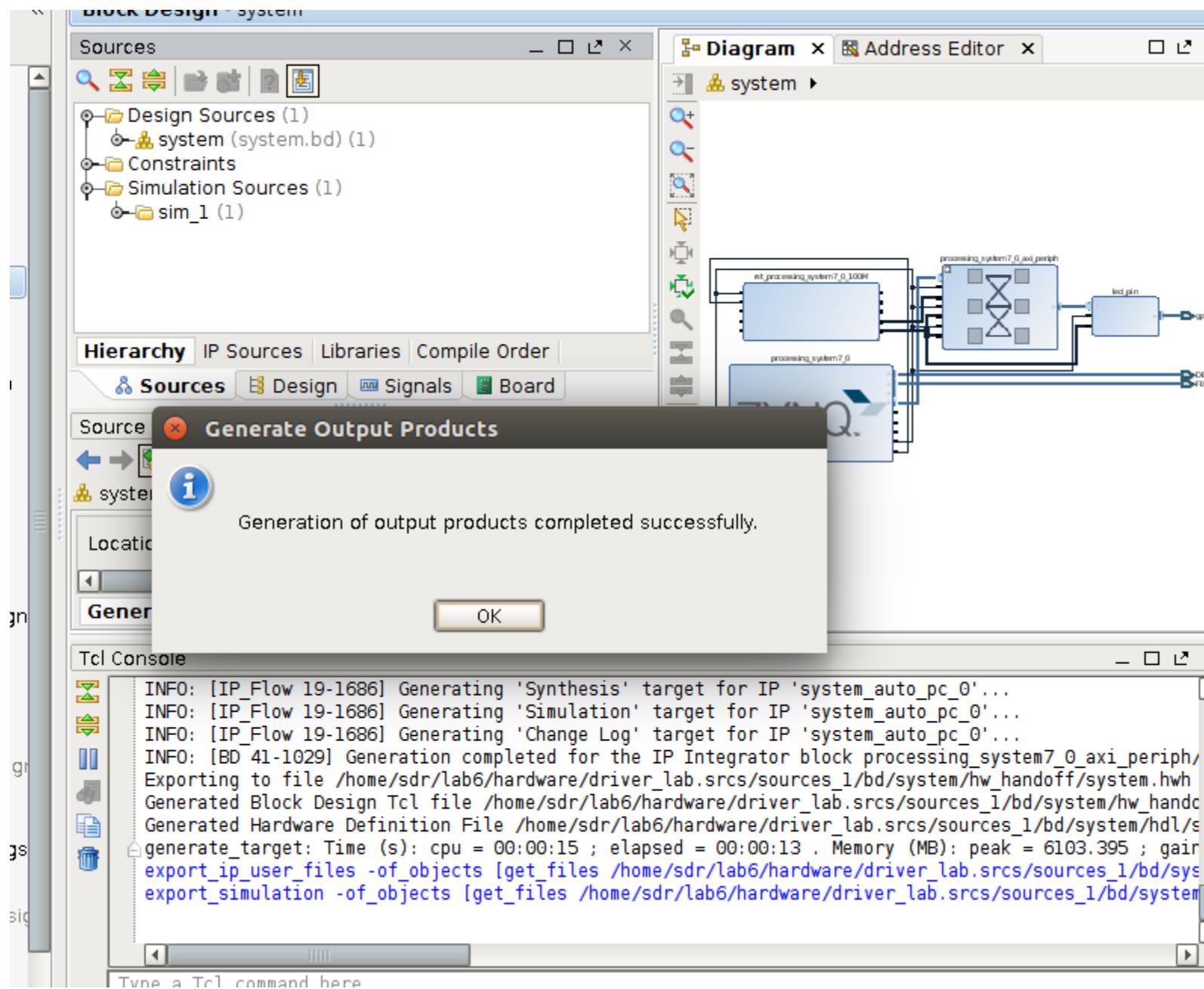
On local host: Number of jobs: 4
 On remote hosts Configure Hosts
 Use LSF: Configure LSF

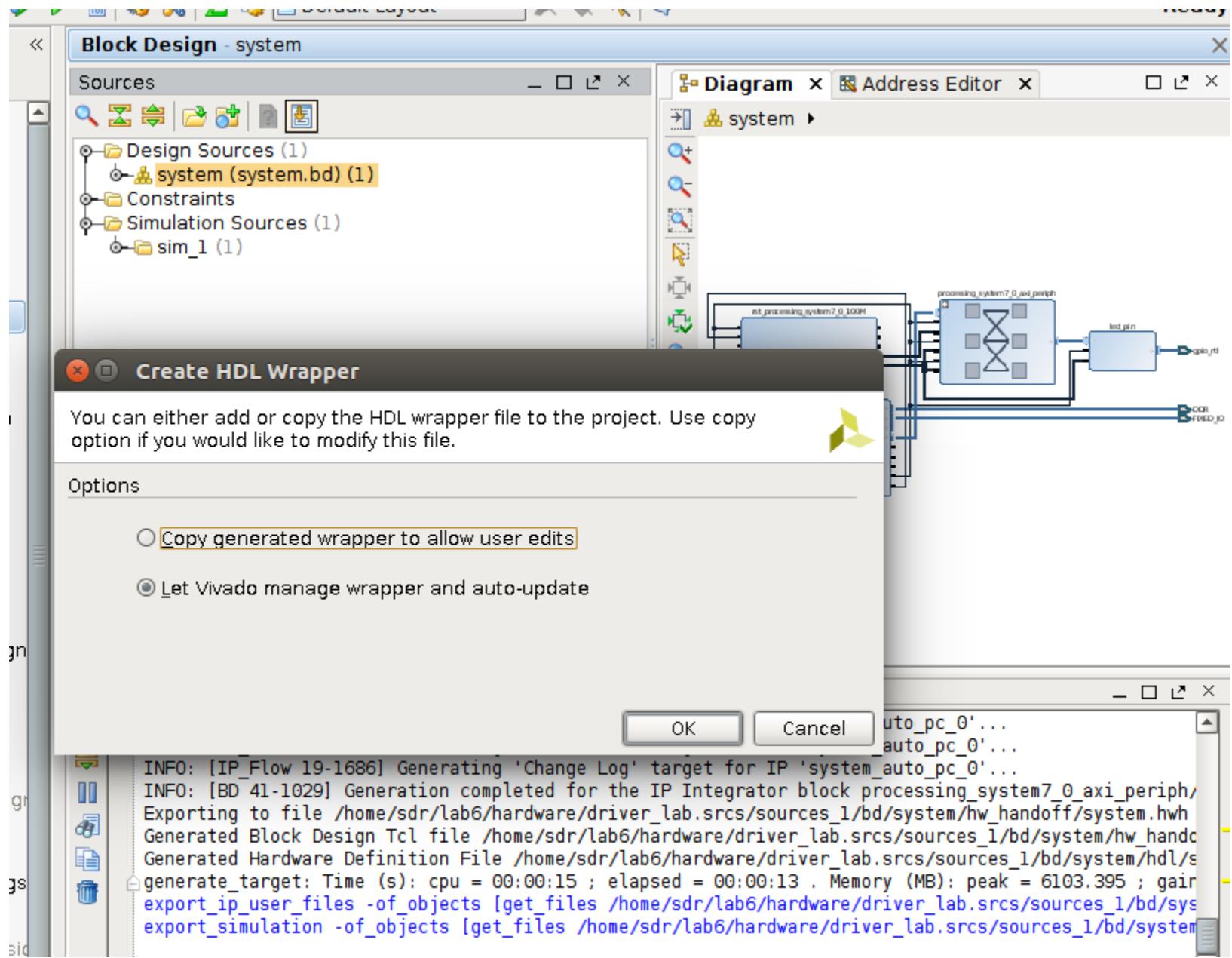
Diagram

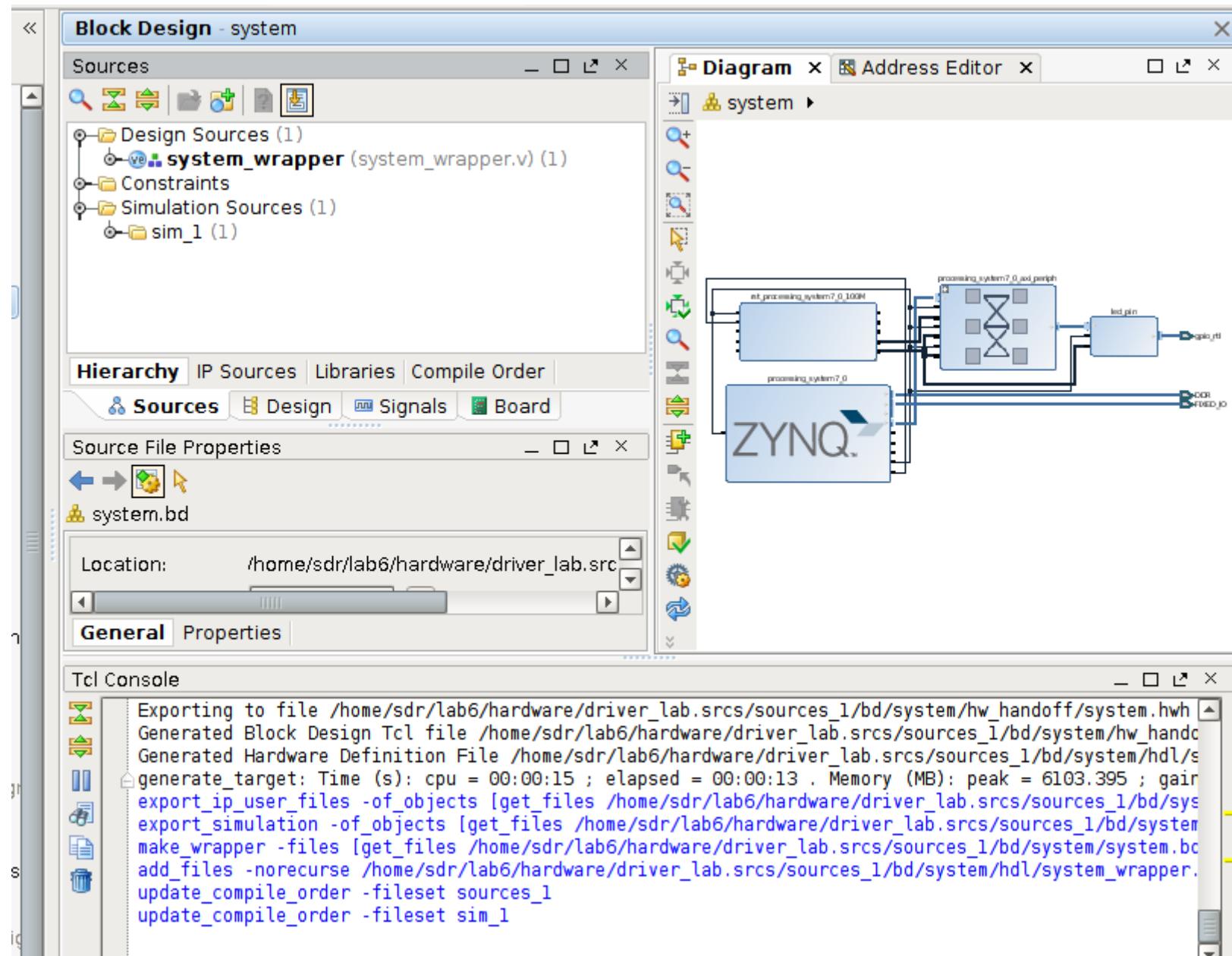
Address Editor

```
BOARD_FLOW true [get_bd_cells /led_pin]
BOARD_INTERFACE Custom [get_bd_cells /led_p
Master -vlnv xilinx.com:interface:gpio_rtl
_gpio_rtl /led_pin/GPIO
ot generate location constraint for /led_pi
_1/bd/system/system.bd>
```

Type a Tcl command here







VIVADO

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Block Design - system

Sources Diagram Address Editor

Add Sources

Add Sources

This guides you through the process of adding and creating sources for your project

- Add or create constraints
- Add or create design sources
- Add or create simulation sources
- Add or create DSP sources
- Add existing block design sources
- Add existing IP

To continue, click Next

< Back Next > Finish Cancel

Add Sources

Add or Create Constraints

Specify or create constraint files for physical and timing constraint to add to your project.

Specify constraint set: constrs_1 (active)

Create Constraints File

Create a new constraints file and add it to your project

File type: XDC

File name: driver

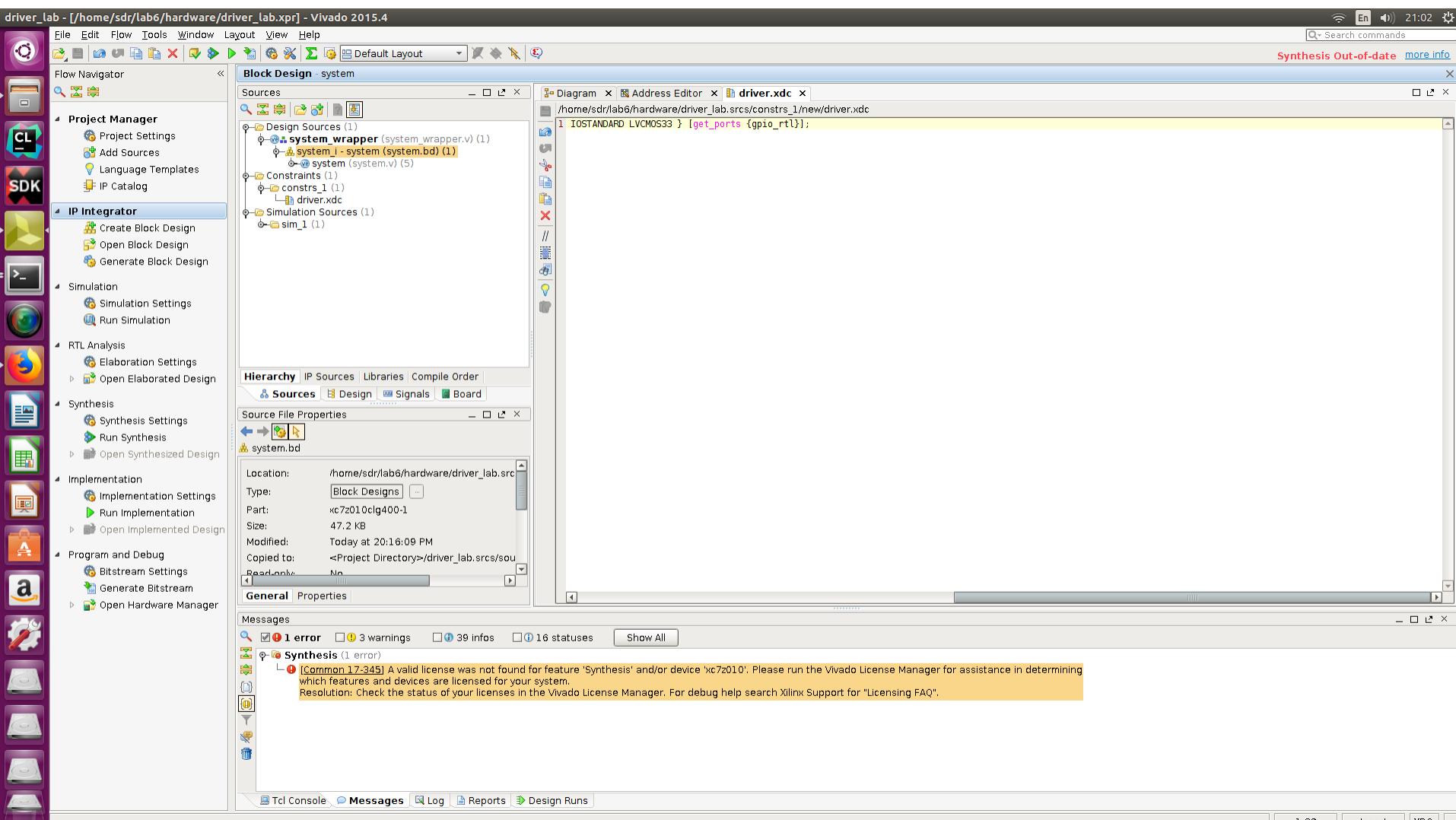
File location: <Local to Project>

OK Cancel

Add Files Create File

Copy constraints files into project

< Back Next > Finish Cancel



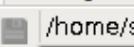
Block Design - system

Sources



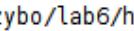
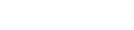
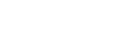
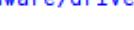
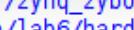
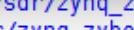
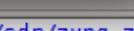
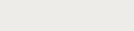
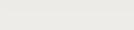
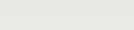
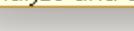
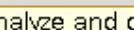
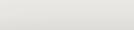
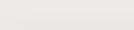
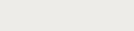
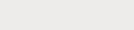
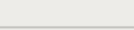
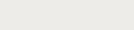
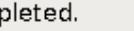
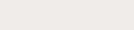
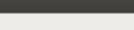
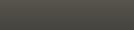
- Design Sources (1)
 - system_wrapper (system_wrapper.v) (1)
- Constraints (1)
 - constrs_1 (1)
 - driver.xdc
- Simulation Sources (1)
 - sim_1 (1)

Diagram



/home/sdr/zynq_zynbo/lab6/hardware/driver_lab.srscs/constrs_1/new

1: { PACKAGE_PIN T20 IOSTANDARD LVCMOS33 } [get_ports {gpi



Synthesis Completed



Synthesis successfully completed.

Next

Run Implementation

Open Synthesized Design

View Reports

Analyze and constrain a post synthesis netlist design

Don't show this dialog again

OK

Cancel

Tcl Console

```
export_ip_user_files -of_objects [get_files /home/sdr/zynq_zynbo/lab6/hardware/driver_lab.srscs/sources_1/bd/system/system.bd]
export_simulation -of_objects [get_files /home/sdr/zynq_zynbo/lab6/hardware/driver_lab.srscs/sources_1/bd/system/system.bd]
make_wrapper -files [get_files /home/sdr/zynq_zynbo/lab6/hardware/driver_lab.srscs/sources_1/bd/system/system.bd]
add_files -norecurse /home/sdr/zynq_zynbo/lab6/hardware/driver_lab.srscs/sources_1/bd/system/hdl/system_wrapper.v
update_compile_order -fileset sources_1
update_compile_order -fileset sim_1
save_bd_design
launch_runs synth_1
[Wed Mar 28 21:16:15 2018] Launched synth_1...
Run output will be captured here: /home/sdr/zynq_zynbo/lab6/hardware/driver_lab.runs/synth_1/runme.log
```

Properties Clock Regions

I/O Ports

Name	Direction	Board Part Pin	Board Part Interface	Neg Diff Pair	Site	Fixed	Bank
All ports (131)						✓	502 (M)
DDR_1497 (71)	INOUT					✓	(Multiple) (M)
FIXED_IO_1497 (59)	INOUT					✓	34 LV
GPIO_8845 (1)	INOUT					✓	34 LV
gpio_rtl_tri_io (1)	INOUT				T20	✓	34 LV
gpio_rtl_tri_io[0]	INOUT					✓	34 LV
Scalar ports (0)							
Scalar ports (0)							

Bitstream Generation Completed



Bitstream Generation successfully completed.

Next

Open Implemented Design

View Reports

Open Hardware Manager

Don't show this dialog again

OK

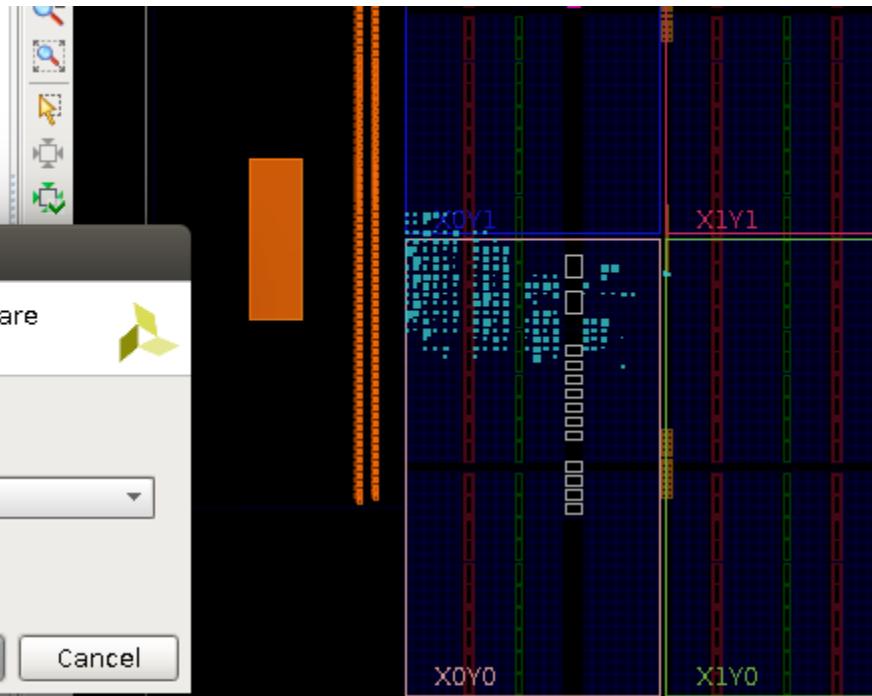
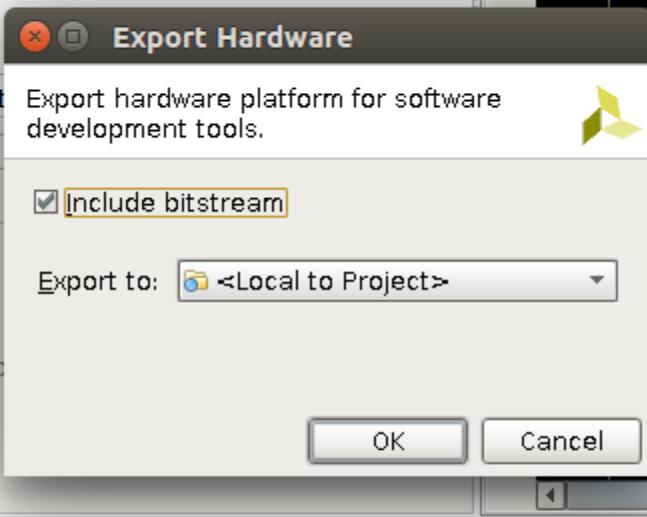
Cancel

General Properties

Name: gpio_r
Direction: INOUT
Site: T20
Site type: IO_L15

Tcl Console

```
place_ports {gpio_rtl_tri_io[0]} T20
set_property target_constrs_file /home/sdr/zynq_zynq/lab6/hardware/driver_lab.srcs/constrs_1/new/driver.xdc [
save_constraints -force
launch_runs impl_1 -to_step write_bitstream
Writing placer database...
Writing XDEF routing.
Writing XDEF routing logical nets.
Writing XDEF routing special nets.
Write XDEF Complete: Time (s): cpu = 00:00:00.12 ; elapsed = 00:00:00.03 . Memory (MB): peak = 6761.203 ; gain = 0.000000
[Wed Mar 28 21:20:11 2018] Launched impl_1...
Run output will be captured here: /home/sdr/zynq_zynq/lab6/hardware/driver_lab.runs/impl_1/runme.log
```



Timing - Timing Summary - impl_1



- (i) This is a [saved report](#)
- General Information
- Timer Settings
- Design Timing Summary**
- Clock Summary (1)
- Check Timing (2)
- Intra-Clock Paths
- Inter-Clock Paths
- Other Path Groups

Design Timing Summary

Setup	Hold	Pulse
Worst Negative Slack (WNS): 3.817 ns	Worst Hold Slack (WHS): 0.059 ns	Wc
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	To
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Nu
Total Number of Endpoints: 1208	Total Number of Endpoints: 1208	To

All user specified timing constraints are met.

이제 기본적인 것들은 모두 진행되었으므로 다음으로 Device Driver 를 만들어보도록 하자!

```
sdr@sdr-Samsung-DeskTop-System: ~/zynq_zybo/lab6
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6$ petalinux-create -t project -n
software --template zynq
INFO: Create project: software
INFO: New project successfully created in /home/sdr/zynq_zybo/lab6/software
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6$
```

프로젝트를 만들고 FPGA 로 만든 HW Description 를 구성한다.

```
sdr@sdr-Samsung-DeskTop-System: ~/zynq_zybo/lab6/hardware/driver_lab.sdk
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6$ clear
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6$ petalinux-create -t project -n softwar
e --template zynq
INFO: Create project: software
INFO: New project successfully created in /home/sdr/zynq_zybo/lab6/software
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6$ cd hardware/driver_lab.sdk/
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/hardware/driver_lab.sdk$ petalinux-conf
ig --get-hw-description -p ~/zynq_zybo/lab6/software
INFO: Checking component...
INFO: Getting hardware description...
INFO: Rename system_wrapper.hdf to system.hdf
```

```
sdr@sdr-Samsung-DeskTop-System: ~/zynq_zybo/lab6
INFO: [Hsi 55-1698] elapsed time for repository loading 0 seconds
INFO: [Common 17-206] Exiting hsi at Wed Mar 28 21:28:52 2018...
INFO: Config linux/kernel
[INFO ] oldconfig linux/kernel
INFO: Config linux/rootfs
[INFO ] oldconfig linux/rootfs
INFO: Config linux/u-boot
[INFO ] generate linux/u-boot configuration files
[INFO ] generate linux/u-boot board header files
INFO: [Hsi 55-1698] elapsed time for repository loading 0 seconds
INFO: [Common 17-206] Exiting hsi at Wed Mar 28 21:29:04 2018...
[INFO ] oldconfig linux/u-boot
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/hardware/driver_lab.sdk$ cd ../../
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6$ ls
hardware software
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6$ petalinux-create -t project -s
hardware/ software/
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6$ petalinux-create -t project -s ~/zynq_
test/ZYBO_petalinux_v2015_4.bsp
INFO: Create project:
INFO: Projects:
INFO: * ZYBO_petalinux_v2015_4
INFO: has been successfully installed to /home/sdr/zynq_zybo/lab6/
INFO: New project successfully created in /home/sdr/zynq_zybo/lab6/
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6$
```

```
sdr@sdr-Samsung-DeskTop-System: ~/zynq_zybo/lab6/ZYBO_petalinux_v2015_4
[INFO ] generate linux/u-boot board header files
INFO: [Hsi 55-1698] elapsed time for repository loading 0 seconds
INFO: [Common 17-206] Exiting hsi at Wed Mar 28 21:29:04 2018...
[INFO ] oldconfig linux/u-boot
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/hardware/driver_lab.sdk$ cd ../..
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6$ ls
hardware software
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6$ petalinux-create -t project -s
hardware/ software/
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6$ petalinux-create -t project -s ~/zynq_
test/ZYBO_petalinux_v2015_4.bsp
INFO: Create project:
INFO: Projects:
INFO: * ZYBO_petalinux_v2015_4
INFO: has been successfully installed to /home/sdr/zynq_zybo/lab6/
INFO: New project successfully created in /home/sdr/zynq_zybo/lab6/
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6$ cd ZYBO_petalinux_v2015_4/
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/ZYBO_petalinux_v2015_4$ ls
components config.project hardware hw-description pre-built subsystems
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/ZYBO_petalinux_v2015_4$ petalinux-creat
e -t apps --name gpio-dev-mem-test
INFO: Create apps: gpio-dev-mem-test
INFO: New apps successfully created in /home/sdr/zynq_zybo/lab6/ZYBO_petalinux_v2015_4/
components/apps/gpio-dev-mem-test
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/ZYBO_petalinux_v2015_4$
```

```
INFO: Create project:  
INFO: Projects:  
INFO: * ZYBO_petalinux_v2015_4  
INFO: has been successfully installed to /home/sdr/zynq_zybo/lab6/  
INFO: New project successfully created in /home/sdr/zynq_zybo/lab6/  
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6$ cd ZYBO_petalinux_v2015_4/  
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/ZYBO_petalinux_v2015_4$ ls  
components config.project hardware hw-description pre-built subsystems  
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/ZYBO_petalinux_v2015_4$ petalinux-create -t apps --name gpio-dev-mem-test  
INFO: Create apps: gpio-dev-mem-test  
INFO: New apps successfully created in /home/sdr/zynq_zybo/lab6/ZYBO_petalinux_v2015_4/  
components/apps/gpio-dev-mem-test  
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/ZYBO_petalinux_v2015_4$ cd components/  
apps/ bootloader/  
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/ZYBO_petalinux_v2015_4$ cd components/a  
pps/gpio-dev-mem-test/  
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/ZYBO_petalinux_v2015_4/components/apps/  
gpio-dev-mem-test$ ls  
gpio-dev-mem-test.c Kconfig Makefile README  
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/ZYBO_petalinux_v2015_4/components/apps/  
gpio-dev-mem-test$ cp /home/sdr/fpga/2015_4_zynq_zybo_sources/lab5/gpio-dev-mem-test/gp  
io-dev-mem-test.c ./  
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/ZYBO_petalinux_v2015_4/components/apps/  
gpio-dev-mem-test$
```

```
sdr@sdr-Samsung-DeskTop-System: ~/zynq_zybo/lab6/software
e --template zynq -s ~/zynq_
zynq_test/ zynq_zybo/
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6$ petalinux-create -t project -n software
e --template zynq -s ~/zynq_test/ZYBO_petalinux_v2015_4.bsp
INFO: Create project: software
INFO: New project successfully created in /home/sdr/zynq_zybo/lab6/software
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6$ ls
hardware software
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6$ cd software/
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/software$ ls
components config.project hardware hw-description pre-built subsystems
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/software$ cd components/
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/software/components$ ls
bootloader
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/software/components$ cd ..
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/software$ petalinux-create -t apps --na
me gpio-dev-mem-test
INFO: Create apps: gpio-dev-mem-test
INFO: New apps successfully created in /home/sdr/zynq_zybo/lab6/software/components/app
s/gpio-dev-mem-test
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/software$ cp /home/sdr/fpga/2015_4_zynq
_zybo_sources/lab5/gpio-dev-mem-test/gpio-dev-mem-test.c .
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/software$ petalinux-config -c rootfs
INFO: Checking component...
```

```
sdr@sdr-Samsung-DeskTop-System: ~/zynq_zybo/lab6/ZYBO_petalinux_v2015_4
/home/sdr/zynq_zybo/lab6/ZYBO_petalinux_v2015_4/subsystems/linux/configs/rootfs/config

----- linux/rootfs Configuration -----
Arrow keys navigate the menu. <Enter> selects submenus ---> (or empty
submenus ----). Highlighted letters are hotkeys. Pressing <Y> includes, <N>
excludes, <M> modularizes features. Press <Esc><Esc> to exit, <?> for Help,
</> for Search. Legend: [*] built-in [ ] excluded <M> module < > module

Filesystem Packages --->
Libs ----
Apps --->
Modules ----
PetaLinux RootFS Settings --->
Debugging --->

<Select>    < Exit >    < Help >    < Save >    < Load >
```

```
sdr@sdr-Samsung-DeskTop-System: ~/zynq_zybo/lab6/ZYBO_petalinux_v2015_4
/home/sdr/zynq_zybo/lab6/ZYBO_petalinux_v2015_4/subsystems/linux/configs/rootfs/config
→ Apps
```

Apps

Arrow keys navigate the menu. <Enter> selects submenus ---> (or empty submenus ----). Highlighted letters are hotkeys. Pressing <Y> includes, <N> excludes, <M> modularizes features. Press <Esc><Esc> to exit, <?> for Help, </> for Search. Legend: [*] built-in [] excluded <M> module < > module

[*] fwupgrade	----
[*] gpio-demo	----
[*] gpio-dev-mem-test	--->
[] latencystat	----
[*] peekpoke	----

<Select> < Exit > < Help > < Save > < Load >

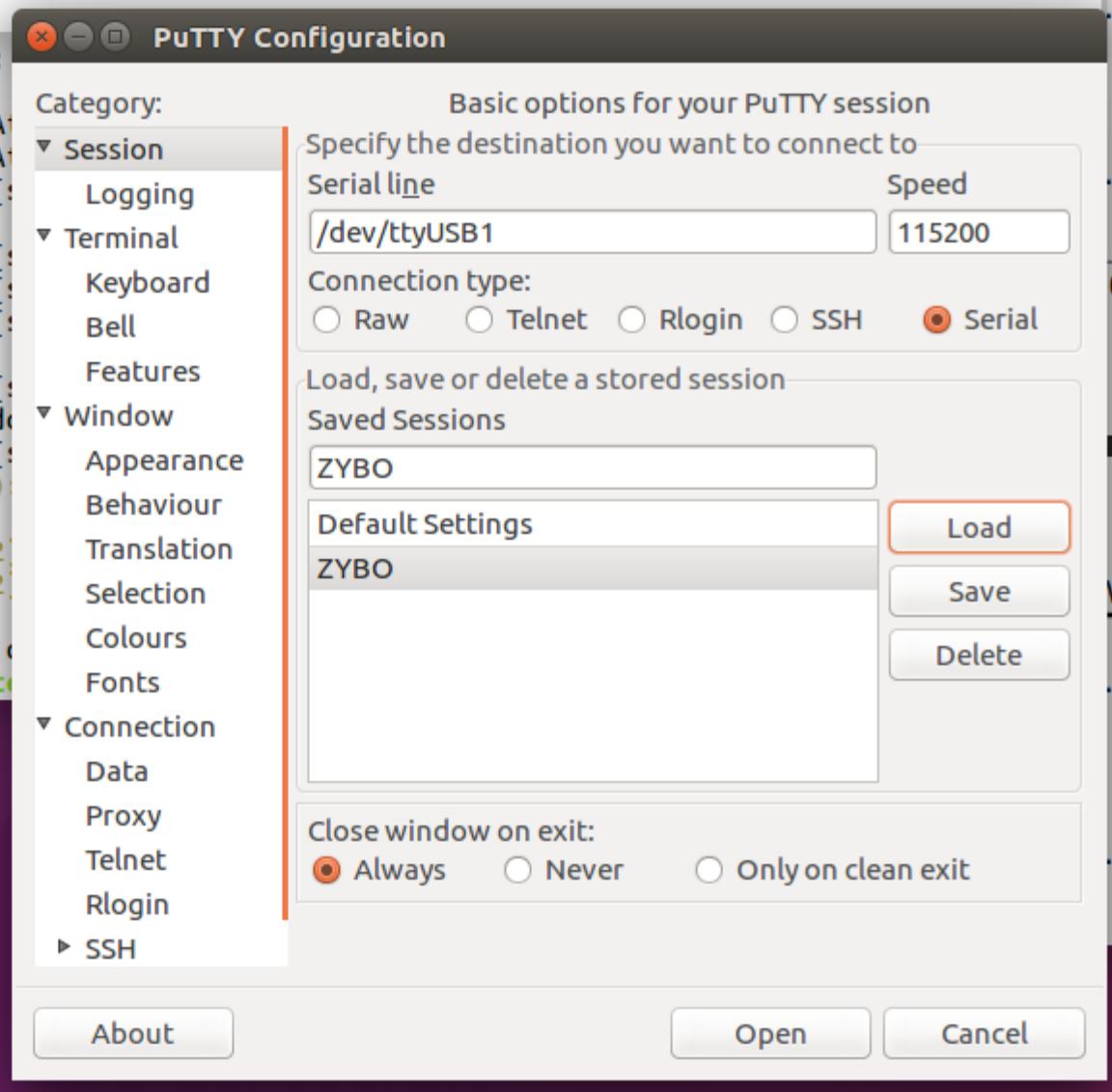
```
sdr@sdr-Samsung-DeskTop-System: ~/zynq_zybo/lab6/software
-p, --project <PROJECT>          path to Petalinux SDK project.
                                         Default is working project.
-c, --component <COMPONENT>       Specify the component
                                         all: to build the whole project
                                         If you specify other component,it will
                                         build that component
                                         E.g. -c rootfs
                                         E.g. -c rootfs/myapp
                                         If you use -c with --help option, it will
                                         show you subcomponents.
                                         E.g. -c rootfs --help shows subcomponents
                                         of rootfs.
-x, --execute <GNU_MAKE_TARGET>   Specify a GNU make command of the component
--makeenv <MAKE ENV>              Pass GNU make environment variables
-v, --verbose                      Show compile messages verbose mode
```

```
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6$ cd software/
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/software$ ls
build      config.project    hardware      pre-built
components  gpio-dev-mem-test.c hw-description subsystems
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/software$ petalinux-build
INFO: Checking component...
INFO: Generating make files and build linux
INFO: Generating make files for the subcomponents of linux
```

```
sdr@sdr-Samsung-DeskTop-System: ~/zynq_zybo/lab6/software/images/linux
[INFO ] install kernel in-tree modules
[INFO ] modules_install linux/kernel
[INFO ] post-install linux/rootfs/fwupgrade
[INFO ] post-install linux/rootfs/gpio-demo
[INFO ] post-install linux/rootfs/gpio-dev-mem-test
[INFO ] post-install linux/rootfs/peekpoke
[INFO ] package rootfs.cpio to /home/sdr/zynq_zybo/lab6/software/images/linux
[INFO ] Update and install vmlinu image
[INFO ] vmlinu linux/kernel
[INFO ] install linux/kernel
[INFO ] package zImage
[INFO ] zImage linux/kernel
[INFO ] install linux/kernel
[INFO ] Package HDF bitstream
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/software$ cd images/linux/
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/software/images/linux$ petalinux-package --boot --fsbl zynq_fsbl.elf --fpga ~zynq_zybo/lab6/hardware/driver_lab.runs/impl_1/system_wrapper.bit --u-boot
INFO: File in BOOT BIN: "/home/sdr/zynq_zybo/lab6/software/images/linux/zynq_fsbl.elf"
INFO: File in BOOT BIN: "/home/sdr/zynq_zybo/lab6/hardware/driver_lab.runs/impl_1/system_wrapper.bit"
INFO: File in BOOT BIN: "/home/sdr/zynq_zybo/lab6/software/images/linux/u-boot.elf"
INFO: Generating zynq binary package BOOT.BIN...
INFO: Binary is ready.
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/software/images/linux$
```

```
INFO: Binary is ready.
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/software/images/linux$ sudo chmod 666 /dev/ttyUSB1
[sudo] password for sdr:
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/software/images/linux$ putty
[...]
0517.999283] scsi 6:0:0:1:
0 ANSI: 4
0517.999793] sd 6:0:0:0: A
0518.000176] sd 6:0:0:1: A
0518.710788] sd 6:0:0:0: [:
ib)
0518.720870] sd 6:0:0:0: [:
0518.720874] sd 6:0:0:0: [:
0518.730793] sd 6:0:0:0: [:
't support DPO or FUA
0518.748219] sd 6:0:0:1: [:
0518.768359] sdd: sdd1 sde
0518.772607] sd 6:0:0:0: [:
0519.085992] FAT-fs (sdd1)
corrupt. Please run fsck.
0519.129530] EXT4-fs (sdd2)
0519.129534] EXT4-fs (sdd2)
ull)
0651.627226] usb 4-2: USB c
r@sdr-Samsung-DeskTop-System
```

The screenshot shows the PuTTY Configuration dialog box. The 'Session' category is selected in the left sidebar. The main pane displays basic options for the session, including the serial line set to '/dev/ttyUSB1' and a speed of 115200. The 'Connection type' section shows that 'Serial' is selected. Below this, there are sections for saved sessions ('Saved Sessions' containing 'ZYBO') and default settings ('Default Settings' also containing 'ZYBO'). Buttons for 'Load', 'Save', and 'Delete' are visible on the right.



/dev/ttyUSB1 - PuTTY

```
Built with PetaLinux v2015.4 (Yocto 1.8) ZYBO_petalinux_v2015_4 /dev/ttys0
ZYBO_petalinux_v2015_4 login: root
Password:
login[875]: root login on 'ttys0'
root@ZYBO_petalinux_v2015_4:~# ls
root@ZYBO_petalinux_v2015_4:~# gpio-dev-mem-test
Hello, PetaLinux World!
cmdline args:
gpio-dev-mem-test
root@ZYBO_petalinux_v2015_4:~# gpio-demo
Usage: gpio-demo [-g GPIO_BASE] COMMAND
    where COMMAND is one of:
        -i          Input value from GPIO and print it
        -o      VALUE  Output value to GPIO
        -c          Cylon test pattern
        -k          KIT test pattern
GPIO_BASE indicates which GPIO chip to talk to (The number can be
found at /sys/class/gpio/gpiochipN).
The highest gpiochipN is the first gpio listed in the dts file,
and the lowest gpiochipN is the last gpio listed in the dts file,
E.g. If the gpiochip240 is the LED_8bit gpio, and I want to output '1'
to the LED_8bit gpio, the command should be:
    gpio-demo -g 240 -o 1

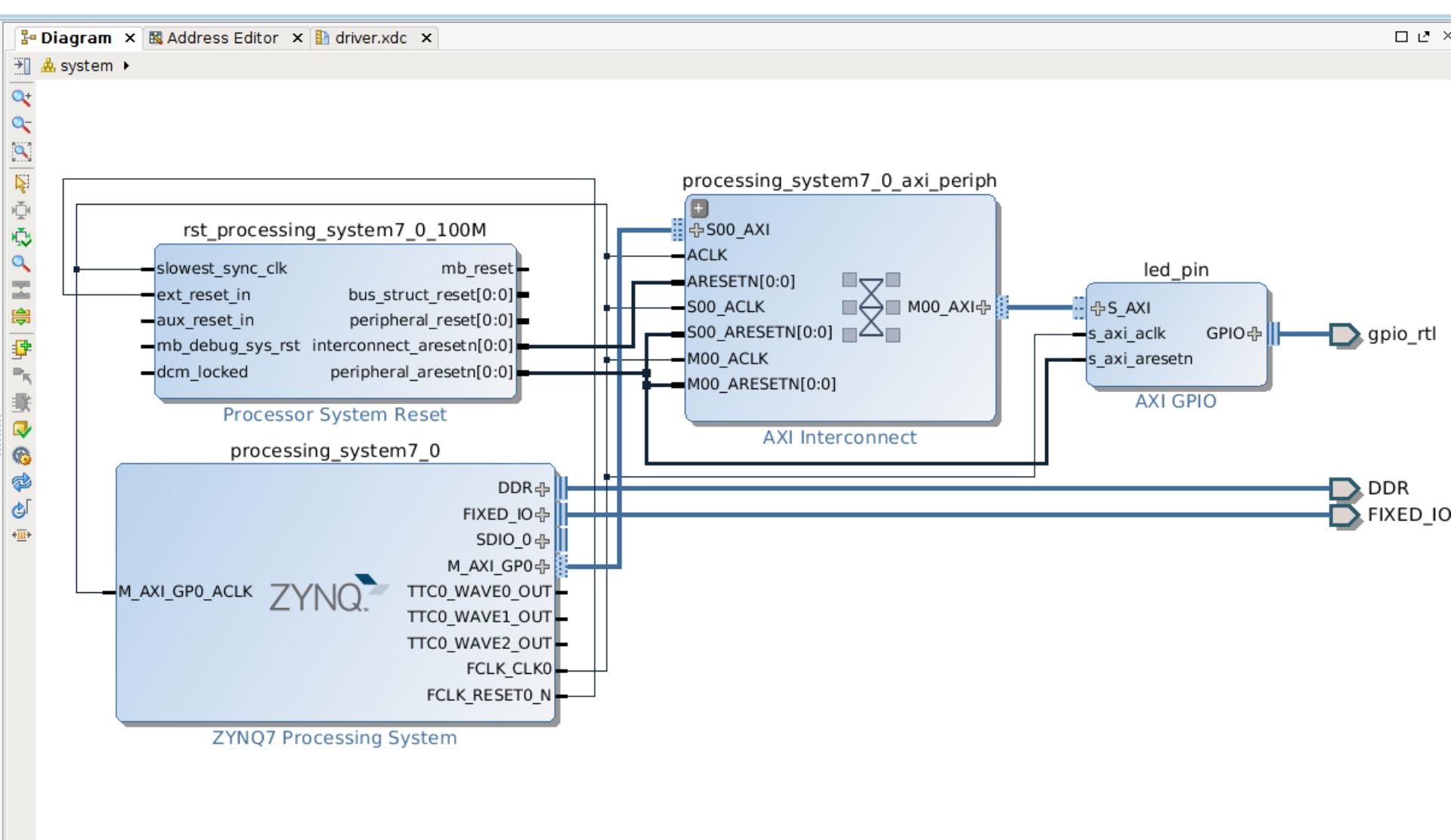
gpio-demo written by Xilinx Inc.

root@ZYBO_petalinux_v2015_4:~#
```

/dev/ttyUSB1 - PuTTY

```
radio_bus e000b000.etherne: scan phy mdio at address 26
radio_bus e000b000.etherne: scan phy mdio at address 27
radio_bus e000b000.etherne: scan phy mdio at address 28
radio_bus e000b000.etherne: scan phy mdio at address 29
radio_bus e000b000.etherne: scan phy mdio at address 30
radio_bus e000b000.etherne: scan phy mdio at address 31
macb e000b000.ethernet eth0: Cadence GEM rev 0x00020118 at 0xe000b000 irq 145 (00:0a:35:00:1e:53)
macb e000b000.ethernet eth0: attached PHY driver [Generic PHY] (mii_bus:phy_addr=e000b000.etherne:00, irq=-1)
e1000e: Intel(R) PRO/1000 Network Driver - 2.3.2-k
e1000e: Copyright(c) 1999 - 2014 Intel Corporation.
ehci_hcd: USB 2.0 'Enhanced' Host Controller (EHCI) Driver
ehci-pci: EHCI PCI platform driver
usbcore: registered new interface driver usb-storage
mousedev: PS/2 mouse device common for all mice
I2c /dev entries driver
Xilinx Zynq CpuIdle Driver started
Driver 'mmcblk' needs updating - please use bus_type methods
sdhci: Secure Digital Host Controller Interface driver
sdhci: Copyright(c) Pierre Ossman
sdhci-pltfm: SDHCI platform and OF driver helper
sdhci-arasan e0100000.sdhci: No vmmc regulator found
sdhci-arasan e0100000.sdhci: No vgmmc regulator found
mmc0: SDHCI controller on e0100000.sdhci [e0100000.sdhci] using ADMA
ledtrig-cpu: registered to indicate activity on CPUs
usbcore: registered new interface driver usbhid
usbhid: USB HID core driver
TCP: cubic registered
NET: Registered protocol family 17
can: controller area network core (rev 20120528 abi 9)
NET: Registered protocol family 29
can: raw protocol (rev 20120528)
can: broadcast manager protocol (rev 20120528 t)
can: netlink gateway (rev 20130117) max_hops=1
Registering SWP/SWPB emulation handler
/home/sdr/petalinux_zynq/petalinux-v2015.4-final/components/linux-kernel/xlnx-4.0/drivers/rtc/hctosys.c: unable to open rtc device (rtc0)
mmc0: new high speed SDHC card at address e624
ALSA device list:
  No soundcards found.
mmcblk0: mmc0:e624 SU08G 7.40 GiB
freeing unused kernel memory: 3956K (c0659000 - c0a36000)
mmcblk0: p1 p2
FAT-fs (mmcblk0p1): Volume was not properly unmounted. Some data may be corrupt. Please run fsck.
EXT4-fs (mmcblk0p2): mounted filesystem with ordered data mode. Opts: (null)
random: dd urandom read with 1 bits of entropy available
NET: Registered protocol family 10
IPv6: ADDRCONF(NETDEV_UP): eth0: link is not ready
random: nonblocking pool is initialized
root@ZYBO_petalinux_v2015_4:/# dmesg | grep gpio
Gpio: /amba_pl/gpio@41200000: registered, base is 905
root@ZYBO_petalinux_v2015_4:/# █
```

```
root@ZYBO_petalinux_v2015_4:~# dmesg | grep gpio
[XGpio: /amba_pl/gpio@41200000: registered, base is 905
root@ZYBO_petalinux_v2015_4:~# gpio-dev-mem-test -g 0x41200000 -o 1
GPIO access through /dev/mem.
root@ZYBO_petalinux_v2015_4:~# gpio-demo -g 905 -o 1
root@ZYBO_petalinux_v2015_4:~# gpio-demo -g 905 -o 0
root@ZYBO_petalinux_v2015_4:~#
```



```
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/sw$ ls
build components config.project hw-description images subsystems
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/sw$ petalinux-create -t apps --name gpio-
vio-test
INFO: Create apps: gpio-vio-test
INFO: New apps successfully created in /home/sdr/zynq_zybo/lab6/sw/components/apps/gpio-u
io-test
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/sw$ cd components/apps/gpio-vio-test/
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/sw/components/apps/gpio-vio-test$ cp ~/fp
ga/2015_4_zynq_zybo_sources/lab5/gpio-vio-test/gpio-vio-test.c .
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/sw/components/apps/gpio-vio-test$ ls
gpio-vio-test.c Kconfig Makefile README
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/sw/components/apps/gpio-vio-test$ cd ../..
./..
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/sw$ ls
build components config.project hw-description images subsystems
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/sw$ petalinux-config -c rootfs
INFO: Checking component...
INFO: Config linux/rootfs
[INFO ] config linux/rootfs
configuration written to /home/sdr/zynq_zybo/lab6/sw/subsystems/linux/configs/rootfs/conf
ig

*** End of the configuration.
*** Execute 'make' to start the build or try 'make help'.
```

```
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/sw$ petalinux-config -c rootfs
INFO: Checking component...
INFO: Config linux/rootfs
[INFO ] config linux/rootfs
configuration written to /home/sdr/zynq_zybo/lab6/sw/subsystems/linux/configs/rootfs/config

*** End of the configuration.
*** Execute 'make' to start the build or try 'make help'.

sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/sw$ petalinux-config -c kernel
INFO: Checking component...
INFO: Config linux/kernel
[INFO ] config linux/kernel
configuration written to /home/sdr/zynq_zybo/lab6/sw/subsystems/linux/configs/kernel/config

*** End of the configuration.
*** Execute 'make' to start the build or try 'make help'.

sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/sw$ vi subsystems/linux/config
config      config.old  configs/
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/sw$ vi subsystems/linux/configs/device-tree/pl.dtsi
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/sw$ vi subsystems/linux/configs/device-tree/system-top.dts
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/sw$ cd ../hardware/
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/hardware$ ls
driver_lab.cache  driver_lab.ip_user_files  driver_lab.sdk  driver_lab.srcs
driver_lab.hw     driver_lab.runs          driver_lab.sim  driver_lab.xpr
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/hardware$ cd driver_lab.sdk/
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/hardware/driver_lab.sdk$ petalinux-config
--get-hw-description -p ~/zynq_zybo/lab6/sw
```

```
sd@sd-Samsung-DeskTop-System:~/zynq_zybo/lab6/sw$ vi subsystems/linux/configs/device-tree/system-top.dts
sd@sd-Samsung-DeskTop-System:~/zynq_zybo/lab6/sw$ cd ../hardware/
sd@sd-Samsung-DeskTop-System:~/zynq_zybo/lab6/hardware$ ls
driver_lab.cache  driver_lab.ip_user_files  driver_lab.sdk  driver_lab.srcs
driver_lab.hw      driver_lab.runs          driver_lab.sim  driver_lab.xpr
sd@sd-Samsung-DeskTop-System:~/zynq_zybo/lab6/hardware$ cd driver_lab.sdk/
sd@sd-Samsung-DeskTop-System:~/zynq_zybo/lab6/hardware/driver_lab.sdk$ petalinux-config
--get-hw-description -p ~/zynq_zybo/lab6/sw
INFO: Checking component...
INFO: Getting hardware description...
cp: omitting directory '/home/sdr/zynq_zybo/lab6/hardware/driver_lab.sdk/led_test'
cp: omitting directory '/home/sdr/zynq_zybo/lab6/hardware/driver_lab.sdk/led_test_bsp'
cp: omitting directory '/home/sdr/zynq_zybo/lab6/hardware/driver_lab.sdk/RemoteSystemsTem
pFiles'
cp: omitting directory '/home/sdr/zynq_zybo/lab6/hardware/driver_lab.sdk/system_wrapper_h
w_platform_0'
cp: omitting directory '/home/sdr/zynq_zybo/lab6/hardware/driver_lab.sdk/webtalk'
INFO: Rename system_wrapper.hdf to system.hdf

***** hsi v2015.4 (64-bit)
**** SW Build 1412921 on Wed Nov 18 09:44:32 MST 2015
** Copyright 1986-2015 Xilinx, Inc. All Rights Reserved.

source /home/sdr/zynq_zybo/lab6/sw/build/linux/hw-description/hw-description.tcl -notrace
INFO: [Common 17-206] Exiting hsi at Fri Mar 30 00:17:52 2018...
INFO: Config linux
[INFO ] oldconfig linux
[INFO ] generate DTS to /home/sdr/zynq_zybo/lab6/sw/subsystems/linux/configs/device-tree
INFO: [Hsi 55-1698] elapsed time for repository loading 0 seconds
WARNING: ps7_ethernet_0: No reset found
INFO: [Common 17-206] Exiting hsi at Fri Mar 30 00:18:00 2018...
[INFO ] generate BSP for zynq_fsbl
INFO: [Hsi 55-1698] elapsed time for repository loading 0 seconds
INFO: [Common 17-206] Exiting hsi at Fri Mar 30 00:18:09 2018...
INFO: Config linux/kernel
[INFO ] oldconfig linux/kernel
```

```
[root@sd... /]# cd /zynq_zybo/lab6/sw
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/sw$ vi subsystems/linux/configs/device-tree/system-top.dts
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/sw$ cd ../
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6$ cd software/
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/software$ vi subsystems/linux/configs/device-tree/system-top.dts
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/software$ cd ../sw
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/sw$ petalinux-config
INFO: Checking component...
INFO: Config linux
[INFO ] config linux

*** End of the configuration.
*** Execute 'make' to start the build or try 'make help'.
```

```
[INFO ] olaconfig linux/u-boot
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/sw$ petalinux-config -c kernel
INFO: Checking component...
INFO: Config linux/kernel
[INFO ] config linux/kernel

*** End of the configuration.
*** Execute 'make' to start the build or try 'make help'.

sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/sw$ petalinux-config -c rootfs
INFO: Checking component...
INFO: Config linux/rootfs
[INFO ] config linux/rootfs

*** End of the configuration.
*** Execute 'make' to start the build or try 'make help'.

sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/sw$ vi subsystems/linux/configs/device-tree/system-top.dts
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/sw$ cd subsystems/linux/configs/device-tree
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/sw/subsystems/linux/configs/device-tree$ cp ~/fpga/2015_4_zynq_zybo_sources/lab6/
output.bif platform-top.h system-top.dts
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/sw/subsystems/linux/configs/device-tree$
```

```
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/sw/images$
```

```
*** End of the configuration.  
*** Execute 'make' to start the build or try 'make help'.  
  
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/sw$ petalinux-config -c rootfs  
INFO: Checking component...  
INFO: Config linux/rootfs  
[INFO ] config linux/rootfs  
  
*** End of the configuration.  
*** Execute 'make' to start the build or try 'make help'.  
  
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/sw$ vi subsystems/linux/configs/device-tree/system-top.dts  
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/sw$ cd subsystems/linux/configs/device-tree  
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/sw/subsystems/linux/configs/device-tree$ cp ~/fpga/2015_4_zynq_zybo_sources/lab6/  
output.bif platform-top.h system-top.dts  
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/sw/subsystems/linux/configs/device-tree$ cp ~/fpga/2015_4_zynq_zybo_sources/lab6/system-top.dts ./  
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/sw/subsystems/linux/configs/device-tree$ vi system-top.dts  
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/sw/subsystems/linux/configs/device-tree$ vi pl.dtsi  
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/sw/subsystems/linux/configs/device-tree$ vi system-top.dts  
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/sw/subsystems/linux/configs/device-tree$ cd ../../..  
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/sw/subsystems$ cd ..  
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/sw$ petalinux-build  
INFO: Checking component...  
INFO: Generating make files and build linux  
INFO: Generating make files for the subcomponents of linux  
INFO: Building linux  
INFO: Cleaning packages
```

sdr@sdr-Samsung-DeskTop-System: ~

```
1 /dts-v1/;
2 /include/ "system-conf.dtsi"
3 /
4 };
5
6 &clkc {
7     ps-clk-frequency = <500000000>;
8 };
9
10 &flash0 {
11     compatible = "s25fl128s1";
12 };
13
14 &usb0 {
15     dr_mode = "otg";
16 } ;
17
18 &gem0 {
19     phy-handle = <&phy0>;
20     mdio {
21         #address-cells = <1>;
22         #size-cells = <0>;
23         phy0: phy@1 {
24             compatible = "realtek,RTL8211E";
25             device_type = "ethernet-phy";
26             reg = <1>;
27         } ;
28     } ;
29 } ;
30
31
32 &led_pin {
33     compatible = "generic-uio";
34 };
```

'zynq_zybo/lab6/sw/subsystems/linux/configs/device-tree/system-top.dts' 34L, 409C

```
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/sw/images/linux
vi system-top.dts
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/sw/subsystems/linux/configs/device-tree$ vi pl.dtsi
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/sw/subsystems/linux/configs/device-tree$ vi system-top.dts
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/sw/subsystems/linux/configs/device-tree$ cd ../../..
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/sw/subsystems$ cd ../..
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/sw$ petalinux-build
INFO: Checking component...
INFO: Generating make files and build linux
INFO: Generating make files for the subcomponents of linux
INFO: Building linux
[INFO ] Cleaning packages
[INFO ] clean linux/rootfs/fwupgrade
[INFO ] clean linux/rootfs/gpio-dev-mem-test
[INFO ] clean linux/rootfs/gpio-uvio-test
[INFO ] clean linux/rootfs/peekpoke
[INFO ] pre-build linux/rootfs/fwupgrade
[INFO ] pre-build linux/rootfs/gpio-dev-mem-test
[INFO ] pre-build linux/rootfs/gpio-uvio-test
[INFO ] pre-build linux/rootfs/peekpoke
[INFO ] build system.dtb
[ERROR] Error: /home/sdr/zynq_zybo/lab6/sw/subsystems/linux/configs/device-tree/system-top.dts:34.2-35.1 syntax error
[ERROR] make[1]: *** [system.dtb] Error 255
ERROR: Failed to build linux
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/sw$ vi subsystems/linux/configs/device-tree/system-top.dts
sdr@sdr-Samsung-DeskTop-System:~/zynq_zybo/lab6/sw$ petalinux-build
INFO: Checking component...
INFO: Generating make files and build linux
INFO: Generating make files for the subcomponents of linux
INFO: Building linux
[INFO ] pre-build linux/rootfs/fwupgrade
[INFO ] pre-build linux/rootfs/gpio-dev-mem-test
[INFO ] pre-build linux/rootfs/gpio-uvio-test
[INFO ] pre-build linux/rootfs/peekpoke
```

```
--file-attribute <DATA File ATTR> Zynq/ZynqMP only. data file file-attribute
--bif-attribute <ATTRIBUTE> Zynq/ZynqMP only. name of BIF attribute
--bif-attribute-value <VALUE> Zynq/ZynqMP only. value of the attribute specified b
y
--fsblconfig <BIF FSBL CONFIG> --attribute argument
--bif <BIF> Zynq/ZynqMP only. BIF fsbl config value
Zynq/ZynqMP only. BIF file. It overrides all
other settings:
--fsbl, --fpga, --u-boot, --add, --fsblconfig,
--file-attribute, --bif-attribute and
--bif-attribute-value.
--boot-device <BOOT_DEV> valid for BIN for Zynq and ZynqMP only.
sd | flash
default will be the one selected from system select
menu
of boot image settings
```

EXAMPLES:

Package BOOT.BIN for Zynq:

```
$ petalinux-package --boot --fsbl <FSBL_ELF> --fpga <BITSTREAM> --u-boot
It will generate a BOOT.BIN in your working directory with:
* specified <BITSTREAM>
* specified <FSBL_ELF>
* newly built u-boot image which is <PROJECT>/images/linux/u-boot.elf
```

ERROR: Output file "/home/sdr/zynq_zynq/zybo/lab6/sw/images/linux/BOOT.BIN" already exists. Please use --force to overwrite it.

```
sdr@sdr-Samsung-DeskTop-System:~/zynq_zynq/zybo/lab6/sw/images/linux$ petalinux-package --boot
--fsbl zynq_fsbl.elf --fpga ~/zynq_zynq/zybo/lab6/hardware/driver_lab.runs/impl_1/system_wrapper.bit --u-boot --force
INFO: File in BOOT BIN: "/home/sdr/zynq_zynq/zybo/lab6/sw/images/linux/zynq_fsbl.elf"
INFO: File in BOOT BIN: "/home/sdr/zynq_zynq/zybo/lab6/hardware/driver_lab.runs/impl_1/system_wrapper.bit"
INFO: File in BOOT BIN: "/home/sdr/zynq_zynq/zybo/lab6/sw/images/linux/u-boot.elf"
INFO: Generating zynq binary package BOOT.BIN...
INFO: Binary is ready.
```

```
sdr@sdr-Samsung-DeskTop-System:~/zynq_zynq/zybo/lab6/sw/images/linux$
```

```
sdr@sdr-Samsung-DeskTop-System:~$ ls
clion          fpga      my_proj       test           vivado_2287.backup.jou  vivado.jou
CLionProjects   ip_repo   petalinux_zynq  Videos        vivado_2287.backup.log  vivado.log
Desktop         lab       Pictures       vivado_10445.backup.jou  vivado_2607.backup.jou  zynq_test
Documents        lab_fpga Public        vivado_10445.backup.log  vivado_2607.backup.log  zynq_zybo
Downloads        lecture  self_drive    vivado_10574.backup.jou  vivado_4313.backup.jou
examples.desktop Music    Templates     vivado_10574.backup.log  vivado_4313.backup.log
sdr@sdr-Samsung-DeskTop-System:~$ putty
sdr@sdr-Samsung-DeskTop-System:~$ sudo chmod 666 /dev/ttyUSB1
[sudo] password for sdr:
sdr@sdr-Samsung-DeskTop-System:~$ putty
sdr@sdr-Samsung-DeskTop-System:~$ sudo chmod 666 /dev/ttyUSB1
sdr@sdr-Samsung-DeskTop-System:~$ putty
sdr@sdr-Samsung-DeskTop-System:~$ sudo chmod 666 /dev/ttyUSB1
[sudo] password for sdr:
sdr@sdr-Samsung-DeskTop-System:~$ putty
sdr@sdr-Samsung-DeskTop-System:~$ sudo chmod 666 /dev/ttyUSB1
[sudo] password for sdr:
sdr@sdr-Samsung-DeskTop-System:~$ putty
sdr@sdr-Samsung-DeskTop-System:~$ sudo chmod 666 /dev/ttyUSB1
[sudo] password for sdr:
sdr@sdr-Samsung-DeskTop-System:~$ putty
sdr@sdr-Samsung-DeskTop-System:~$ sudo chmod 666 /dev/ttyUSB1
[sudo] password for sdr:
sdr@sdr-Samsung-DeskTop-System:~$ putty
sdr@sdr-Samsung-DeskTop-System:~$
```

```
#include <stdio.h>
#include <stdlib.h>
#include <unistd.h>
#include <sys/mman.h>
#include <fcntl.h>

#define IN 0
#define OUT 1

#define GPIO_MAP_SIZE 0x10000

#define GPIO_DATA_OFFSET 0x00
#define GPIO_TRI_OFFSET 0x04
#define GPIO2_DATA_OFFSET 0x00
#define GPIO2_TRI_OFFSET 0x04

void usage(void)
{
    printf("*argv[0] -d <UIO_DEV_FILE> -i|-o <VALUE>\n");
    printf("    -d           UIO device file. e.g. /dev/uio0");
    printf("    -i           Input from GPIO");
    printf("    -o <VALUE>   Output to GPIO");
    return;
}
```

```
int main(int argc, char *argv[])
{
    int c;
    int fd;
    int direction=IN;
    char *uiod;
    int value = 0;

    void *ptr;

    printf("GPIO UIO test.\n");
    while((c = getopt(argc, argv, "d:io:h")) != -1)
    {
        switch(c)
        {
            case 'd':
                uiod=optarg;
                break;
            case 'i':
                direction=IN;
                break;
            case 'o':
                direction=OUT;
                value=atoi(optarg);
                break;
            case 'h':
                usage();
                return 0;
            default:
                printf("invalid option: %c\n", (char)c);
                usage();
                return -1;
        }
    }
}
```

```
fd = open(uiod, O_RDWR);

if (fd < 1)
{
    perror(argv[0]);
    printf("Invalid UIO device file:%s.\n", uiod);
    usage();
    return -1;
}

ptr = mmap(NULL, GPIO_MAP_SIZE, PROT_READ|PROT_WRITE, MAP_SHARED, fd, 0);

if (direction == IN)
{
    *((unsigned *) (ptr + GPIO_TRI_OFFSET)) = 255;
    value = *((unsigned *) (ptr + GPIO_DATA_OFFSET));
    printf("%s: input: %08x\n", argv[0], value);
}
else
{
    *((unsigned *) (ptr + GPIO_TRI_OFFSET)) = 0;

    *((unsigned *) (ptr + GPIO_DATA_OFFSET)) = value;
}

munmap(ptr, GPIO_MAP_SIZE);

return 0;
}
```

