Pmod External LED Control with Vivado SDK

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우선 Vivado 에 이어서 SDK 도 언제든 편하게 킬 수 있도록 좌측에 탭을 만들도록 하자!

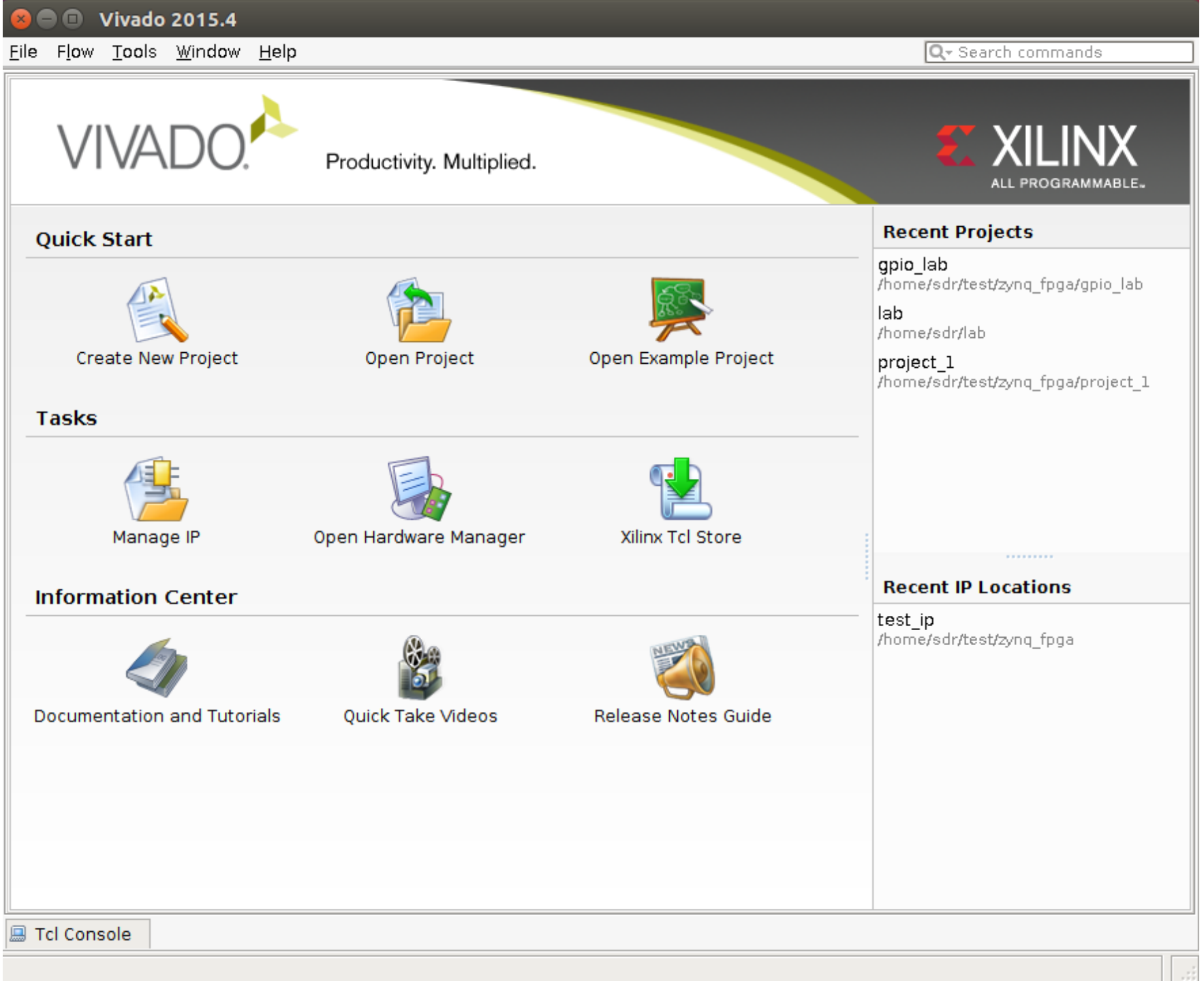
```
sdr@sdr-Samsung-DeskTop-System: ~/Desktop
sdr@sdr-Samsung-DeskTop-System:~$ cd Desktop/
sdr@sdr-Samsung-DeskTop-System:~/Desktop$ ls
vivado.desktop
sdr@sdr-Samsung-DeskTop-System:~/Desktop$ vi sdk.desktop
```

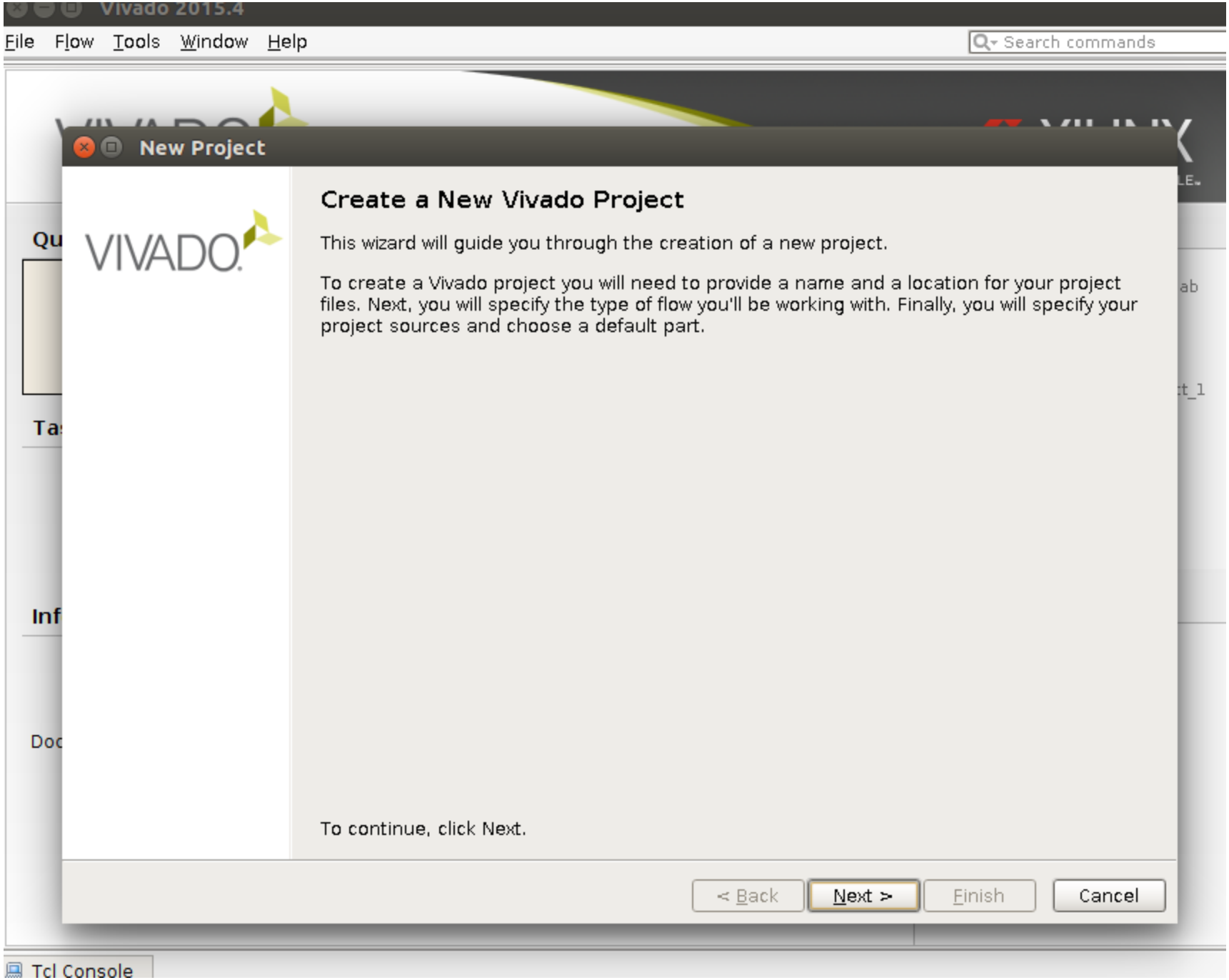
그리고 여기에 아래와 같이 내용을 적는다.

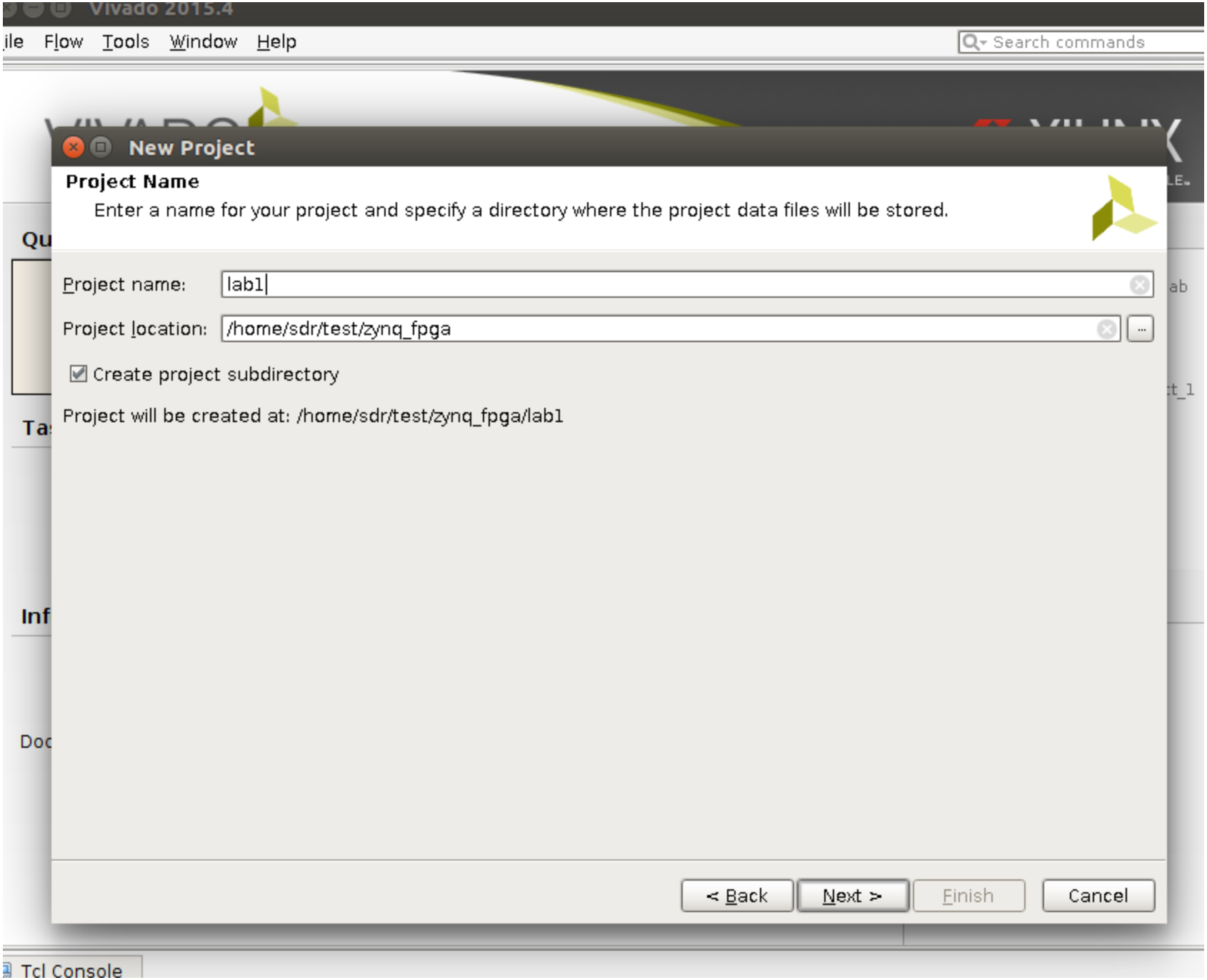
```
sdr@sdr-Samsung-DeskTop-System: ~/Desktop
#!/usr/bin/env xdg-open
[Desktop Entry]
Name=Xilinx SDK
Type=Application
Exec=/opt/Xilinx/SDK/2015.4/bin/xsdk
Terminal=false
Icon=/opt/Xilinx/SDK/2015.4/data/sdk/images/sdk_logo.ico
Comment=Xilinx SDK Program
NoDisplay=false
Categories=Development;IDE;
Name[en]=SDK
```

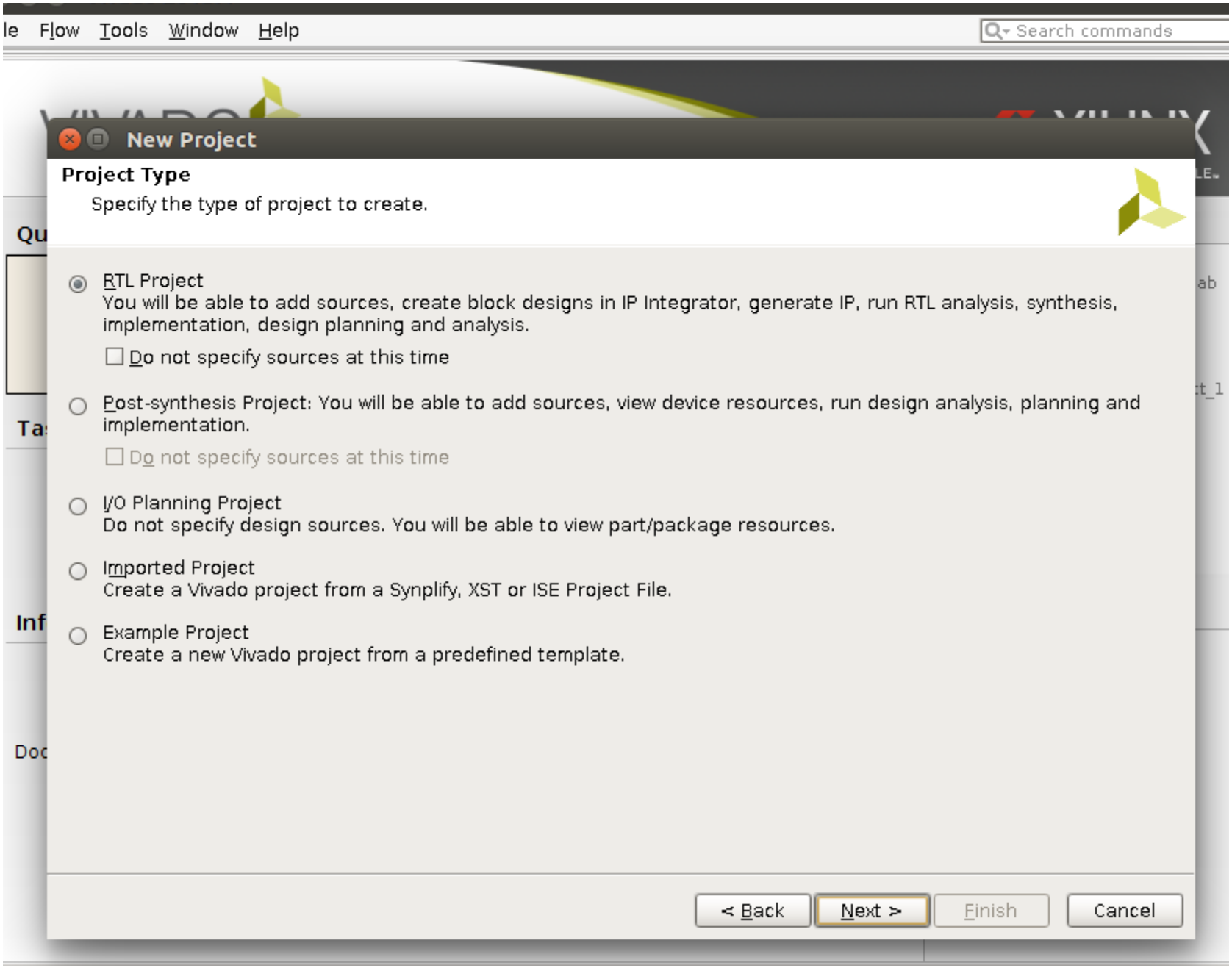
속성에 들어가서 Execute 부분에 체크하면 아래와 같이 활성화가 된다.

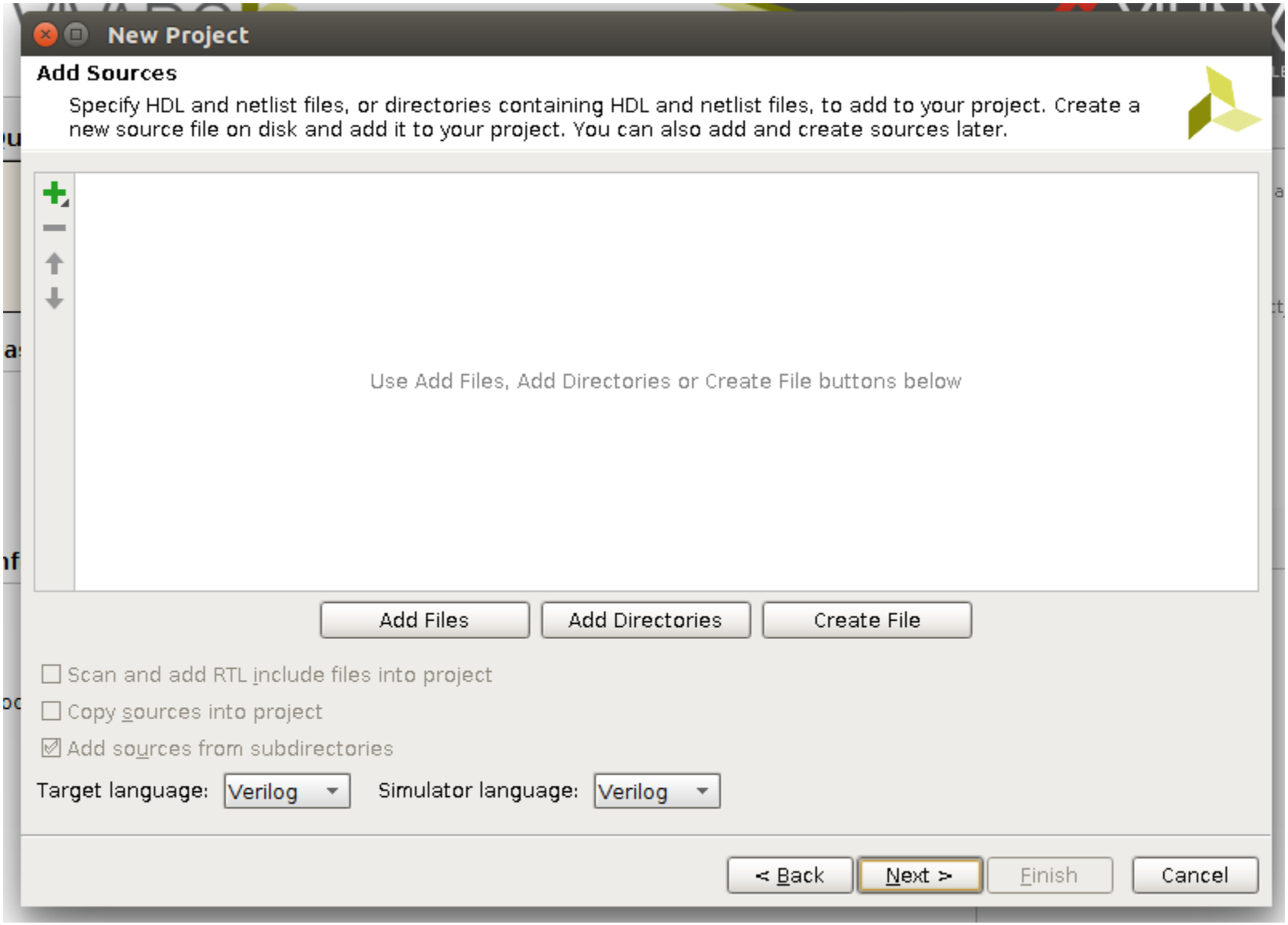
그리고 활성화된 아이콘을 좌측 탭에 밀어넣으면 아래 그림과 같이 들어가는 것을 볼 수 있다.

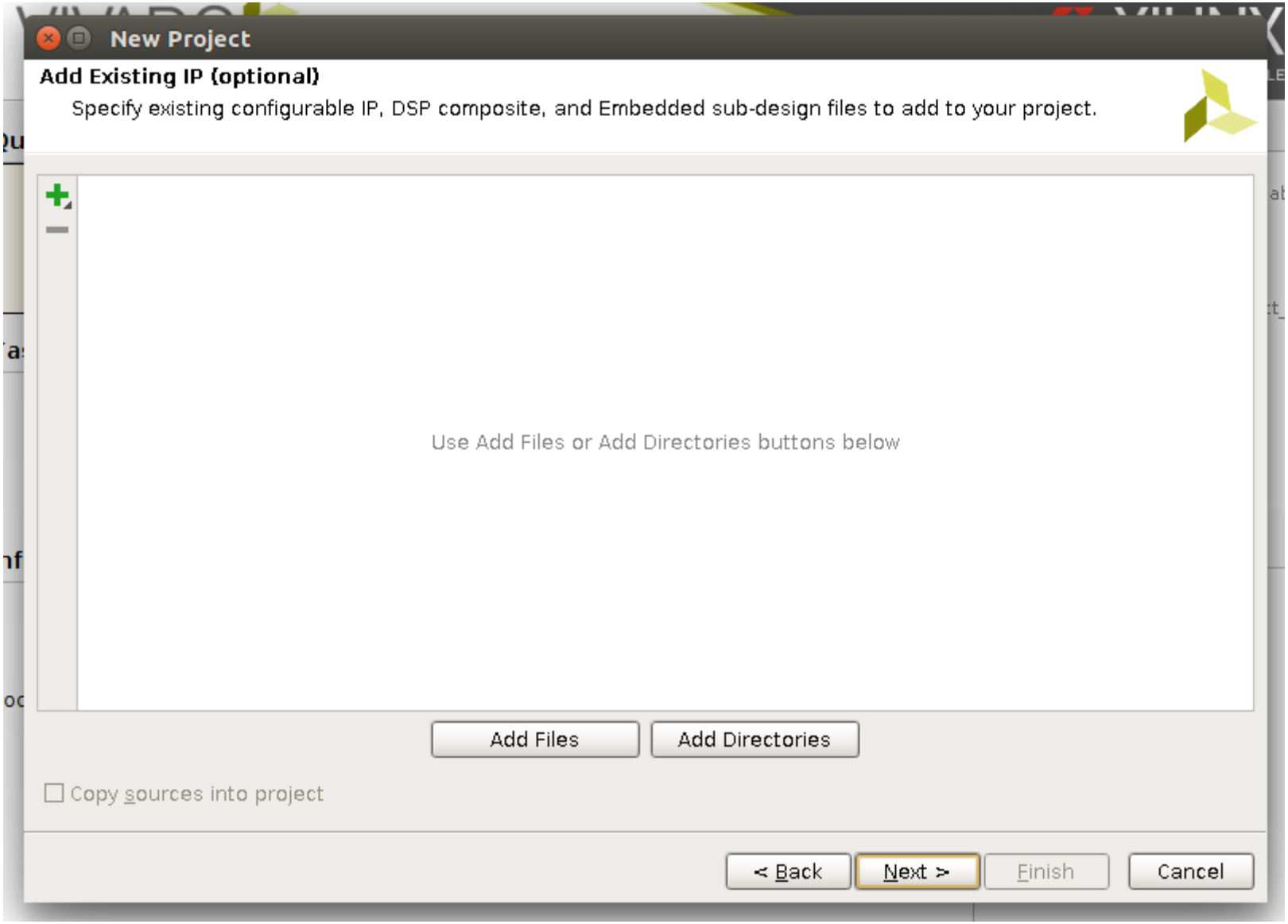

Vivado 2015.4
File Flow Tools Window Help
Search commands
VIVADO
Productivity. Multiplied.
XILINX
ALL PROGRAMMABLE.
Quick Start
Create New Project
Open Project
Open Example Project
Tasks
Manage IP
Open Hardware Manager
Xilinx Tcl Store
Information Center
Documentation and Tutorials
Quick Take Videos
Release Notes Guide
Recent Projects
gpio_lab
/home/sdr/test/zynq_fpga/gpio_lab
lab
/home/sdr/lab
project_1
/home/sdr/test/zynq_fpga/project_1
Recent IP Locations
test_ip
/home/sdr/test/zynq_fpga
Tcl Console

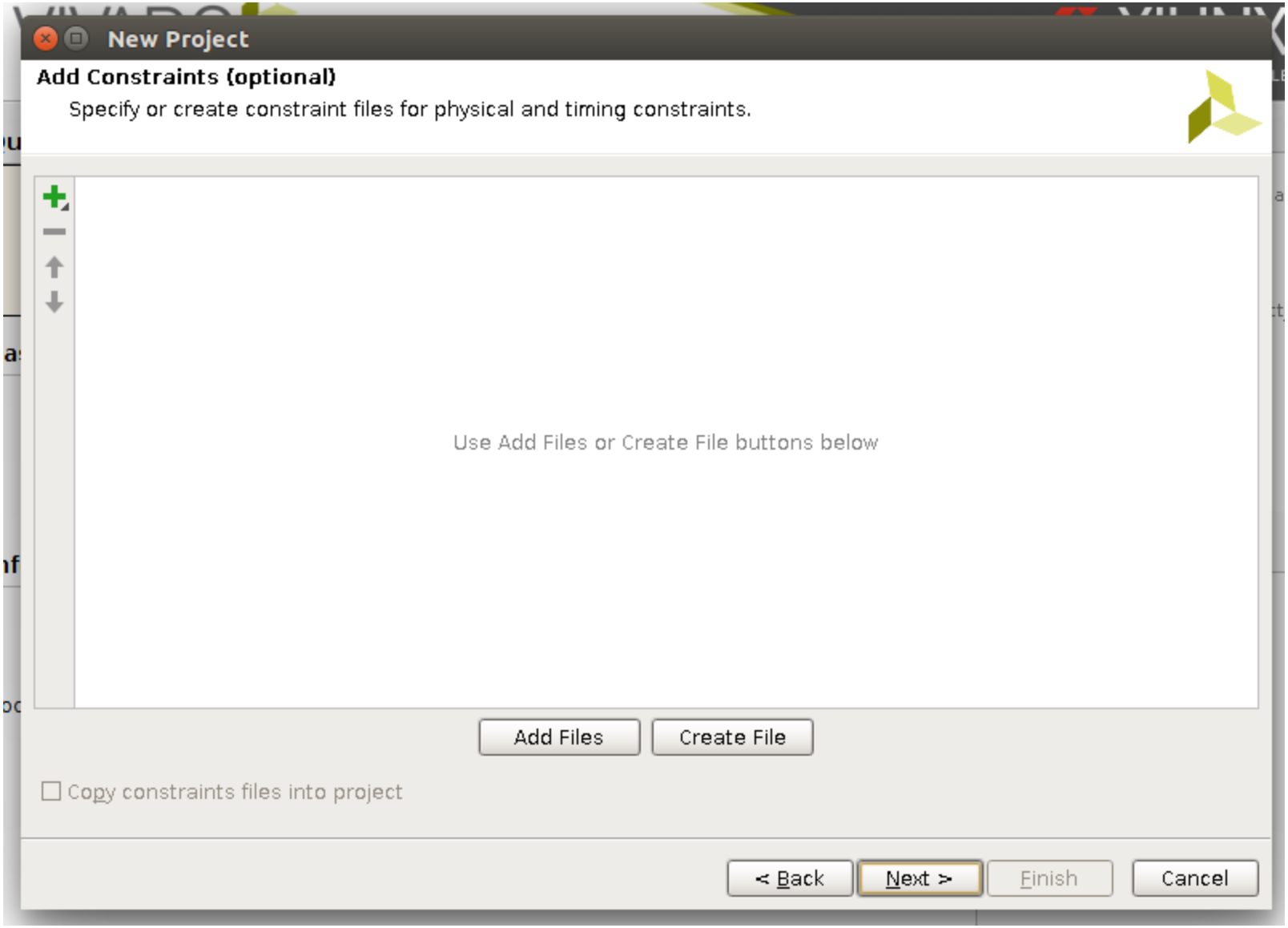

Vivado 2015.4
File Flow Tools Window Help
Search commands
New Project
VIVADO
Create a New Vivado Project
This wizard will guide you through the creation of a new project.
To create a Vivado project you will need to provide a name and a location for your project files. Next, you will specify the type of flow you'll be working with. Finally, you will specify your project sources and choose a default part.
To continue, click Next.
< Back
Next >
Finish
Cancel
Tcl Console

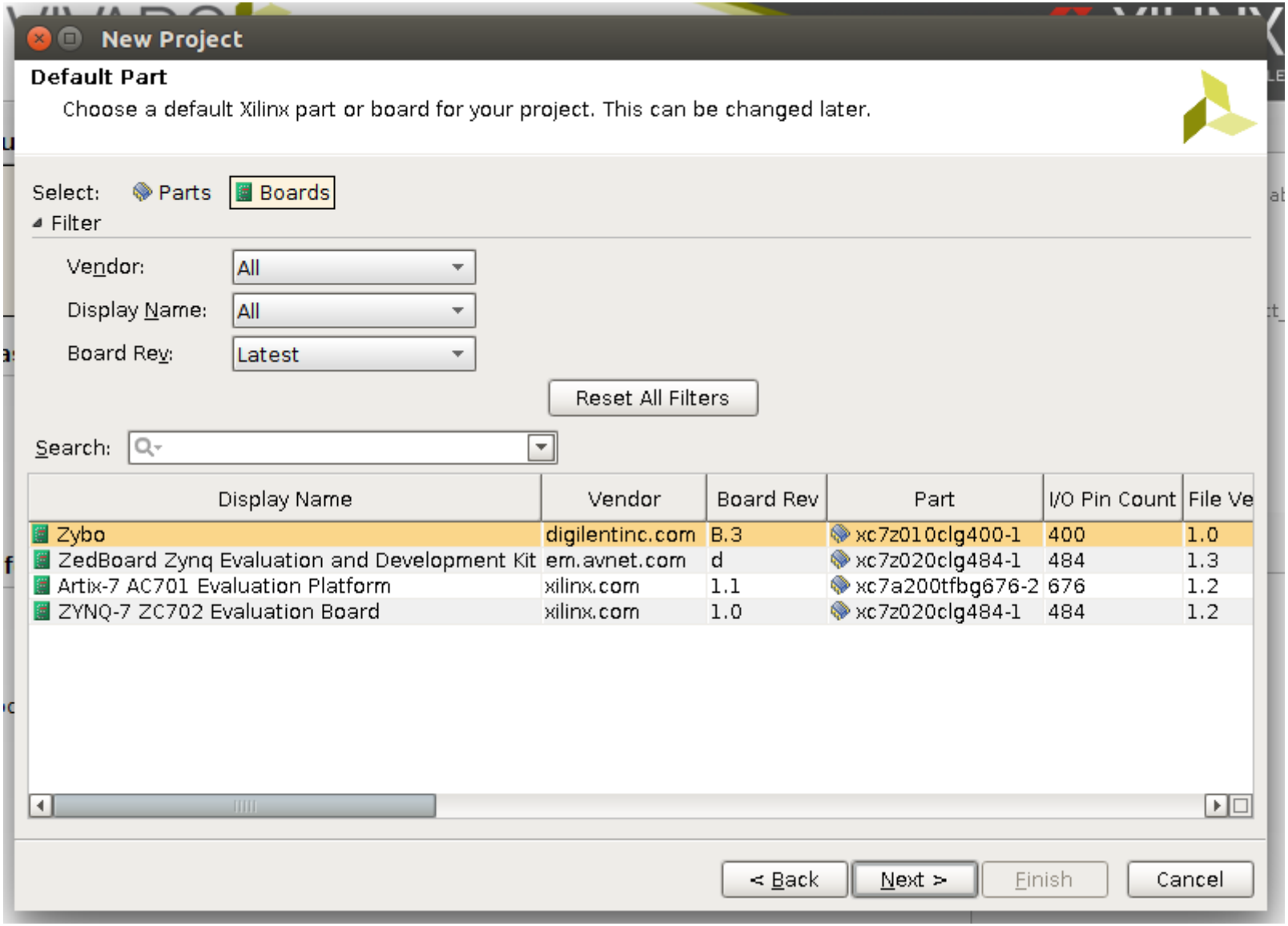

Vivado 2015.4
File Flow Tools Window Help
Search commands
New Project
Project Name
Enter a name for your project and specify a directory where the project data files will be stored.
Project name: lab1
Project location: /home/sdr/test/zynq_fpga
Create project subdirectory
Project will be created at: /home/sdr/test/zynq_fpga/lab1
< Back
Next >
Finish
Cancel
Tcl Console

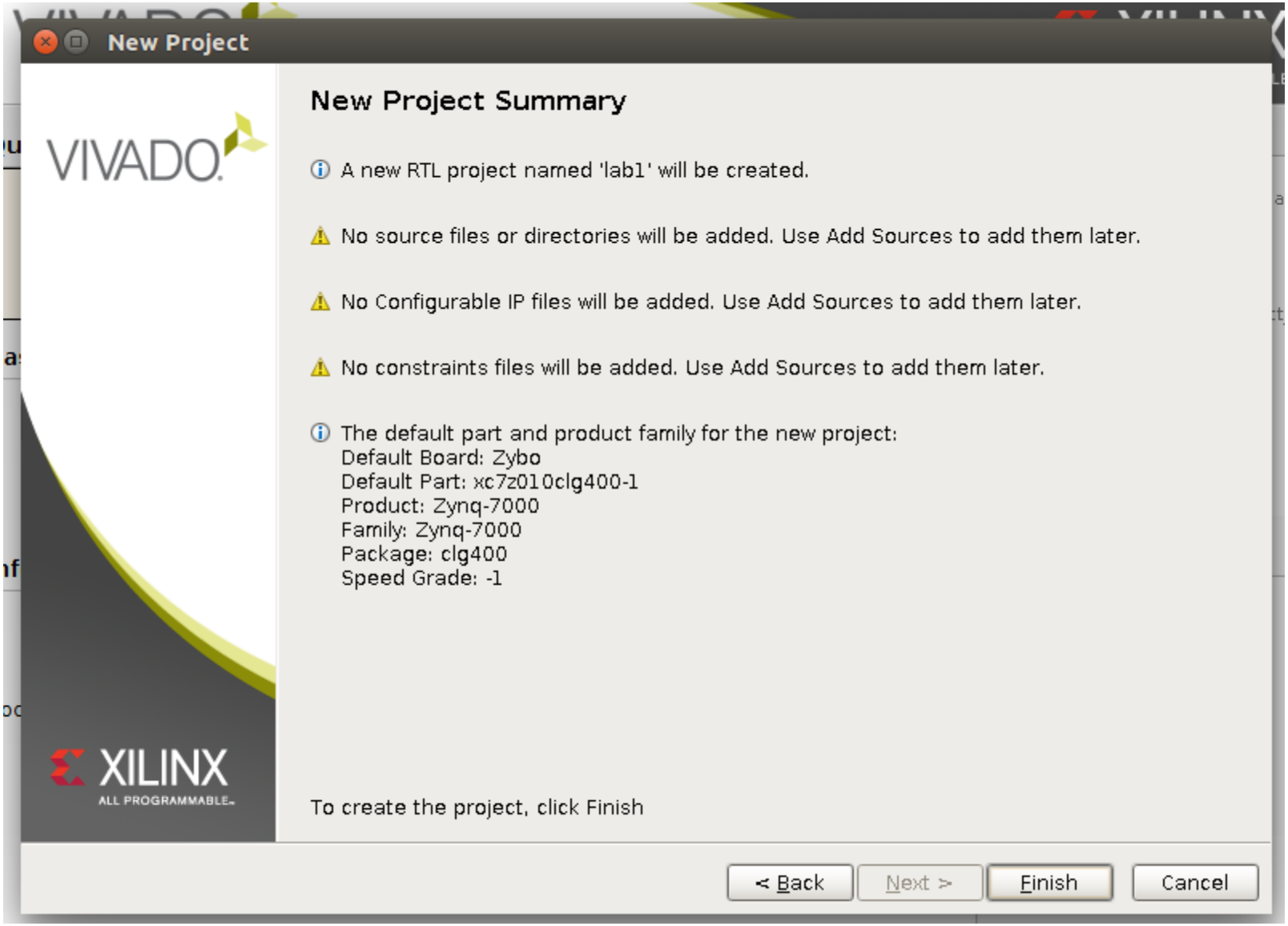

le Flow Tools Window Help
Search commands
New Project
Project Type
Specify the type of project to create.
RTL Project
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.
Do not specify sources at this time
Post-synthesis Project: You will be able to add sources, view device resources, run design analysis, planning and implementation.
Do not specify sources at this time
I/O Planning Project
Do not specify design sources. You will be able to view part/package resources.
Imported Project
Create a Vivado project from a Synplify, XST or ISE Project File.
Example Project
Create a new Vivado project from a predefined template.
< Back
Next >
Finish
Cancel

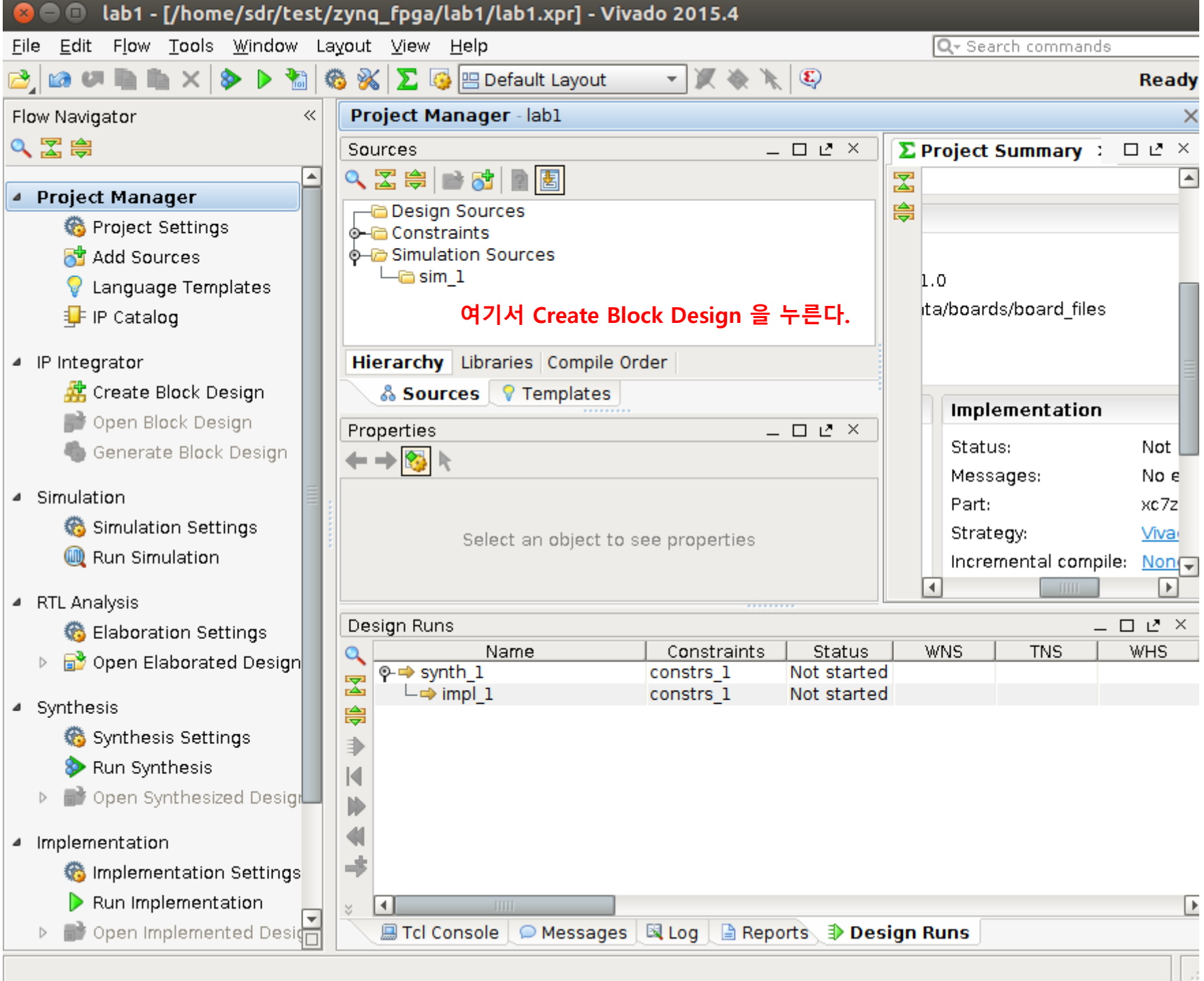

New Project
Add Sources
Specify HDL and netlist files, or directories containing HDL and netlist files, to add to your project. Create a new source file on disk and add it to your project. You can also add and create sources later.
Use Add Files, Add Directories or Create File buttons below
Add Files
Add Directories
Create File
Scan and add RTL include files into project
Copy sources into project
Add sources from subdirectories
Target language:
Verilog
Simulator language:
Verilog
< Back
Next >
Finish
Cancel

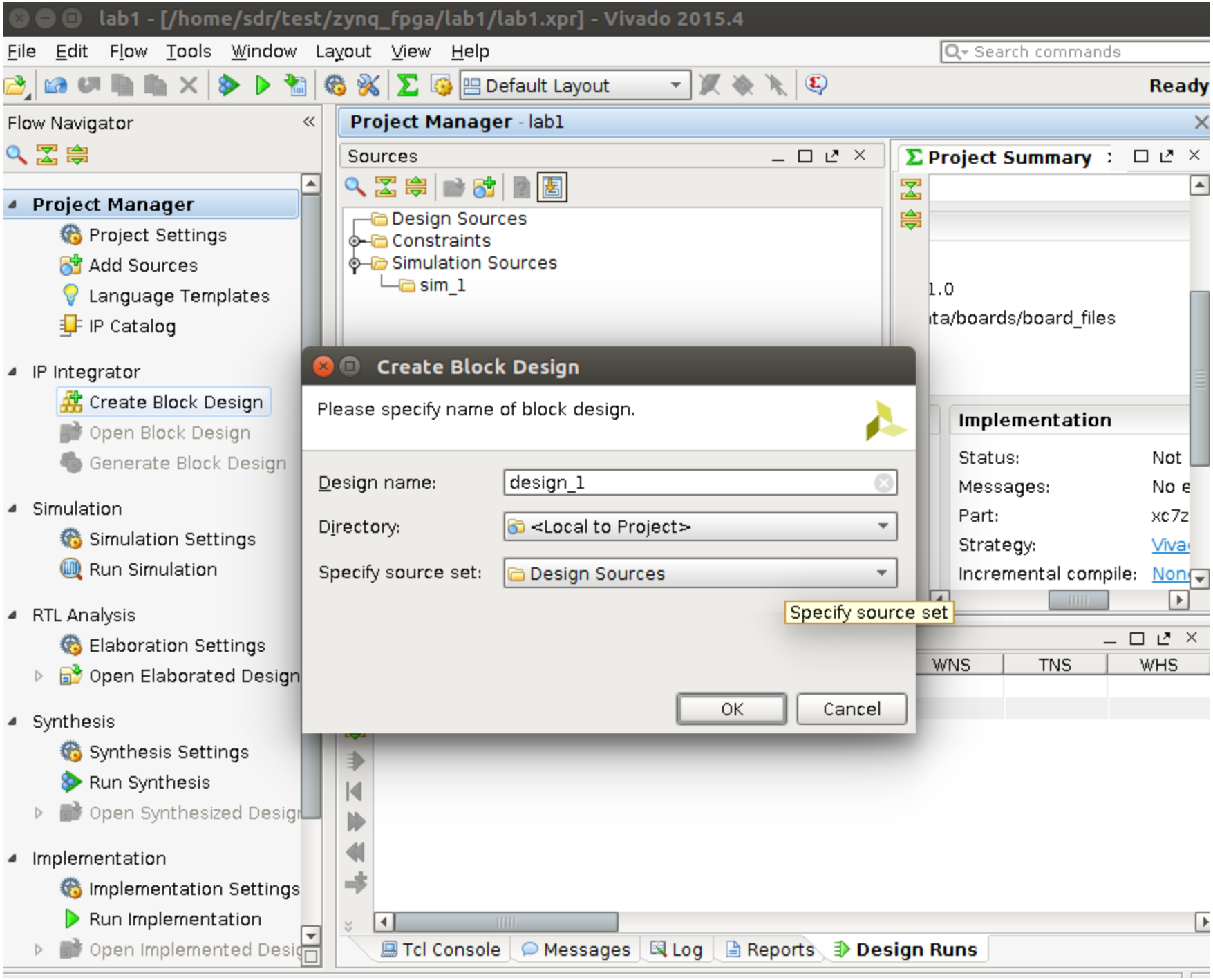

New Project
Add Existing IP (optional)
Specify existing configurable IP, DSP composite, and Embedded sub-design files to add to your project.
Use Add Files or Add Directories buttons below
Add Files
Add Directories
Copy sources into project
< Back
Next >
Finish
Cancel

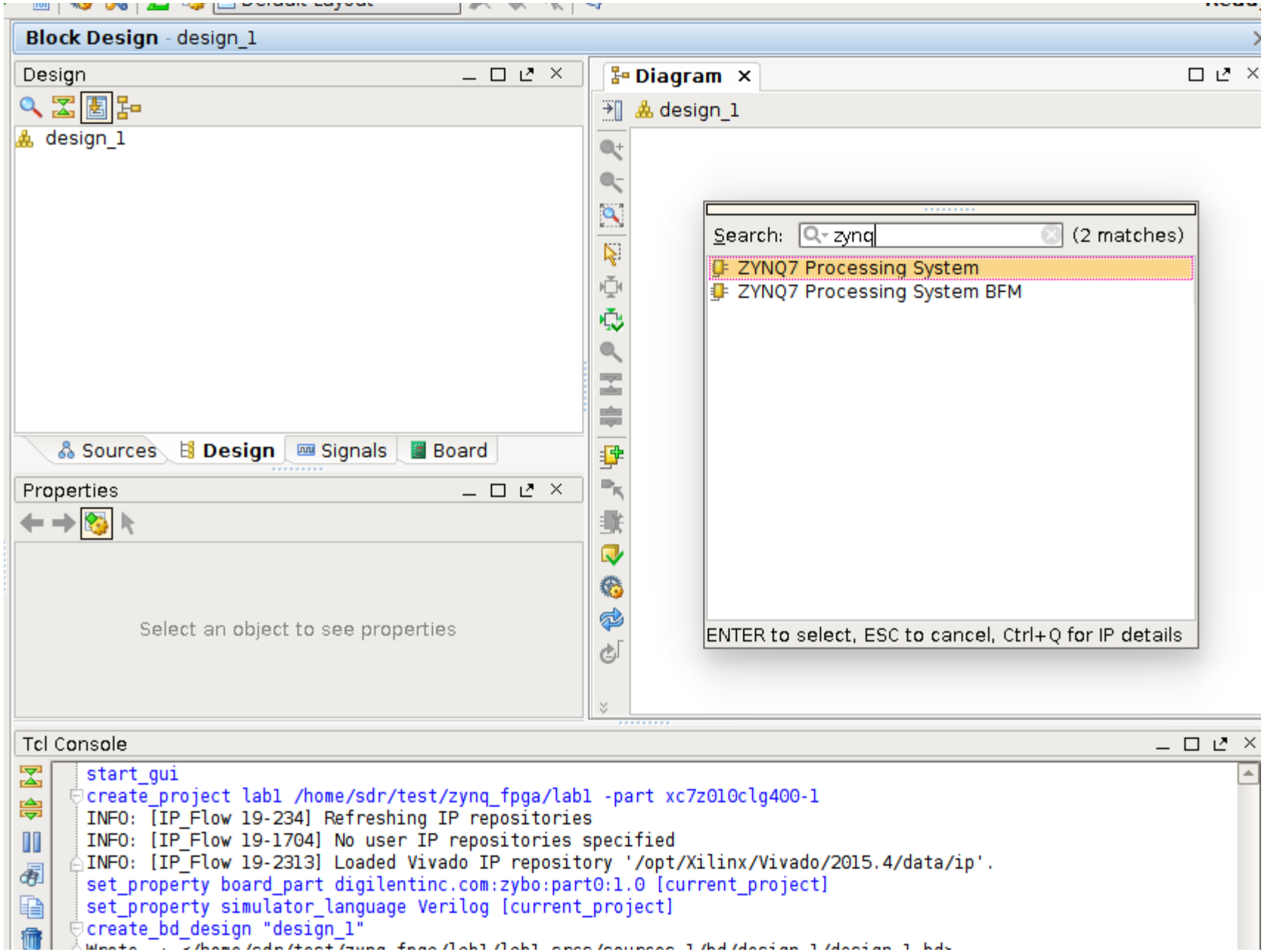

New Project
Add Constraints (optional)
Specify or create constraint files for physical and timing constraints.
Use Add Files or Create File buttons below
Add Files
Create File
Copy constraints files into project
< Back
Next >
Finish
Cancel

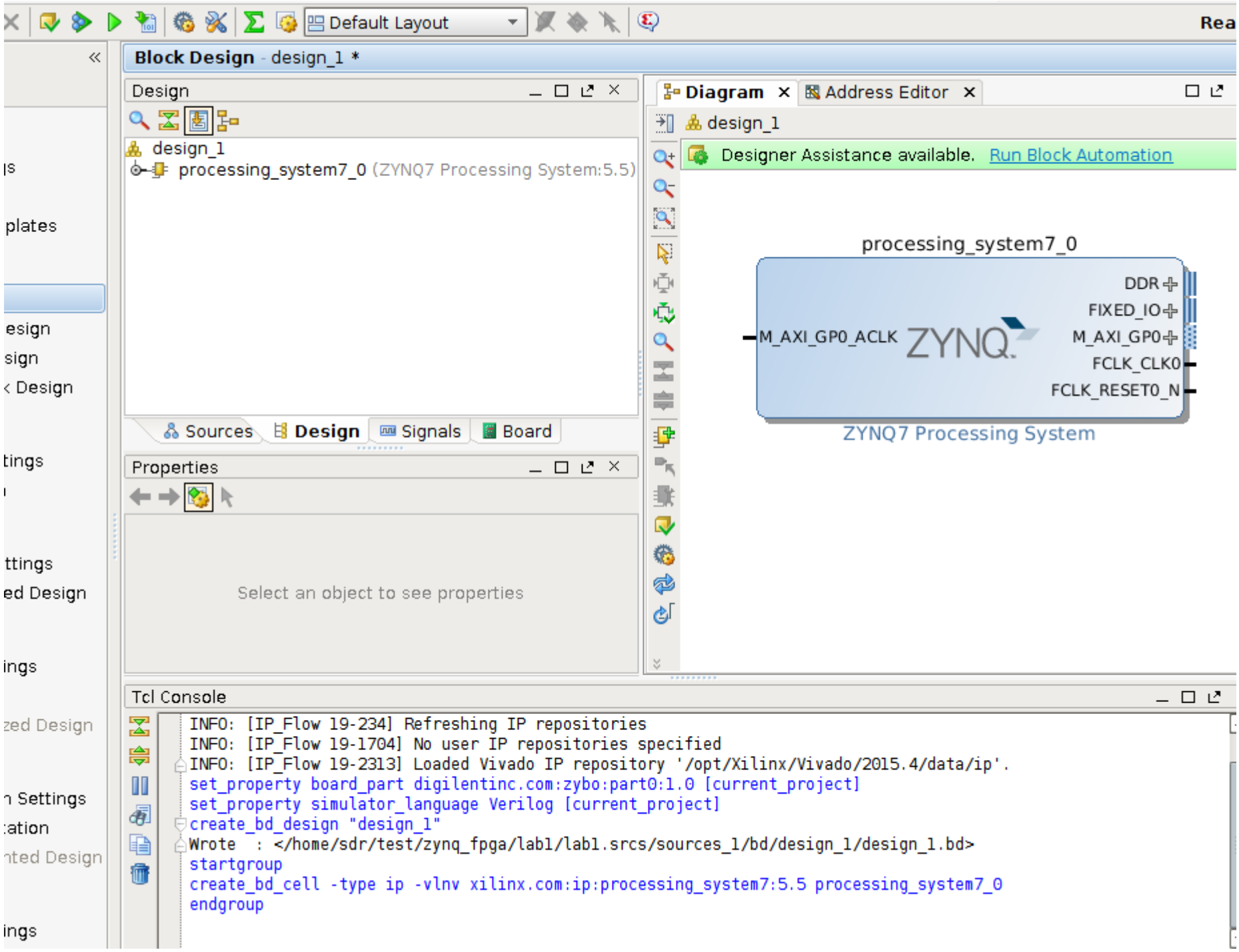

New Project
Default Part
Choose a default Xilinx part or board for your project. This can be changed later.
Select:
Parts
Boards
Filter
Vendor:
All
Display Name:
All
Board Rev:
Latest
Reset All Filters
Search:
Display Name
Vendor
Board Rev
Part
I/O Pin Count
File Ve
Zybo
digilentinc.com
B.3
xc7z010clg400-1
400
1.0
ZedBoard Zynq Evaluation and Development Kit
em.avnet.com
d
xc7z020clg484-1
484
1.3
Artix-7 AC701 Evaluation Platform
xilinx.com
1.1
xc7a200tfbg676-2
676
1.2
ZYNQ-7 ZC702 Evaluation Board
xilinx.com
1.0
xc7z020clg484-1
484
1.2
< Back
Next >
Finish
Cancel

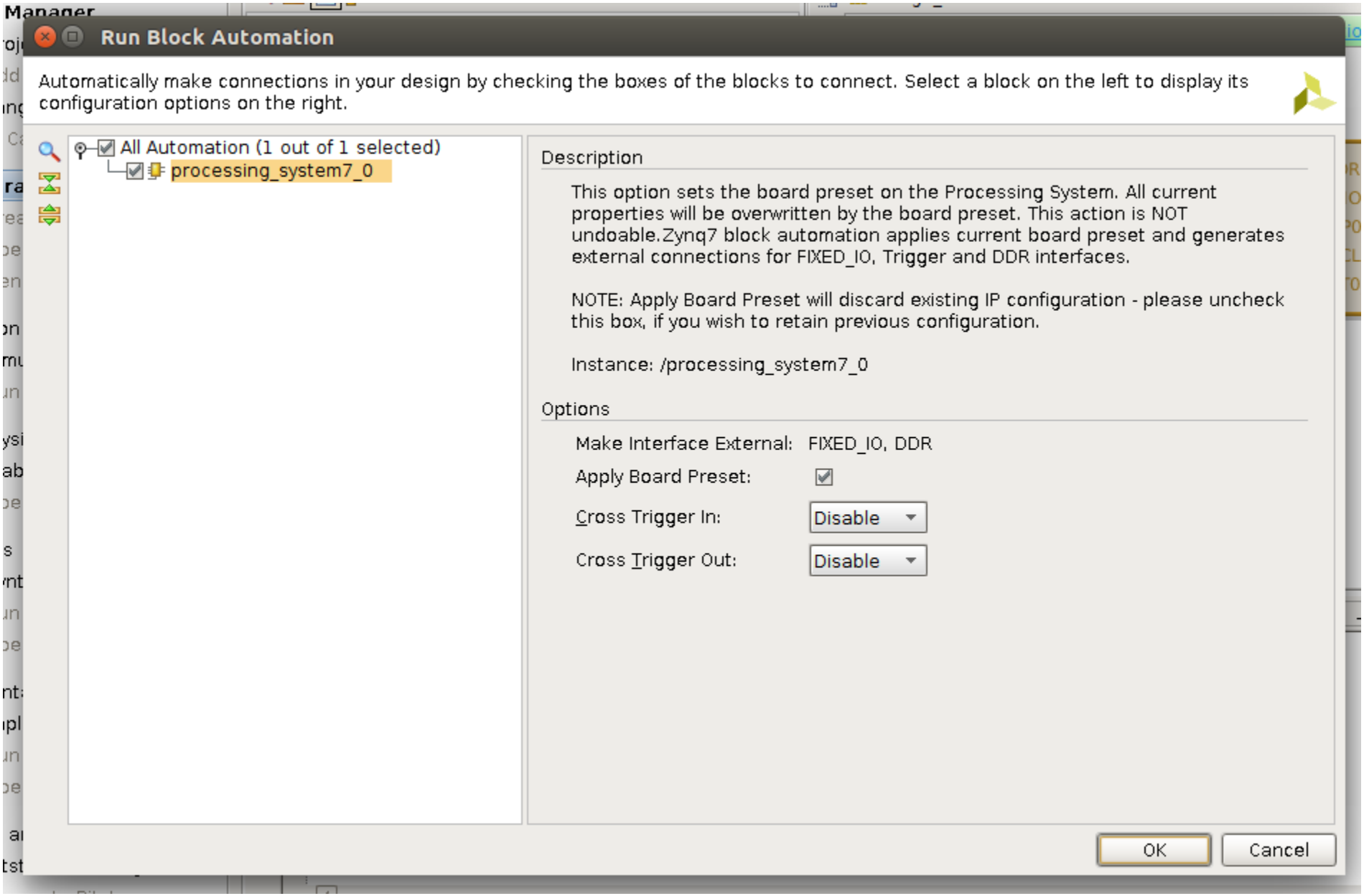

New Project
VIVADO
New Project Summary
A new RTL project named 'lab1' will be created.
No source files or directories will be added. Use Add Sources to add them later.
No Configurable IP files will be added. Use Add Sources to add them later.
No constraints files will be added. Use Add Sources to add them later.
The default part and product family for the new project:
Default Board: Zybo
Default Part: xc7z010clg400-1
Product: Zynq-7000
Family: Zynq-7000
Package: clg400
Speed Grade: -1
XILINX
ALL PROGRAMMABLE.
To create the project, click Finish
< Back
Next >
Finish
Cancel

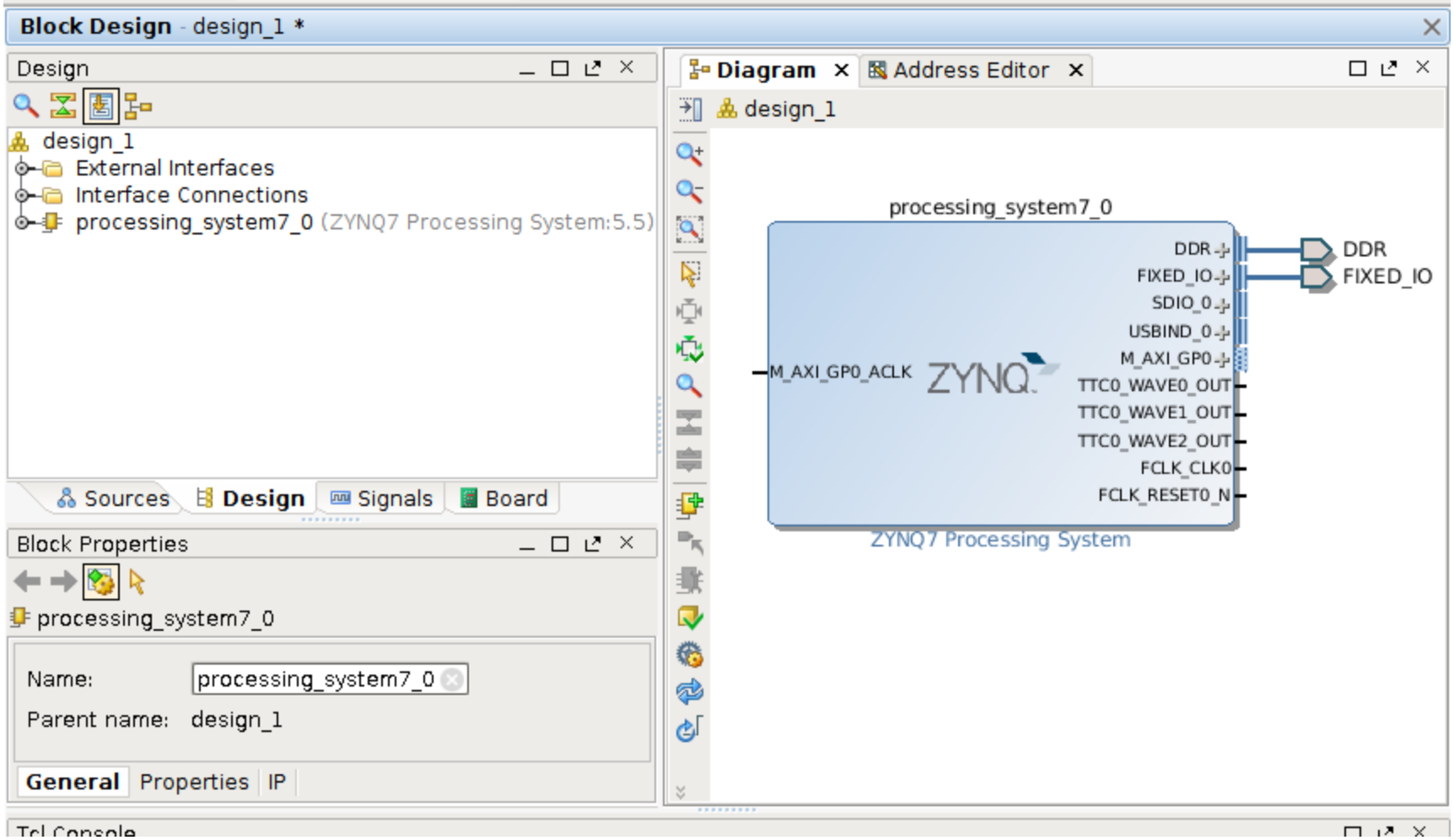

lab1 - [/home/sdr/test/zynq_fpga/lab1/lab1.xpr] - Vivado 2015.4
File Edit Flow Tools Window Layout View Help
Search commands
Default Layout
Ready
Flow Navigator
Project Manager
Project Settings
Add Sources
Language Templates
IP Catalog
IP Integrator
Create Block Design
Open Block Design
Generate Block Design
Simulation
Simulation Settings
Run Simulation
RTL Analysis
Elaboration Settings
Open Elaborated Design
Synthesis
Synthesis Settings
Run Synthesis
Open Synthesized Design
Implementation
Implementation Settings
Run Implementation
Open Implemented Design
Project Manager - lab1
Sources
Design Sources
Constraints
Simulation Sources
sim_1
여기서 Create Block Design 을 누른다.
Hierarchy Libraries Compile Order
Sources Templates
Properties
Select an object to see properties
Project Summary
1.0
ta/boards/board_files
Implementation
Status: Not
Messages: No e
Part: xc7z
Strategy: Viva
Incremental compile: Non
Design Runs
Name Constraints Status WNS TNS WHS
synth_1 constrs_1 Not started
impl_1 constrs_1 Not started
Tcl Console Messages Log Reports Design Runs

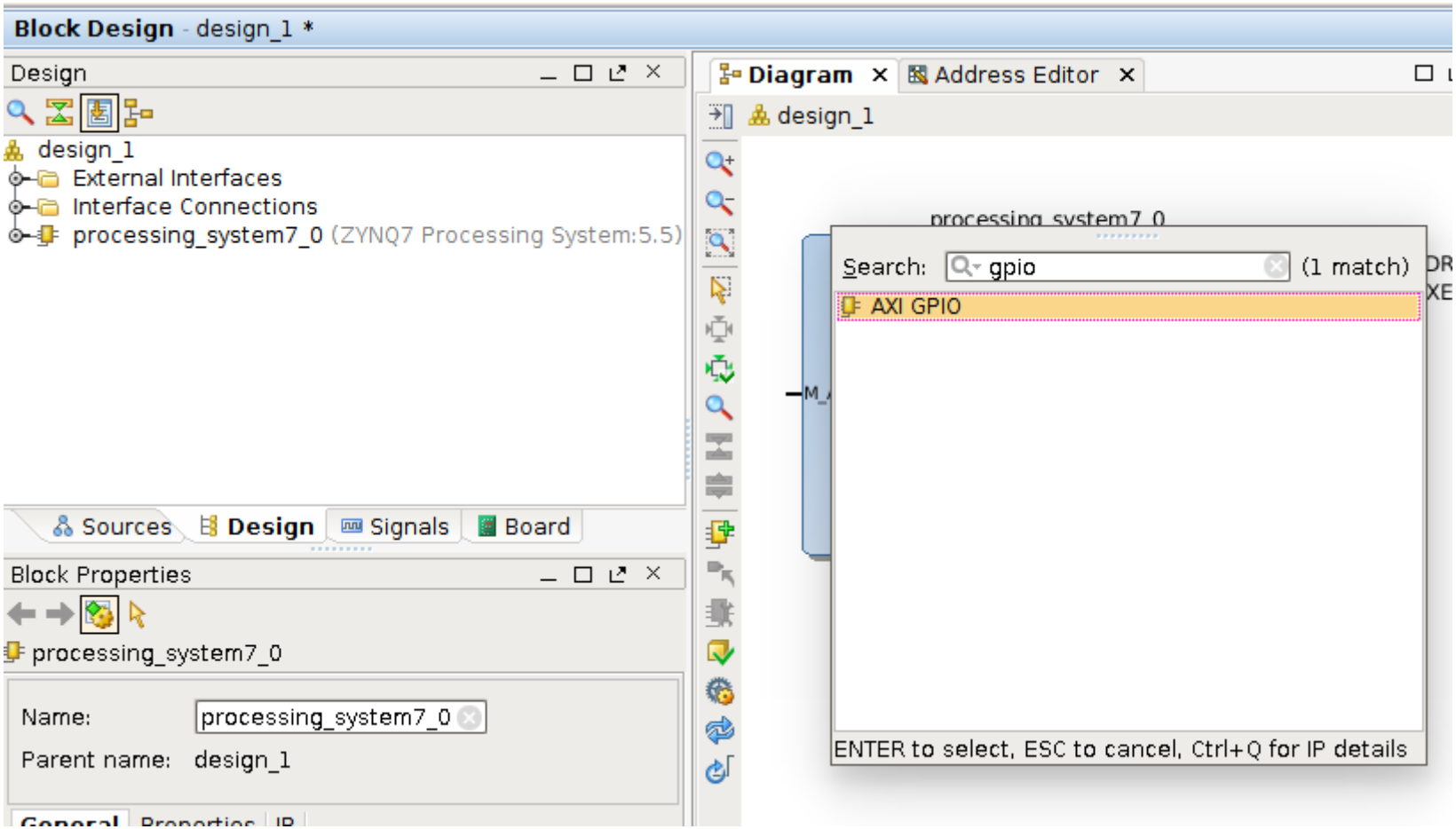

lab1 - [/home/sdr/test/zynq_fpga/lab1/lab1.xpr] - Vivado 2015.4
File Edit Flow Tools Window Layout View Help
Search commands
Default Layout
Ready
Flow Navigator
Project Manager
Project Settings
Add Sources
Language Templates
IP Catalog
IP Integrator
Create Block Design
Open Block Design
Generate Block Design
Simulation
Simulation Settings
Run Simulation
RTL Analysis
Elaboration Settings
Open Elaborated Design
Synthesis
Synthesis Settings
Run Synthesis
Open Synthesized Design
Implementation
Implementation Settings
Run Implementation
Open Implemented Design
Project Manager - lab1
Sources
Design Sources
Constraints
Simulation Sources
sim_1
Project Summary
1.0
ta/boards/board_files
Implementation
Status: Not
Messages: No e
Part: xc7z
Strategy: Viva
Incremental compile: Non
WNS
TNS
WHS
Create Block Design
Please specify name of block design.
Design name: design_1
Directory: <Local to Project>
Specify source set: Design Sources
Specify source set
OK
Cancel
Tcl Console
Messages
Log
Reports
Design Runs

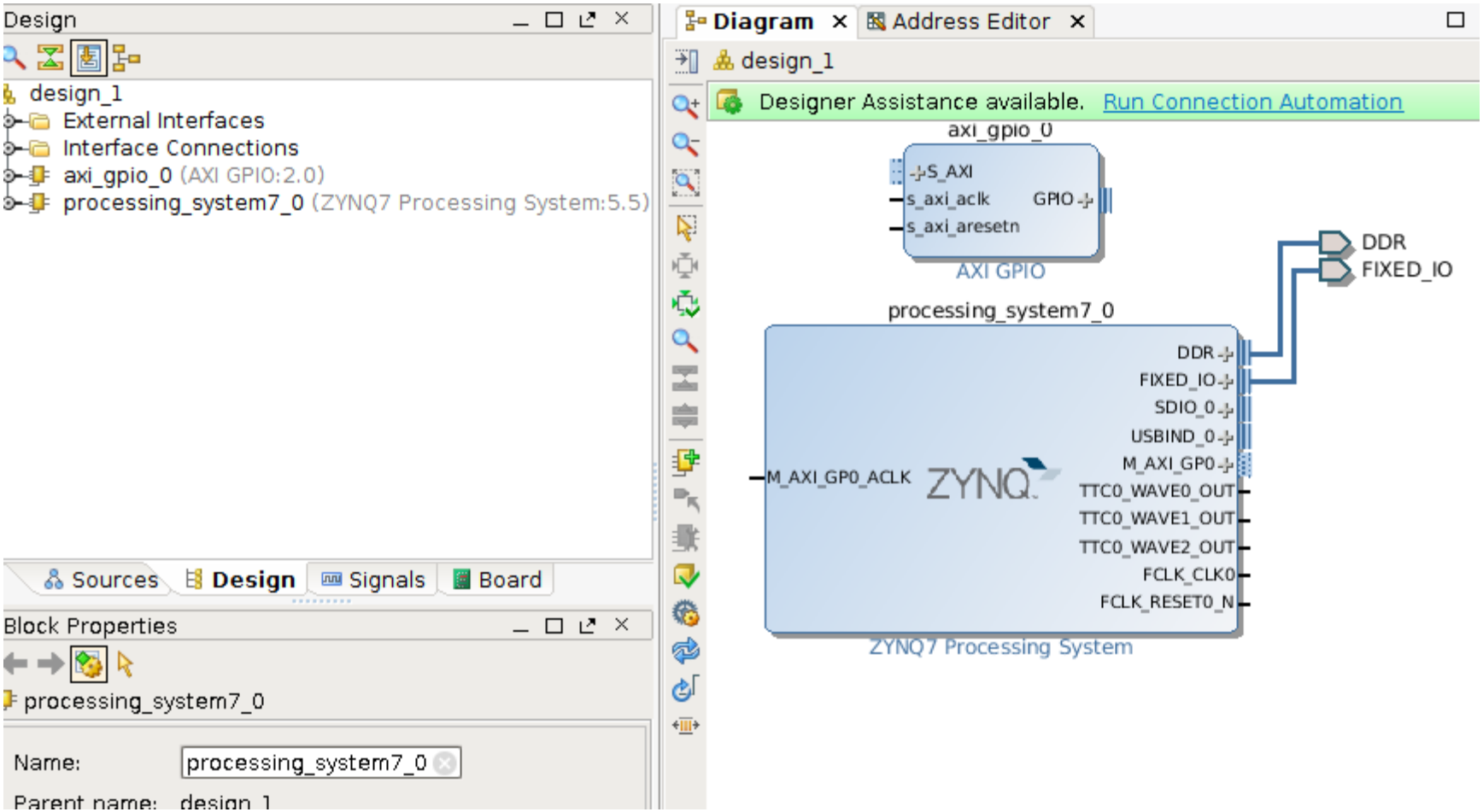

Block Design - design_1
Design
design_1
Sources
Design
Signals
Board
Properties
Select an object to see properties
Diagram
design_1
Search: zynq (2 matches)
ZYNQ7 Processing System
ZYNQ7 Processing System BFM
ENTER to select, ESC to cancel, Ctrl+Q for IP details
Tcl Console
start_gui
create_project lab1 /home/sdr/test/zynq_fpga/lab1 -part xc7z010clg400-1
INFO: [IP_Flow 19-234] Refreshing IP repositories
INFO: [IP_Flow 19-1704] No user IP repositories specified
INFO: [IP_Flow 19-2313] Loaded Vivado IP repository '/opt/Xilinx/Vivado/2015.4/data/ip'.
set_property board_part digilentinc.com:zybo:part0:1.0 [current_project]
set_property simulator_language Verilog [current_project]
create_bd_design "design_1"


Default Layout
Block Design - design_1 *
Design
design_1
processing_system7_0 (ZYNQ7 Processing System:5.5)
Sources
Design
Signals
Board
Properties
Select an object to see properties
Diagram
Address Editor
design_1
Designer Assistance available.
Run Block Automation
processing_system7_0
M_AXI_GP0_ACLK
ZYNQ
DDR
FIXED_IO
M_AXI_GP0
FCLK_CLK0
FCLK_RESET0_N
ZYNQ7 Processing System
Tcl Console
INFO: [IP_Flow 19-234] Refreshing IP repositories
INFO: [IP_Flow 19-1704] No user IP repositories specified
INFO: [IP_Flow 19-2313] Loaded Vivado IP repository '/opt/Xilinx/Vivado/2015.4/data/ip'.
set_property board_part digilentinc.com:zybo:part0:1.0 [current_project]
set_property simulator_language Verilog [current_project]
create_bd_design "design_1"
Wrote : </home/sdr/test/zynq_fpga/lab1/lab1.srcs/sources_1/bd/design_1/design_1.bd>
startgroup
create_bd_cell -type ip -vlnv xilinx.com:ip:processing_system7:5.5 processing_system7_0
endgroup


Run Block Automation
Automatically make connections in your design by checking the boxes of the blocks to connect. Select a block on the left to display its configuration options on the right.
All Automation (1 out of 1 selected)
processing_system7_0
Description
This option sets the board preset on the Processing System. All current properties will be overwritten by the board preset. This action is NOT undoable.Zynq7 block automation applies current board preset and generates external connections for FIXED_IO, Trigger and DDR interfaces.
NOTE: Apply Board Preset will discard existing IP configuration - please uncheck this box, if you wish to retain previous configuration.
Instance: /processing_system7_0
Options
Make Interface External: FIXED_IO, DDR
Apply Board Preset:
Cross Trigger In: Disable
Cross Trigger Out: Disable
OK
Cancel


Block Design - design_1 *
Design
design_1
External Interfaces
Interface Connections
processing_system7_0 (ZYNQ7 Processing System:5.5)
Sources
Design
Signals
Board
Block Properties
processing_system7_0
Name:
processing_system7_0
Parent name:
design_1
General
Properties
IP
Diagram
Address Editor
design_1
processing_system7_0
M_AXI_GP0_ACLK
ZYNQ
DDR
FIXED_IO
SDIO_0
USBIND_0
M_AXI_GP0
TTC0_WAVE0_OUT
TTC0_WAVE1_OUT
TTC0_WAVE2_OUT
FCLK_CLK0
FCLK_RESET0_N
DDR
FIXED_IO
ZYNQ7 Processing System
Tcl Console


Block Design - design_1 *
Design
design_1
External Interfaces
Interface Connections
processing_system7_0 (ZYNQ7 Processing System:5.5)
Sources
Design
Signals
Board
Block Properties
processing_system7_0
Name:
processing_system7_0
Parent name:
design_1
Diagram
Address Editor
design_1
processing_system7_0
Search:
gpio
(1 match)
AXI GPIO
ENTER to select, ESC to cancel, Ctrl+Q for IP details

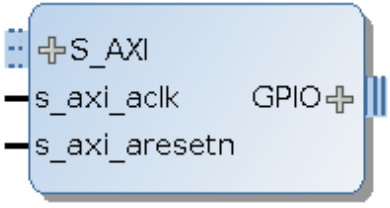

Design
design_1
External Interfaces
Interface Connections
axi_gpio_0 (AXI GPIO:2.0)
processing_system7_0 (ZYNQ7 Processing System:5.5)
Sources
Design
Signals
Board
Block Properties
processing_system7_0
Name:
processing_system7_0
Parent name:
design_1
Diagram
Address Editor
design_1
Designer Assistance available.
Run Connection Automation
axi_gpio_0
S_AXI
s_axi_aclk
s_axi_aresetn
GPIO
AXI GPIO
processing_system7_0
M_AXI_GP0_ACLK
ZYNQ
DDR
FIXED_IO
SDIO_0
USBIND_0
M_AXI_GP0
TTC0_WAVE0_OUT
TTC0_WAVE1_OUT
TTC0_WAVE2_OUT
FCLK_CLK0
FCLK_RESET0_N
ZYNQ7 Processing System
DDR
FIXED_IO

Re-customize IP

AXI GPIO (2.0)

Documentation | IP Location

Show disabled ports



Component Name: design_1_axi_gpio_0_0

Board | IP Configuration

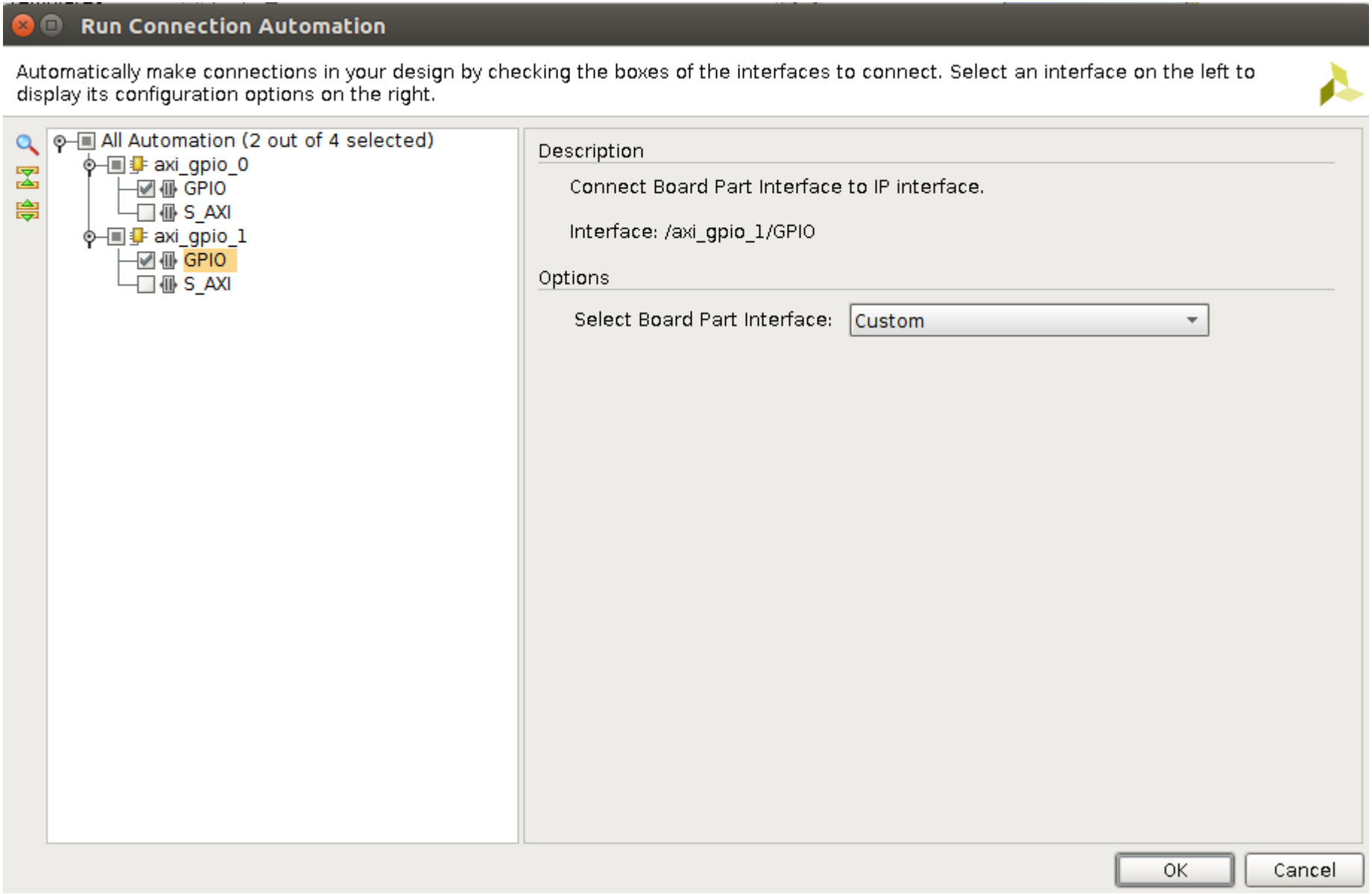
Associate IP interface with board interface

IP Interface	Board Interface
GPIO	Custom
GPIO2	Custom

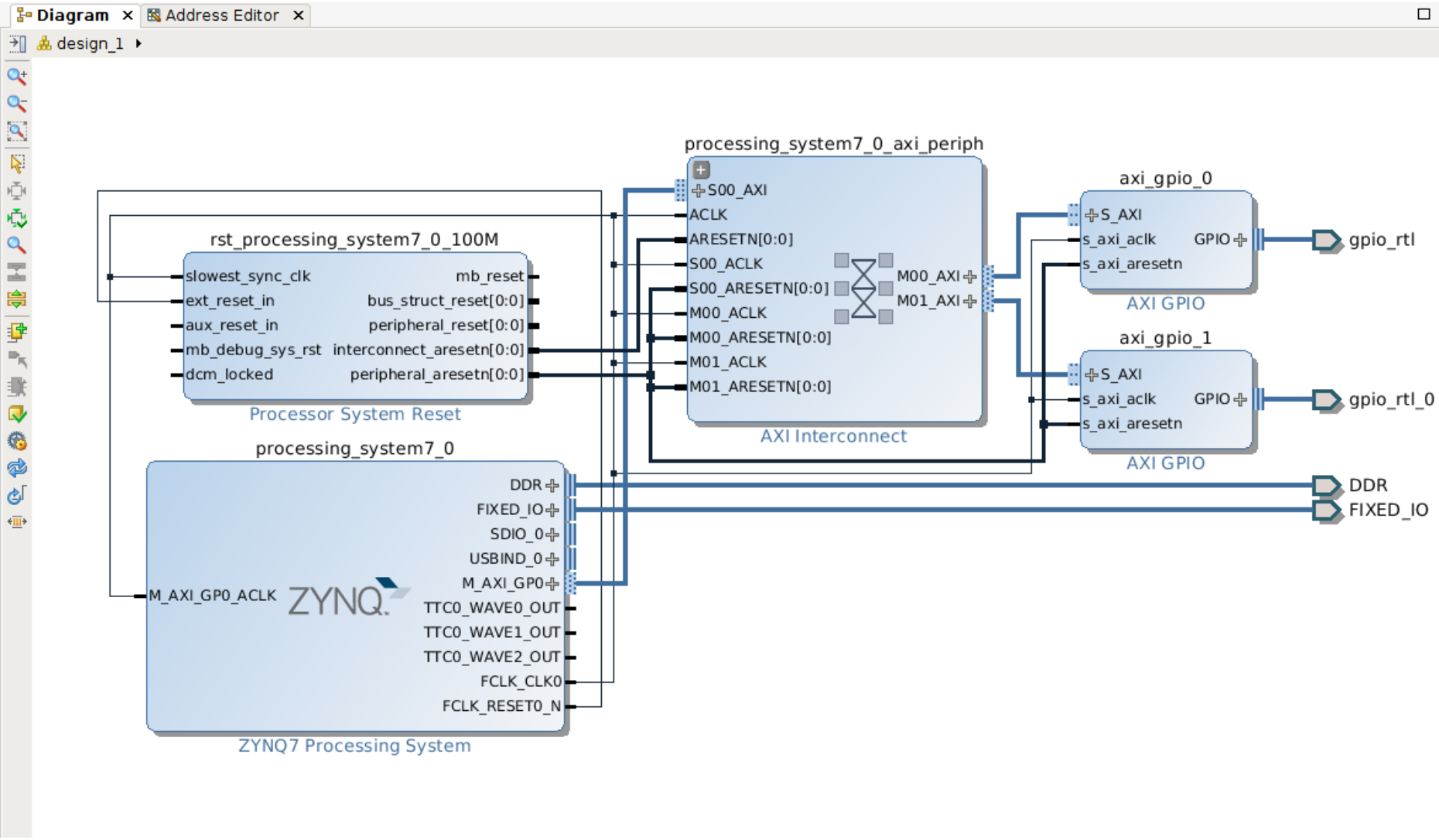
Clear Board Parameters

Enable Interrupt

OK | Cancel


Run Connection Automation
Automatically make connections in your design by checking the boxes of the interfaces to connect. Select an interface on the left to display its configuration options on the right.
All Automation (2 out of 4 selected)
axi_gpio_0
GPIO
S_AXI
axi_gpio_1
GPIO
S_AXI
Description
Connect Board Part Interface to IP interface.
Interface: /axi_gpio_1/GPIO
Options
Select Board Part Interface:
Custom
OK
Cancel

마저 나머지 부분도 자동 연결을 구성하도록 한다.



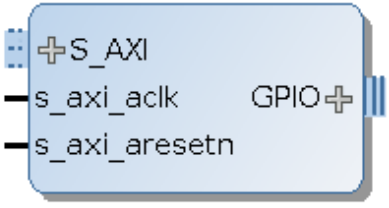
Re-customize IP

AXI GPIO (2.0)

LED 1 개만 킬 것이므로 1 비트를 사용한다.

Documentation IP Location

Show disabled ports



Component Name: test_design_axi_gpio_0_0

Board | IP Configuration

GPIO

- All Inputs
- All Outputs
- GPIO Width: 1 [1 - 32]
- Default Output Value: 0x00000000 [0x00000000,0xFFFFFFFF]
- Default Tri State Value: 0xFFFFFFFF [0x00000000,0xFFFFFFFF]

Enable Dual Channel

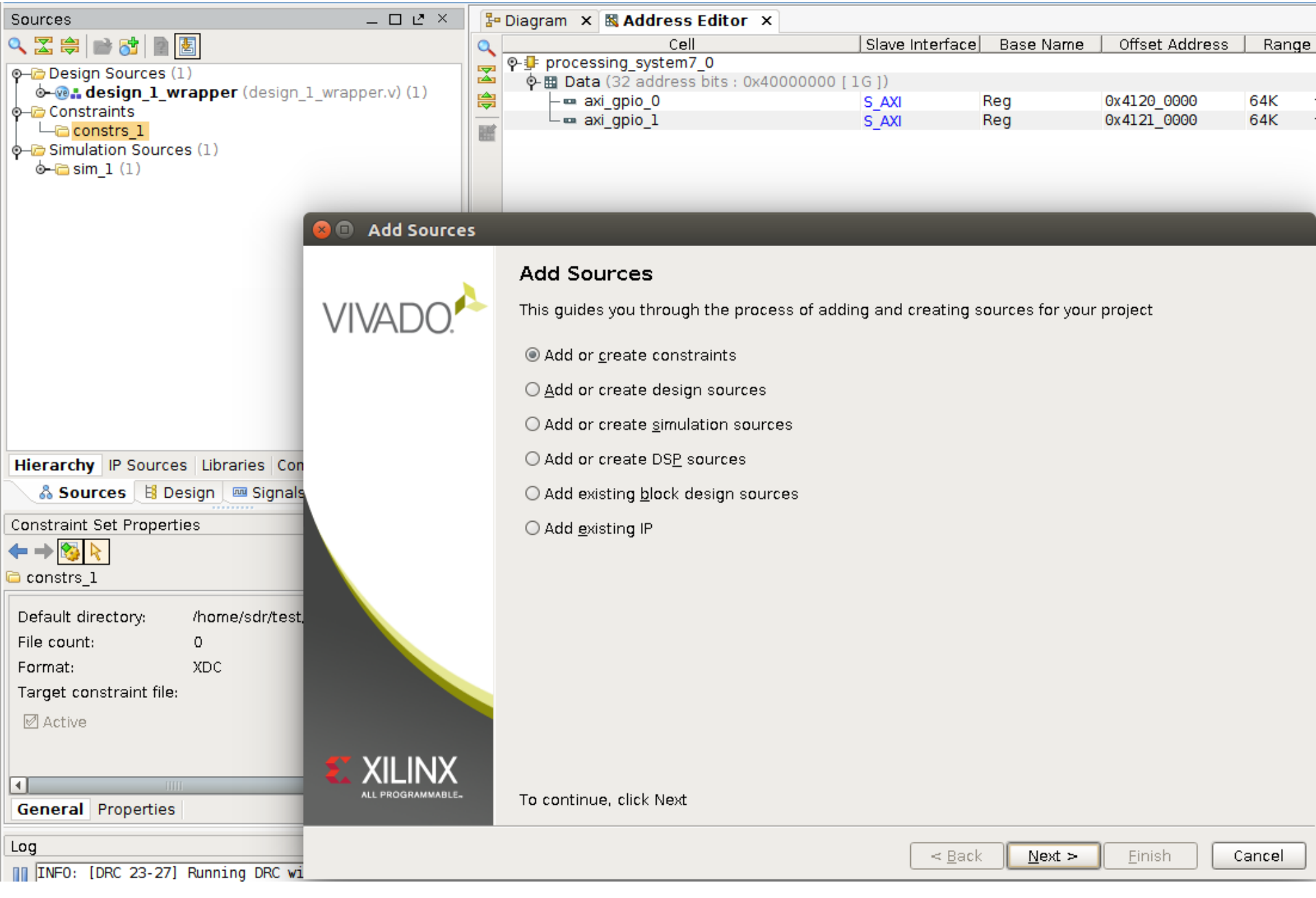
GPIO 2

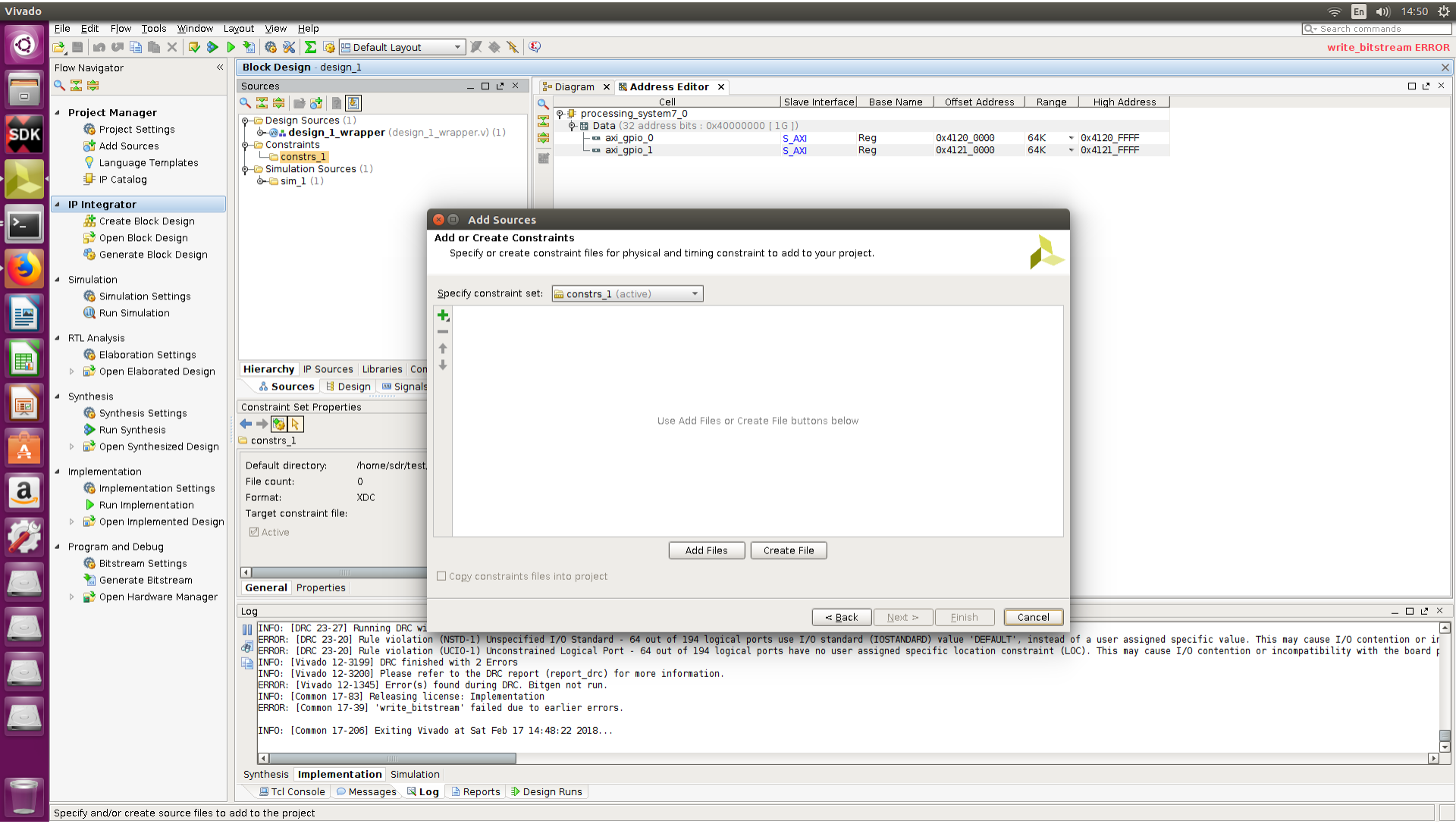
- All Inputs
- All Outputs
- GPIO Width: 32 [1 - 32]
- Default Output Value: 0x00000000 [0x00000000,0xFFFFFFFF]
- Default Tri State Value: 0xFFFFFFFF [0x00000000,0xFFFFFFFF]

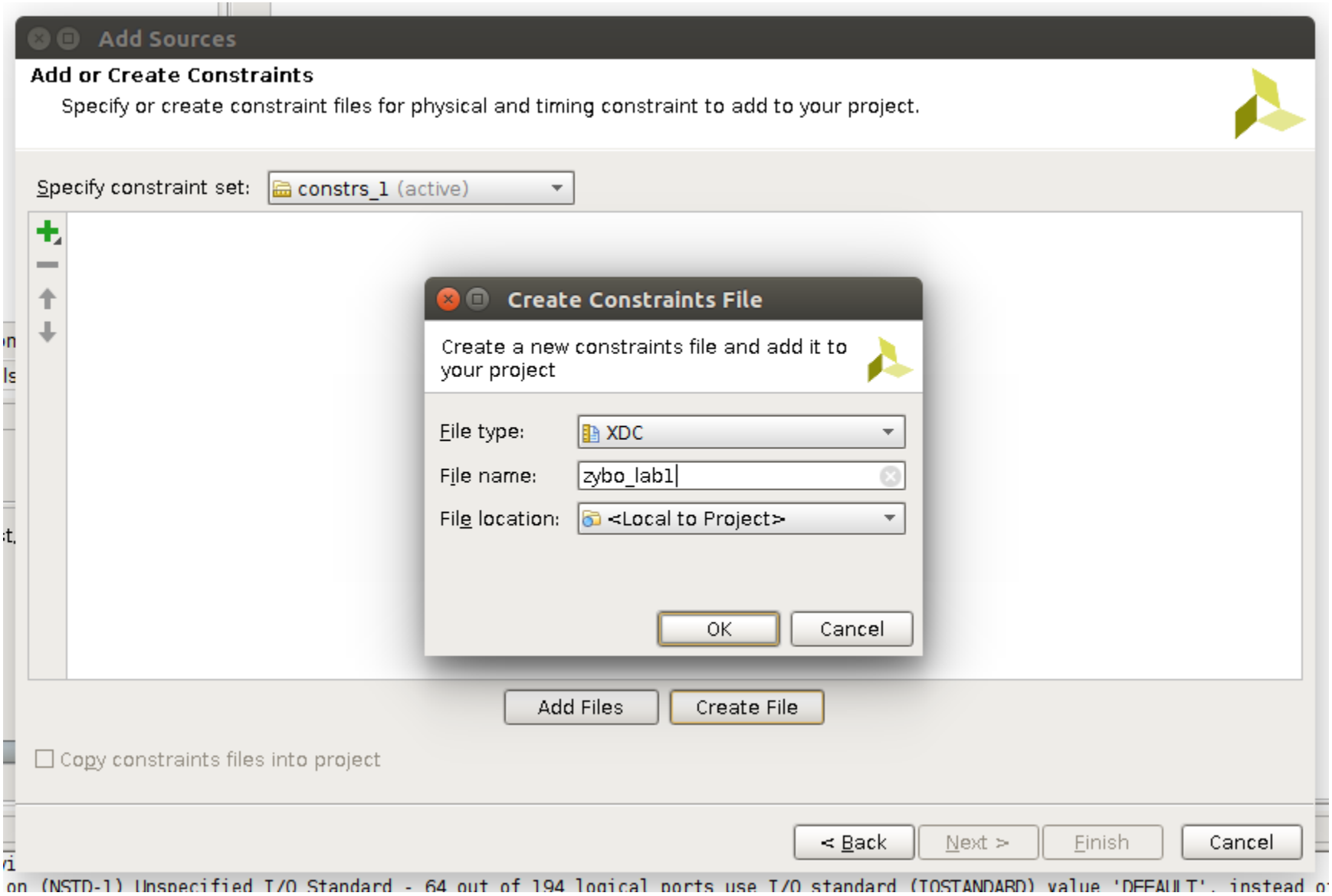
Enable Interrupt

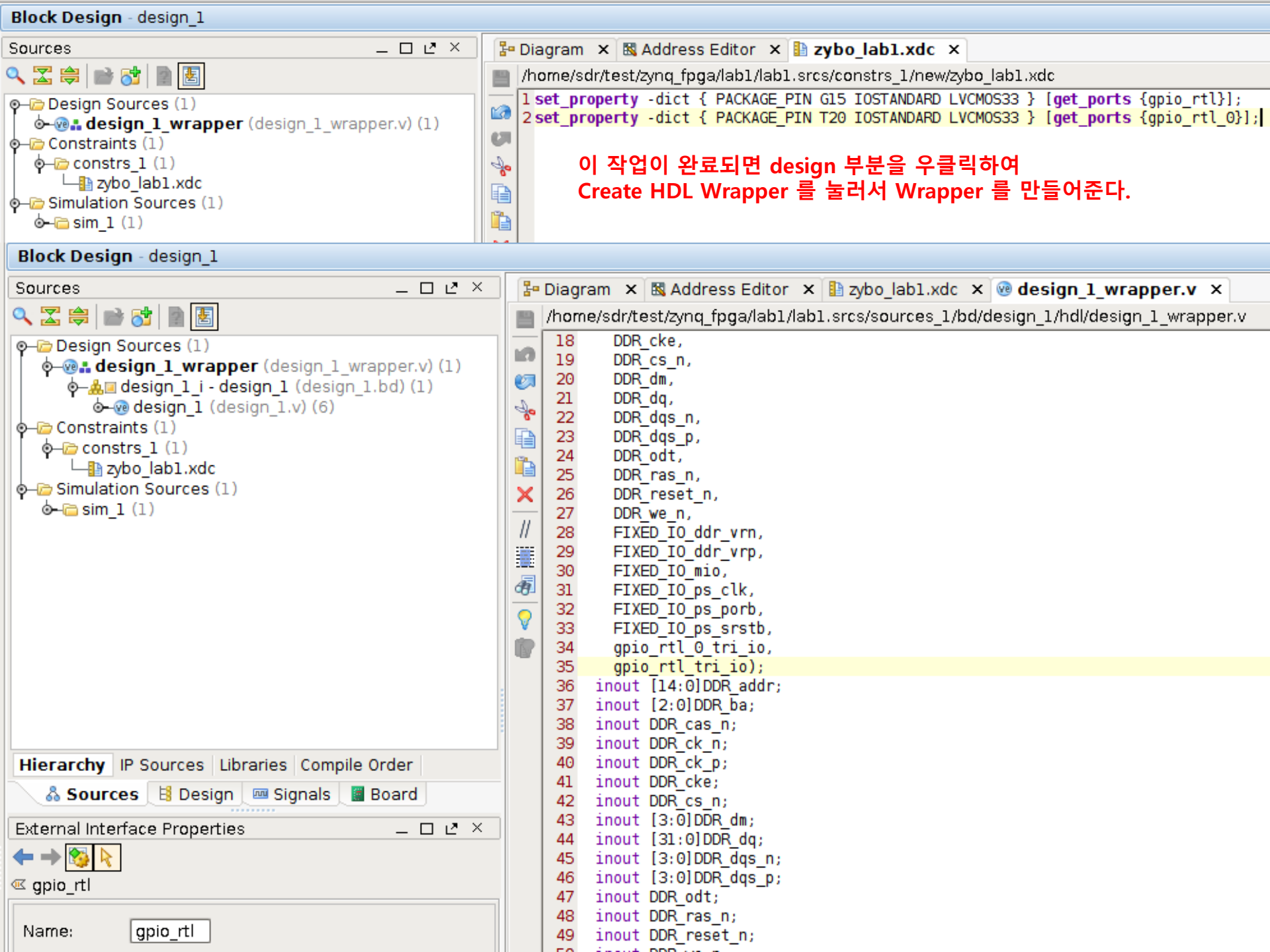
OK Cancel

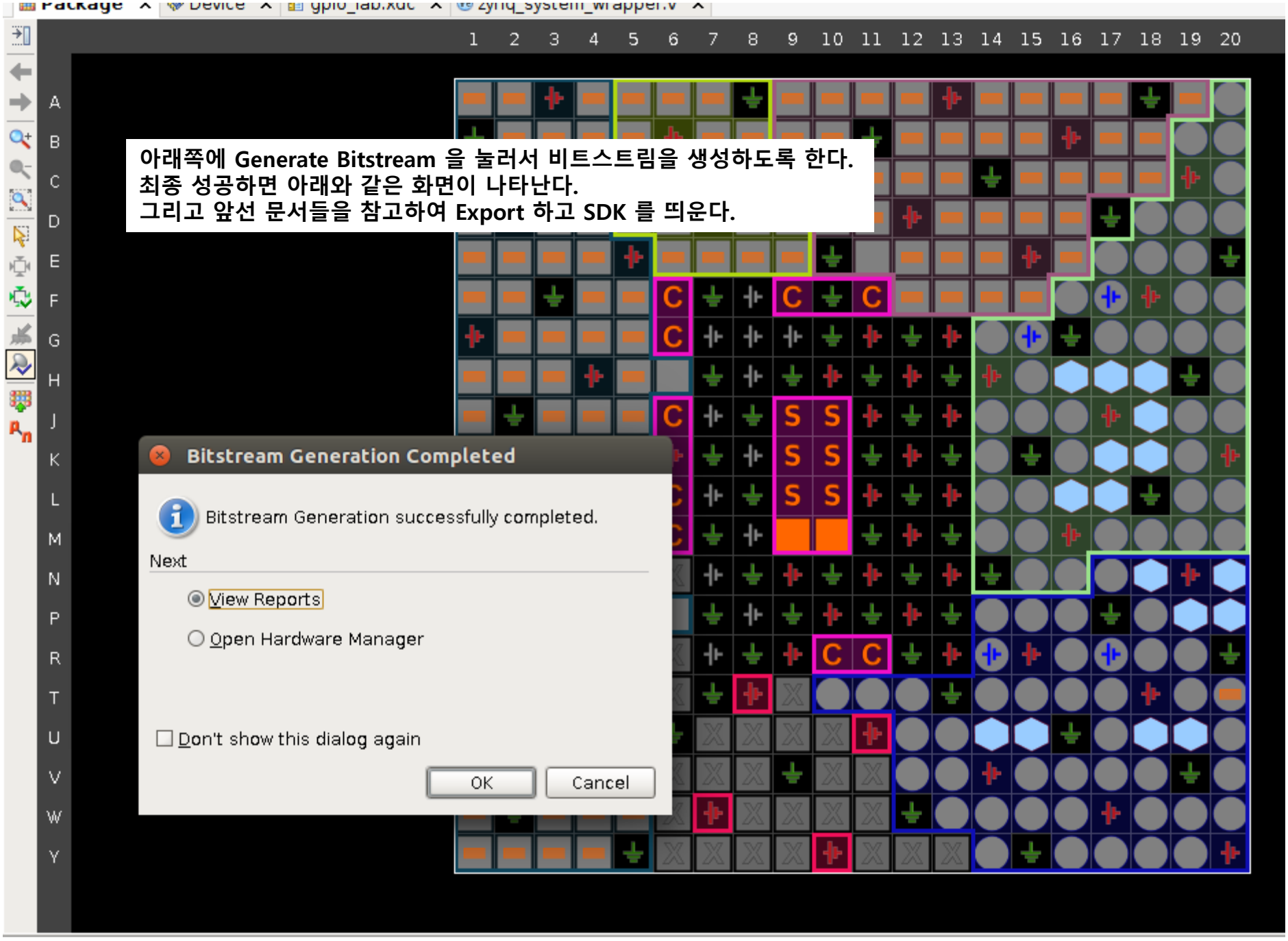
Constraints 부분에 우클릭하여 제약 사항을 설정하도록 한다.

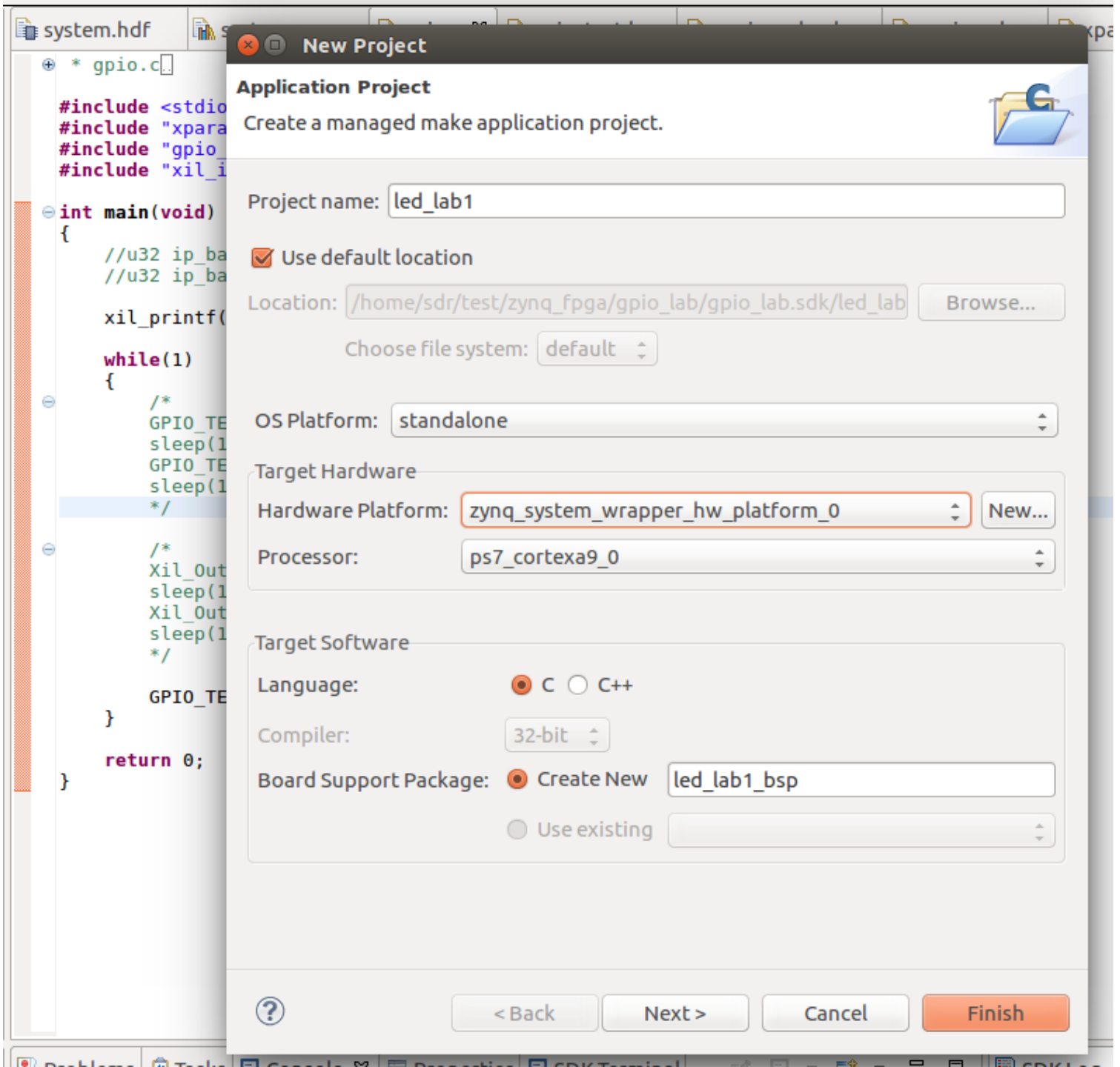


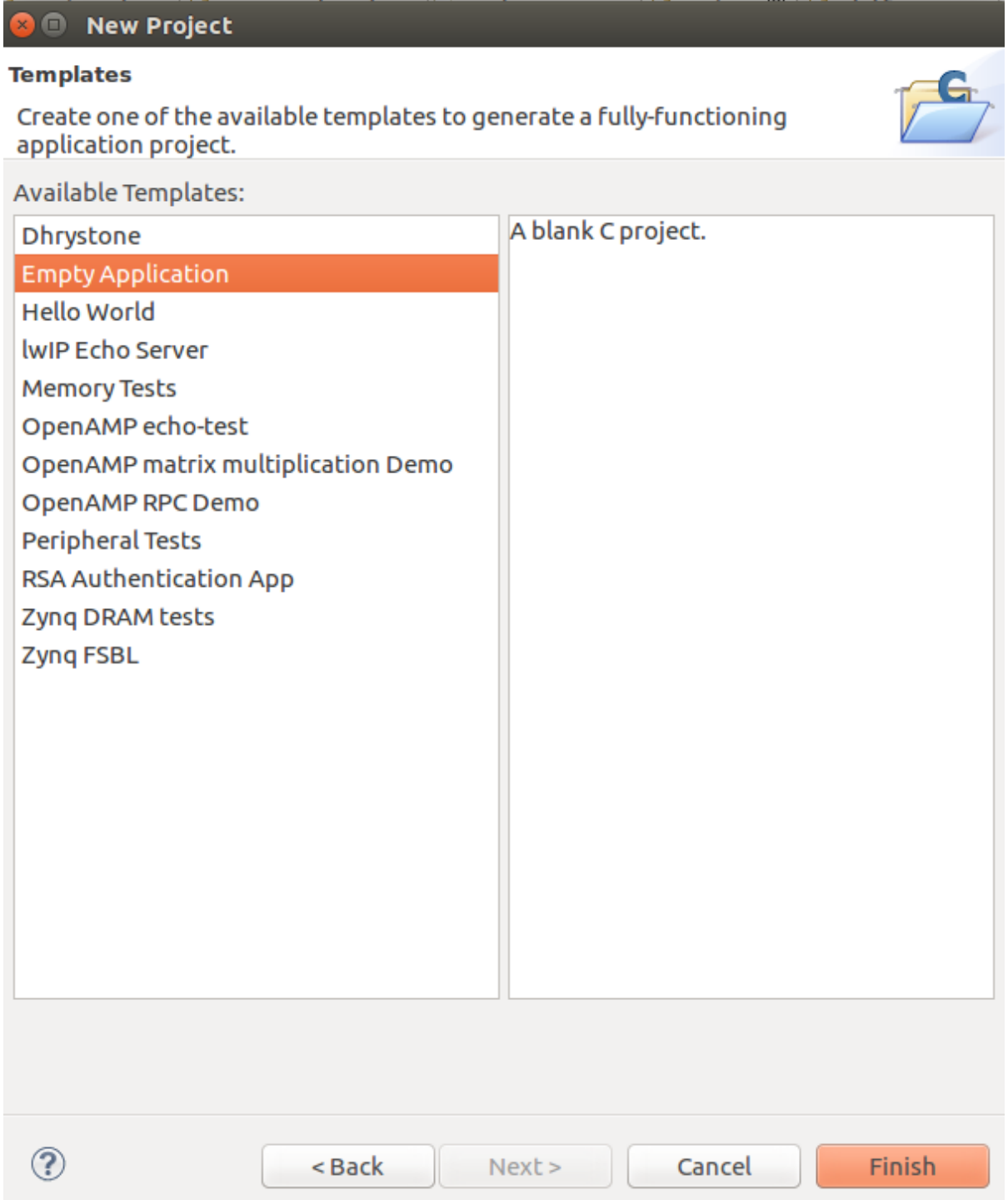

Vivado
File Edit Flow Tools Window Layout View Help
write_bitstream ERROR
Flow Navigator
Project Manager
Project Settings
Add Sources
Language Templates
IP Catalog
IP Integrator
Create Block Design
Open Block Design
Generate Block Design
Simulation
Simulation Settings
Run Simulation
RTL Analysis
Elaboration Settings
Open Elaborated Design
Synthesis
Synthesis Settings
Run Synthesis
Open Synthesized Design
Implementation
Implementation Settings
Run Implementation
Open Implemented Design
Program and Debug
Bitstream Settings
Generate Bitstream
Open Hardware Manager
Block Design - design_1
Sources
Design Sources (1)
design_1_wrapper (design_1_wrapper.v) (1)
Constraints
constrs_1
Simulation Sources (1)
sim_1 (1)
Diagram
Address Editor
Cell
Slave Interface
Base Name
Offset Address
Range
High Address
processing_system7_0
Data (32 address bits : 0x40000000 [1G])
axi_gpio_0
S_AXI
Reg
0x4120_0000
64K
0x4120_FFFF
axi_gpio_1
S_AXI
Reg
0x4121_0000
64K
0x4121_FFFF
Add Sources
Add or Create Constraints
Specify or create constraint files for physical and timing constraint to add to your project.
Specify constraint set:
constrs_1 (active)
Use Add Files or Create File buttons below
Add Files
Create File
Copy constraints files into project
< Back
Next >
Finish
Cancel
Hierarchy
IP Sources
Libraries
Sources
Design
Signals
Constraint Set Properties
constrs_1
Default directory:
/home/sdr/test
File count:
0
Format:
XDC
Target constraint file:
Active
General
Properties
Log
INFO: [DRC 23-27] Running DRC wi
ERROR: [DRC 23-20] Rule violation (NSTD-1) Unspecified I/O Standard - 64 out of 194 logical ports use I/O standard (IOSTANDARD) value 'DEFAULT', instead of a user assigned specific value. This may cause I/O contention or ir
ERROR: [DRC 23-20] Rule violation (UCIO-1) Unconstrained Logical Port - 64 out of 194 logical ports have no user assigned specific location constraint (LOC). This may cause I/O contention or incompatibility with the board p
INFO: [Vivado 12-3199] DRC finished with 2 Errors
INFO: [Vivado 12-3200] Please refer to the DRC report (report_drc) for more information.
ERROR: [Vivado 12-1345] Error(s) found during DRC. Bitgen not run.
INFO: [Common 17-83] Releasing license: Implementation
ERROR: [Common 17-39] 'write_bitstream' failed due to earlier errors.
INFO: [Common 17-206] Exiting Vivado at Sat Feb 17 14:48:22 2018...
Synthesis
Implementation
Simulation
Tcl Console
Messages
Log
Reports
Design Runs
Specify and/or create source files to add to the project

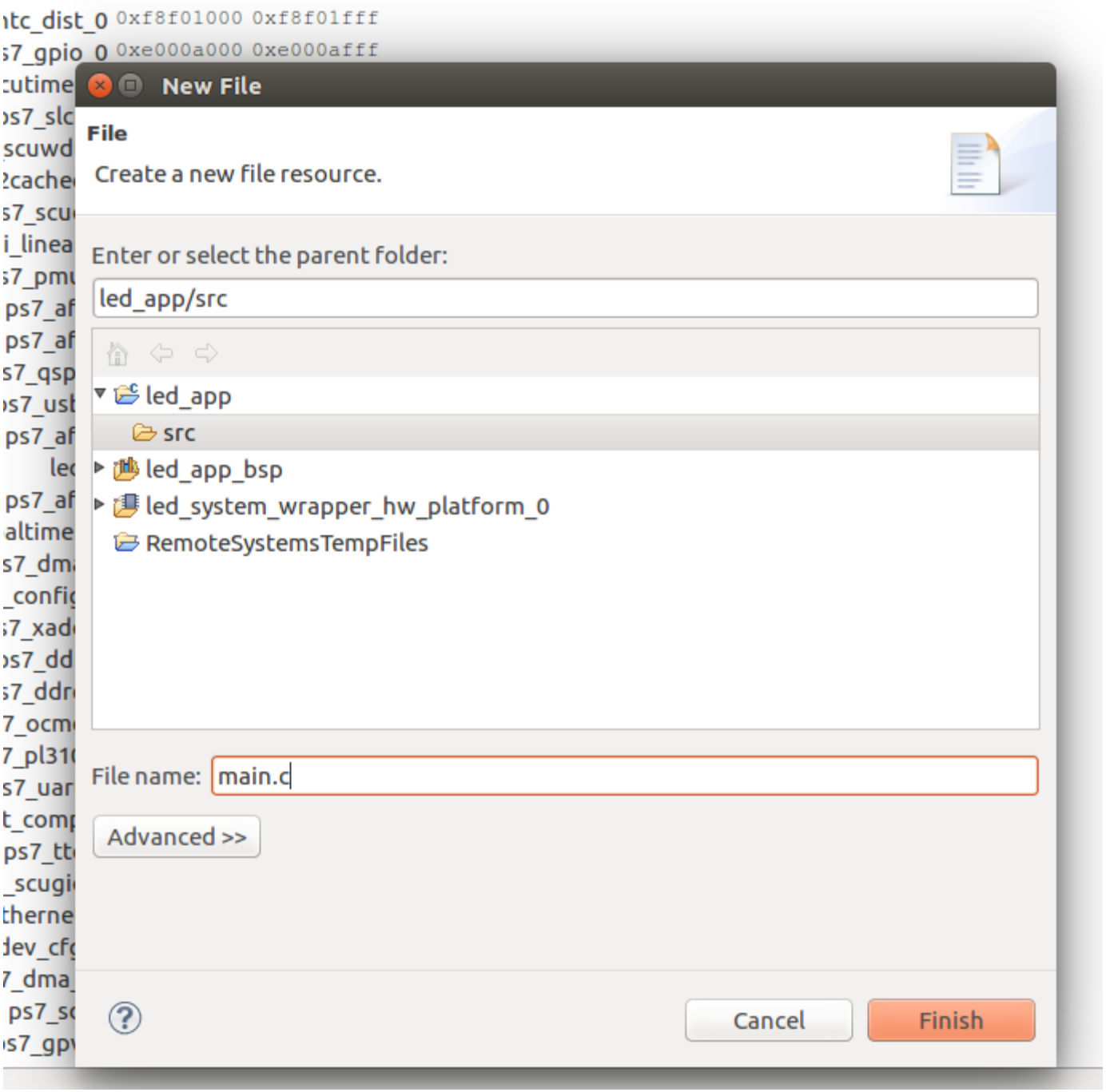

Add Sources
Add or Create Constraints
Specify or create constraint files for physical and timing constraint to add to your project.
Specify constraint set:
constrs_1 (active)
Create Constraints File
Create a new constraints file and add it to your project
File type:
XDC
File name:
zybo_lab1
File location:
<Local to Project>
OK
Cancel
Add Files
Create File
Copy constraints files into project
< Back
Next >
Finish
Cancel


Block Design - design_1
Sources
Design Sources (1)
design_1_wrapper (design_1_wrapper.v) (1)
Constraints (1)
constrs_1 (1)
zybo_lab1.xdc
Simulation Sources (1)
sim_1 (1)
Diagram
Address Editor
zybo_lab1.xdc
/home/sdr/test/zynq_fpga/lab1/lab1.srcs/constrs_1/new/zybo_lab1.xdc
1 set_property -dict { PACKAGE_PIN G15 IOSTANDARD LVCMOS33 } [get_ports {gpio_rtl}];
2 set_property -dict { PACKAGE_PIN T20 IOSTANDARD LVCMOS33 } [get_ports {gpio_rtl_0}];
이 작업이 완료되면 design 부분을 우클릭하여
Create HDL Wrapper 를 눌러서 Wrapper 를 만들어준다.
Block Design - design_1
Sources
Design Sources (1)
design_1_wrapper (design_1_wrapper.v) (1)
design_1_i - design_1 (design_1.bd) (1)
design_1 (design_1.v) (6)
Constraints (1)
constrs_1 (1)
zybo_lab1.xdc
Simulation Sources (1)
sim_1 (1)
Hierarchy
IP Sources
Libraries
Compile Order
Sources
Design
Signals
Board
External Interface Properties
gpio_rtl
Name:
gpio_rtl
Diagram
Address Editor
zybo_lab1.xdc
design_1_wrapper.v
/home/sdr/test/zynq_fpga/lab1/lab1.srcs/sources_1/bd/design_1/hdl/design_1_wrapper.v
18 DDR_cke,
19 DDR_cs_n,
20 DDR_dm,
21 DDR_dq,
22 DDR_dqs_n,
23 DDR_dqs_p,
24 DDR_odt,
25 DDR_ras_n,
26 DDR_reset_n,
27 DDR_we_n,
28 FIXED_IO_ddr_vrn,
29 FIXED_IO_ddr_vrp,
30 FIXED_IO_mio,
31 FIXED_IO_ps_clk,
32 FIXED_IO_ps_porb,
33 FIXED_IO_ps_srstb,
34 gpio_rtl_0_tri_io,
35 gpio_rtl_tri_io);
36 inout [14:0]DDR_addr;
37 inout [2:0]DDR_ba;
38 inout DDR_cas_n;
39 inout DDR_ck_n;
40 inout DDR_ck_p;
41 inout DDR_cke;
42 inout DDR_cs_n;
43 inout [3:0]DDR_dm;
44 inout [31:0]DDR_dq;
45 inout [3:0]DDR_dqs_n;
46 inout [3:0]DDR_dqs_p;
47 inout DDR_odt;
48 inout DDR_ras_n;
49 inout DDR_reset_n;


아래쪽에 Generate Bitstream 을 눌러서 비트스트림을 생성하도록 한다.
최종 성공하면 아래와 같은 화면이 나타난다.
그리고 앞선 문서들을 참고하여 Export 하고 SDK 를 띄운다.
Bitstream Generation Completed
Bitstream Generation successfully completed.
Next
View Reports
Open Hardware Manager
Don't show this dialog again
OK
Cancel

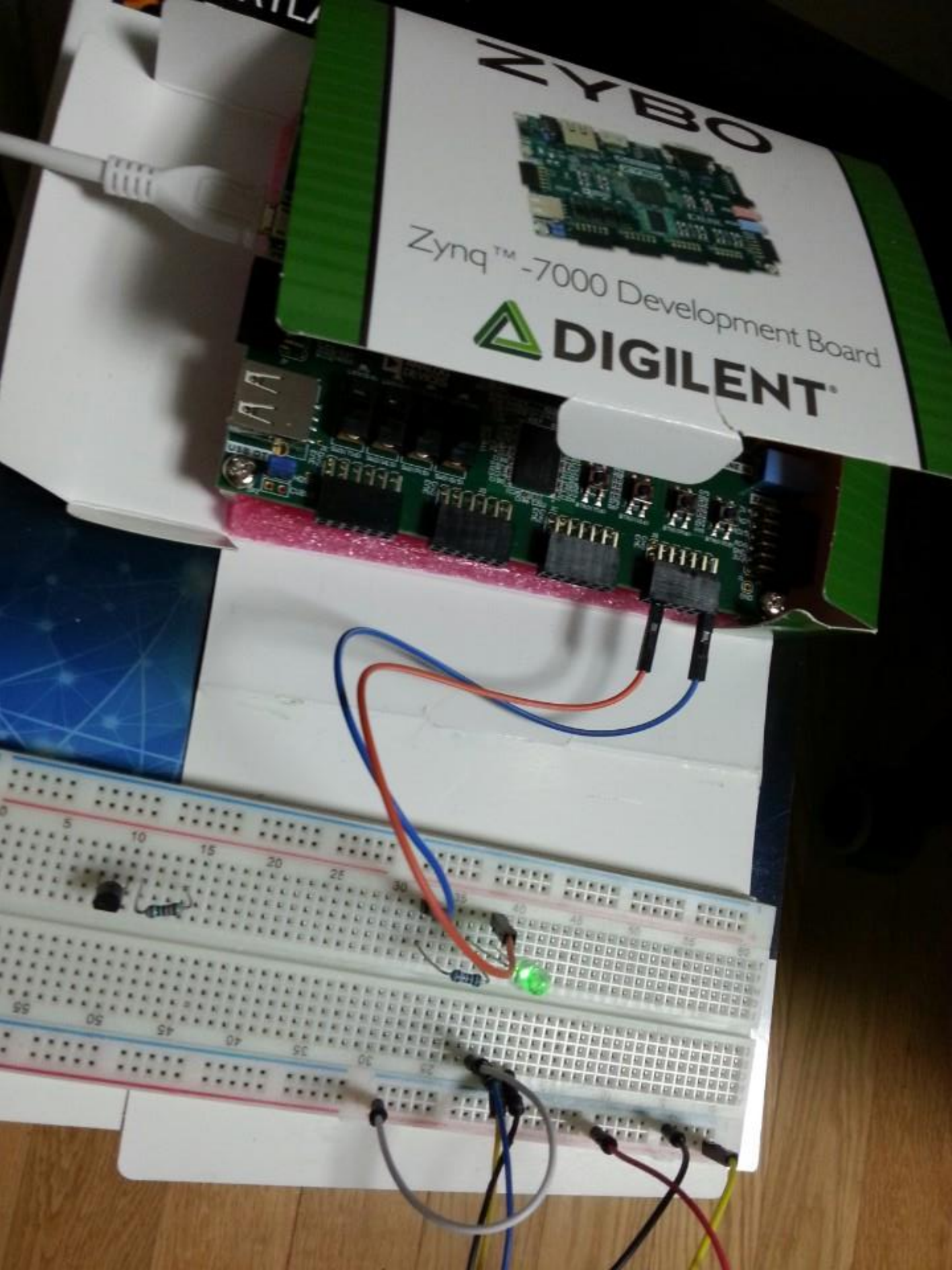

system.hdf
* gpio.c
#include <stdio
#include "xpara
#include "gpio_
#include "xil_i
int main(void)
{
//u32 ip_ba
//u32 ip_ba
xil_printf(
while(1)
{
/*
GPIO_TE
sleep(1
GPIO_TE
sleep(1
*/
/*
Xil_Out
sleep(1
Xil_Out
sleep(1
*/
GPIO_TE
}
return 0;
}
New Project
Application Project
Create a managed make application project.
Project name: led_lab1
Use default location
Location: /home/sdr/test/zynq_fpga/gpio_lab/gpio_lab.sdk/led_lab
Browse...
Choose file system: default
OS Platform: standalone
Target Hardware
Hardware Platform: zynq_system_wrapper_hw_platform_0
New...
Processor: ps7_cortexa9_0
Target Software
Language: C C++
Compiler: 32-bit
Board Support Package: Create New led_lab1_bsp
Use existing
< Back
Next >
Cancel
Finish


New Project
Templates
Create one of the available templates to generate a fully-functioning application project.
Available Templates:
Dhrystone
Empty Application
Hello World
lwIP Echo Server
Memory Tests
OpenAMP echo-test
OpenAMP matrix multiplication Demo
OpenAMP RPC Demo
Peripheral Tests
RSA Authentication App
Zynq DRAM tests
Zynq FSBL
A blank C project.
< Back
Next >
Cancel
Finish


tc_dist_0 0xf8f01000 0xf8f01fff
s7_gpio_0 0xe000a000 0xe000afff
New File
File
Create a new file resource.
Enter or select the parent folder:
led_app/src
led_app
src
led_app_bsp
led_system_wrapper_hw_platform_0
RemoteSystemsTempFiles
File name: main.c
Advanced >>
Cancel
Finish

system.hdf | system.mss | main.c | xparameters.h

```c
#include <stdio.h>
#include <xgpio.h>
#include "xparameters.h"
#include "sleep.h"

int main(void)
{
    XGpio in, out;
    //int sw_data = 0;

    XGpio_Initialize(&in, XPAR_AXI_GPIO_0_DEVICE_ID);
    XGpio_Initialize(&out, XPAR_AXI_GPIO_1_DEVICE_ID);

    XGpio_SetDataDirection(&in, 1, 0xF);

    XGpio_SetDataDirection(&out, 1, 0x0);

    while(1)
    {
        /*
        XGpio_DiscreteWrite(&out, 1, 0xFFFFFFFF);
        sleep(1);
        XGpio_DiscreteWrite(&out, 1, 0x0);
        sleep(1);
        */
        Xil_Out32(0x41210000, 0xFFFFFFFF);
        sleep(1);
        Xil_Out32(0x41210000, 0x0);
        sleep(1);
    }

    return 0;
}
```


ZYBO
Zynq™ -7000 Development Board
DIGILENT