

# I2C Lidar with Zynq

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```
sdr@sdr-Samsung-DeskTop-System: ~
PetaLinux environment set to '/home/sdr/petalinux_zynq/petalinux-v2015.4-final'
INFO: Checking free disk space
INFO: Checking installed tools
INFO: Checking installed development libraries
INFO: Checking network and other services
sdr@sdr-Samsung-DeskTop-System:~$ vivado

***** Vivado v2015.4 (64-bit)
**** SW Build 1412921 on Wed Nov 18 09:44:32 MST 2015
**** IP Build 1412160 on Tue Nov 17 13:47:24 MST 2015
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```



Productivity. Multiplied.



### Quick Start



Create New Project



Open Project



Open Example Project

### Tasks



Manage IP



Open Hardware Manager



Xilinx Tcl Store

### Information Center



Documentation and Tutorials



Quick Take Videos



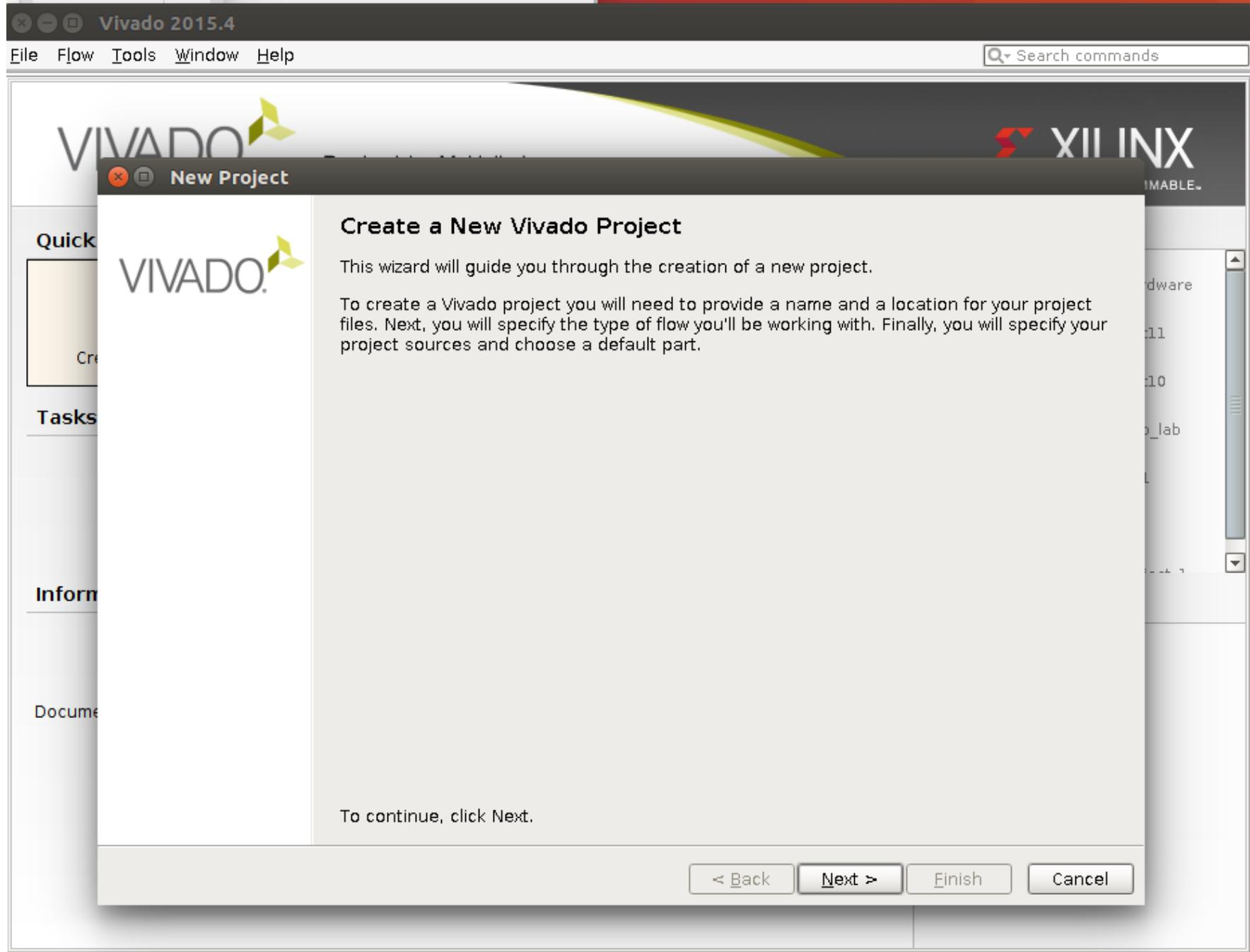
Release Notes Guide

### Recent Projects

- driver\_lab  
/home/sdr/zynq\_zynq\_fpga/lab6/hardware
- test11  
/home/sdr/test/zynq\_fpga/test11
- test10  
/home/sdr/test/zynq\_fpga/test10
- gpio\_lab  
/home/sdr/test/zynq\_fpga/gpio\_lab
- lab1  
/home/sdr/test/zynq\_fpga/lab1
- lab  
/home/sdr/lab
- project\_1  
/home/sdr/test/zynq\_fpga/project\_1

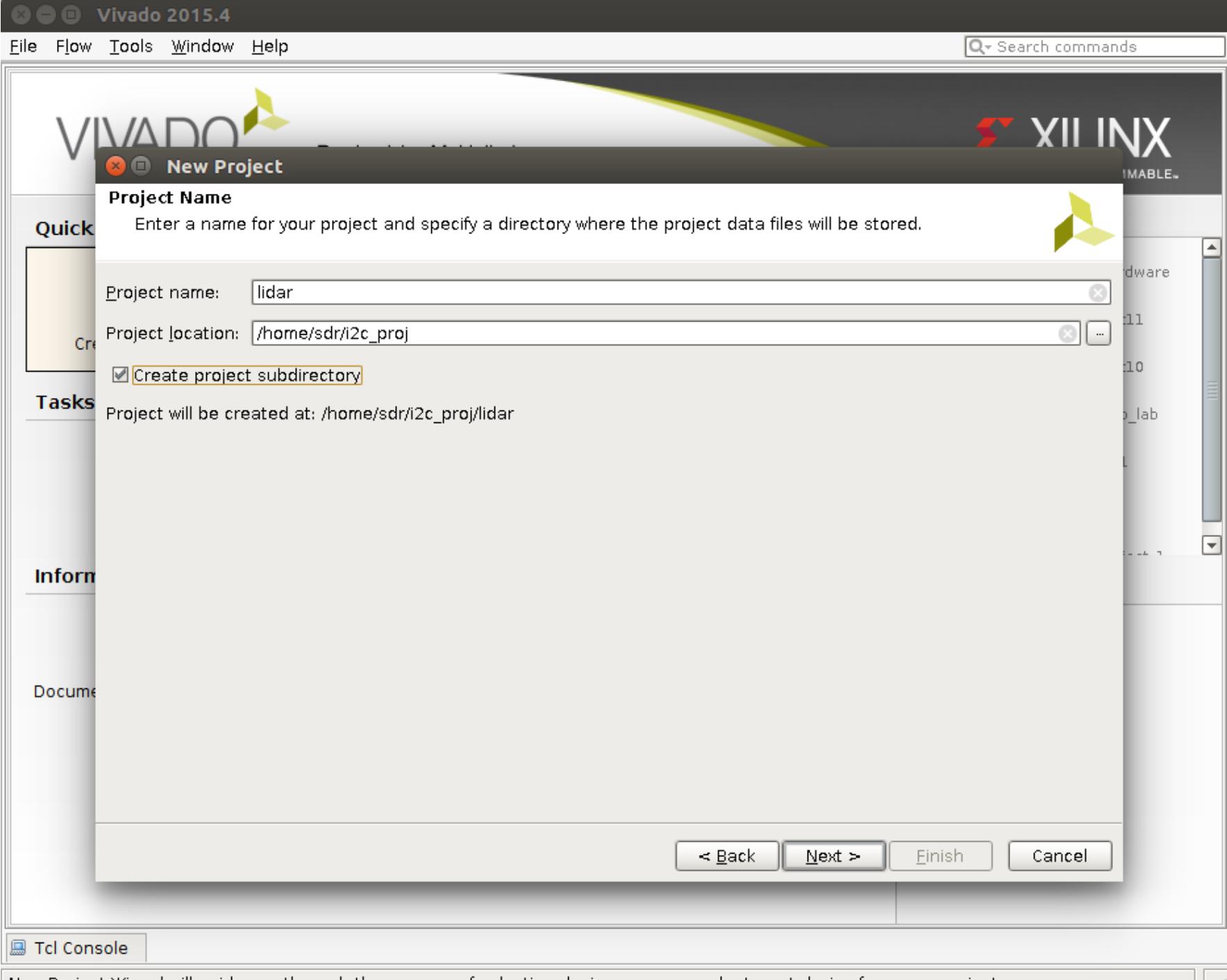
### Recent IP Locations

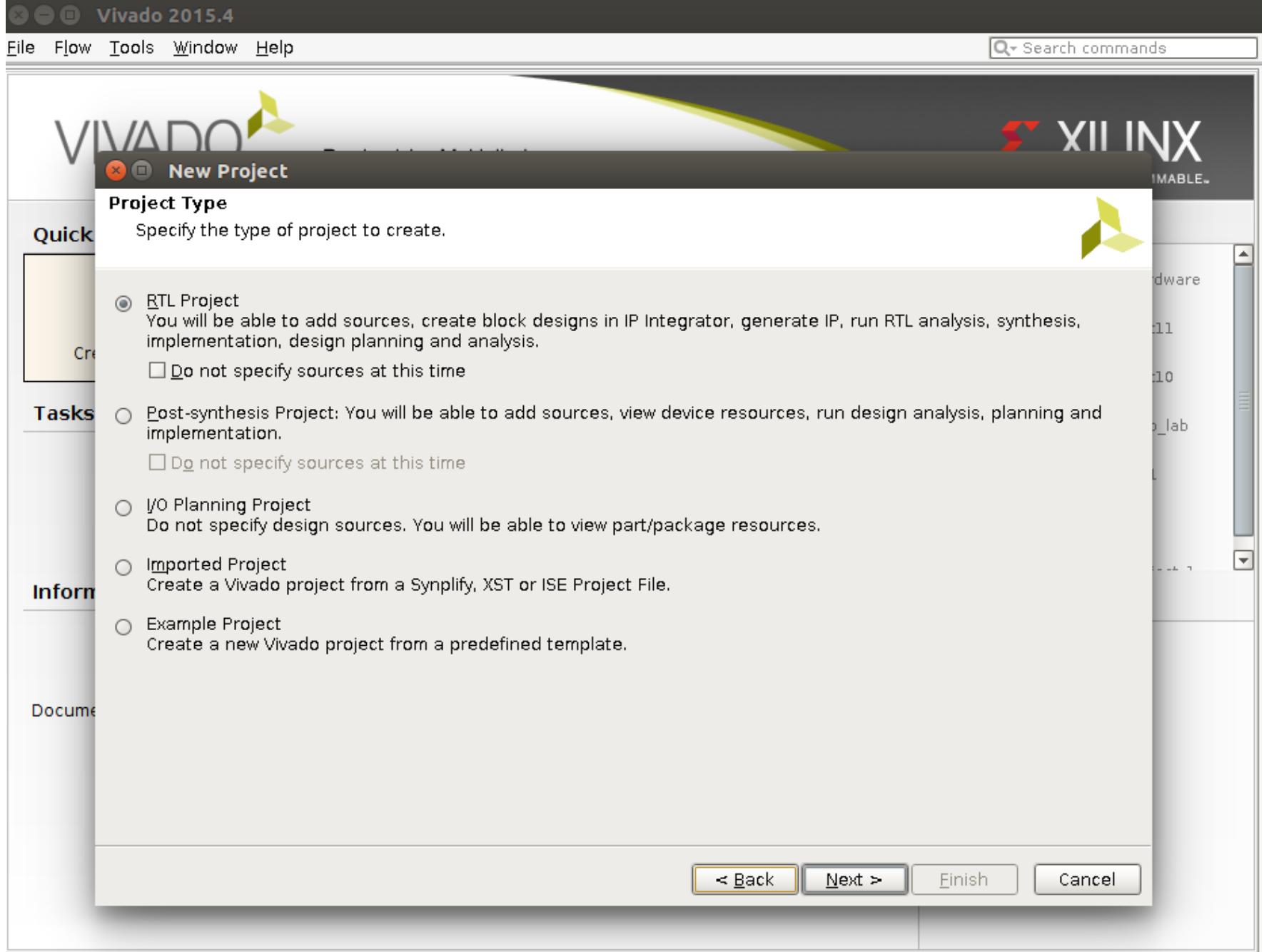
- zynq\_fpga  
/home/sdr/test
- test\_ip  
/home/sdr/test/zynq\_fpga



Tcl Console

New Project Wizard will guide you through the process of selecting design sources and a target device for a new project.





# VIVADO

## New Project

**Project Type**  
Specify the type of project to create.

**RTL Project**  
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.  
 Do not specify sources at this time

**Post-synthesis Project:** You will be able to add sources, view device resources, run design analysis, planning and implementation.  
 Do not specify sources at this time

**I/O Planning Project**  
Do not specify design sources. You will be able to view part/package resources.

**Imported Project**  
Create a Vivado project from a Synplify, XST or ISE Project File.

**Example Project**  
Create a new Vivado project from a predefined template.

**Tasks**

**Information**

**Documentation**

**Search**

< Back **Next >** Finish Cancel

**Vivado 2015.4**

File Flow Tools Window Help  Search commands

# VIVADO

## New Project

**Add Sources**

Specify HDL and netlist files, or directories containing HDL and netlist files, to add to your project. Create a new source file on disk and add it to your project. You can also add and create sources later.

Tasks

Information

Use Add Files, Add Directories or Create File buttons below

Add Files    Add Directories    Create File

Document  Scan and add RTL include files into project  
 Copy sources into project  
 Add sources from subdirectories Make a local copy of these files into your project directory

Target language:  Simulator language:

< Back  Finish Cancel

Tcl Console

New Project Wizard will guide you through the process of selecting design sources and a target device for a new project.



New Project

XILINX  
IMABLE

## Add Existing IP (optional)

Specify existing configurable IP, DSP composite, and Embedded sub-design files to add to your project.



Use Add Files or Add Directories buttons below

Add Files

Add Directories

 Copy sources into project

&lt; Back

Next &gt;

Finish

Cancel



New Project

XILINX  
IMABLE.

## Add Constraints (optional)

Specify or create constraint files for physical and timing constraints.



## Tasks

Use Add Files or Create File buttons below

Add Files

Create File

 Copy constraints files into project

&lt; Back

Next &gt;

Finish

Cancel

Vivado 2015.4

File Flow Tools Window Help Search commands

## New Project

### Default Part

Choose a default Xilinx part or board for your project. This can be changed later.

Select:  Parts  Boards

Filter

Vendor: All

Display Name: All

Board Rev: Latest

Reset All Filters

Search:

Display Name	Vendor	Board Rev	Part	I/O Pin Count	File Ve
Zybo	diligentinc.com	B.3	xc7z010clg400-1	400	1.0
ZedBoard Zynq Evaluation and Development Kit	ern.avnet.com	d	xc7z020clg484-1	484	1.3
Artix-7 AC701 Evaluation Platform	xilinx.com	1.1	xc7a200tfgb676-2	676	1.2
ZYNQ-7 ZC702 Evaluation Board	xilinx.com	1.0	xc7z020clg484-1	484	1.2

< Back  Finish Cancel

Tcl Console

New Project Wizard will guide you through the process of selecting design sources and a target device for a new project.



New Project

Quick



Create

Tasks

Information

Documentation



## New Project Summary

i A new RTL project named 'lidar' will be created.

! No source files or directories will be added. Use Add Sources to add them later.

! No Configurable IP files will be added. Use Add Sources to add them later.

! No constraints files will be added. Use Add Sources to add them later.

i The default part and product family for the new project:

Default Board: Zynq-7000  
Default Part: xc7z010clg400-1  
Product: Zynq-7000  
Family: Zynq-7000  
Package: clg400  
Speed Grade: -1

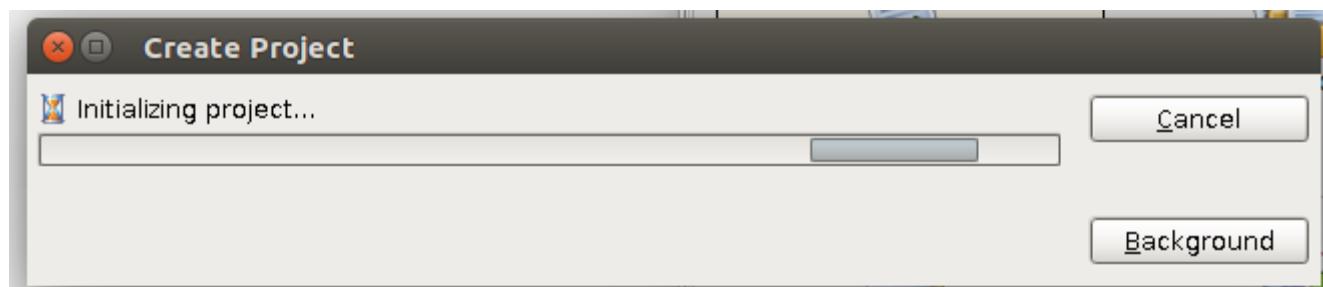
To create the project, click Finish

&lt; Back

Next &gt;

Finish

Cancel



Flow Navigator <>

**Project Manager**

- Project Settings
- Add Sources
- Language Templates
- IP Catalog

**IP Integrator**

- Create Block Design
- Open Block Design
- Generate Block Design

**Simulation**

- Simulation Settings
- Run Simulation

**RTL Analysis**

- Elaboration Settings
- Open Elaborated Design

**Synthesis**

- Synthesis Settings
- Run Synthesis
- Open Synthesized Design

**Implementation**

- Implementation Settings
- Run Implementation
- Open Implemented Design

**Program and Debug**

**Project Manager - lidar**

## Sources

- Design Sources
- Constraints
- Simulation Sources
  - sim\_1

**Hierarchy**

## Libraries | Compile Order

- Sources
- Templates

## Properties



Select an object to see properties

## Design Runs



## Name

## Constraints

## Status

## WNS

## TNS

## WHS

## THS

synth_1	constrs_1	Not started					
impl_1	constrs_1	Not started					

**Project Summary**

o:part0:1.0  
015.4/data/boards/board\_files  
[nc.com](#)

**Implementation**

Status: Not s  
Messages: No e  
Part: xc7z0  
Strategy: Vivad  
Incremental compile: [None](#)

lidar - [/home/sdr/i2c\_proj/lidar/lidar.xpr] - Vivado 2015.4

File Edit Flow Tools Window Layout View Help

Search commands

Ready

Flow Navigator

Project Manager - lidar

Sources

Design Sources

Constraints

Simulation Sources

sim\_1

Project Summary

o:part0:1.0  
115.4/data/boards/board\_files  
com

Create Block Design

Please specify name of block design.

Design name: i2c\_system

Directory: <Local to Project>

Specify source set: Design Sources

Implementation

Status: Not started

Messages: None

Part: xc7z020clg484-1

Strategy: Vivado

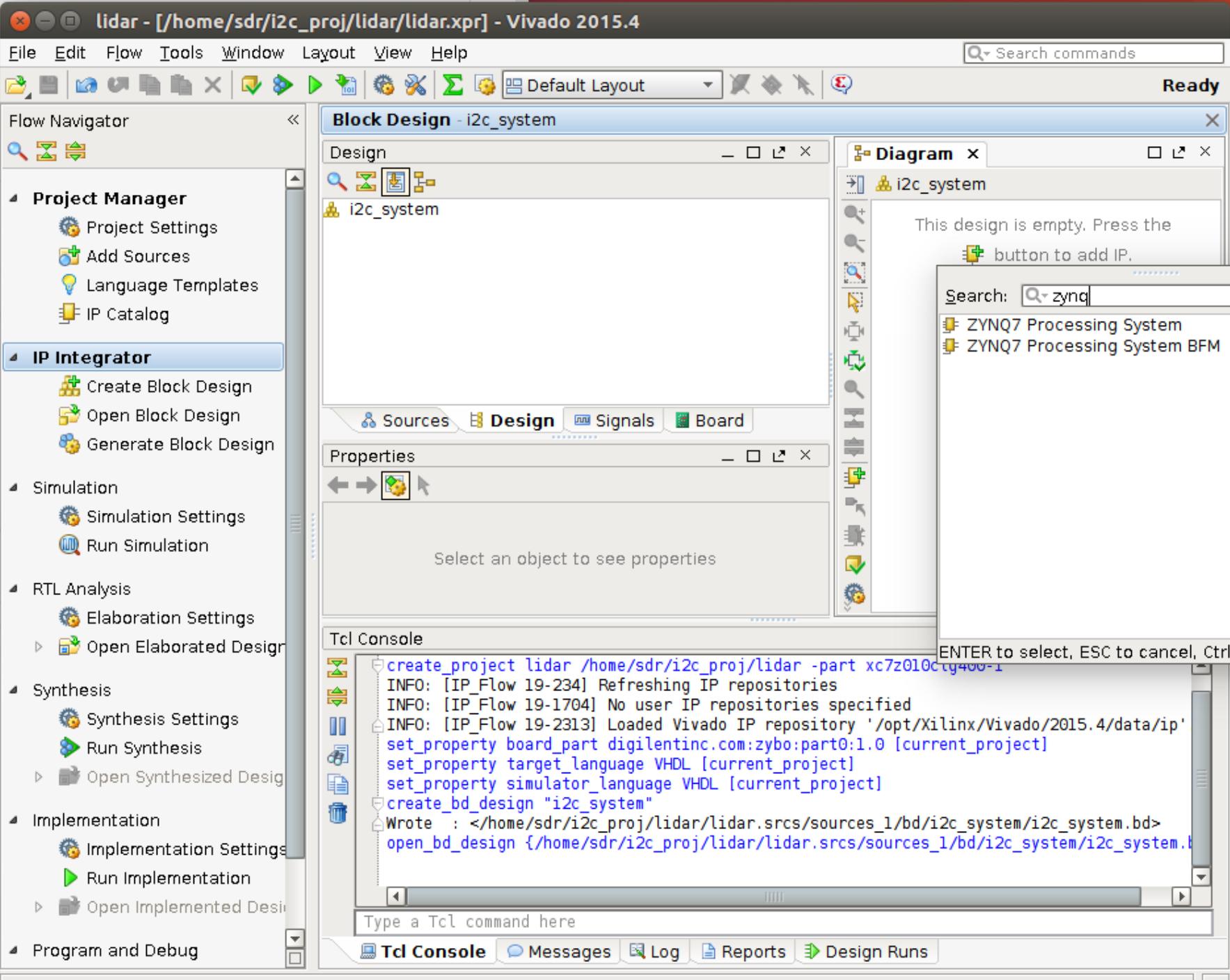
Incremental compile: None

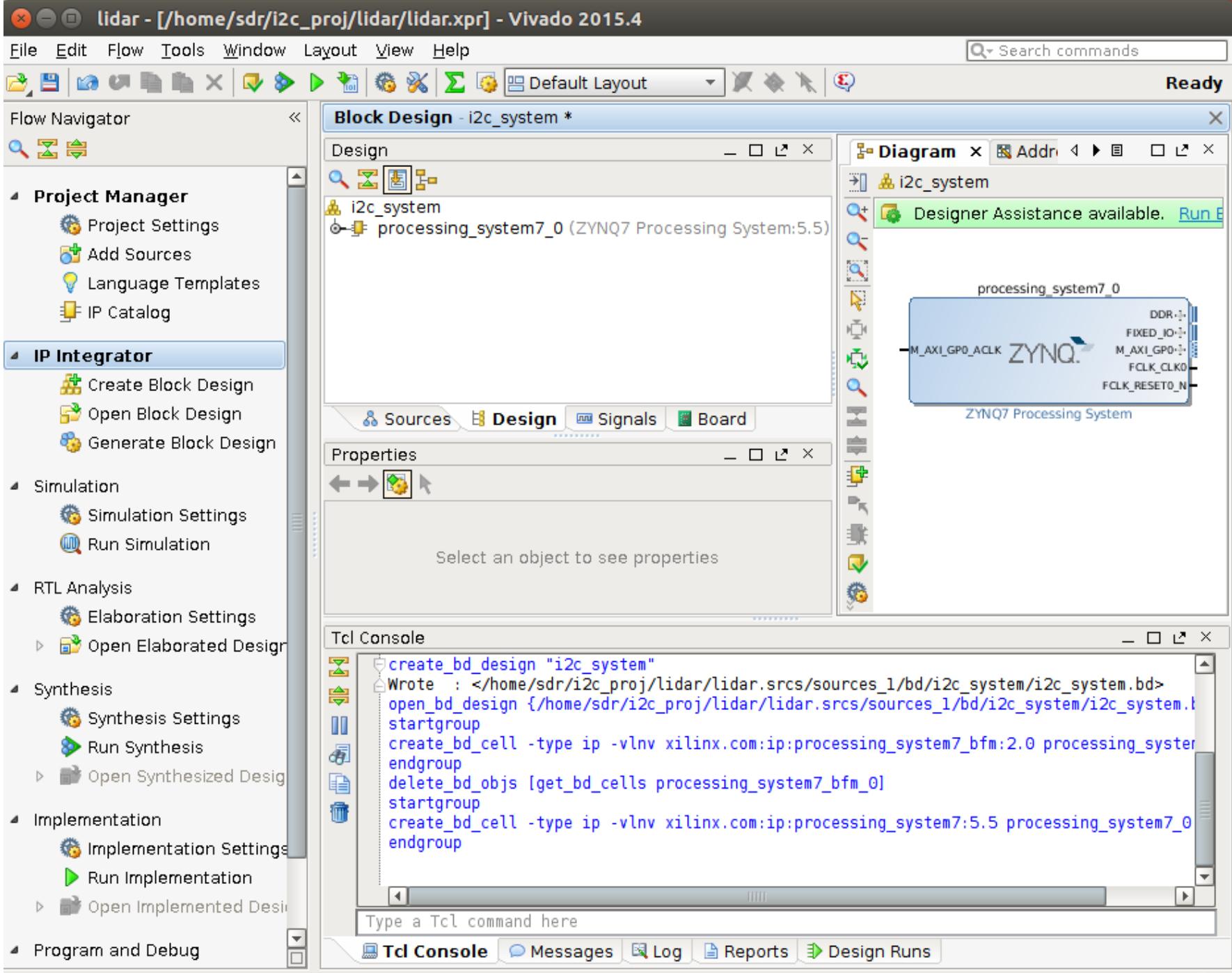
OK Cancel

TNS TNS WHS THS

Tcl Console Messages Log Reports Design Runs

Create and add an IP subsystem to the project





File Edit Flow Tools Window Layout View Help Search commands

Ready

Flow Navigator

Project Manager

- Project Settings
- Add Sources
- Language Templates
- IP Catalog

IP Integrator

- Create Block Design
- Open Block Design
- Generate Block Design

Simulation

- Simulation Settings
- Run Simulation

RTL Analysis

- Elaboration Settings
- Open Elaborated Design

Synthesis

- Synthesis Settings
- Run Synthesis
- Open Synthesized Design

Implementation

- Implementation Settings
- Run Implementation
- Open Implemented Design

Program and Debug

Block: processing\_system7\_0

Block Design i2c\_system \*

Diagram Address Editor

i2c\_system processing\_system7\_0 (ZYNQ7 Processing System-5.5)

Run Block Automation

Automatically make connections in your design by checking the boxes of the blocks to connect. Select a block on the left to display its configuration options on the right.

All Automation (1 out of 1 selected)  processing\_system7\_0

Description

This option sets the board preset on the Processing System. All current properties will be overwritten by the board preset. This action is NOT undoable. Zynq7 block automation applies current board preset and generates external connections for FIXED\_IO, Trigger and DDR interfaces.

NOTE: Apply Board Preset will discard existing IP configuration - please uncheck this box, if you wish to retain previous configuration.

Instance: /processing\_system7\_0

Options

Make Interface External: FIXED\_IO, DDR

Apply Board Preset:

Cross Trigger In:

Cross Trigger Out:

OK Cancel

Block Design - i2c\_system \*

Design Diagram Address Editor

i2c\_system

External Interfaces

Interface Connections

processing\_system7\_0 (ZYNQ7 Processing System:5.5)

Sources Design Signals Board

Block Properties

processing\_system7\_0

Name: processing system7 0

General Properties IP

Tcl Console

```
Wrote : </home/sdr/i2c_proj/lidar/lidar.srcs/sources_1/bd/i2c_system/i2c_system.bd>
open_bd_design {/home/sdr/i2c_proj/lidar/lidar.srcs/sources_1/bd/i2c_system/i2c_system.bd}
startgroup
create_bd_cell -type ip -vlnv xilinx.com:ip:processing_system7_bfm:2.0 processing_system7_bfm_0
endgroup
delete_bd_objs [get_bd_cells processing_system7_bfm_0]
startgroup
create_bd_cell -type ip -vlnv xilinx.com:ip:processing_system7:5.5 processing_system7_0
endgroup
apply_bd_automation -rule xilinx.com:bd_rule:processing_system7 -config {make_external "FIXED_IO, DDR" apply_board_preset "1" Master}
```

Type a Tcl command here

Tcl Console Messages Log Reports Design Runs

The diagram shows the ZYNQ7 Processing System block with its various pins and connections. The block is labeled 'processing\_system7\_0' and 'ZYNQ'. External pins include DDR+, FIXED\_IO+, SDIO\_0+, USBIND\_0+, M\_AXI\_GP0+, M\_AXI\_GP0\_ACLK, TTC0\_WAVE0\_OUT, TTC0\_WAVE1\_OUT, TTC0\_WAVE2\_OUT, FCLK\_CLK0, and FCLK\_RESET0\_N.



## ZYNQ7 Processing System (5.5)

[Documentation](#) [Presets](#) [IP Location](#) [Import XPS Settings](#)

Page Navigator &lt;&gt;

## Zynq Block Design

[Summary Report](#)

Zynq Block Design

PS-PL Configuration

Peripheral I/O Pins

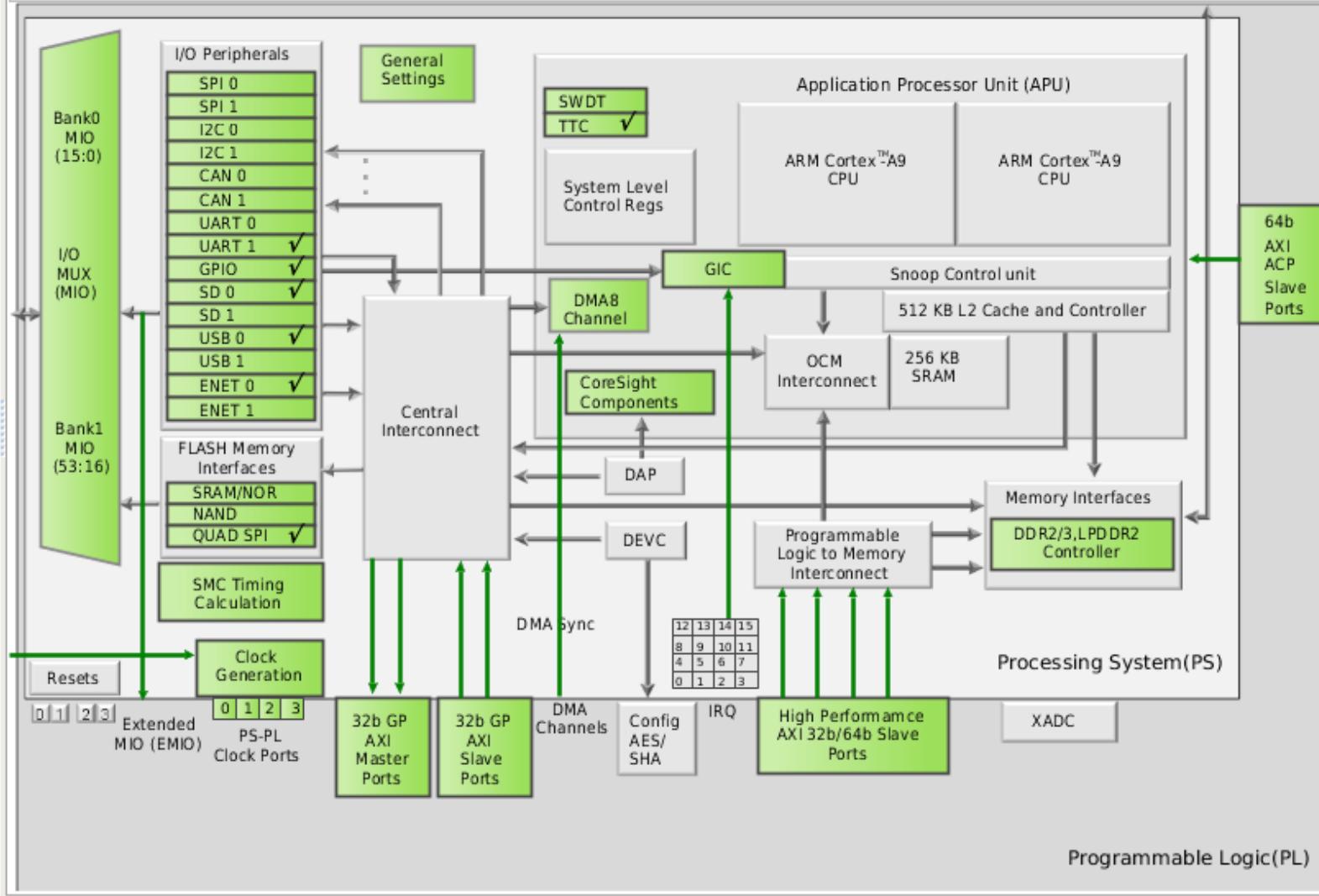
MIO Configuration

Clock Configuration

DDR Configuration

SMC Timing Calculation

Interrupts



OK

Cancel

File Layout View Help

Re-customize IP

ZYNQ7 Processing System (5.5)

Documentation Presets IP Location Import XPS Settings

Page Navigator <>

Zynq Block Design

PS-PL Configuration

Peripheral I/O Pins

MIO Configuration

Clock Configuration

DDR Configuration

SMC Timing Calculation

Interrupts

**MIO Configuration**

Bank 0 I/O Voltage: LVCMS 3.3V

Bank 1 I/O Voltage: LVCMS 1.8V

Search:

Peripheral IO Signal IO Type Speed Pullup Direction

- Memory Interfaces
- I/O Peripherals
- Application Processor Unit
- Programmable Logic Test and Debug

OK Cancel

The screenshot shows the 'MIO Configuration' window of the ZYNQ7 Processing System (5.5) software. The window title is 'MIO Configuration'. At the top, there are dropdown menus for 'Bank 0 I/O Voltage' set to 'LVCMS 3.3V' and 'Bank 1 I/O Voltage' set to 'LVCMS 1.8V'. Below these are search and filter icons. A table header row includes columns for 'Peripheral', 'IO', 'Signal', 'IO Type', 'Speed', 'Pullup', and 'Direction'. Under the 'Peripheral' column, four categories are listed: 'Memory Interfaces', 'I/O Peripherals', 'Application Processor Unit', and 'Programmable Logic Test and Debug'. On the left side of the window, a 'Page Navigator' sidebar lists various configuration tabs, with 'MIO Configuration' currently selected. The top menu bar includes 'File', 'Layout', 'View', 'Help', 'Documentation', 'Presets', 'IP Location', and 'Import XPS Settings'. The bottom right corner features 'OK' and 'Cancel' buttons.



## ZYNQ7 Processing System (5.5)

[Documentation](#) [Presets](#) [IP Location](#) [Import XPS Settings](#)

Page Navigator &lt;&gt;

Zynq Block Design

PS-PL Configuration

Peripheral I/O Pins

MIO Configuration

Clock Configuration

DDR Configuration

SMC Timing Calculation

Interrupts

## MIO Configuration

[Summary Report](#)Bank 0 I/O Voltage [LVC MOS 3.3V](#)Bank 1 I/O Voltage [LVC MOS 1.8V](#)

Search:



Peripheral	IO	Signal	IO Type	Speed	Pullup	Directive
------------	----	--------	---------	-------	--------	-----------

Memory Interfaces						
-------------------	--	--	--	--	--	--

I/O Peripherals						
-----------------	--	--	--	--	--	--

ENET 0	<a href="#">MIO 16 .. 27</a>					
--------	------------------------------	--	--	--	--	--

ENET 1						
--------	--	--	--	--	--	--

USB 0	<a href="#">MIO 28 .. 39</a>					
-------	------------------------------	--	--	--	--	--

USB 1						
-------	--	--	--	--	--	--

SD 0	<a href="#">MIO 40 .. 45</a>					
------	------------------------------	--	--	--	--	--

SD 1						
------	--	--	--	--	--	--

UART 0						
--------	--	--	--	--	--	--

UART 1	<a href="#">MIO 48 .. 49</a>					
--------	------------------------------	--	--	--	--	--

I2C 0						
-------	--	--	--	--	--	--

I2C 1						
-------	--	--	--	--	--	--

SPI 0						
-------	--	--	--	--	--	--

SPI 1						
-------	--	--	--	--	--	--

CAN 0						
-------	--	--	--	--	--	--

CAN 1						
-------	--	--	--	--	--	--

GPIO						
------	--	--	--	--	--	--

Application Processor Unit						
----------------------------	--	--	--	--	--	--

Programmable Logic Test and Debug						
-----------------------------------	--	--	--	--	--	--

OK

Cancel



## ZYNQ7 Processing System (5.5)

[Documentation](#) [Presets](#) [IP Location](#) [Import XPS Settings](#)

Page Navigator &lt;&lt;

Zynq Block Design

PS-PL Configuration

Peripheral I/O Pins

MIO Configuration

Clock Configuration

DDR Configuration

SMC Timing Calculation

Interrupts

## MIO Configuration

[Summary Report](#)Bank 0 I/O Voltage [LVCMOS 3.3V](#)Bank 1 I/O Voltage [LVCMOS 1.8V](#)

Search:

Peripheral	IO	Signal	IO Type	Speed	Pullup	Directive
Memory Interfaces						
I/O Peripherals						
<input checked="" type="checkbox"/> ENET 0	MIO 16 .. 27					
<input type="checkbox"/> ENET 1						
<input checked="" type="checkbox"/> USB 0	MIO 28 .. 39					
<input type="checkbox"/> USB 1						
<input checked="" type="checkbox"/> SD 0	MIO 40 .. 45					
<input type="checkbox"/> SD 1						
<input type="checkbox"/> UART 0						
<input checked="" type="checkbox"/> UART 1	MIO 48 .. 49					
<input checked="" type="checkbox"/> I2C 0	EMIO					
<input type="checkbox"/> I2C 1						
<input type="checkbox"/> SPI 0						
<input type="checkbox"/> SPI 1						
<input type="checkbox"/> CAN 0						
<input type="checkbox"/> CAN 1						
<input type="checkbox"/> GPIO						
Application Processor Unit						
Programmable Logic Test and Debug						



OK

Cancel

Default Layout

Block Design - i2c\_system \*

Design

i2c\_system

- External Interfaces
- Interface Connections
- processing\_system7\_0 (ZYNQ7 Processing System:5.5)
  - DDR
  - FIXED\_IO
  - IIC\_0
  - M\_AXI\_GPO
  - SDIO\_0
  - USBIND\_0

Sources Design Signals Board

Block Interface Properties

Name: IIC\_0

General Properties

Tcl Console

```

create_bd_cell -type ip -vlnv xilinx.com:ip:processing_system7:5.5 processing_system7_0
endgroup
apply_bd_automation -rule xilinx.com:bd_rule:processing_system7 -config {make_external "FIXED_IO, DDR" apply_board_preset "1" Master
startgroup
set_property -dict [list CONFIG.POW_QSPI_GRP_SINGLE_SS_ENABLE {1} CONFIG.POW_I2C0_PERIPHERAL_ENABLE {1}] [get_bd_cells processing_sy
endgroup
startgroup
create_bd_intf_port -mode Master -vlnv xilinx.com:interface:iic_rtl:1.0 IIC_0
connect_bd_intf_net [get_bd_intf_pins processing_system7_0/IIC_0] [get_bd_intf_ports IIC_0]
endgroup

```

Type a Tcl command here

Tcl Console Messages Log Reports Design Runs

Diagram x Address Editor x

i2c\_system

processing\_system7\_0

ZYNQ

ZYNQ7 Processing System

**Block Design - i2c\_system \***

Sources    Diagram    Address Editor

Design Sources (1)  
 Constraints  
 Simulation Sources (1)  
 sim\_1 (1)

Hierarchy IP Sources Libraries Compile Order

Sources Design Signals Board

System Net Properties

+ processing\_system7\_0\_FCLK\_CLK0

Name: processing system7\_0 FCLK CLK0

General Properties Pins

Tcl Console

```
apply_bd_automation -rule xilinx.com:bd_rule:processing_system7 -config {make_external "FIXED_IO, DDR" apply_board_preset "1" Master startgroup set_property -dict [list CONFIG.PCW_QSPI_GRP_SINGLE_SS_ENABLE {1} CONFIG.PCW_I2C0_PERIPHERAL_ENABLE {1}] [get_bd_cells processing_system7_0] endgroup startgroup create_bd_intf_port -mode Master -vlnv xilinx.com:interface:iic_rtl:1.0 IIC_0 connect_bd_intf_net [get_bd_intf_pins processing_system7_0/IIC_0] [get_bd_intf_ports IIC_0] endgroup connect_bd_net [get_bd_pins processing_system7_0/FCLK_CLK0] [get_bd_pins processing_system7_0/M_AXI_GP0_ACLK] open_bd_design {/home/sdr/i2c_proj/lidar/lidar.srcc/sources_1/bd/i2c_system/i2c_system.bd}
```

Type a Tcl command here

Tcl Console Messages Log Reports Design Runs

Default Layout



Ready

Design - i2c\_system \*

Diagram Address Editor

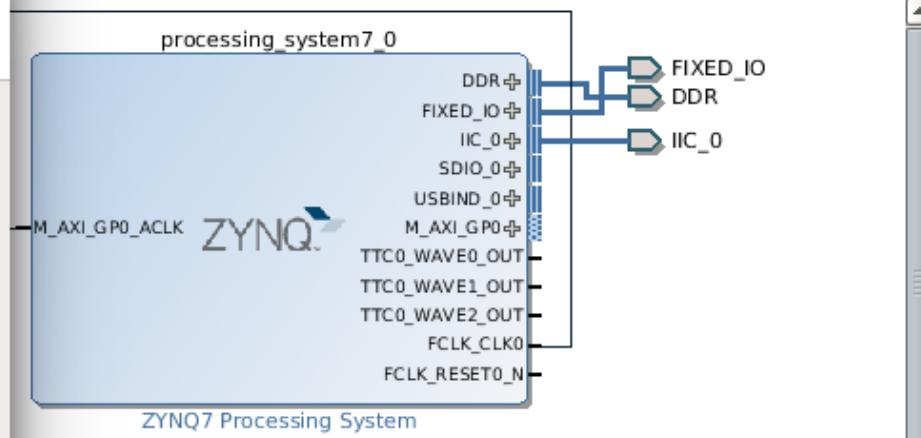
## Generate Output Products

The following output products will be generated.



## Preview

- i2c\_system.bd (Global)
  - Synthesis
  - Implementation
  - Simulation



## Synthesis Options



- Global
- Out of context per IP
- Out of context per Block Design

## Run Settings

- On local host: Number of jobs: 1
- On remote hosts
- Use LSF:

Apply

Generate

Cancel

a Tcl command here

```
config {make_external "FIXED_IO, DDR" apply_board_preset "1" Master
CONFIG.POW_I2C0_PERIPHERAL_ENABLE {1}} [get_bd_cells processing_system7_0]
l:1.0 IIC_0
[get_bd_intf_ports IIC_0]
d_pins processing_system7_0/M_AXI_GPO_ACLK
2c_system/i2c_system.bd}
```

**Block Design - i2c\_system \***

Sources

- Waiting to Update Source File Hierarchy...
- Design Sources (1)
  - i2c\_system (i2c\_system.bd) (1)
- Constraints
- Simulation Sources (1)
  - sim\_1 (1)

Hierarchy IP Sources Libraries Compile Order

Sources Design Signals Board

Source File Properties

**Diagram** x Address Editor x

i2c\_system

processing\_system7\_0

ZYNQ Processing System

Pins (from left to right):  
 DDR+, FIXED\_IO+, IIC\_0+, SDIO\_0+, USBIND\_0+, M\_AXI\_GP0+, TTC0\_WAVE0\_OUT, TTC0\_WAVE1\_OUT, TTC0\_WAVE2\_OUT, FCLK\_CLK0, FCLK\_RESET0\_N

**Managing Output Products**

Generating output products...

Cancel

Background

```

set_property -dict {list CONFIG.POW_QSPI_SNR_SINGLE_SS_ENABLE {1} CONFIG.POW_I2C0_PDNnRnRnRAL_ENABLE {1}} [get_bd_cells processing_system7_0]
endgroup
startgroup
create_bd_intf_port -mode Master -vlnv xilinx.com:interface:iic_rtl:1.0 IIC_0
connect_bd_intf_net [get_bd_intf_pins processing_system7_0/IIC_0] [get_bd_intf_ports IIC_0]
endgroup
connect_bd_net [get_bd_pins processing_system7_0/FCLK_CLK0] [get_bd_pins processing_system7_0/M_AXI_GP0_ACLK]
open_bd_design {/home/sdr/i2c_proj/lidar/lidar.srcts/sources_1/bd/i2c_system/i2c_system.bd}
set_property synth_checkpoint_mode Hierarchical [get_files /home/sdr/i2c_proj/lidar/lidar.srcts/sources_1/bd/i2c_system/i2c_system.bd]
generate_target all [get_files /home/sdr/i2c_proj/lidar/lidar.srcts/sources_1/bd/i2c_system/i2c_system.bd]
  
```

Type a Tcl command here

Tcl Console Messages Log Reports Design Runs

Default Layout

## Design - i2c\_system

Running i2c\_system\_processing\_system7\_0\_0\_synth\_1

Cancel

Design Sources (1)

- i2c\_system (i2c\_system.bd) (1)
- Constraints
- Simulation Sources (1)
- sim\_1 (1)

Hierarchy IP Sources Libraries Compile Order

Sources Design Signals Board

## Generate Output Products



Out-of-context module run was launched for generating output products.

OK

```

Exporting to file /home/sdr/i2c_proj/lidar/lidar.srcs/sources_1/bd/i2c_system/hw_handoff/i2c_system.hwh
Generated Block Design Tcl file /home/sdr/i2c_proj/lidar/lidar.srcs/sources_1/bd/i2c_system/hw_handoff/i2c_system_bd.tcl
Generated Hardware Definition File /home/sdr/i2c_proj/lidar/lidar.srcs/sources_1/bd/i2c_system/hdl/i2c_system.hwdef
generate_target: Time (s): cpu = 00:00:17 ; elapsed = 00:00:15 . Memory (MB): peak = 6020.395 ; gain = 42.008 ; free physical = 514
export_ip_user_files -of_objects [get_files /home/sdr/i2c_proj/lidar/lidar.srcs/sources_1/bd/i2c_system/i2c_system.bd] -no_script -f
create_ip_run [get_files -of_objects [get_fileset sources_1]] /home/sdr/i2c_proj/lidar/lidar.srcs/sources_1/bd/i2c_system/i2c_system.
launch_run i2c_system_processing_system7_0_0_synth_1
[Sun May 13 23:30:27 2018] Launched i2c_system_processing_system7_0_0_synth_1...
Run output will be captured here: /home/sdr/i2c_proj/lidar/runs/i2c_system_processing_system7_0_0_synth_1/runme.log
export_simulation -of_objects [get_files /home/sdr/i2c_proj/lidar/lidar.srcs/sources_1/bd/i2c_system/i2c_system.bd] -directory /home

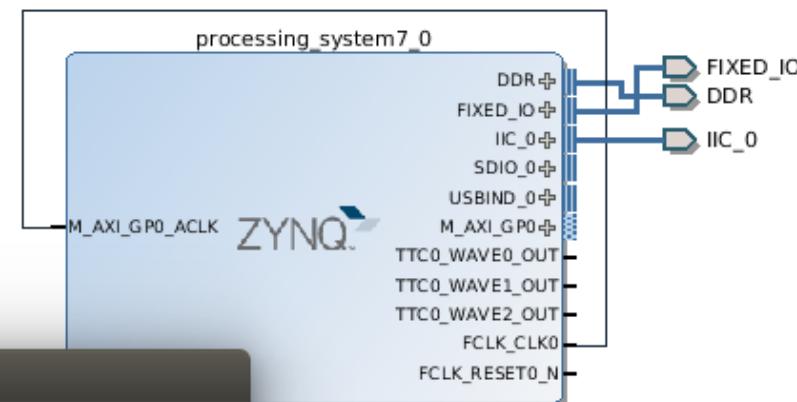
```

Type a Tcl command here

Tcl Console Messages Log Reports Design Runs

## Diagram x Address Editor x

## i2c\_system



Processing System

**Design - i2c\_system**

Sources

- Design Sources (1)
  - i2c\_system (i2c\_system.bd) (1)
- Constraints
- Simulation Sources (1)
  - sim\_1 (1)

**Diagram** x Address Editor x

i2c\_system

processing\_system7\_0

ZYNQ  
Q7 Processing System

DDR+  
FIXED\_IO+  
IIC\_0+  
SDIO\_0+  
USBIND\_0+  
M\_AXI\_GPO+  
TTC0\_WAVE0\_OUT  
TTC0\_WAVE1\_OUT  
TTC0\_WAVE2\_OUT  
FCLK\_CLK0  
FCLK\_RESET0\_N

**Create HDL Wrapper**

You can either add or copy the HDL wrapper file to the project. Use copy option if you would like to modify this file.

Options

Copy generated wrapper to allow user edits

Let Vivado manage wrapper and auto-update

OK Cancel

```

w_handoff/i2c_system.hwh
d/i2c_system/hw_handoff/i2c_system_bd.tcl
l/bd/i2c_system/hdl/i2c_system.hwdef

generate_target: Time (s): cpu = 00:00:17 ; elapsed = 00:00:15 . Memory (MB): peak = 6020.395 ; gain = 42.008 ; free physical = 514
export_ip_user_files -of_objects [get_files /home/sdr/i2c_proj/lidar/lidar.srcs/sources_1/bd/i2c_system/i2c_system.bd] -no_script -f
create_ip_run [get_files -of_objects [get_fileset sources_1] /home/sdr/i2c_proj/lidar/lidar.srcs/sources_1/bd/i2c_system/i2c_system.
launch_run i2c_system_processing_system7_0_0_synth_1
[Sun May 13 23:30:27 2018] Launched i2c_system_processing_system7_0_0_synth_1...
Run output will be captured here: /home/sdr/i2c_proj/lidar/lidar.runs/i2c_system_processing_system7_0_0_synth_1/runme.log
export_simulation -of_objects [get_files /home/sdr/i2c_proj/lidar/lidar.srcs/sources_1/bd/i2c_system/i2c_system.bd] -directory /home

```

Type a Tcl command here

Tcl Console Messages Log Reports Design Runs

Default Layout

Design - i2c\_system

Design Sources (1)

i2c\_system\_wrapper - STRUCTURE (i2c\_system)

Constraints

Simulation Sources (1)

sim\_1 (1)

**Synthesis Completed**

Synthesis successfully completed.

Next

- Run Implementation
- Open Synthesized Design
- View Reports

 Don't show this dialog again

OK

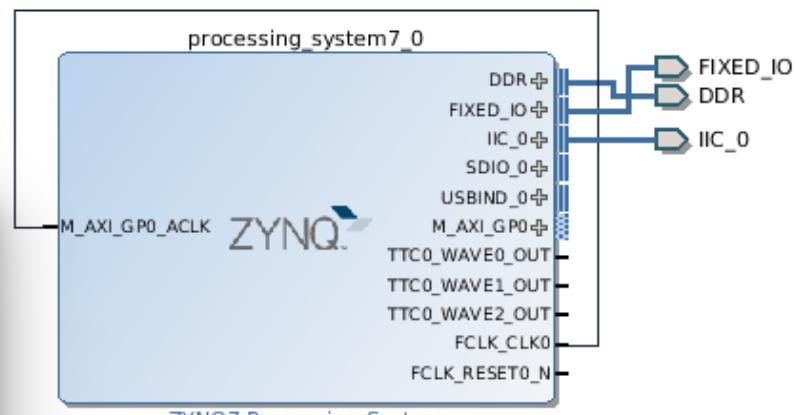
Cancel

```
[Sun May 13 23:30:00 2018] Run output will be captured here: /home/sdr/i2c_proj/lidar.runs/synth_1/runme.log
[Sun May 13 23:30:00 2018] Launched synth_1...
[Sun May 13 23:32:24 2018] Launched synth_1...
[Sun May 13 23:32:24 2018] Launched synth_1...
```



Diagram x Address Editor x

i2c\_system



Sources

File Properties

system.bd

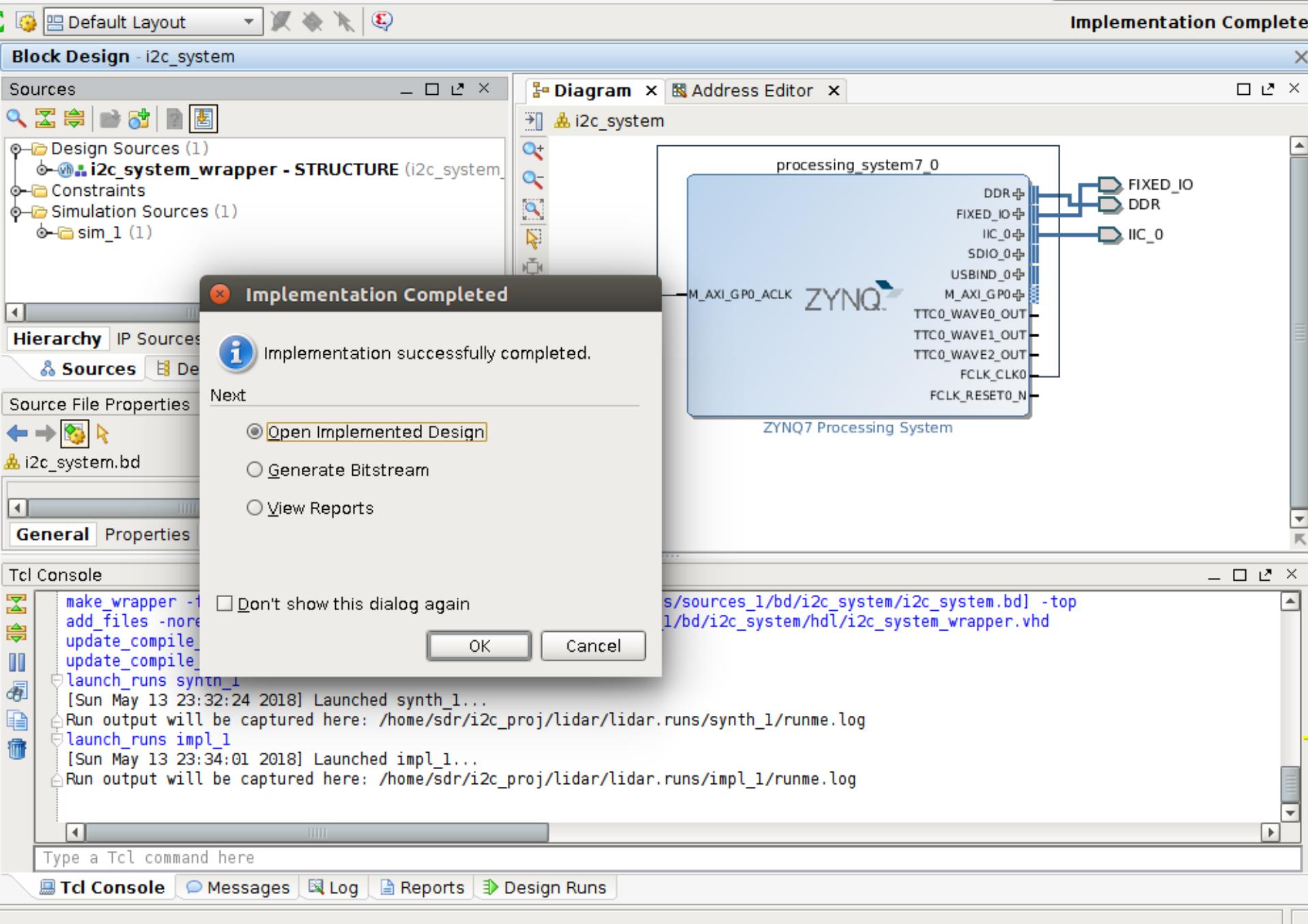
Properties

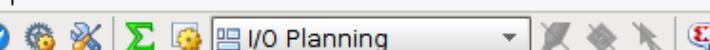
Console

```
[Sun May 13 23:30:00 2018] Run output will be captured here: /home/sdr/i2c_proj/lidar.runs/synth_1/runme.log
[Sun May 13 23:30:00 2018] Launched synth_1...
[Sun May 13 23:32:24 2018] Launched synth_1...
[Sun May 13 23:32:24 2018] Launched synth_1...
```

```
[Sun May 13 23:30:00 2018] Run output will be captured here: /home/sdr/i2c_proj/lidar.runs/synth_1/runme.log
[Sun May 13 23:30:00 2018] Launched synth_1...
[Sun May 13 23:32:24 2018] Launched synth_1...
[Sun May 13 23:32:24 2018] Launched synth_1...
```

Type a Tcl command here





Implementation Complete

## Implemented Design - impl\_1 | xc7z010clg400-1 (active)

## Device Constraints



## Internal VREF

- 0.6V
- 0.675V
- 0.75V
- 0.9V
- NONE (2)
  - I/O Bank 34

Drop I/O banks on voltages or the "NONE" folder to set/unset Internal VREF.

[Sources](#) [Netlist](#) [Device Constraints](#)

## Properties



Select an object to see properties

## Properties

## Clock Regions

## Timing - Timing Summary - impl\_1

This is a [saved report](#)

- General Information
- Timer Settings
- Design Timing Summary**
- Clock Summary (1)
- Check Timing (0)
- Intra-Clock Paths
- Inter-Clock Paths
- Other Path Groups
- User Ignored Paths
- Unconstrained Paths

## Timing Summary - impl\_1

## Design Timing Summary

## Setup

Worst Negative Slack (WNS): NA

Total Negative Slack (TNS): NA

Number of Failing Endpoints: NA

Total Number of Endpoints: NA

## Hold

Worst Hold Slack (WHS): NA

Total Hold Slack (THS): NA

Number of Failing Endpoints: NA

Total Number of Endpoints: NA

## Pulse Width

Worst Pulse Width Slack (WPWS):

Total Pulse Width Negative Slack (TPWNS):

Number of Failing Endpoints:

Total Number of Endpoints:

**All user specified timing constraints are met.**

Tcl Console

Messages

Log

Reports

Design Runs

Package Pins

I/O Ports

Timing

## Package



A

B

C

D

E

F

G

H

J

K

L

M

N

P

R

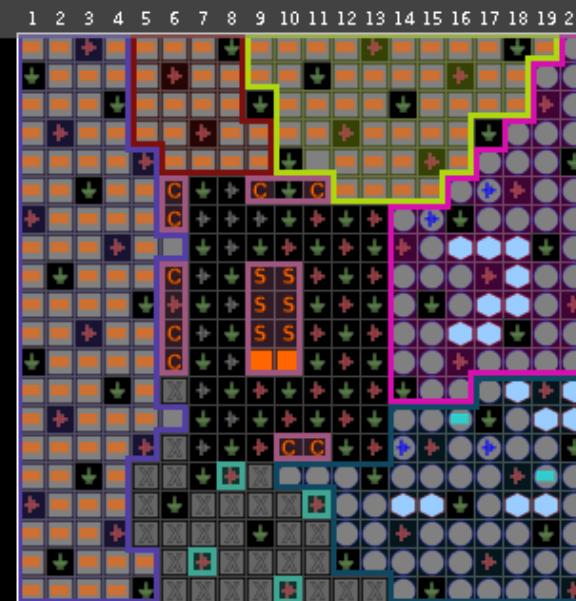
T

U

V

W

Y

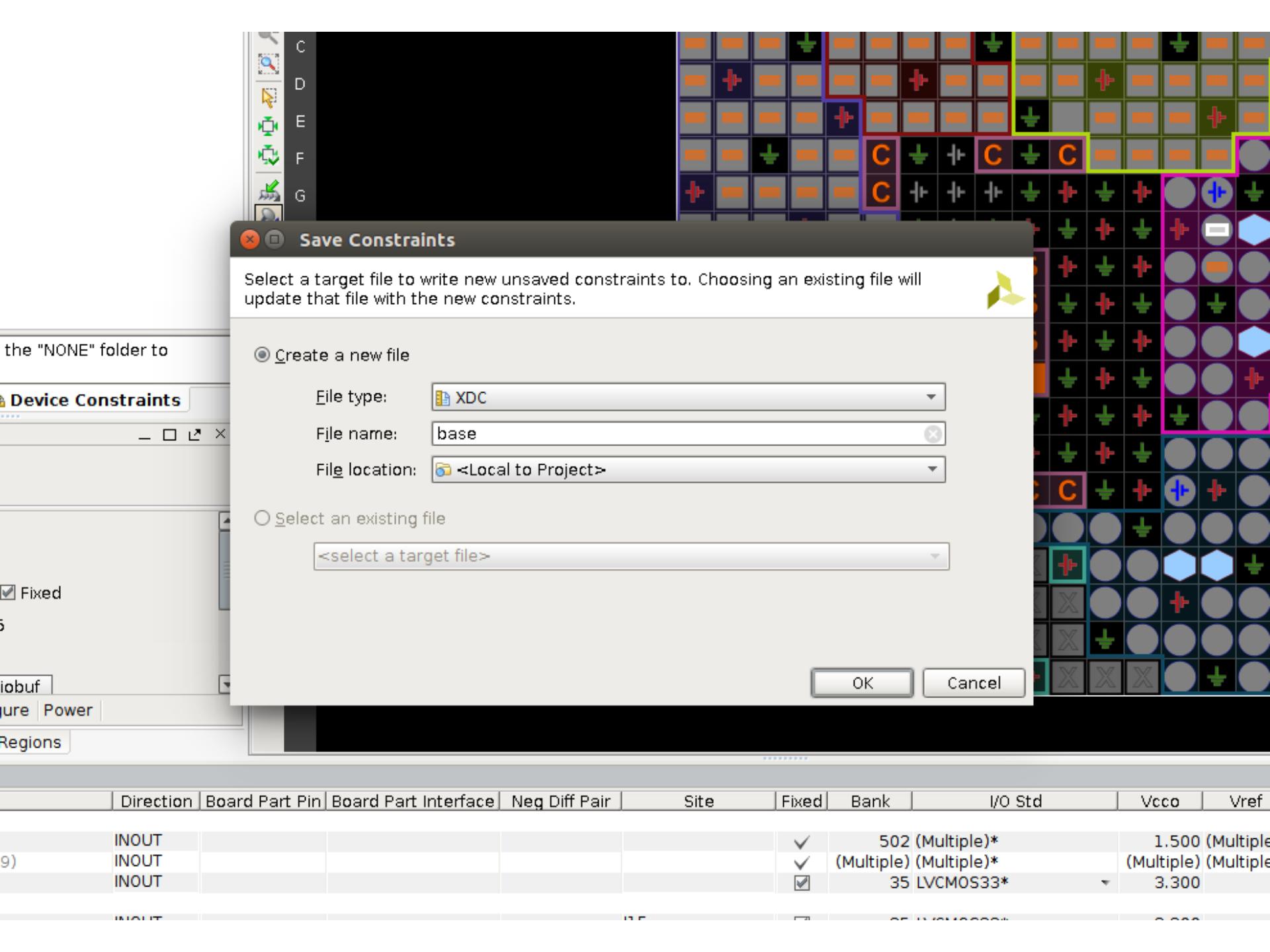


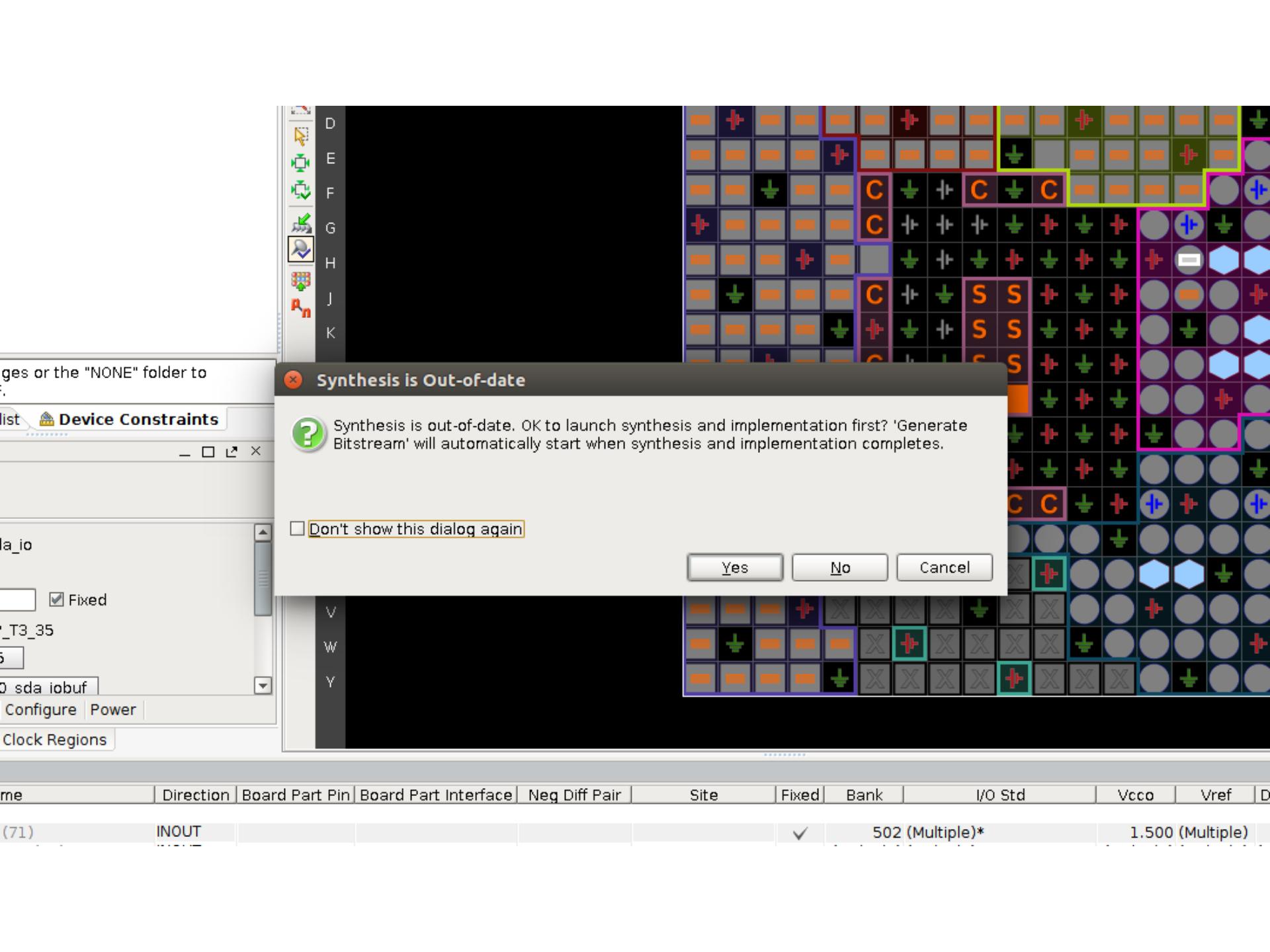
**Properties**   **Clock Regions**

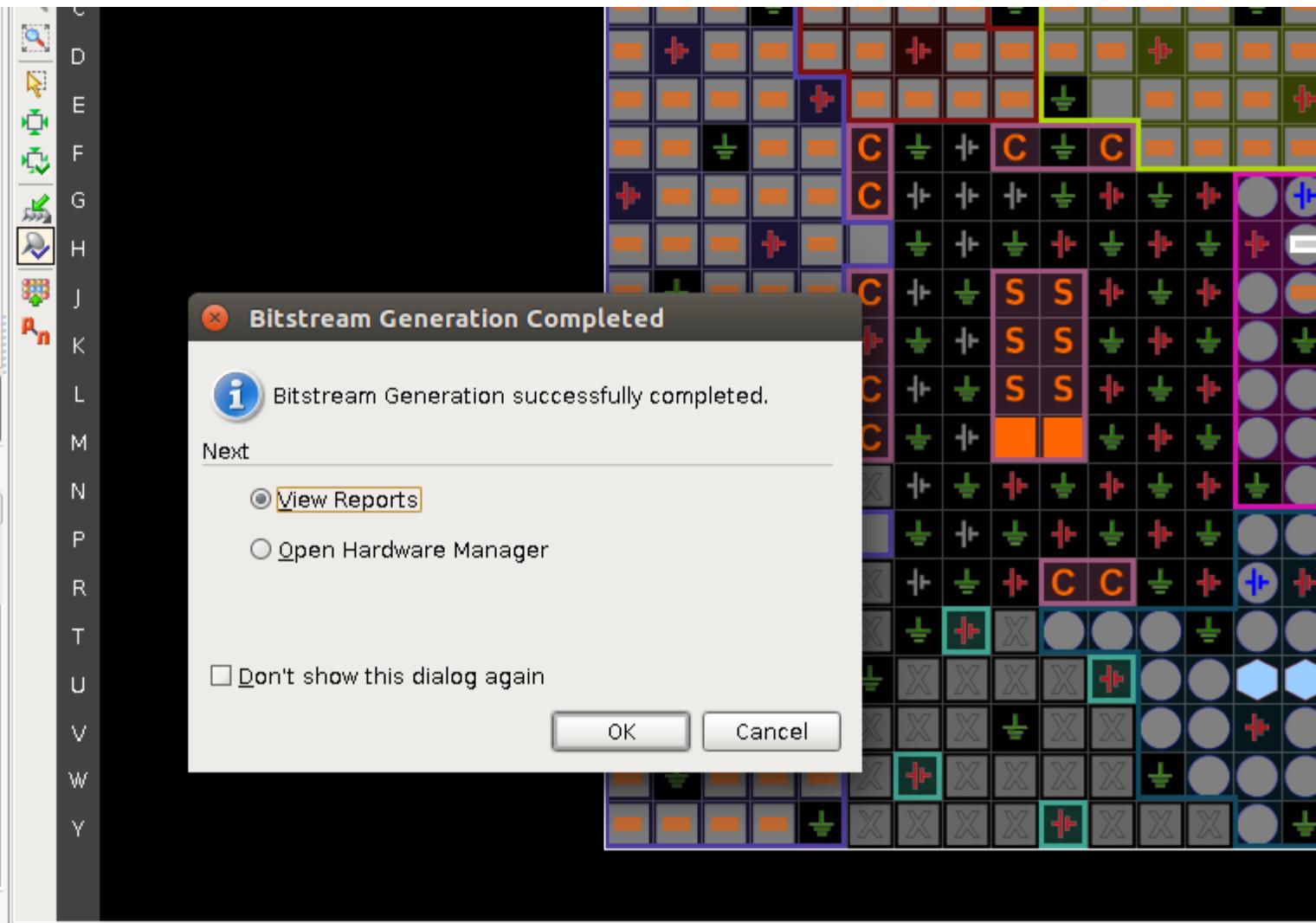
**I/O Ports**

	Name	Direction	Board Part Pin	Board Part Interface	Neg Diff Pair	Site	Fixed	Bank	I/O Std	Vcco
🔍	All ports (132)						✓		502 (Multiple)*	1.500 (Mu...)
📁	DDR_53145 (71)	INOUT					✓		(Multiple) (Multiple)*	(Multiple) (Mu...)
📁	FIXED_IO_53145 (59)	INOUT					✓		35 LVCMOS33*	3.300
📁	IIC_0_53145 (2)	INOUT					✓		35 LVCMOS33*	3.300
Scalar ports (2)	iic_0_scl_io	INOUT			J15		✓		35 LVCMOS33*	3.300
Scalar ports (2)	iic_0_sda_io	INOUT			H15		✓		35 LVCMOS33*	3.300
Scalar ports (0)										

Tcl Console   Messages   Log   Reports   Design Runs   Package Pins   I/O Ports   Timing







INOUT

502 (Multiple)\*

1.500 (M)

)  
ank 34  
ank 35

s on voltages or the "NONE" folder to  
ernal VREF.

s Netlist Device Constraints

Properties

iic\_0\_sda\_io

INOUT

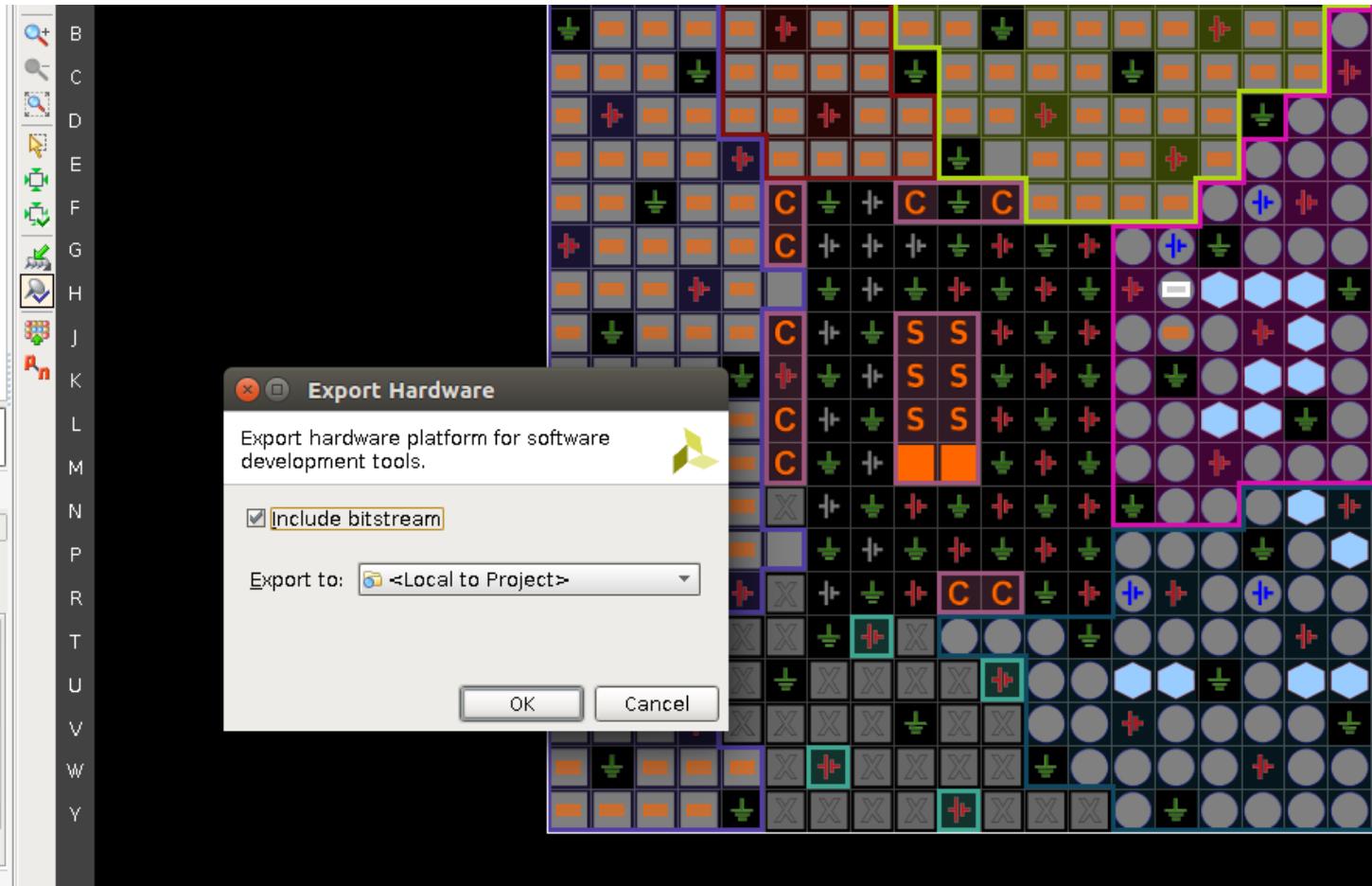
H15  Fixed

IO\_L19P\_T3\_35

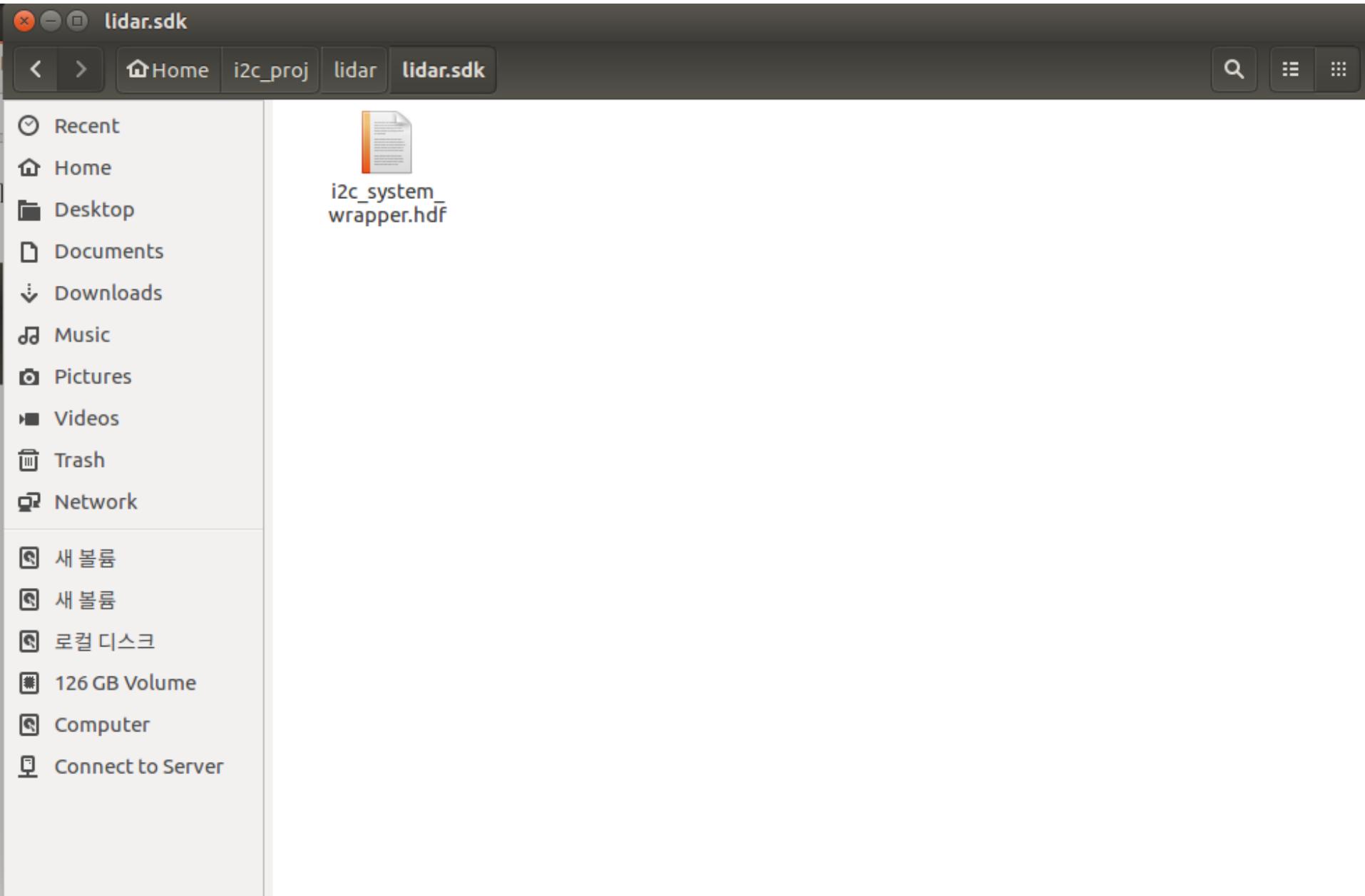
H15

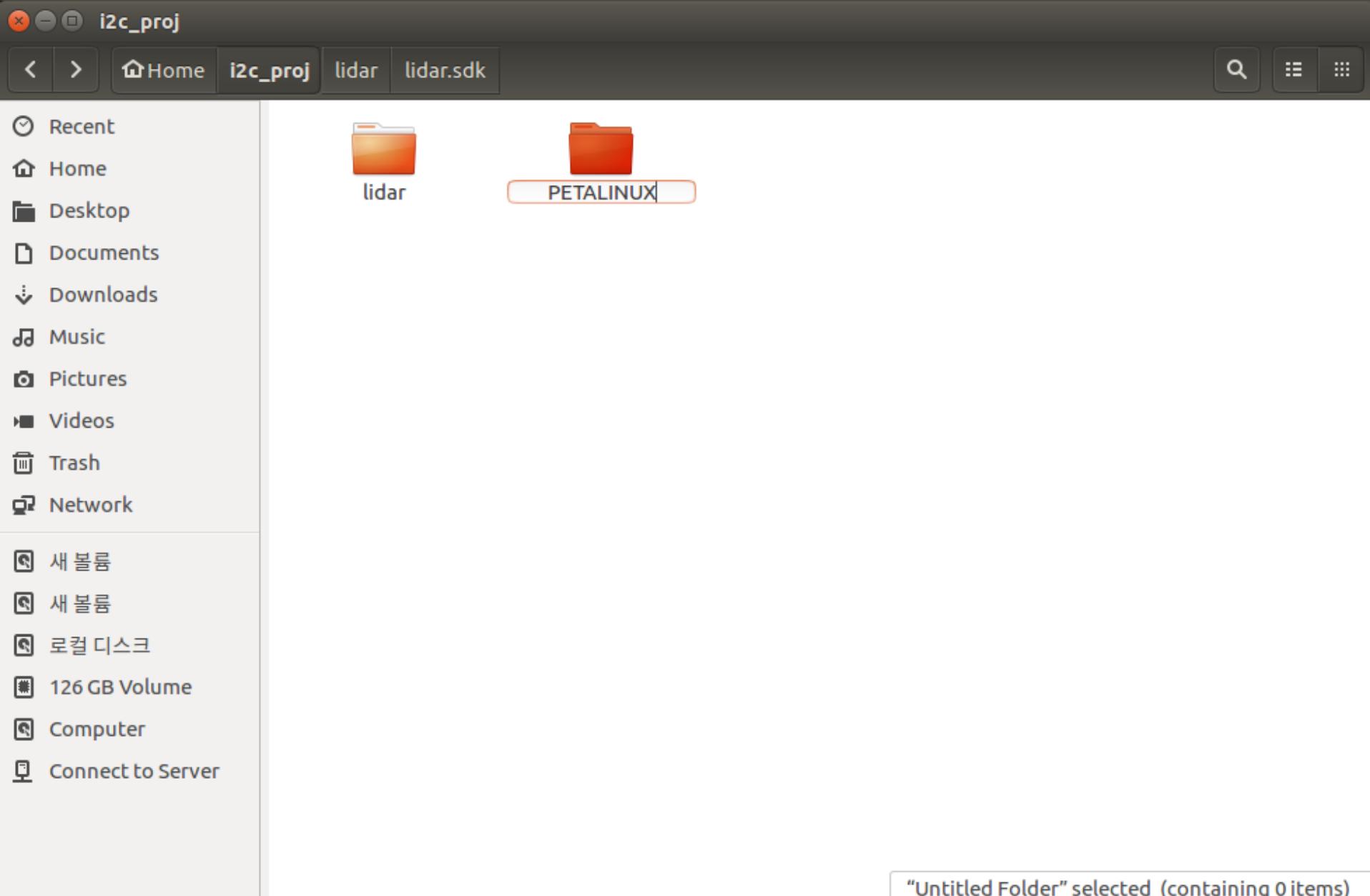
Properties Configure Power

Properties Clock Regions



Name	Modified	Size	GUI Report
sis			
n_1			
Vivado Synthesis Report 5/14/18 12:44 AM	5/14/18 12:44 AM	51.7 KB	
Utilization Report	5/14/18 12:44 AM	7.9 KB	
of-Context Module Runs			





```
sdr@sdr-Samsung-DeskTop-System: ~/i2c_proj/PETALINUX/i2c_lidar
sdr@sdr-Samsung-DeskTop-System:~/i2c_proj$ ls
lidar PETALINUX
sdr@sdr-Samsung-DeskTop-System:~/i2c_proj$ cd PETALINUX/
sdr@sdr-Samsung-DeskTop-System:~/i2c_proj/PETALINUX$ petalinux-create -t project -n i2c_lidar --template zynq
INFO: Create project: i2c_lidar
INFO: New project successfully created in /home/sdr/i2c_proj/PETALINUX/i2c_lidar
sdr@sdr-Samsung-DeskTop-System:~/i2c_proj/PETALINUX$ ls
i2c_lidar
sdr@sdr-Samsung-DeskTop-System:~/i2c_proj/PETALINUX$ cd i2c_lidar/
sdr@sdr-Samsung-DeskTop-System:~/i2c_proj/PETALINUX/i2c_lidar$ ls
config.project hw-description subsystems
sdr@sdr-Samsung-DeskTop-System:~/i2c_proj/PETALINUX/i2c_lidar$ petalinux-config --get-hw-description=~/i2c_proj/lidar/lidar.sdk
INFO: Checking component...
INFO: Getting hardware description...
INFO: Rename i2c_system_wrapper.hdf to system.hdf

***** hsi v2015.4 (64-bit)
**** SW Build 1412921 on Wed Nov 18 09:44:32 MST 2015
** Copyright 1986-2015 Xilinx, Inc. All Rights Reserved.

source /home/sdr/i2c_proj/PETALINUX/i2c_lidar/build/linux/hw-description/hw-description.tcl
-notrace
```

sdr@sdr-Samsung-DeskTop-System: ~/i2c\_proj/PETALINUX/i2c\_lidar

/home/sdr/i2c\_proj/PETALINUX/i2c\_lidar/subsystems/linux/config - linux System Configuration

linux System Configuration

Arrow keys navigate the menu. <Enter> selects submenus ---> (or empty submenus ----). Highlighted letters are hotkeys. Pressing <Y> includes, <N> excludes, <M> modularizes features. Press <Esc><Esc> to exit, <?> for Help, </> for Search. Legend: [\*] built-in [ ] excluded <M> module < > module capable

linux Components Selection --->  
Auto Config Settings --->  
-\*\*- Subsystem AUTO Hardware Settings --->  
Kernel Bootargs --->  
u-boot Configuration --->  
Image Packaging Configuration --->  
Firmware Version Configuration --->

<Select>

< Exit >

< Help >

< Save >

< Load >

sdr@sdr-Samsung-DeskTop-System: ~/i2c\_proj/PETALINUX/i2c\_lidar  
/home/sdr/i2c\_proj/PETALINUX/i2c\_lidar/subsystems/linux/config - linux System Configuration

Do you wish to save your new configuration?  
(Press <ESC><ESC> to continue kernel configuration.)

< Yes >      < No >

```
sdr@sdr-Samsung-DeskTop-System: ~/i2c_proj/PETALINUX/i2c_lidar
***** hsi v2015.4 (64-bit)
**** SW Build 1412921 on Wed Nov 18 09:44:32 MST 2015
** Copyright 1986-2015 Xilinx, Inc. All Rights Reserved.

source /home/sdr/i2c_proj/PETALINUX/i2c_lidar/build/linux/hw-description/hw-description.tcl
-notrace
INFO: [Common 17-206] Exiting hsi at Mon May 14 07:56:09 2018...
INFO: Config linux
[INFO ] config linux
configuration written to /home/sdr/i2c_proj/PETALINUX/i2c_lidar/subsystems/linux/config

*** End of the configuration.
*** Execute 'make' to start the build or try 'make help'.

[INFO ] generate DTS to /home/sdr/i2c_proj/PETALINUX/i2c_lidar/subsystems/linux/configs/dev
ice-tree
INFO: [Hsi 55-1698] elapsed time for repository loading 3 seconds
WARNING: ps7_ethernet_0: No reset found
WARNING: ps7_i2c_0: No reset found
WARNING: ps7_usb_0: No reset found
INFO: [Common 17-206] Exiting hsi at Mon May 14 08:02:10 2018...
[INFO ] generate BSP for zynq_fsbl
INFO: [Hsi 55-1698] elapsed time for repository loading 0 seconds
INFO: [Common 17-206] Exiting hsi at Mon May 14 08:02:20 2018...
INFO: Config linux/kernel
[INFO ] oldconfig linux/kernel
INFO: Config linux/rootfs
[INFO ] oldconfig linux/rootfs
INFO: Config linux/u-boot
[INFO ] generate linux/u-boot configuration files
[INFO ] generate linux/u-boot board header files
INFO: [Hsi 55-1698] elapsed time for repository loading 0 seconds
INFO: [Common 17-206] Exiting hsi at Mon May 14 08:02:34 2018...
[INFO ] oldconfig linux/u-boot
sdr@sdr-Samsung-DeskTop-System:~/i2c_proj/PETALINUX/i2c_lidar$ ls
build components config.project hw-description subsystems
sdr@sdr-Samsung-DeskTop-System:~/i2c_proj/PETALINUX/i2c_lidar$
```

```
sdr@sdr-Samsung-DeskTop-System: ~/i2c_proj/PETALINUX/i2c_lidar/components/bootloader/zynq_fsbl
sdr@sdr-Samsung-DeskTop-System:~/i2c_proj/PETALINUX/i2c_lidar$ ls
build components config.project hw-description subsystems
sdr@sdr-Samsung-DeskTop-System:~/i2c_proj/PETALINUX/i2c_lidar$ cd components/
sdr@sdr-Samsung-DeskTop-System:~/i2c_proj/PETALINUX/i2c_lidar/components$ ls
bootloader
sdr@sdr-Samsung-DeskTop-System:~/i2c_proj/PETALINUX/i2c_lidar/components$ cd bootloader/
sdr@sdr-Samsung-DeskTop-System:~/i2c_proj/PETALINUX/i2c_lidar/components/bootloader$ ls
zynq_fsbl
sdr@sdr-Samsung-DeskTop-System:~/i2c_proj/PETALINUX/i2c_lidar/components/bootloader/zynq_fsbl$ cd zynq_fsbl/
sdr@sdr-Samsung-DeskTop-System:~/i2c_proj/PETALINUX/i2c_lidar/components/bootloader/zynq_fsbl$ ls
fsbl_debug.h    image_mover.c  md5.c    nor.h        ps7_parameters.xml  sd.c
fsbl.h          image_mover.h  md5.h    pcap.c      qspi.c           sd.h
fsbl_handoff.S lscript.ld     nand.c   pcap.h      qspi.h          zynq_fsbl_bsp
fsbl_hooks.c   main.c         nand.h   ps7_init.c  rsa.c
fsbl_hooks.h   Makefile       nor.c    ps7_init.h  rsa.h
sdr@sdr-Samsung-DeskTop-System:~/i2c_proj/PETALINUX/i2c_lidar/components/bootloader/zynq_fsbl$
```

```
sdr@sdr-Samsung-DeskTop-System: ~/i2c_proj/PETALINUX/i2c_lidar
sdr@sdr-Samsung-DeskTop-System:~/i2c_proj/PETALINUX/i2c_lidar$ ls
build components config.project hw-description subsystems
sdr@sdr-Samsung-DeskTop-System:~/i2c_proj/PETALINUX/i2c_lidar$ petalinux-config -c u-boot
INFO: Checking component...
INFO: Config linux/u-boot
[INFO ] generate linux/u-boot configuration files
#
# configuration written to .config
#
[INFO ] config linux/u-boot
```

sdr@sdr-Samsung-DeskTop-System: ~/i2c\_proj/PETALINUX/i2c\_lidar

/home/sdr/i2c\_proj/PETALINUX/i2c\_lidar/subsystems/linux/configs/u-boot/config - U-Boot 201

5

U-Boot 2015.07 Configuration

Arrow keys navigate the menu. <Enter> selects submenus ---> (or empty submenus ----). Highlighted letters are hotkeys. Pressing <Y> includes, <N> excludes, <M> modularizes features. Press <Esc><Esc> to exit, <?> for Help, </> for Search. Legend: [\*] built-in [ ] excluded <M> module < > module capable

[ ] **Architecture select (ARM architecture) --->**

ARM architecture --->  
General setup --->  
Boot images --->  
Command line interface --->  
Device Tree Control --->  
-\* Network support --->  
Device Drivers --->  
[ ] Custom physical to bus address mapping  
File systems ----  
Library routines --->  
[ ] Unit tests ----

<Select>

< Exit >

< Help >

< Save >

< Load >

sdr@sdr-Samsung-DeskTop-System: ~/i2c\_proj/PETALINUX/i2c\_lidar

/home/sdr/i2c\_proj/PETALINUX/i2c\_lidar/subsystems/linux/configs/u-boot/config - U-Boot 201

5

U-Boot 2015.07 Configuration

Arrow keys navigate the menu. <Enter> selects submenus ---> (or empty submenus ----). Highlighted letters are hotkeys. Pressing <Y> includes, <N> excludes, <M> modularizes features. Press <Esc><Esc> to exit, <?> for Help, </> for Search. Legend: [\*] built-in [ ] excluded <M> module < > module capable

- Architecture select (ARM architecture) --->
- ARM architecture --->
- General setup --->
- Boot images --->
- Command line interface --->
- Device Tree Control --->
- \*- Networking support --->
- Device Drivers --->**
- [ ] Custom physical to bus address mapping
- File systems ----
- Library routines --->
- [ ] Unit tests ----

<**Select**>

< Exit >

< Help >

< Save >

< Load >

sdr@sdr-Samsung-DeskTop-System: ~/i2c\_proj/PETALINUX/i2c\_lidar

/home/sdr/i2c\_proj/PETALINUX/i2c\_lidar/subsystems/linux/configs/u-boot/config - U-Boot 201  
5> Device Drivers

Device Drivers

Arrow keys navigate the menu. <Enter> selects submenus ---> (or empty submenus ----). Highlighted letters are hotkeys. Pressing <Y> includes, <N> excludes, <M> modularizes features. Press <Esc><Esc> to exit, <?> for Help, </> for Search. Legend: [\*] built-in [ ] excluded <M> module < > module capable

- \*- Enable Driver Model
  - [\*] Enable warnings in driver model
  - [\*] Support device removal
  - [\*] Support stdio registration
  - [\*] Support numbered aliases in device tree
  - [ ] Enable CPU drivers using Driver Model
  - [ ] Enable demo uclass support
- PCI --->
- NAND Device Support --->
- SPI Flash Support --->
- [ ] Enable Chrome OS EC
- [ ] Enable FSL SEC\_MON Driver
- [ ] Enable PCA9551 LED driver
- [ ] Enable Driver Model for Ethernet drivers
- [ ] Network device support ----
- [ ] Enable Chrome OS EC keyboard support
- [ ] Enable Driver Model for serial drivers
- [ ] Enable an early debug UART for debugging
- [ ] Enable sandbox TPM driver
- [ ] Enable Driver Model for I2C drivers
- Enable I2C compatibility layer**
- SPI Support --->
- [ ] Enable Driver Model for GPIO drivers

+(+)

<Select> < Exit > < Help > < Save > < Load >

sdr@sdr-Samsung-DeskTop-System: ~/i2c\_proj/PETALINUX/i2c\_lidar

/home/sdr/i2c\_proj/PETALINUX/i2c\_lidar/subsystems/linux/configs/u-boot/config - U-Boot 201  
5> Device Drivers

Device Drivers

Arrow keys navigate the menu. <Enter> selects submenus ---> (or empty submenus ----). Highlighted letters are hotkeys. Pressing <Y> includes, <N> excludes, <M> modularizes features. Press <Esc><Esc> to exit, <?> for Help, </> for Search. Legend: [\*] built-in [ ] excluded <M> module < > module capable

```
-*- Enable Driver Model
[*]  Enable warnings in driver model
[*]  Support device removal
[*]  Support stdio registration
[*]  Support numbered aliases in device tree
[ ]  Enable CPU drivers using Driver Model
[ ]  Enable demo uclass support
PCI  --->
    NAND Device Support  --->
        SPI Flash Support  --->
[ ]  Enable Chrome OS EC
[ ]  Enable FSL SEC_MON Driver
[ ]  Enable PCA9551 LED driver
[ ]  Enable Driver Model for Ethernet drivers
[ ]  Network device support  ----
[ ]  Enable Chrome OS EC keyboard support
[ ]  Enable Driver Model for serial drivers
[ ]  Enable an early debug UART for debugging
[ ]  Enable sandbox TPM driver
[*]  Enable Driver Model for I2C drivers
[*]  Enable I2C compatibility layer
    SPI Support  --->
[ ]  Enable Driver Model for GPIO drivers
(+)
```

<Select>

< Exit >

< Help >

< Save >

< Load >

sdr@sdr-Samsung-DeskTop-System: ~/i2c\_proj/PETALINUX/i2c\_lidar

/home/sdr/i2c\_proj/PETALINUX/i2c\_lidar/subsystems/linux/configs/u-boot/config - U-Boot 201

5

Do you wish to save your new configuration?  
(Press <ESC><ESC> to continue kernel configuration.)

< Yes >      < No >

```
sdr@sdr-Samsung-DeskTop-System: ~/i2c_proj/PETALINUX/i2c_lidar
sdr@sdr-Samsung-DeskTop-System:~/i2c_proj/PETALINUX/i2c_lidar$ ls
build components config.project hw-description subsystems
sdr@sdr-Samsung-DeskTop-System:~/i2c_proj/PETALINUX/i2c_lidar$ petalinux-config -c u-boot
INFO: Checking component...
INFO: Config linux/u-boot
[INFO ] generate linux/u-boot configuration files
#
# configuration written to .config
#
[INFO ] config linux/u-boot
configuration written to /home/sdr/i2c_proj/PETALINUX/i2c_lidar/subsystems/linux/configs/u-
boot/config

*** End of the configuration.
*** Execute 'make' to start the build or try 'make help'.

sdr@sdr-Samsung-DeskTop-System:~/i2c_proj/PETALINUX/i2c_lidar$
```

```
sdr@sdr-Samsung-DeskTop-System:~/i2c_proj/PETALINUX/i2c_lidar
sdr@sdr-Samsung-DeskTop-System:~/i2c_proj/PETALINUX/i2c_lidar$ petalinux-build
INFO: Checking component...
INFO: Generating make files and build linux
INFO: Generating make files for the subcomponents of linux
INFO: Building linux
[INFO ] pre-build linux/rootfs/fwupgrade
[INFO ] pre-build linux/rootfs/peekpoke
[INFO ] build system.dtb
[INFO ] build linux/kernel
[INFO ] generate linux/u-boot configuration files
[INFO ] update linux/u-boot source
[INFO ] build linux/u-boot
[INFO ] build zynq_fsbl
[INFO ] Setting up stage config
[INFO ] Setting up rootfs config
[INFO ] Updating for cortexa9-vfp-neon
[INFO ] Updating package manager
[INFO ] Expanding stagefs
[INFO ] build linux/rootfs/fwupgrade
[INFO ] build linux/rootfs/peekpoke
[INFO ] build kernel in-tree modules
[INFO ] modules linux/kernel
[INFO ] post-build linux/rootfs/fwupgrade
[INFO ] post-build linux/rootfs/peekpoke
[INFO ] pre-install linux/rootfs/fwupgrade
[INFO ] pre-install linux/rootfs/peekpoke
[INFO ] install system.dtb
[INFO ] install linux/kernel
[INFO ] generate linux/u-boot configuration files
[INFO ] update linux/u-boot source
[INFO ] build linux/u-boot
[INFO ] install linux/u-boot
[INFO ] Expanding rootfs
[INFO ] install sys_init
[INFO ] install linux/rootfs/fwupgrade
[INFO ] install linux/rootfs/peekpoke
[INFO ] install kernel in-tree modules
[INFO ] modules_install linux/kernel
[INFO ] post-install linux/rootfs/fwupgrade
[INFO ] post-install linux/rootfs/peekpoke
[INFO ] package rootfs.cpio to /home/sdr/i2c_proj/PETALINUX/i2c_lidar/images/linux
[INFO ] Update and install vmlinuz image
[INFO ] vmlinuz linux/kernel
[INFO ] install linux/kernel
[INFO ] package zImage
[INFO ] zImage linux/kernel
[INFO ] install linux/kernel
[INFO ] Package HDF bitstream
sdr@sdr-Samsung-DeskTop-System:~/i2c_proj/PETALINUX/i2c_lidar$
```

```
sdr@sdr-Samsung-DeskTop-System: ~/i2c_proj/PETALINUX/i2c_lidar/components/apps/i2c_lidar
sdr@sdr-Samsung-DeskTop-System:~/i2c_proj/PETALINUX/i2c_lidar$ petalinux-create -t apps -n i2c_lidar --enable
INFO: Create apps: i2c_lidar
INFO: New apps successfully created in /home/sdr/i2c_proj/PETALINUX/i2c_lidar/components/apps/i2c_lidar
INFO: Enabling created component...
INFO: It has been enabled to linux/rootfs
webtalk failed:PetaLinux statistics:extra lines detected:notsent_nofile!
webtalk failed:Failed to get PetaLinux usage statistics!
sdr@sdr-Samsung-DeskTop-System:~/i2c_proj/PETALINUX/i2c_lidar$ ls
build components config.project hw-description images subsystems
sdr@sdr-Samsung-DeskTop-System:~/i2c_proj/PETALINUX/i2c_lidar$ cd components/apps/
sdr@sdr-Samsung-DeskTop-System:~/i2c_proj/PETALINUX/i2c_lidar/components/apps$ ls
i2c_lidar
sdr@sdr-Samsung-DeskTop-System:~/i2c_proj/PETALINUX/i2c_lidar/components/apps$ cd i2c_lidar
/
sdr@sdr-Samsung-DeskTop-System:~/i2c_proj/PETALINUX/i2c_lidar/components/apps/i2c_lidar$ ls
i2c_lidar.c Kconfig Makefile README
sdr@sdr-Samsung-DeskTop-System:~/i2c_proj/PETALINUX/i2c_lidar/components/apps/i2c_lidar$ vi i2c_lidar.c
```



```
46 unsigned get_status();
47 void i_read(unsigned char, unsigned, unsigned char*);
48 void i_write(unsigned char reg, unsigned char value);
49 void measurement(unsigned char, unsigned char, unsigned char*);
50 void display(unsigned char, unsigned char*);
51
52 int fd = 0;
53
54 int main(int argc, char *argv[]) {
55     unsigned char receives[8] = {AR_VELOCITY, 0, 0, AR_PEAK_CORR, AR_NOISE_PEAK
56         , AR_SIGNAL_STRENGTH, AR_FULL_DELAY_HIGH, AR_FULL_DELAY_LOW};
57     unsigned char i, options;
58     char *file_name = NULL;
59
60     if(argc < 2) printf("%s\n", USAGE);
61     else if(argc > 2 && atoi(argv[2])) file_name = I2C_FILE_NAME_1;
62     else file_name = I2C_FILE_NAME_0;
63
64     options = atoi(argv[1]);
65
66     if((fd = open(file_name, O_RDWR)) < 0) {
67         perror("----OPEN DEVICE ERROR ");
68         return -1;
69     }
70
71     if(ioctl(fd, I2C_SLAVE, LIDAR_SLAVE_ADDR) < 0) {
72         perror("----SLAVE ADDR CONNECT ERROR ");
73         return -1;
74     }
75
76     i_write(SIG_COUNT_VAL, 0x80);
77     i_write(ACQ_CONFIG_REG, 0x08);
78     i_write(THRESHOLD_BYPASS, 0x00);
79
80     while(1) {
81         measurement(CORRECTION, options, receives);
82         for(i=0; i<99; i++) measurement(NO_CORRECTION, options, receives);
83         // power state control
84         // close
85         // if() close(fd);
86     }
87
88     close(fd);
89
90     return 0;
91 }
```

```
93 unsigned get_status() {
94     unsigned char buf[1] = {STATUS};
95
96     if(write(fd, buf, 1) != 1) {
97         perror("---WRITE REGISTER ERROR ");
98         return -1;
99     }
100
101    if(read(fd, buf, 1) != 1) {
102        perror("---WRITE REGISTER ERROR ");
103        return -1;
104    }
105
106    return buf[0] & 0x01;
107 }
108
109 void i_read(unsigned char reg, unsigned read_size, unsigned char *receives) {
110     unsigned char buf[1] = {reg};
111     unsigned busy_flag = 1, busy_counter = 0;
112
113     while(busy_flag) {
114         busy_flag = get_status();
115         busy_counter++;
116         if(busy_counter > 9999) {
117             printf("BUSY COUNT TIME OUT !\n");
118             return ;
119         }
120     }
121     if(!busy_flag) {
122         if(write(fd, buf, 1) != 1) {
123             perror("---WRITE REGISTER ERROR ");
124             return -1;
125         }
126
127         if(read(fd, receives, read_size) != read_size) {
128             perror("---WRITE REGISTER ERROR ");
129             return -1;
130         }
131     }
132 }
```

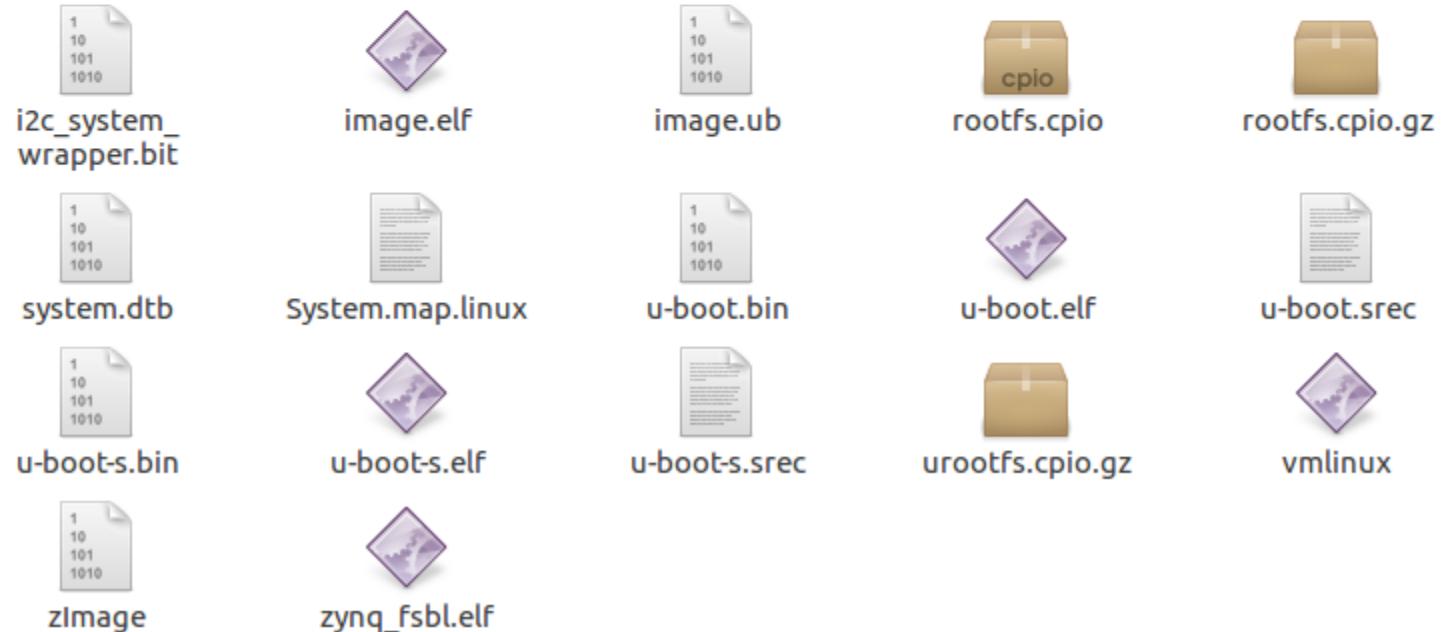
```
; 134 void i_write(unsigned char reg, unsigned char value) {
135     unsigned char buf[2] = {reg, value};
136
137     if(write(fd, buf, 2) != 2) {
138         perror("---WRITE REGISTER ERROR ");
139         return -1;
140     }
141     usleep(1000);
142 }
143
144 void measurement(unsigned char is_correction, unsigned char options, unsigned char *buf
) {
145     unsigned char i;
146     if(is_correction) i_write(ACQ_COMMAND, 0x04);
147     else i_write(ACQ_COMMAND, 0x03);
148
149     i_read(RAED_FROM, 8, buf);
150
151     for(i=1; i<6; i++) buf[i] = buf[i + 2];
152
153     display(options, buf);
154 }
```

```
155
156 void display(unsigned char options, unsigned char *buf) {
157     unsigned char i;
158     char* strings[5] = {"Velocity", "Peak value in correlation record"
159     , "Correlation record noise floor", "Received signal strength", "Distance"};
160     buf[AR_FULL_DELAY_HIGH] = buf[AR_FULL_DELAY_HIGH] << 8 | buf[AR_FULL_DELAY_LOW];
161
162     /*
163         AR_VELOCITY          0
164         AR_PEAK_CORR        1
165         AR_NOISE_PEAK       2
166         AR_SIGNAL_STRENGTH  3
167         AR_FULL_DELAY_HIGH  4
168         AR_FULL_DELAY_LOW   5
169     */
170
171     switch(options) {
172         case OUTPUT_OF_ALL :
173             for(i=0; i<5; i++) printf("%s \t\t\t\t = %d\n", strings[i], buf[i]);
174             break;
175         case DISTANCE_ONLY :
176             printf("%s \t\t\t\t = %d\n", strings[4], buf[AR_FULL_DELAY_HIGH]);
177             break;
178         case DISTANCE_WITH_VELO :
179             printf("%s \t\t\t\t = %d\n", strings[0], buf[AR_VELOCITY]);
180             printf("%s \t\t\t\t = %d\n", strings[4], buf[AR_FULL_DELAY_HIGH]);
181             break;
182         case VELOCITY_ONLY :
183             printf("%s \t\t\t\t = %d\n", strings[0], buf[AR_VELOCITY]);
184             break;
185     }
186     printf("\n");
187 }
```

```
sdr@sdr-Samsung-DeskTop-System: ~/i2c_proj/PETALINUX/i2c_lidar/images/linux
```

```
sdr@sdr-Samsung-DeskTop-System:~/i2c_proj/PETALINUX/i2c_lidar$ ls  
build components config.project hw-description images subsystems  
sdr@sdr-Samsung-DeskTop-System:~/i2c_proj/PETALINUX/i2c_lidar$ cd images/  
sdr@sdr-Samsung-DeskTop-System:~/i2c_proj/PETALINUX/i2c_lidar/images$ ls  
linux  
sdr@sdr-Samsung-DeskTop-System:~/i2c_proj/PETALINUX/i2c_lidar/images$ cd linux/  
sdr@sdr-Samsung-DeskTop-System:~/i2c_proj/PETALINUX/i2c_lidar/images/linux$ ls  
i2c_system_wrapper.bit rootfs.cpio.gz u-boot.elf u-boot-s.srec zynq_fsbl.elf  
image.elf system.dtb u-boot-s.bin urootfs.cpio.gz  
image.ub System.map.linux u-boot-s.elf vmlinux  
rootfs.cpio u-boot.bin u-boot.srec zImage  
sdr@sdr-Samsung-DeskTop-System:~/i2c_proj/PETALINUX/i2c_lidar/images/linux$ nautilus ./  
(nautilus:20669): GLib-GIO-CRITICAL **: g_dbus_interface_skeleton_unexport: assertion 'inte  
rface->priv->connections != NULL' failed
```

Home i2c\_proj PETALINUX i2c\_lidar images linux



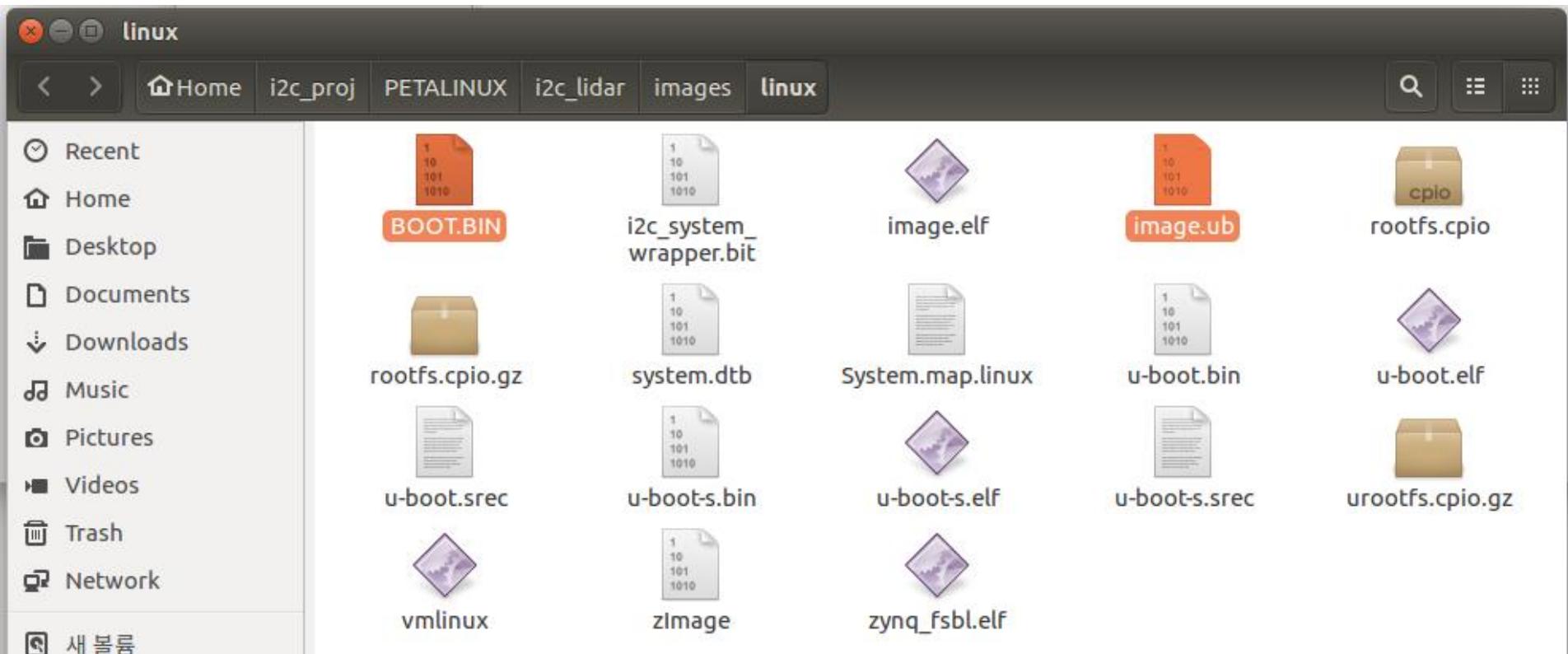
```
sdr@sdr-Samsung-DeskTop-System: ~/i2c_proj/PETALINUX/i2c_lidar/images/linux
```

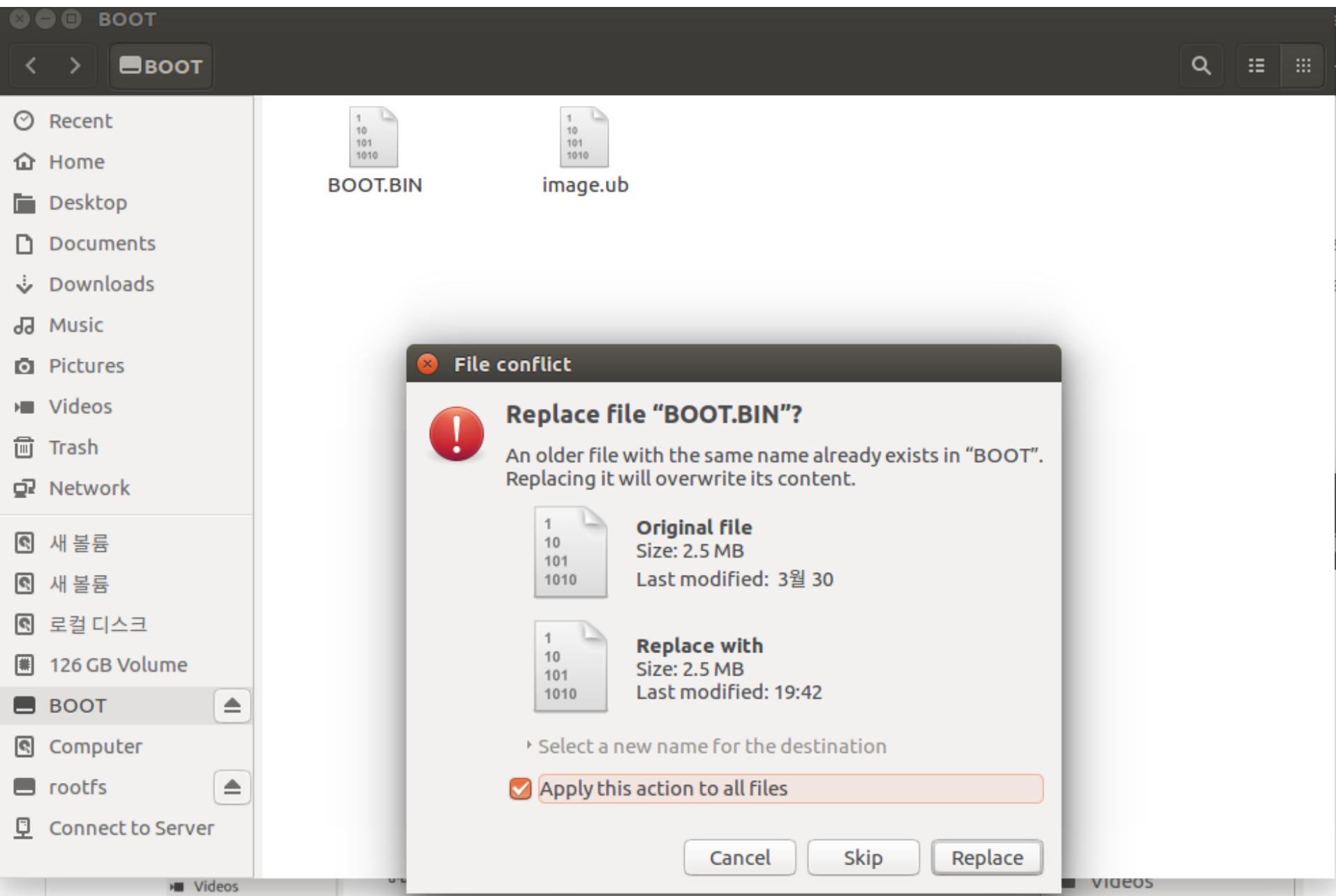
```
sdr@sdr-Samsung-DeskTop-System:~/i2c_proj/PETALINUX/i2c_lidar/images/linux$ ls  
i2c_system_wrapper.bit  rootfs.cpio.gz    u-boot.elf      u-boot-s.srec   zynq_fsbl.elf  
image.elf                system.dtb        u-boot-s.bin   urootfs.cpio.gz  
image.ub                 System.map.linux  u-boot-s.elf   vmlinuz  
rootfs.cpio              u-boot.bin       u-boot.srec   zImage
```

```
sdr@sdr-Samsung-DeskTop-System:~/i2c_proj/PETALINUX/i2c_lidar/images/linux$ petalinux-build
```

```
INFO: Checking component...  
INFO: Generating make files and build linux  
INFO: Generating make files for the subcomponents of linux  
INFO: Building linux  
[INFO ] Cleaning packages  
[INFO ] clean linux/rootfs/fwupgrade  
[INFO ] clean linux/rootfs/i2c_lidar  
[INFO ] clean linux/rootfs/peekpoke  
[INFO ] pre-build linux/rootfs/fwupgrade  
[INFO ] pre-build linux/rootfs/i2c_lidar  
[INFO ] pre-build linux/rootfs/peekpoke  
[INFO ] build system.dtb  
[INFO ] build linux/kernel  
[INFO ] generate linux/u-boot configuration files  
[INFO ] update linux/u-boot source  
[INFO ] build linux/u-boot  
[INFO ] build zynq_fsbl  
[INFO ] Setting up stage config  
[INFO ] Setting up rootfs config  
[INFO ] Updating for cortexa9-vfp-neon  
[INFO ] Updating package manager  
[INFO ] Expanding stagefs  
[INFO ] build linux/rootfs/fwupgrade  
[INFO ] build linux/rootfs/i2c_lidar  
[INFO ] build linux/rootfs/peekpoke  
[INFO ] build kernel in-tree modules  
[INFO ] modules linux/kernel  
[INFO ] post-build linux/rootfs/fwupgrade  
[INFO ] post-build linux/rootfs/i2c_lidar  
[INFO ] post-build linux/rootfs/peekpoke
```

```
sdr@sdr-Samsung-DeskTop-System: ~/i2c_proj/PETALINUX/i2c_lidar/images/linux
sdr@sdr-Samsung-DeskTop-System: ~/i2c_proj/PETALINUX/i2c_lidar/images/linux$ petalinux-package --boot --fsbl zynq_fsbl.elf --fpga ./i2c_system_wrapper.bit --u-boot --force
INFO: File in BOOT BIN: "/home/sdr/i2c_proj/PETALINUX/i2c_lidar/images/linux/zynq_fsbl.elf"
INFO: File in BOOT BIN: "/home/sdr/i2c_proj/PETALINUX/i2c_lidar/images/linux/i2c_system_wrapper.bit"
INFO: File in BOOT BIN: "/home/sdr/i2c_proj/PETALINUX/i2c_lidar/images/linux/u-boot.elf"
INFO: Generating zynq binary package BOOT.BIN...
INFO: Binary is ready.
sdr@sdr-Samsung-DeskTop-System: ~/i2c_proj/PETALINUX/i2c_lidar/images/linux$
```







파일 시스템이 fat32 인 부분을 우클릭하고 delete 한다.

