NAME _____ DATE _____

10-2 LAB EXPERIMENT: 3-BIT PARALLEL ADDER

OBJECTIVE

To wire and operate a 3-bit parallel adder using AND, NAND, and XOR gates.

MATERIALS

Qty.		Qty.	
2	7400 two-input NAND gate ICs	1	7408 two-input AND gate IC
2	7486 two-input XOR gates ICs	6	logic switches
4	LED indicator-light assemblies	1	5-V dc regulated power supply

SYSTEM DIAGRAM

The wiring diagram for a 3-bit parallel adder using gates is drawn in Fig. 10-6. It will add two 3-bit binary numbers ($A_2A_1A_0 + B_2B_1B_0$) and show the sum on the display at the lower right. The top XOR and AND gates form a half adder for adding the two inputs from the 1s column. The middle five gates (two XORs and three NANDs) form a full adder, used to add the carry in (C_{in}) plus the two inputs from the 2s column. The bottom five gates also form a full adder, used to add the inputs from the 4s column plus the carry in (C_{in}) from the 2s full-adder circuit. The carry out (C_o) from the lower-right full adder is the overflow or carry into the 8s position of the sum.

PROCEDURE

1. Insert the two 7400, one 7408, and two 7486 ICs into the mounting board.
2. Power OFF. Connect power (V_{CC} and GND) to each of the five ICs.
3. Wire the 3-bit adder shown in Fig. 10-6. Use six switches for the input numbers $A_2A_1A_0$ and $B_2B_1B_0$. Wire the five ICs. Connect the outputs to the four LED indicator-light assemblies.
4. Power ON. Operate the 3-bit parallel adder. Try adding binary 111 to 111. The answer should be 1110 (decimal 14). Try five binary addition problems of your choice (not over 3 bits long). Record your *inputs* and *outputs.*
5. Show your instructor your 3-bit parallel adder circuit. Be prepared to demonstrate the circuit and answer questions about the circuit's operation.
6. Power OFF. Take down the circuit, and return all equipment to its proper place.

QUESTIONS

Complete questions 1 to 5.

1. Refer to Fig. 10-6. If inputs A_2 and B_2 and C_{in} of the bottom full adder are all 1, then indicators _____ and _____ [1s, 2s, 4s, 8s] are sure to be lit. **1.** _____ _____
2. Refer to Fig. 10-6. Indicator _____ [1s, 2s, 4s, 8s] could be considered an overflow or carry indicator. **2.** _____
3. Refer to Fig. 10-6. If A_0, B_0, A_1, and B_1 are all at 1, then the 1s indicator will read _____ (0, 1) and the 2s indicator _____ (0, 1). **3.** _____ _____
4. Refer to Fig. 10-6. What is the highest binary sum this adder will handle? This equals what in decimal? **4.** _____ _____
5. What do LSB and MSB mean in relation to a binary number? **5.** _____ _____

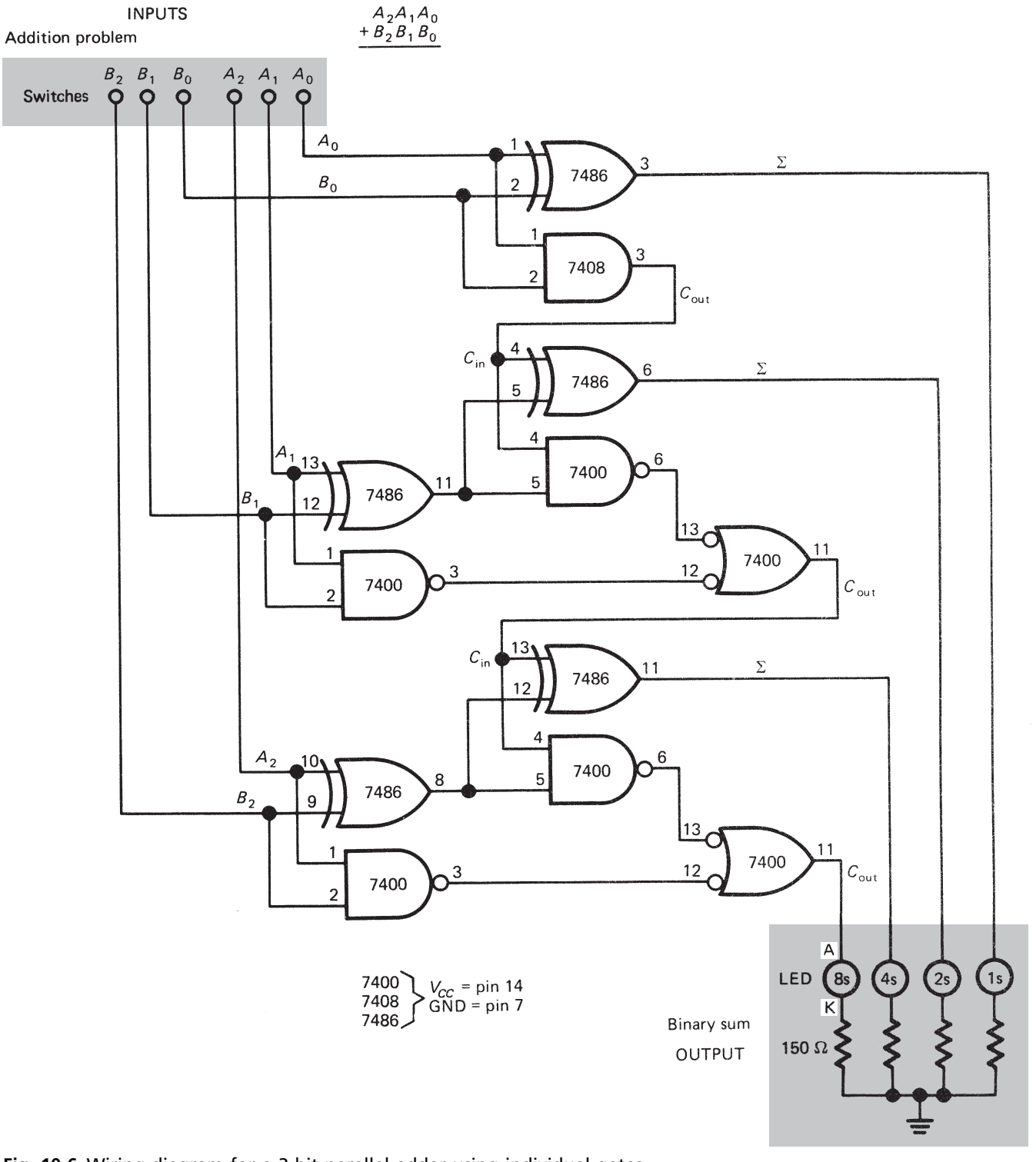

Fig. 10-6 Wiring diagram for a 3-bit parallel adder using individual gates.