CHAPTER-1

INTRODUCTION

A binary sequence contains either 1's or 0's. It is necessary to count number of one's and zero's in the given sequence. As while transmitting we can have a count of how many one's and zero's we are transmitting. If we have counter even at receiver we can count the number of one's and zero's that are received. So that we can check whether the count of the given sequence while transmitting equal to the count at the receiver. In order to develop a counter for counting number of one's and zero's in the given sequence we need to have two ripple counters (one to count the occurrence of one's and other for zero's), a shift register which stores the given binary sequence and shifts the bits as soon as the input bit stream is loaded into register. A BCD to 7-segment decoder is also used to display the count of one's and zero's in 7- segment display.

1.1 Flip Flops

- Flip-flops are 1 bit memory storage devices.
- In this project we are using flip-flops to store the input binary sequence.
- For an n-bit input binary sequence n flip-flops are used .
- A series of flip-flops are said to be a register.
- A Shift Register shifts the data that is stored in flip-flops.
- In this project a Parallel in – Serial out Shift Register is used for loading the input data and shifting that data

1.2 Shift Register

- In digital circuits, a shift register is a cascade of flip flops, sharing the same clock, in which the output of each flip-flop is connected to the data input of the next flip-flop in the chain, resulting in a circuit that shifts by one position the bit array stored in it, shifting in the data present at its input and shifting out the last bit in the array, at each transition of the clock input.

- Shift registers can have both parallel and serial inputs and outputs. These are often configured as 'serial-in, parallel-out' (SIPO) or as 'parallel-in, serial-out' (PISO). There are also types that have both serial and parallel input and types with serial and parallel output.

1.3 Parallel-in Serial-out (PISO) Shift Register

- The inputs to the register are given in parallel and the outputs are taken in a serial order. So the name Parallel-in Serial-out Shift Regsiter.
- In this type of shift register , first the input has to be loaded to the register and then the shifting operation has to be done.
- This configuration has the data input on lines D1 through D4 in parallel format, being D1 the MSB. To write the data to the register, the Write/Shift control line must be held LOW. To shift the data, the W/S control line is brought HIGH and the registers are clocked. The arrangement now acts as a PISO shift register, with D1 as the Data Input. However, as long as the number of clock cycles is not more than the length of the data-string, the Data Output, Q, will be the parallel data read off in order.

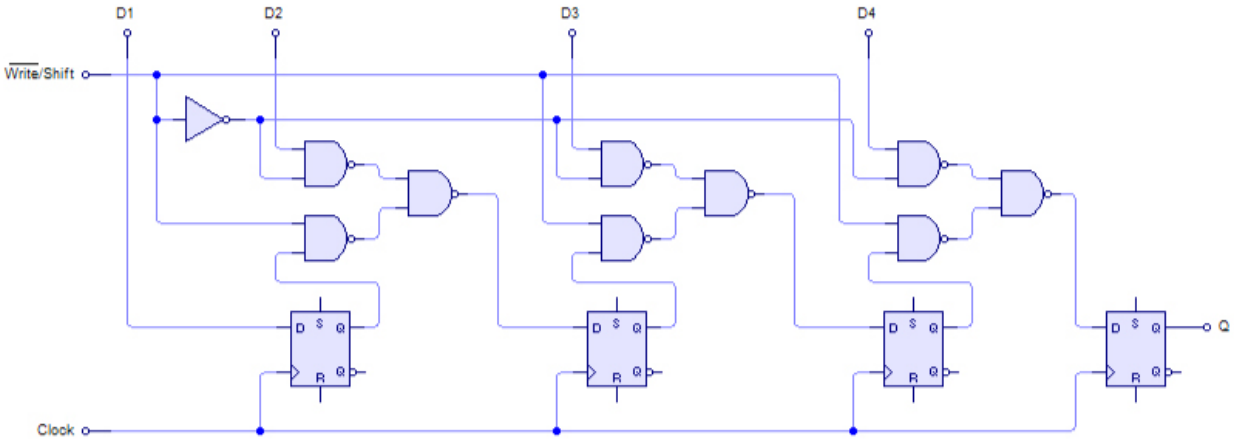

Fig no. : 1.1 Parallel-In-Serial Out Shift Register

1.4 Ripple Counter

- A ripple counter is an asynchronous counter where only the first flip-flop is clocked by an external clock. All subsequent flip-flops are clocked by the output of the preceding flip-flop. Asynchronous counters are also called ripple-counters because of the way the clock pulse ripples it way through the flip-flops.
- The MOD of the ripple counter or asynchronous counter is 2^n if n flip-flops are used. For a 4-bit counter, the range of the count is 0000 to 1111 (2^4-1)

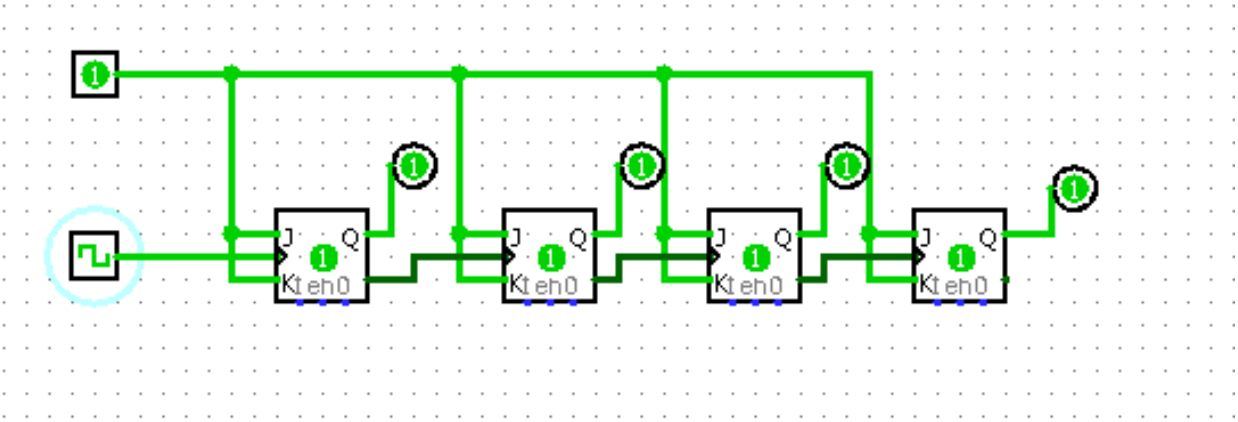

Fig no. 1.2 4 – bit Ripple Counter

- As we are going to count the number of one's and zero's in the given sequence, two counters are used one for counting the occurrence of one's and other for zero's.
- The outputs of the counters gives the occurrence of one's ad zero's.

1.5 BCD to 7-Segment Decoder

A binary coded decimal (BCD) to 7-segment display decoder have 4 BCD inputs and 7 output lines, one for each LED segment. This allows a smaller 4-bit binary number (half a byte) to be used to display all the denary numbers from 0 to 9 and by adding two displays together, a full range of numbers from 00 to 99 can be displayed with just a single byte of 8 data bits.

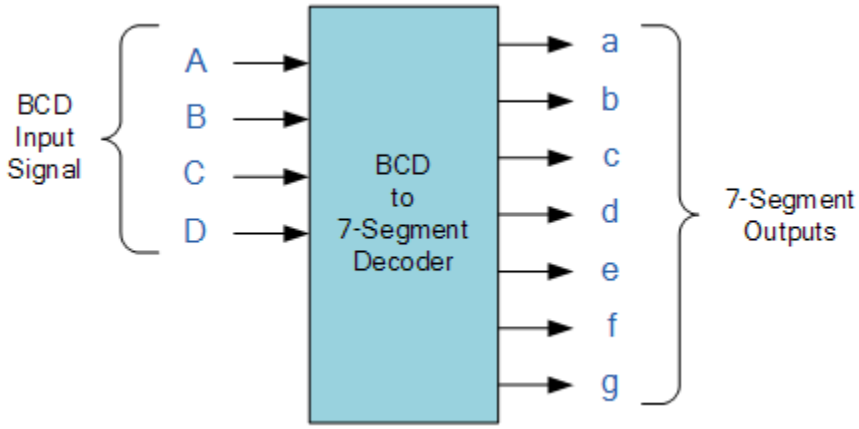

Fig no. : 1.3 BCD to 7-Segment Decoder

CHAPTER-2

PROJECT DESIGN

The input bit sequence is given as the input to the shift register. This sequence has to be loaded in the register. The number of bits that are to be loaded in the register depends on the number of flip-flops present in the register. Once loaded the mode of the shift register is changed to shifting. The bits that are loaded are shifted one by one for each clock pulse. Based on number of flip-flops placed in shift register the number of clock pulses that are to be applied depends. The output bit of the shift register will be either one or zero. If this bit is one then this goes to a particular ripple counter. If the bit is zero then it goes to another ripple counter which counts the occurrence of the zero bit. As we know that a ripple counter is the one which counts the occurrence of an event. This output of ripple counter gives the count of the occurrence of number of ones's and zero's in given input sequence. This output of ripple counter is connected to BCD to 7-Segment Decoder. This output of decoder is given to 7-Segment display. Which displays the count of occurrence of number of one's and zero's in given input sequence in decimal format.

CHAPTER- 3

IMPLEMENTATION OF PROJECT

As per the project design, the input sequence has to be loaded to shift register, so the input sequence is given to Parallel-in-serial-out shift register. The output of shift register is either one or zero, based on this it goes to respective ripple counter. So, the output of shift register is connected to ripple counter. The output of ripple counter gives the count of one's and zero's in the given input sequence in binary format. In-order to display this in decimal format, This output of ripple counter is connected to BCD to 7-Segment display which in-turn connected to 7 segment display, which displays the count of one's and zero's in decimal format.

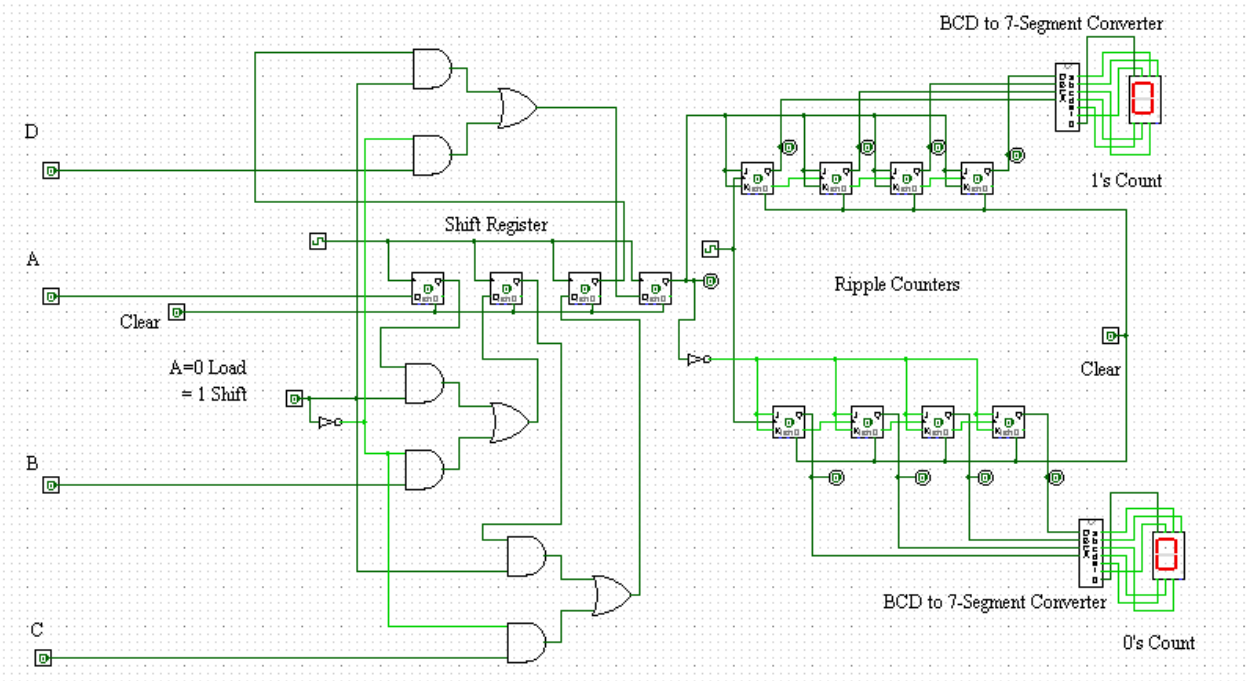

Fig no. : 3.1 Circuit Diagram

CHAPTER- 4

RESULTS

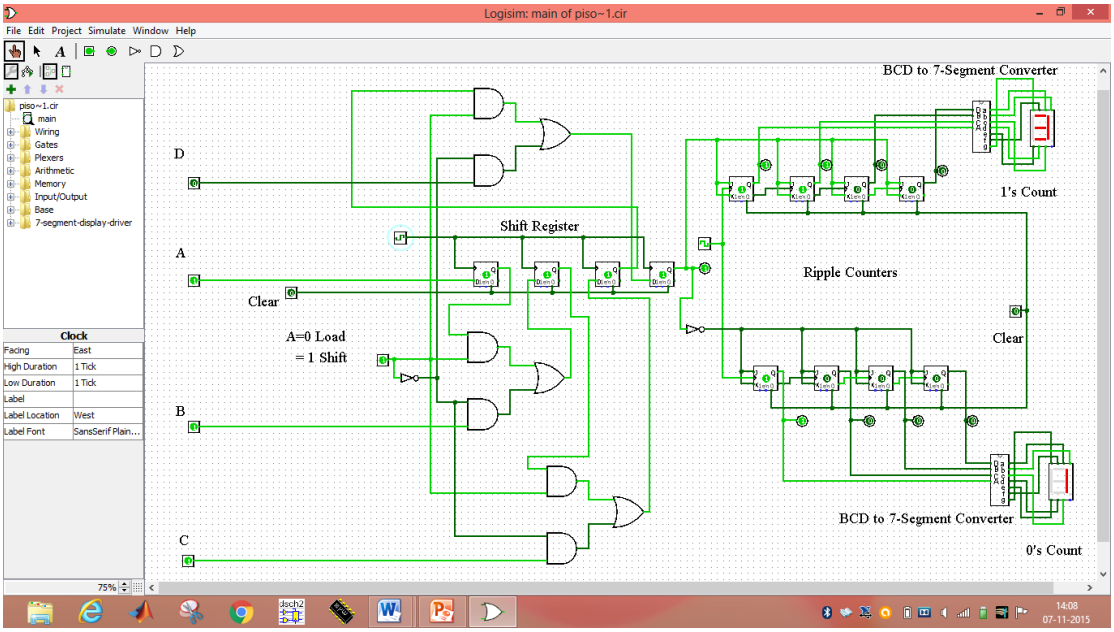

Fig no. : 4.1 Input Sequence has 3 one's and a zero

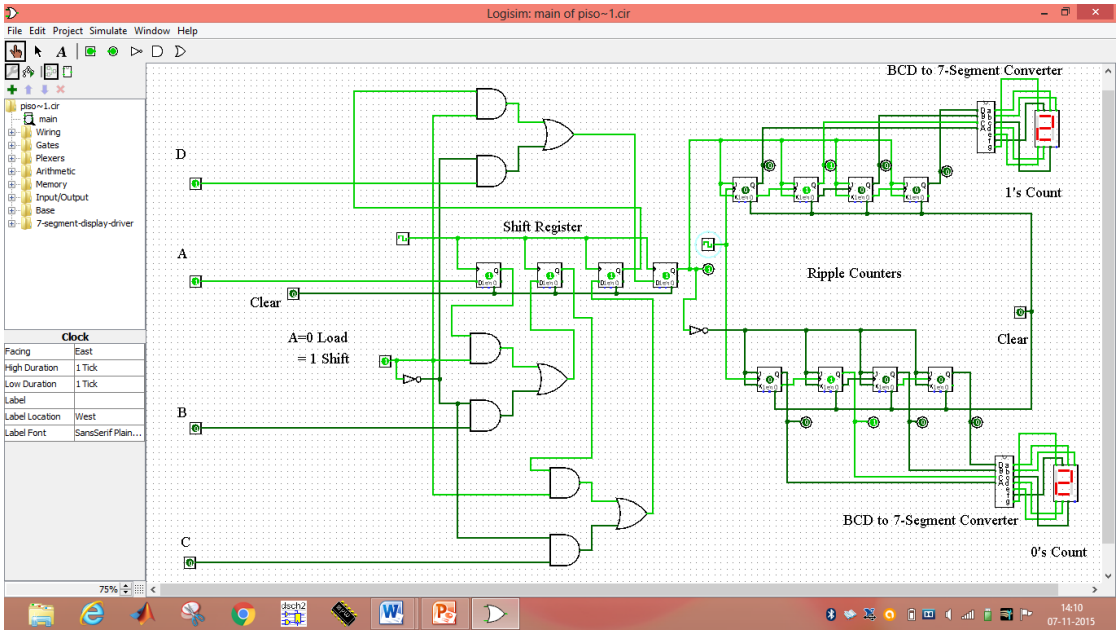

Fig no. : 4.1 Input Sequence has 2 one's and 2 zero's

CHAPTER-5

5.1 Advantages

1. Circuit complexity is low.
2. This circuit is the cheapest error detecting circuit.

5.2 Dis-advantages

1. By using this technique we can detect the errors but we cant rectify the errors.
2. Asynchronous counter is slow, as the propagation delays of the flip-flops add together to produce the overall delay. Hence, the more bits or number of flip-flops in an asynchronous counter, the slower it will be.

5.3 Applications

1. Counting the number of one's and zero's can be used for error detection techniques.
2. If we use this counting circuit both at transmitting end and receiving end then we can detect the error. If the count at transmitter end and receiver end are not equal then we can say that there is an error in received signal.

CHAPTER - 6

CONCLUSION

A circuit which the counts the occurrence of one's and zero's in the given bit stream is designed using shift register and ripple counter. Here in this circuit we considered only 4 data bits .similarly we can design the circuit for number of bits in a binary sequence by increasing the flip flops which is used to store one bit data and shift registers to shift and load the data and bcd counters to count the occurrence of 1's and 0's.

BIBILOGRAPHY

1. Computer Organization And ArchitectureBy William Stallings-8th edition.

2. Computer Organization And Design By P. Pal Chauduri-3rd edition.

3. Computer Organization And Design By David A Patterson and John L Henessey -4th edition.

4. Digital Logic And Computer Design By Morris Mano-3rd edition.