EE2401 Analog Lab: Crystal Oscillator

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Introduction

- Crystal oscillators are essential for timing applications due to their excellent frequency stability.
- Conventional designs face trade-offs between:
  - Power consumption
  - Startup time
- We propose a low-power, fast start-up crystal oscillator.
- It features an autonomous, dynamically adjusted load.
- The design adapts load conditions to:
  - Accelerate startup
  - Minimize steady-state power consumption

Approach

- We began by mathematically deriving all the key equations relevant to oscillator behavior.
- Relationships were plotted using MATLAB to visualize dependencies and trends.
- The problem was broken down into smaller sub-blocks for modular understanding.
- Each sub-block was studied and implemented step-by-step.
- Finally, the complete system was simulated using Cadence Virtuoso.

Advantages of the Proposed Oscillator

- **Low Power Consumption:** Ideal for energy-constrained applications.
- **Fast Start-Up:** Achieves stable oscillation quickly after power-on.
- **Autonomous Load Adjustment:**
  - Temporarily increases load during startup to accelerate oscillation.
  - Reduces load after startup to minimize steady-state power usage.

Factors Affecting Startup Time

- Quality factor (Q): Higher Q = slower startup.
- Negative resistance ($|R_N|$): Helps overcome losses.
- Frequency: Higher frequency $\rightarrow$ quicker startup.

Methodology

- Pierce oscillator with NMOS negative resistance.
- Components:
  - Switched capacitor bank.
  - Envelope detector + comparator.
  - Finite-state machine (FSM) for control.
- Fully autonomous startup and load adjustment.

Existing Methods to Improve Startup

- **Increase** g_m: reduces T_s but increases power.
- **Signal Injection**: needs calibration and is PVT-sensitive.
- **Chirp Injection (CI)**: frequency sweep, limited effectiveness.
- **Proposed DAL**: adjusts load capacitance dynamically.

Proposed Method and Negative Resistance

- **No Signal Injection:** Startup achieved without external signal injection.
- **Autonomous Load Control:**
  - XO clock controls the load after it becomes available.
  - No need for external RC oscillator.
- **Performance:**
  - Fast startup time: as low as 200 μs.
  - Ultra-low energy: less than 40 nJ.
- **Efficiency:**
  - Reduced system complexity and area.
  - Suitable for IoT and space-constrained applications.

Need for Negative resistance

- Oscillators experience losses due to components like inductors and capacitors.
- Without compensation, oscillations die out.
- Negative resistance feeds energy back, sustaining oscillation.
- Cross-coupled transistors provide the necessary negative resistance.
- For startup, negative resistance (R_N) must cancel crystal loss (R_m): $|R_N| > R_m$.

Negative Resistance Derivation

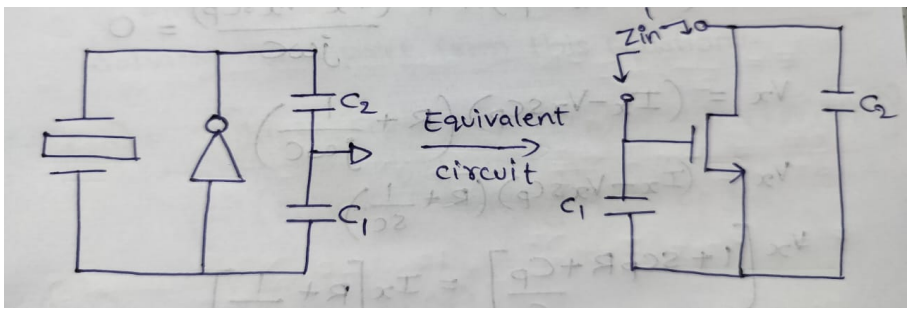


Figure: Equivalent Circuit

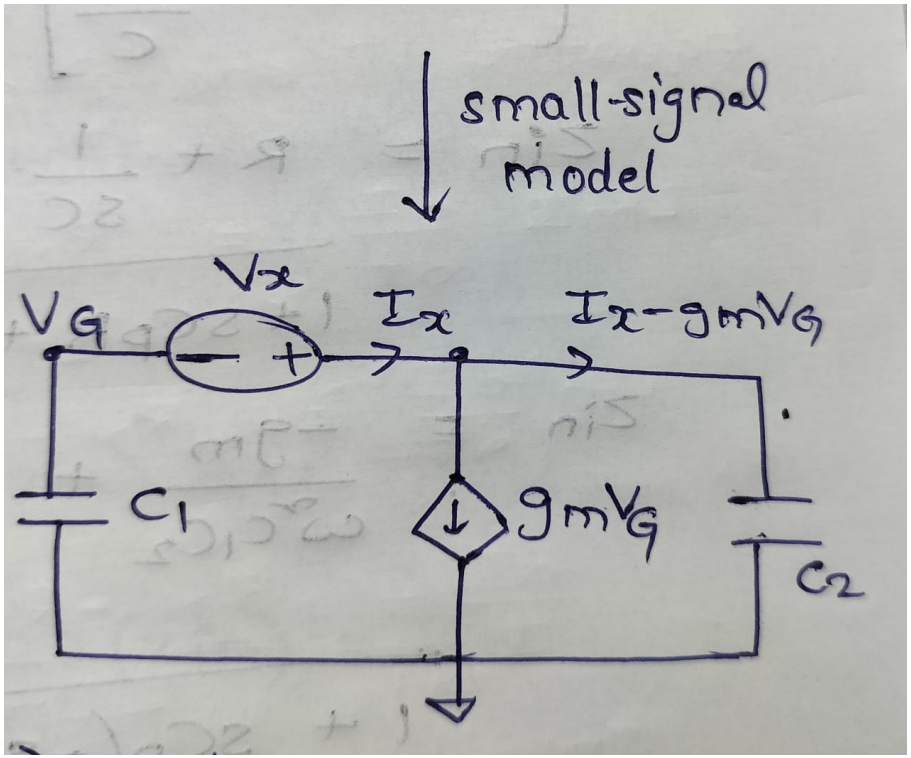


Figure: Small-signal model

$$V_g = -\frac{I_x}{sC_1}, \tag{1}$$

$$\frac{I_x}{sC_1} = V_x - \frac{I_x - g_m V_g}{sC_2}. \tag{2}$$

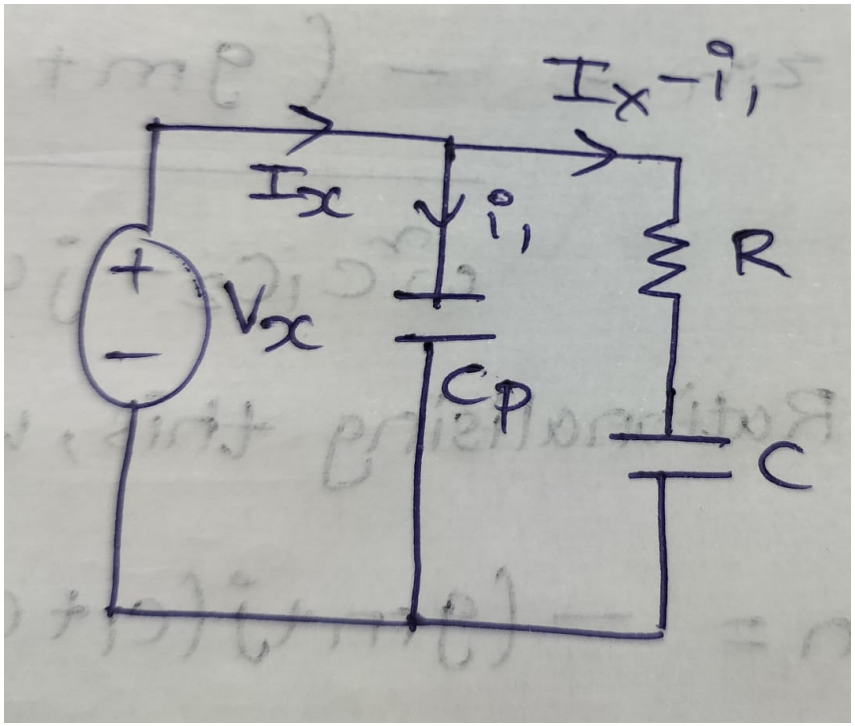
Substituting (1) into (2):

$$I_x\left(\frac{1}{C_1} + \frac{1}{C_2}\right)\frac{1}{s} + \frac{g_m}{sC_1}\left(\frac{I_x}{sC_2}\right) = V_x$$

$$\frac{V_x}{I_x} = Z_{\text{in}} = \frac{C_1 + C_2}{j\omega C_1 C_2} - \frac{g_m}{\omega^2 C_1 C_2}.$$

$$\text{Re}\{Z_{\text{in}}\} = -\frac{g_m}{\omega^2 C_1 C_2}, \qquad \text{Im}\{Z_{\text{in}}\} = \frac{1}{\omega}\frac{C_1 + C_2}{C_1 C_2}.$$

2. Calculating Negative Resistance



$$R = -\frac{g_m}{\omega^2 C_1 C_2}, \quad C = \frac{C_1 C_2}{C_1 + C_2}, \quad i_1 = V_x s C_p.$$

$$-V_x + (I_x - V_x s C_p)R + \frac{I_x - V_x s C_p}{j\omega C} = 0$$

$$Z_{\text{in}} = \frac{R + 1/sC}{1 + sC_p R + C_p/C}.$$

$$\boxed{|R_N| = \frac{g_m C_1 C_2}{\omega^2 (C_1 C_2 + C_p C_1 + C_p C_2)^2 + g_m^2 C_p^2}}$$

Results

Figure: Impedance vs frequency plot

Results

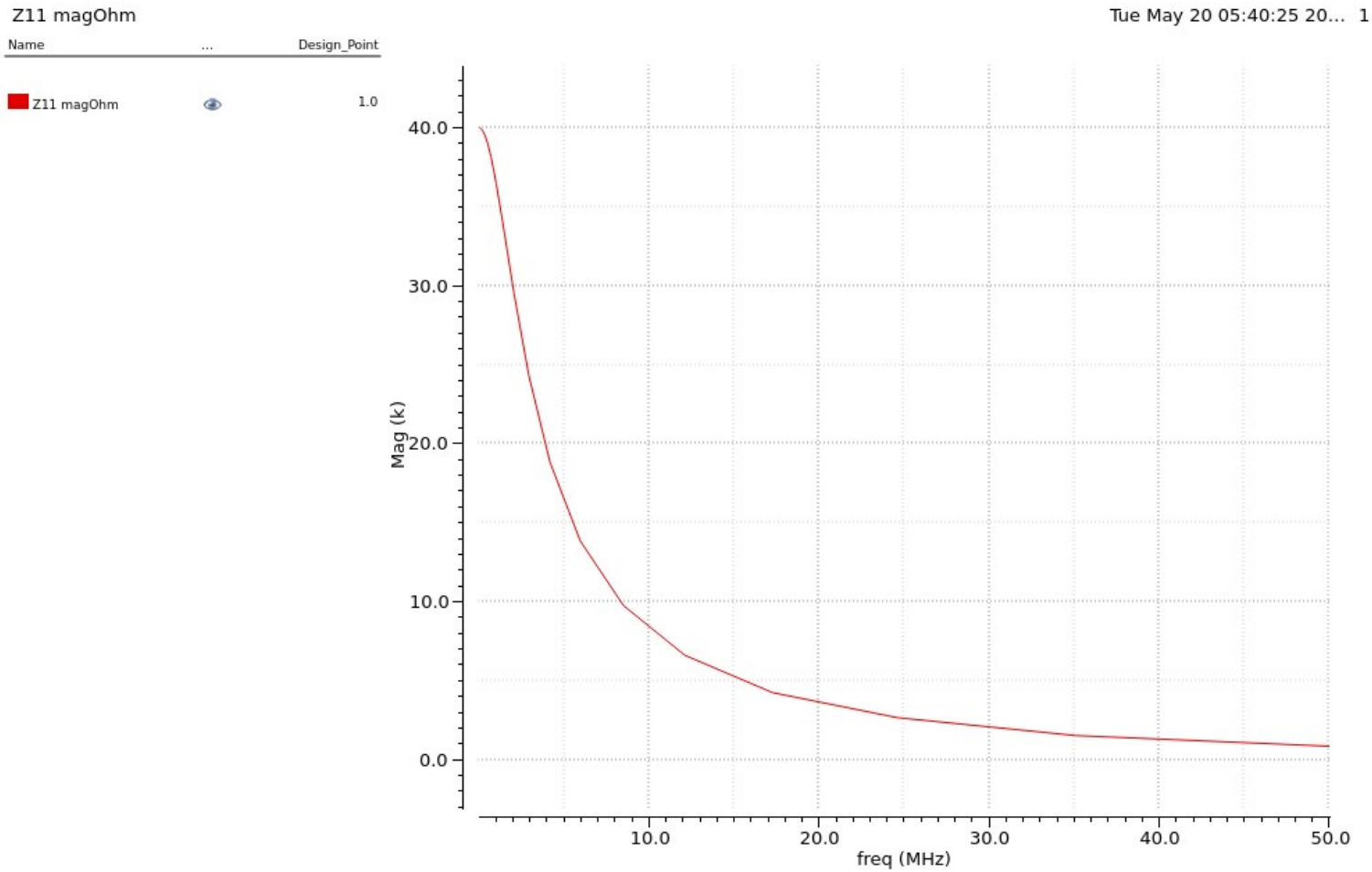


Figure: Impedance plot

Results

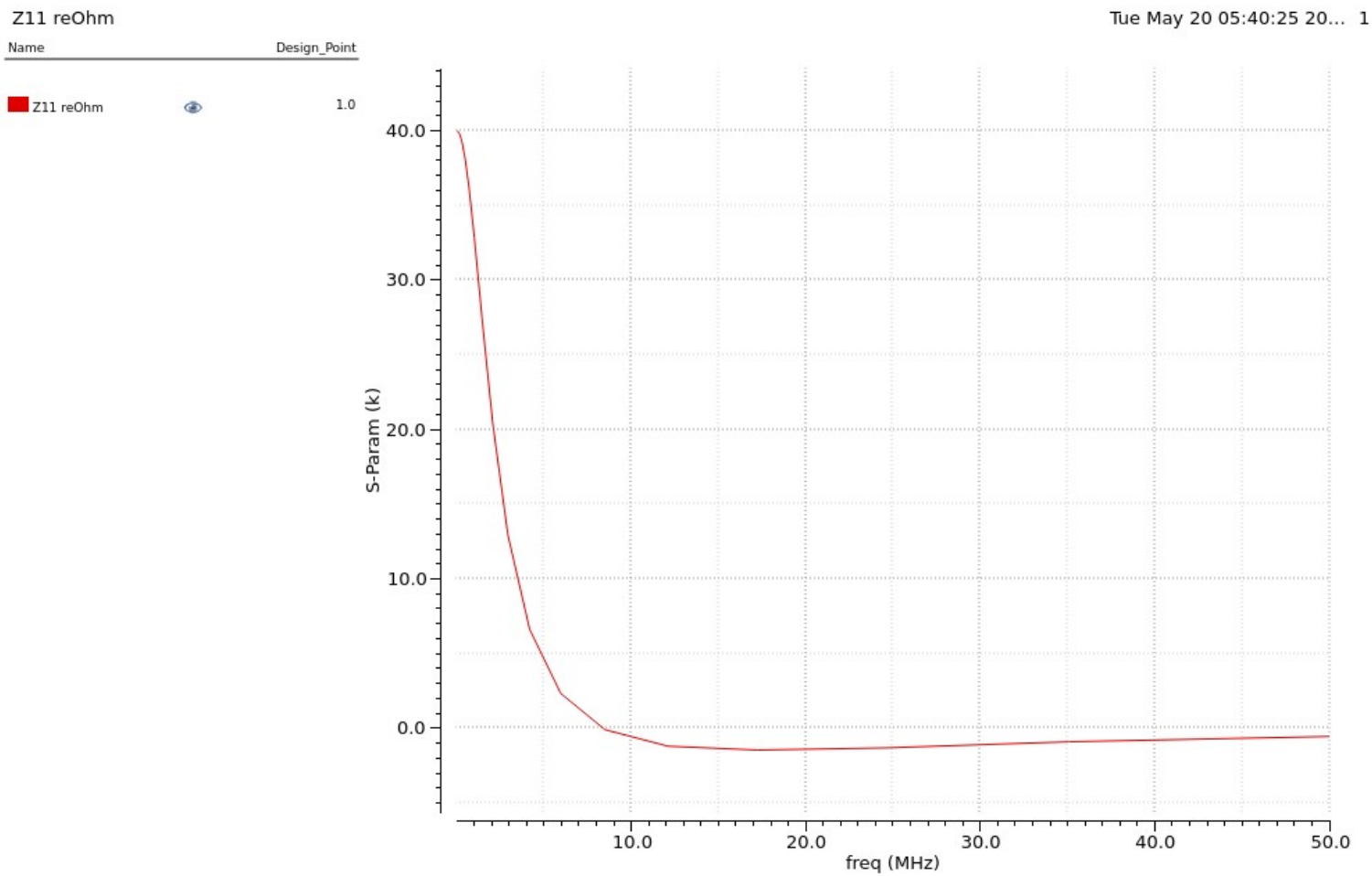


Figure: Impedance (real part) plot

Start up time

Once the internal losses of the crystal oscillator are over- come by the circuit's negative resistance, the oscillation ampli- tude grows exponentially from noise until it reaches a steady state. The time taken for this amplitude build-up, known as the start-up time, is a key parameter that impacts the oscillator's performance in timing and communication applications.

Start-Up Time for Oscillation

Energy in the inductor:

$$E = \frac{1}{2} L_m I^2$$

Differentiating:

$$\frac{dE}{dt} = L_m I \frac{dI}{dt} \tag{1}$$

$$P = R_{\text{net}} I_{\text{rms}}^2 = (|R_N| - R_m)\frac{I^2}{2} \tag{2}$$

Equating (1) and (2):

$$L_m I \frac{dI}{dt} = (|R_N| - R_m)\frac{I^2}{2} \Rightarrow \frac{dI}{I} = \frac{|R_N| - R_m}{2L_m} dt$$

Integrating:

$$\ln(I(t)) = \frac{|R_N| - R_m}{2L_m} t + c \Rightarrow I(t) = I_m(0)\, e^{\left(\frac{|R_N| - R_m}{2L_m}\right)t}$$

At $t = T_s$, $I(t) = I_{\text{target}}$:

$$T_s = \frac{2L_m}{|R_N| - R_m} \ln\left(\frac{I(t)}{I_m(0)}\right)$$

Start up time derivation

At steady-state:

$$V(t) = V_{DD}\sin(\omega t), \quad I(t) = C_T\frac{dV}{dt} = C_T\omega V_{DD}\cos(\omega t) \Rightarrow I_{\text{peak}} = C_T\omega V_D$$

For the detection of oscillation:

$$I_{\text{target}} = 0.9 \cdot I_{\text{peak}} = 0.9C_T\omega V_{DD}$$

Where:

$$C_T = \frac{C_1 C_2}{C_1 + C_2} + C_P$$

$$\boxed{T_s = \frac{2L_m}{|R_N| - R_m}\ln\left(\frac{0.9C_T\omega V_{DD}}{I_m(0)}\right)}$$

Optimized g_m for Maximum R_N

To maximize negative resistance:

$$R_N = \frac{g_m C_1 C_2}{\omega^2 (C_1 C_2 + C_1 C_P + C_2 C_P)^2 + g_m^2 C_P^2}$$

Differentiate R_N w.r.t. g_m using quotient rule and set derivative to zero:

$$C_1 C_2 \left[(g_m C_P)^2 + \omega^2 (C_1 C_2 + C_1 C_P + C_2 C_P)^2 \right] - g_m C_1 C_2 \left[2 g_m C_P^2 \right] = 0$$

Simplifying:

$$\omega^2 (C_1 C_2 + C_1 C_P + C_2 C_P)^2 = g_m^2 C_P^2$$

Taking the square root:

$$\therefore \boxed{g_{m,\text{opt}} = \omega \left(\frac{C_1 C_2 + C_1 C_P + C_2 C_P}{C_P} \right)}$$

Start-Up Time at Optimized g_m

Substitute $g_{m,\text{opt}}$ into R_N to get:

$$R_{N,\text{max}} = \frac{1}{2\omega C_P \left(1 + \frac{C_P(C_1+C_2)}{C_1 C_2}\right)}$$

Now substituting $R_{N,\text{max}}$ into the start-up time equation:

$$T_s = \frac{2L_m}{\left(\frac{1}{2\omega C_P \left(1+\frac{C_P(C_1+C_2)}{C_1 C_2}\right)} - R_m\right)} \ln\left(\frac{0.9 C_T \omega V_{DD}}{I_m(0)}\right)$$

Where:

$$C_T = \frac{C_1 C_2}{C_1 + C_2} + C_P$$

Total Energy During Start-Up

Total energy drawn from supply:

$$E = P \cdot t = V_{DD} \cdot I_D \cdot T_s$$

where I_D is the supply current drawn by the XO.

Expression for drain current:

$$I_D = \frac{\mu C_{ox} \omega}{2L}(V_{GS} - V_{th})^2$$

Transconductance of the transistor:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{\mu C_{ox} \omega}{L}(V_{GS} - V_{th}) \Rightarrow V_{ov} = V_{GS} - V_{th}$$

Using g_m and V_{ov}:

$$I_D = \frac{1}{2}\left[\frac{\mu C_{ox} \omega}{L}(V_{GS} - V_{th})\right](V_{GS} - V_{th}) = \frac{1}{2} g_m V_{ov}$$

$$\boxed{I_D = \frac{1}{2} g_m V_{ov}}$$

Voltage Variation Due to Switching Capacitors

Initial charge before switching:

$$Q_0 = C_0 V_0$$

When an additional capacitor C_u is switched in (charge conserved):

$$C_{\text{new}} = C_0 + C_u \quad \Rightarrow \quad Q_0 = (C_0 + C_u)V$$

Solving for new voltage:

$$V = \frac{C_0 V_0}{C_0 + C_u} = V_0 \left(\frac{1}{1 + \frac{C_u}{C_0}} \right)$$

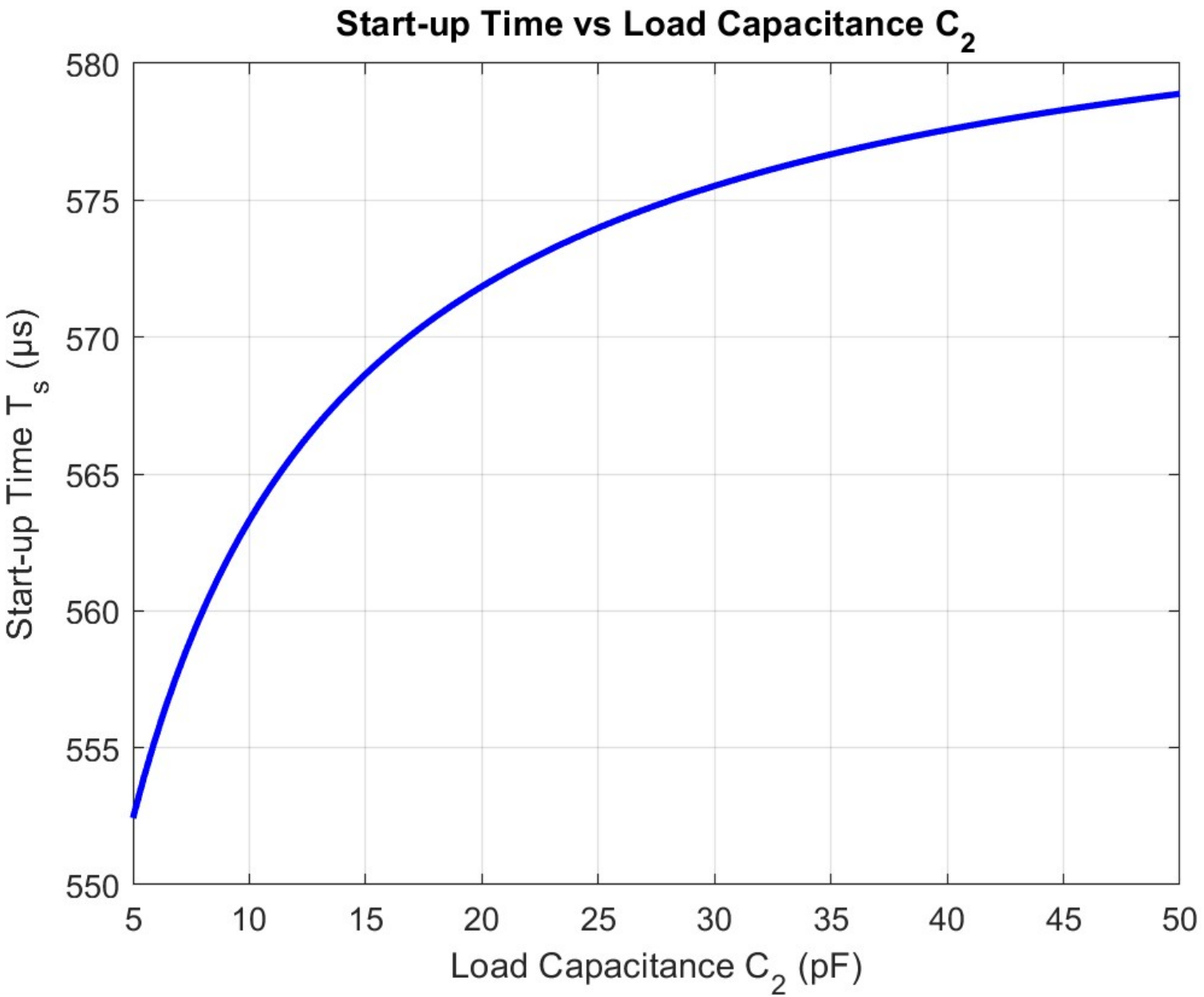
Voltage drop due to switching:

$$\Delta V = V_0 - V = V_0 \left(1 - \frac{1}{1 + \frac{C_u}{C_0}} \right) = V_0 \left(\frac{\frac{C_u}{C_0}}{1 + \frac{C_u}{C_0}} \right)$$

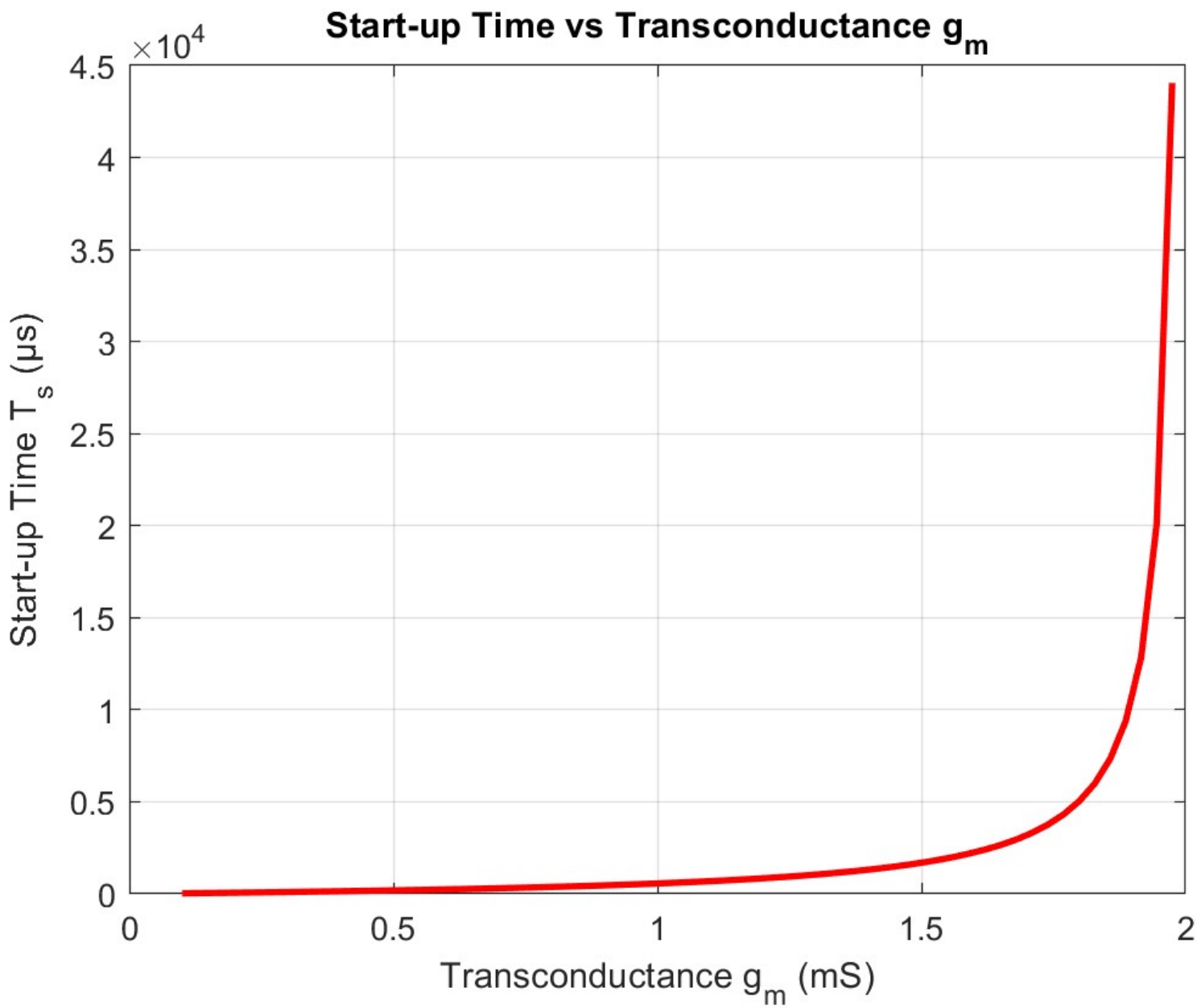
Or equivalently:

$$\boxed{\Delta V = V_0 \left(\frac{1}{1 + \frac{C_0}{C_u}} \right)}$$

Startup Time vs Load Capacitance



Startup Time vs Transconductance



Negative Resistance vs Load Capacitance

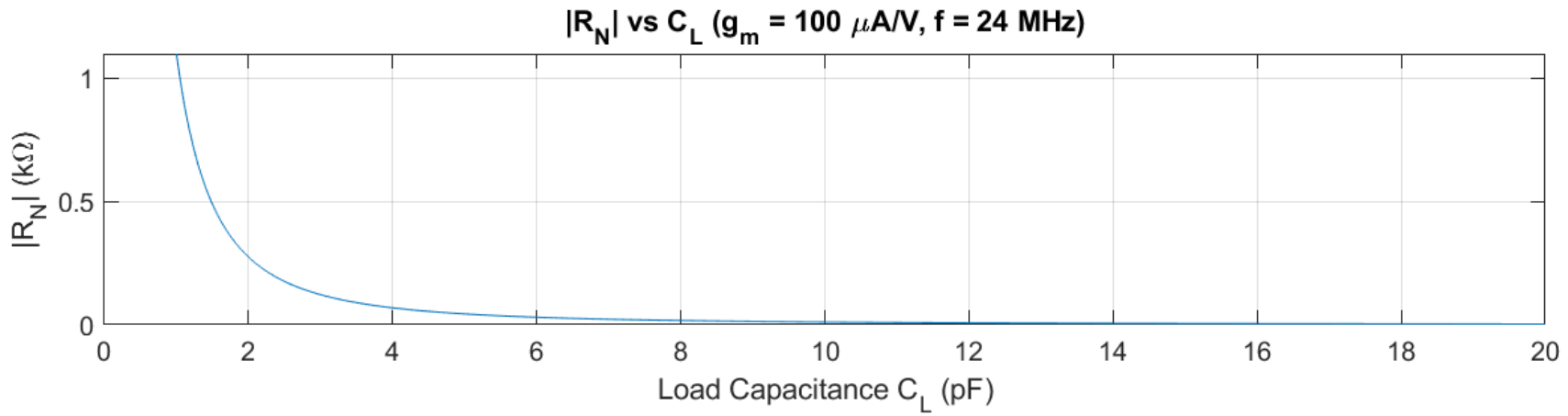


Figure: Negative Resistance vs Load Capacitance

Negative Resistance vs Transconductance

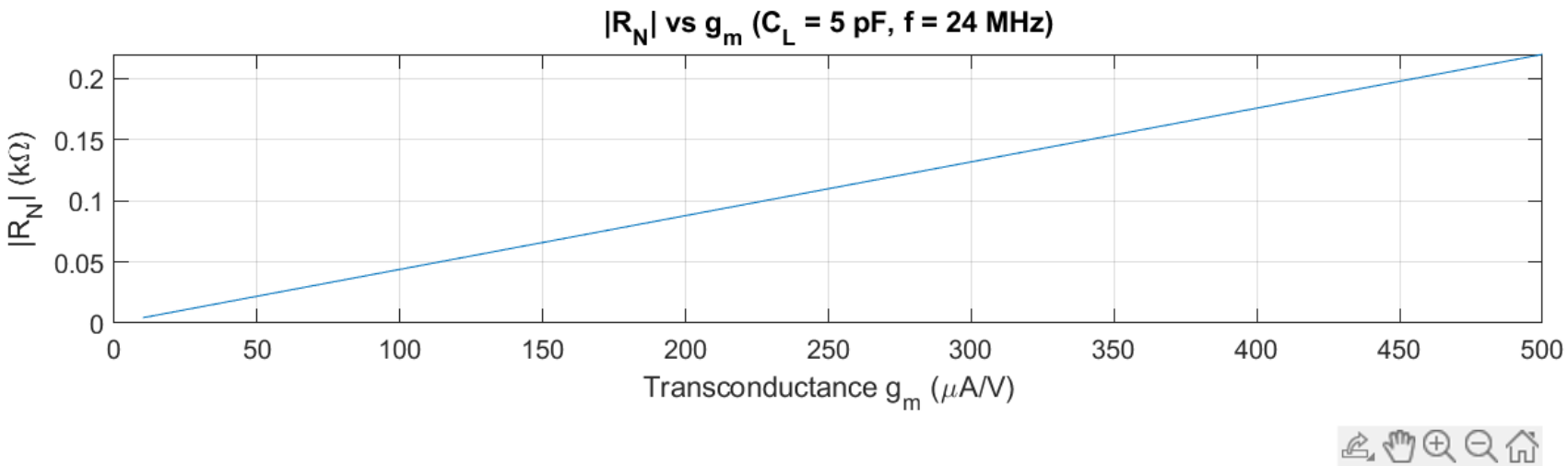


Figure: Negative Resistance vs Transconductance

Negative Resistance vs Frequency

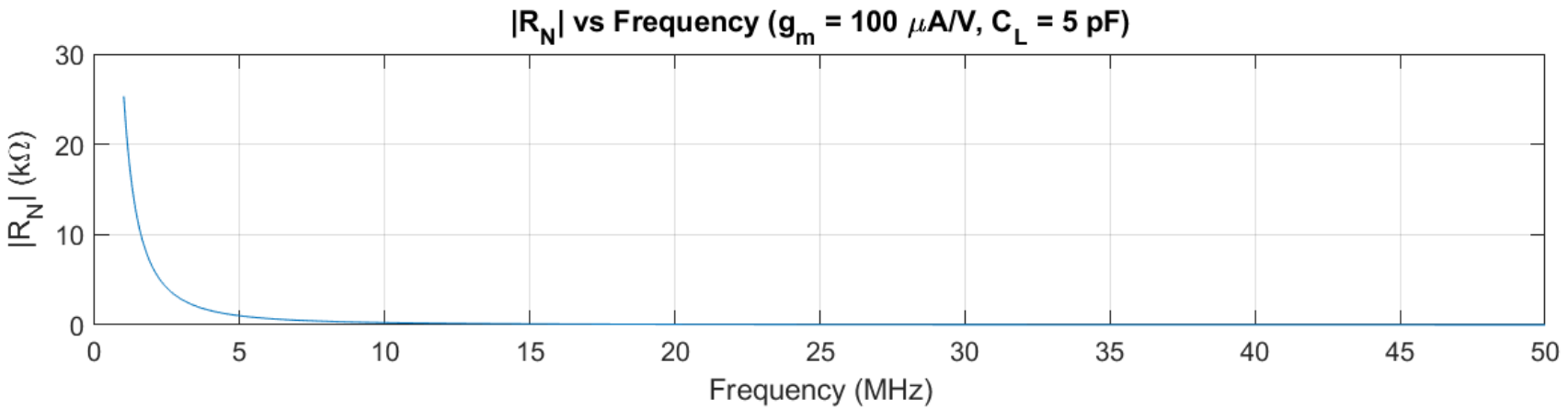


Figure: Negative Resistance vs Frequency

DAL Architecture: Detection and Cap Bank Control

- **Objective:** Achieve fast start-up and low steady-state power in a crystal oscillator.
- **Clock Detection:**
  - A **Clock Detector** monitors oscillator output.
  - Combines an **Envelope Detector** and a **Digital Detector**.
  - Detects when stable oscillation begins.
- **Capacitor Bank Activation:**
  - Detection triggers the activation of digitally controlled capacitor banks.
  - Uses two 8×8 switched-capacitor arrays: C_{1a} and C_{2a}.
  - Placed across XON and XOP terminals.
  - Enables precise, stepwise tuning of load capacitance.

DAL Architecture: Current Scaling and FSM

- **Adaptive Current Scaling:**
  - Controlled by switches $S\langle 0\rangle$ to $S\langle 3\rangle$.
  - Current sources activated in steps: $1\times$, $2.5\times$, $2.5\times$, $5\times$, $10\times$, and $20\times$.
  - Helps boost start-up current initially, then reduce for power savings.
- **Finite State Machine (FSM):**
  - Coordinates actions of the DAL loop.
  - Takes input from the envelope and digital detectors.
  - Controls capacitor bank and current scaling logic.
- **DAL Loop Summary:**
  - Feedback-based autonomous control system.
  - Optimizes oscillator startup and minimizes steady-state energy use.

Oscillator

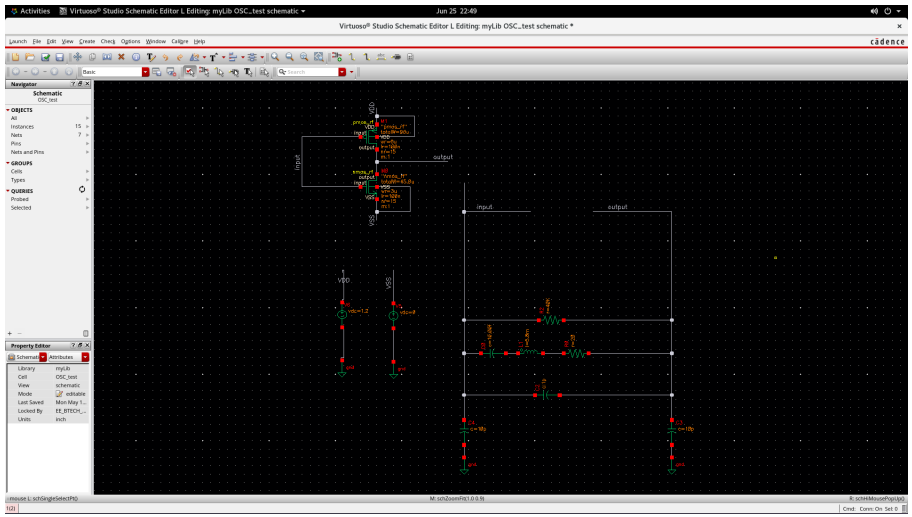


Figure: Pierce Oscillator Schematic

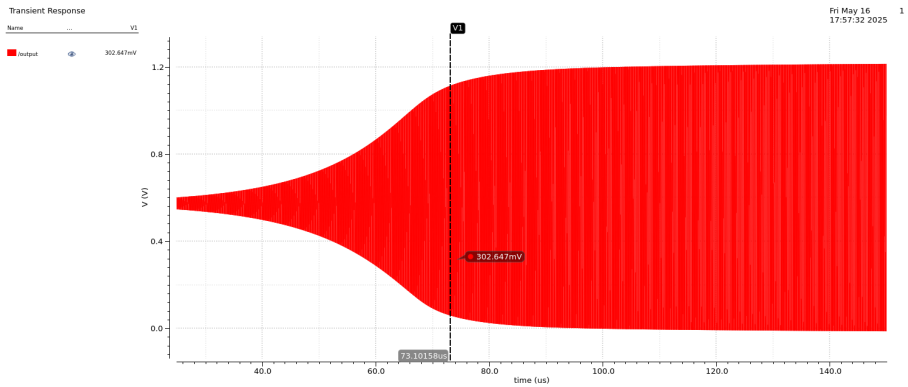


Figure: Simulation Output

Oscillator

- The oscillator replaces a crystal with an RLC network in parallel with C_P, along with discrete capacitors C_1 and C_2.
- The RLC network emulates the resonant behavior and energy storage characteristics of a quartz crystal.
- Capacitors C_1 and C_2 are connected from each terminal of the RLC network to ground, forming a capacitive voltage divider.
- This configuration introduces the necessary phase shift for the feedback loop.
- The RLC + C_1, C_2 network acts as a frequency-selective path in the feedback of a CMOS inverter.
- At startup, internal noise is amplified and filtered by the RLC network.
- Oscillations are sustained only at the resonant frequency; all others are attenuated.
- The Barkhausen criteria (loop gain 1 and phase shift = 0 or 360 degrees) are satisfied through the amplifier and feedback network.
- The result is a stable sinusoidal output at the RLC's resonant frequency, mimicking a crystal oscillator in fully-integrated designs.

Current Mirroring with PMOS

- A current mirror replicates a reference current into other branches, acting as a precise current source or sink.
- Widely used in biasing circuits of analog blocks like amplifiers, differential pairs, and op-amps.
- Operates on the principle that matched transistors biased with the same V_{GS} and in the saturation region will mirror current proportionally to their W/L ratios.
- In a PMOS current mirror:
  - Sources are connected to V_{DD}.
  - Reference PMOS is diode-connected (gate and drain shorted).
  - This gate voltage is shared with output PMOS transistors.
  - Ensures all transistors experience the same V_{GS}, enabling current mirroring.

Current Mirroring with PMOS

To improve oscillator performance:

- Start-up time and power efficiency are optimized using current scaling via switched PMOS mirrors.
- Begins with a base reference current of 23μA.
- Additional branches scale current using factors of: $1.25\times$, $1.25\times$, $2.5\times$, $5\times$, and $10\times$.
- Resulting in mirrored currents: 69μA, 69μA, 139μA, 280μA, and 535μA.
- Total current is close to 1.1 mA when all switches are on.

This strategy supports fast oscillator start-up while maintaining low steady-state power consumption.

D Flip-Flop: Circuit Overview

- This schematic implements a CMOS D Flip-Flop using transmission gates and inverter-based master-slave latches.
- It consists of:
  - Two cross-coupled inverters forming master and slave latches.
  - Transmission gates controlled by CLK and its complement.
- Operation:
  - When CLK is high, the master latch captures the input D.
  - When CLK goes low, the slave latch transfers the stored value to output Q, making it edge-triggered.

circuit overview

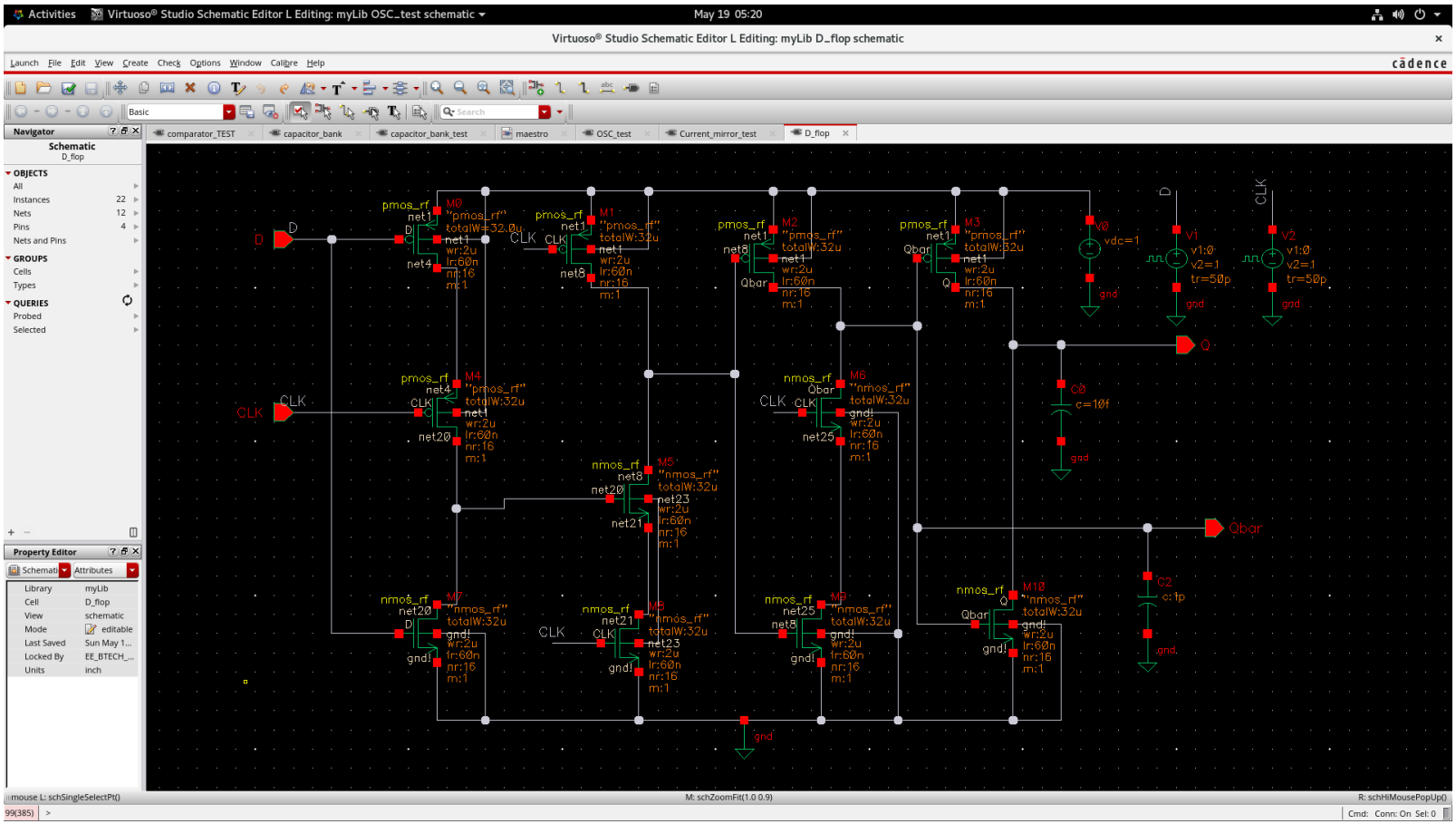


Figure: Transistor-Level Design of D Flip-Flop

D Flip-Flop: Simulation Output

- Simulation confirms correct master-slave DFF behavior.
- The output Q changes only at the falling edge of CLK, reflecting the input D.
- The complementary output $\overline{Q}$ maintains opposite logic.
- Rise/fall times, propagation delay, and setup/hold time characteristics can be analyzed from the waveform.

Frequency Divider: Operation

- This is a divide-by-4 (f/4) frequency divider using two positive-edge-triggered D Flip-Flops in series.
- Each DFF has a feedback loop from $\overline{Q}$ to D, making it behave like a toggle flip-flop.
- Operation:
  - First DFF toggles at every rising edge of input clock $f_{\text{in}} \rightarrow$ divides frequency by 2.
  - Its output becomes the clock for the second DFF, which again divides by 2.
  - Final output: $f_{\text{out}} = \frac{f_{\text{in}}}{4}$
- The result is a clean square wave output with one-fourth the frequency of the original input clock.

Frequency Divider: Circuit & Simulation

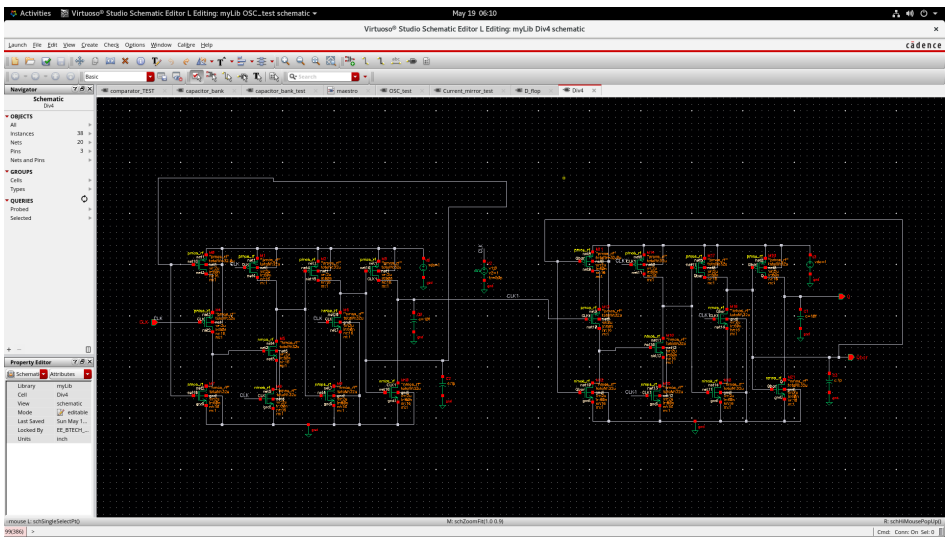


Figure: Schematic

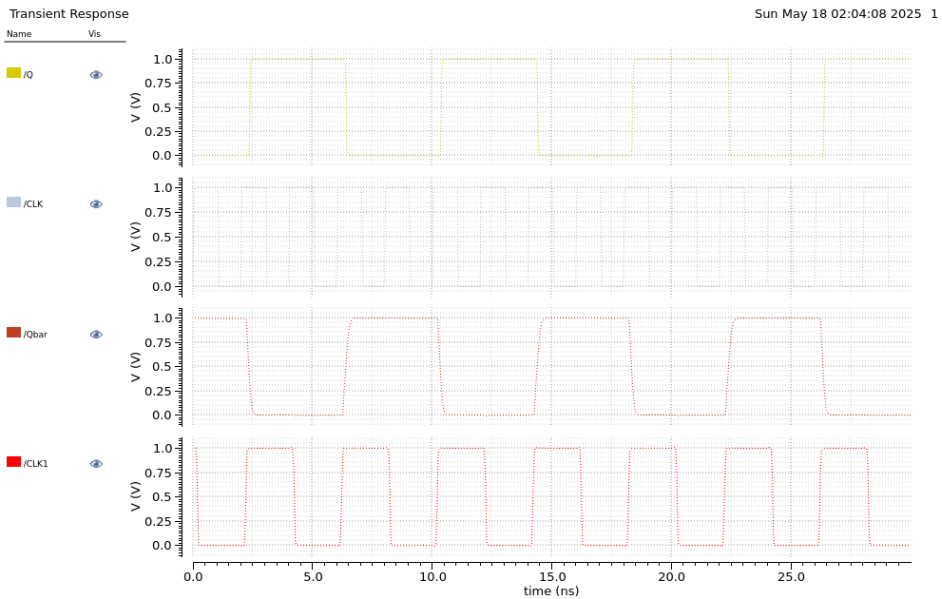


Figure: Simulation Output

Envelope

- An envelope detector is an analog circuit used to extract the envelope of an amplitude-modulated (AM) signal.
- It typically consists of:
  - A diode (for rectification)
  - A resistor-capacitor (RC) low-pass filter
- Operation:
  - The diode rectifies the signal, passing only positive half-cycles.
  - The capacitor charges quickly to signal peaks and discharges slowly through the resistor.
- This charging-discharging behavior allows the output to follow the envelope of the AM waveform.
- The RC time constant is chosen to:
  - Filter out the high-frequency carrier
  - Accurately track slower envelope variations

Comparator

- After envelope detection, a comparator is used to convert the analog envelope into a digital signal.
- The comparator is typically implemented using an operational amplifier in open-loop mode.
- It compares the envelope signal to a fixed reference voltage (V_{ref}).
- Operation:
  - If the envelope signal $> V_{\text{ref}} \rightarrow$ output is high (logic 1).
  - If the envelope signal $< V_{\text{ref}} \rightarrow$ output is low (logic 0).
- This digitized signal enables:
  - Event detection
  - Pulse counting
  - Signal timing and further digital processing

Envelope Detector and Comparator circuit

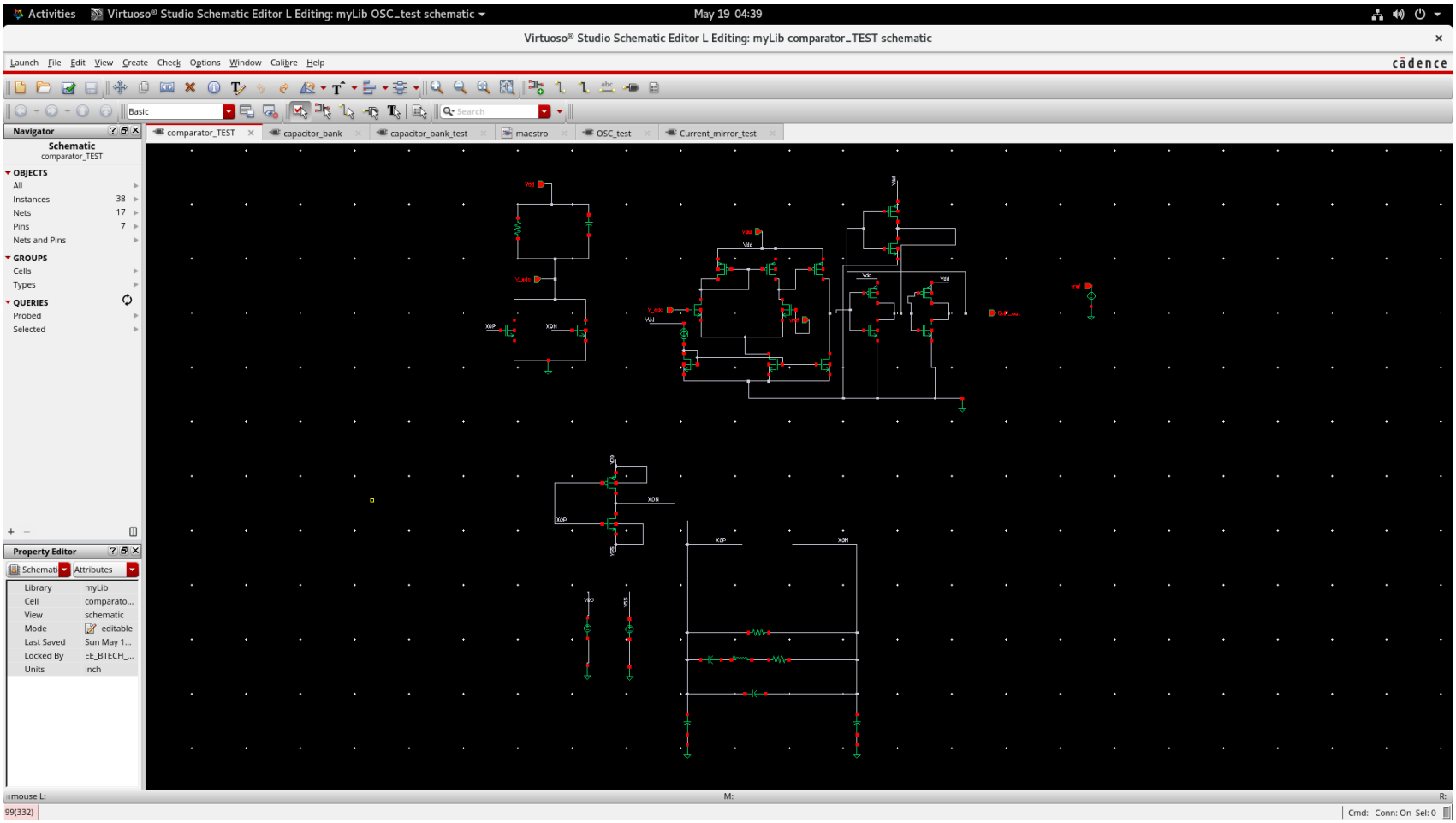


Figure: Schematic of Envelope Detector and Comparator Circuit

Capacitor Bank Logic and Implementation

- A digitally controlled capacitor bank enables programmable control of load capacitance in the oscillator.
- The design is based on a **binary-weighted architecture**.
- A **4-bit synchronous counter** (built from edge-triggered D flip-flops) is used to select capacitance values in binary steps.
- The counter remains idle during rest conditions and activates only upon receiving a control pulse.
- This control pulse is generated by a **comparator circuit** that monitors oscillator amplitude or stability.
- Capacitance scaling occurs only when the oscillator is ready to transition from startup to steady-state operation.

Capacitor Bank – Mechanism

- Comparator output is connected to the **clock input** of a digital counter.
- The counter drives an array of **MOSFET switches** to connect or disconnect capacitors selectively.
- Capacitors are **binary weighted**: 4 pF, 8 pF, 16 pF, and 32 pF.
- Total capacitance tunable from **0 pF to 60 pF** in **4 pF steps**.
- At startup, only the **4 pF capacitor** is connected to reduce load and enable faster oscillation.

Capacitor Bank

- As the counter increments, more capacitors are progressively added in **binary fashion**.
- This leads to a smooth increase in capacitance, enabling:
  - **Frequency stabilization**
  - **Improved phase noise**
- Binary-weighted architecture ensures:
  - **High linearity**
  - **Low area overhead**
- **Event-driven activation** (via comparator) avoids unnecessary switching during transients.
- Well-suited for **low-power precision timing applications**.

Capacitor Bank

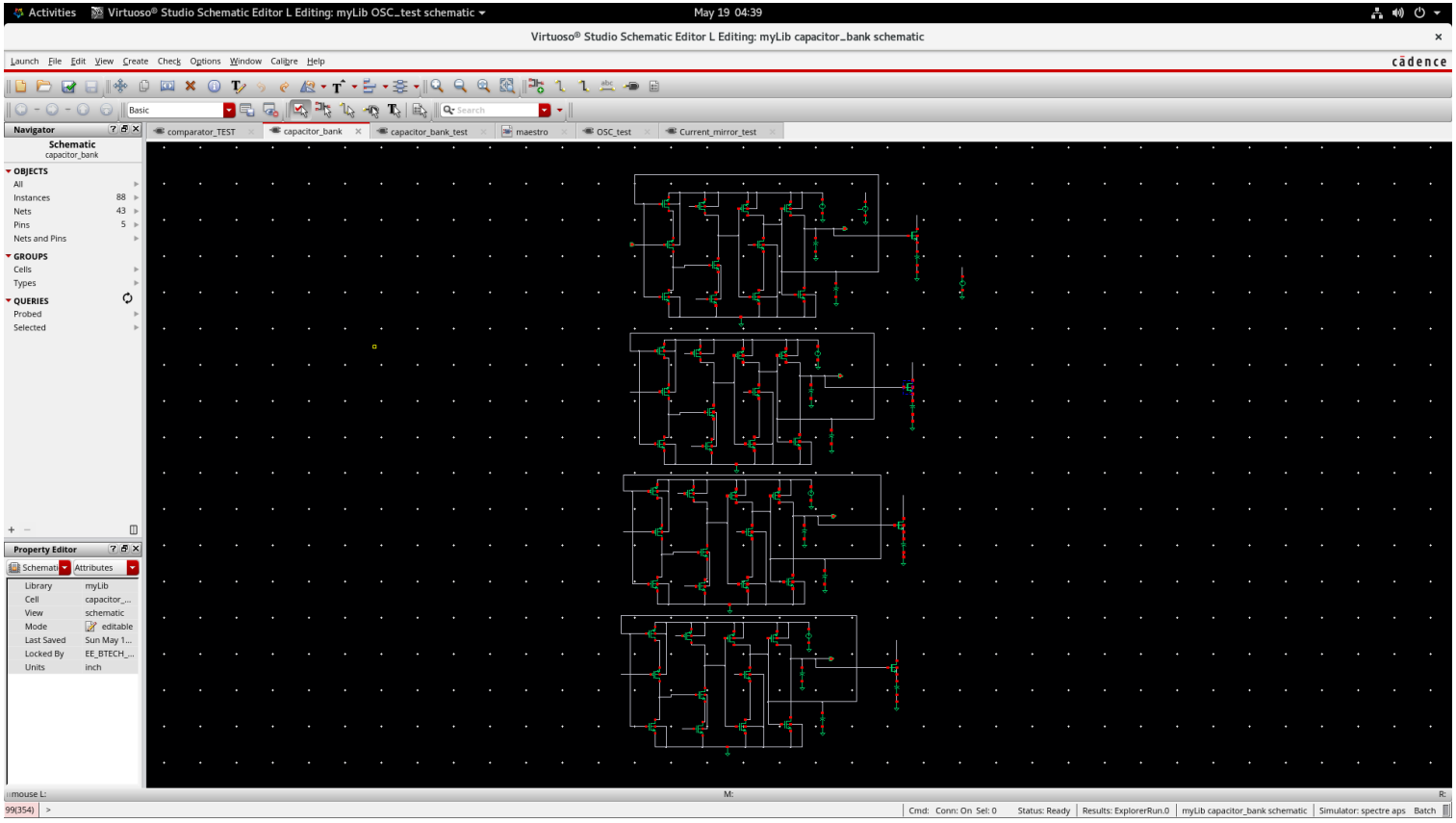


Figure: Capacitor Bank

Capacitor Bank Simulation

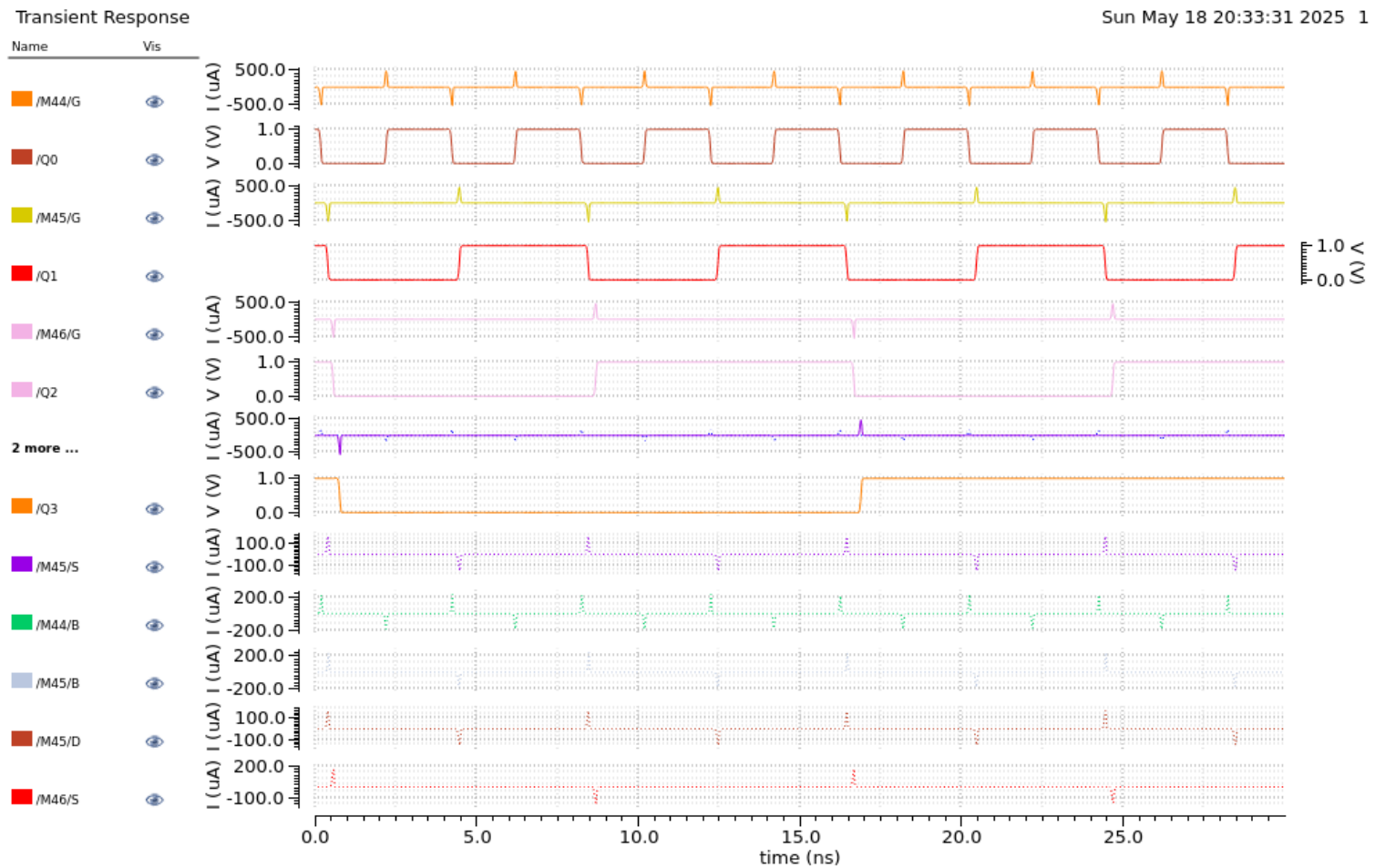


Figure: Capacitor Bank Simulation

Simulation results - Introduction

- We shall discuss in detail the capacitors in the bank.
- Capacitors used: 4pF, 8pF, 16pF, and 32pF.
- The simulation results are shown in the following slides.

Simulation: 4pF Capacitor

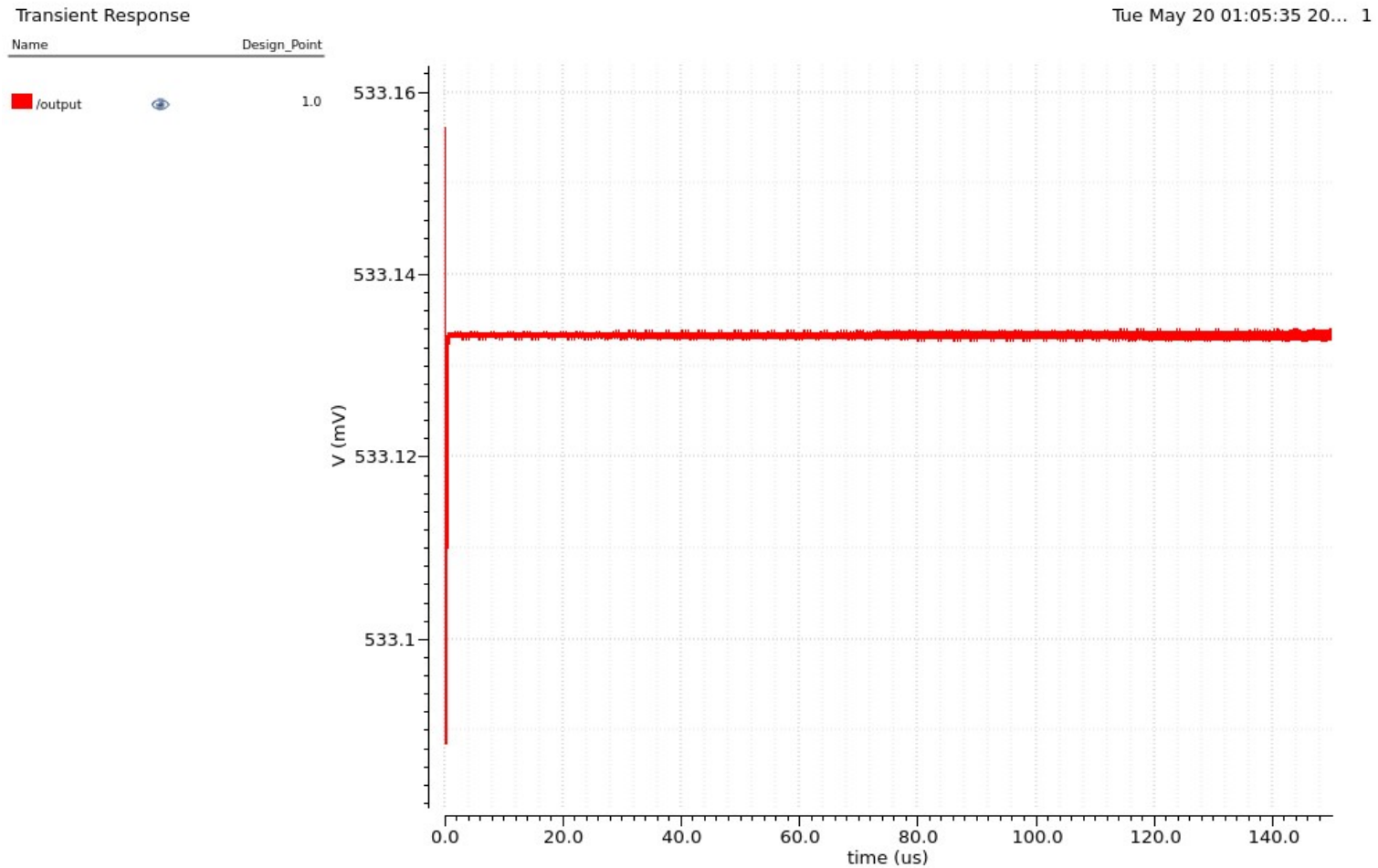


Figure: Simulation of 4pF capacitor

Simulation: 8pF Capacitor

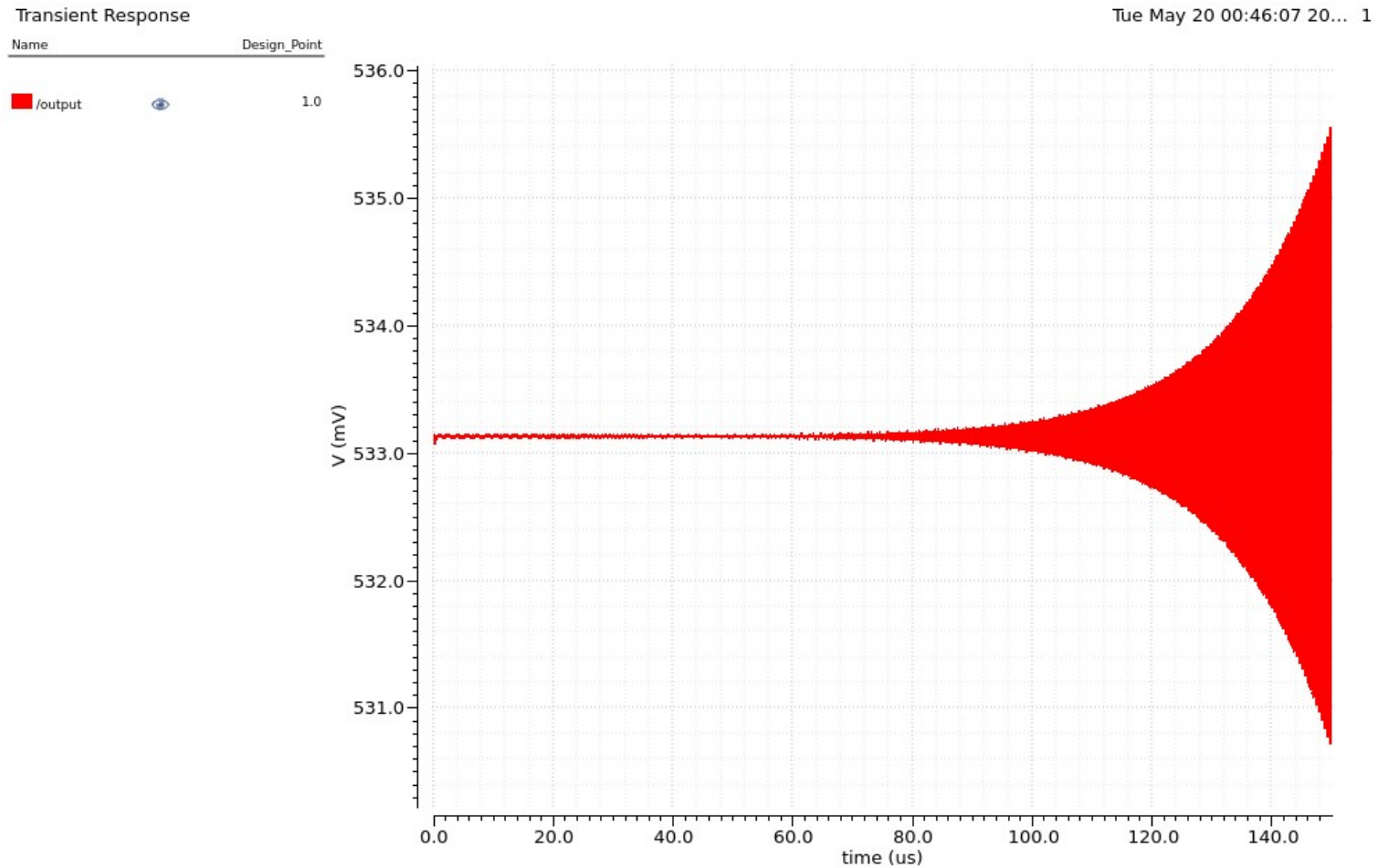


Figure: Simulation of 8pF capacitor

Simulation: 16pF Capacitor

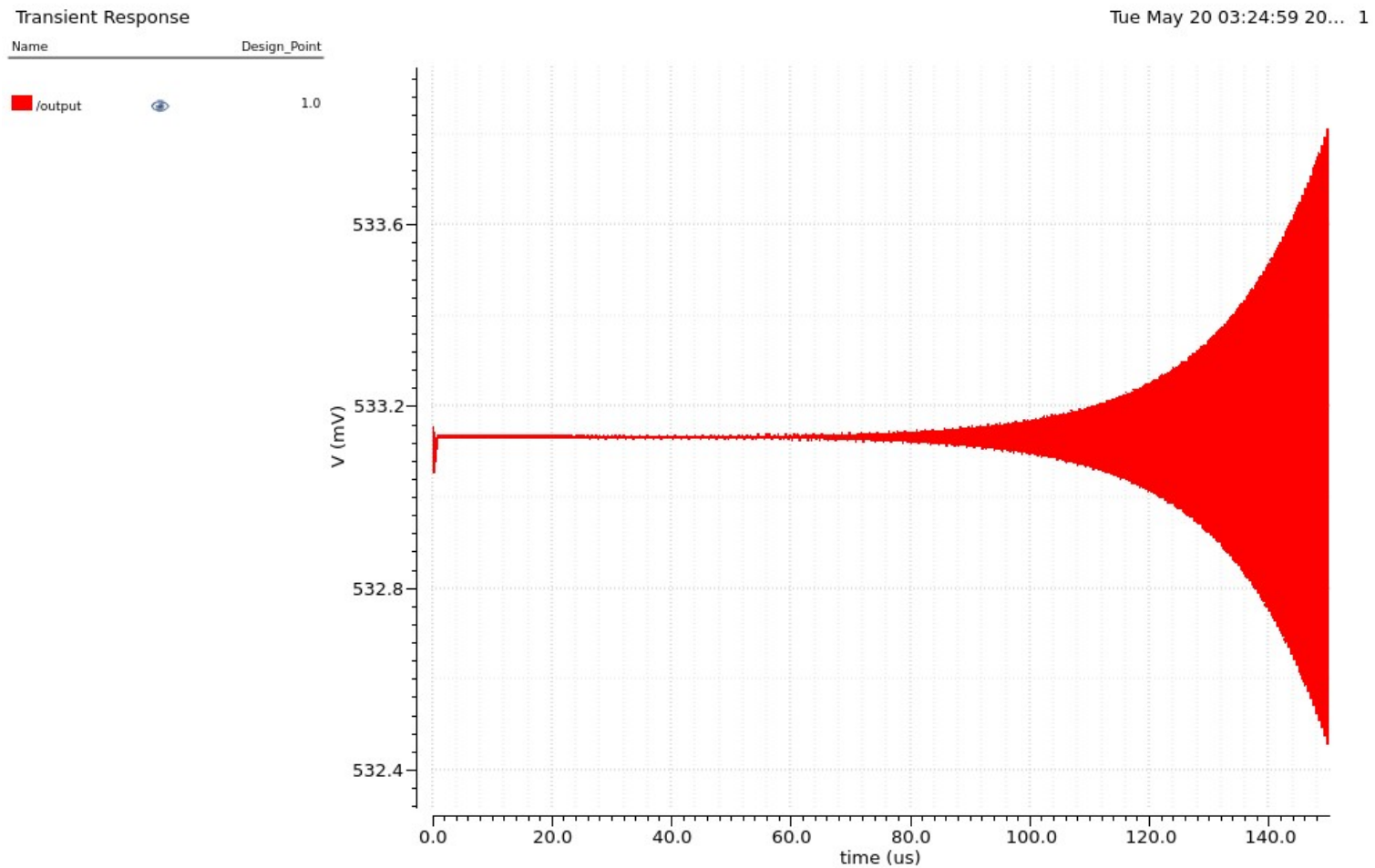


Figure: Simulation of 16pF capacitor

Simulation: 32pF Capacitor

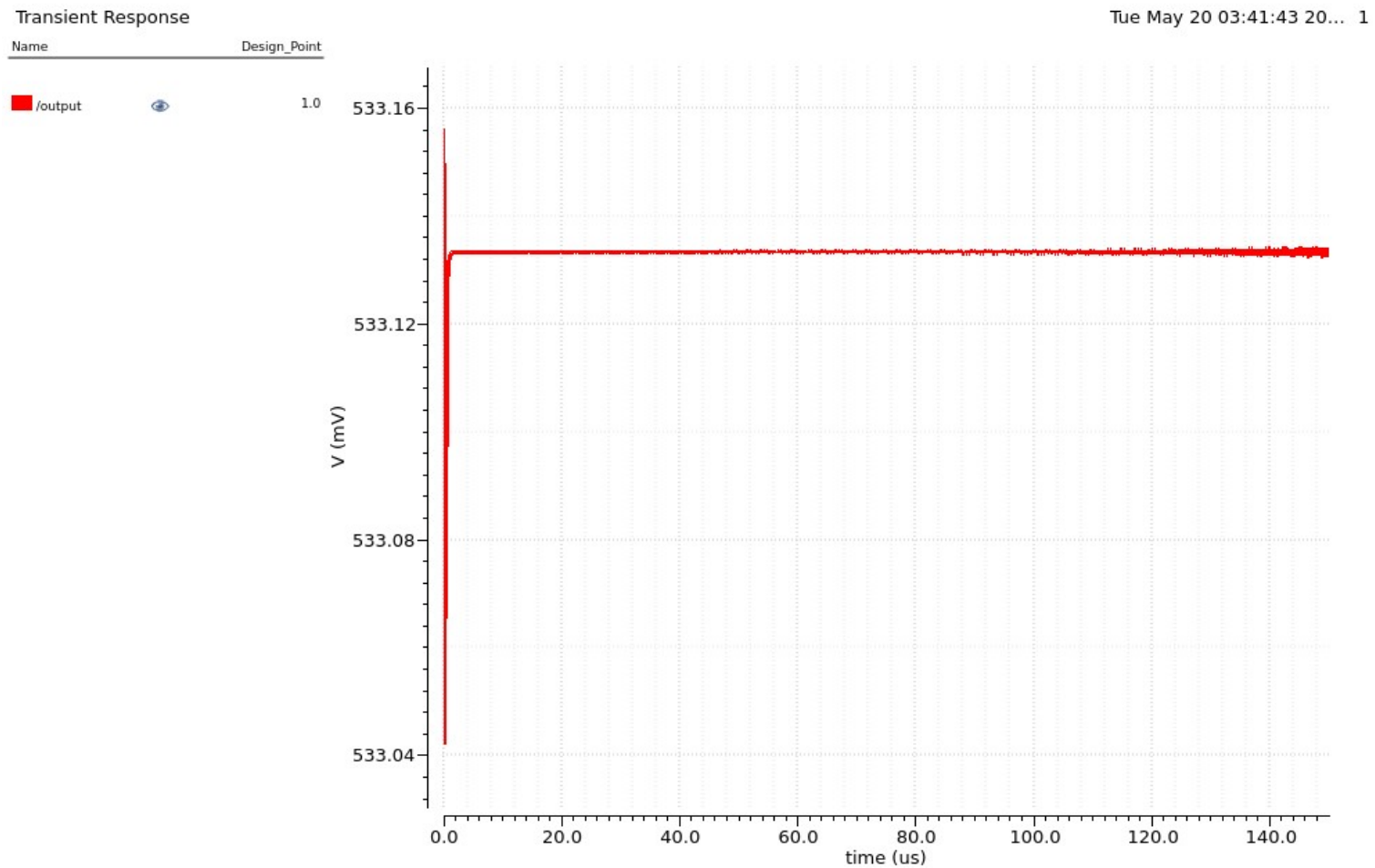


Figure: Simulation of 32pF capacitor

Minimum Current Test – 4pF

- 4pF doesn't oscillate with all current sources on.
- Each mirror tested individually to find minimum.
- Minimum current found: 69 μA.

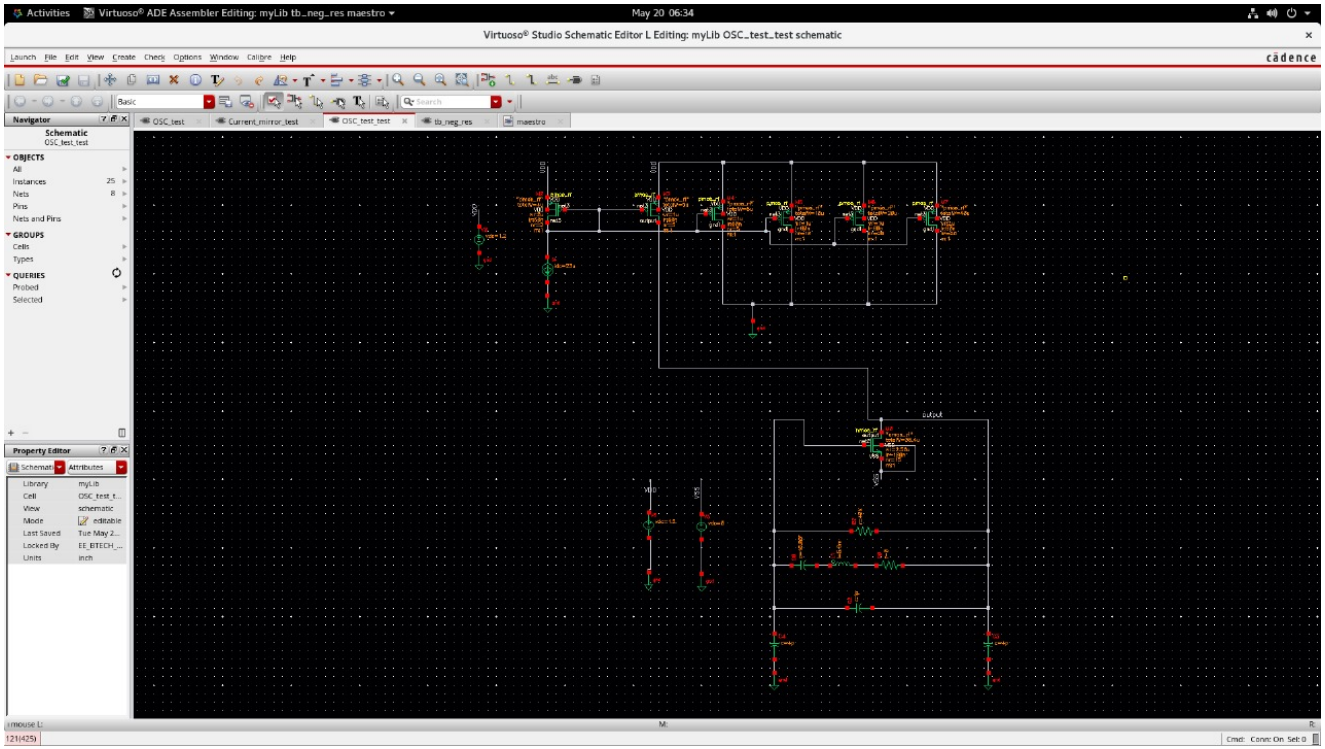


Figure: Setup to find minimum current using current mirror (4pF)

Simulation: 4pF at Minimum Current

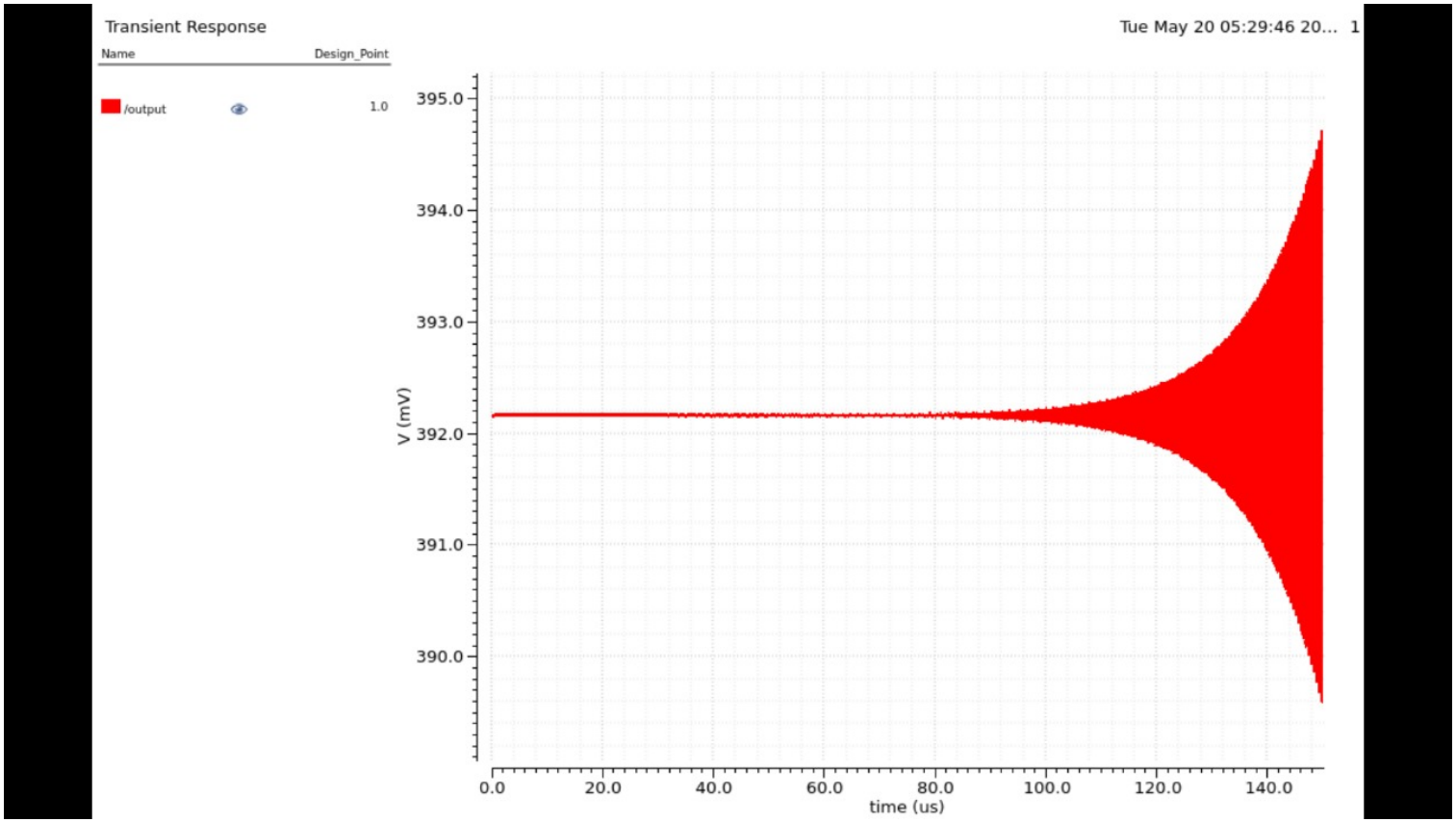


Figure: Simulation of 4pF with 69 μA current

Minimum Current Test – 8pF

- Oscillations observed with all current sources.
- Minimum current needed: 69 μA (first mirror).

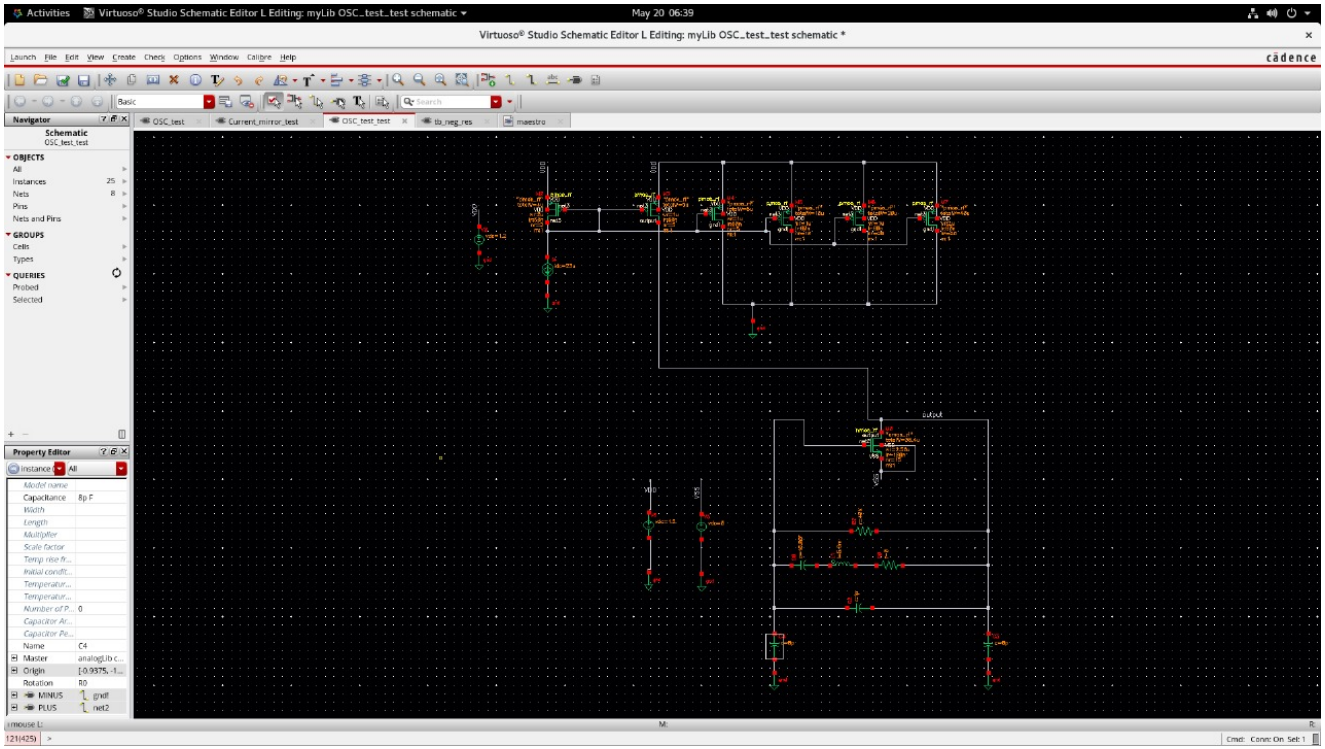


Figure: Setup for minimum current test (8pF)

Simulation: 8pF at Minimum Current

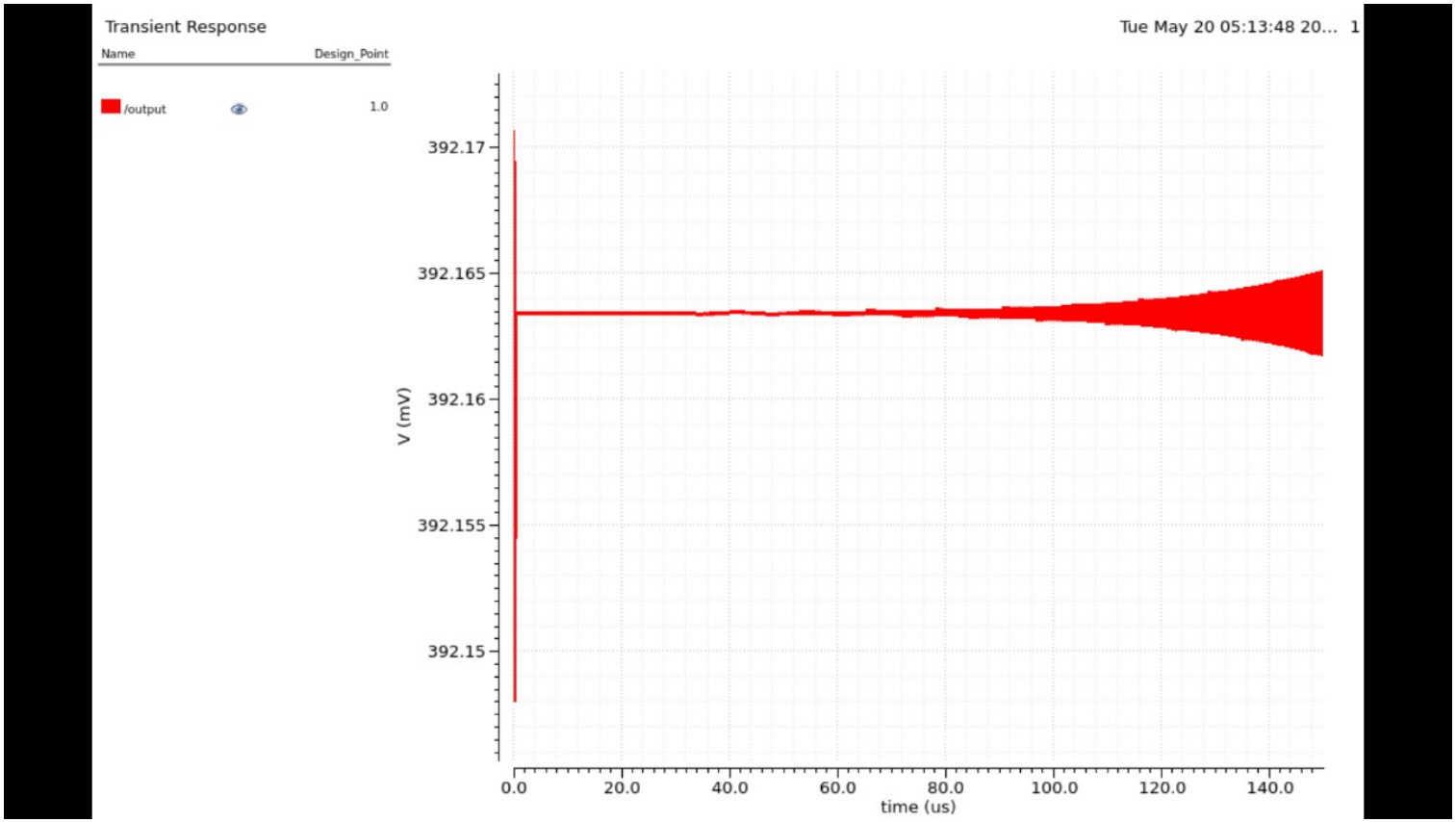


Figure: Simulation of 8pF with 69 μA current

Minimum Current Test – 16pF

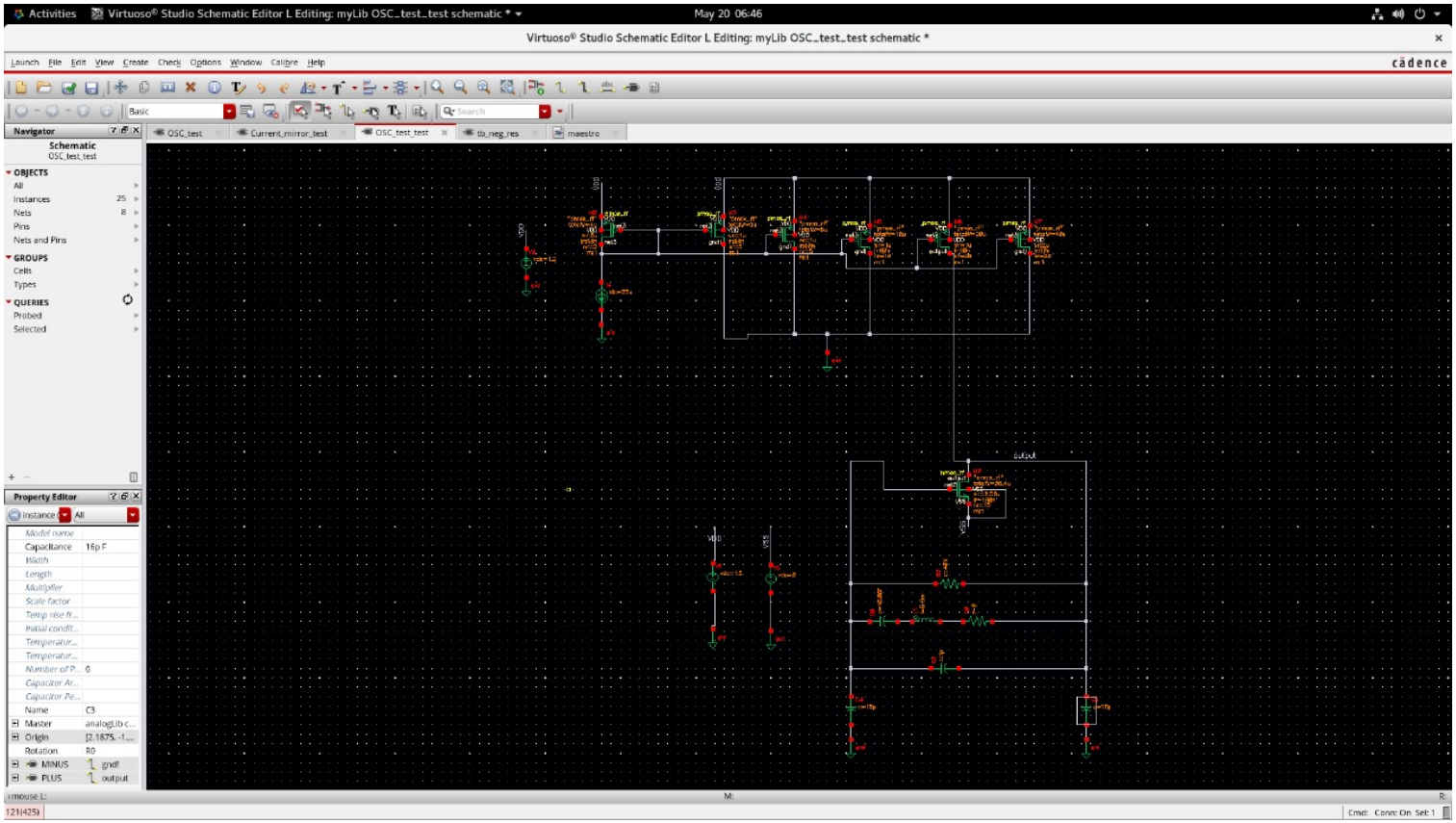


Figure: Setup for minimum current test (16pF)

Simulation: 16pF at Minimum Current

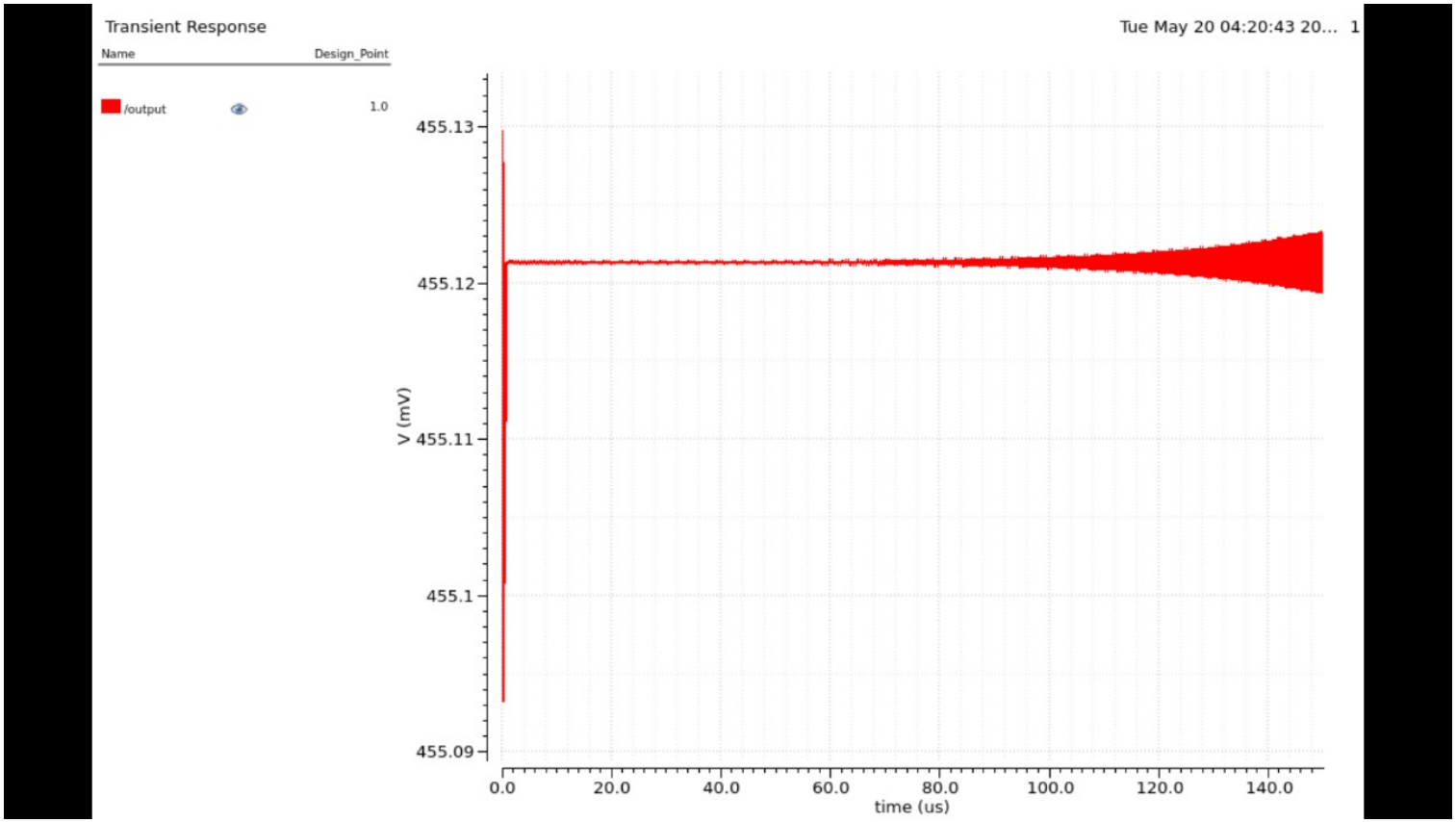


Figure: Simulation of 16pF with current source

Capacitor Bank Overview

- Capacitors used in the bank: 4pF, 8pF, 16pF, and 32pF.
- Oscillations are observed for 8pF and 16pF.
- No oscillations observed for 4pF and 32pF.

Conclusion

The DAL method achieves a fast, low-power start-up of crystal oscillators. It is fully automatic, simple to integrate, robust to variations, and ready for practical use in IoT applications- cations where duty-cycling is heavy and the power budget is very tight.