

PCB Design Assignment

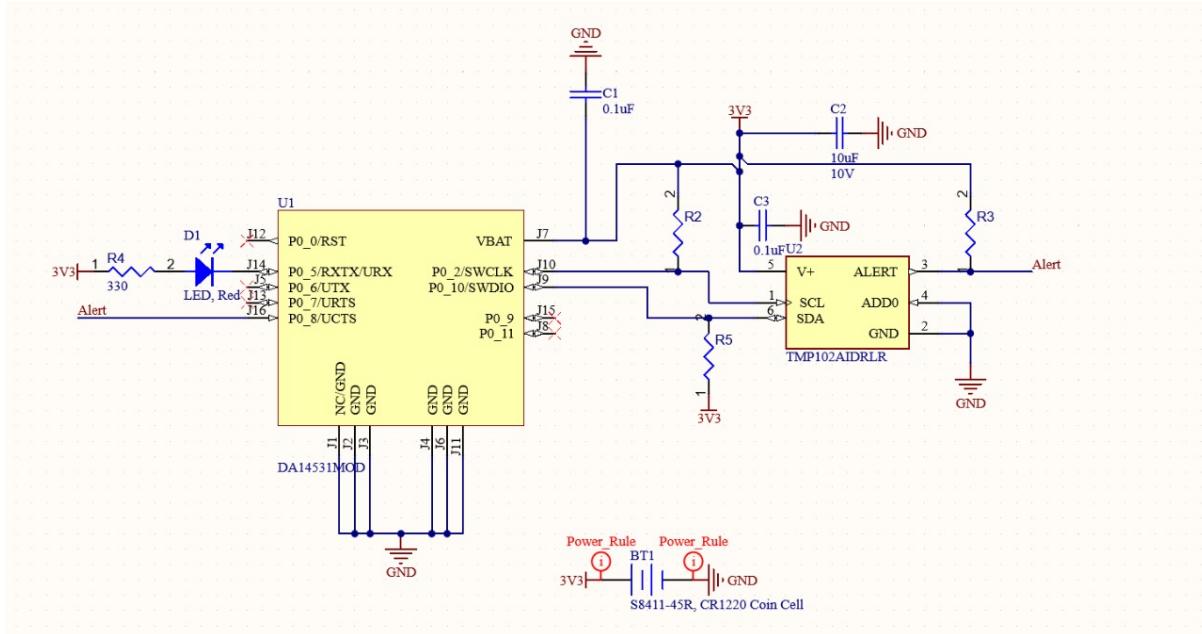
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Section - Easy

1. Temperature Monitoring System

Design a temperature monitoring circuit using the DA14531 MCU and an I²C temperature sensor (e.g., TMP102). Include proper power supply filtering, decoupling capacitors, and I²C pull-up resistors. The circuit should include an LED indicator that toggles when temperature exceeds a threshold.

Schematic:



Temperature monitoring system Schematic

0.1 Hardware Design

- **Power:** VBAT → decoupling ($C_1 = 0.1 \mu F$, $C_2 = 10 \mu F$).
- **I²C pull-ups:** R2, R5 to 3V3.
- **TMP102:** ADD0 address pin, ALERT → P0_9.
- **MCU (DA14531):** P0_1 SDA, P0_2 SCL, P0_8 LED out, P0_9 ALERT in.
- **LED indicator:** D1.

0.2 Component Selection

- **DA14531:** Ultra-low-power BLE MCU (key specs).
- **TMP102:** Digital I²C sensor ($\pm 0.5^\circ\text{C}$ accuracy, 12-bit).
- **Passives:** 0.1 μF decoupling close to VCC pins, 10 μF bulk for stability.

Components

- **DA14531 MCU (U1):** A Bluetooth Low Energy (BLE) microcontroller from Dialog Semiconductor.
- **TMP102 (U2):** A digital temperature sensor with an I²C interface.
- **LED (D1):** Indicates when temperature exceeds a defined threshold.
- **Capacitors (C1, C2, C3):** Used for power supply filtering and decoupling.
- **Resistors (R2, R3):** I²C pull-up resistors.
- **Resistor (R4):** Current limiting resistor for the LED.
- **Battery (BT1):** Powers the system (3V coin cell).

Working Principle

Power Supply: The system is powered by a 3.3V coin cell battery. Decoupling capacitors (C1 = 0.1 μF , C2 = 10 μF , C3 = 0.1 μF) are used to stabilize the voltage and suppress noise.

I²C Communication: The TMP102 communicates with the DA14531 MCU over the I²C bus via SCL and SDA lines. Pull-up resistors R2 and R3 ensure the lines are properly biased.

Temperature Monitoring: TMP102 measures ambient temperature and sends the data digitally to the MCU via I²C. When the temperature exceeds a predefined threshold, the ALERT pin of TMP102 goes LOW.

Alert Mechanism and LED Indication: The ALERT pin is connected to both the MCU and an LED. When the ALERT pin goes LOW:

- The MCU detects the change and can toggle the LED.
- Alternatively, the LED can be lit directly by the ALERT pin sinking current.

I²C Address Configuration: The ADD0 pin of TMP102 is tied to GND, which sets its I²C address.

Summary

- TMP102 senses temperature and communicates with the MCU via I²C.
- If the temperature exceeds the threshold, TMP102 pulls the ALERT line LOW.
- The LED is activated to indicate the condition.
- The MCU may also process or transmit the temperature data as needed.

0.3 Approach:

- We made a Schematic as shown in the above figure using the data sheets of DA14531 and TMP102.
- We made the connection of the components and the gave the net-labels, power supply, pull-up resistors and decoupling capacitors accordingly.
- **Schematic annotation:**

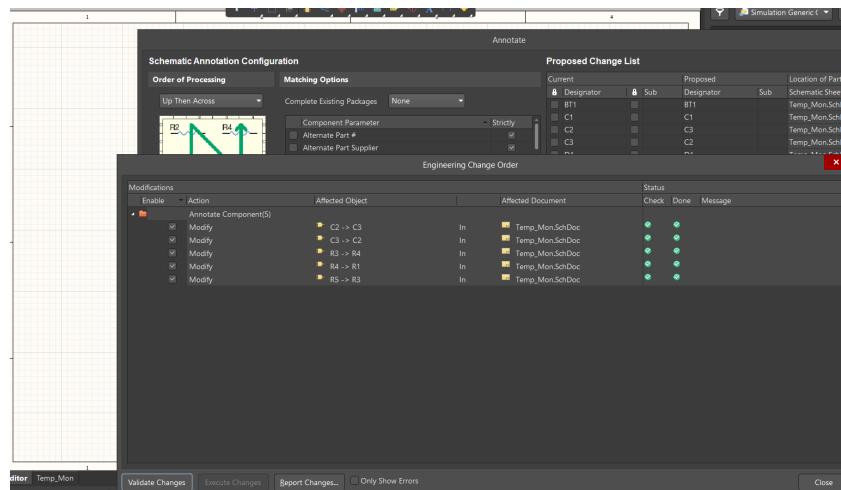


Figure 1: Schematic Annotation and ECO

• Width Constraints and Clearance Width:

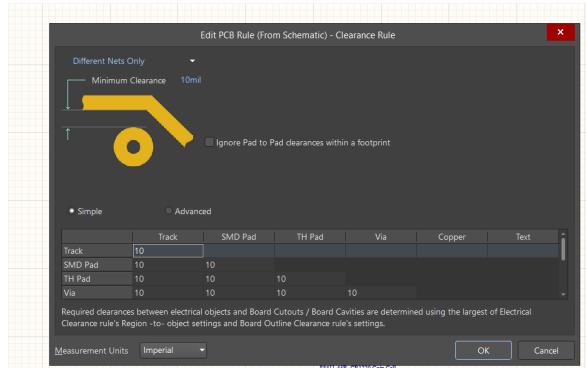


Figure 2: Clearance Width

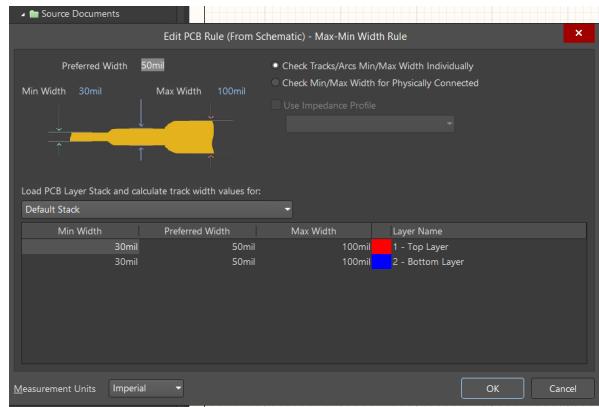


Figure 3: Width Constraints

- **Error Validation:**

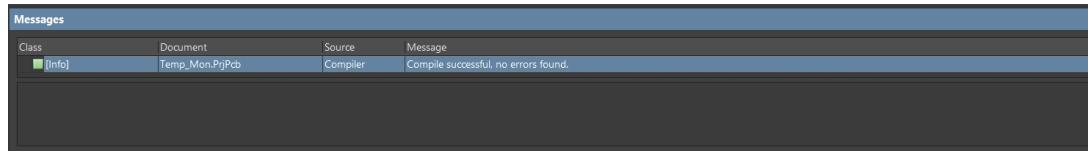


Figure 4

- **Board Configuration**

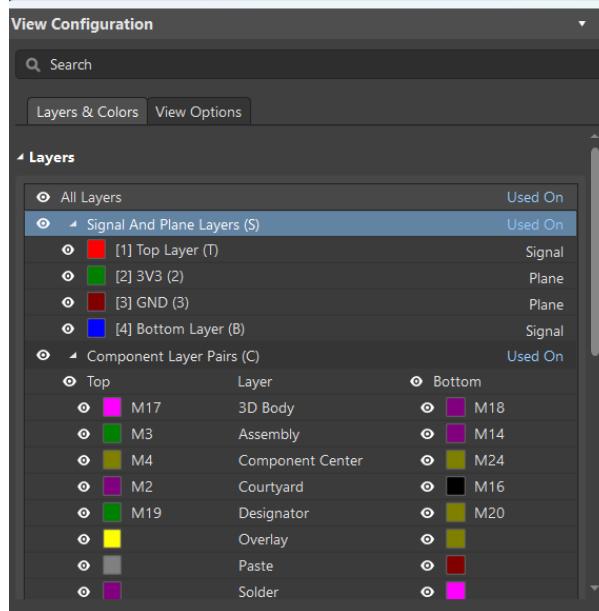


Figure 5: Signal Layers

- Board outline dimensions are 955 mil x 885 mil



Figure 6: Mechanical Layers

- **Layer stack Manager and Via types**

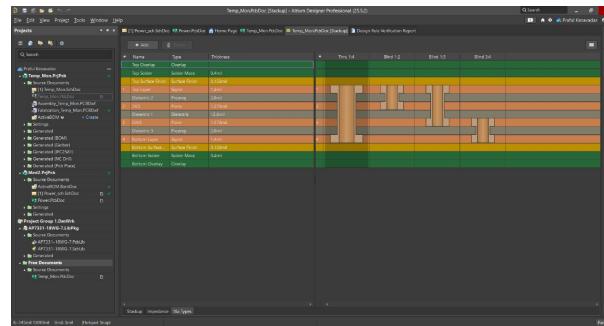


Figure 7

- **PCB Clearance widths and Rule priorities**

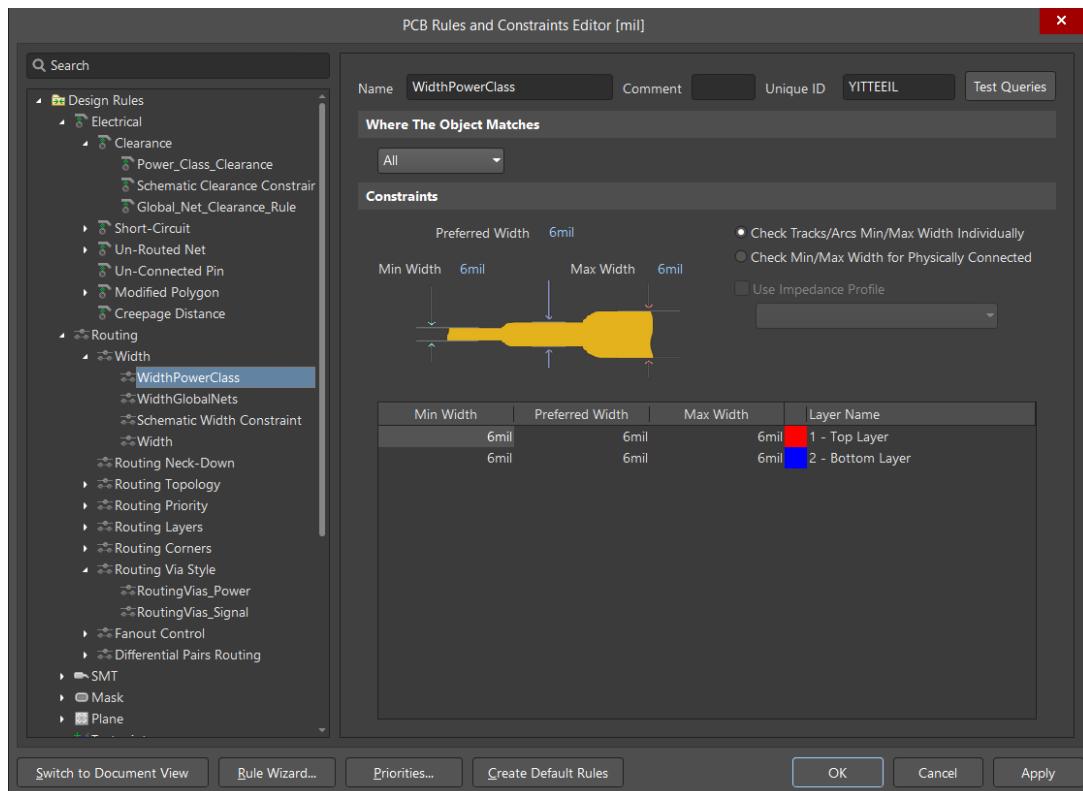


Figure 8

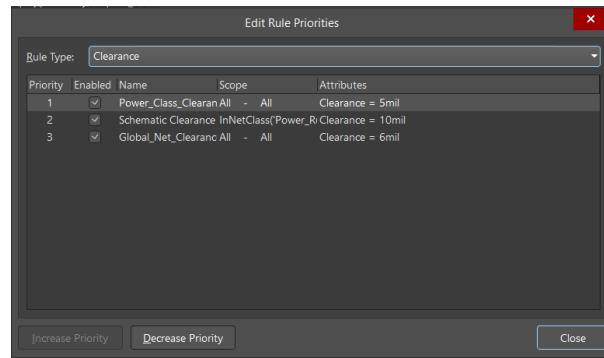


Figure 9

- Setting Via Size

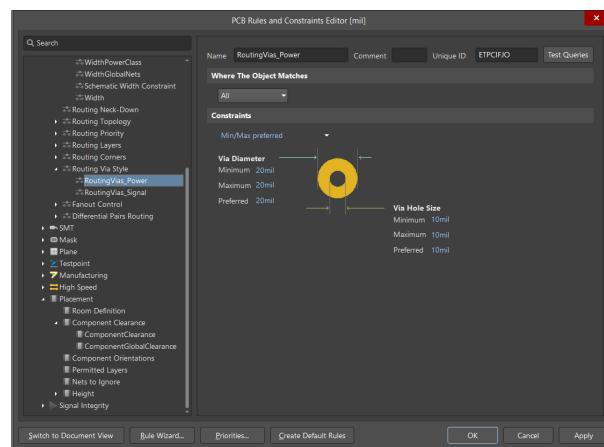
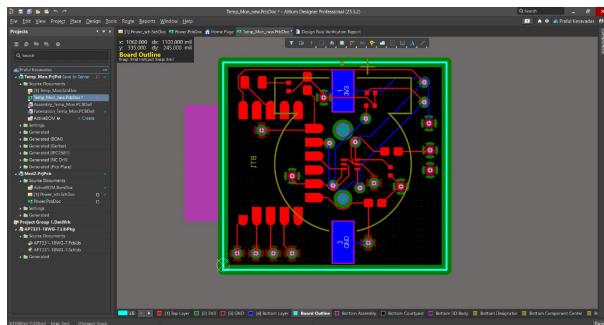


Figure 10: Power Via Size

- ROUTING



- 3D view

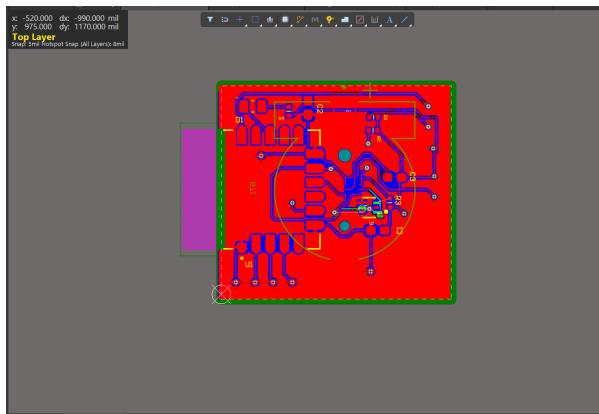


Figure 11: Final layout

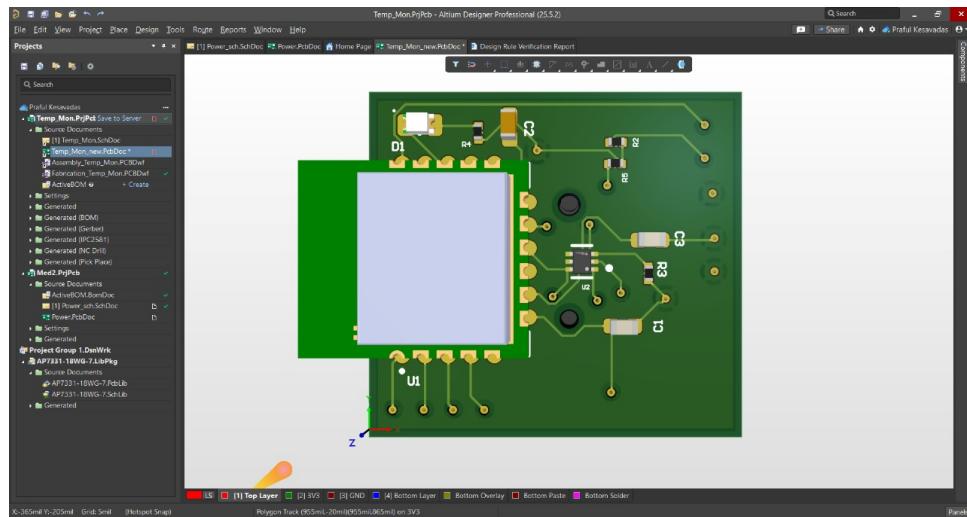


Figure 12: TOP VIEW

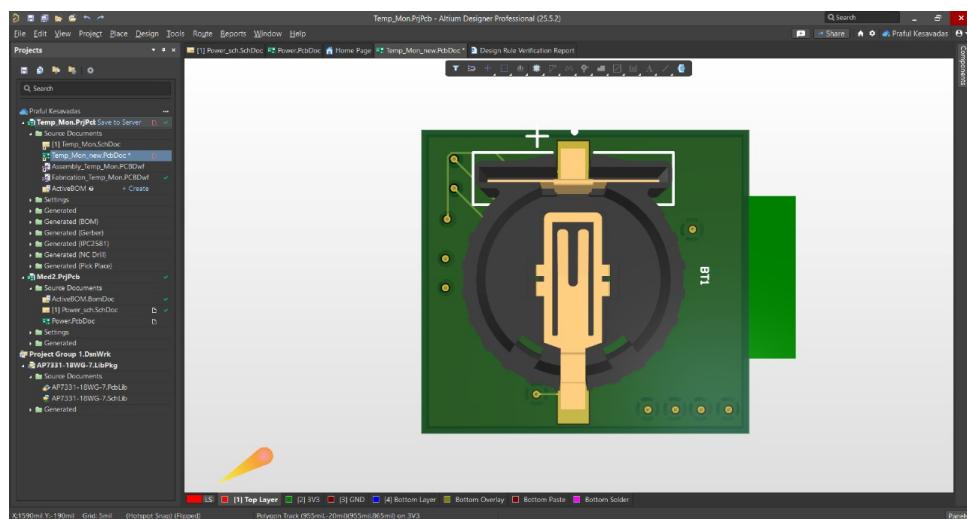
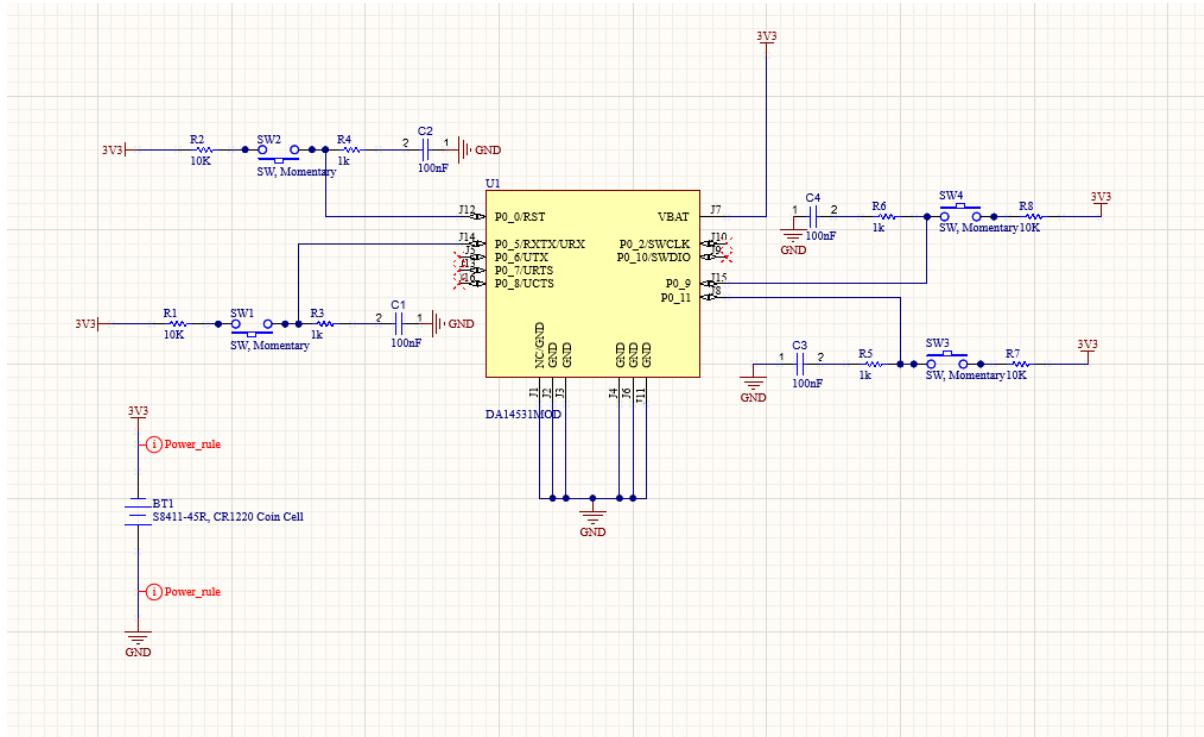


Figure 13: Bottom View

2. Button Interface Expansion

Modify the existing DA14531 dev board design to add four tactile buttons with proper debouncing circuits. Include pull-up/pull-down resistors and ensure the buttons are connected to GPIO pins that support interrupt functionality.

Schematic:



Button Interface Schematic

Hardware Design

- **Switches (SW1–SW4):** Standard tactile momentary push-buttons.
- **Series resistor ($R_{deb} = 10k\Omega$):** Limits switch bounce and isolates the RC debounce network.
- **Debounce capacitor ($C_{deb} = 100nF$):** Forms a first-order RC low-pass with R_{deb} for 1.6ms time constant.
- **Pull resistors ($R_{pu/pd} = 10k\Omega$):** Tie GPIO to 3.3V or GND when switch is open.
- **GPIO pins:**
 - P0_4 → SW1
 - P0_5 → SW2
 - P0_6 → SW3
 - P0_7 → SW4

The modified DA14531 development board schematic incorporates four tactile buttons designed for GPIO-based interrupt functionality. Each button interface includes a pull-up resistor, a debouncing circuit, and connection to a GPIO pin that supports interrupts.

Circuit Description

Each tactile button circuit follows the below structure:

- **Pull-up Resistor (10kΩ):** Connected between the 3.3V supply and the GPIO pin. This ensures the pin remains at a defined high logic level when the button is pressed, preventing floating inputs.
- **Momentary Push Button:** When unpressed, it pulls the GPIO pin to GND, resulting in a falling edge that can be detected via an interrupt.
- **RC Debouncing Network (1kΩ + 100nF):** This low-pass filter smooths out voltage fluctuations caused by mechanical bouncing of the switch. The time constant of the RC filter is:

$$\tau = R \times C = 1\text{k}\Omega \times 100\text{nF} = 100\ \mu\text{s}$$

This effectively filters out spurious transitions due to bounce.

- **GPIO Connection:** The filtered signal is routed to interrupt-capable GPIOs on the DA14531 .

Approach:

- **Schematic annotation:**

Modifications	Action	Affected Object	Affected Document	Status	Check	Done	Message
Enable	Annotation Component(10)	B11 -> B17	In	Sheet1.SchDoc			
Modify		C1 -> C7	In	Sheet1.SchDoc			
Modify		C2 -> C7	In	Sheet1.SchDoc			
Modify		C3 -> C7	In	Sheet1.SchDoc			
Modify		C4 -> C7	In	Sheet1.SchDoc			
Modify		R11 -> R7	In	Sheet1.SchDoc			
Modify		R2 -> R7	In	Sheet1.SchDoc			
Modify		R3 -> R7	In	Sheet1.SchDoc			
Modify		R4 -> R7	In	Sheet1.SchDoc			
Modify		R5 -> R7	In	Sheet1.SchDoc			
Modify		R6 -> R7	In	Sheet1.SchDoc			
Modify		R7 -> R7	In	Sheet1.SchDoc			
Modify		R8 -> R7	In	Sheet1.SchDoc			
Modify		R9 -> R7	In	Sheet1.SchDoc			
Modify		SW1 -> SW7	In	Sheet1.SchDoc			
Modify		SW2 -> SW7	In	Sheet1.SchDoc			
Modify		SW4 -> SW7	In	Sheet1.SchDoc			
Modify		U1 -> U7	In	Sheet1.SchDoc			

Figure 14: Schematic Annotation

- **Width Constraints and Clearance Width**
- **Error Validation:**

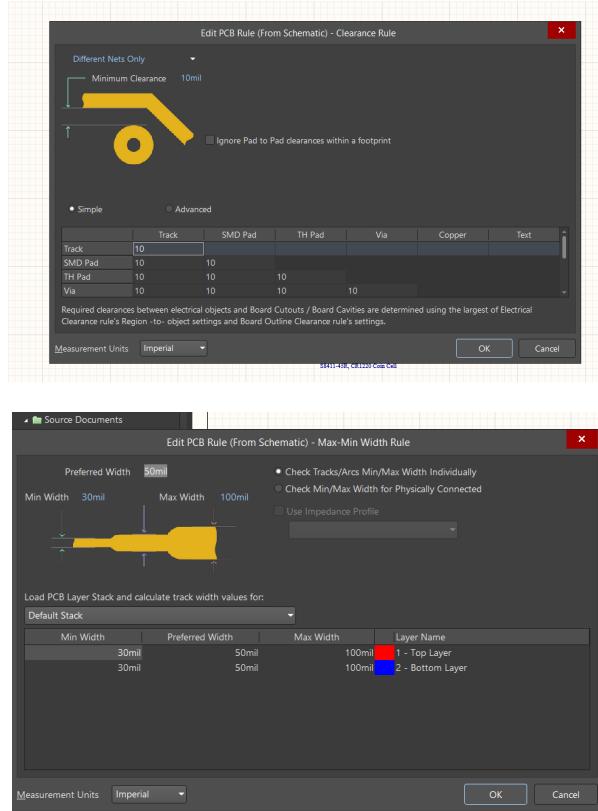


Figure 15: Width Constraints

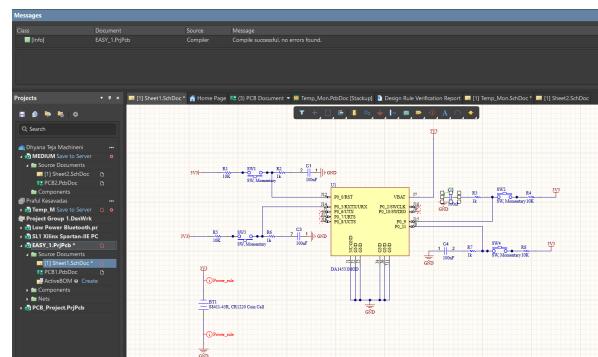


Figure 16: Error Validation

• Board Configuration

- We defined the board layer and board outlines.
- Board outline dimensions are 1560mil x 855 mil.

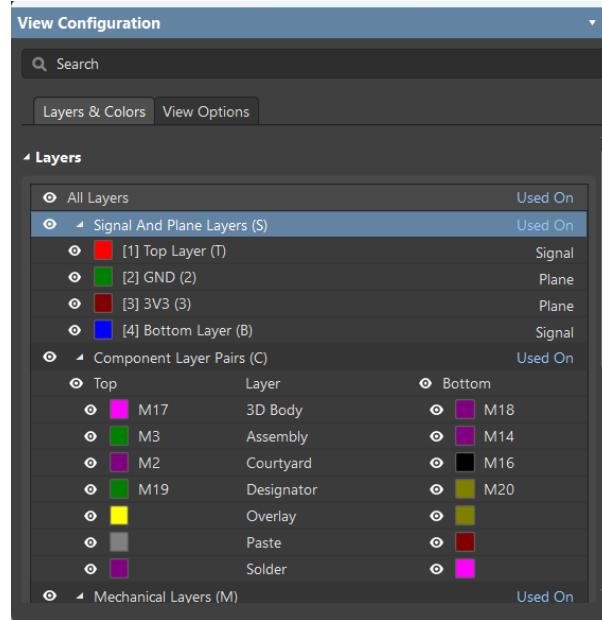


Figure 17

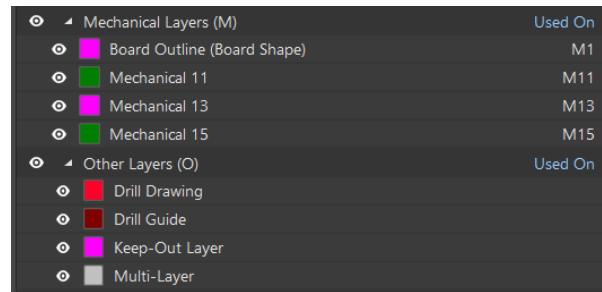


Figure 18: mechanical Layer

- **Layer Stack manager**

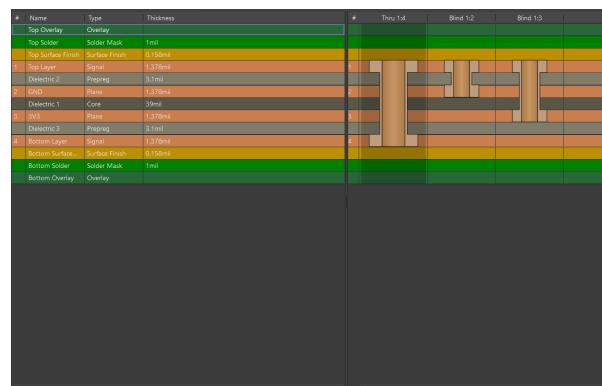


Figure 19: Via Types

- **PCB Clearance Widths and Rule Priorities**

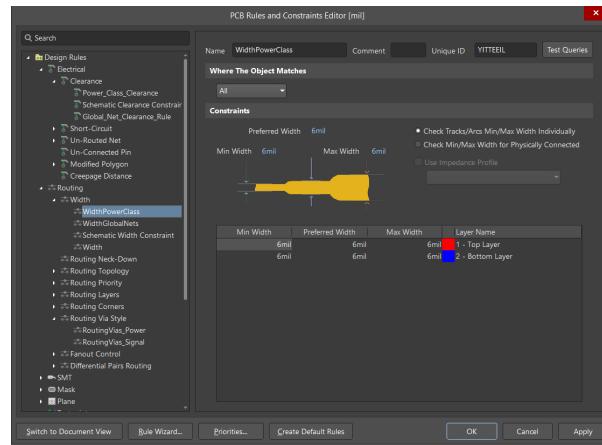


Figure 20

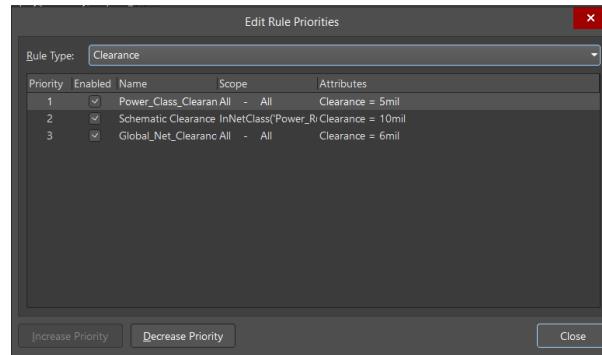
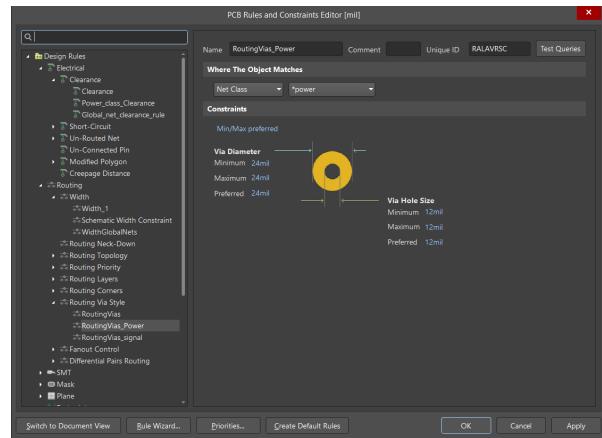


Figure 21

• Setting Via Size



• Routing

• Final Layout

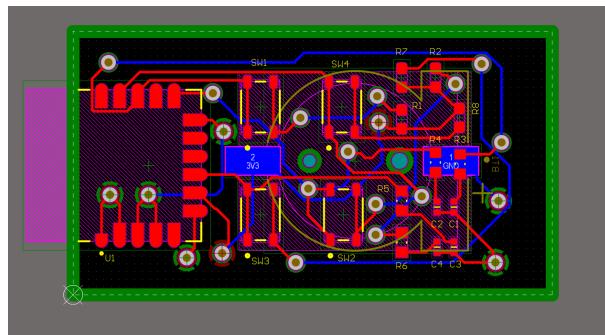
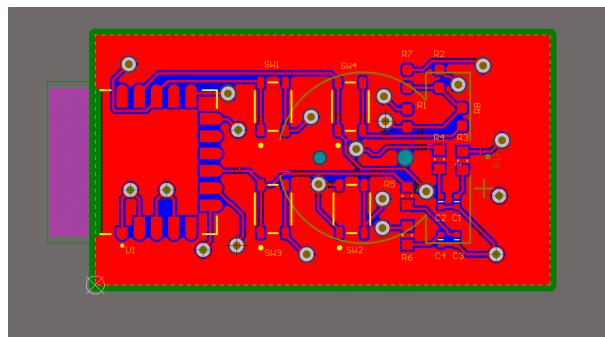
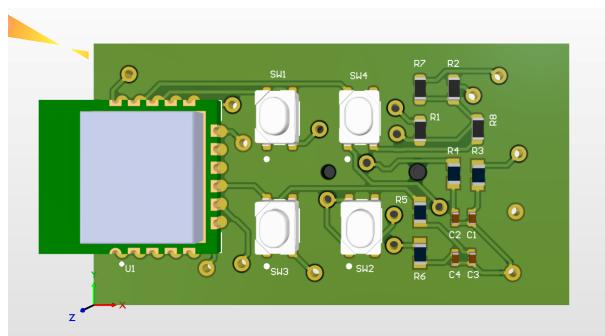


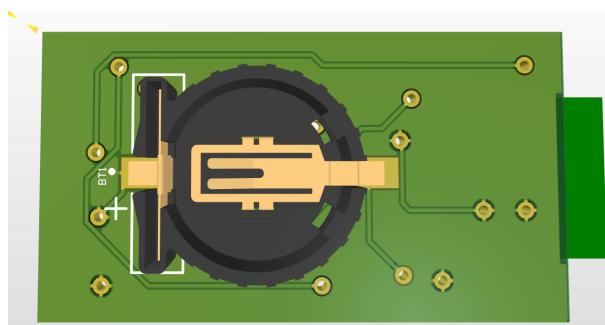
Figure 22: Routing



• TOP VIEW



• BOTTOM View



3. OLED Display Integration

Create a schematic and PCB layout to interface an SPI OLED display (e.g., SSD1306 128x64) with the DA14531 MCU. Ensure proper signal routing, decoupling, and include level shifters if necessary for compatible voltage levels.

Schematic:

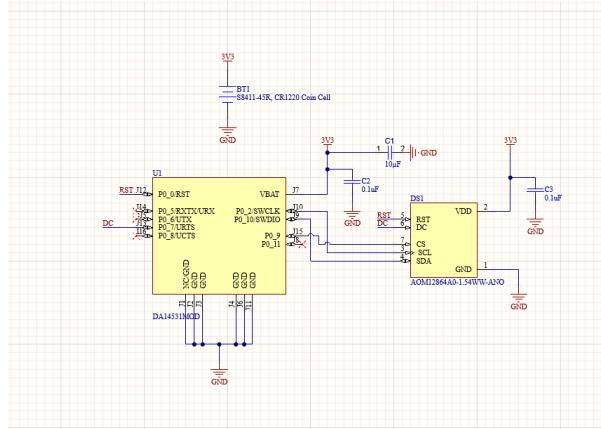


Figure 23: Schematic

OLED Display Interface with DA14531 – Working Principle

This circuit schematic establishes SPI communication between the DA14531 SoC and a low-power OLED display module (AOM12864A0-1-S4WW-ANO, SSD1306 compatible). The design ensures signal integrity, decoupling, and logic-level compatibility for reliable operation.

Overview of the System

- **Microcontroller Unit (U1):** DA14531MOD, a BLE 5.1 SoC, responsible for controlling the display.
- **Display Module (DS1):** AOM12864A0-1-S4WW-ANO, a 128x64 graphical OLED screen, controlled via SPI interface.
- **Power Supply:** 3.3V provided by a coin cell battery (CR1220) through BT1.

Connections and Signal Routing

- **Power Supply and Decoupling:**

- The OLED module and DA14531 both operate at 3.3V.
- **C1 (10μF), C2, C3 (0.1μF)** are decoupling capacitors placed close to VDD pins of the MCU and OLED to suppress power rail noise and ensure stable operation.

- **SPI Interface:**

- CS (Chip Select), SCL (Clock), and SDA (Data) of the OLED are connected to GPIOs of DA14531.
- These pins are configured in firmware as SPI Master mode.

- **Reset and DC Pins:**

- RST (Reset) and DC (Data/Command) pins of the OLED are connected to GPIOs of DA14531.
- These allow software control to reset the OLED and switch between command and data modes.

Approach:

- We made the schematic based on the data sheets and made all the connections as per the requirements.
- **Schematic annotation**

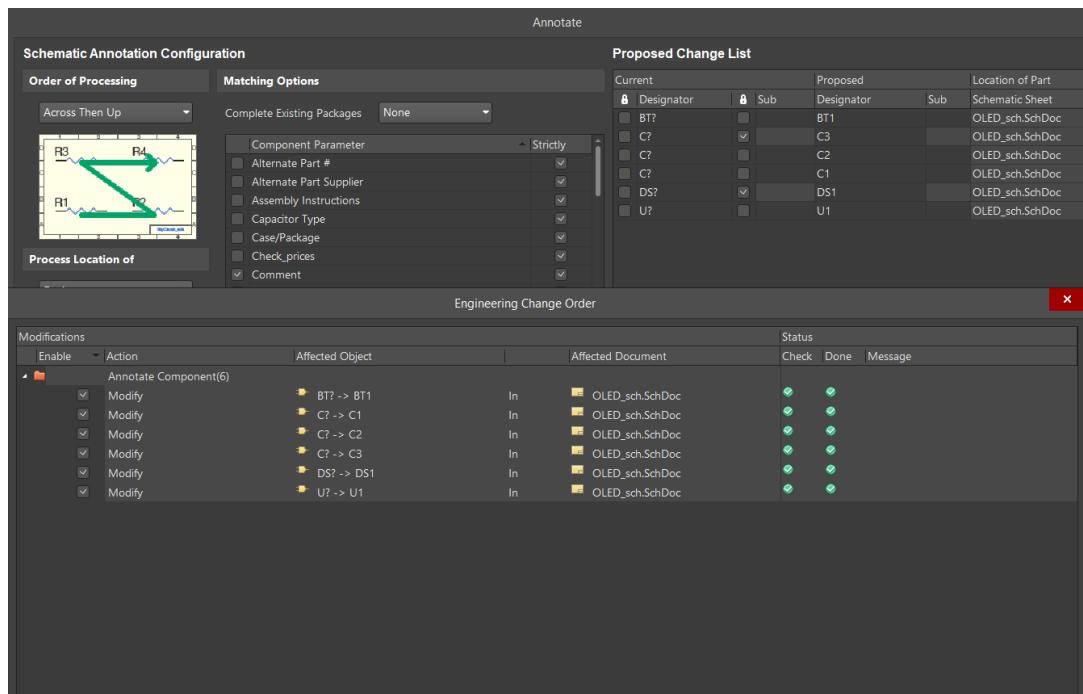


Figure 24: Annotation

- Width Constraints and Clearance Width

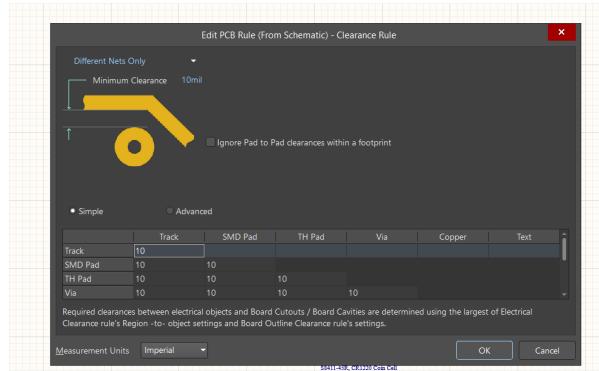


Figure 25

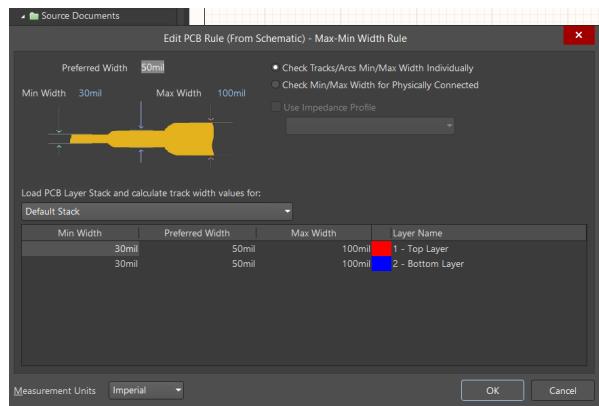


Figure 26

- Error Validation



Figure 27

- Board Configuration:

- Board outline Dimensions 2585 mil x 1885 mil.

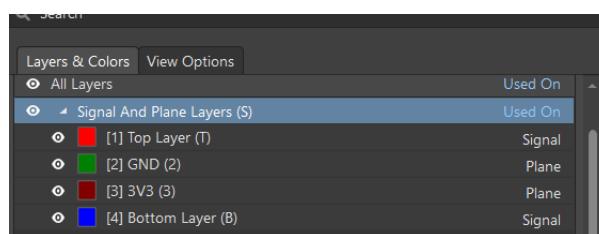


Figure 28

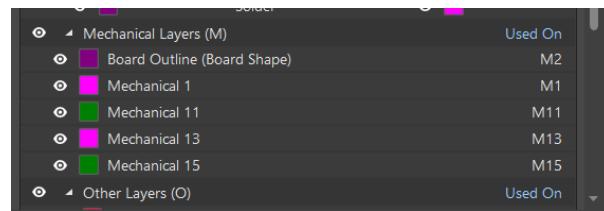


Figure 29

• Layer Stack Manager

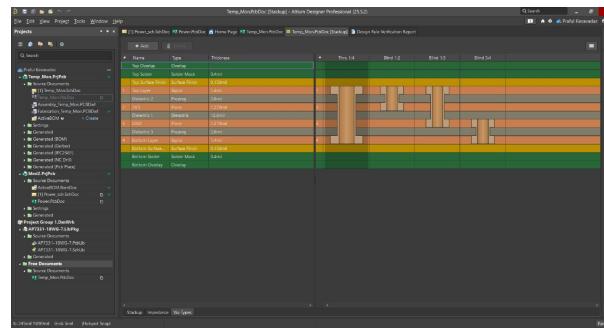


Figure 30

• PCB CLEARANCE AND RULE PRIORITIES

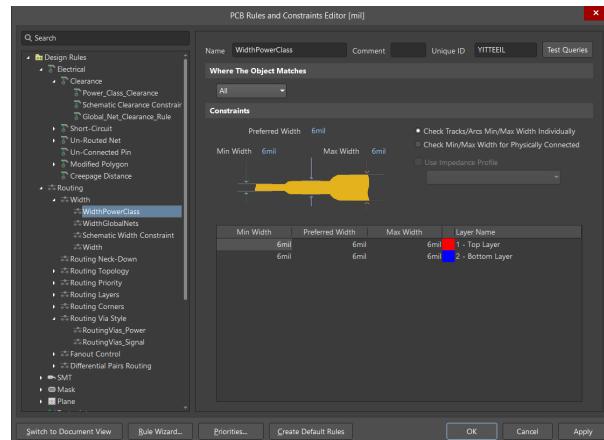


Figure 31

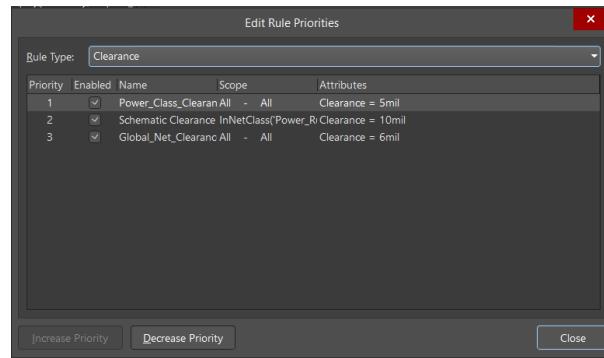


Figure 32

• Setting Via Size

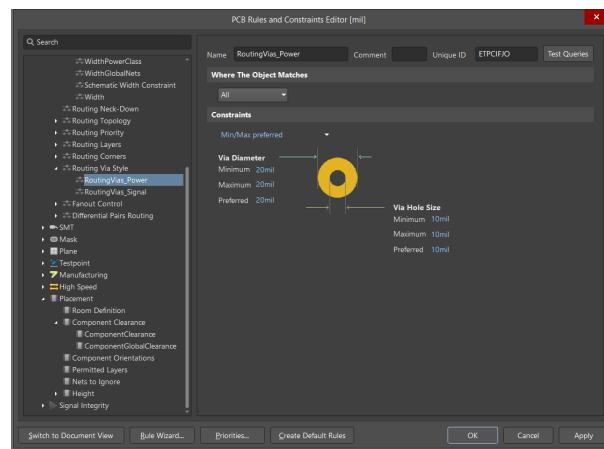


Figure 33

• Routing

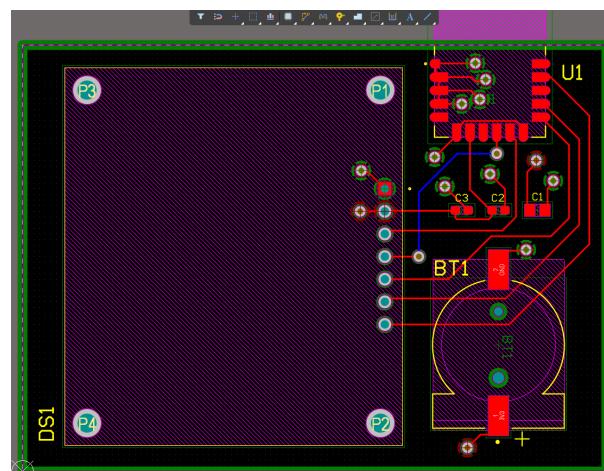


Figure 34

- Final Layout

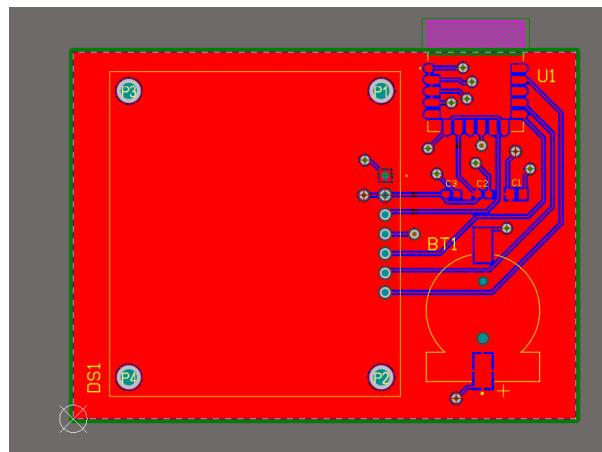


Figure 35

- TOP VIEW

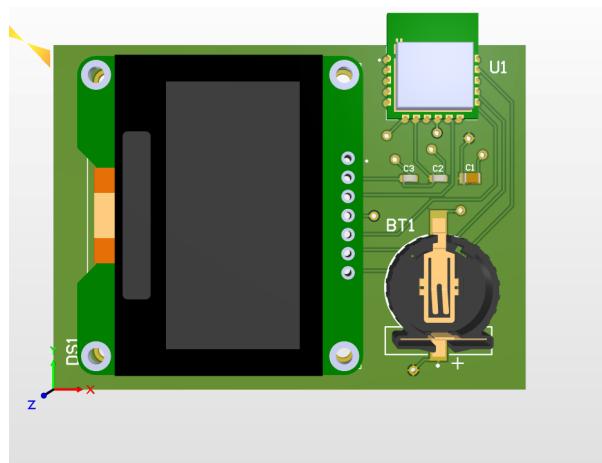


Figure 36

- Bottom View

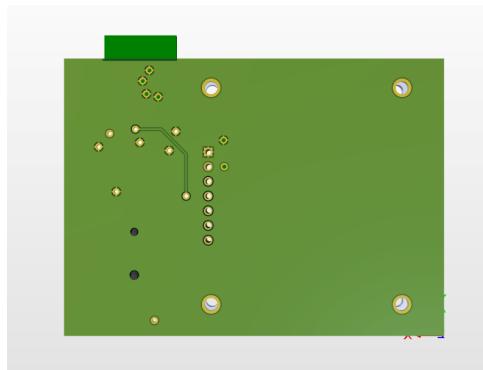


Figure 37

Section - Medium

2. Mixed-Signal Design with Ground Isolation

Create a circuit connecting an analog microphone and digital audio processor to the DA14531. Design a proper ground plane strategy with isolated analog and digital grounds connected at a single point. Include power supply filtering for noise reduction, implement guard rings around sensitive analog traces, and design a star-grounding topology. Document your ground isolation strategy and power filtering approach.

1. Overview of the Circuit

This circuit interfaces:

- An Analog Microphone
- A Digital Audio Processor / ADC
- The DA14531 SoC
- A 3.3V power supply (via LDO or battery)

Focus is given to signal integrity, power noise rejection, and analog/digital ground management.

2. Component Selection & Roles

Component	Role
Analog Microphone	Captures sound and outputs analog audio signal
Digital Audio Processor / ADC	Converts analog audio to digital
DA14531 SoC	Processes or transmits digital audio over BLE
LDO Regulator	Regulates 5V to clean 3.3V
Ferrite Beads / Inductors	Filters high-frequency noise between analog and digital rails
Bypass Capacitors	Suppress voltage spikes and transients
Guard Ring	Shields analog signal traces from interference

3. Circuit Description and Working

A. Microphone Front-End

- The Audio signal is amplified using an Amplifier
- VCC is supplied through a ferrite bead with decoupling capacitors ($10 \mu\text{F}$ and $0.1 \mu\text{F}$).
- OUT is AC-coupled via a capacitor ($1 \mu\text{F}$) to the ADC input
- Ground connects to AGND.

B. Digital Audio Processor / ADC

- Converts analog signal to digital using I2S or SPI.
- Analog input pins referenced to AGND.
- Digital output interfaces with DA14531 using I2S/SPI.

C. DA14531 SoC

- Receives digital audio.
- Powered from digital 3.3V rail, referenced to DGND.
- Optionally controls ADC via I2C.

4. Power Supply Filtering Strategy

Analog Power (AVDD)

- Isolated from digital rail using a ferrite bead .
- Decoupled using a $10 \mu\text{F} + 0.1 \mu\text{F}$ capacitor.

Digital Power (DVDD)

- Directly from 3.3V LDO with local decoupling capacitors on each digital IC.

Result:

Analog power is filtered from digital switching noise, ensuring low-noise operation.

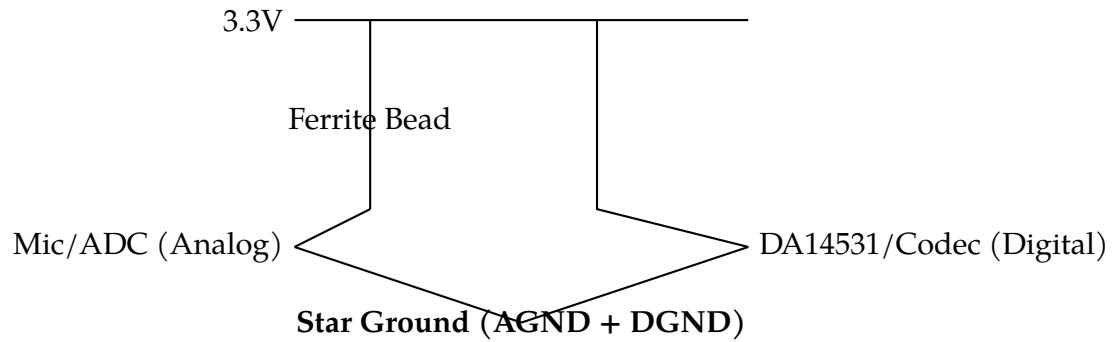
5. Ground Plane Strategy

A. Split Ground Planes

- **AGND** serves the microphone and analog sections of the ADC.
- **DGND** serves the DA14531 and digital circuits.
- Grounds are connected at a **single point** (star ground), typically near the ADC or power supply entry.

B. Star Ground Topology

All ground currents return to a central star point to prevent digital noise coupling into analog paths.



6. Guard Ring Strategy

- Guard rings (connected to AGND) are routed around sensitive analog traces, especially microphone output and ADC inputs.
- They reduce coupling from digital traces and shield analog signals.

7. Circuit Operation Summary

1. The microphone captures sound and outputs an analog signal.
2. The signal passes through an AC coupling capacitor to the ADC.
3. The ADC digitizes the signal and transmits it to the DA14531.
4. DA14531 handles BLE transmission or processing.
5. Power is filtered and routed to reduce cross-domain noise.
6. Analog and digital grounds are isolated and joined at a single star point.

APPROACH

- Schematic

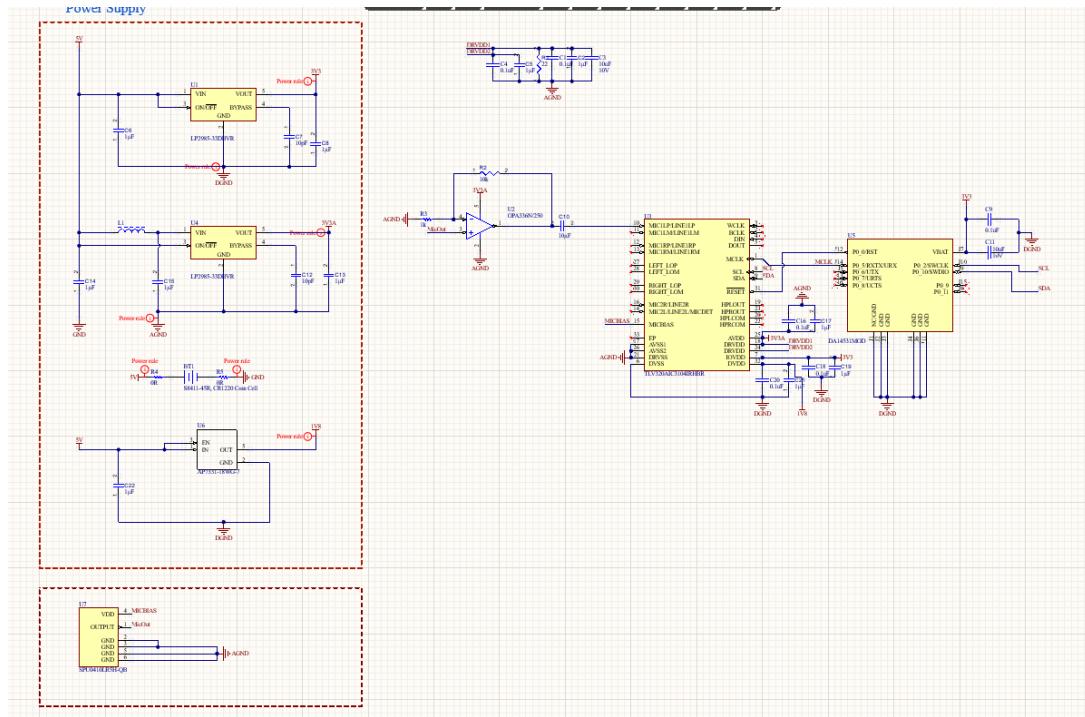


Figure 38: Schematic

- **Annotation**

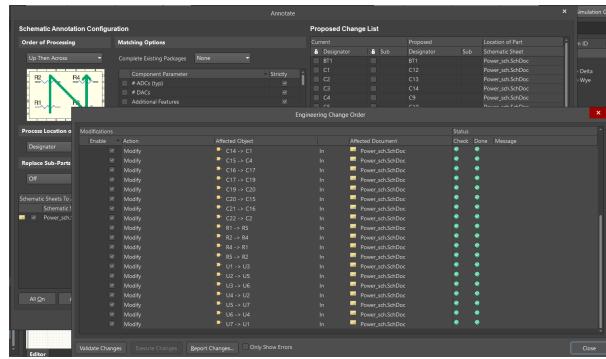


Figure 39: Annotation and ECO

- **Board Configuration:** Board Size is 2535mil x 920mil.

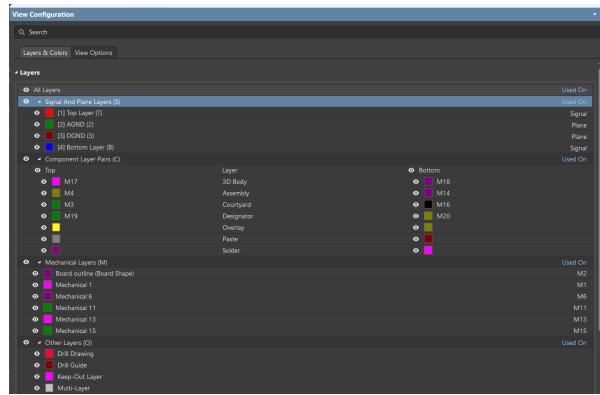


Figure 40: Board Configuration

- **Layer Stack Manager and Via Types**

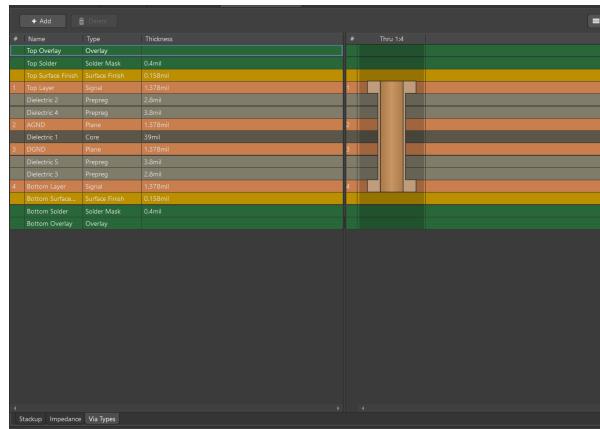


Figure 41

- **PCB CLEARANCE**

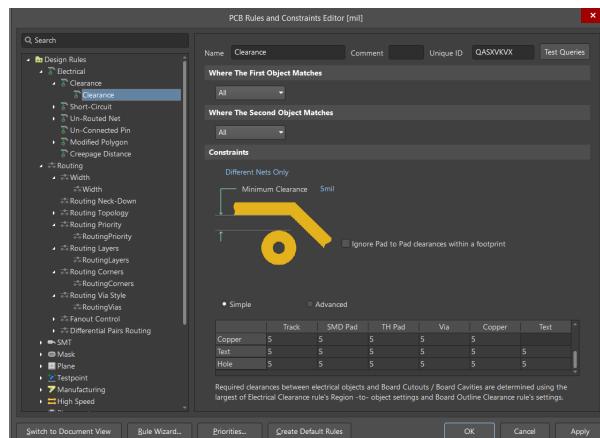


Figure 42: Clearance

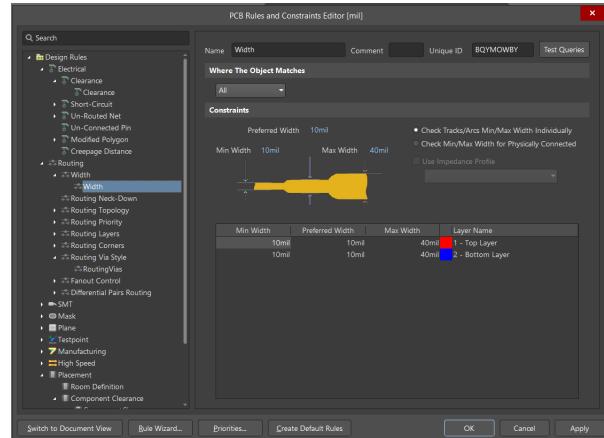


Figure 43

• Vias Size

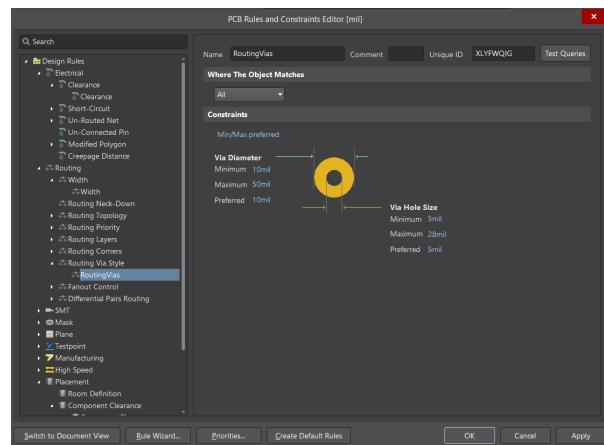


Figure 44

• Final Layout

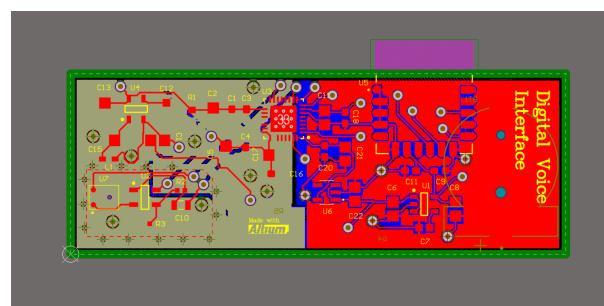


Figure 45: Final LAYout

- We used the gaurd rings in th bottom left of the layout to shield the analog traces like mircophone output and ADC inputs.

• Views

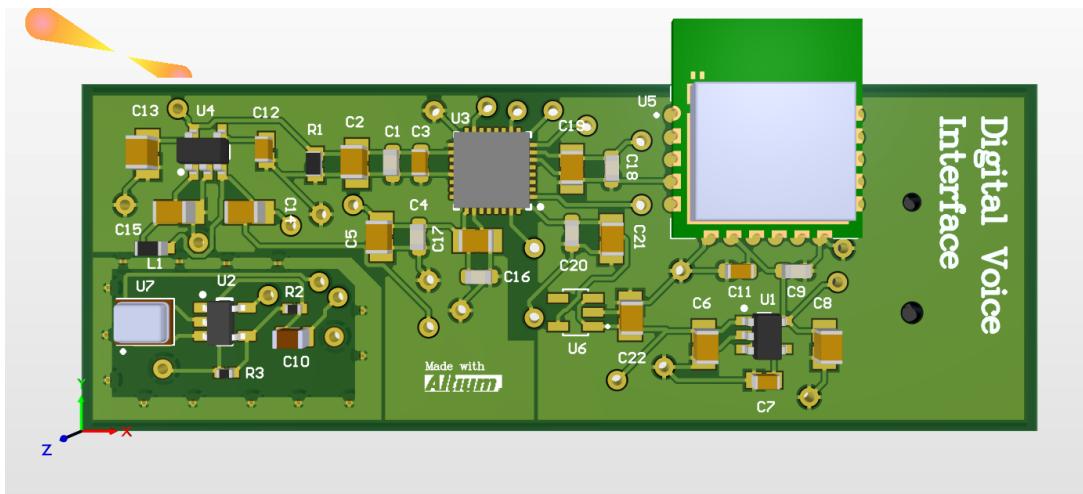


Figure 46: Top View

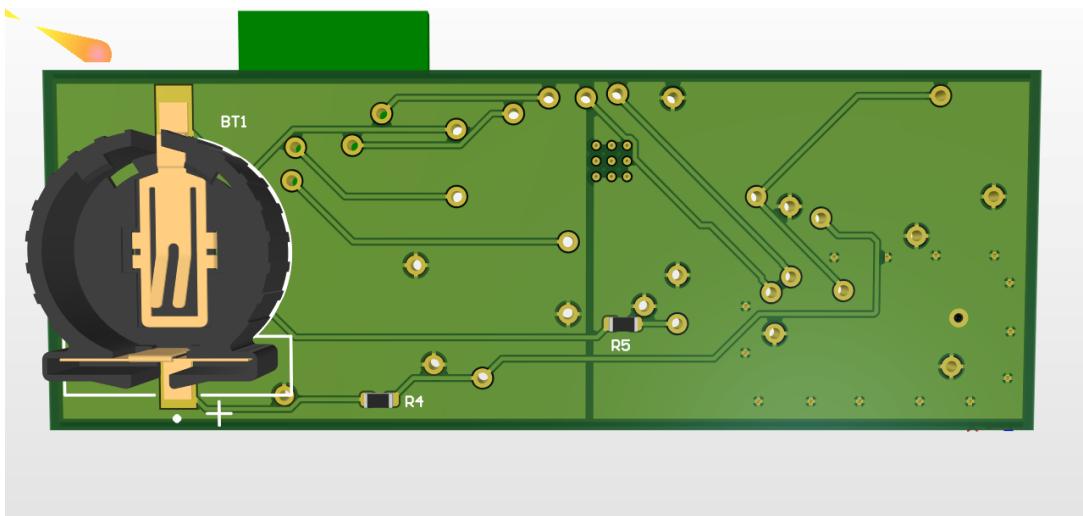


Figure 47: Bottom View

3. Power Supply Noise Mitigation System

Design a circuit that powers the DA14531 and several noisy peripherals (motor driver, solenoid, etc.) from a single supply. Implement multiple power domains with proper isolation using ferrite beads and decoupling capacitors. Design power plane splits, filter networks, and add test points for measuring power supply noise. Include a ripple calculation for each power domain and justify your component selection.

1. System Overview

The system is designed to power a Bluetooth Low Energy (BLE) SoC (DA14531) along with several noisy peripherals such as motor drivers and solenoids from a single power source. Noise isolation and power integrity are maintained using multiple power domains, each filtered through ferrite beads and decoupling capacitors.

Power Domains and Ferrite Beads Explanation

Clean Power Domain (DA14531)

Ferrite Bead: FB1

- **Purpose:** Isolates the noise-sensitive BLE SoC from ripple and high-frequency switching noise.
- **Associated Capacitors:**
 - C5 (10 μ F): Bulk decoupling for low-frequency ripple.
 - C8 (0.1 μ F): High-frequency bypass.
 - C9 (1 μ F): Mid-frequency filtering.
- **Result:** Clean and stable 3.3V for the DA14531 ensures reliable BLE and analog performance.

Noisy Domain 1 (Motor Driver)

Ferrite Bead: FB2

- **Purpose:** Supplies power to DRV8833 motor driver and blocks switching noise.
- **Associated Capacitors:**
 - C6 (10 μ F): Bulk storage.
 - C10 (0.1 μ F): High-frequency filtering.
- **Result:** Isolates the driver from the clean 3.3V logic supply.

Noisy Domain 2 (Solenoid or Secondary Motor)

Ferrite Bead: FB3

- **Purpose:** Powers additional solenoid or inductive load.
- **Associated Capacitors:**
 - C7 (10 μ F): Ripple smoothing.
- **Result:** Prevents large transient currents from affecting other domains.

3. Voltage Regulation

Component: LP2985-33DBVR (U1)

- Provides clean 3.3V from coin cell/battery.
- High PSRR (75 dB at 1kHz) suppresses upstream noise.
- Works with FB1 to deliver an ultra-clean power rail to DA14531.

Test Points

Table 1: Test Point Descriptions for Power Supply Noise Mitigation

TP	Net Name	Location	Purpose
TP1	3V	Before ferrite beads	Main supply reference
TP2	V_per_clean	After FB1 (to DA14531)	Clean MCU supply check
TP3	V_mosfet	After FB2	Gate driver domain check
TP4	V_motor	After FB3	Motor/solenoid noise check
TP5	LDO_OUT	LDO output (U1)	Check LDO ripple/stability
TP6	Gate_Q1	Gate of Q1	Monitor switching control
TP7	Source_Q1	Source of Q1	Monitor switch output
TP8	VBAT	After D1	Battery voltage drop check

Approach:

- **Schematic:**

- We designed the following circuit based on the data-sheets and the requirements.

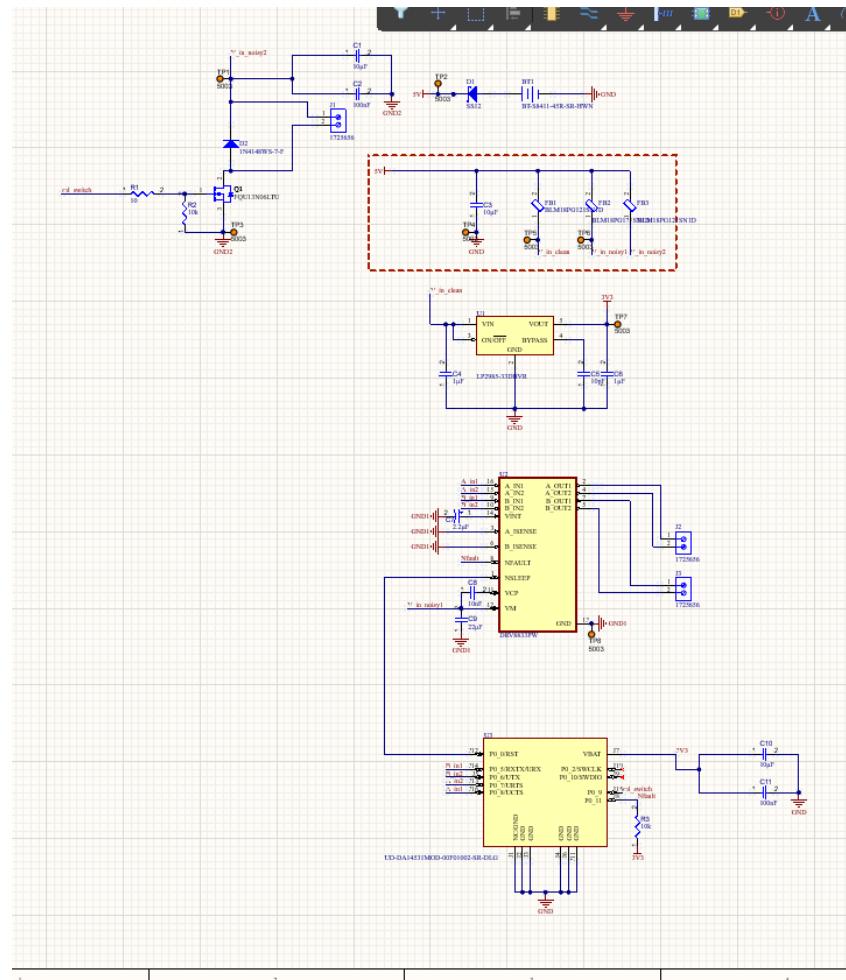


Figure 48: Schematic

• Error Validation

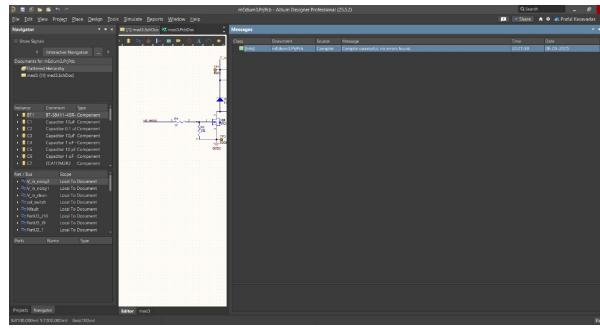


Figure 49: Error Validation

• Board Configuration

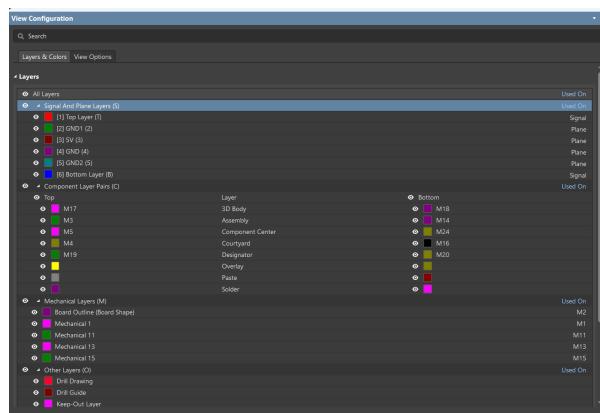


Figure 50: Board Configuration

• Board Outline dimensions are 2900mil x 2350mil

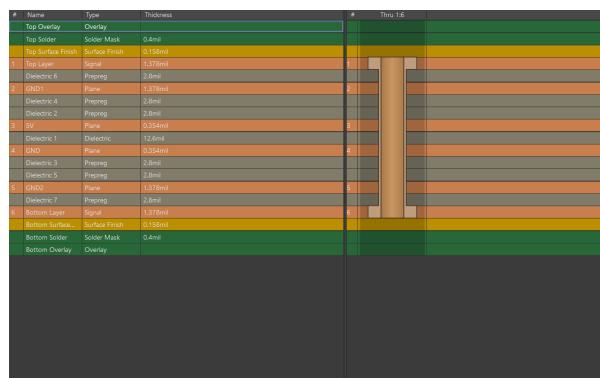


Figure 51: Layer Stack Manager

• PCB CLEARANCE AND RULE PRIORITIES

We made trace width of the Power driver high handle High currents

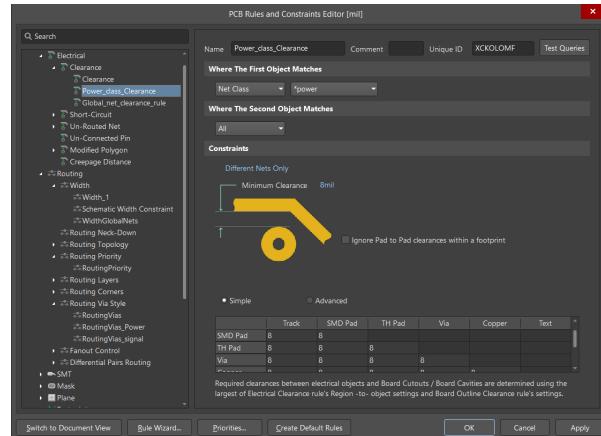


Figure 52: Power Clearance

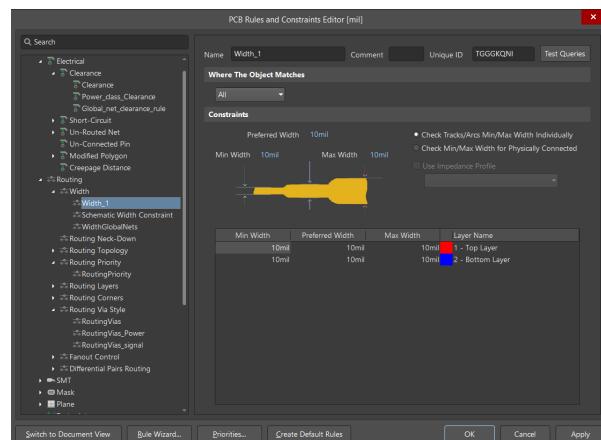


Figure 53: Width Constraints

• Setting Different Via sizes

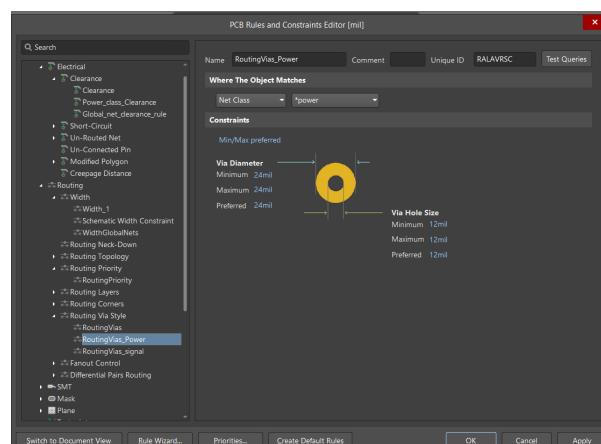


Figure 54: Power Vias

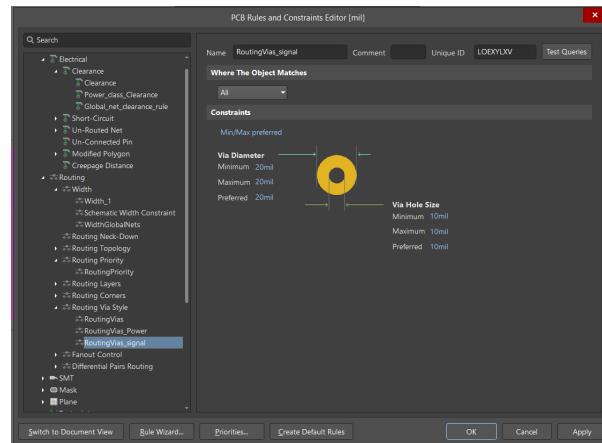


Figure 55: Signal Vias

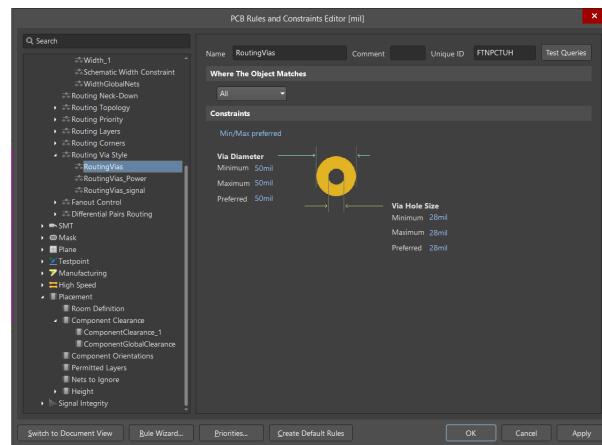


Figure 56: Routing Vias size

- Final Layout

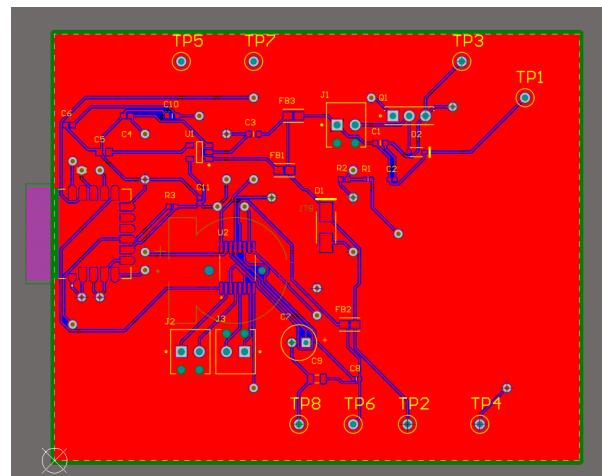


Figure 57: Caption

- Top view

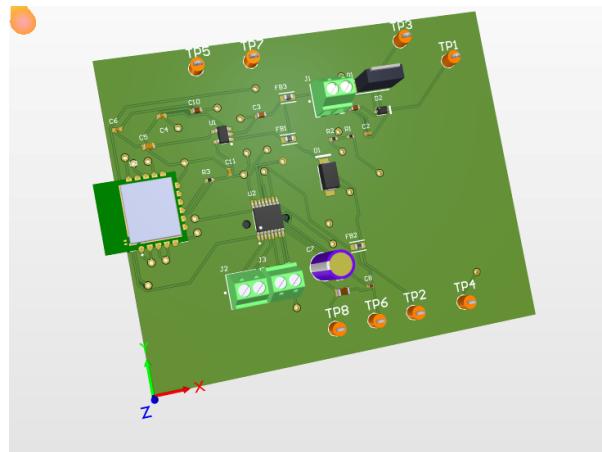


Figure 58

- **Bottom View**

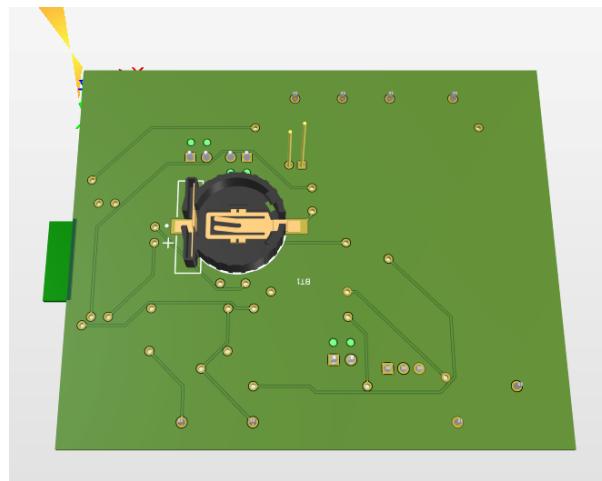


Figure 59: Bottom view

Star Grounding

Here we are isolating grounds for each of the devices (motor, solenoid and DA14531) from the main ground using ferrite bead. Each of the grounds (GND1 and GND2) is connected to the main ground (GND) at a single point (star connection)

Ripple Calculation:

To calculate the ripple voltage across the supply capacitor feeding the DRV8833 motor driver at full load, we use the classic capacitor ripple equation:

Ripple Voltage Formula (Approximate):

$$V_{\text{ripple}} = \frac{I}{fC}$$

Where:

- $I = 1.5 \text{ A}$ (Load current at full load)
- $f = 500 \text{ kHz} = 50,000 \text{ Hz}$ (Ripple frequency)
- $C = 2.2 \mu\text{F} = 2.2 \times 10^{-6} \text{ F}$ (Output capacitor)

Substituting the Values:

$$V_{\text{ripple}} = \frac{1.5}{50,000 \times 2.2 \times 10^{-6}} \approx 1.364 \text{ V}$$

Section - Hard

2. Power Integrity Analysis for Mixed Voltage System

Design a system with the DA14531 that incorporates multiple voltage domains (1.2V, 1.8V, 3.3V, 5V). Create a sophisticated power distribution network with PDN impedance analysis. Include decoupling capacitor selection optimization across multiple frequencies, implement dedicated power planes with appropriate plane splits, and design AC and DC current return paths. Document your power integrity simulation results and provide target impedance calculations for each power rail.

1 System Overview

This document describes the power distribution network, ground isolation strategy, and signal integrity techniques used in a DA14531-based embedded system. The system incorporates four distinct power domains: 5V, 3.3V, 1.8V, and 1.2V, each serving different subcomponents. It also implements proper analog-digital ground isolation, decoupling capacitor optimization, and impedance-controlled power delivery.

2 Power Domains and Subdomains

1. 5V Domain (Primary Input)

- Source: USB or CR1220 Coin Cell Battery
- Powers: 3.3V LDO (U1), directly feeds HC-SR04 sensor
- Filtering: Ferrite bead (FB2), bulk capacitor ($1\mu\text{F}$ + $0.1\mu\text{F}$)

2. 3.3V Domain

- Generated by: LP2953-33DBVR (U1)
- Powers: TMP102, DA14531 VBAT, 3.3V I2C pull-ups
- Filtering: Ferrite beads (FB1, FB4), local 100nF + $10\mu\text{F}$ decoupling

3. 1.8V Domain

- Generated by: AP7331 LDO (U4)
- Powers: SHT40 sensor and 1.8V I2C pull-ups
- Filtering: FB3, local 100nF + $10\mu\text{F}$ decoupling

4. 1.2V Domain (DA14531 Core)

- Generated by: DA14531 internal regulator
- Powers: DA14531 core
- Filtering: Local bypass capacitor near VDD

3 Signal Domains and Isolation

Domain	Devices	Signal Type	Voltage Level	Isolation Method
Digital Control	DA14531, I2C lines	GPIO, I2C	1.8V / 3.3V	Ferrite beads
Sensor Analog	TMP102, SHT40	I2C, Alert	1.8V / 3.3V	Isolated sub-rail
Ultrasonic	HC-SR04	TRIG/ECHO	5V	Separate bead + decoupling
Power Management	U1, U4	VIN/VOUT	5V to 3.3V/1.8V	LDO isolation

Table 2: Signal Domains and Isolation Strategy

4 Power Integrity Techniques

Ferrite Beads (e.g., BLM18PG181SN1D)

- High impedance at high frequency (~100 MHz)
- Low DC resistance
- These are the standard values for PDN analysis.

Frequency Range	Cap Value	Placement
10 kHz – 1 MHz	10 μ F	Near LDOs
1 – 10 MHz	1 μ F	Near sensors
10 – 100 MHz	0.1 μ F	At IC power pins
>100 MHz	100nF (low ESL)	For fast switching lines

Table 3: Decoupling Capacitor Strategy

5 Grounding Strategy

Ground Plane Zoning

- **Digital GND:** DA14531, I2C bus
- **Analog GND:** TMP102, SHT40
- **Power GND:** LDOs and input rails

Star Grounding Topology

- All GND zones meet at a single low-impedance node
- Prevents ground loops and noise propagation

Current Return Paths

- **AC signals:** Return directly under signal traces, avoid crossing splits
- **DC power:** Wide GND pours for low-impedance paths

6 Target Impedance Calculations

Target impedance for power rails is given by:

$$Z_{\text{target}} = \frac{V \times \text{tolerance}}{I_{\max}}$$

APPROACH

- Schematic:**

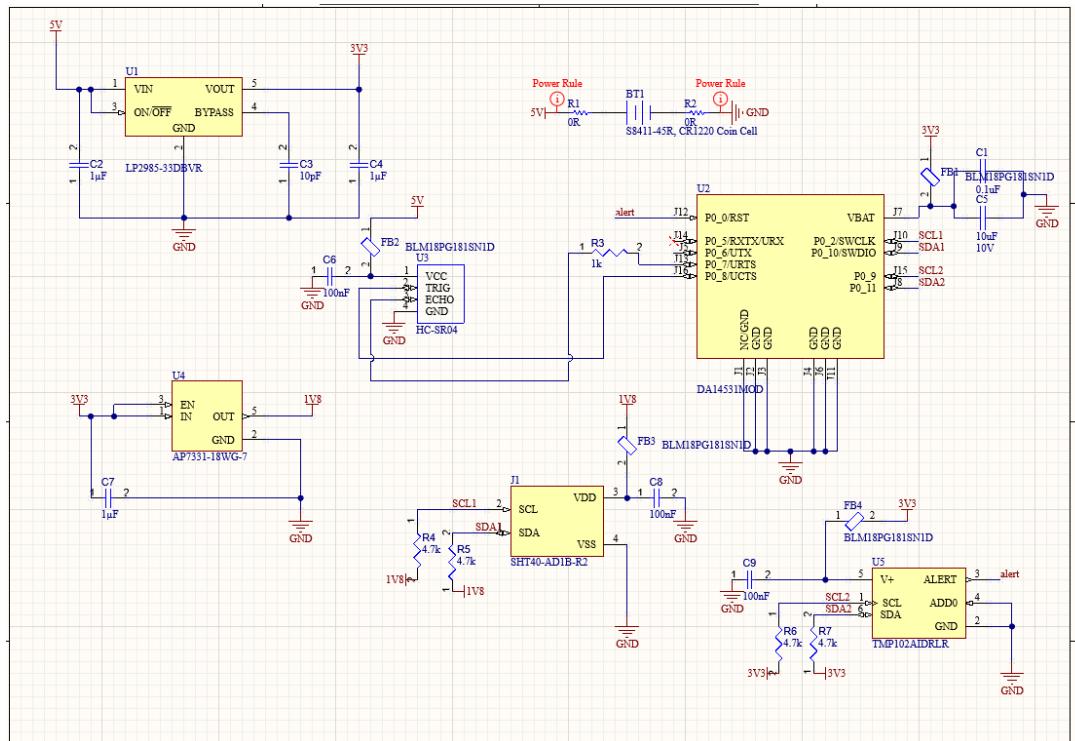


Figure 60

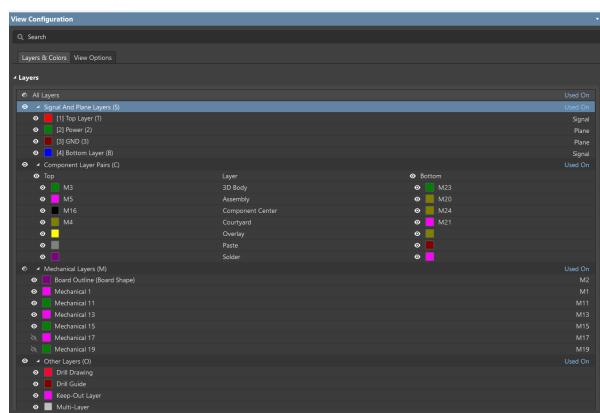


Figure 61: Board Configuration

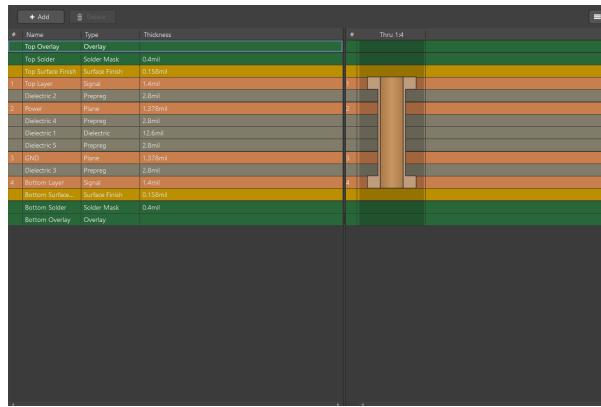


Figure 62: layer Stack Manager

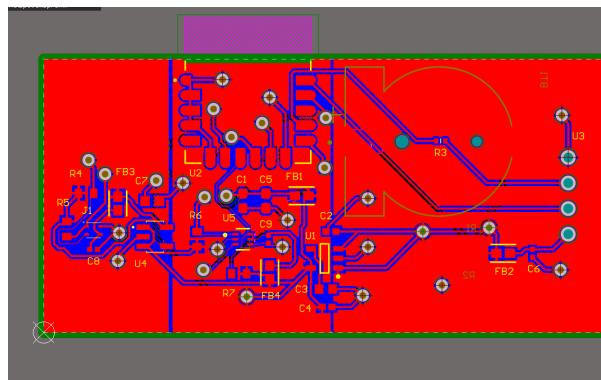


Figure 63: Final Layout

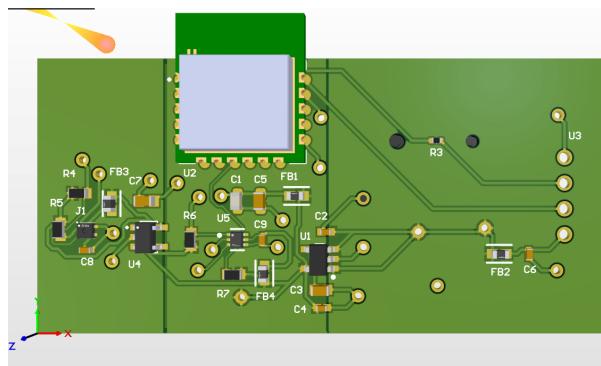


Figure 64: Top view

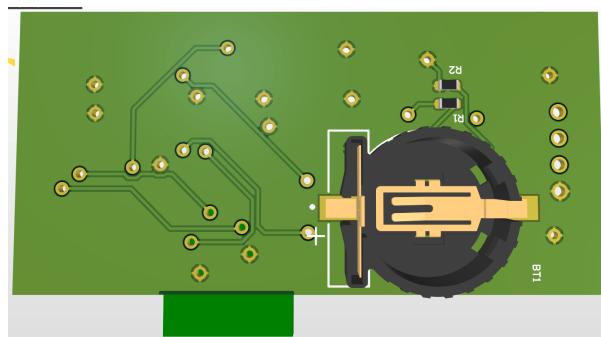


Figure 65: Bottom view