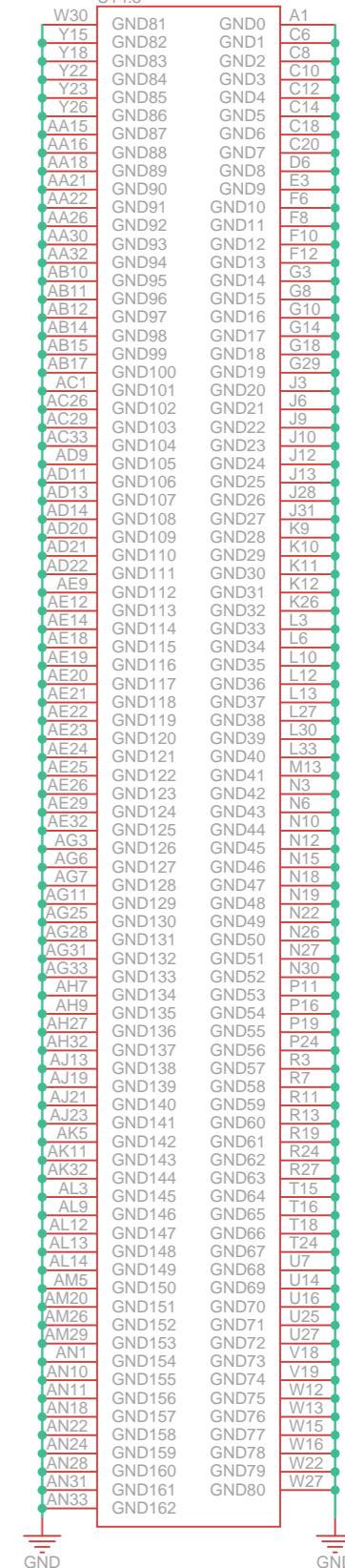
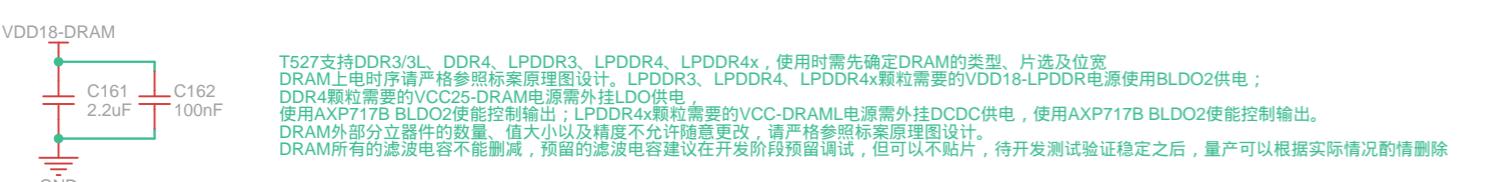
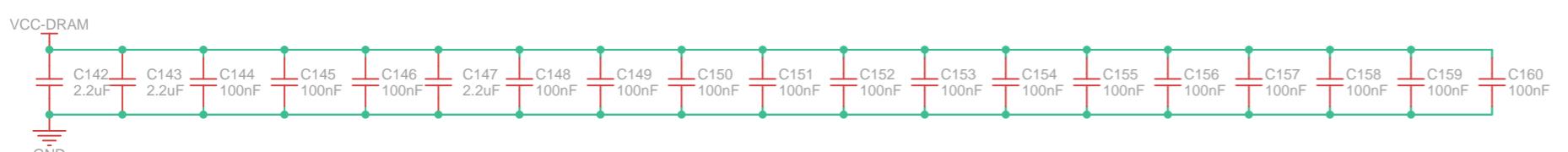
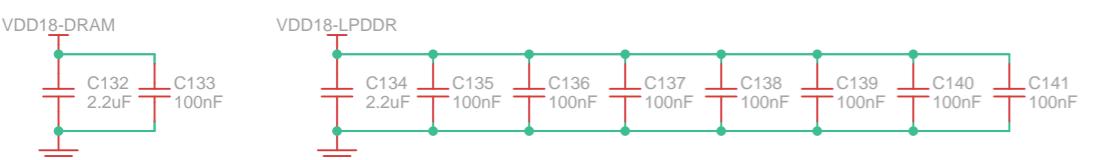
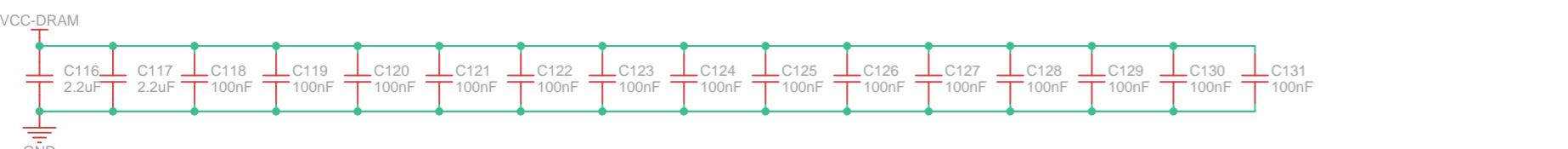
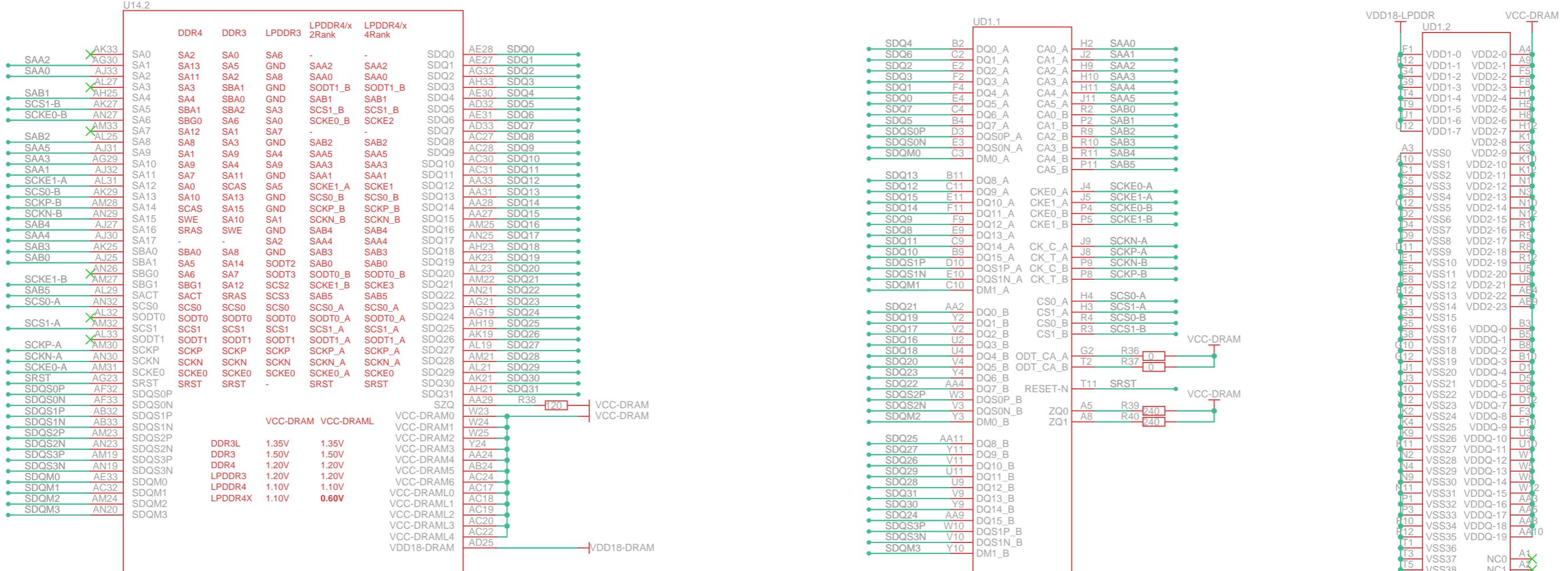


NO.	R1	R2	Boot Select type
1	NC	10K	SMHC0->MLC NAND->SLC NAND->try(except SPI in PJ)
2	10K	1K	SMHC0->SLC NAND->MLC NAND->try(except SPI in PJ)
3	10K	2K2	SMHC0->EMMC_USER->EMMC_BOOT->try(except SPI in PJ)
4	10K	3K9	SMHC0->EMMC_BOOT->EMMC_USER->try(except SPI in PJ)
5	6K8	4K7	SMHC0->SPI NOR->try(except SPI in PJ)
6	6K8	6K8	SMHC0->SPI NAND->try(except SPI in PJ)
7	4K3	6K8	SMHC0->SPI NOR in PJ->try
8	2K2	10K	SMHC0->SPI NAND in PJ->try
9	10K	NC	Reserved

try default order:(selected fail media will not try)
EMMC USER->EMMC BOOT->S1 C NAND->M1 C NAND->SPI NOR->SPI NAND

JTAG-SEL默认为高电平，默认浮空；若要配置为低电平，直接接地即可。此信号为敏感信号，易受ESD等干扰，禁止在实际产品中引出一段浮空走线。
TEST为内部测试引脚，实际应用请做悬空处理，禁止引出一段浮空走线。
FEL/LRADC模块信号接按键时要接1nF去抖动电容，请勿删除或者更改为其他容值。
BOOT_SEL_ADC为存储介质启动先后顺序配置脚，用于调整NAND和EMMC的启动顺序，可以根据产品的需求进行相关配置。T527默认开启BOOT_SEL_ADC pin识别启动顺序。

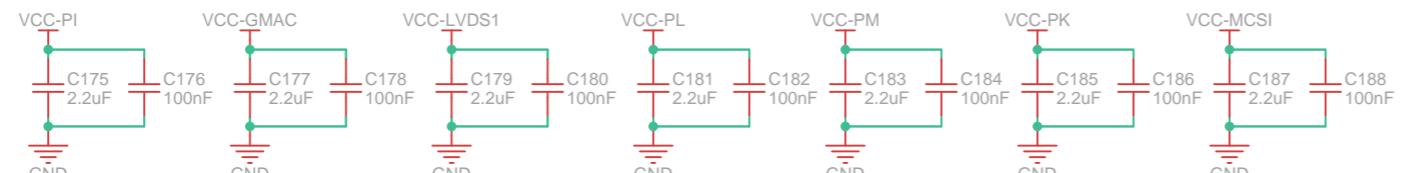


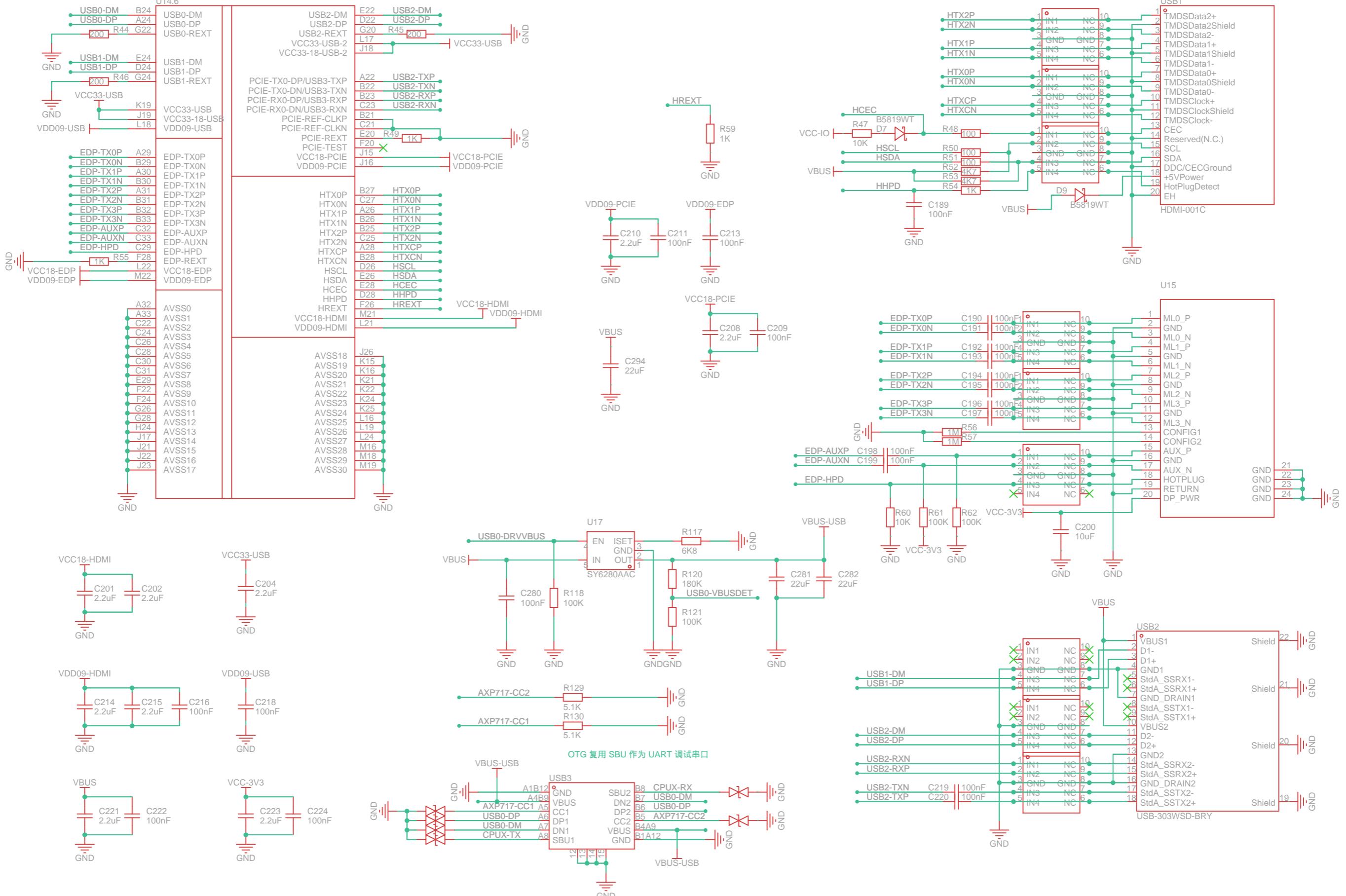


T527支持DDR3/3L、DDR4、LPDDR3、LPDDR4、LPDDR4x，使用时需先确定DRAM的类型、片选及位宽。
DRAM上电时序请严格参照本原理图设计。LPDDR3、LPDDR4、LPDDR4x颗粒需要的VDD18-LPDDR电源使用BLDO2供电；
DDR4颗粒需要的VCC25-DRAM电源需外挂LDO供电。
使用AXP717B BLDO2使能控制输出；LPDDR4颗粒需要的VCC-DRAML电源需外挂DCDC供电，使用AXP717B BLDO2使能控制输出。
DRAM外部部分立器件的数量、值大小以及精度不允许随意更改。请严格参照本原理图设计。
DRAM所有的速度由容不能影响，预留的灌通由容设计在开始阶段预留测试，但不可以不贴片。待开发测试验证稳定之后，量产可以根据实际情况酌情删除。

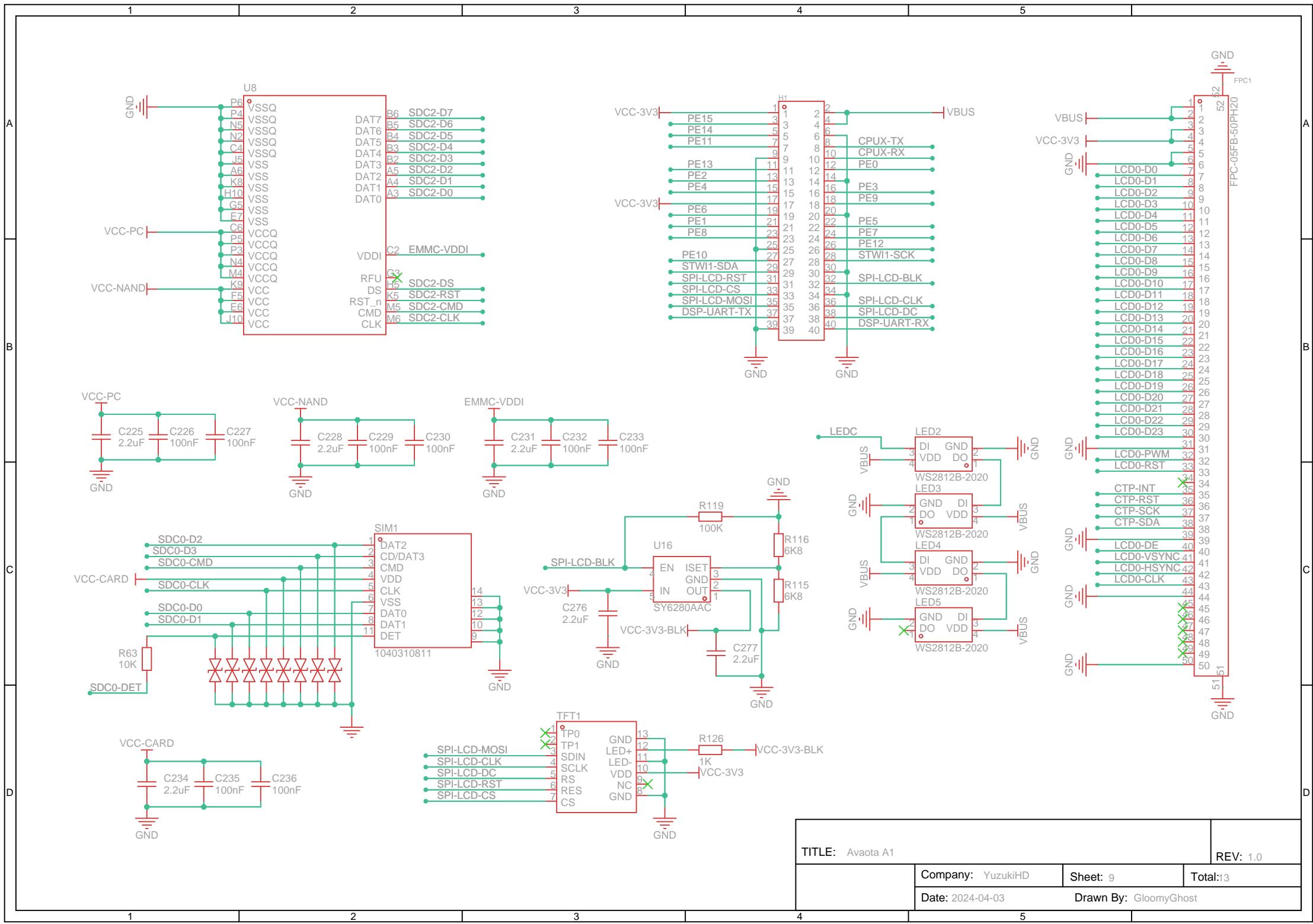
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Date: 2024-02-20 Drawn By: GloomyGhost			
7		8	

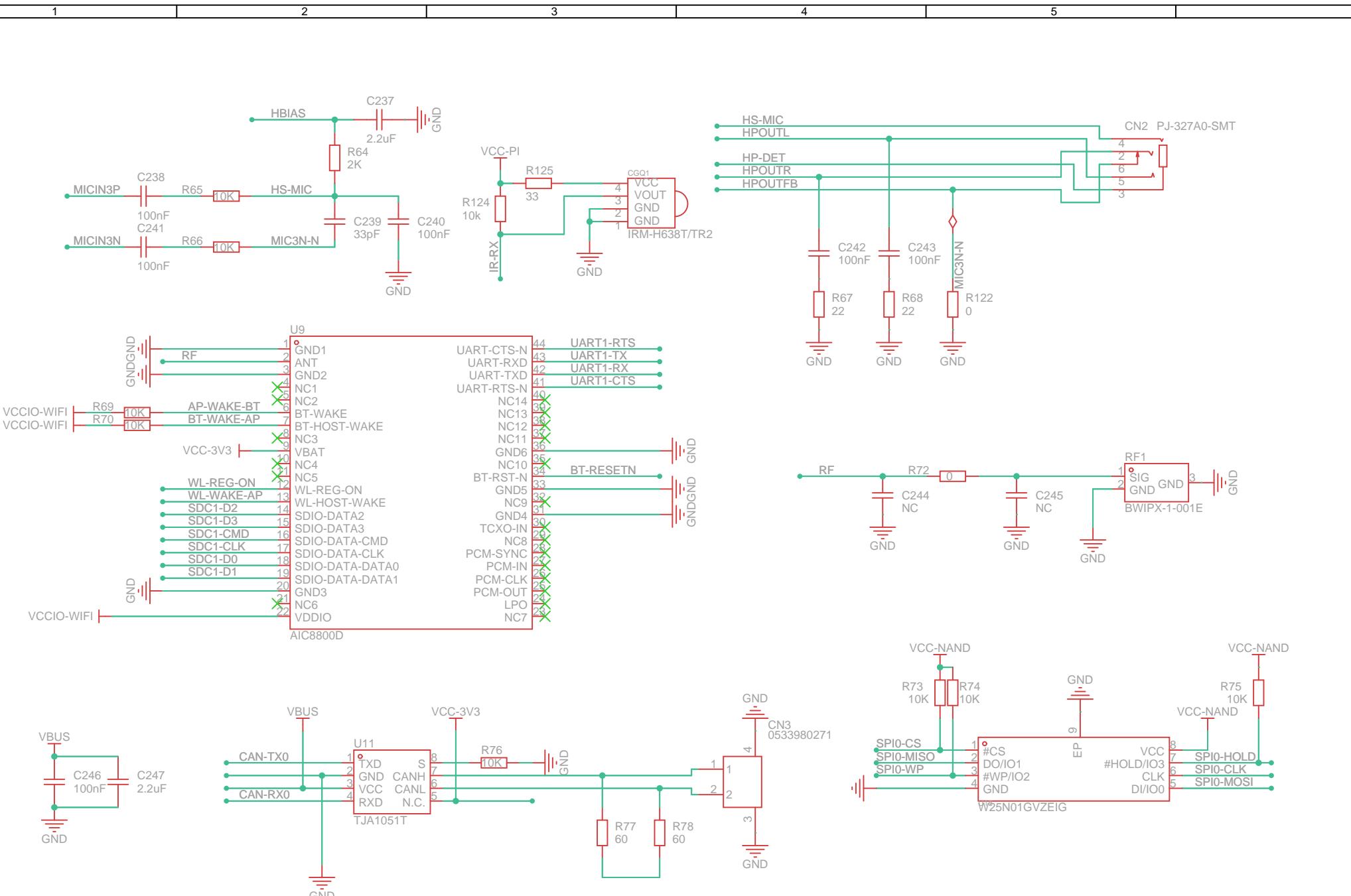






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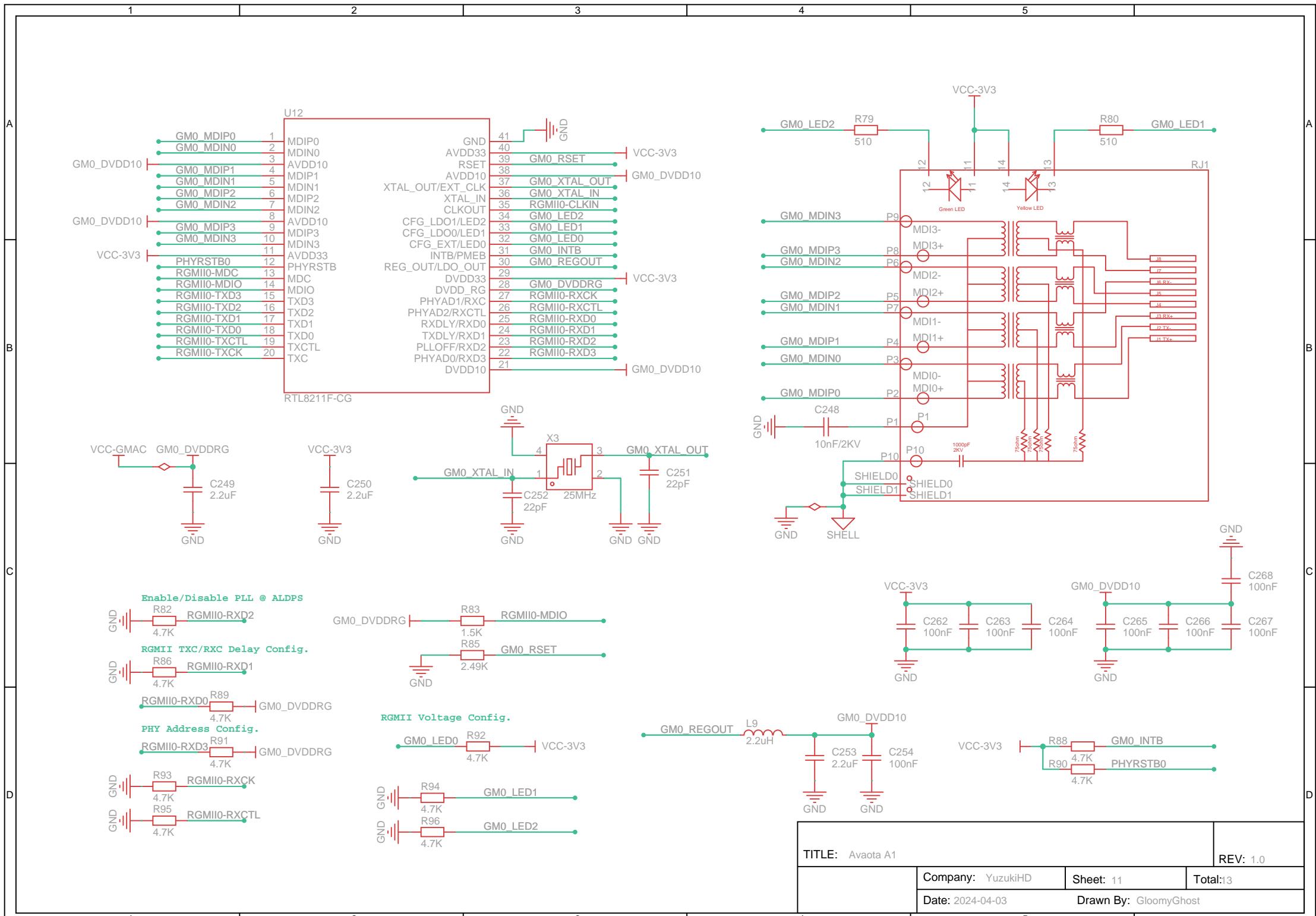


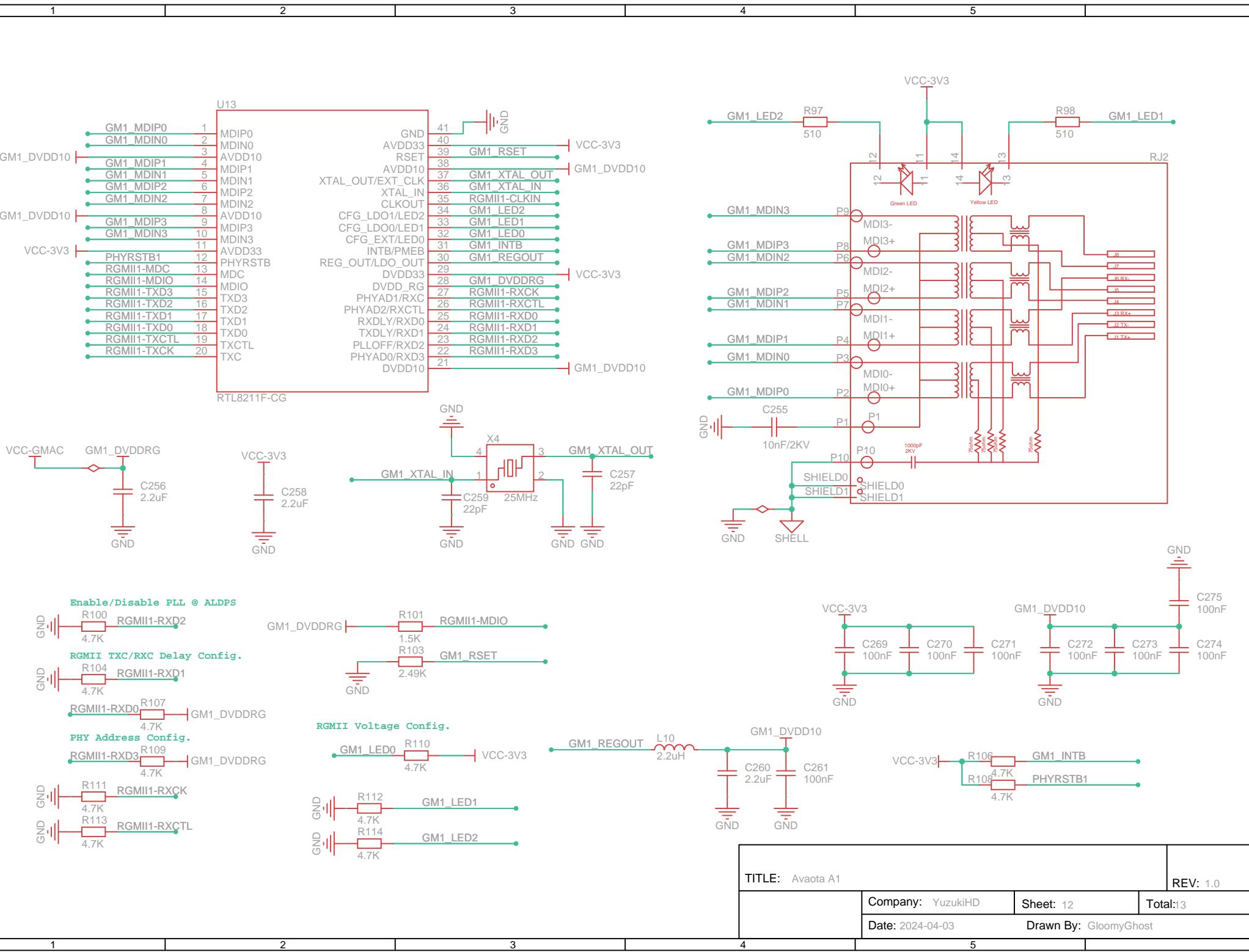


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A

B

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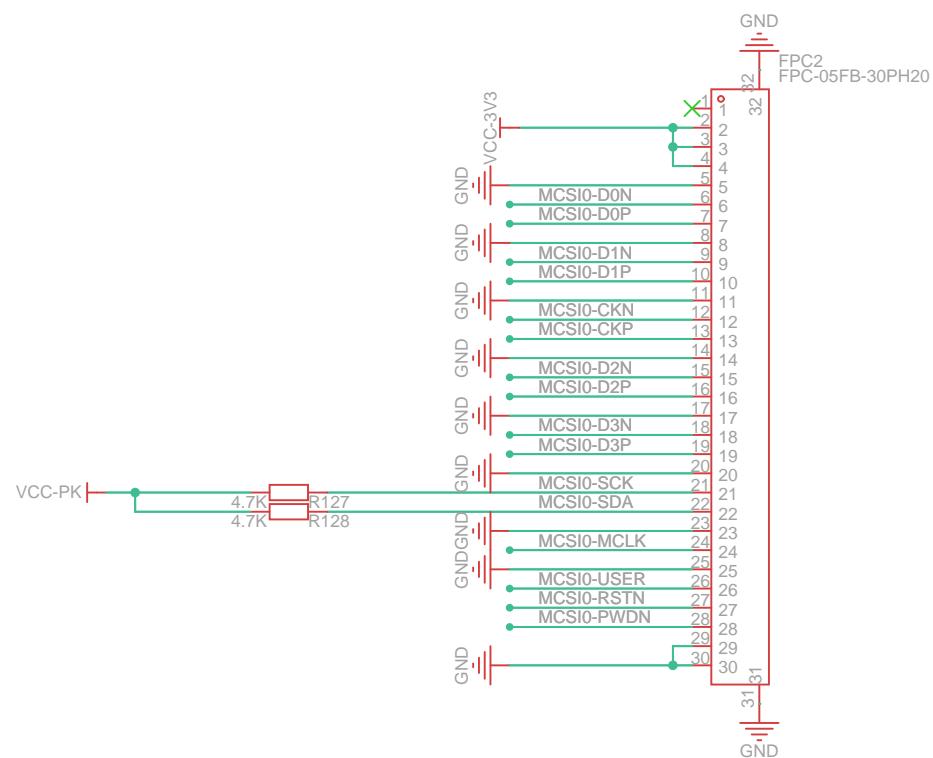
D

A

B

C

D



TITLE: Avaota A1

REV: 1.0

Company: YuzukiHD

Sheet: 13

Total: 13

Date: 2024-02-28

Drawn By: GloomyGhost