

R61529

16,777,216–Color, 320x480-Dot Graphics Liquid Crystal Controller Driver for TFT Panel

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Description

The R61529 is liquid crystal controller driver LSI for TFT panel sized 320RGB x 480-dot at maximum. For efficient data transfer, the R61529 supports MIPI DSI (1 data lane) and MDDI (Ver.1.2 Type 1, 1 data lane) as system interface to microcomputer. The R61529 also supports MIPI DPI, MIPI DBI (Type B), MIPI DBI (Type C), and I²C.

The R61529 incorporates step-up and voltage follower circuits to generate drive voltage required for a-Si TFT and a dynamic backlight control function to control backlight brightness depending on image data, reducing power consumption at the backlight with the slightest influence on image quality. By synchronizing the moving picture data rewrite operation with VSYNC interface/TE effect, the R61529 can display moving picture without tearing.

Other features include a power management function, making the R61529 best suitable for small-and-mid-sized portable devices with color graphics display such as digital mobile phones, small PDAs and Smartphone.

*MIPI: Mobile Industry Processor Interface, *DCS: Display Command Set, *DSI: Display Serial Interface, *DPI: Display Pixel Interface, *DBI: Display Bus Interface, MDDI: Mobile Display Digital Interface, *VESA: Video Electronics Standards Association, *I²C: Inter-Integrated Circuit.

Note: The MDDI supported by the R61529 is designed and produced based on the licensing of technology from Qualcomm. The MDDI must be adopted in the module, which incorporates a Qualcomm's CDMA ASIC. Any claims, including, but not limited to the third party's right to use the MDDI for industrial purposes shall not be accepted by Renesas Electronics unless the above-mentioned condition is met.

Features

- Single chip driver for 16, 777, 216-color TFT 320RGB x 480-dot graphics with LCM power supply circuit
- Resolution: 320RGB x 480 dots
- Panel drive method: Dot inversion and column inversion
- Command set (Compliant with MIPI DCS Version 1.01.00) *DCS: Display Command Set, MDDI
- System interface
 - MIPI DSI (380Mbps/lane @video mode, TBD): 1 data lane/1 clock lane
MIPI DSI: Version 1.01.00r11 21-Feb-2008 (Command mode and video mode are supported)
MIPI D-PHY: Version 1.00.00 14-May-2009
 - MIPI DBI Type B 8bits/16bits/18bits/24bits (MIPI DBI Version 2.00)
 - MIPI DBI Type C Option 1/Option 3 (MIPI DBI Version 2.00)
 - MIPI DPI (MIPI DPI Version 2.00)
 - MDDI Ver.1.2 Type 1 (VESA Mobile Display Digital Interface Standard Version 1,2 July 9, 2008)
 - I²C (Inter-Integrated Circuit)

- Video image display interface (see Note 1)
 - TE-I/F (MIPI DBI + TE synchronization signal output)
 - VSYNC-I/F (MIPI DBI + VSYNC)
 - MIPI DSI TE-reporting
 - MDDI + TE synchronization signal output
- Abundant color display and drawing functions
 - 16,777,216-color display
 - RGB separate γ correction function
 - Partial display function
- Low-power consumption architecture (allowing direct input of interface I/O power supply)
 - Deep standby mode
 - Input power supply voltage:

Interface and logic power supply:	IOVCC1
Analog power supply:	VCI
MIPI D-PHY/MDDI power supply:	IOVCC2
- Dynamic backlight control function
- Internal liquid crystal drive power supply circuit
 - Source driver and VCOM: VSP-AGND
 AGND-VSN
 - DC power supply for VCOM drive: VCOMDC
 - Gate drive power supply: VGH-AGND
 AGND-VGL
- Internal frame memory: 460,800 bytes (320 x 480 x 24 bits)
- Liquid crystal display drive circuits: 960 source signal lines and 480 gate signal lines
- One-chip solution for COG module
- Internal NVM: Data can be rewritten up to 5 times.
- Dummy pins used to fix pin to VCC or GND (see note 2)

Notes: 1. Japanese Patent No. 3,826,159
Korean Patent No. 747,636
United States Patent No. 7,176,870
2. Japanese Patent No. 3,980,066
Korean Patent No. 401,270
Taiwan Patent No. 175,413
United States Patent No. 6,323,930
Japanese Patent No. 4,226,627
United States Patent No. 6,924,868

Power Supply Specification

Table 1 R61529 Power Supply Specification

No.	Item	R61529
1	TFT data lines drive circuit	960 outputs
2	TFT gate lines drive circuit	480 outputs
3	Liquid crystal drive output	S1-S960 V0 ~ V255 grayscales
		G1-G480 VGH-VGL
		VCOMDC VCOMDC = -0.3V ~ -3.0V
4	Input voltages	IOVCC1 (interface voltage) 1.65V ~ 3.30V (See note 1)
		VCI (power supply voltage for LCD drive) 2.40V ~ 3.30V (See note 1)
		IOVCC2 (MIPI DSI-PHY/MDDI power supply) 2.40V ~ 3.30V (See note 2)
5	System interface (MIPI DBI Type B, MIPI DBI Type C, I ² C)	CSX, DCX, WRX, RDX, DIN, DOUT, IM[3:0], RESX, DB23-DB0 (used for DPI, too) IOVCC1-GND (See note 1)
6	Video image display interface (MIPI DPI)	VSYNC, HSYNC, DE, PCLK, DB23- DB0 (used for DBI, too) IOVCC1-GND (See note 1)
7	Differential small- amplitude interface	STB_CLKP/N, DATA0P/N, IOVCC2-GND (See note 2)
8	LED I/F	LEDPWM IOVCC1-GND (See note 1)
9	LCD drive supply voltages	VSP 4.6V ~ 6.0V
		VSN -4.6V ~ -6.0V
		VGH 11.4V ~ 17.8V
		VGL -7.6V ~ -12.8V
		VGH-VGL Max. 28V

Notes:

1. Connect these power supplies to other power supplies on the FPC when they are set at the same electrical potential as other power supplies.
2. Connect to VCI on the FPC. For voltage, see DC Characteristics in Electrical Characteristics.

Block Diagram

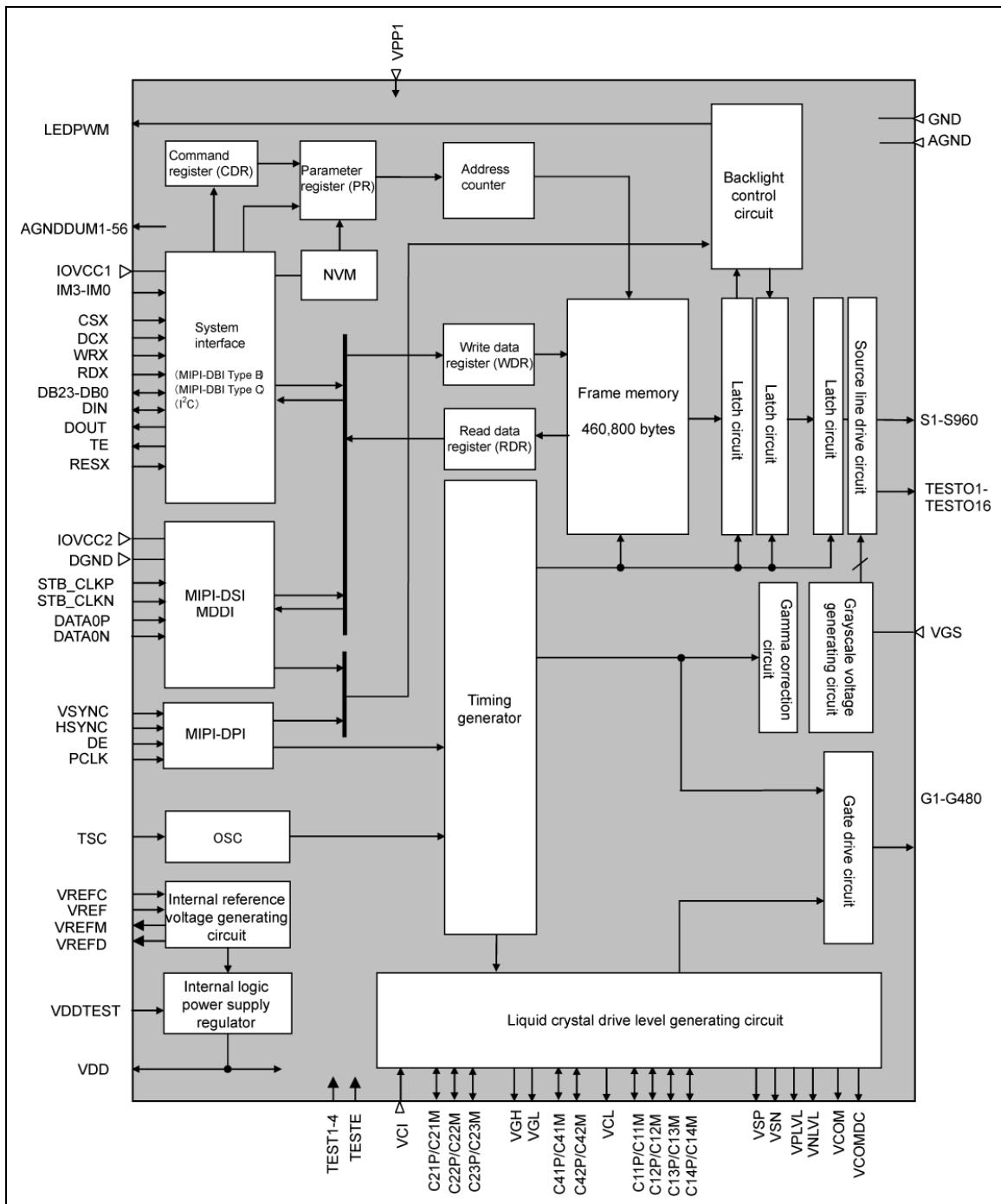


Figure 1

Block Function

1. System Interface

The R61529 supports MIPI DSI (Command Mode and Video Mode), MDDI (Command Mode and Active Refresh Mode), MIPI DBI Type B, MIPI DBI Type C (Option 1 and Option 3), MIPI DPI, and I²C. The R61529 also supports TE synchronization signal and VSYNC interface as display interface for video image.

The interface is selected by setting IM0-3 pins. Using more than one interface set by the IM pins at the same time is inhibited. When MIPI DBI Type C or I²C is selected, display data can be transferred via DPI. When MIPI DBI Type B is selected, display data can be transferred via VSYNC interface. Recommended frame frequency is 58Hz to 63Hz (60Hz±5%). When MIPI DPI, MIPI DSI Video Mode, or MDDI Active Refresh Mode is selected, VSYNC and HSYNC should be input according to frame frequency. Set the number of available colors using set_pixel_format (3Ah).

Changing interface and mode is impossible and prohibited while selected system interface is used.

Table 2

IM3	IM2	IM1	IM0	Interface	Used pin	Number of available colors
0	0	0	0	I ² C (Mode 1) (Notes 2 and 4)	DIN	-
0	0	0	1	MIPI DBI Type C 9 bits (Option 1) (Note 3)	DIN, DOUT	-
0	0	1	0	MDDI	DATA0P/N	262,144 / 16,777,216
0	0	1	1	MIPI DSI Command Mode	DATA0P/N	262,144 / 16,777,216
0	1	0	0	MIPI DBI Type B 8 bits (Note 4)	DB7-DB0	65,536 / 262,144 / 16,777,216
0	1	0	1	MIPI DBI Type B 16 bits (Note 4)	DB15-DB0	65,536 / 262,144 / 16,777,216
0	1	1	0	MIPI DBI Type B 18 bits (Notes 1 and 4)	DB17-DB0	65,536 / 262,144 / 16,777,216
0	1	1	1	MIPI DBI Type B 24 bits (Notes 1 and 4)	DB23-DB0	65,536 / 262,144 / 16,777,216
1	0	0	0	I ² C (Mode 2) (Notes 2 and 4)	DIN	-
1	0	0	1	MIPI DBI Type C 8 bits (Option 3) (Note 3)	DIN, DOUT	-
1	0	1	0	MDDI Active Refresh Mode	DATA0P/N	262,144 / 16,777,216
1	0	1	1	MIPI DSI Video Mode	DATA0P/N	262,144 / 16,777,216
1	1	0	0	Setting inhibited	-	-
1	1	0	1	Setting inhibited	-	-
1	1	1	0	Setting inhibited	-	-
1	1	1	1	Setting inhibited	-	-

- Notes:
1. MIPI DBI Type B standard does not define these interfaces.
 2. When I²C is selected, DPI is selected for display operation. For details, see "System Interface Configuration (I²C)."
 3. When MIPI DBI Type C is selected, DPI is selected for display operation.
 4. When I²C or MIPI DBI Type B is selected, display operation is selected by DM[1:0] of B4h command.

(a) MIPI DSI

The R61529 supports MIPI DSI (Command Mode and Video Mode).

(b) MIPI DBI Type B

The R61529 supports MIPI DBI Type B (8/16/18/24 bits) that uses command method which has 8-bit command registers and 8-bit parameter registers. Also, the R61529 has a 24-bit write register (WDR) and read register (RDR). The WDR is used to store data temporarily that is automatically written to the internal frame memory through internal operation of the chip. The RDR is used to temporarily store the data read out from the frame memory. When reading data from the frame memory, the R61529 first stores the data in the RDR. For this reason, invalid data is sent to the data bus at first and valid data is sent as the R61529 reads second and subsequent data from the frame memory.

Table 3 Register Selection

DCX	RDX	WRX	Function
0	1	↑	Command
1	↑	1	Read parameter
1	1	↑	Write parameter

(c) MIPI DBI Type C (Option 1 and Option 3)

The R61529 supports 9-bit (Option 1) and 8-bit (Option 3) serial interface that uses signals CSX, DCX, WRX, DIN, and DOUT.

(d) MDDI

The R61529 supports MDDI as a differential small amplitude serial interface for high-speed data transfer via STB_CLKP, STB_CLKN, DATA0P and DATA0N. The number of data lanes can be chosen.

2. Video Image Interface

The R61529 supports TE synchronization signal, DPI, and VSYNC interface as display interface for video image. When DBI is selected, display data is written in synchronization with TE signal which is generated from internal clock to prevent flicker on the panel. When DSI is selected, display data is written in synchronization with a start of the frame period by TE-reporting function. This enables updating image data without flicker on the panel.

In VSYNC interface operation, the display operation is synchronized with the internal clock except frame synchronization, i.e. synchronization with the VSYNC signal. The R61529 writes display data to the frame memory via system interface (DBI).

When DPI is selected, externally supplied VSYNC, HSYNC, and PCLK signals drive the chip. Display data (DB[23:0]) is written in synchronization with those synchronous signals following data enable signal (DE). This enables updating image data without flicker on the panel. The R61529 does not write the display data to the frame memory.

Data written in MIPI DSI Video Mode and MDDI Active Refresh Mode, too, is directly output as display data without being written to internal RAM.

3. Frame Memory

The R61529 incorporates the frame memory that has a capacity of 460,800 bytes, which can store bit-pattern data of 320RGB x 480 graphics display at the maximum using 24 bits to represent one pixel.

4. Grayscale Voltage Generating Circuit

The grayscale voltage generating circuit generates liquid crystal drive voltage according to the grayscale setting value in the γ correction register. RGB separate γ correction setting enables maximum 16,777,216-color display.

5. LCD Drive Power Supply Circuit

The LCD drive power supply circuit generates VPLVL, VNLVL, VGH, VGL, VCOMDC levels to drive the liquid crystal panel.

6. Timing Generator

The timing generator is used to generate timing signals for operating internal circuits.

7. Oscillator (OSC)

The R61529 incorporates an oscillator.

8. LCD Driver Circuit

The LCD driver circuit has a 960-channel source driver (S1-S960). When 320RGB pixels of data are input, the display pattern data is latched. The voltage is output from the source driver according to the latched data. The gate driver circuit consists of a 480-channel gate driver (G1-480). The voltage at VGH level or VGL level is output from the gate driver. The shift direction of gate output can be changed by GS bit (C0h). The scan mode of the gate driver can be changed by SM bit (C0h) according to the mounting condition.

9. Internal Logic Power Supply Regulator

The internal logic power supply regulator generates power supply for the internal logic circuit.

10. Backlight Control Circuit

The backlight control circuit adjusts backlight brightness according to the histogram of image to reduce power consumption at the backlight. Brightness of the backlight and display data is adjusted.

11. NVM

The R61529 supports NVM that stores manufacturer command setting values.

Pin Function

Table 4 External Power Supply Pins

Signal	I/O	Connect to	Function	Connection when signal is unused
VCI	I	Power supply	Power supply to analog circuit. VCI < 0.3V (When power is turned off.)	-
IOVCC1	I	Power supply	Power supply to interface pins. IOVCC1 < 0.3V (When power is turned off.)	-
IOVCC2	I	Power supply	Power supply to MIPI DSI D-PHY and MDDI. Connect to VCI on the FPC to prevent noise in case of COG.	-
GND	I	Power supply	GND for internal logic and interface pins. GND=0V.	-
AGND	I	Power supply	Analog GND (logic regulator and LCD power supply circuit). AGND = 0V. Connect to GND on the FPC to prevent noise in case of COG.	-
DGND	I	Power supply	GND for MIPI DSI D-PHY and MDDI. Connect to GND on the FPC to prevent noise in case of COG.	-

Table 5 System Interface Pins (Amplitude: IOVCC1 - GND)

Signal	I/O	Connect to	Function	Connection when signal is unused
IM0, IM1, IM2, IM3	I	IOVCC1 or GND	Interface select signal. Select interface from MIPI DSI, MIPI DBI Type B, MIPI DBI Type C (Option 1 and Option 3), MDDI, I ² C, and MIPI DPI. See "Block Function."	-
RESX	I	Host Processor or external RC circuit	Reset pin. The R61529 is initialized when RESX is Low. Make sure to execute power-on reset when turning power supply on.	-
TE	O	Host processor	Tearing effect output signal. When data is written to NVM, it can be used as a verify signal according to register setting. Leave open if it is not used.	Open

Table 6 MIPI DBI Type B/MIPI DBI Type C/I²C Pins (Amplitude: IOVCC1 - GND)

Signal	I/O	Connect to	Function	Connection when signal is unused
CSX	I	Host Processor	Chip select signal. Low: Select (Accessible) High: Not Select (Inaccessible) Make sure to connect to the host processor and control following AC characteristics. This pin releases shutdown mode.	IOVCC1
DCX	I	Host Processor	Command/data select signal. Low: Select command High: Select data	IOVCC1
WRX	I	Host Processor	Write strobe signal in MIPI DBI Type B operation When WRX is Low, write data. A synchronous clock signal in MIPI DBI Type C and I ² C operation.	IOVCC1
RDX	I	Host Processor	Read strobe signal. Read out data when RDX is Low.	IOVCC1
DB23-0	I/O	Host Processor	In MIPI DBI Type-B operation. 8-bit interface: Use DB7-0 16-bit interface: Use DB15-0 18-bit interface: Use DB17-0 24-bit interface: Use DB23-0 DPI operation Use DB23-0 Abnormal current (through current) does not occur when CSX is High and the data bus is Hi-Z.	IOVCC1 or GND
DIN	I/O	Host Processor	A serial data input pin in MIPI Type C operation to input data on the rising edge of the SCL signal. A serial input/output and ACK output pin in I ² C operation.	IOVCC1 or GND
DOUT	O	Host Processor	A serial data output pin in MIPI DBI Type C operation to input data on the rising edge of the SCL signal.	Open

Table 7 MIPI DPI Pins (Amplitude: IOVCC1 - GND)

Signal	I/O	Connect to	Function	Connection when signal is unused
VSYNC	I	Host Processor	Flame synchronous signal in MIPI DPI operation. Signal polarity can be chosen by VSPL (C6h). For details, see section "DPI Polarity Control (C6h)."	IOVCC1 or GND
H SYNC	I	Host Processor	Line synchronous signal in DPI operation. Signal polarity can be chosen by HSPL (C6h). For details, see section "DPI Polarity Control (C6h)."	IOVCC1 or GND
DE	I	Host Processor	Data Enable signal in MIPI DPI operation. Signal polarity can be chosen by EPL (C6h). For details, see section "DPI Polarity Control (C6h)."	IOVCC1 or GND
PCLK	I	Host Processor	Pixel clock signal in MIPI DPI operation. Signal polarity can be chosen by DPL (C6h). For details, see section "DPI Polarity Control (C6h)."	IOVCC1 or GND

Table 8 MIPI DSI Pins (Amplitude: IOVCC2 - GND)

Signal	I/O	Connect to	Function	Connection when signal is unused
STB_CLKP	I	Host Processor	MIPI DSI Clock / MDDI strobe signal line (+).	DGND
STB_CLKN	I	Host Processor	MIPI DSI Clock / MDDI strobe signal line (-).	DGND
DATA0P	I/O	Host Processor	MIPI DSI / MDDI data-0 signal lines (+).	DGND
DATA0N	I/O	Host Processor	MIPI DSI / MDDI data-0 signal line (-).	DGND

Table 9 LED Driver Control Pins (Amplitude: IOVCC1 -GND)

Signal	I/O	Connect to	Function	Connection when signal is unused
LEDPWM	O	LED driver	Control signal for brightness of LED backlight. PWM signal's width is selected from 256 values between 0% (Low) and 100% (High). When light is turned on, LEDPWM is High. When light is turned off, LEDPWM is Low.	Open

Table 10 Power Supply Circuit Pins

Signal	I/O	Connect to	Function	Connection when signal is unused
VDD	O	Stabilizing capacitor	Outputs from internal logic power supply regulator. Connect to stabilizing capacitor.	-
VGH	O	Liquid crystal panel	Liquid crystal drive power supply. Pin to output voltage from positive side of liquid crystal panel. Sleep mode: GND NVM write/erase operation: about 9V Display on sequence and display operation: VGH (according to VC1[2:0] and VC2[2:0] setting)	-
VGL	O	Liquid crystal panel	Liquid crystal drive power supply. Pin to output voltage from negative side of liquid crystal panel. Sleep mode: GND NVM write/erase operation: about -9V Display on sequence and display operation: VGL (according to VC1[2:0] and VC2[2:0] setting)	-
C11P, C11M, C12P, C12M C13P, C13M, C14P, C14M	I/O	Step-up capacitor	Capacitor connection pins to generate VSP and VSN with a circuit. For details, see "Power Supply Generating Circuit."	-
C21P, C21M, C22P, C22M C23P, C23M	I/O	Step-up capacitor	Capacitor connection pins for the step-up circuit. For details, see "Power Supply Generating Circuit."	-
C41P, C41M, C42P, C42M	I/O	Step-up capacitor	Connect to external capacitor for generating VCL. For details, see "Power Supply Generating Circuit."	-
VCL	O	Liquid crystal panel	Used for VSN reference voltage.	-

Table 11 Liquid Crystal Drive Pins

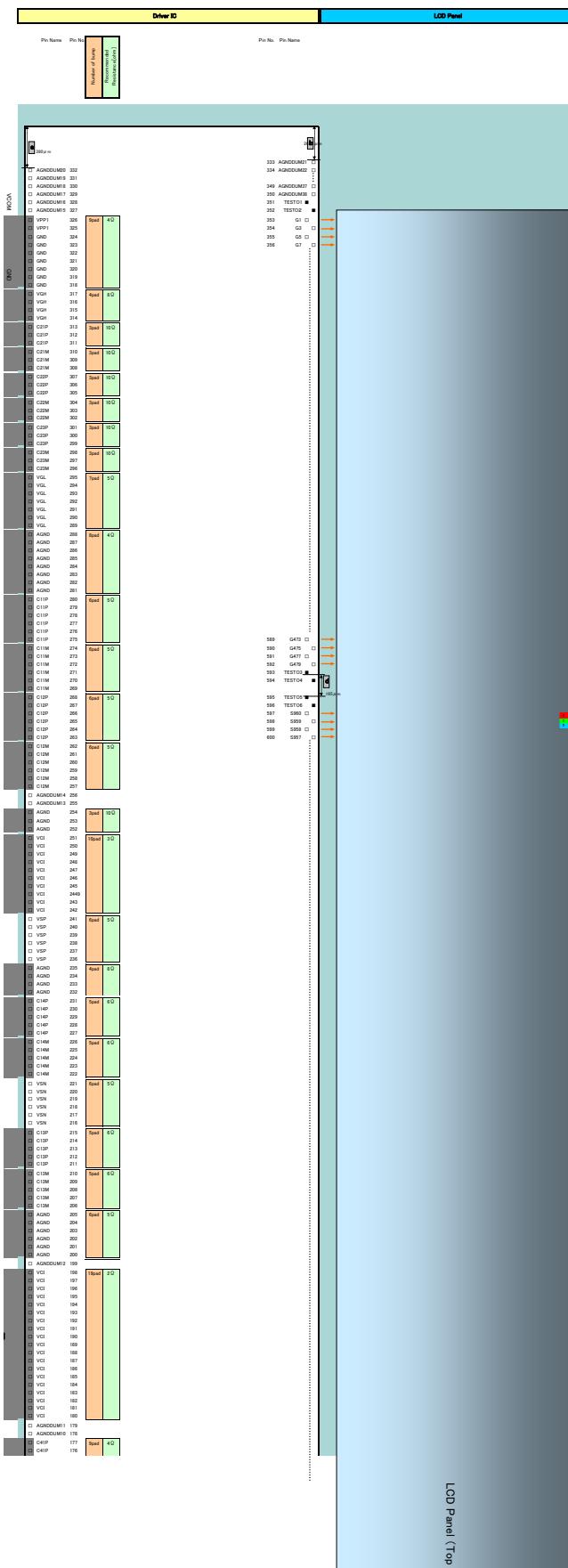
Signal	I/O	Connect to	Function	Connection when signal is unused
VCOMDC	O	Stabilizing capacitor	VCOMDC level, which is set by internal electronic volume. Do not use VCOMDC as VCOM that supplies voltage to liquid crystal panel. Stabilizing capacitor can be omitted according to image quality.	-
VCOM	O	Liquid crystal display	VCOM level, which is supplied to liquid crystal panel.	-
VGS	I	AGND	Reference level of the grayscale voltage generating circuit (GND level).	-
VSN	O	Open	Negative step-up voltage for source drivers and gamma circuit.	-
VSP	O	Open	Positive step-up voltage for source drivers and gamma circuit.	-
VPLVL	O	Stabilizing capacitor	Reference voltage for liquid crystal display at positive side. Stabilizing capacitor can be removed according to image quality.	-
VNLVL	O	Stabilizing capacitor	Reference voltage for liquid crystal display at negative side. Stabilizing capacitor can be removed according to image quality.	-
S1-S960	O	Liquid crystal panel	Liquid crystal application voltages.	Open
G1-G480	O	Liquid crystal display	Gate line output signals. VGH: Gate line is selected. VGL: Gate line is not selected.	Open
TESTO1-TESTO16	O	Open	Test pins. Leave open.	Open

Table 12 Other Pins (Test and Dummy)

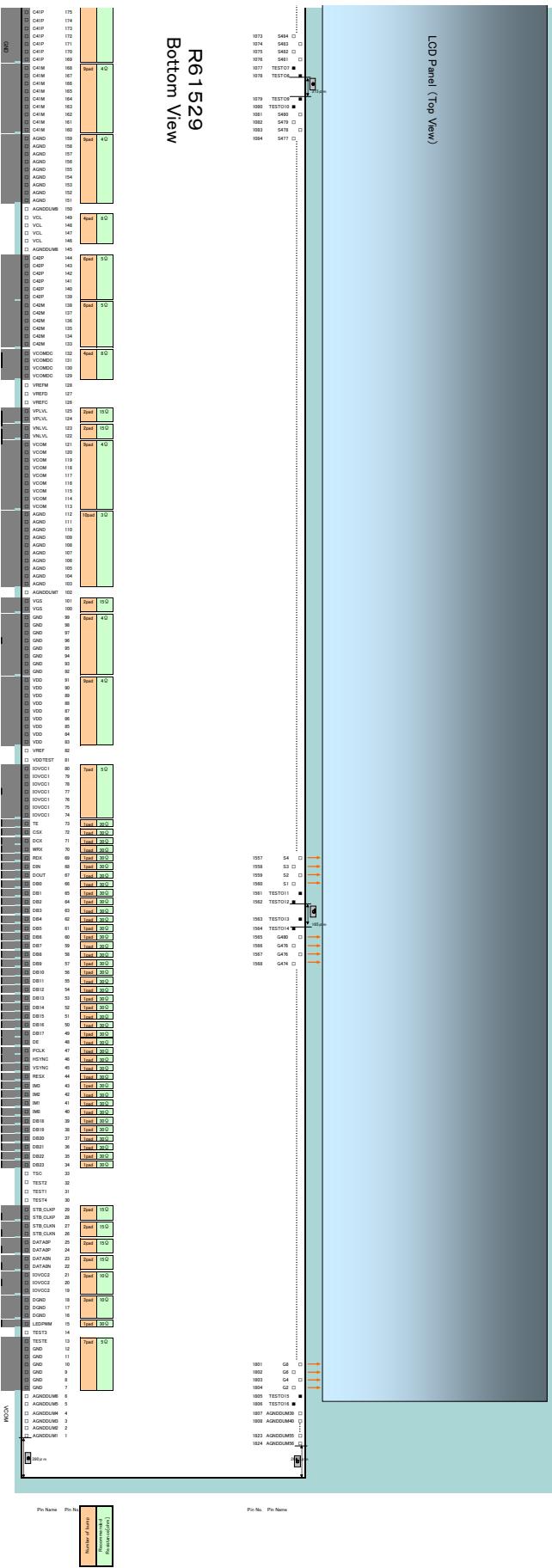
Signal	I/O	Connect to	Function	Connection when signal is unused
VREFC	I	GND	Test pin. Leave open.	Open
VREF	O	Open	Test pin. Leave open.	Open
VREFM	O	Open	Test pin. Leave open.	Open
VREFD	O	Open	Test pin. Leave open.	Open
VDDTEST	I	GND	Test pin. Leave open.	Open
AGNDDUM 1-56	O	—	Used to fix electric potential. Connect to unused interface or test pins to fix electric potential on the glass. If not, leave open.	Open
TEST1-4	I	GND	Test pins. Leave open.	Open
TESTE	I	GND	Test pins. Connects VREFC, VDDTEST, TEST1-4, and TSC to GND via a pull-down resistor.	GND
TSC	I	GND	Test pin. Leave open.	Open
VPP1	I	GND	Test pin. Connect to AGND or leave open. To leave open, do not draw ITO wiring.	Open or GND

Pad Arrangement

2010/7/9 The same contents as Recommended Resistance/Recommended Connection (Rev.0.4 2010.04.22)
 (Updated!) drawn for a bottom view (glass: top view). The number of pads added.



LCD Panel (Top View)



R61529 Pad Coordinate (Unit: μm)

pad No	pad name	X	Y
1	AGNDDUM1	-11585	-419
2	AGNDDUM2	-11515	-419
3	AGNDDUM3	-11445	-419
4	AGNDDUM4	-11375	-419
5	AGNDDUM5	-11305	-419
6	AGNDDUM6	-11235	-419
7	GND	-11165	-419
8	GND	-11095	-419
9	GND	-11025	-419
10	GND	-10955	-419
11	GND	-10885	-419
12	GND	-10815	-419
13	TESTE	-10745	-419
14	TEST3	-10675	-419
15	LEDPWM	-10605	-419
16	DGND	-10535	-419
17	DGND	-10465	-419
18	DGND	-10395	-419
19	IOVCC2	-10325	-419
20	IOVCC2	-10255	-419
21	IOVCC2	-10185	-419
22	DATA0N	-10115	-419
23	DATA0N	-10045	-419
24	DATA0P	-9975	-419
25	DATA0P	-9905	-419
26	STB_CLKN	-9835	-419
27	STB_CLKN	-9765	-419
28	STB_CLKP	-9695	-419
29	STB_CLKP	-9625	-419
30	TEST4	-9555	-419
31	TEST1	-9485	-419
32	TEST2	-9415	-419
33	TSC	-9345	-419
34	DB23	-9275	-419
35	DB22	-9205	-419
36	DB21	-9135	-419
37	DB20	-9065	-419
38	DB19	-8995	-419
39	DB18	-8925	-419
40	IM0	-8855	-419
41	IM1	-8785	-419
42	IM2	-8715	-419
43	IM3	-8645	-419
44	RESX	-8575	-419
45	VSYNC	-8505	-419
46	HSYNC	-8435	-419
47	PCLK	-8365	-419
48	DE	-8295	-419
49	DB17	-8225	-419
50	DB16	-8155	-419

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pad No	pad name	X	Y
51	DB15	-8085	-419
52	DB14	-8015	-419
53	DB13	-7945	-419
54	DB12	-7875	-419
55	DB11	-7805	-419
56	DB10	-7735	-419
57	DB9	-7665	-419
58	DB8	-7595	-419
59	DB7	-7525	-419
60	DB6	-7455	-419
61	DB5	-7385	-419
62	DB4	-7315	-419
63	DB3	-7245	-419
64	DB2	-7175	-419
65	DB1	-7105	-419
66	DB0	-7035	-419
67	DOUT	-6965	-419
68	DIN	-6895	-419
69	RDX	-6825	-419
70	WRX	-6755	-419
71	DCX	-6685	-419
72	CSX	-6615	-419
73	TE	-6545	-419
74	IOVCC1	-6475	-419
75	IOVCC1	-6405	-419
76	IOVCC1	-6335	-419
77	IOVCC1	-6265	-419
78	IOVCC1	-6195	-419
79	IOVCC1	-6125	-419
80	IOVCC1	-6055	-419
81	VDDTEST	-5985	-419
82	VREF	-5915	-419
83	VDD	-5845	-419
84	VDD	-5775	-419
85	VDD	-5705	-419
86	VDD	-5635	-419
87	VDD	-5565	-419
88	VDD	-5495	-419
89	VDD	-5425	-419
90	VDD	-5355	-419
91	VDD	-5285	-419
92	GND	-5215	-419
93	GND	-5145	-419
94	GND	-5075	-419
95	GND	-5005	-419
96	GND	-4935	-419
97	GND	-4865	-419
98	GND	-4795	-419
99	GND	-4725	-419
100	VGS	-4655	-419

R61529 Pad Coordinate (Unit : μm)

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pad No	pad name	X	Y
101	VGS	-4585	-419
102	AGNDDUM7	-4515	-419
103	AGND	-4445	-419
104	AGND	-4375	-419
105	AGND	-4305	-419
106	AGND	-4235	-419
107	AGND	-4165	-419
108	AGND	-4095	-419
109	AGND	-4025	-419
110	AGND	-3955	-419
111	AGND	-3885	-419
112	AGND	-3815	-419
113	VCOM	-3745	-419
114	VCOM	-3675	-419
115	VCOM	-3605	-419
116	VCOM	-3535	-419
117	VCOM	-3465	-419
118	VCOM	-3395	-419
119	VCOM	-3325	-419
120	VCOM	-3255	-419
121	VCOM	-3185	-419
122	VNLVL	-3115	-419
123	VNLVL	-3045	-419
124	VPLVL	-2975	-419
125	VPLVL	-2905	-419
126	VREFC	-2835	-419
127	VREFD	-2765	-419
128	VREFM	-2695	-419
129	VCOMDC	-2625	-419
130	VCOMDC	-2555	-419
131	VCOMDC	-2485	-419
132	VCOMDC	-2415	-419
133	C42M	-2345	-419
134	C42M	-2275	-419
135	C42M	-2205	-419
136	C42M	-2135	-419
137	C42M	-2065	-419
138	C42M	-1995	-419
139	C42P	-1925	-419
140	C42P	-1855	-419
141	C42P	-1785	-419
142	C42P	-1715	-419
143	C42P	-1645	-419
144	C42P	-1575	-419
145	AGNDDUM8	-1505	-419
146	VCL	-1435	-419
147	VCL	-1365	-419
148	VCL	-1295	-419
149	VCL	-1225	-419
150	AGNDDUM9	-1155	-419

pad No	pad name	X	Y
151	AGND	-1085	-419
152	AGND	-1015	-419
153	AGND	-945	-419
154	AGND	-875	-419
155	AGND	-805	-419
156	AGND	-735	-419
157	AGND	-665	-419
158	AGND	-595	-419
159	AGND	-525	-419
160	C41M	-455	-419
161	C41M	-385	-419
162	C41M	-315	-419
163	C41M	-245	-419
164	C41M	-175	-419
165	C41M	-105	-419
166	C41M	-35	-419
167	C41M	35	-419
168	C41M	105	-419
169	C41P	175	-419
170	C41P	245	-419
171	C41P	315	-419
172	C41P	385	-419
173	C41P	455	-419
174	C41P	525	-419
175	C41P	595	-419
176	C41P	665	-419
177	C41P	735	-419
178	AGNDDUM10	805	-419
179	AGNDDUM11	875	-419
180	VCI	945	-419
181	VCI	1015	-419
182	VCI	1085	-419
183	VCI	1155	-419
184	VCI	1225	-419
185	VCI	1295	-419
186	VCI	1365	-419
187	VCI	1435	-419
188	VCI	1505	-419
189	VCI	1575	-419
190	VCI	1645	-419
191	VCI	1715	-419
192	VCI	1785	-419
193	VCI	1855	-419
194	VCI	1925	-419
195	VCI	1995	-419
196	VCI	2065	-419
197	VCI	2135	-419
198	VCI	2205	-419
199	AGNDDUM12	2275	-419
200	AGND	2345	-419

R61529 Pad Coordinate (Unit : μm)

pad No	pad name	X	Y
201	AGND	2415	-419
202	AGND	2485	-419
203	AGND	2555	-419
204	AGND	2625	-419
205	AGND	2695	-419
206	C13M	2765	-419
207	C13M	2835	-419
208	C13M	2905	-419
209	C13M	2975	-419
210	C13M	3045	-419
211	C13P	3115	-419
212	C13P	3185	-419
213	C13P	3255	-419
214	C13P	3325	-419
215	C13P	3395	-419
216	VSN	3465	-419
217	VSN	3535	-419
218	VSN	3605	-419
219	VSN	3675	-419
220	VSN	3745	-419
221	VSN	3815	-419
222	C14M	3885	-419
223	C14M	3955	-419
224	C14M	4025	-419
225	C14M	4095	-419
226	C14M	4165	-419
227	C14P	4235	-419
228	C14P	4305	-419
229	C14P	4375	-419
230	C14P	4445	-419
231	C14P	4515	-419
232	AGND	4585	-419
233	AGND	4655	-419
234	AGND	4725	-419
235	AGND	4795	-419
236	VSP	4865	-419
237	VSP	4935	-419
238	VSP	5005	-419
239	VSP	5075	-419
240	VSP	5145	-419
241	VSP	5215	-419
242	VCI	5285	-419
243	VCI	5355	-419
244	VCI	5425	-419
245	VCI	5495	-419
246	VCI	5565	-419
247	VCI	5635	-419
248	VCI	5705	-419
249	VCI	5775	-419
250	VCI	5845	-419

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pad No	pad name	X	Y
251	VCI	5915	-419
252	AGND	5985	-419
253	AGND	6055	-419
254	AGND	6125	-419
255	AGNDDUM13	6195	-419
256	AGNDDUM14	6265	-419
257	C12M	6335	-419
258	C12M	6405	-419
259	C12M	6475	-419
260	C12M	6545	-419
261	C12M	6615	-419
262	C12M	6685	-419
263	C12P	6755	-419
264	C12P	6825	-419
265	C12P	6895	-419
266	C12P	6965	-419
267	C12P	7035	-419
268	C12P	7105	-419
269	C11M	7175	-419
270	C11M	7245	-419
271	C11M	7315	-419
272	C11M	7385	-419
273	C11M	7455	-419
274	C11M	7525	-419
275	C11P	7595	-419
276	C11P	7665	-419
277	C11P	7735	-419
278	C11P	7805	-419
279	C11P	7875	-419
280	C11P	7945	-419
281	AGND	8015	-419
282	AGND	8085	-419
283	AGND	8155	-419
284	AGND	8225	-419
285	AGND	8295	-419
286	AGND	8365	-419
287	AGND	8435	-419
288	AGND	8505	-419
289	VGL	8575	-419
290	VGL	8645	-419
291	VGL	8715	-419
292	VGL	8785	-419
293	VGL	8855	-419
294	VGL	8925	-419
295	VGL	8995	-419
296	C23M	9065	-419
297	C23M	9135	-419
298	C23M	9205	-419
299	C23P	9275	-419
300	C23P	9345	-419

R61529 Pad Coordinate (Unit : μm)

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pad No	pad name	X	Y
301	C23P	9415	-419
302	C22M	9485	-419
303	C22M	9555	-419
304	C22M	9625	-419
305	C22P	9695	-419
306	C22P	9765	-419
307	C22P	9835	-419
308	C21M	9905	-419
309	C21M	9975	-419
310	C21M	10045	-419
311	C21P	10115	-419
312	C21P	10185	-419
313	C21P	10255	-419
314	VGH	10325	-419
315	VGH	10395	-419
316	VGH	10465	-419
317	VGH	10535	-419
318	GND	10605	-419
319	GND	10675	-419
320	GND	10745	-419
321	GND	10815	-419
322	GND	10885	-419
323	GND	10955	-419
324	GND	11025	-419
325	VPP1	11095	-419
326	VPP1	11165	-419
327	AGNDDUM15	11235	-419
328	AGNDDUM16	11305	-419
329	AGNDDUM17	11375	-419
330	AGNDDUM18	11445	-419
331	AGNDDUM19	11515	-419
332	AGNDDUM20	11585	-419
333	AGNDDUM21	11730	430
334	AGNDDUM22	11700	430
335	AGNDDUM23	11670	430
336	AGNDDUM24	11640	430
337	AGNDDUM25	11610	430
338	AGNDDUM26	11580	430
339	AGNDDUM27	11550	430
340	AGNDDUM28	11520	430
341	AGNDDUM29	11490	430
342	AGNDDUM30	11460	430
343	AGNDDUM31	11430	430
344	AGNDDUM32	11400	430
345	AGNDDUM33	11370	430
346	AGNDDUM34	11340	430
347	AGNDDUM35	11310	430
348	AGNDDUM36	11280	430
349	AGNDDUM37	11250	430
350	AGNDDUM38	11220	430

pad No	pad name	X	Y
351	TESTO1	11205	305
352	TESTO2	11190	430
353	G1	11175	305
354	G3	11160	430
355	G5	11145	305
356	G7	11130	430
357	G9	11115	305
358	G11	11100	430
359	G13	11085	305
360	G15	11070	430
361	G17	11055	305
362	G19	11040	430
363	G21	11025	305
364	G23	11010	430
365	G25	10995	305
366	G27	10980	430
367	G29	10965	305
368	G31	10950	430
369	G33	10935	305
370	G35	10920	430
371	G37	10905	305
372	G39	10890	430
373	G41	10875	305
374	G43	10860	430
375	G45	10845	305
376	G47	10830	430
377	G49	10815	305
378	G51	10800	430
379	G53	10785	305
380	G55	10770	430
381	G57	10755	305
382	G59	10740	430
383	G61	10725	305
384	G63	10710	430
385	G65	10695	305
386	G67	10680	430
387	G69	10665	305
388	G71	10650	430
389	G73	10635	305
390	G75	10620	430
391	G77	10605	305
392	G79	10590	430
393	G81	10575	305
394	G83	10560	430
395	G85	10545	305
396	G87	10530	430
397	G89	10515	305
398	G91	10500	430
399	G93	10485	305
400	G95	10470	430

R61529 Pad Coordinate (Unit : μm)

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pad No	pad name	X	Y
401	G97	10455	305
402	G99	10440	430
403	G101	10425	305
404	G103	10410	430
405	G105	10395	305
406	G107	10380	430
407	G109	10365	305
408	G111	10350	430
409	G113	10335	305
410	G115	10320	430
411	G117	10305	305
412	G119	10290	430
413	G121	10275	305
414	G123	10260	430
415	G125	10245	305
416	G127	10230	430
417	G129	10215	305
418	G131	10200	430
419	G133	10185	305
420	G135	10170	430
421	G137	10155	305
422	G139	10140	430
423	G141	10125	305
424	G143	10110	430
425	G145	10095	305
426	G147	10080	430
427	G149	10065	305
428	G151	10050	430
429	G153	10035	305
430	G155	10020	430
431	G157	10005	305
432	G159	9990	430
433	G161	9975	305
434	G163	9960	430
435	G165	9945	305
436	G167	9930	430
437	G169	9915	305
438	G171	9900	430
439	G173	9885	305
440	G175	9870	430
441	G177	9855	305
442	G179	9840	430
443	G181	9825	305
444	G183	9810	430
445	G185	9795	305
446	G187	9780	430
447	G189	9765	305
448	G191	9750	430
449	G193	9735	305
450	G195	9720	430

pad No	pad name	X	Y
451	G197	9705	305
452	G199	9690	430
453	G201	9675	305
454	G203	9660	430
455	G205	9645	305
456	G207	9630	430
457	G209	9615	305
458	G211	9600	430
459	G213	9585	305
460	G215	9570	430
461	G217	9555	305
462	G219	9540	430
463	G221	9525	305
464	G223	9510	430
465	G225	9495	305
466	G227	9480	430
467	G229	9465	305
468	G231	9450	430
469	G233	9435	305
470	G235	9420	430
471	G237	9405	305
472	G239	9390	430
473	G241	9375	305
474	G243	9360	430
475	G245	9345	305
476	G247	9330	430
477	G249	9315	305
478	G251	9300	430
479	G253	9285	305
480	G255	9270	430
481	G257	9255	305
482	G259	9240	430
483	G261	9225	305
484	G263	9210	430
485	G265	9195	305
486	G267	9180	430
487	G269	9165	305
488	G271	9150	430
489	G273	9135	305
490	G275	9120	430
491	G277	9105	305
492	G279	9090	430
493	G281	9075	305
494	G283	9060	430
495	G285	9045	305
496	G287	9030	430
497	G289	9015	305
498	G291	9000	430
499	G293	8985	305
500	G295	8970	430

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pad No	pad name	X	Y
501	G297	8955	305
502	G299	8940	430
503	G301	8925	305
504	G303	8910	430
505	G305	8895	305
506	G307	8880	430
507	G309	8865	305
508	G311	8850	430
509	G313	8835	305
510	G315	8820	430
511	G317	8805	305
512	G319	8790	430
513	G321	8775	305
514	G323	8760	430
515	G325	8745	305
516	G327	8730	430
517	G329	8715	305
518	G331	8700	430
519	G333	8685	305
520	G335	8670	430
521	G337	8655	305
522	G339	8640	430
523	G341	8625	305
524	G343	8610	430
525	G345	8595	305
526	G347	8580	430
527	G349	8565	305
528	G351	8550	430
529	G353	8535	305
530	G355	8520	430
531	G357	8505	305
532	G359	8490	430
533	G361	8475	305
534	G363	8460	430
535	G365	8445	305
536	G367	8430	430
537	G369	8415	305
538	G371	8400	430
539	G373	8385	305
540	G375	8370	430
541	G377	8355	305
542	G379	8340	430
543	G381	8325	305
544	G383	8310	430
545	G385	8295	305
546	G387	8280	430
547	G389	8265	305
548	G391	8250	430
549	G393	8235	305
550	G395	8220	430

pad No	pad name	X	Y
551	G397	8205	305
552	G399	8190	430
553	G401	8175	305
554	G403	8160	430
555	G405	8145	305
556	G407	8130	430
557	G409	8115	305
558	G411	8100	430
559	G413	8085	305
560	G415	8070	430
561	G417	8055	305
562	G419	8040	430
563	G421	8025	305
564	G423	8010	430
565	G425	7995	305
566	G427	7980	430
567	G429	7965	305
568	G431	7950	430
569	G433	7935	305
570	G435	7920	430
571	G437	7905	305
572	G439	7890	430
573	G441	7875	305
574	G443	7860	430
575	G445	7845	305
576	G447	7830	430
577	G449	7815	305
578	G451	7800	430
579	G453	7785	305
580	G455	7770	430
581	G457	7755	305
582	G459	7740	430
583	G461	7725	305
584	G463	7710	430
585	G465	7695	305
586	G467	7680	430
587	G469	7665	305
588	G471	7650	430
589	G473	7635	305
590	G475	7620	430
591	G477	7605	305
592	G479	7590	430
593	TESTO3	7575	305
594	TESTO4	7560	430
595	TESTO5	7395	305
596	TESTO6	7380	430
597	S960	7365	305
598	S959	7350	430
599	S958	7335	305
600	S957	7320	430

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pad No	pad name	X	Y
601	S956	7305	305
602	S955	7290	430
603	S954	7275	305
604	S953	7260	430
605	S952	7245	305
606	S951	7230	430
607	S950	7215	305
608	S949	7200	430
609	S948	7185	305
610	S947	7170	430
611	S946	7155	305
612	S945	7140	430
613	S944	7125	305
614	S943	7110	430
615	S942	7095	305
616	S941	7080	430
617	S940	7065	305
618	S939	7050	430
619	S938	7035	305
620	S937	7020	430
621	S936	7005	305
622	S935	6990	430
623	S934	6975	305
624	S933	6960	430
625	S932	6945	305
626	S931	6930	430
627	S930	6915	305
628	S929	6900	430
629	S928	6885	305
630	S927	6870	430
631	S926	6855	305
632	S925	6840	430
633	S924	6825	305
634	S923	6810	430
635	S922	6795	305
636	S921	6780	430
637	S920	6765	305
638	S919	6750	430
639	S918	6735	305
640	S917	6720	430
641	S916	6705	305
642	S915	6690	430
643	S914	6675	305
644	S913	6660	430
645	S912	6645	305
646	S911	6630	430
647	S910	6615	305
648	S909	6600	430
649	S908	6585	305
650	S907	6570	430

pad No	pad name	X	Y
651	S906	6555	305
652	S905	6540	430
653	S904	6525	305
654	S903	6510	430
655	S902	6495	305
656	S901	6480	430
657	S900	6465	305
658	S899	6450	430
659	S898	6435	305
660	S897	6420	430
661	S896	6405	305
662	S895	6390	430
663	S894	6375	305
664	S893	6360	430
665	S892	6345	305
666	S891	6330	430
667	S890	6315	305
668	S889	6300	430
669	S888	6285	305
670	S887	6270	430
671	S886	6255	305
672	S885	6240	430
673	S884	6225	305
674	S883	6210	430
675	S882	6195	305
676	S881	6180	430
677	S880	6165	305
678	S879	6150	430
679	S878	6135	305
680	S877	6120	430
681	S876	6105	305
682	S875	6090	430
683	S874	6075	305
684	S873	6060	430
685	S872	6045	305
686	S871	6030	430
687	S870	6015	305
688	S869	6000	430
689	S868	5985	305
690	S867	5970	430
691	S866	5955	305
692	S865	5940	430
693	S864	5925	305
694	S863	5910	430
695	S862	5895	305
696	S861	5880	430
697	S860	5865	305
698	S859	5850	430
699	S858	5835	305
700	S857	5820	430

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pad No	pad name	X	Y
701	S856	5805	305
702	S855	5790	430
703	S854	5775	305
704	S853	5760	430
705	S852	5745	305
706	S851	5730	430
707	S850	5715	305
708	S849	5700	430
709	S848	5685	305
710	S847	5670	430
711	S846	5655	305
712	S845	5640	430
713	S844	5625	305
714	S843	5610	430
715	S842	5595	305
716	S841	5580	430
717	S840	5565	305
718	S839	5550	430
719	S838	5535	305
720	S837	5520	430
721	S836	5505	305
722	S835	5490	430
723	S834	5475	305
724	S833	5460	430
725	S832	5445	305
726	S831	5430	430
727	S830	5415	305
728	S829	5400	430
729	S828	5385	305
730	S827	5370	430
731	S826	5355	305
732	S825	5340	430
733	S824	5325	305
734	S823	5310	430
735	S822	5295	305
736	S821	5280	430
737	S820	5265	305
738	S819	5250	430
739	S818	5235	305
740	S817	5220	430
741	S816	5205	305
742	S815	5190	430
743	S814	5175	305
744	S813	5160	430
745	S812	5145	305
746	S811	5130	430
747	S810	5115	305
748	S809	5100	430
749	S808	5085	305
750	S807	5070	430

pad No	pad name	X	Y
751	S806	5055	305
752	S805	5040	430
753	S804	5025	305
754	S803	5010	430
755	S802	4995	305
756	S801	4980	430
757	S800	4965	305
758	S799	4950	430
759	S798	4935	305
760	S797	4920	430
761	S796	4905	305
762	S795	4890	430
763	S794	4875	305
764	S793	4860	430
765	S792	4845	305
766	S791	4830	430
767	S790	4815	305
768	S789	4800	430
769	S788	4785	305
770	S787	4770	430
771	S786	4755	305
772	S785	4740	430
773	S784	4725	305
774	S783	4710	430
775	S782	4695	305
776	S781	4680	430
777	S780	4665	305
778	S779	4650	430
779	S778	4635	305
780	S777	4620	430
781	S776	4605	305
782	S775	4590	430
783	S774	4575	305
784	S773	4560	430
785	S772	4545	305
786	S771	4530	430
787	S770	4515	305
788	S769	4500	430
789	S768	4485	305
790	S767	4470	430
791	S766	4455	305
792	S765	4440	430
793	S764	4425	305
794	S763	4410	430
795	S762	4395	305
796	S761	4380	430
797	S760	4365	305
798	S759	4350	430
799	S758	4335	305
800	S757	4320	430

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pad No	pad name	X	Y
801	S756	4305	305
802	S755	4290	430
803	S754	4275	305
804	S753	4260	430
805	S752	4245	305
806	S751	4230	430
807	S750	4215	305
808	S749	4200	430
809	S748	4185	305
810	S747	4170	430
811	S746	4155	305
812	S745	4140	430
813	S744	4125	305
814	S743	4110	430
815	S742	4095	305
816	S741	4080	430
817	S740	4065	305
818	S739	4050	430
819	S738	4035	305
820	S737	4020	430
821	S736	4005	305
822	S735	3990	430
823	S734	3975	305
824	S733	3960	430
825	S732	3945	305
826	S731	3930	430
827	S730	3915	305
828	S729	3900	430
829	S728	3885	305
830	S727	3870	430
831	S726	3855	305
832	S725	3840	430
833	S724	3825	305
834	S723	3810	430
835	S722	3795	305
836	S721	3780	430
837	S720	3765	305
838	S719	3750	430
839	S718	3735	305
840	S717	3720	430
841	S716	3705	305
842	S715	3690	430
843	S714	3675	305
844	S713	3660	430
845	S712	3645	305
846	S711	3630	430
847	S710	3615	305
848	S709	3600	430
849	S708	3585	305
850	S707	3570	430

pad No	pad name	X	Y
851	S706	3555	305
852	S705	3540	430
853	S704	3525	305
854	S703	3510	430
855	S702	3495	305
856	S701	3480	430
857	S700	3465	305
858	S699	3450	430
859	S698	3435	305
860	S697	3420	430
861	S696	3405	305
862	S695	3390	430
863	S694	3375	305
864	S693	3360	430
865	S692	3345	305
866	S691	3330	430
867	S690	3315	305
868	S689	3300	430
869	S688	3285	305
870	S687	3270	430
871	S686	3255	305
872	S685	3240	430
873	S684	3225	305
874	S683	3210	430
875	S682	3195	305
876	S681	3180	430
877	S680	3165	305
878	S679	3150	430
879	S678	3135	305
880	S677	3120	430
881	S676	3105	305
882	S675	3090	430
883	S674	3075	305
884	S673	3060	430
885	S672	3045	305
886	S671	3030	430
887	S670	3015	305
888	S669	3000	430
889	S668	2985	305
890	S667	2970	430
891	S666	2955	305
892	S665	2940	430
893	S664	2925	305
894	S663	2910	430
895	S662	2895	305
896	S661	2880	430
897	S660	2865	305
898	S659	2850	430
899	S658	2835	305
900	S657	2820	430

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pad No	pad name	X	Y
901	S656	2805	305
902	S655	2790	430
903	S654	2775	305
904	S653	2760	430
905	S652	2745	305
906	S651	2730	430
907	S650	2715	305
908	S649	2700	430
909	S648	2685	305
910	S647	2670	430
911	S646	2655	305
912	S645	2640	430
913	S644	2625	305
914	S643	2610	430
915	S642	2595	305
916	S641	2580	430
917	S640	2565	305
918	S639	2550	430
919	S638	2535	305
920	S637	2520	430
921	S636	2505	305
922	S635	2490	430
923	S634	2475	305
924	S633	2460	430
925	S632	2445	305
926	S631	2430	430
927	S630	2415	305
928	S629	2400	430
929	S628	2385	305
930	S627	2370	430
931	S626	2355	305
932	S625	2340	430
933	S624	2325	305
934	S623	2310	430
935	S622	2295	305
936	S621	2280	430
937	S620	2265	305
938	S619	2250	430
939	S618	2235	305
940	S617	2220	430
941	S616	2205	305
942	S615	2190	430
943	S614	2175	305
944	S613	2160	430
945	S612	2145	305
946	S611	2130	430
947	S610	2115	305
948	S609	2100	430
949	S608	2085	305
950	S607	2070	430

pad No	pad name	X	Y
951	S606	2055	305
952	S605	2040	430
953	S604	2025	305
954	S603	2010	430
955	S602	1995	305
956	S601	1980	430
957	S600	1965	305
958	S599	1950	430
959	S598	1935	305
960	S597	1920	430
961	S596	1905	305
962	S595	1890	430
963	S594	1875	305
964	S593	1860	430
965	S592	1845	305
966	S591	1830	430
967	S590	1815	305
968	S589	1800	430
969	S588	1785	305
970	S587	1770	430
971	S586	1755	305
972	S585	1740	430
973	S584	1725	305
974	S583	1710	430
975	S582	1695	305
976	S581	1680	430
977	S580	1665	305
978	S579	1650	430
979	S578	1635	305
980	S577	1620	430
981	S576	1605	305
982	S575	1590	430
983	S574	1575	305
984	S573	1560	430
985	S572	1545	305
986	S571	1530	430
987	S570	1515	305
988	S569	1500	430
989	S568	1485	305
990	S567	1470	430
991	S566	1455	305
992	S565	1440	430
993	S564	1425	305
994	S563	1410	430
995	S562	1395	305
996	S561	1380	430
997	S560	1365	305
998	S559	1350	430
999	S558	1335	305
1000	S557	1320	430

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pad No	pad name	X	Y
1001	S556	1305	305
1002	S555	1290	430
1003	S554	1275	305
1004	S553	1260	430
1005	S552	1245	305
1006	S551	1230	430
1007	S550	1215	305
1008	S549	1200	430
1009	S548	1185	305
1010	S547	1170	430
1011	S546	1155	305
1012	S545	1140	430
1013	S544	1125	305
1014	S543	1110	430
1015	S542	1095	305
1016	S541	1080	430
1017	S540	1065	305
1018	S539	1050	430
1019	S538	1035	305
1020	S537	1020	430
1021	S536	1005	305
1022	S535	990	430
1023	S534	975	305
1024	S533	960	430
1025	S532	945	305
1026	S531	930	430
1027	S530	915	305
1028	S529	900	430
1029	S528	885	305
1030	S527	870	430
1031	S526	855	305
1032	S525	840	430
1033	S524	825	305
1034	S523	810	430
1035	S522	795	305
1036	S521	780	430
1037	S520	765	305
1038	S519	750	430
1039	S518	735	305
1040	S517	720	430
1041	S516	705	305
1042	S515	690	430
1043	S514	675	305
1044	S513	660	430
1045	S512	645	305
1046	S511	630	430
1047	S510	615	305
1048	S509	600	430
1049	S508	585	305
1050	S507	570	430

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pad No	pad name	X	Y
1051	S506	555	305
1052	S505	540	430
1053	S504	525	305
1054	S503	510	430
1055	S502	495	305
1056	S501	480	430
1057	S500	465	305
1058	S499	450	430
1059	S498	435	305
1060	S497	420	430
1061	S496	405	305
1062	S495	390	430
1063	S494	375	305
1064	S493	360	430
1065	S492	345	305
1066	S491	330	430
1067	S490	315	305
1068	S489	300	430
1069	S488	285	305
1070	S487	270	430
1071	S486	255	305
1072	S485	240	430
1073	S484	225	305
1074	S483	210	430
1075	S482	195	305
1076	S481	180	430
1077	TEST07	165	305
1078	TEST08	150	430
1079	TEST09	-150	430
1080	TEST010	-165	305
1081	S480	-180	430
1082	S479	-195	305
1083	S478	-210	430
1084	S477	-225	305
1085	S476	-240	430
1086	S475	-255	305
1087	S474	-270	430
1088	S473	-285	305
1089	S472	-300	430
1090	S471	-315	305
1091	S470	-330	430
1092	S469	-345	305
1093	S468	-360	430
1094	S467	-375	305
1095	S466	-390	430
1096	S465	-405	305
1097	S464	-420	430
1098	S463	-435	305
1099	S462	-450	430
1100	S461	-465	305

R61529 Pad Coordinate (Unit : μm)

pad No	pad name	X	Y
1101	S460	-480	430
1102	S459	-495	305
1103	S458	-510	430
1104	S457	-525	305
1105	S456	-540	430
1106	S455	-555	305
1107	S454	-570	430
1108	S453	-585	305
1109	S452	-600	430
1110	S451	-615	305
1111	S450	-630	430
1112	S449	-645	305
1113	S448	-660	430
1114	S447	-675	305
1115	S446	-690	430
1116	S445	-705	305
1117	S444	-720	430
1118	S443	-735	305
1119	S442	-750	430
1120	S441	-765	305
1121	S440	-780	430
1122	S439	-795	305
1123	S438	-810	430
1124	S437	-825	305
1125	S436	-840	430
1126	S435	-855	305
1127	S434	-870	430
1128	S433	-885	305
1129	S432	-900	430
1130	S431	-915	305
1131	S430	-930	430
1132	S429	-945	305
1133	S428	-960	430
1134	S427	-975	305
1135	S426	-990	430
1136	S425	-1005	305
1137	S424	-1020	430
1138	S423	-1035	305
1139	S422	-1050	430
1140	S421	-1065	305
1141	S420	-1080	430
1142	S419	-1095	305
1143	S418	-1110	430
1144	S417	-1125	305
1145	S416	-1140	430
1146	S415	-1155	305
1147	S414	-1170	430
1148	S413	-1185	305
1149	S412	-1200	430
1150	S411	-1215	305

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pad No	pad name	X	Y
1151	S410	-1230	430
1152	S409	-1245	305
1153	S408	-1260	430
1154	S407	-1275	305
1155	S406	-1290	430
1156	S405	-1305	305
1157	S404	-1320	430
1158	S403	-1335	305
1159	S402	-1350	430
1160	S401	-1365	305
1161	S400	-1380	430
1162	S399	-1395	305
1163	S398	-1410	430
1164	S397	-1425	305
1165	S396	-1440	430
1166	S395	-1455	305
1167	S394	-1470	430
1168	S393	-1485	305
1169	S392	-1500	430
1170	S391	-1515	305
1171	S390	-1530	430
1172	S389	-1545	305
1173	S388	-1560	430
1174	S387	-1575	305
1175	S386	-1590	430
1176	S385	-1605	305
1177	S384	-1620	430
1178	S383	-1635	305
1179	S382	-1650	430
1180	S381	-1665	305
1181	S380	-1680	430
1182	S379	-1695	305
1183	S378	-1710	430
1184	S377	-1725	305
1185	S376	-1740	430
1186	S375	-1755	305
1187	S374	-1770	430
1188	S373	-1785	305
1189	S372	-1800	430
1190	S371	-1815	305
1191	S370	-1830	430
1192	S369	-1845	305
1193	S368	-1860	430
1194	S367	-1875	305
1195	S366	-1890	430
1196	S365	-1905	305
1197	S364	-1920	430
1198	S363	-1935	305
1199	S362	-1950	430
1200	S361	-1965	305

R61529 Pad Coordinate (Unit : μm)

pad No	pad name	X	Y
1201	S360	-1980	430
1202	S359	-1995	305
1203	S358	-2010	430
1204	S357	-2025	305
1205	S356	-2040	430
1206	S355	-2055	305
1207	S354	-2070	430
1208	S353	-2085	305
1209	S352	-2100	430
1210	S351	-2115	305
1211	S350	-2130	430
1212	S349	-2145	305
1213	S348	-2160	430
1214	S347	-2175	305
1215	S346	-2190	430
1216	S345	-2205	305
1217	S344	-2220	430
1218	S343	-2235	305
1219	S342	-2250	430
1220	S341	-2265	305
1221	S340	-2280	430
1222	S339	-2295	305
1223	S338	-2310	430
1224	S337	-2325	305
1225	S336	-2340	430
1226	S335	-2355	305
1227	S334	-2370	430
1228	S333	-2385	305
1229	S332	-2400	430
1230	S331	-2415	305
1231	S330	-2430	430
1232	S329	-2445	305
1233	S328	-2460	430
1234	S327	-2475	305
1235	S326	-2490	430
1236	S325	-2505	305
1237	S324	-2520	430
1238	S323	-2535	305
1239	S322	-2550	430
1240	S321	-2565	305
1241	S320	-2580	430
1242	S319	-2595	305
1243	S318	-2610	430
1244	S317	-2625	305
1245	S316	-2640	430
1246	S315	-2655	305
1247	S314	-2670	430
1248	S313	-2685	305
1249	S312	-2700	430
1250	S311	-2715	305

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pad No	pad name	X	Y
1251	S310	-2730	430
1252	S309	-2745	305
1253	S308	-2760	430
1254	S307	-2775	305
1255	S306	-2790	430
1256	S305	-2805	305
1257	S304	-2820	430
1258	S303	-2835	305
1259	S302	-2850	430
1260	S301	-2865	305
1261	S300	-2880	430
1262	S299	-2895	305
1263	S298	-2910	430
1264	S297	-2925	305
1265	S296	-2940	430
1266	S295	-2955	305
1267	S294	-2970	430
1268	S293	-2985	305
1269	S292	-3000	430
1270	S291	-3015	305
1271	S290	-3030	430
1272	S289	-3045	305
1273	S288	-3060	430
1274	S287	-3075	305
1275	S286	-3090	430
1276	S285	-3105	305
1277	S284	-3120	430
1278	S283	-3135	305
1279	S282	-3150	430
1280	S281	-3165	305
1281	S280	-3180	430
1282	S279	-3195	305
1283	S278	-3210	430
1284	S277	-3225	305
1285	S276	-3240	430
1286	S275	-3255	305
1287	S274	-3270	430
1288	S273	-3285	305
1289	S272	-3300	430
1290	S271	-3315	305
1291	S270	-3330	430
1292	S269	-3345	305
1293	S268	-3360	430
1294	S267	-3375	305
1295	S266	-3390	430
1296	S265	-3405	305
1297	S264	-3420	430
1298	S263	-3435	305
1299	S262	-3450	430
1300	S261	-3465	305

R61529 Pad Coordinate (Unit : μm)

pad No	pad name	X	Y
1301	S260	-3480	430
1302	S259	-3495	305
1303	S258	-3510	430
1304	S257	-3525	305
1305	S256	-3540	430
1306	S255	-3555	305
1307	S254	-3570	430
1308	S253	-3585	305
1309	S252	-3600	430
1310	S251	-3615	305
1311	S250	-3630	430
1312	S249	-3645	305
1313	S248	-3660	430
1314	S247	-3675	305
1315	S246	-3690	430
1316	S245	-3705	305
1317	S244	-3720	430
1318	S243	-3735	305
1319	S242	-3750	430
1320	S241	-3765	305
1321	S240	-3780	430
1322	S239	-3795	305
1323	S238	-3810	430
1324	S237	-3825	305
1325	S236	-3840	430
1326	S235	-3855	305
1327	S234	-3870	430
1328	S233	-3885	305
1329	S232	-3900	430
1330	S231	-3915	305
1331	S230	-3930	430
1332	S229	-3945	305
1333	S228	-3960	430
1334	S227	-3975	305
1335	S226	-3990	430
1336	S225	-4005	305
1337	S224	-4020	430
1338	S223	-4035	305
1339	S222	-4050	430
1340	S221	-4065	305
1341	S220	-4080	430
1342	S219	-4095	305
1343	S218	-4110	430
1344	S217	-4125	305
1345	S216	-4140	430
1346	S215	-4155	305
1347	S214	-4170	430
1348	S213	-4185	305
1349	S212	-4200	430
1350	S211	-4215	305

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pad No	pad name	X	Y
1351	S210	-4230	430
1352	S209	-4245	305
1353	S208	-4260	430
1354	S207	-4275	305
1355	S206	-4290	430
1356	S205	-4305	305
1357	S204	-4320	430
1358	S203	-4335	305
1359	S202	-4350	430
1360	S201	-4365	305
1361	S200	-4380	430
1362	S199	-4395	305
1363	S198	-4410	430
1364	S197	-4425	305
1365	S196	-4440	430
1366	S195	-4455	305
1367	S194	-4470	430
1368	S193	-4485	305
1369	S192	-4500	430
1370	S191	-4515	305
1371	S190	-4530	430
1372	S189	-4545	305
1373	S188	-4560	430
1374	S187	-4575	305
1375	S186	-4590	430
1376	S185	-4605	305
1377	S184	-4620	430
1378	S183	-4635	305
1379	S182	-4650	430
1380	S181	-4665	305
1381	S180	-4680	430
1382	S179	-4695	305
1383	S178	-4710	430
1384	S177	-4725	305
1385	S176	-4740	430
1386	S175	-4755	305
1387	S174	-4770	430
1388	S173	-4785	305
1389	S172	-4800	430
1390	S171	-4815	305
1391	S170	-4830	430
1392	S169	-4845	305
1393	S168	-4860	430
1394	S167	-4875	305
1395	S166	-4890	430
1396	S165	-4905	305
1397	S164	-4920	430
1398	S163	-4935	305
1399	S162	-4950	430
1400	S161	-4965	305

R61529 Pad Coordinate (Unit : μm)

pad No	pad name	X	Y
1401	S160	-4980	430
1402	S159	-4995	305
1403	S158	-5010	430
1404	S157	-5025	305
1405	S156	-5040	430
1406	S155	-5055	305
1407	S154	-5070	430
1408	S153	-5085	305
1409	S152	-5100	430
1410	S151	-5115	305
1411	S150	-5130	430
1412	S149	-5145	305
1413	S148	-5160	430
1414	S147	-5175	305
1415	S146	-5190	430
1416	S145	-5205	305
1417	S144	-5220	430
1418	S143	-5235	305
1419	S142	-5250	430
1420	S141	-5265	305
1421	S140	-5280	430
1422	S139	-5295	305
1423	S138	-5310	430
1424	S137	-5325	305
1425	S136	-5340	430
1426	S135	-5355	305
1427	S134	-5370	430
1428	S133	-5385	305
1429	S132	-5400	430
1430	S131	-5415	305
1431	S130	-5430	430
1432	S129	-5445	305
1433	S128	-5460	430
1434	S127	-5475	305
1435	S126	-5490	430
1436	S125	-5505	305
1437	S124	-5520	430
1438	S123	-5535	305
1439	S122	-5550	430
1440	S121	-5565	305
1441	S120	-5580	430
1442	S119	-5595	305
1443	S118	-5610	430
1444	S117	-5625	305
1445	S116	-5640	430
1446	S115	-5655	305
1447	S114	-5670	430
1448	S113	-5685	305
1449	S112	-5700	430
1450	S111	-5715	305

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pad No	pad name	X	Y
1451	S110	-5730	430
1452	S109	-5745	305
1453	S108	-5760	430
1454	S107	-5775	305
1455	S106	-5790	430
1456	S105	-5805	305
1457	S104	-5820	430
1458	S103	-5835	305
1459	S102	-5850	430
1460	S101	-5865	305
1461	S100	-5880	430
1462	S99	-5895	305
1463	S98	-5910	430
1464	S97	-5925	305
1465	S96	-5940	430
1466	S95	-5955	305
1467	S94	-5970	430
1468	S93	-5985	305
1469	S92	-6000	430
1470	S91	-6015	305
1471	S90	-6030	430
1472	S89	-6045	305
1473	S88	-6060	430
1474	S87	-6075	305
1475	S86	-6090	430
1476	S85	-6105	305
1477	S84	-6120	430
1478	S83	-6135	305
1479	S82	-6150	430
1480	S81	-6165	305
1481	S80	-6180	430
1482	S79	-6195	305
1483	S78	-6210	430
1484	S77	-6225	305
1485	S76	-6240	430
1486	S75	-6255	305
1487	S74	-6270	430
1488	S73	-6285	305
1489	S72	-6300	430
1490	S71	-6315	305
1491	S70	-6330	430
1492	S69	-6345	305
1493	S68	-6360	430
1494	S67	-6375	305
1495	S66	-6390	430
1496	S65	-6405	305
1497	S64	-6420	430
1498	S63	-6435	305
1499	S62	-6450	430
1500	S61	-6465	305

R61529 Pad Coordinate (Unit : μm)

pad No	pad name	X	Y
1501	S60	-6480	430
1502	S59	-6495	305
1503	S58	-6510	430
1504	S57	-6525	305
1505	S56	-6540	430
1506	S55	-6555	305
1507	S54	-6570	430
1508	S53	-6585	305
1509	S52	-6600	430
1510	S51	-6615	305
1511	S50	-6630	430
1512	S49	-6645	305
1513	S48	-6660	430
1514	S47	-6675	305
1515	S46	-6690	430
1516	S45	-6705	305
1517	S44	-6720	430
1518	S43	-6735	305
1519	S42	-6750	430
1520	S41	-6765	305
1521	S40	-6780	430
1522	S39	-6795	305
1523	S38	-6810	430
1524	S37	-6825	305
1525	S36	-6840	430
1526	S35	-6855	305
1527	S34	-6870	430
1528	S33	-6885	305
1529	S32	-6900	430
1530	S31	-6915	305
1531	S30	-6930	430
1532	S29	-6945	305
1533	S28	-6960	430
1534	S27	-6975	305
1535	S26	-6990	430
1536	S25	-7005	305
1537	S24	-7020	430
1538	S23	-7035	305
1539	S22	-7050	430
1540	S21	-7065	305
1541	S20	-7080	430
1542	S19	-7095	305
1543	S18	-7110	430
1544	S17	-7125	305
1545	S16	-7140	430
1546	S15	-7155	305
1547	S14	-7170	430
1548	S13	-7185	305
1549	S12	-7200	430
1550	S11	-7215	305

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pad No	pad name	X	Y
1551	S10	-7230	430
1552	S9	-7245	305
1553	S8	-7260	430
1554	S7	-7275	305
1555	S6	-7290	430
1556	S5	-7305	305
1557	S4	-7320	430
1558	S3	-7335	305
1559	S2	-7350	430
1560	S1	-7365	305
1561	TESTO11	-7380	430
1562	TESTO12	-7395	305
1563	TESTO13	-7560	430
1564	TESTO14	-7575	305
1565	G480	-7590	430
1566	G478	-7605	305
1567	G476	-7620	430
1568	G474	-7635	305
1569	G472	-7650	430
1570	G470	-7665	305
1571	G468	-7680	430
1572	G466	-7695	305
1573	G464	-7710	430
1574	G462	-7725	305
1575	G460	-7740	430
1576	G458	-7755	305
1577	G456	-7770	430
1578	G454	-7785	305
1579	G452	-7800	430
1580	G450	-7815	305
1581	G448	-7830	430
1582	G446	-7845	305
1583	G444	-7860	430
1584	G442	-7875	305
1585	G440	-7890	430
1586	G438	-7905	305
1587	G436	-7920	430
1588	G434	-7935	305
1589	G432	-7950	430
1590	G430	-7965	305
1591	G428	-7980	430
1592	G426	-7995	305
1593	G424	-8010	430
1594	G422	-8025	305
1595	G420	-8040	430
1596	G418	-8055	305
1597	G416	-8070	430
1598	G414	-8085	305
1599	G412	-8100	430
1600	G410	-8115	305

R61529 Pad Coordinate (Unit : μm)

pad No	pad name	X	Y
1601	G408	-8130	430
1602	G406	-8145	305
1603	G404	-8160	430
1604	G402	-8175	305
1605	G400	-8190	430
1606	G398	-8205	305
1607	G396	-8220	430
1608	G394	-8235	305
1609	G392	-8250	430
1610	G390	-8265	305
1611	G388	-8280	430
1612	G386	-8295	305
1613	G384	-8310	430
1614	G382	-8325	305
1615	G380	-8340	430
1616	G378	-8355	305
1617	G376	-8370	430
1618	G374	-8385	305
1619	G372	-8400	430
1620	G370	-8415	305
1621	G368	-8430	430
1622	G366	-8445	305
1623	G364	-8460	430
1624	G362	-8475	305
1625	G360	-8490	430
1626	G358	-8505	305
1627	G356	-8520	430
1628	G354	-8535	305
1629	G352	-8550	430
1630	G350	-8565	305
1631	G348	-8580	430
1632	G346	-8595	305
1633	G344	-8610	430
1634	G342	-8625	305
1635	G340	-8640	430
1636	G338	-8655	305
1637	G336	-8670	430
1638	G334	-8685	305
1639	G332	-8700	430
1640	G330	-8715	305
1641	G328	-8730	430
1642	G326	-8745	305
1643	G324	-8760	430
1644	G322	-8775	305
1645	G320	-8790	430
1646	G318	-8805	305
1647	G316	-8820	430
1648	G314	-8835	305
1649	G312	-8850	430
1650	G310	-8865	305

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pad No	pad name	X	Y
1651	G308	-8880	430
1652	G306	-8895	305
1653	G304	-8910	430
1654	G302	-8925	305
1655	G300	-8940	430
1656	G298	-8955	305
1657	G296	-8970	430
1658	G294	-8985	305
1659	G292	-9000	430
1660	G290	-9015	305
1661	G288	-9030	430
1662	G286	-9045	305
1663	G284	-9060	430
1664	G282	-9075	305
1665	G280	-9090	430
1666	G278	-9105	305
1667	G276	-9120	430
1668	G274	-9135	305
1669	G272	-9150	430
1670	G270	-9165	305
1671	G268	-9180	430
1672	G266	-9195	305
1673	G264	-9210	430
1674	G262	-9225	305
1675	G260	-9240	430
1676	G258	-9255	305
1677	G256	-9270	430
1678	G254	-9285	305
1679	G252	-9300	430
1680	G250	-9315	305
1681	G248	-9330	430
1682	G246	-9345	305
1683	G244	-9360	430
1684	G242	-9375	305
1685	G240	-9390	430
1686	G238	-9405	305
1687	G236	-9420	430
1688	G234	-9435	305
1689	G232	-9450	430
1690	G230	-9465	305
1691	G228	-9480	430
1692	G226	-9495	305
1693	G224	-9510	430
1694	G222	-9525	305
1695	G220	-9540	430
1696	G218	-9555	305
1697	G216	-9570	430
1698	G214	-9585	305
1699	G212	-9600	430
1700	G210	-9615	305

R61529 Pad Coordinate (Unit : μm)

pad No	pad name	X	Y
1701	G208	-9630	430
1702	G206	-9645	305
1703	G204	-9660	430
1704	G202	-9675	305
1705	G200	-9690	430
1706	G198	-9705	305
1707	G196	-9720	430
1708	G194	-9735	305
1709	G192	-9750	430
1710	G190	-9765	305
1711	G188	-9780	430
1712	G186	-9795	305
1713	G184	-9810	430
1714	G182	-9825	305
1715	G180	-9840	430
1716	G178	-9855	305
1717	G176	-9870	430
1718	G174	-9885	305
1719	G172	-9900	430
1720	G170	-9915	305
1721	G168	-9930	430
1722	G166	-9945	305
1723	G164	-9960	430
1724	G162	-9975	305
1725	G160	-9990	430
1726	G158	-10005	305
1727	G156	-10020	430
1728	G154	-10035	305
1729	G152	-10050	430
1730	G150	-10065	305
1731	G148	-10080	430
1732	G146	-10095	305
1733	G144	-10110	430
1734	G142	-10125	305
1735	G140	-10140	430
1736	G138	-10155	305
1737	G136	-10170	430
1738	G134	-10185	305
1739	G132	-10200	430
1740	G130	-10215	305
1741	G128	-10230	430
1742	G126	-10245	305
1743	G124	-10260	430
1744	G122	-10275	305
1745	G120	-10290	430
1746	G118	-10305	305
1747	G116	-10320	430
1748	G114	-10335	305
1749	G112	-10350	430
1750	G110	-10365	305

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pad No	pad name	X	Y
1751	G108	-10380	430
1752	G106	-10395	305
1753	G104	-10410	430
1754	G102	-10425	305
1755	G100	-10440	430
1756	G98	-10455	305
1757	G96	-10470	430
1758	G94	-10485	305
1759	G92	-10500	430
1760	G90	-10515	305
1761	G88	-10530	430
1762	G86	-10545	305
1763	G84	-10560	430
1764	G82	-10575	305
1765	G80	-10590	430
1766	G78	-10605	305
1767	G76	-10620	430
1768	G74	-10635	305
1769	G72	-10650	430
1770	G70	-10665	305
1771	G68	-10680	430
1772	G66	-10695	305
1773	G64	-10710	430
1774	G62	-10725	305
1775	G60	-10740	430
1776	G58	-10755	305
1777	G56	-10770	430
1778	G54	-10785	305
1779	G52	-10800	430
1780	G50	-10815	305
1781	G48	-10830	430
1782	G46	-10845	305
1783	G44	-10860	430
1784	G42	-10875	305
1785	G40	-10890	430
1786	G38	-10905	305
1787	G36	-10920	430
1788	G34	-10935	305
1789	G32	-10950	430
1790	G30	-10965	305
1791	G28	-10980	430
1792	G26	-10995	305
1793	G24	-11010	430
1794	G22	-11025	305
1795	G20	-11040	430
1796	G18	-11055	305
1797	G16	-11070	430
1798	G14	-11085	305
1799	G12	-11100	430
1800	G10	-11115	305

R61529 Pad Coordinate (Unit : μm)

pad No	pad name	X	Y
1801	G8	-11130	430
1802	G6	-11145	305
1803	G4	-11160	430
1804	G2	-11175	305
1805	TESTO15	-11190	430
1806	TESTO16	-11205	305
1807	AGNDDUM39	-11220	430
1808	AGNDDUM40	-11250	430
1809	AGNDDUM41	-11280	430
1810	AGNDDUM42	-11310	430
1811	AGNDDUM43	-11340	430
1812	AGNDDUM44	-11370	430
1813	AGNDDUM45	-11400	430
1814	AGNDDUM46	-11430	430
1815	AGNDDUM47	-11460	430
1816	AGNDDUM48	-11490	430
1817	AGNDDUM49	-11520	430
1818	AGNDDUM50	-11550	430
1819	AGNDDUM51	-11580	430
1820	AGNDDUM52	-11610	430
1821	AGNDDUM53	-11640	430
1822	AGNDDUM54	-11670	430
1823	AGNDDUM55	-11700	430
1824	AGNDDUM56	-11730	430

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Alignment mark	X	Y
1-a	-11891.0	421.0
1-b	11891.0	421.0

BUMP Arrangement

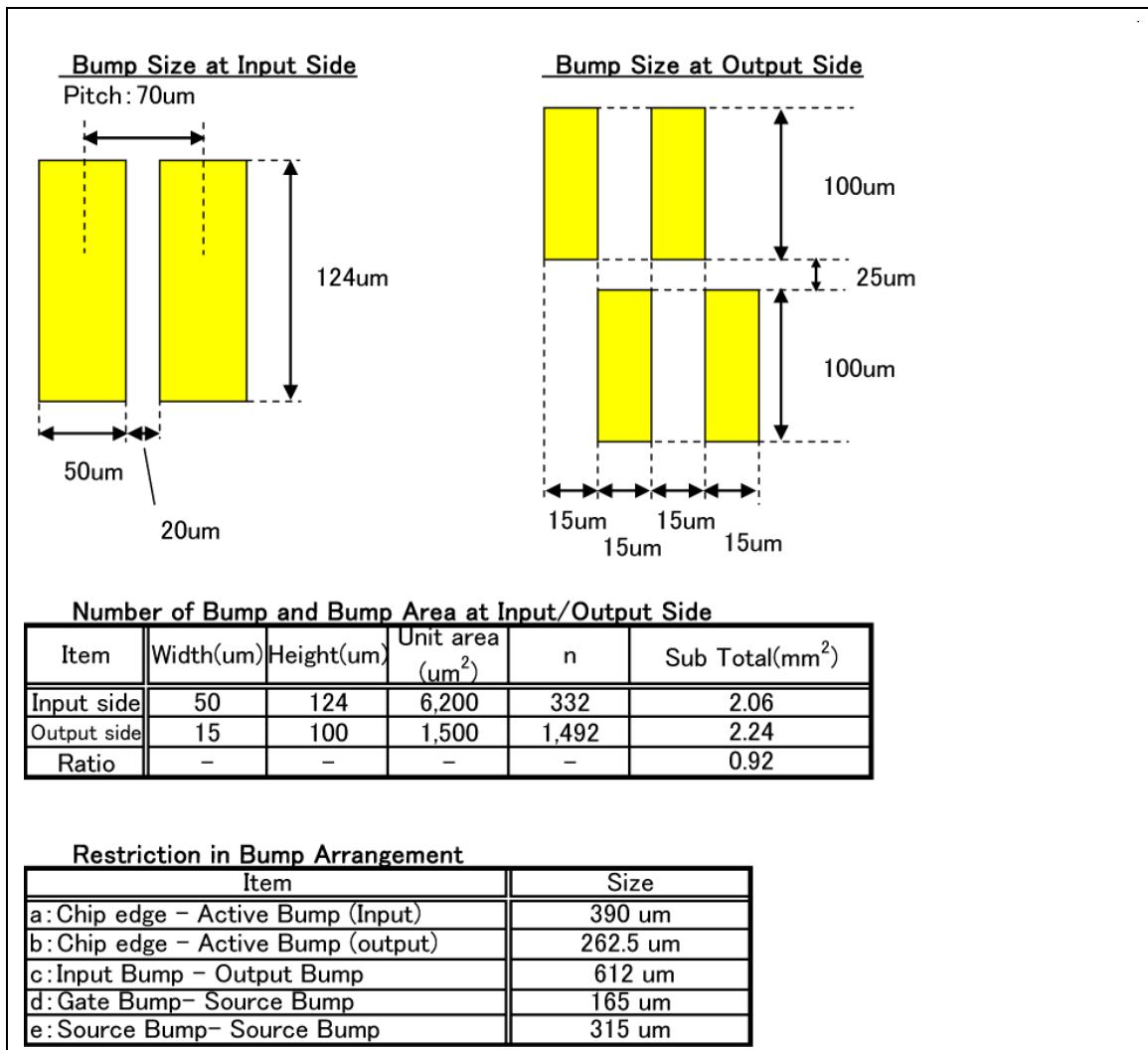


Figure 2

Alignment Mark

- Chip size: 24.00×1.06 mm
- Chip thickness: 230 μm
- Pad coordinates: Pad center
- Coordinate origin: Chip center
- Au bump pitch: Refer to "Pad Coordinate."
- Au bump height: 12 μm
- Alignment mark size

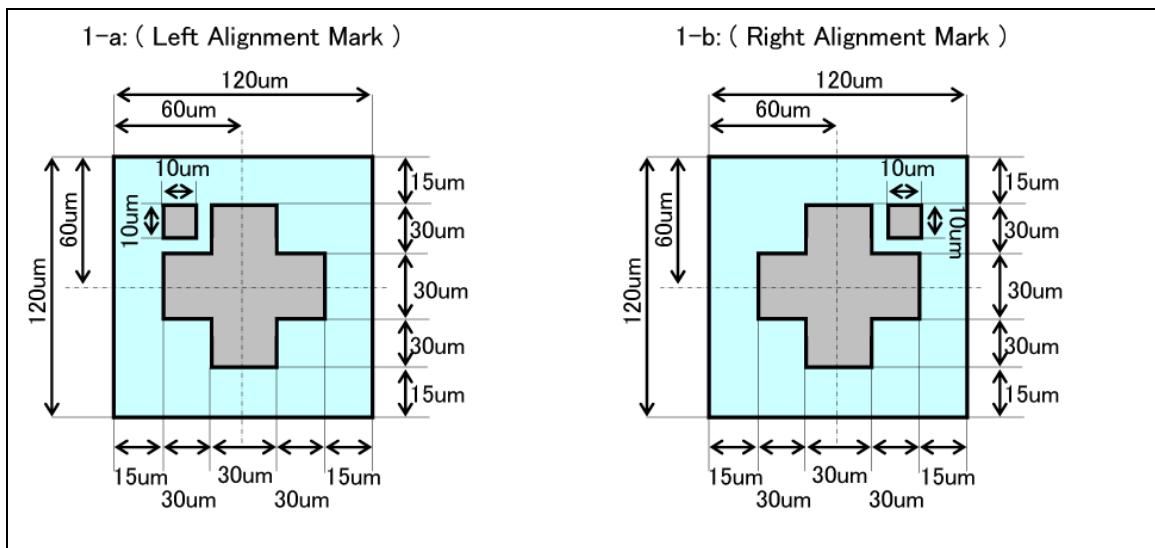
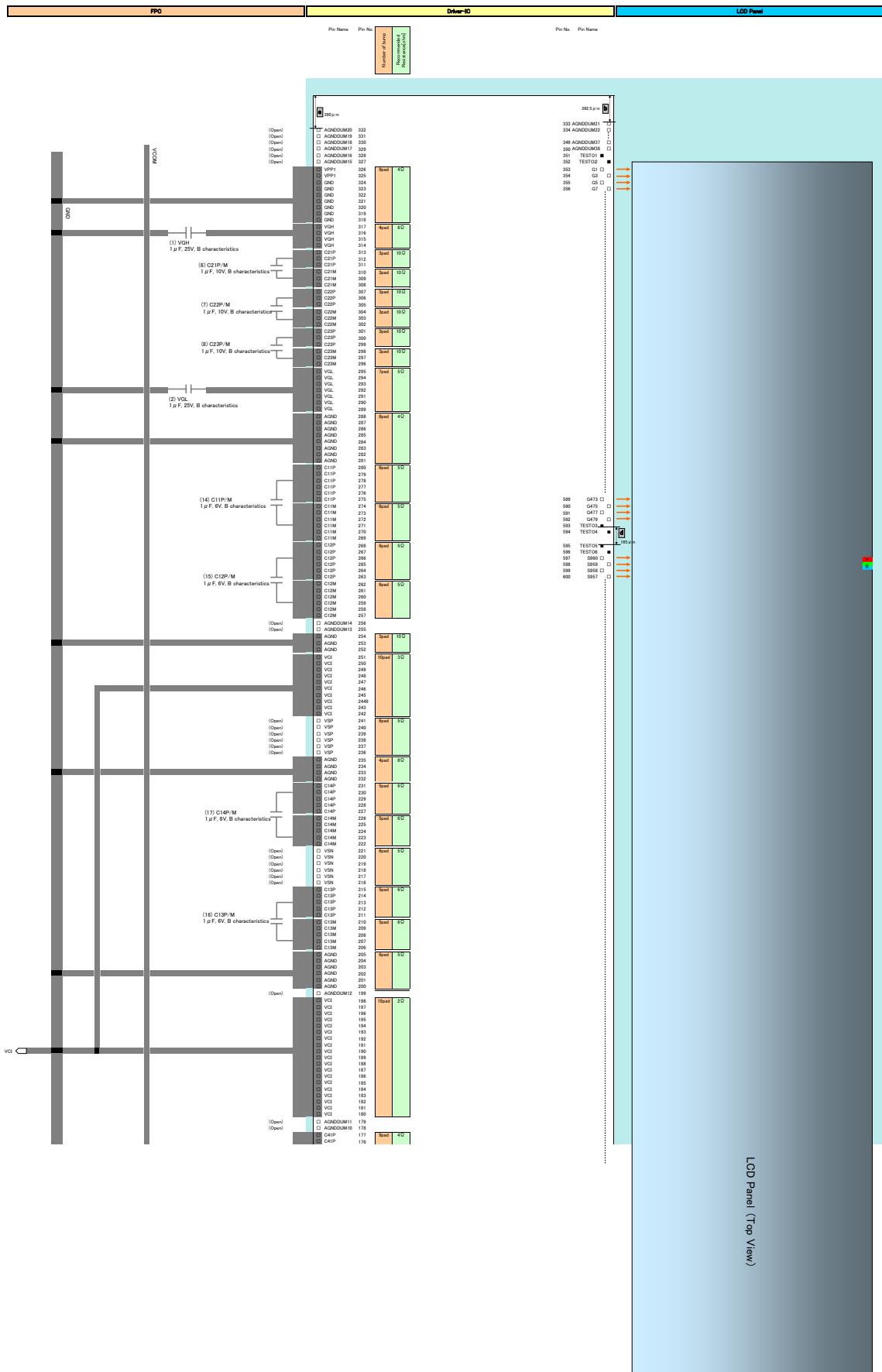
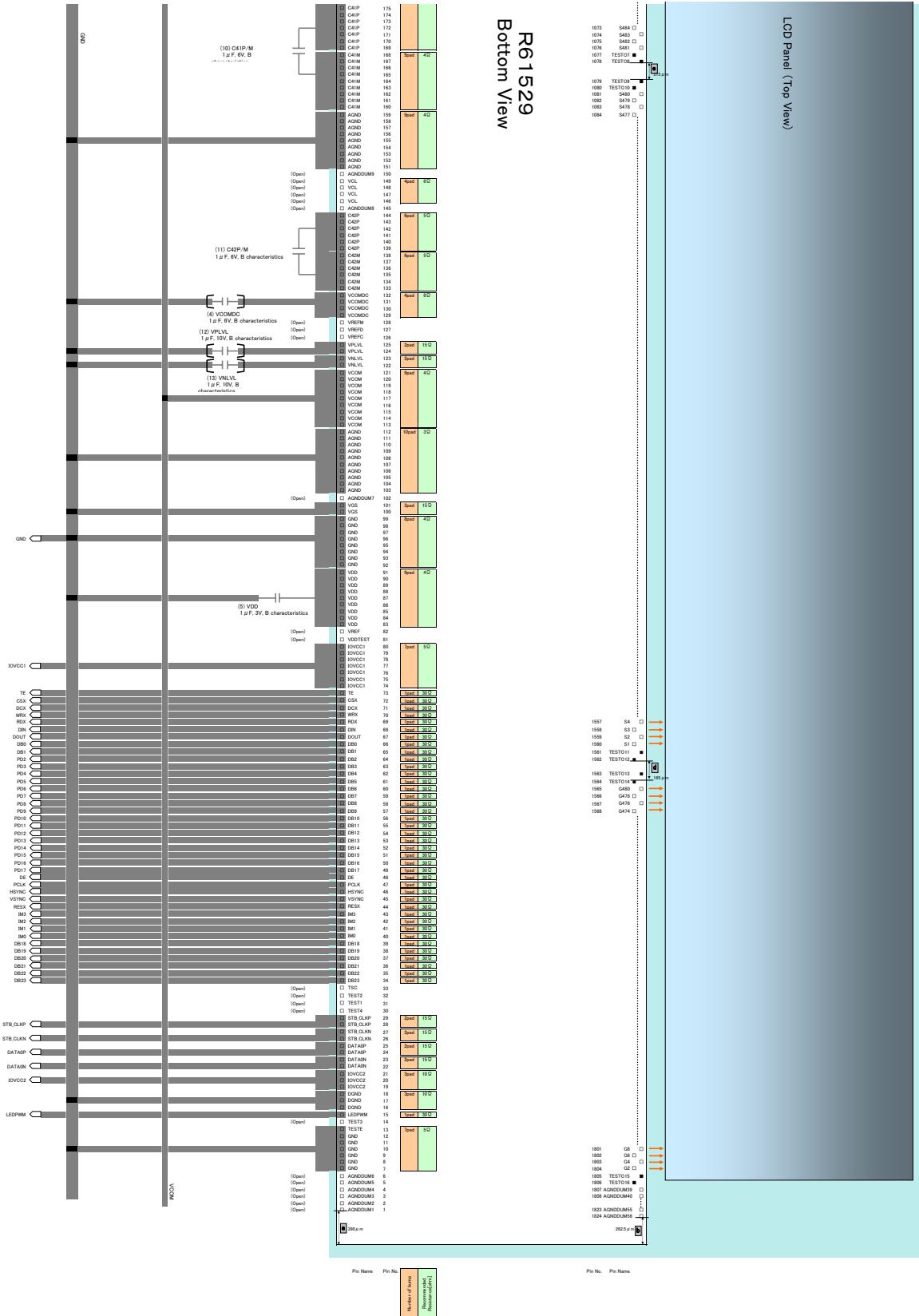


Figure 3

Recommended Resistance/Recommended Connection

2010/7/9 The same contents as Recommended Resistance/Recommended Connection (Rev.0.4 2010.04.22 (Updated)) drawn for a bottom view (glass: top view). The number of pads added.





System Interface Configuration (MIPI DBI Type B)

Outline

The R61529 adopts 24-/18-/16-/8-bit bus display command interface to interface to high-performance host processor. The R61529 starts internal processing after storing control information of externally sent 24-/18-/16-/8-bit data in the command register (CDR) and the parameter register (PR). Since the internal operation of the R61529 is determined by signals sent from the host processor, command/parameter signal, read/write status signal (RDX/WRX), and internal 24-bit data bus signals (DB[23:0]) are called command.

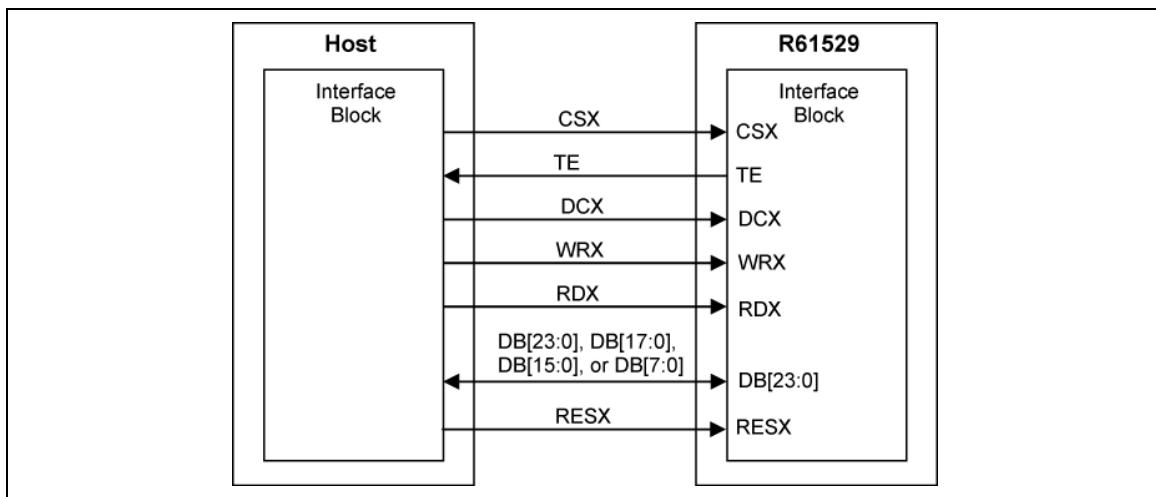
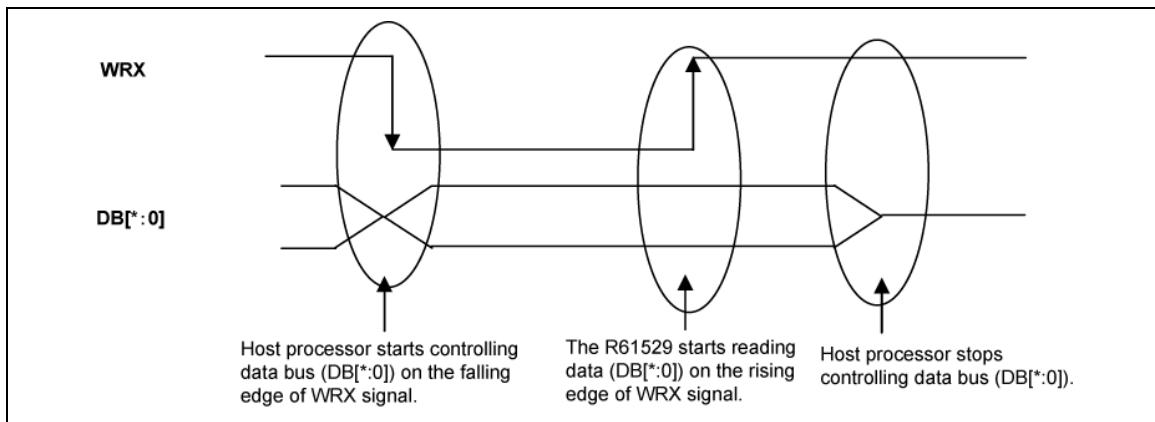


Figure 4 Example of DBI Type B

Write Cycle Sequence

In write cycle, data and/or command are written to the R61529 via the interface between the R61529 and the host processor. Each step of write cycle sequence (WRX high, WRX low, WRX high) comprises three control signals (DCX, RDX, WRX) and 24(DB[23:0])-bit data. The DCX bit indicates signal that is used to select command or data sent on the data bus.

When DCX = 0, data on DB[7:0] is command. When DCX="1", data on DB[15:0] is command parameter and data on DB[23:0] is image data. Setting RDX and WRX to "Low" simultaneously is prohibited. See the figure below for the write cycle sequences.



Note: WRX is not a synchronous signal (can be halted).

Figure 5 Write Cycle Sequence

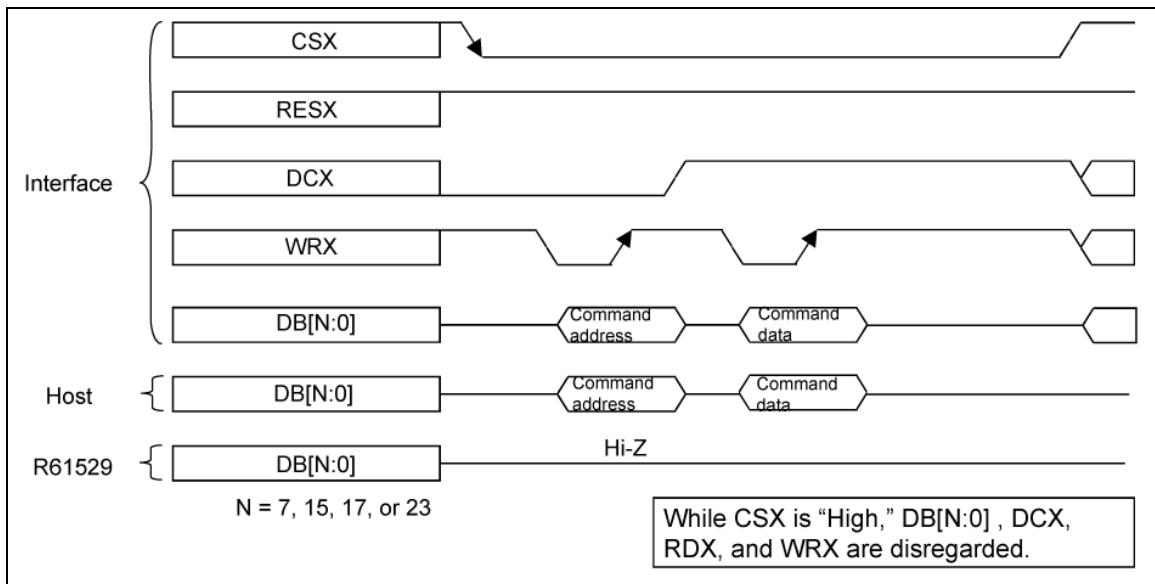
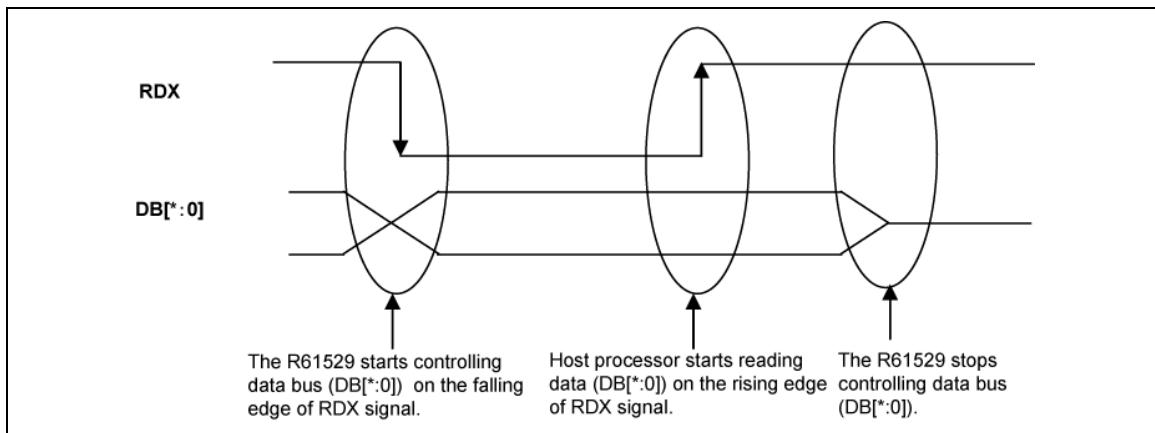


Figure 6 Write Cycle Sequence

Read Cycle Sequence

In read cycle, data and/or commands are read from the R61529 via the interface between the R61529 and the host processor. The data (DB[23:0], DB[17:0], DB[15:0], or DB[7:0]) are transmitted from the R61529 to the host processor on the falling edge of RDX. The host processor reads the data on the rising edge of RDX. Setting RDX and WRX to Low simultaneously is prohibited. See below for the write cycle sequence.



Note: RDX is not a synchronous signal (can be halted).

Figure 7 Read Cycle Sequence

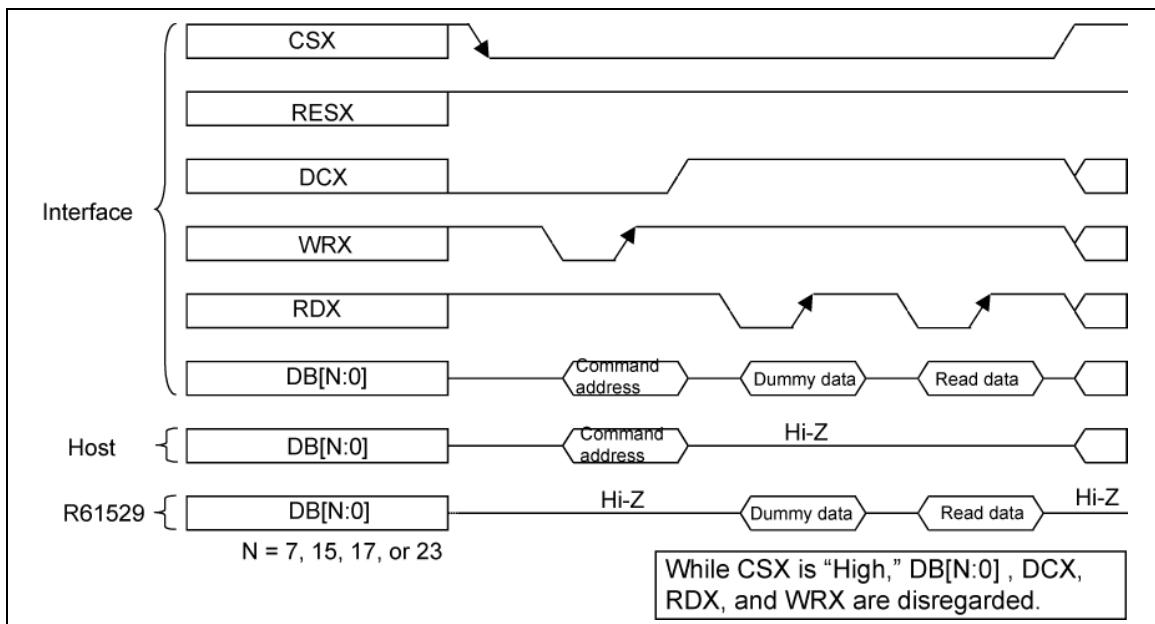


Figure 8 Read Cycle Sequence

Data Transfer Break

As shown in the figure below, in the transmission of parameter for command from the host processor to the R61529, the command parameters sent to the R61529 before the break occurs are stored in the register of the R61529 when the following two conditions are met. One is that a break occurs before the last parameter of the command is sent to the R61529. The other is that the host processor transmits the parameter(s) of a new command, not the parameters of the interrupted command, when the break occurs. However, those parameters sent after the break is disregarded, and the data in the register is not overwritten.

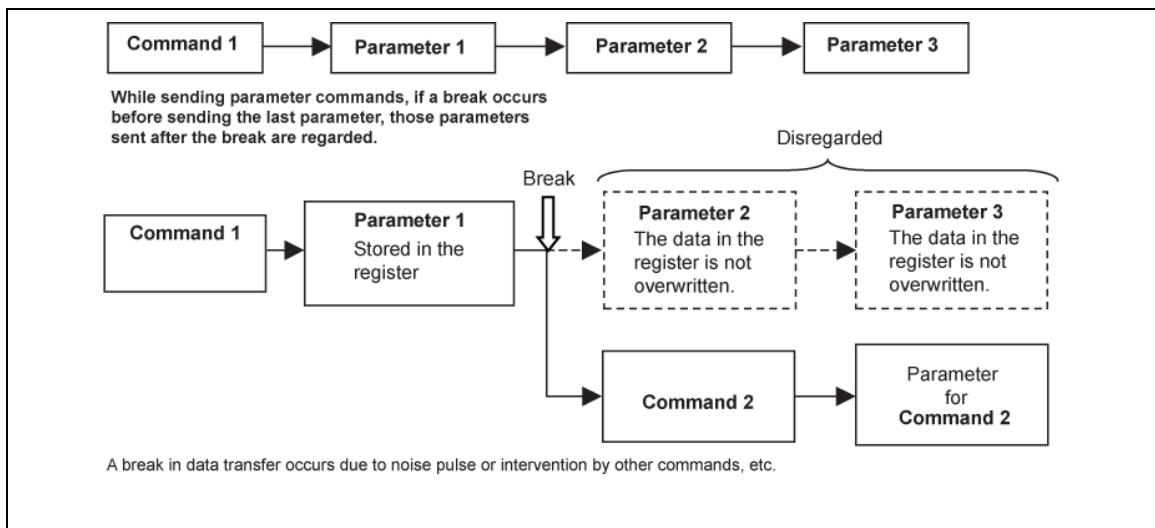
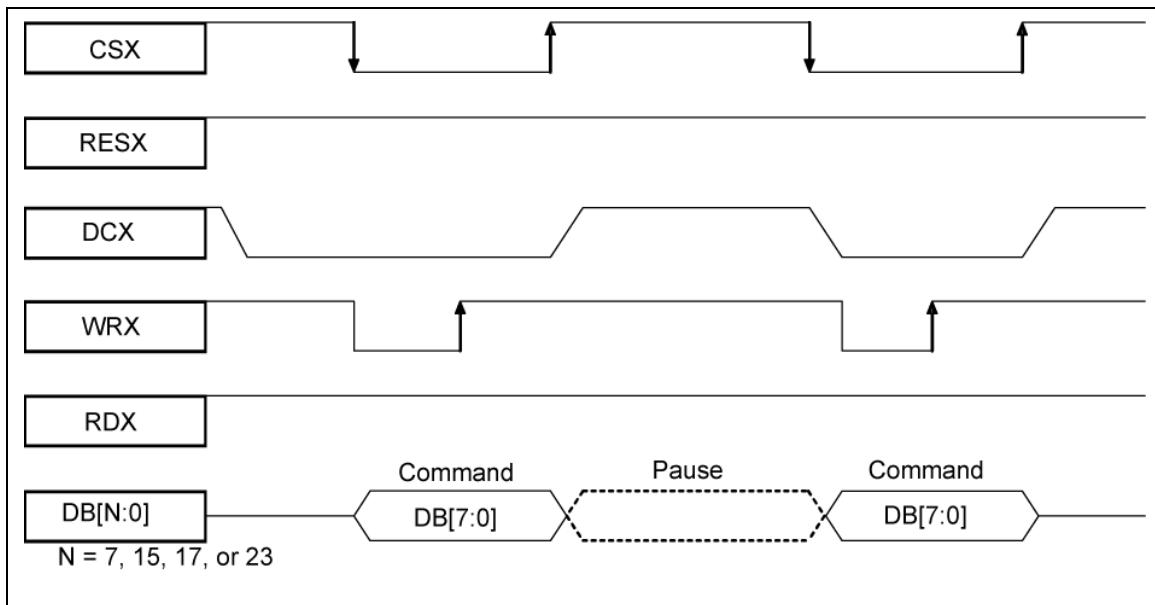
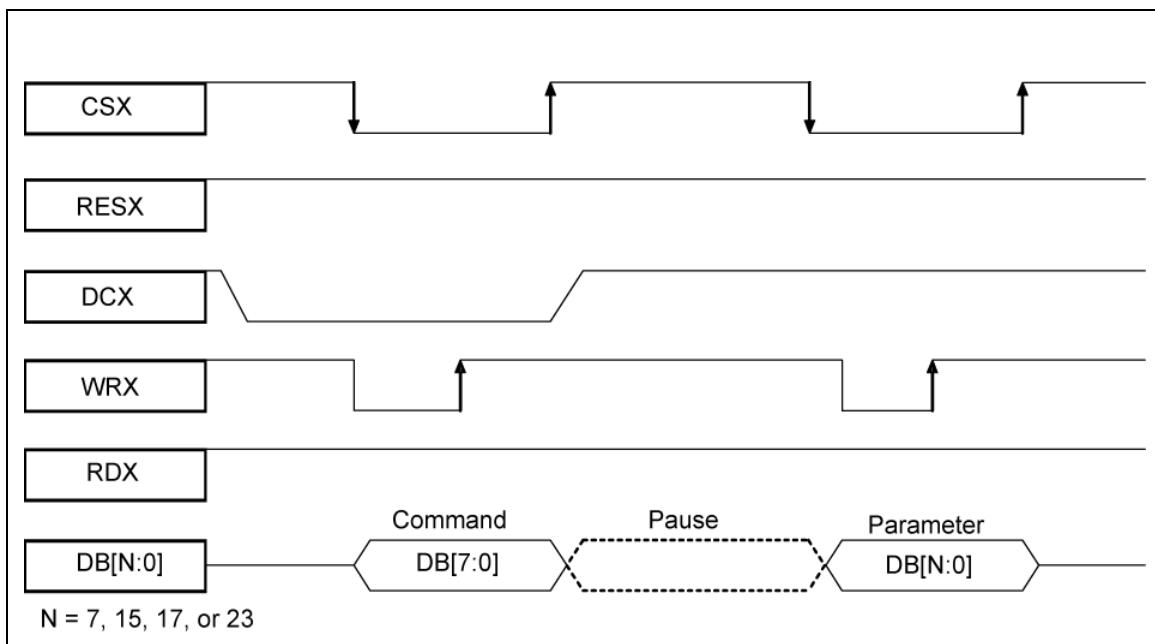
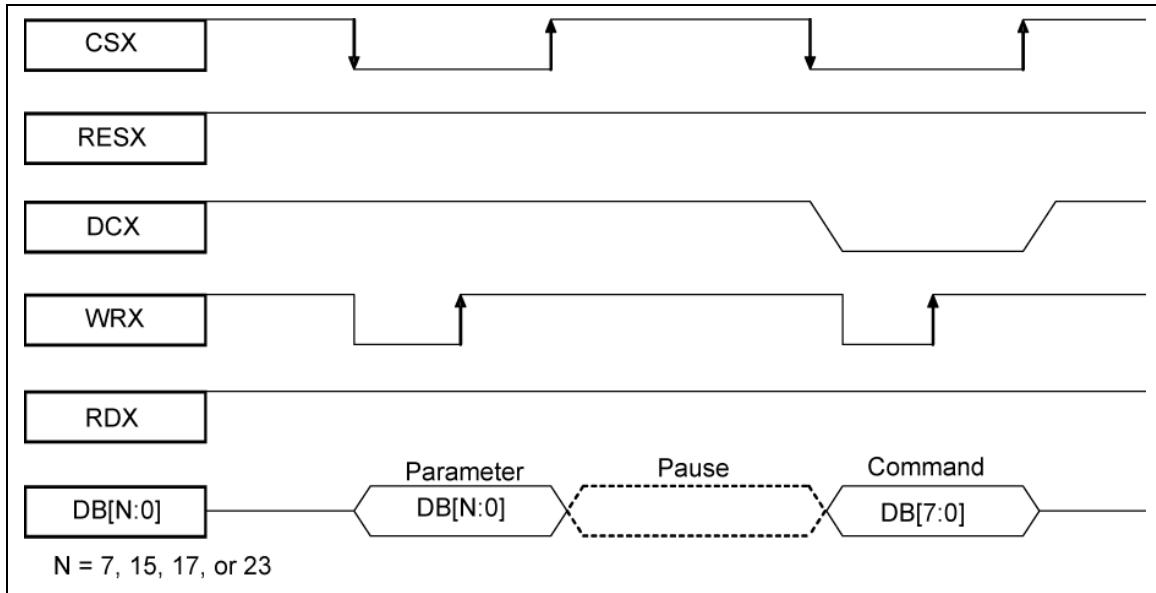
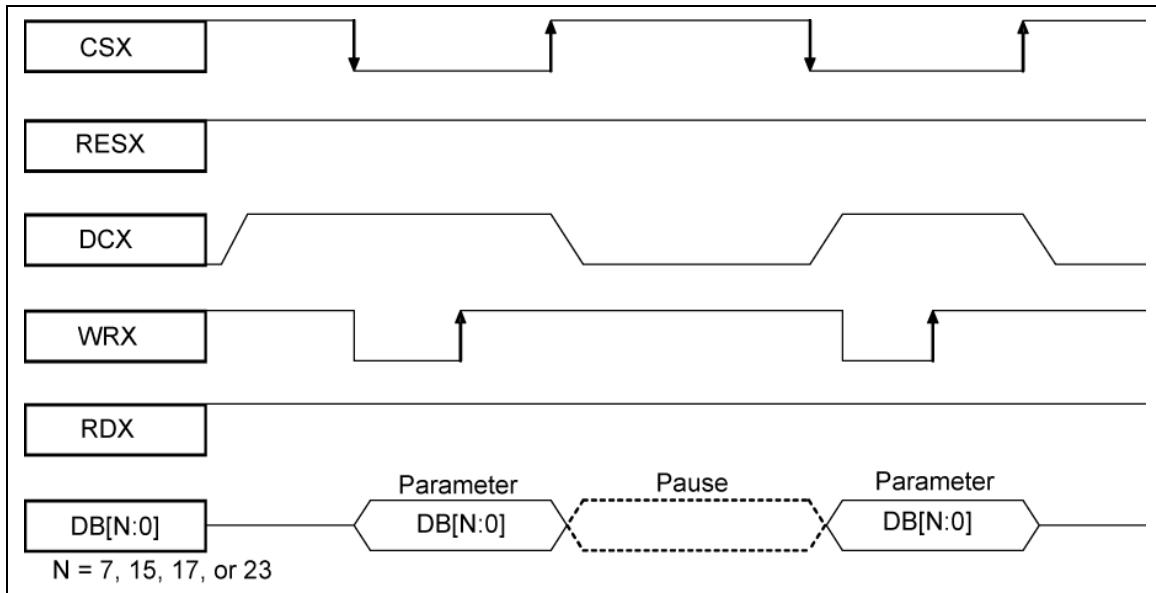


Figure 9

Data Transfer Pause (Command/Pause/Command)**Figure 10****Data Transfer Pause (Command/Pause/Parameter)****Figure 11**

Data Transfer Pause (Parameter/Pause/Command)**Figure 12****Data Transfer Pause (Parameter/Pause/Parameter)****Figure 13**

Data Transfer Mode

Two methods are available for writing data to the frame memory in the R61529.

Write Method 1 (Default)

One frame of image data is written to the frame memory. The amount of the transmitted data is over 1 frame, the data are disregarded. The write operation of the data to the frame memory is terminated when a command intervenes in the middle of the course. The R61529 writes the image data to the next frame when write_memory_start command (2Ch) is written. Set WEMODE =0 (Frame Memory Access and Interface Setting (B3h)).

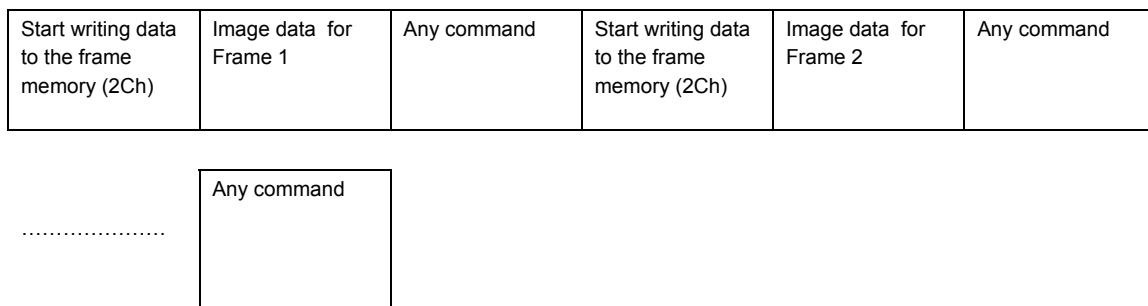


Figure 14

Write Method 2

The image data are written consecutively to the frame memory. The frame memory pointer is reset to the start point when the frame memory becomes full and the driver starts writing the image data of the next frame. Set WEMODE =1 (Frame Memory Access and Interface Setting (B3h)).

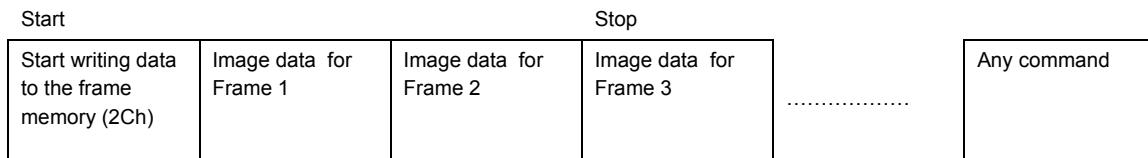


Figure 15

- Notes:
1. Two write methods are available for all data transfer color modes in 16-/8-bit bus display command interface.
 2. The number of pixel in one frame can be odd or even in both download methods. Only complete data sets are retained in the frame memory.
 3. The data write operation to the frame memory is terminated when a command intervenes in the middle of the course. In this case, if write_memory_continue (3Ch) is executed, the write operation can be started again from the address where the write operation is halted.

DBI Type B Data Format

The R61529 supports color formats shown below.

Table 13

Type	IM3-0	Data pin	Color format	MIPI Spec.	R61529 implementation
Type B	0111	DB[23:0]	16bpp	No	Yes
			18bpp	No	Yes
			24bpp	No	Yes
	0110	DB[17:0]	16bpp	No	Yes
			18bpp	No	Yes
			24bpp	No	Yes
	0101	DB[15:0]	8bpp	Yes	No
			12bpp	Yes	No
			16bpp	Yes	Yes
			18bpp (262,144-color Option1)	Yes	Yes
			18bpp (262,144-color Option2)	Yes	Yes
			24bpp (16,777,216-color Option1)	Yes	Yes
			24bpp (16,777,216-color Option2)	Yes	Yes
	-	DB[8:0]	18bpp	Yes	No
	0100	DB[7:0]	8bpp	Yes	No
			12bpp	Yes	No
			16bpp	Yes	Yes
			18bpp	Yes	Yes
			24bpp	Yes	Yes

Yes: Supported

No: Unsupported

1. 24-Bit Bus Interface [IM3-0 = 0111]

(a) Command/Parameter Write

set_pixel_format (3Ah) = *. DFM = *.

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
																D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

Figure 16

(b) Command/Parameter Read

set_pixel_format (3Ah) = *. DFM = *.

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
																D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

Figure 17

The first Command/Parameter Read after read command is issued is invalid. (Dummy read)

(c) 24bpp Frame Memory Write

set_pixel_format (3Ah) = 3'h7. DFM = *.

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R[7]	R[6]	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[7]	G[6]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

Figure 18

(d) 18bpp Frame Memory Write

set_pixel_format (3Ah) = 3'h6. DFM = *.

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
					R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]	

Figure 19

(e) 16bpp Frame Memory Write

set_pixel_format (3Ah) = 3'h5. DFM = *.

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
								R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]

Figure 20

(f) 24bpp Frame Memory Read

set_pixel_format (3Ah) = *. DFM = *.

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
r[7]	r[6]	r[5]	r[4]	r[3]	r[2]	r[1]	r[0]	g[7]	g[6]	g[5]	g[4]	g[3]	g[2]	g[1]	g[0]	b[7]	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0]

Figure 21

2. 18-Bit Bus Interface [IM3-0 = 0110]

(a) Command/Parameter Write

set_pixel_format (3Ah) = *. DFM = *.

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
																D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

Figure 22

(b) Command/Parameter Read

set_pixel_format (3Ah) = *. DFM = *.

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
																D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

Figure 23

The first Command/Parameter Read after read command is issued is invalid. (Dummy read)

(c) 24bpp Frame Memory Write (Option 1)

set_pixel_format (3Ah) = 3'h7. DFM = *.

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1 st transfer								R1[7]	R1[6]	R1[5]	R1[4]	R1[3]	R1[2]	R1[1]	R1[0]	G1[7]	G1[6]	G1[5]	G1[4]	G1[3]	G1[2]	G1[1]	G1[0]
D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
2 nd transfer								B1[7]	B1[6]	B1[5]	B1[4]	B1[3]	B1[2]	B1[1]	B1[0]	R2[7]	R2[6]	R2[5]	R2[4]	R2[3]	R2[2]	R2[1]	R2[0]
D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
3 rd transfer								G2[7]	G2[6]	G2[5]	G2[4]	G2[3]	G2[2]	G2[1]	G2[0]	B2[7]	B2[6]	B2[5]	B2[4]	B2[3]	B2[2]	B2[1]	B2[0]

Figure 24

The first pixel data is written to frame memory after the 2nd transfer. If data transfer stops after the 2nd transfer, the first pixel data are written normally. This applies to the last address when the number of pixels is odd according to window setting.

(d) 18bpp Frame Memory Write (Option 1)

set_pixel_format (3Ah) = 3'h6. DFM = *.

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
						R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

Figure 25

(e) 16bpp Frame Memory Write

set_pixel_format (3Ah) = 3'h5. DFM = *.

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
						R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]		

Figure 26

(f) 24bpp Frame Memory Read

set_pixel_format (3Ah) = 3'h*. DFM = *.

	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1 st transfer									r1[7]	r1[6]	r1[5]	r1[4]	r1[3]	r1[2]	r1[1]	r1[0]	g1[7]	g1[6]	g1[5]	g1[4]	g1[3]	g1[2]	g1[1]	g1[0]
2 nd transfer								b1[7]	b1[6]	b1[5]	b1[4]	b1[3]	b1[2]	b1[1]	b1[0]	r2[7]	r2[6]	r2[5]	r2[4]	r2[3]	r2[2]	r2[1]	r2[0]	
3 rd transfer								g2[7]	g2[6]	g2[5]	g2[4]	g2[3]	g2[2]	g2[1]	g2[0]	b2[7]	b2[6]	b2[5]	b2[4]	b2[3]	b2[2]	b2[1]	b2[0]	

Figure 27

3. 16-Bit Bus Interface [IM3-0 = 0101]

(a) Command/Parameter Write

set_pixel_format (3Ah) = *. DFM = *.

	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
																	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

Figure 28

(b) Command/Parameter Read

set_pixel_format (3Ah) = *. DFM = *.

	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
																	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

Figure 29

The first Command/Parameter Read after read command is issued is invalid. (Dummy read)

(c) 24bpp Frame Memory Write (Option 1)

set_pixel_format (3Ah) = 3'h7. DFM = 0.

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1 st transfer								R1[7]	R1[6]	R1[5]	R1[4]	R1[3]	R1[2]	R1[1]	R1[0]	G1[7]	G1[6]	G1[5]	G1[4]	G1[3]	G1[2]	G1[1]	G1[0]
D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
2 nd transfer								B1[7]	B1[6]	B1[5]	B1[4]	B1[3]	B1[2]	B1[1]	B1[0]	R2[7]	R2[6]	R2[5]	R2[4]	R2[3]	R2[2]	R2[1]	R2[0]
D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
3 rd transfer								G2[7]	G2[6]	G2[5]	G2[4]	G2[3]	G2[2]	G2[1]	G2[0]	B2[7]	B2[6]	B2[5]	B2[4]	B2[3]	B2[2]	B2[1]	B2[0]

Figure 30

The first pixel data is written to frame memory after the 2nd transfer. If data transfer stops after the 2nd transfer, the first pixel data are written normally. This applies to the last address when the number of pixels is odd according to window setting.

(d) 24bpp Frame Memory Write (Option 2)

set_pixel_format (3Ah) = 3'h7. DFM = 1.

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1 st transfer																R1[7]	R1[6]	R1[5]	R1[4]	R1[3]	R1[2]	R1[1]	R1[0]
D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
2 nd transfer								G1[7]	G1[6]	G1[5]	G1[4]	G1[3]	G1[2]	G1[1]	G1[0]	B1[7]	B1[6]	B1[5]	B1[4]	B1[3]	B1[2]	B1[1]	B1[0]

Figure 31

Data are written to the Frame Memory when data for one pixel are input.

(e) 18bpp Frame Memory Write (Option 1)

set_pixel_format (3Ah) = 3'h6. DFM = 0.

	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1 st transfer									R1[5]	R1[4]	R1[3]	R1[2]	R1[1]	R1[0]			G1[5]	G1[4]	G1[3]	G1[2]	G1[1]	G1[0]		
2 nd transfer	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
									B1[5]	B1[4]	B1[3]	B1[2]	B1[1]	B1[0]			R2[5]	R2[4]	R2[3]	R2[2]	R2[1]	R2[0]		
3 rd transfer	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
									G2[5]	G2[4]	G2[3]	G2[2]	G2[1]	G2[0]			B2[5]	B2[4]	B2[3]	B2[2]	B2[1]	B2[0]		

Figure 32

The first pixel data is written to frame memory after the 2nd transfer. If data transfer stops after the 2nd transfer, the first pixel data are written normally. This applies to the last address when the number of pixels is odd according to window setting.

(f) 18bpp Frame Memory Write (Option 2)

set_pixel_format (3Ah) = 3'h6. DFM = 1.

	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1 st transfer																	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]		
2 nd transfer	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
									G[5]	G[4]	G[3]	G[2]	G[1]	G[0]			B[5]	B[4]	B[3]	B[2]	B[1]	B[0]		

Figure 33

Data are written to the Frame Memory when data for one pixel are input.

(g) 18bpp Frame Memory Write (Option 3)

set_pixel_format (3Ah) = 3'h6. DFM = 2.

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
1 st transfer								R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	
2 nd transfer	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
								B[1]	B[0]															

Figure 34

Data are written to the Frame Memory when data for one pixel are input.

(h) 16bpp Frame Memory Write

set_pixel_format (3Ah) = 3'h5. DFM = *.

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
								R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]

Figure 35

(i) 24bpp Frame Memory Read

set_pixel_format (3Ah) = *. DFM = 0.

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
1 st transfer								r1[7]	r1[6]	r1[5]	r1[4]	r1[3]	r1[2]	r1[1]	r1[0]	r1[7]	g1[6]	g1[5]	g1[4]	g1[3]	g1[2]	g1[1]	g1[0]	
2 nd transfer	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
								b1[7]	b1[6]	b1[5]	b1[4]	b1[3]	b1[2]	b1[1]	b1[0]	r2[7]	r2[6]	r2[5]	r2[4]	r2[3]	r2[2]	r2[1]	r2[0]	
3 rd transfer	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
								g2[7]	g2[6]	g2[5]	g2[4]	g2[3]	g2[2]	g2[1]	g2[0]	b2[7]	b2[6]	b2[5]	b2[4]	b2[3]	b2[2]	b2[1]	b2[0]	

Figure 36

(j) 24bpp Frame Memory Read

set_pixel_format (3Ah) = *. DFM = 1.

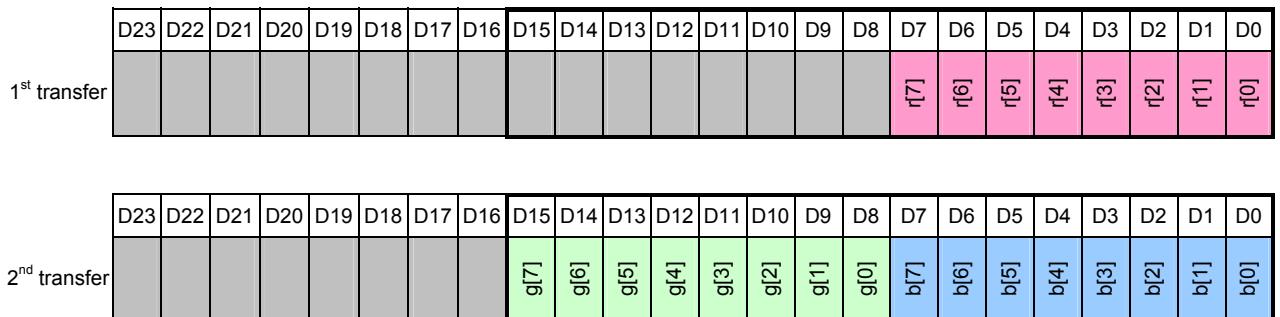


Figure 37

4. 8-Bit Bus Interface [IM3-0 = 0100]

(a) Command/Parameter Write

set_pixel_format (3Ah) = *. DFM = *.

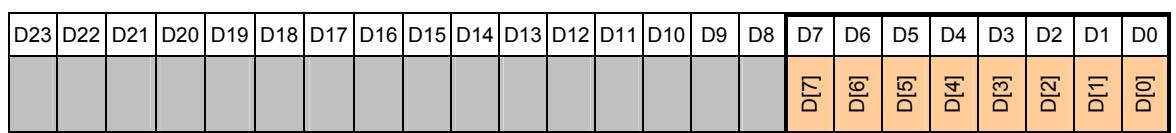


Figure 38

(b) Command/Parameter Read

set_pixel_format (3Ah) = *. DFM = *.

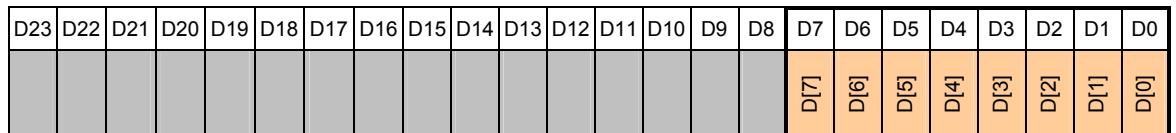


Figure 39

The first Command/Parameter Read after read command is issued is invalid. (Dummy read)

(c) 24bpp Frame Memory Write

set_pixel_format (3Ah) = 3'h7. DFM = *.

	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
1 st transfer																	R[7]	R[6]	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	
2 nd transfer		D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
																	G[7]	G[6]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	
3 rd transfer		D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
																	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]	

Figure 40

(d) 18bpp Frame Memory Write (Option 1)

set_pixel_format (3Ah) = 3'h6. DFM = 0.

	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
1 st transfer																	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]			
2 nd transfer		D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
																	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]			
3 rd transfer		D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
																	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]			

Figure 41

(e) 18bpp Frame Memory Write (Option 2)

set_pixel_format (3Ah) = 3'h6. DFM = 1.

	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1 st transfer																		R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	
2 nd transfer	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
																	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]		
3 rd transfer	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
																	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]		

Figure 42

(f) 16bpp Frame Memory Write (Option 1)

set_pixel_format (3Ah) = 3'h5. DFM = 0.

	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1 st transfer																	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]
2 nd transfer	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
																	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]

Figure 43

(g) 16bpp Frame Memory Write (Option 2)

set_pixel_format (3Ah) = 3'h5. DFM = 1.

	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1 st transfer																				R[4]	R[3]	R[2]	R[1]	R[0]
2 nd transfer	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
																		G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	
3 rd transfer	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
																		B[4]	B[3]	B[2]	B[1]	B[0]		

Figure 44

(h) 24bpp Frame Memory Read

set_pixel_format (3Ah) = 3'h*. DFM = *.

	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0			
1 st transfer																				r[7]	r[6]	r[5]	r[4]	r[3]	r[2]	r[1]	r[0]
2 nd transfer	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0			
																			g[7]	g[6]	g[5]	g[4]	g[3]	g[2]	g[1]	g[0]	
3 rd transfer	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0			
																			b[7]	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0]	

Figure 45

5. Extended Format for 24 Bits/Pixel Data in 16-/18-Bit Interface Operation

The R61529 supports a format extended from 16bpp or 18bpp to 24bpp as shown below. A method for extending a format is set by EPF.

	Frame memory data (24 bits)																									
	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0		
24bpp																										
18bpp EPF=2'h0 (Note 1)	R[4]	R[4]	R[5]	R[5]	R[6]	R[6]	R[7]	R[7]																		
18bpp EPF=2'h1 (Note 2)	R[3]	R[3]	R[4]	R[4]	R[5]	R[5]	R[6]	R[6]																		
18bpp EPF=2'h2	R[2]	R[2]	R[3]	R[3]	R[4]	R[4]	R[5]	R[5]																		
16bpp EPF=2'h0 (Note 3)	R[1]	R[1]	R[2]	R[2]	R[1]	R[1]	R[0]	R[0]	R[0]	R[0]	R[0]	R[0]	R[0]	R[0]	R[0]	R[0]	R[0]	R[0]	R[0]	R[0]	R[0]	R[0]	R[0]	R[0]	R[0]	
16bpp EPF=2'h1 (Note 4)	R[0]	R[0]	R[1]	R[1]	R[0]	R[0]	R[1]	R[1]	R[1]	R[1]	R[1]	R[1]	R[1]	R[1]	R[1]	R[1]	R[1]	R[1]	R[1]	R[1]	R[1]	R[1]	R[1]	R[1]	R[1]	
16bpp EPF=2'h2	R[4]	R[4]	R[5]	R[5]	R[6]	R[6]	R[7]	R[7]	G[5]	G[5]	G[6]	G[6]	G[7]	G[7]	G[8]	G[8]	G[9]	G[9]	G[10]	G[10]	G[11]	G[11]	G[12]	G[12]	G[13]	
	R[3]	R[3]	R[4]	R[4]	R[5]	R[5]	R[6]	R[6]	G[4]	G[4]	G[5]	G[5]	G[6]	G[6]	G[7]	G[7]	G[8]	G[8]	G[9]	G[9]	G[10]	G[10]	G[11]	G[11]	G[12]	G[12]
	R[2]	R[2]	R[3]	R[3]	R[4]	R[4]	R[5]	R[5]	G[3]	G[3]	G[4]	G[4]	G[5]	G[5]	G[6]	G[6]	G[7]	G[7]	G[8]	G[8]	G[9]	G[9]	G[10]	G[10]	G[11]	G[11]
	R[1]	R[1]	R[2]	R[2]	R[3]	R[3]	R[4]	R[4]	G[2]	G[2]	G[3]	G[3]	G[4]	G[4]	G[5]	G[5]	G[6]	G[6]	G[7]	G[7]	G[8]	G[8]	G[9]	G[9]	G[10]	G[10]
	R[0]	R[0]	R[1]	R[1]	R[2]	R[2]	R[3]	R[3]	G[1]	G[1]	G[2]	G[2]	G[3]	G[3]	G[4]	G[4]	G[5]	G[5]	G[6]	G[6]	G[7]	G[7]	G[8]	G[8]	G[9]	G[9]
	G[5]	G[5]	G[6]	G[6]	G[7]	G[7]	G[8]	G[8]	G[9]	G[9]	G[10]	G[10]	G[11]	G[11]	G[12]	G[12]	G[13]	G[13]	G[14]	G[14]	G[15]	G[15]	G[16]	G[16]	G[17]	G[17]
	G[4]	G[4]	G[5]	G[5]	G[6]	G[6]	G[7]	G[7]	G[8]	G[8]	G[9]	G[9]	G[10]	G[10]	G[11]	G[11]	G[12]	G[12]	G[13]	G[13]	G[14]	G[14]	G[15]	G[15]	G[16]	G[16]
	G[3]	G[3]	G[4]	G[4]	G[5]	G[5]	G[6]	G[6]	G[7]	G[7]	G[8]	G[8]	G[9]	G[9]	G[10]	G[10]	G[11]	G[11]	G[12]	G[12]	G[13]	G[13]	G[14]	G[14]	G[15]	G[15]
	G[2]	G[2]	G[3]	G[3]	G[4]	G[4]	G[5]	G[5]	G[6]	G[6]	G[7]	G[7]	G[8]	G[8]	G[9]	G[9]	G[10]	G[10]	G[11]	G[11]	G[12]	G[12]	G[13]	G[13]	G[14]	G[14]
	G[1]	G[1]	G[2]	G[2]	G[3]	G[3]	G[4]	G[4]	G[5]	G[5]	G[6]	G[6]	G[7]	G[7]	G[8]	G[8]	G[9]	G[9]	G[10]	G[10]	G[11]	G[11]	G[12]	G[12]	G[13]	G[13]
	G[0]	G[0]	G[1]	G[1]	G[2]	G[2]	G[3]	G[3]	G[4]	G[4]	G[5]	G[5]	G[6]	G[6]	G[7]	G[7]	G[8]	G[8]	G[9]	G[9]	G[10]	G[10]	G[11]	G[11]	G[12]	G[12]
	G[5]	G[5]	G[6]	G[6]	G[7]	G[7]	G[8]	G[8]	G[9]	G[9]	G[10]	G[10]	G[11]	G[11]	G[12]	G[12]	G[13]	G[13]	G[14]	G[14]	G[15]	G[15]	G[16]	G[16]	G[17]	G[17]
	G[4]	G[4]	G[5]	G[5]	G[6]	G[6]	G[7]	G[7]	G[8]	G[8]	G[9]	G[9]	G[10]	G[10]	G[11]	G[11]	G[12]	G[12]	G[13]	G[13]	G[14]	G[14]	G[15]	G[15]	G[16]	G[16]
	B[4]	B[4]	B[5]	B[5]	B[6]	B[6]	B[7]	B[7]	B[8]	B[8]	B[9]	B[9]	B[10]	B[10]	B[11]	B[11]	B[12]	B[12]	B[13]	B[13]	B[14]	B[14]	B[15]	B[15]	B[16]	B[16]
	B[3]	B[3]	B[4]	B[4]	B[5]	B[5]	B[6]	B[6]	B[7]	B[7]	B[8]	B[8]	B[9]	B[9]	B[10]	B[10]	B[11]	B[11]	B[12]	B[12]	B[13]	B[13]	B[14]	B[14]	B[15]	B[15]
	B[2]	B[2]	B[3]	B[3]	B[4]	B[4]	B[5]	B[5]	B[6]	B[6]	B[7]	B[7]	B[8]	B[8]	B[9]	B[9]	B[10]	B[10]	B[11]	B[11]	B[12]	B[12]	B[13]	B[13]	B[14]	B[14]
	B[1]	B[1]	B[2]	B[2]	B[3]	B[3]	B[4]	B[4]	B[5]	B[5]	B[6]	B[6]	B[7]	B[7]	B[8]	B[8]	B[9]	B[9]	B[10]	B[10]	B[11]	B[11]	B[12]	B[12]	B[13]	B[13]
	B[0]	B[0]	B[1]	B[1]	B[2]	B[2]	B[3]	B[3]	B[4]	B[4]	B[5]	B[5]	B[6]	B[6]	B[7]	B[7]	B[8]	B[8]	B[9]	B[9]	B[10]	B[10]	B[11]	B[11]	B[12]	B[12]
	B[4]	B[4]	B[5]	B[5]	B[6]	B[6]	B[7]	B[7]	B[8]	B[8]	B[9]	B[9]	B[10]	B[10]	B[11]	B[11]	B[12]	B[12]	B[13]	B[13]	B[14]	B[14]	B[15]	B[15]	B[16]	B[16]
	B[3]	B[3]	B[4]	B[4]	B[5]	B[5]	B[6]	B[6]	B[7]	B[7]	B[8]	B[8]	B[9]	B[9]	B[10]	B[10]	B[11]	B[11]	B[12]	B[12]	B[13]	B[13]	B[14]	B[14]	B[15]	B[15]
	B[2]	B[2]	B[3]	B[3]	B[4]	B[4]	B[5]	B[5]	B[6]	B[6]	B[7]	B[7]	B[8]	B[8]	B[9]	B[9]	B[10]	B[10]	B[11]	B[11]	B[12]	B[12]	B[13]	B[13]	B[14]	B[14]

Figure 46

- Notes:
- Special processing: R[5:0], G[5:0], B[5:0] = 6'h3F → 8'hFF
 - Special processing: R[5:0], G[5:0], B[5:0] = 6'h00 → 8'h00
 - Special processing: R[5:0], B[5:0] = 5'h1F → 8'hFF
G[5:0] = 6'h3F → 8'hFF
 - Special processing: R[4:0], B[4:0] = 5'h00 → 8'h00
G[5:0] = 6'h00 → 8'h00
 - Setting EPF to 2'h3 is prohibited.

6. BGR Register Setting and Write/Read Data in Frame Memory

Data written by the host processor is stored in frame memory. When data is stored in frame memory, allocation of R and B in frame memory is swapped according to BGR register setting. Data written to frame memory corresponds to display data. The host processor outputs write and read data in the same RGB order. Examples of BGR register setting are as follows.

BGR = 0

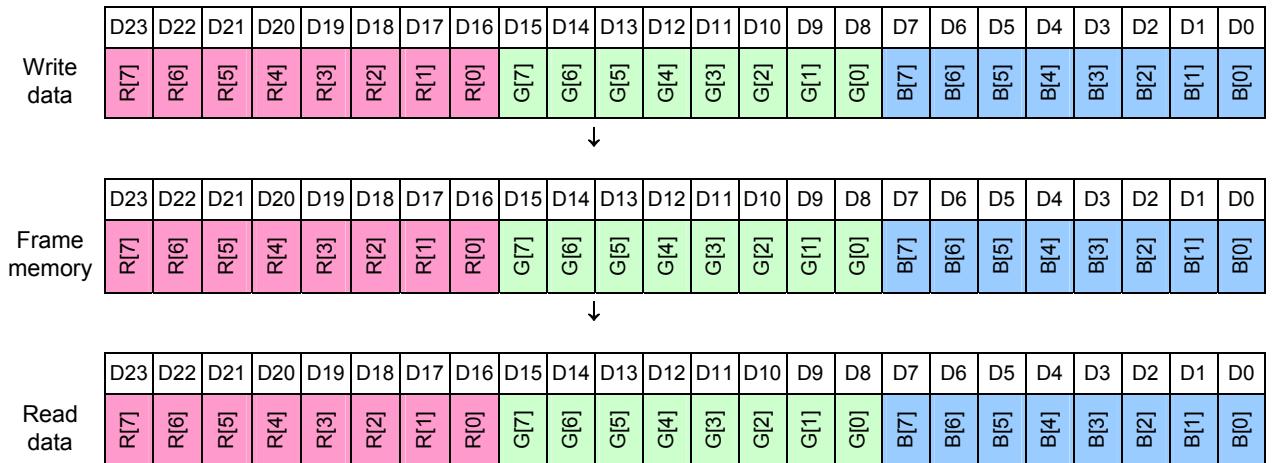
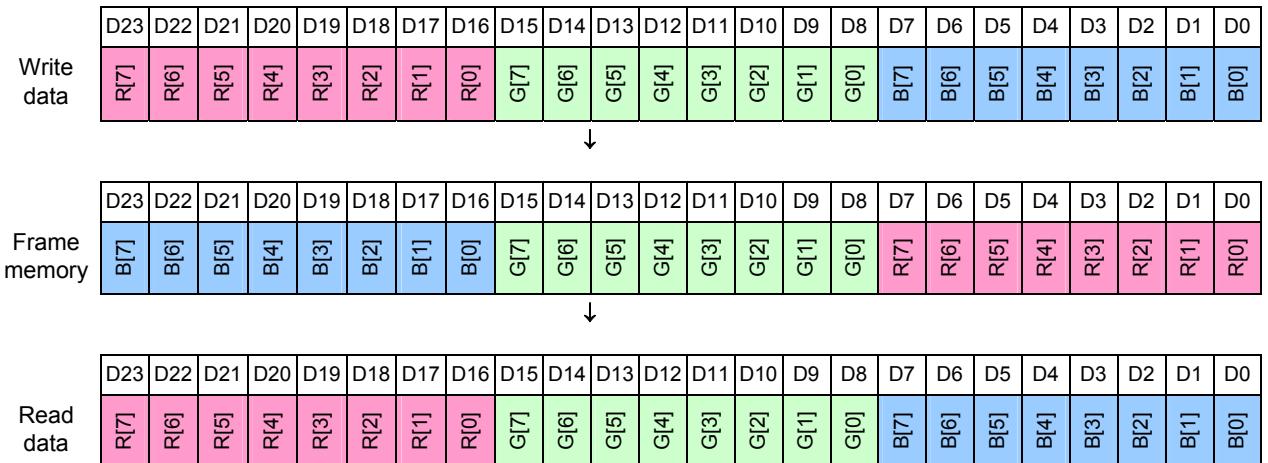


Figure 47

BGR = 1**Figure 48**

A function of B3 bit (36h command) is the same as that of the BGR bit. When data is stored in frame memory, allocation of R and B in frame memory is not swapped. After display data is read from frame memory (before source voltage is output), allocation of R and B in frame memory is swapped. A relationship between B3 bit and BGR bit is Exclusive OR (EOR).

System Interface Configuration (MIPI DBI Type C)

Outline

The R61529 supports serial interface DBI Type C (Option 1 and Option 3). Nine/Eight bit data, transmitted from the R61529 to the host processor, is stored in command register (CDR) or parameter register (PR) to start internal operation which is determined by signals from the host processor.

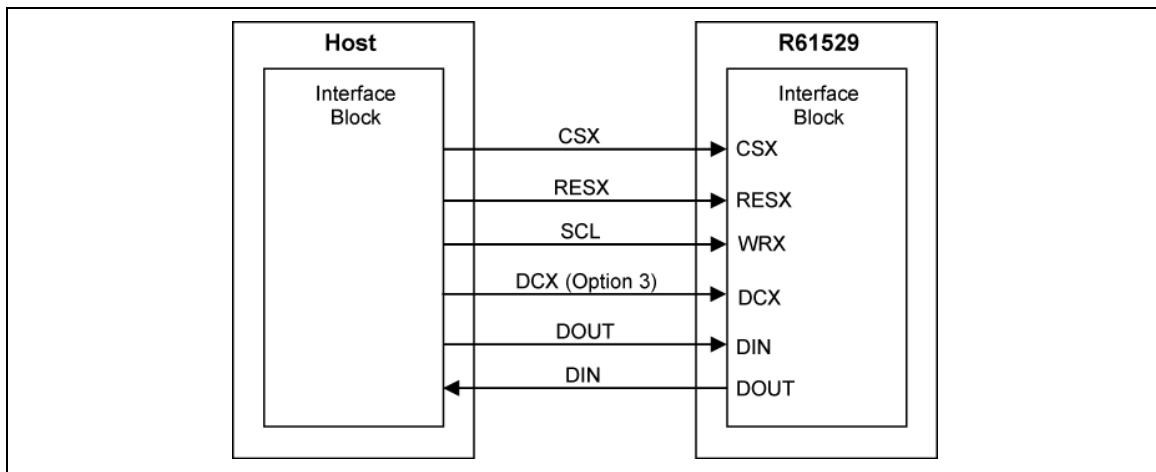
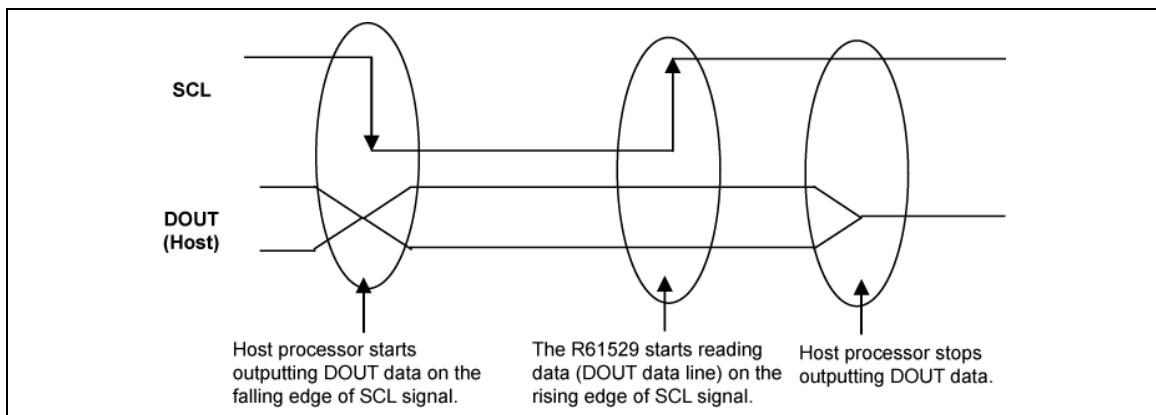


Figure 49 Example of DBI Type C

Write Cycle Sequence

In write cycle, data and/or command are written to the R61529 via the interface between the R61529 and the host processor. During Write Cycle Sequence, the host processor outputs data while the R61529 accepts data at the rising edge of SCL. See next figures for write cycle sequence.



Note: SCL is not a synchronous signal (can be halted).

Figure 50 Write Cycle Sequence

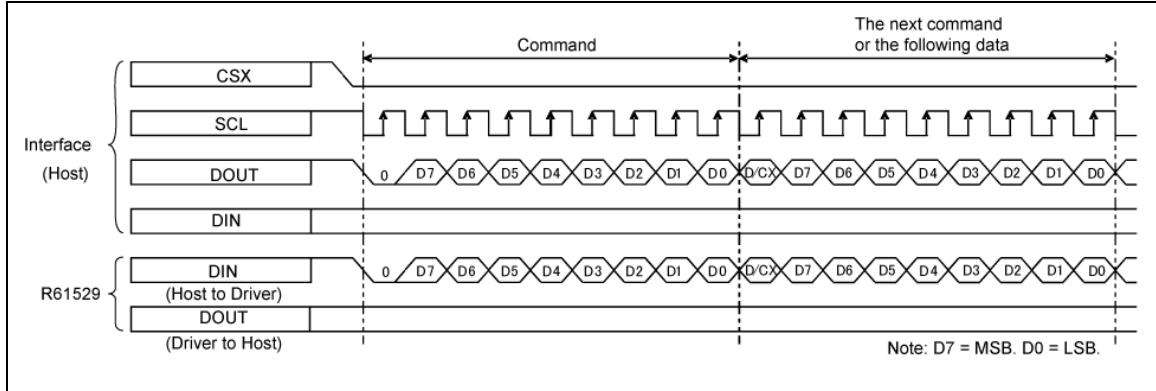


Figure 51 Example of MIPI DBI Type C Write Sequence (Option 1)

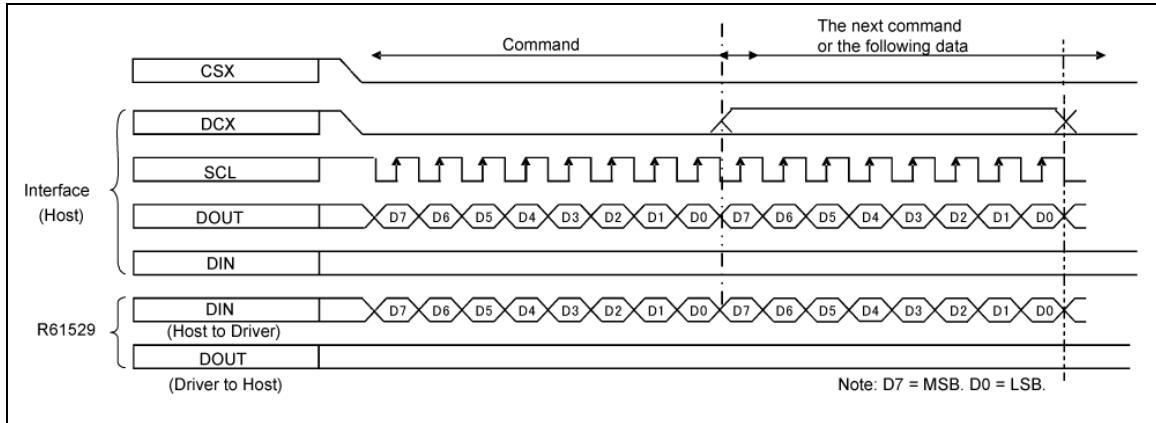
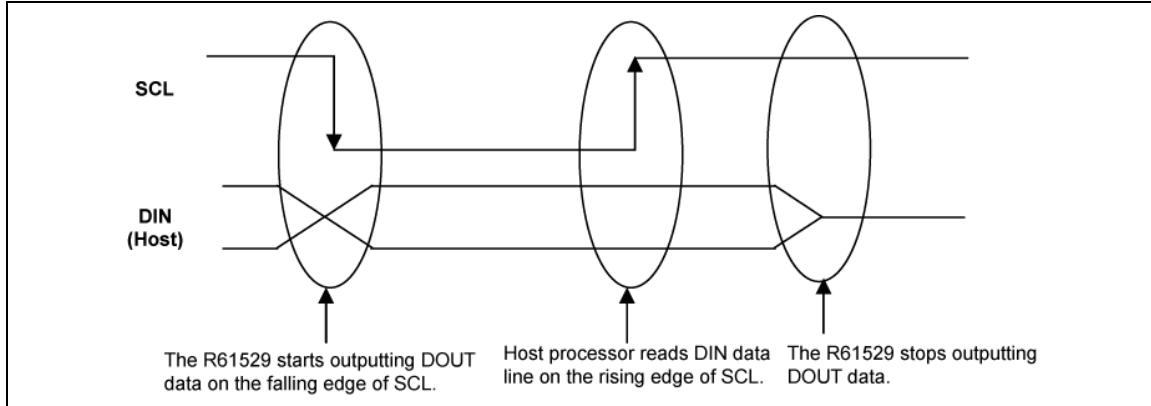


Figure 52 Example of MIPI DBI Type C Write Sequence (Option 3)

Read Cycle Sequence

In read cycle, data and/or commands are read from the R61529 via the interface between the R61529 and the host processor. DOUT data are transmitted from the R61529 to the host processor on the falling edge of SCL. The host processor reads the data on the rising edge of SCL. See next figure for the read cycle sequence.



Note: SCL is not a synchronous signal (can be halted).

Figure 53 Read Cycle Sequence

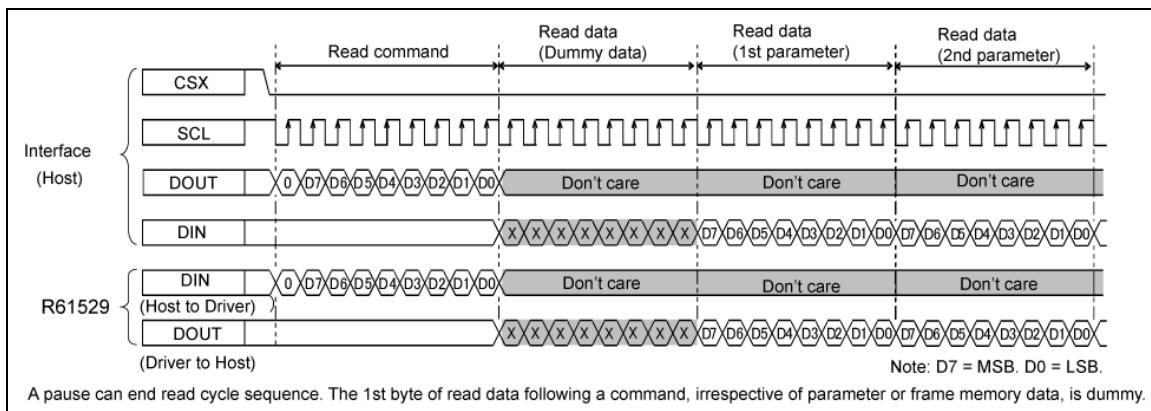


Figure 54 Example of MIPI DBI Type C Read Cycle Sequence (Option 1)

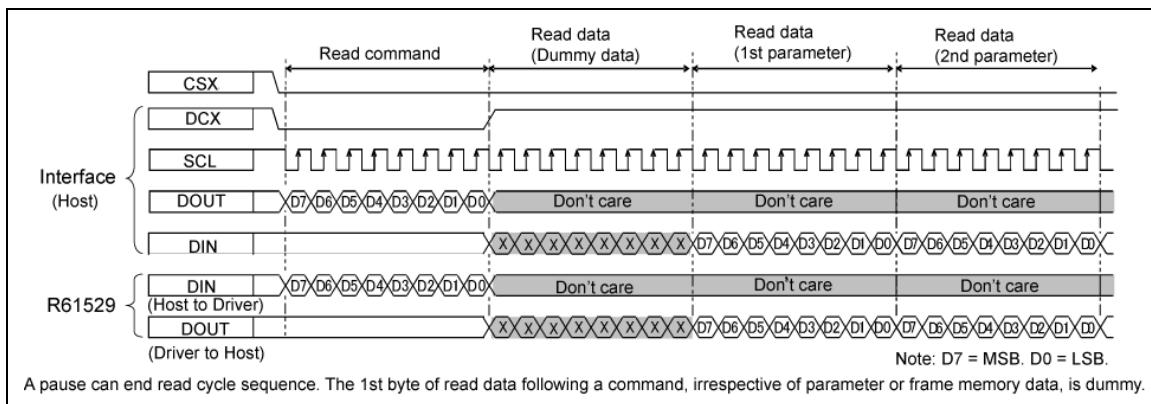


Figure 55 Example of MIPI DBI Type C Read Cycle Sequence (Option 3)

Example of MIPI DBI Type C Read Cycle Sequence (Option 1) Using Read Mode In Command.

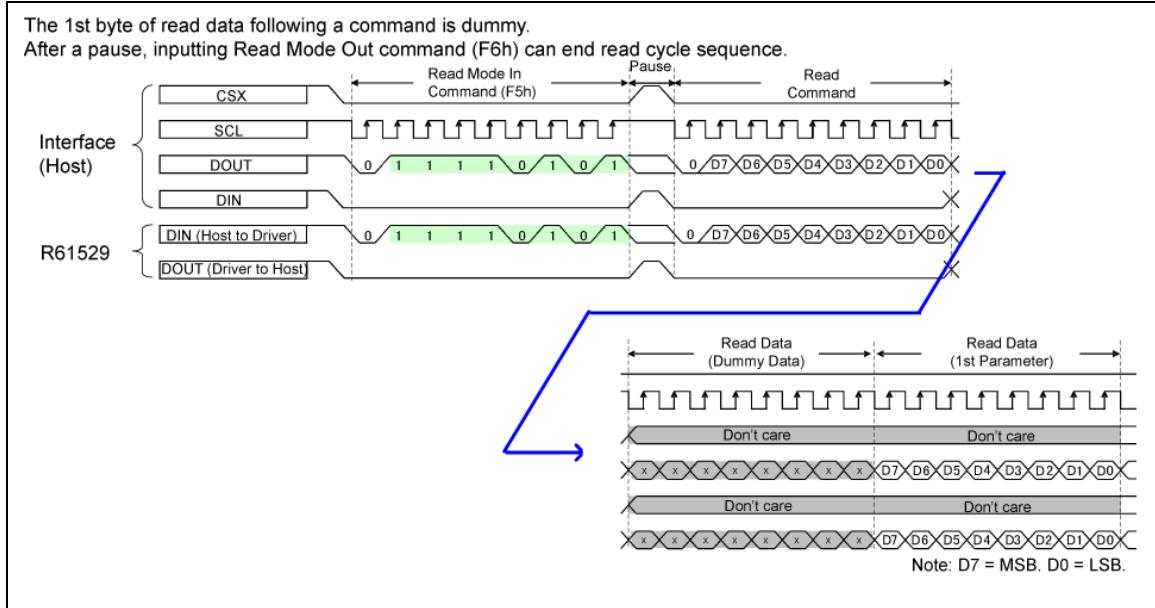


Figure 56

Example of MIPI DBI Type C Read Cycle Sequence (Option 3) Using Read Mode In Command

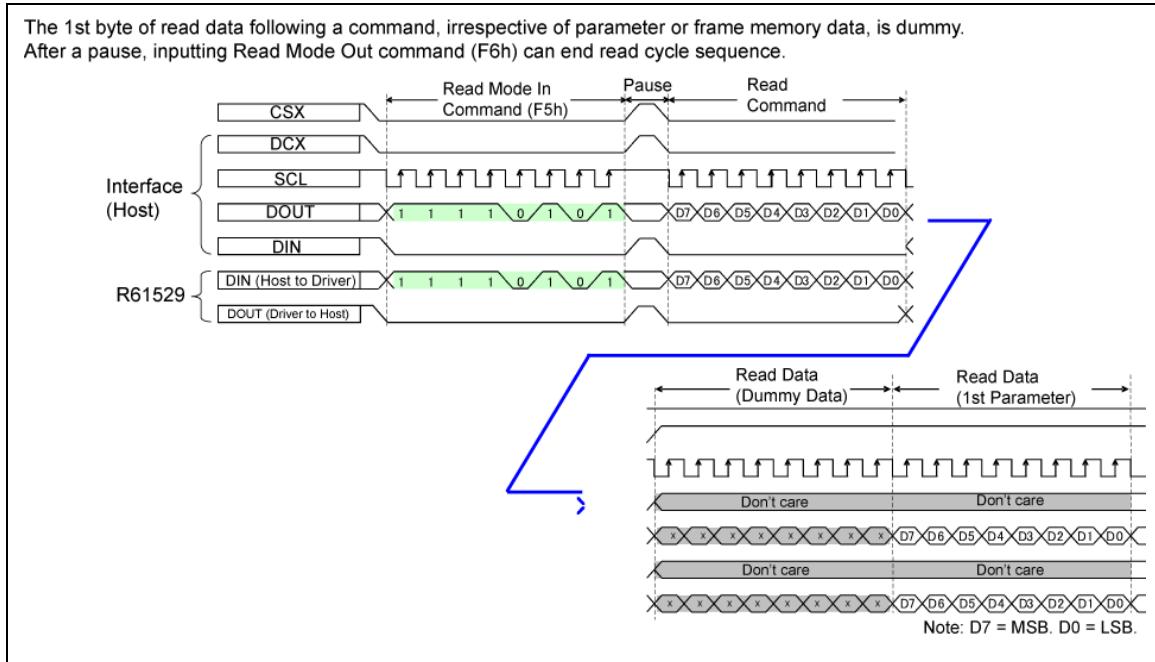


Figure 57

Data Transfer Break

In read cycle, data and/or commands are read from the R61529 via the interface between the R61529 and the host processor. As shown in the figure below, in the transmission of parameter for command from the host processor to the R61529, the command parameters sent to the R61529 before the break occurs are stored in the register of the R61529 when the following two conditions are met. One is that a break occurs before the last parameter of the command is sent to the R61529. The other is that the host processor transmits the parameter(s) of a new command, not the parameters of the interrupted command, when the break occurs. However, those parameters sent after the break is disregarded, and the data in the register is not overwritten.

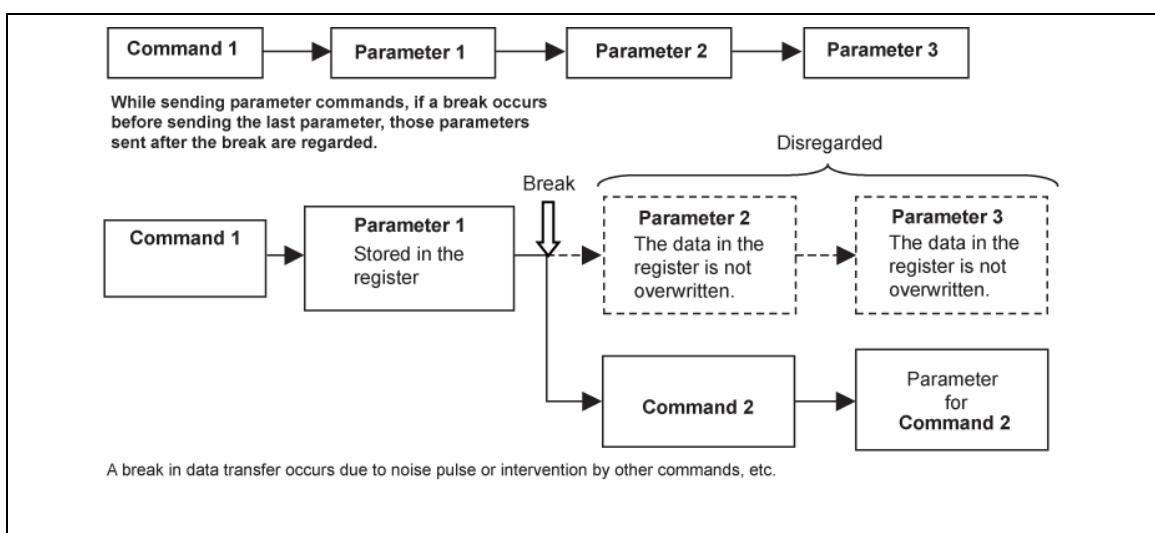


Figure 58

Data Transfer Pause

After transfer of command/parameter ends, write operation resumes from command/parameter right before a stop of transfer if transfer is stopped by setting CSX to “High.” Next transfer starts by setting CSX to “Low.”

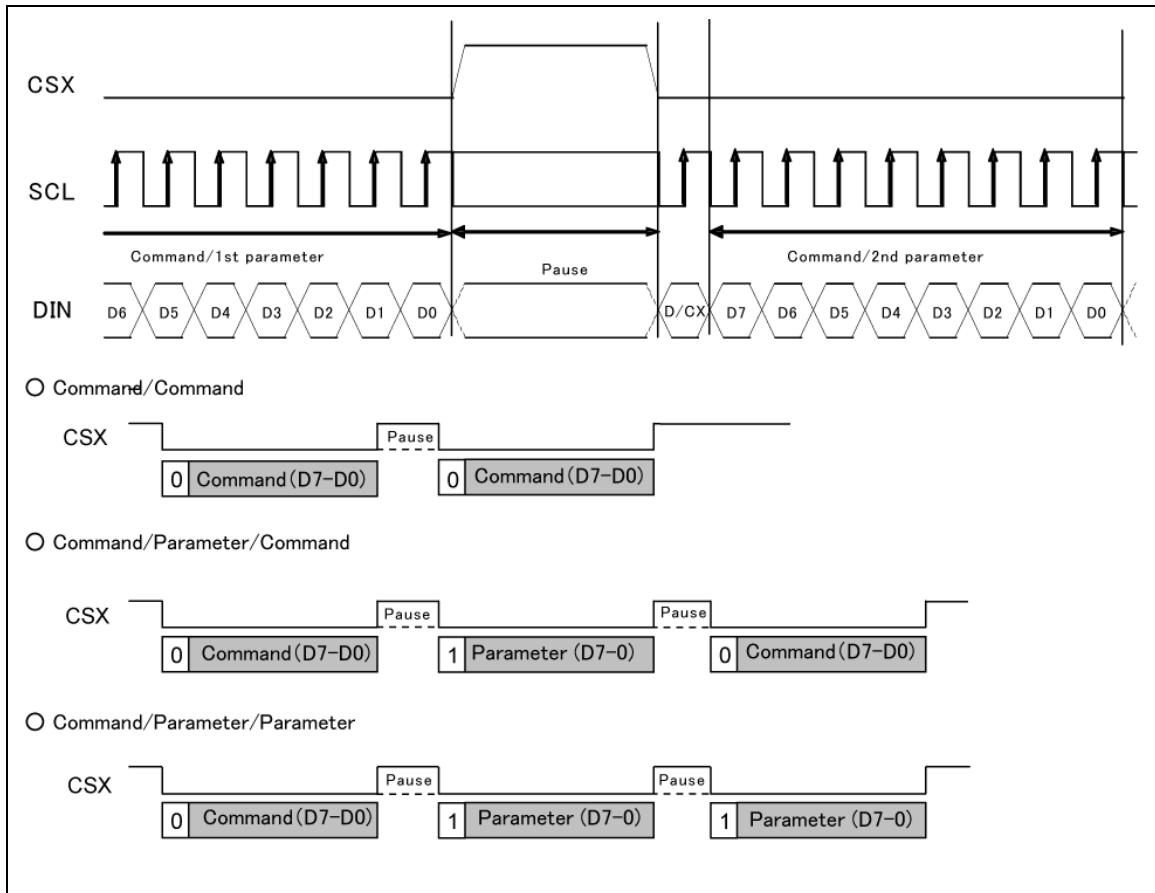


Figure 59

If a pause is invoked during read cycle sequence, transfer should be started with command.

DBI Type C Data Format

The R61529 does not support DCS command (such as 2Ch, 2Eh, 3Ch, 3Eh) to write/read the data to/from the frame memory.

Table 14

Type	IM3-0	Data pin	Color format	MIPI Spec.	R61529 implementation
Type C (Option 1)	0001	DIN DOUT	3bpp (8-color Option 1)	Yes	No
			3bpp (8-color Option 2)	Yes	No
			16bpp (65,536-color Option 1)	No	No
			16bpp (65,536-color Option 2)	No	No
			18bpp (262,144-color Option1)	No	No
			18bpp (262,144-color Option2)	No	No
			24bpp	No	No
Type C (Option 3)	1001	DIN DOUT	3bpp (8-color Option 1)	Yes	No
			3bpp (8-color Option 2)	Yes	No
			16bpp (65,536-color Option 1)	No	No
			16bpp (65,536-color Option 2)	No	No
			18bpp (262,144-color Option1)	No	No
			18bpp (262,144-color Option2)	No	No
			24bpp	No	No

Yes: Supported

No: Unsupported

System Interface Configuration (I^2C)

The R61529 supports I^2C bus interface as serial interface. Data is transferred via serial transmit/receive data bus (DIN) and serial transfer clock line (SCL). In the I^2C bus system, the R61529 is a bidirectional slave device.

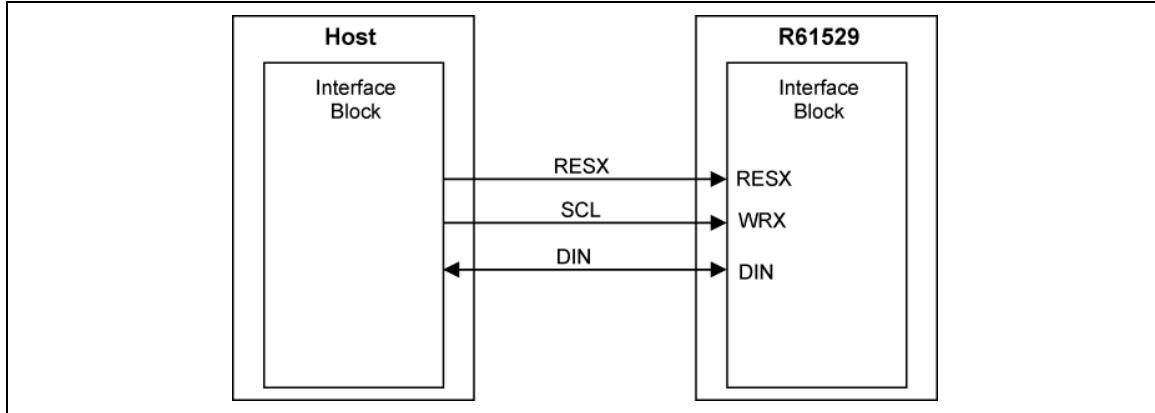


Figure 60 Example of I^2C

Operation mode can be selected from Mode 1 or Mode 2 by setting the IM pins.

- Mode 1: Normal operation
When the R61529 enters Mode 1, it starts data transfer according to a specified slave address.
- Mode 2: NVM Operation
When the R61529 enters Mode 2, it always starts data transfer regardless of a slave address. Write data to NVM in this mode before a slave address is specified.

Note: To connect the interface bus to a device, start data transfer according to a slave address from one specified in other devices.

First Byte of I²C Bus**Table 15**

First byte	Start	1	2	3	4	5	6	7	8	9
		I ² C slave address							R/W	ACK
Mode 1 (normal operation)	Start	IFID [6]	IFID [5]	IFID [4]	IFID [3]	IFID [2]	IFID [1]	IFID [0]	R/W	ACK/NACK
Mode 2 (NVM operation)	Start	X	X	X	X	X	X	X	R/W	ACK/NACK

Table 16

R/W	Function
0	Command write
1	Command read

Table 17

ACK	Function
0	ACK
Hi-Z	NACK

The 7-bit data after the start of transfer is treated as an I²C slave address. In Mode 1, an ID code (IFID[6:0]) stored in NVM beforehand is used as a slave address. If a slave address transferred by host corresponds to the ID code, the subsequent data transfer is treated as access to the R61529. The R61529 returns ACK to host by setting the ninth bit to “L” (ACK operation). If a slave address transferred by host does not correspond to the ID code, the R61529 does not set the ninth bit to “L”. The bit is set to “H” by an external pull-up resistor (NACK operation). In Mode 2, data transfer is treated as access to the R61529 regardless of a slave address.

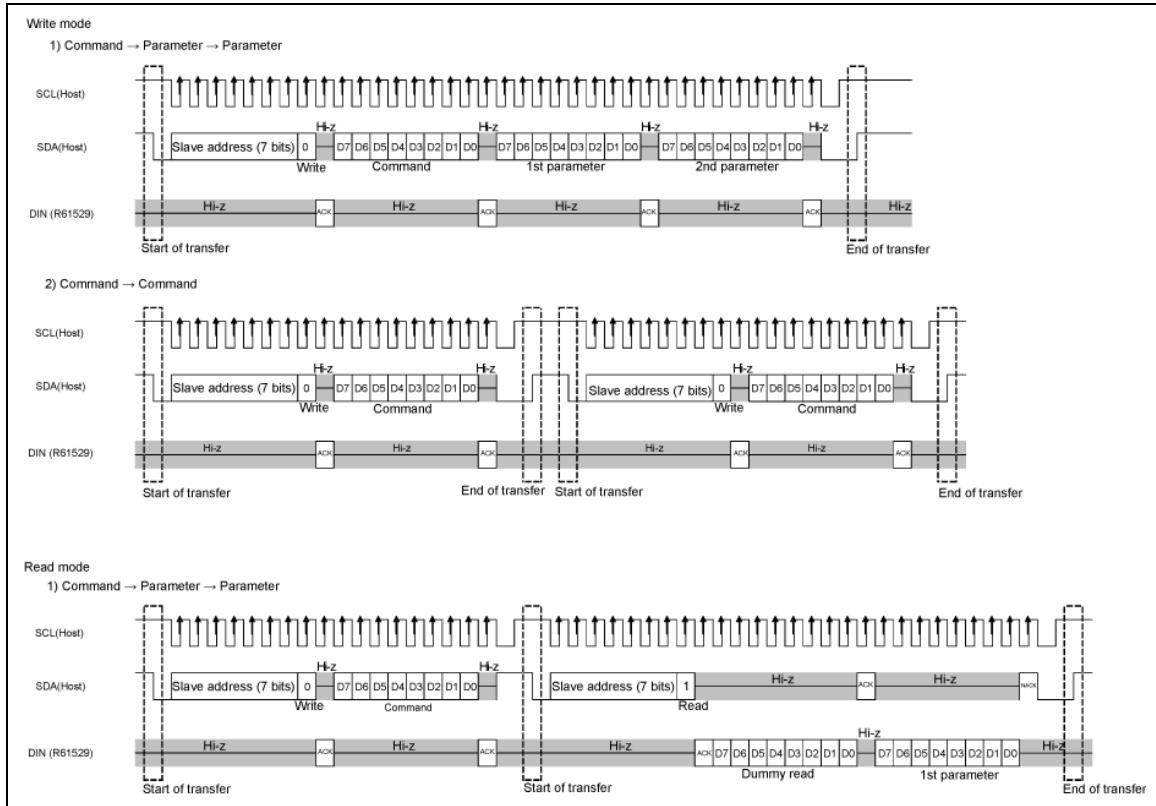


Figure 61 Serial Data Transfer via I²C Bus Interface

I²C Data Format

The R61529 does not support DCS (such as 2Ch, 2Eh, 3Ch, 3Eh) to write/read the data to/from the frame memory.

Table 18

Type	IM3-0	Data pin	Color format	R61529 implementation
I ² C	0000, 1000	DIN	3bpp (8-color Option 1)	No
			3bpp (8-color Option 2)	No
			16bpp (65,536-color Option 1)	No
			16bpp (65,536-color Option 2)	No
			18bpp (262,144-color Option1)	No
			18bpp (262,144-color Option2)	No
			24bpp	No

Yes: Supported

No: Unsupported

System Interface Configuration (MIPI DSI)

The DSI incorporated in the R61529 complies with the following standards:

MIPI DSI: Version 1.01.00r11 21-Feb-2008

MIPI D-PHY: Version 1.00.00 14-May-2009

MIPI DCS: Version 1.01.00

(1) Basic DSI Specification

- Number of data lanes: 1 data lane
- Maximum data rate: 380Mbps/lane @video mode
- Command Mode and Video Mode supported
 - Video data received in Video Mode is directly output as display data without being written to internal RAM
- B5 of set_address_mode command (36h): Setting to 0 (horizontal direction) is supported
- RAM window address setting
 - set_column_address (2Ah)
 - SC[9:0] = 2n (n = 0, 1, 2, ...159)
 - EC[9:0] = 2m – 1 (m = 1, 2, ...160)
 - EC – SC > 2 pixels

(2) DSI System Configuration

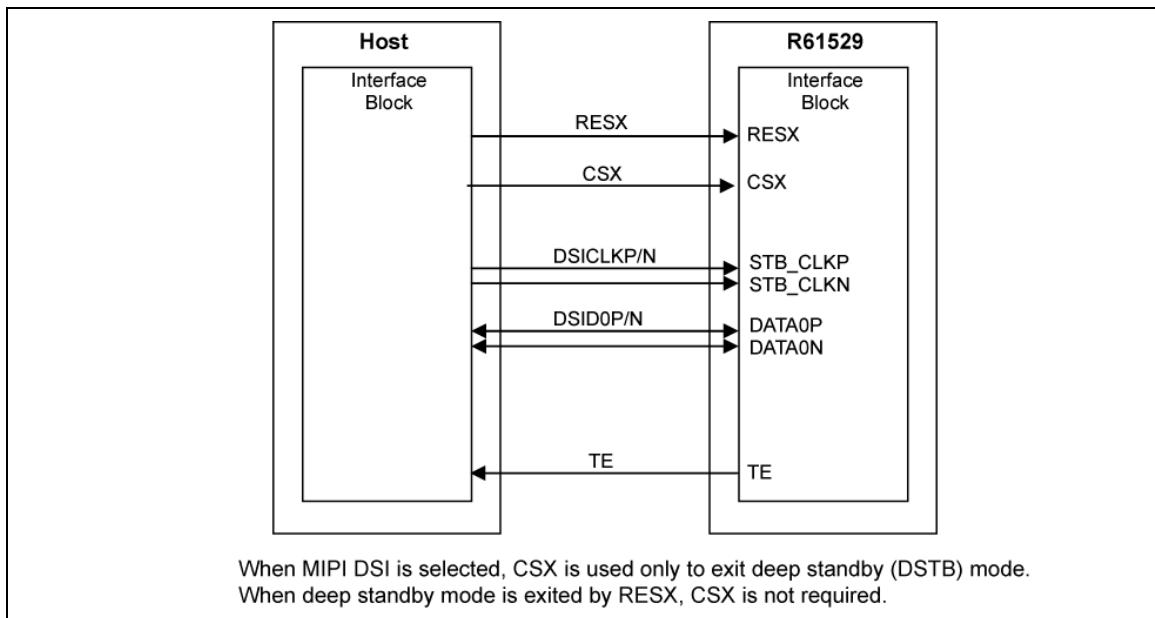


Figure 62 Example of DSI

(3) Lane State Definition

Table 19 Lane State Description

State code	Line voltage levels		High speed	Low power	
	Dp-line	Dn-line	Burst mode	Control mode	Escape mode
HS-0	HS Low	HS High	Differential-0	1	1
HS-1	HS High	HS Low	Differential-1	1	1
LP-00	LP Low	LP Low	N/A	Bridge	Space
LP-01	LP Low	LP High	N/A	HS-Rqst	Mark-0
LP-10	LP High	LP Low	N/A	LP-Rqst	Mark-1
LP-11	LP High	LP High	N/A	Stop	2

Notes:

- During high-speed transmission, the low power receivers observe LP-00 on the lines.
- If LP-11 occurs during Escape mode, the lane returns to Stop state (Control mode LP-11).

(4) DSI-CLK Lane

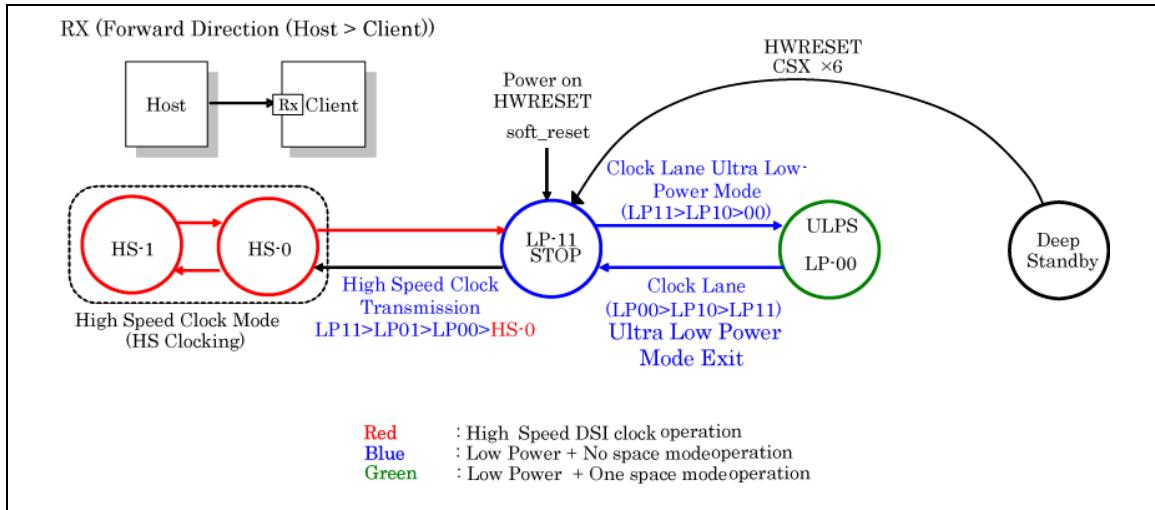
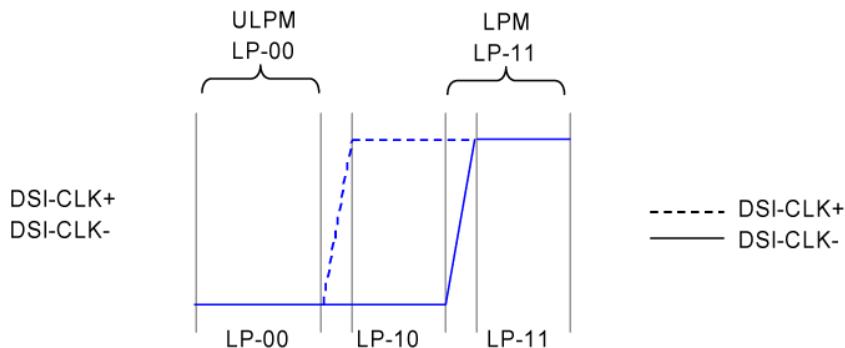


Figure 63 Clock Lane State Diagram

1) Low Power Mode (LP-11: STOP)

- Power on, HWREST
The data lanes and clock lane should be in LP-11 state during power on and HWRESET sequences.
- ULPM → (LP00>LP10>LP11) → LP-11(LPM)



- High Speed Clock Mode (HSCM) → (HS-0) → LP-11(LPM)

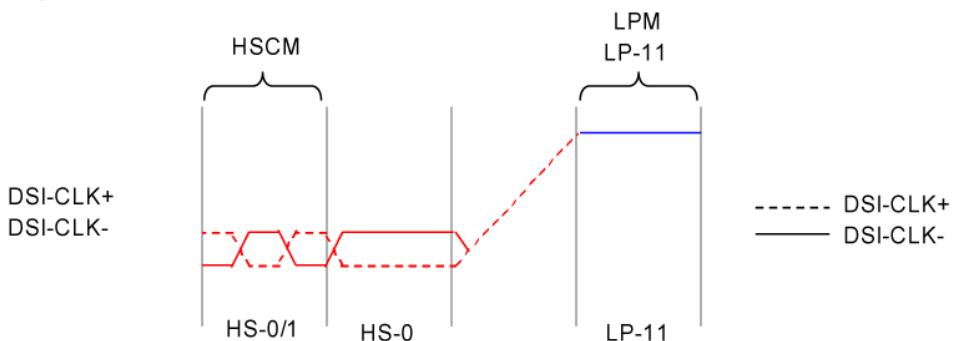


Figure 64 Switching the Clock Lane between Clock Transmission and Low Power Mode 1

2) Ultra Low Power Mode (LP-00: ULPM)

- Ultra Low Power Mode (LP-00:ULPM)
 - LP-11(LPM) → LP-10 → LP-00(ULPM)

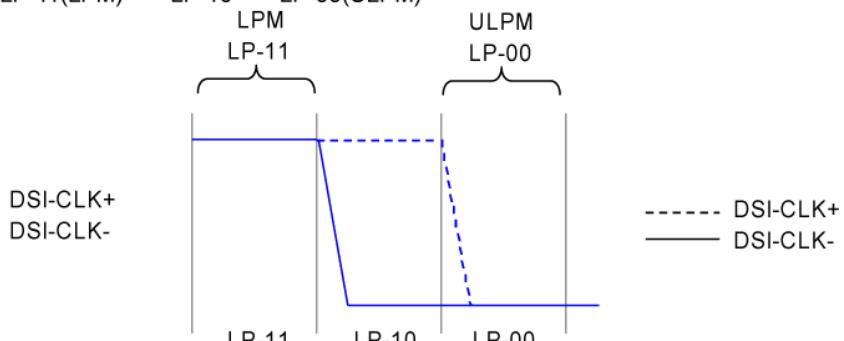


Figure 65 Switching the Clock Lane between Clock Transmission and Low Power Mode 2

3) High Speed Clock Mode

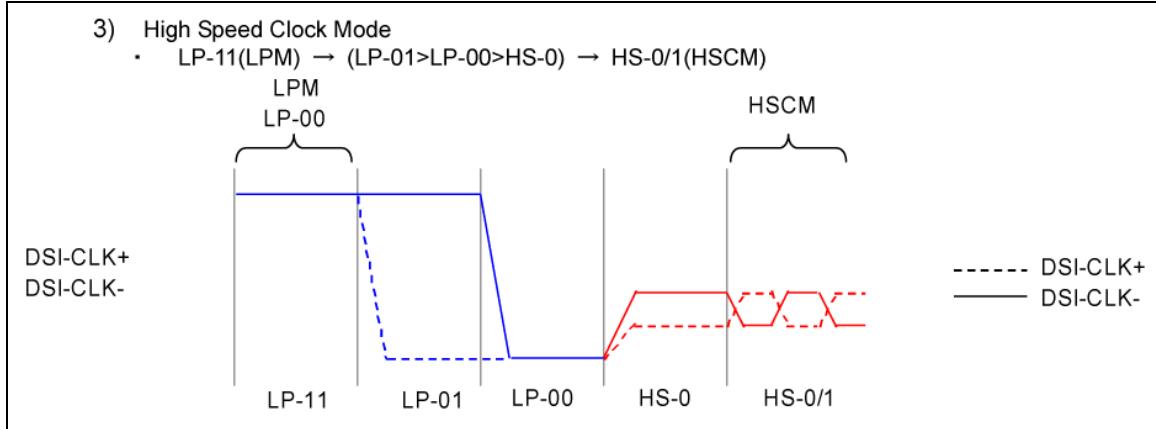


Figure 66 Switching the Clock Lane between Clock Transmission and Low Power Mode 3

4) High Speed Clock Burst

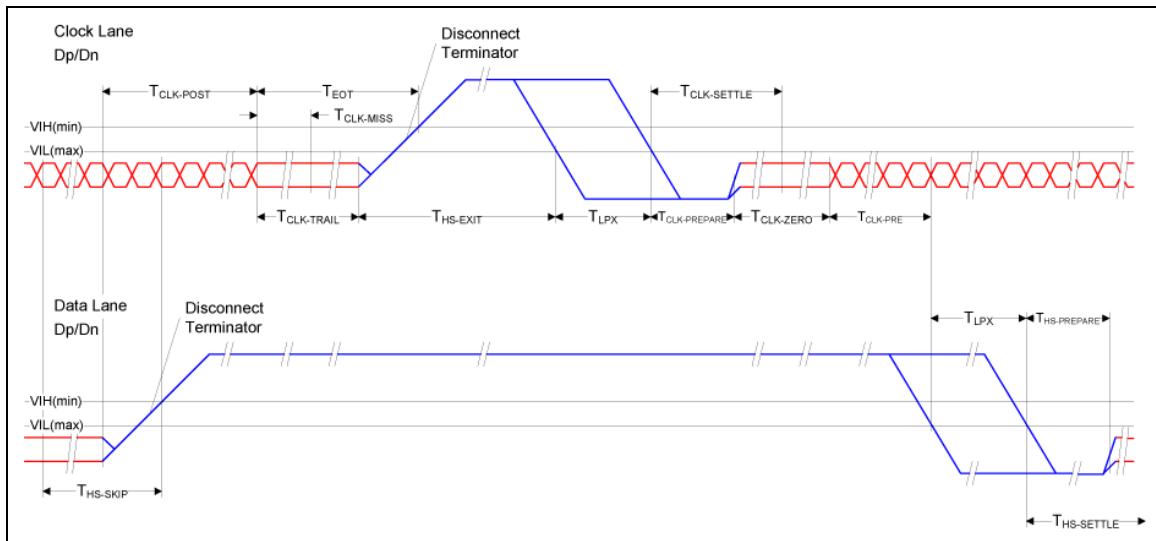


Figure 67 Switching the Clock Lane between Clock Transmission and Low Power Mode 4

(5) DSI-D0 Data Lane

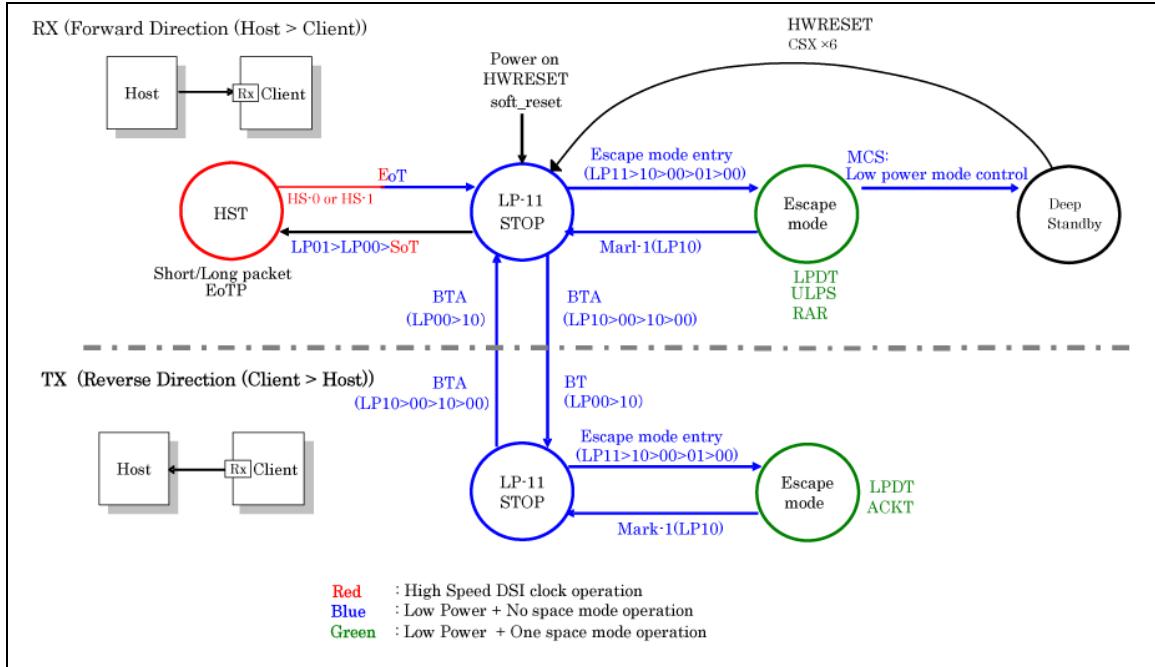


Figure 68 DSI-D0 Data Lane State Diagram

Table 20 Data Lane Operating Modes

No.	Description	Operation code	Note
1	High Speed Data Transmission Burst	LP-11 > L-P01 > LP-00	
2	Escape mode entry	LP-11 > LP-10 > LP-00 > LP-01 > LP-00	
3	Turnaround	LP-11 > LP-10 > LP-00 > LP-10 > LP-00	1
4	Exit Escape mode (Mark-1)	L-10	
5	Deep Standby Mode	DSTB=1	2
6	Exit Deep Standby Mode	CSX × 6, HWRESET	3

- Note:
1. Before Turnaround operation, DBI Packet must be sent.
 2. DSTB must be sent by Escape mode in Sleep mode.
 3. After exiting from the Deep Standby Mode, all of commands are reset.

1) Power On, HWRESET → LP-11

The data lanes and clock lane should be in the LP-11 state during power-on, HWRESET, and soft_reset sequences.

2) Escape Mode

- Escape mode entry
- Mark-1 (exit Escape mode)

Table 21 Escape Entry Code

No.	Symbol	Escape Mode Action	Command Type	Entry Command Pattern (first bit transmitted to last bit transmitted)	R61529 implementation		Note
					LP-RX	LP-TX	
1	LPDT	Low Power Data Transmission	Mode	1110_0001	Yes	Yes	
2	ULPS	Ultra-Low Power State	Mode	0001_1110	Yes	No	
3	UDF1	Undefined-1	Mode	1001_1111	No	No	
4	UDF2	Undefined-2	Mode	1101_1110	No	No	
5	RAR	Remote Application Reset	Trigger	0110_0010	Yes	No	See note.
6	TER	TE-Report	Trigger	0101_1101	No	No	
7	ACKT	Unknown-4 (Acknowledge Trigger)	Trigger	0010_0001	No	Yes	
8	UNK5	Unknown-5	Trigger	1010_0000	No	No	

Note: DSI circuit is reset by Remote Application Reset.

3) Escape Mode (Host > Client): Low Power Data Transmission (LPDT)

An example of DSI read sequence by LPDT is shown below.

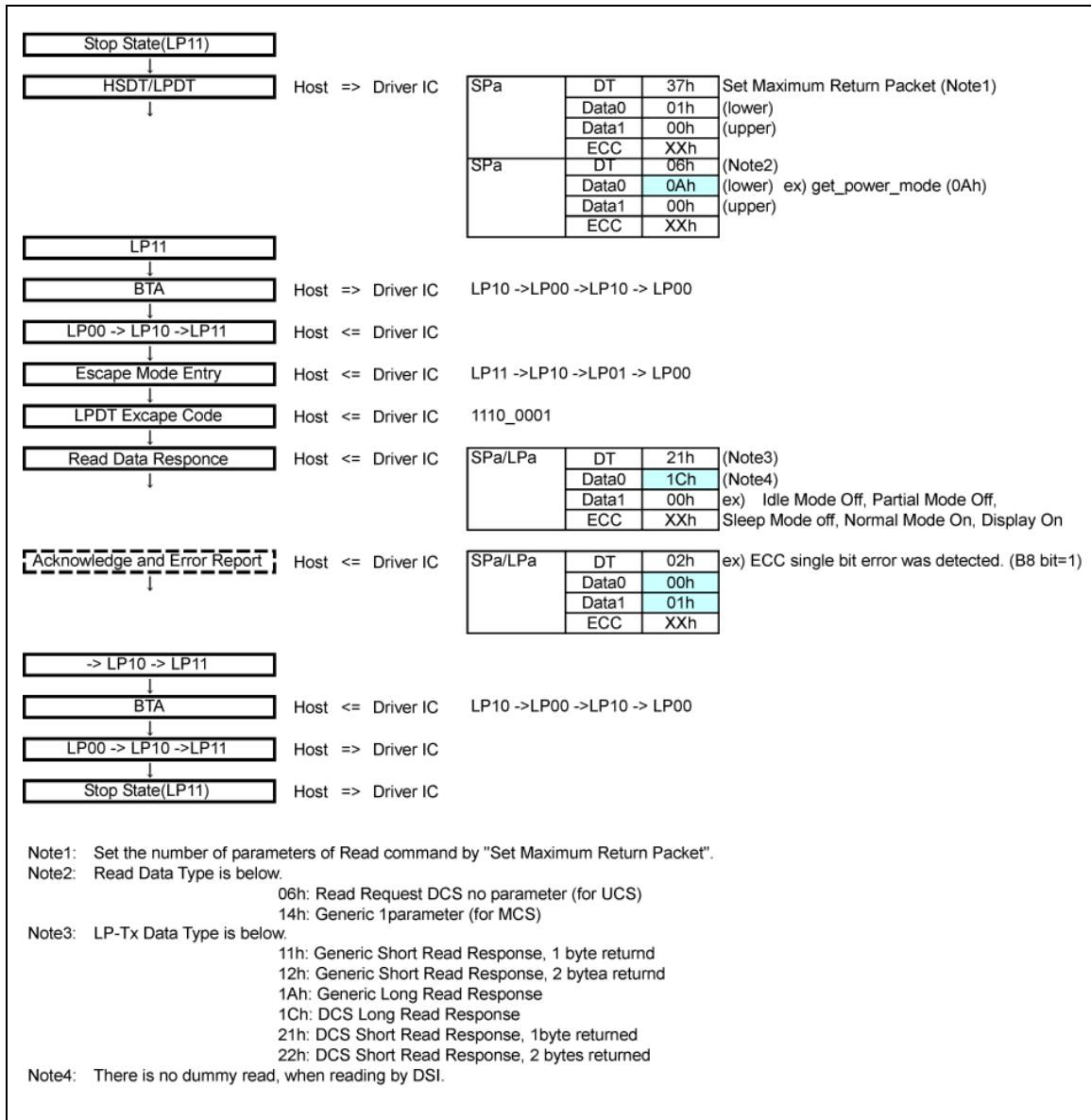


Figure 69

4) Escape Mode (Host > Client): Ultra Low Power State (ULPS)**5) Escape Mode (Host > Client): Remote Application Reset (RAR)****6) Escape mode (Client > Host): Tearing Report (TER)**

The R61529 supports TE Report function. Procedures are as follows:

Host to Client: send set_tear_on of DCS

Host to Client: send BTA

Client to Host: send Acknowledge Trigger

Client to Host: send BTA

Host: check Error Report

Host to Client: send BTA

Client to Host: send TE Report when TE occurred at the line of set_scan_line

Client to Host: send BTA

Host to Client: send image data by HST

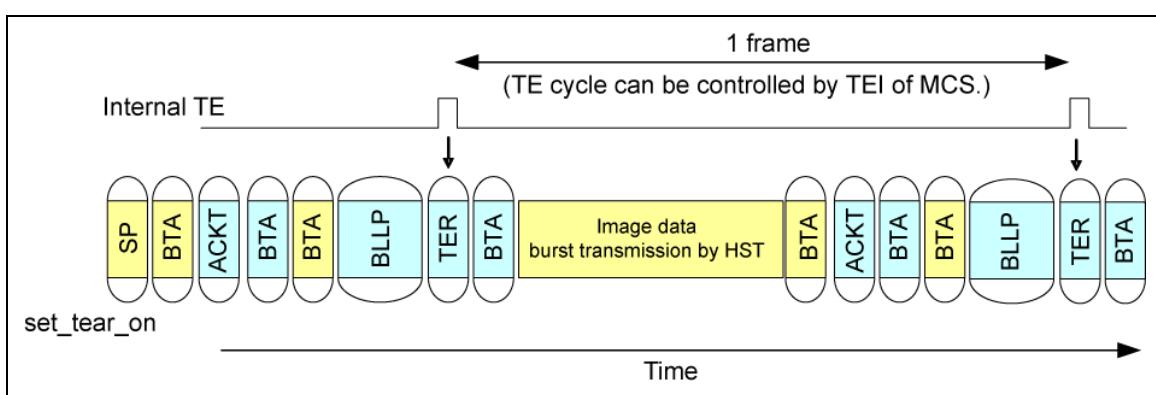


Figure 70

7) Escape Mode (Client > Host): Acknowledge Trigger (ACKT)**8) High Speed Data Transmission (HST)****9) Bus Turnaround (Host > Client) (BTA)****10) Bus Turnaround (Client > Host) (BTA)**

(6) Packet Level Communication

1) Short Packet (SPa) Structure

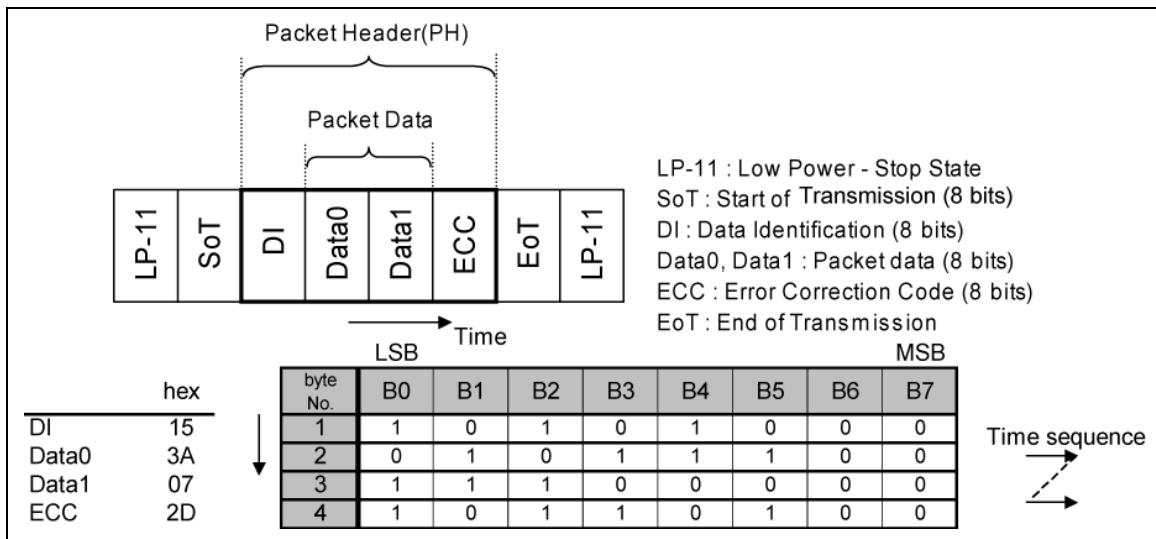
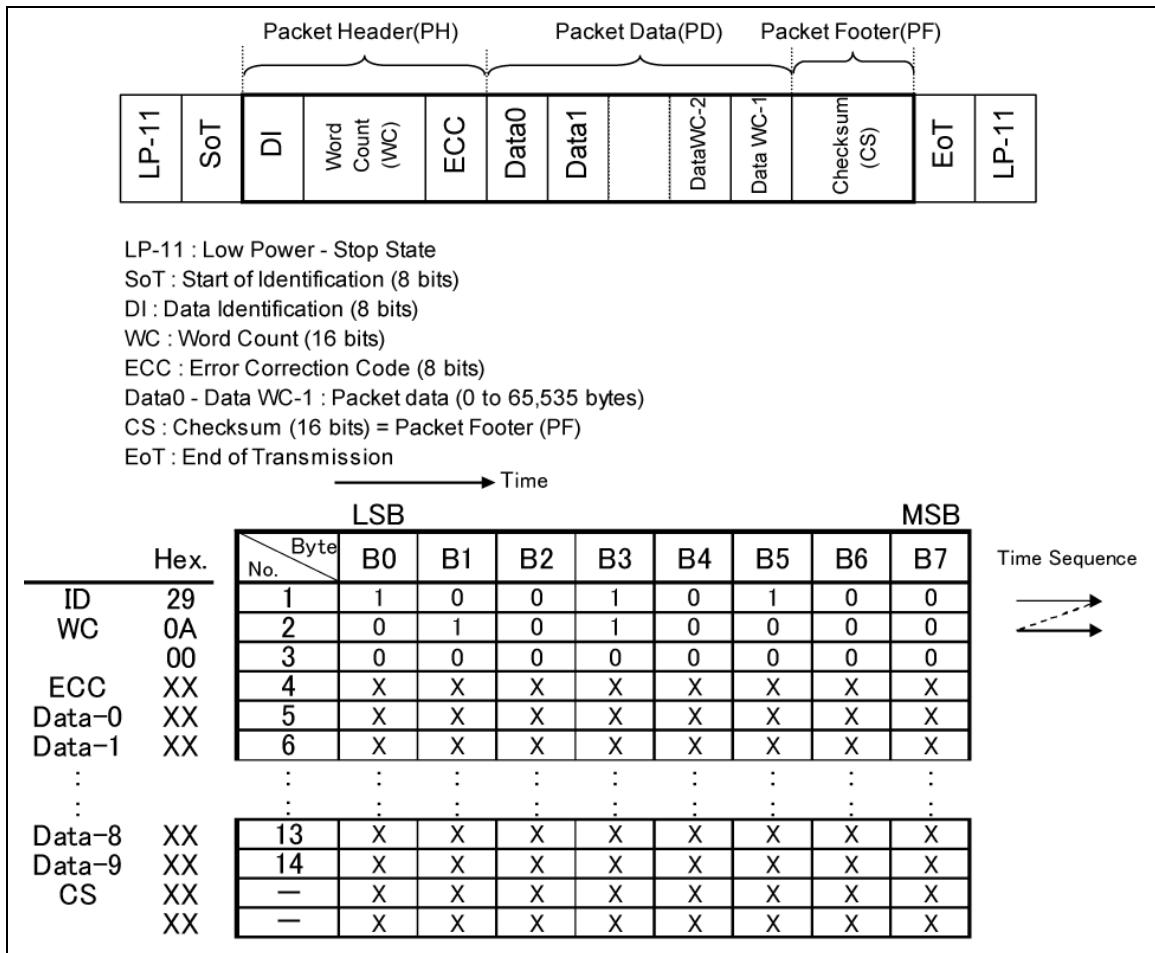


Figure 71 Example of Short Packet (SPa) (DCS WRITE, 1 Parameter)

2) Long Packet (LPa) Structure



3) Multiple Packet Sending

In LP-11 state, multiple Short Packets (SPa) and Long Packets (LPa) can be received between SoT and EoT.

LP-11 → SoT → SPa → SPa → EoT

LP-11 → SoT → SPa → LPa → EoT

LP-11 → SoT → LPa → LPa → EoT

LP-11 → SoT → LPa → SPa → EoT

LP-11 → SoT → Combination of the above methods → EoT

(7) Data Identification (DI)**1) Virtual Channel (VC)**

The R61529 supports Virtual Channel only when VC = 00. Set VC = 00 during packet transmission. If a packet is received when VC is other than 00, the packet is regarded as invalid. This result is reflected on an Error Report.

2) Data Type (DT)

If a Data Type undefined in the MIPI DSI specification is received, the subsequent data cannot be received. Transmit data again after checking that the R61529 is in LP-11 state by Error Report. If a Data Type unsupported in the R61529 is received, it is regarded as NOP, and the result is not reflected on the Error Report.

Table 22

Data Identification (DI)							
Virtual Channel (VC)		Data Type (DT)					
B7 (0)	B6 (0)	B5	B4	B3	B2	B1	B0

Table 23 R61529 Rx Data Type List

Data Type	Description	Packet size	DBI packet	DPI packet	R61529 (Rx) implementation	Note
01h	Sync Event, V Sync Start	Short		Yes	Yes	
11h	Sync Event, V Sync End	Short		Yes	No	5
21h	Sync Event, H Sync Start	Short		Yes	Yes	
31h	Sync Event, H Sync End	Short		Yes	No	5
08h	End of Transmission packet (EoT)	Short			Yes	4
02h	Color Mode (CM) Off Command	Short		Yes	No	
12h	Color Mode (CM) On Command	Short		Yes	No	
22h	Shut Down Peripheral Command	Short		Yes	Yes	7
32h	Turn On Peripheral Command	Short		Yes	Yes	7
03h	Generic Short WRITE, no parameters	Short	Yes		No	5
13h	Generic Short WRITE, 1 parameter	Short	Yes		Yes	1, 2
23h	Generic Short WRITE, 2 parameters	Short	Yes		Yes	1, 2
04h	Generic READ, no parameters	Short	Yes		No	5
14h	Generic READ, 1 parameter	Short	Yes		Yes	
24h	Generic READ, 2 parameters	Short	Yes		Yes	1, 2
05h	DCS WRITE, no parameters	Short	Yes		Yes	1, 2
15h	DCS WRITE, 1 parameter	Short	Yes		Yes	1, 2
06h	DCS READ, no parameters	Short	Yes		Yes	1, 2
37h	Set Maximum Return Packet Size (default 0001h)	Short	Yes		Yes	6
09h	Null Packet, no data	Long			Yes	
19h	Blanking Packet, no data	Long		Yes	Yes	
29h	Generic Long Write	Long	Yes		Yes	
39h	DCS Long Write/write_LUT Command Packet	Long	Yes		Yes	
0Eh	Packed Pixel Stream, 16-bit RGB, 5-6-5 Format	Long		Yes	No	3
1Eh	Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long		Yes	No	3
2Eh	Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long		Yes	Yes	3
3Eh	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format	Long		Yes	Yes	3
other	All unspecified codes are reserved	-	-	-	-	

Table 24 R61529 LP-Tx Data Type List

Data Type	Description	Packet size	R61529 (LP-Tx) implementation	Note
00h-01h	Reserved	—	—	
02h	Acknowledge with Error Report	Short	Yes	
03h-7h	Reserved	—	—	
08h	End of Transmission packet (EoT)	Short	No	
09h-10h	Reserved	—	—	
11h	Generic Short READ Response, 1 byte returned	Short	Yes	
12h	Generic Short READ Response, 2 bytes returned	Short	Yes	
13h-18h	Reserved	—	—	
1Ah	Generic Long READ Response	Long	Yes	
1Bh	Reserved	—	—	
1Ch	DCS Long READ Response	Long	Yes	
1Dh-20h	Reserved	—	—	
21h	DCS Short READ Response, 1 byte returned	Short	Yes	
22h	DCS Short READ Response, 2 bytes returned	Short	Yes	
23h-28h	Reserved	—	—	
29h-3Fh	Reserved	—	—	

- Notes:
1. Generic Command is Manufacturer Command.
DCS Command is User Command.
 2. Generic XXX 1 parameter is Manufacturer Command + 1 byte (all "0").
Generic XXX 2 parameter is Manufacturer Command + 1 parameter.
DCS XXX no parameter is User Command + 1 byte (all "0").
DCS XXX 1 parameter is User Command + 1 parameter.
 3. Line data (320RGB) must be sent by one packet.
 4. EoT packet (Data Type: 08h) is not defined in the MIPI Alliance Standard for Display Serial Interface Version 1.01.00 Release 11.
 5. Any packet with data type that MIPI Specification defines and the R61529 doesn't support is treated as NOP.
 6. When the host processor requests a response from the R61529, the R61529 returns the data of the same number as the maximum packet size. Default value of the maximum packet size is 000Fh (15 bytes). If the number of the valid data which the R61529 returns is less than the maximum packet size, the R61529 returns the valid data and "00h" as dummy data.
 7. Using Data Types 22h and 32h with 01h, 10h, 11h, 28h, or 29h command (DCS) is prohibited.

(8) Word Count (WC) on Long Packet (LPa)

Word Count (WC) = 2 bytes: The number of packet data on Long Packet (0 to 65,535 bytes)

(9) Error Correction Code (ECC)

ECC detects 1-bit errors or multiple-bit errors in each Packet Header. ECC is performed on the following:

- Short Packet: DI, Data0, Data1, and ECC
- Long Packet: DI, WC (2 bytes), and ECC

(10) Packet Footer on Long Packet (LPa)

In the Long Packet, Packet Footer is added after Packet Data. Packet footer includes CRC calculated from Packet Data as checksum.

- Checksum (2 bytes) = CRC (Packet Data): $CRC = X^{16} + X^{12} + X^5 + X^0$

(11) Video Mode

The R61529 supports Video Mode for moving pictures. There are three formats of transmission packet sequences. The R61529 supports two of these formats. See the following table.

Table 25

Transmission packet sequence in video mode	R61529 implementation
Non-burst mode with sync pulses	Not supported
Non-burst mode with sync events	Supported
Burst mode (Clock Lane/Data Lane)	Supported

1) Display Timing (Video Mode)

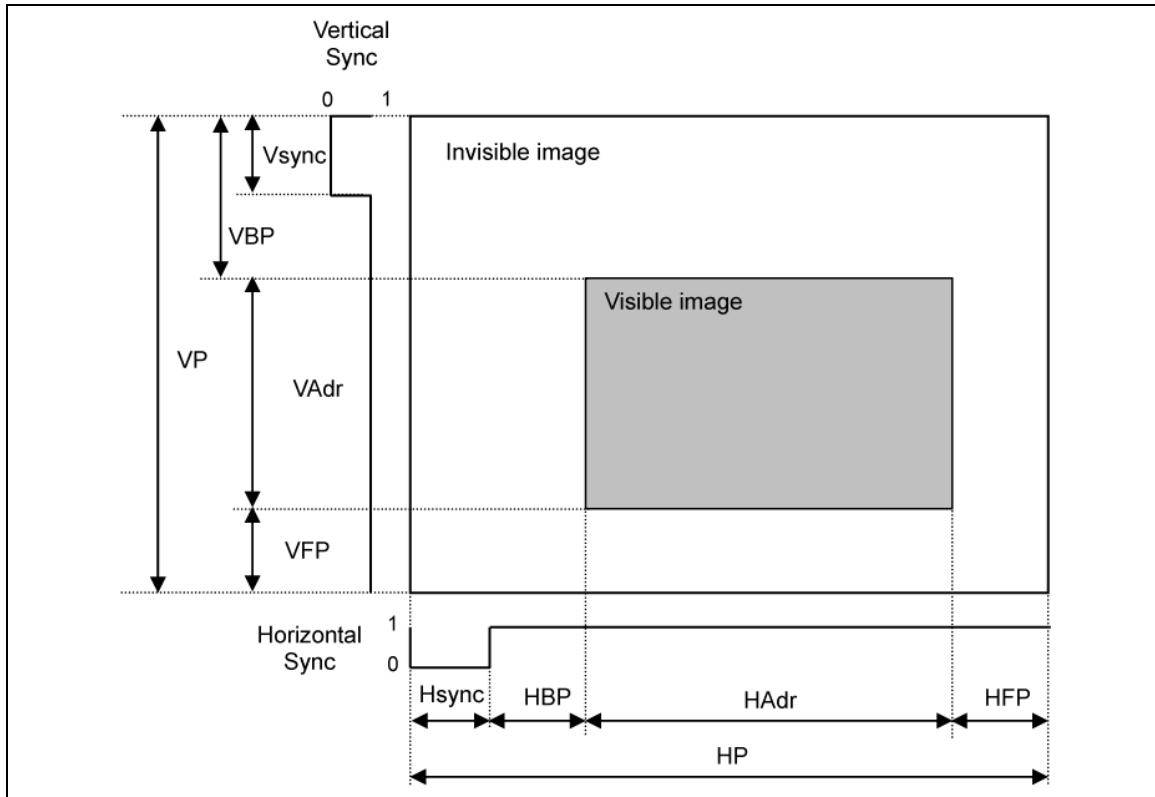


Figure 73

2) Vertical Display Timing (Video Mode)

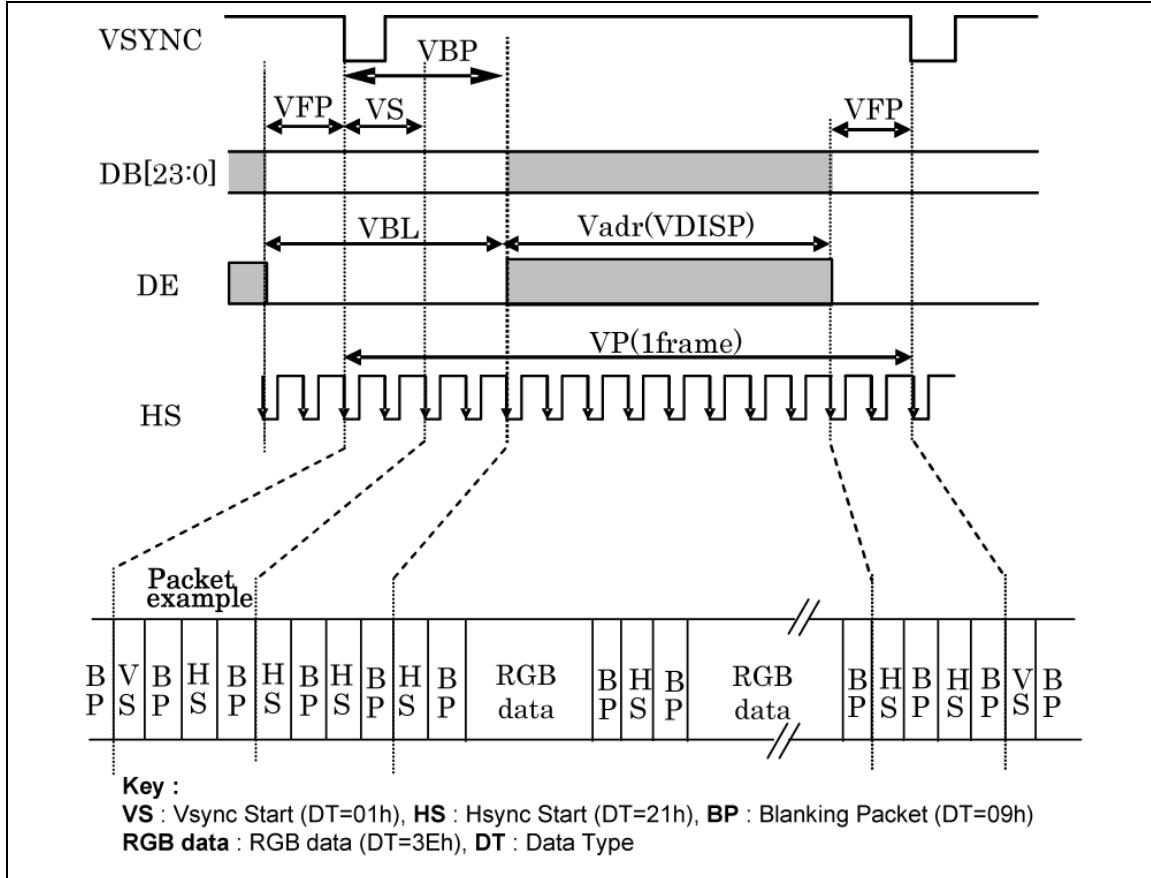


Figure 74

Table 26 Example of Vertical Display Timing Setting

Item	Symbol	Condition	Unit	Min.	Typ.	Max.	Notes
Vertical cycle	VP		Line	-	496	-	(1)
Vertical low pulse width	VS		Line	-	1	-	(1),(2)
Vertical front porch	VFP		Line	4	-	-	(1)
Vertical back porch	VBP		Line	4	-	-	(1),(2)
Vertical data start point	-	VBP	Line	4	-	-	(1)
Vertical blanking period	VBL	VBP+VFP	Line	8	-	-	(1)
Vertical active area	Vadr		Line	240	480	480	(1)

Notes: 1. [VBP, VFP, Vadr=NL] is set by C1h (Panel Driving Setting 2) command.

- The number of Hsync packet in 1 frame shall be the same as the total number of horizontal lines. Hsync packets shall be set during BP period.

3) Horizontal Display Timing (MIPI-DSI)

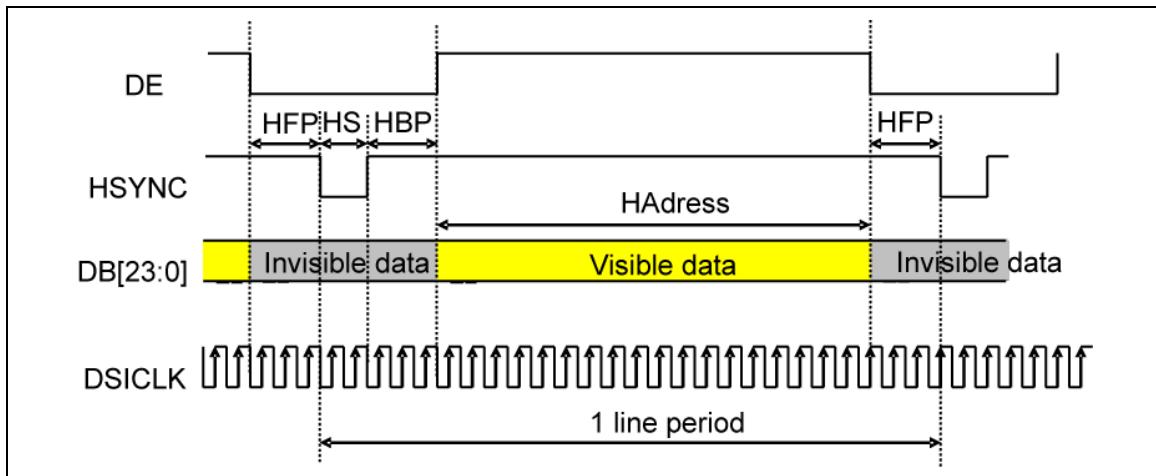


Figure 75

Table 27 Example of Horizontal Display Timing Setting

Item	Symbol	Condition	Unit	Min.	Typ.	Max.	Notes
Horizontal front porch	HFP		ByteClock	300	-	-	
Horizontal data start point	-	HS+HBP	ByteClock	3	-	-	
Horizontal active area	HAdr		Pixel	320	320	320	

Note: $f_{\text{ByteClock}} = (1/4)*f_{\text{DSICLK}}$. $f_{\text{ByteClock}}$ is the frequency of ByteClock. In video mode, DSICLK is high-speed clock.

4) Burst Transfer

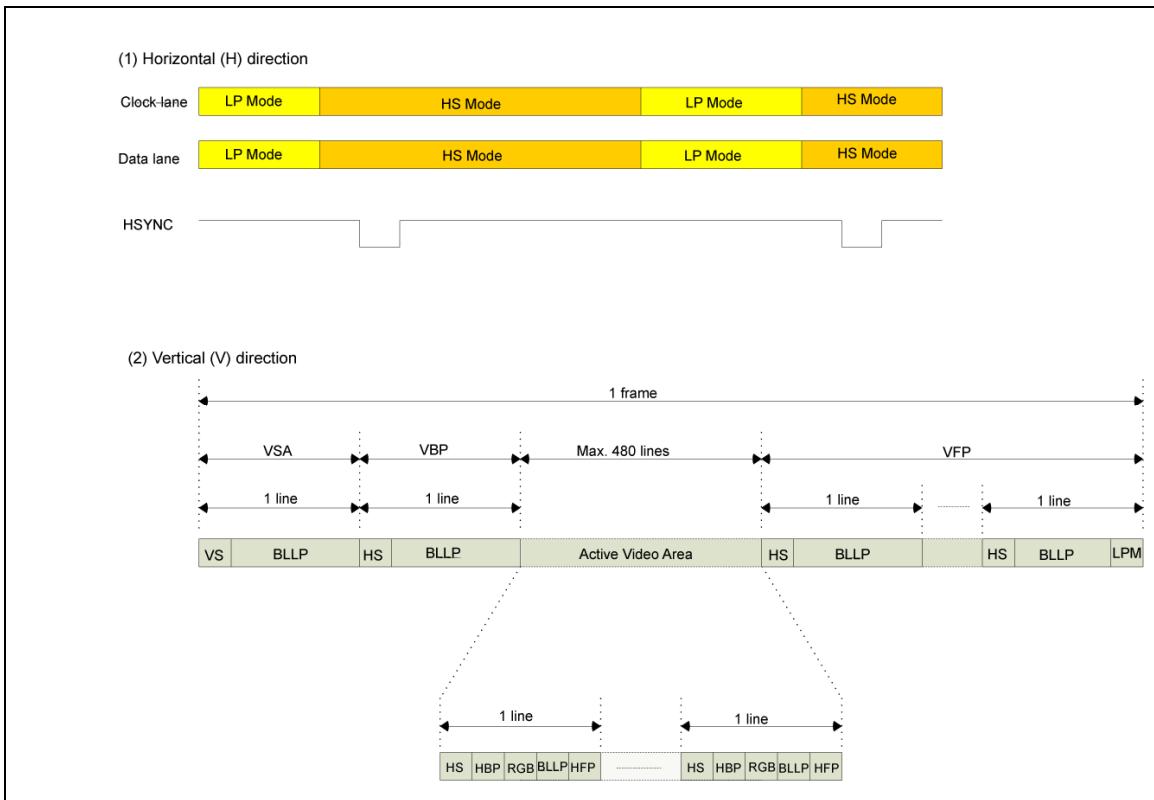


Figure 76

5) Packed Pixel Stream, 24-Bit Format, Long Packet, Data Type 11 1110 (3Eh)

Packet pixel stream of 24-bit format (packed) is a long packet. It is used to transmit image data formatted as 24-bit pixels to a display module in video mode. In this format, pixel boundaries are lined up with byte boundaries every three bytes.

This long packet shall be transmitted at a sufficient high rate (in HS mode) to avoid flickers or other visible artifacts.

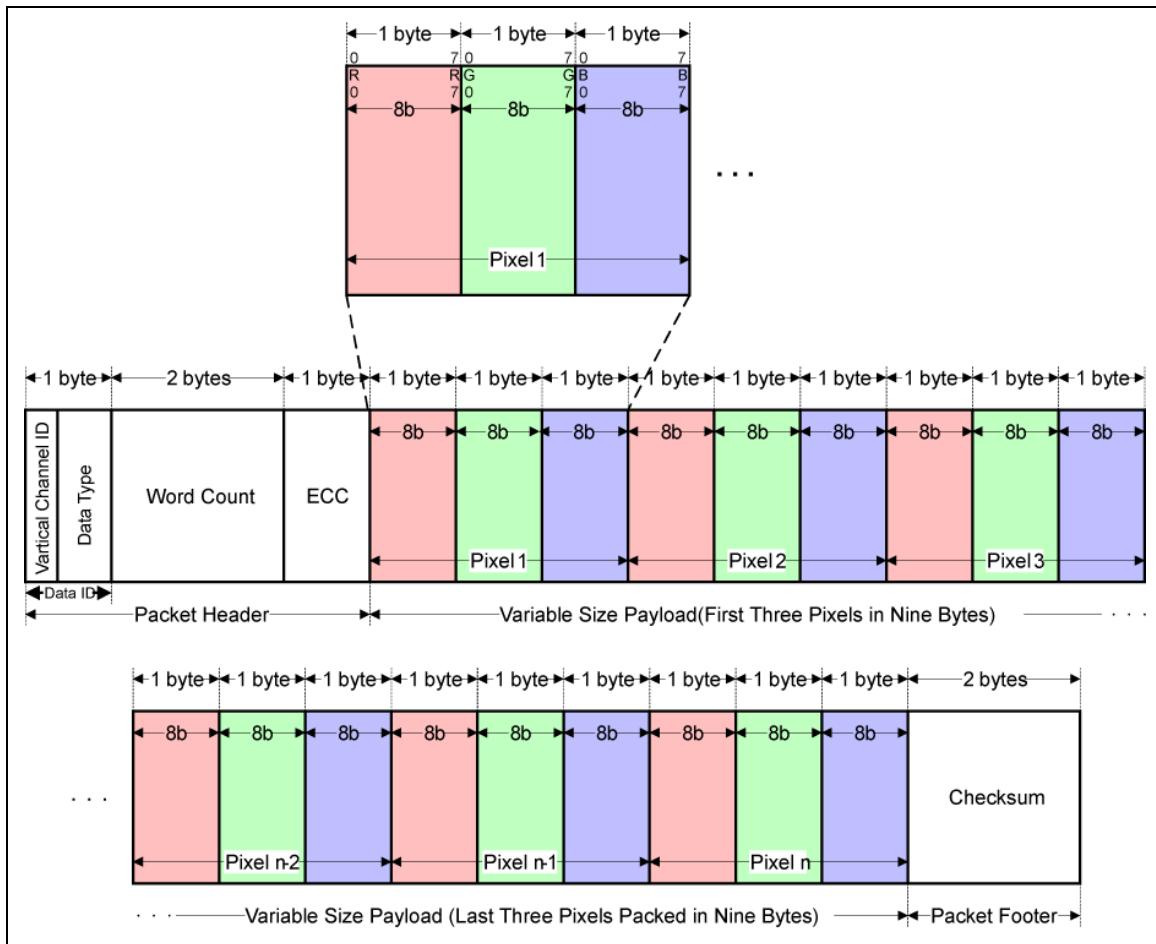


Figure 77 24bpp – RGB Color Format (Long Packet)

6) Pixel Stream, 18-Bit Format in Three Bytes, Long Packet, Data Type 10 1110 (2Eh)

Loosely packed pixel stream of 18-bit format is a long packet. It is used to transmit image data formatted as 18-bit pixels to a display module in video mode. In this format, pixel boundaries are lined up with byte boundaries every three bytes.

This long packet shall be transmitted at a sufficient high rate (in HS mode) to avoid flickers or other visible artifacts.

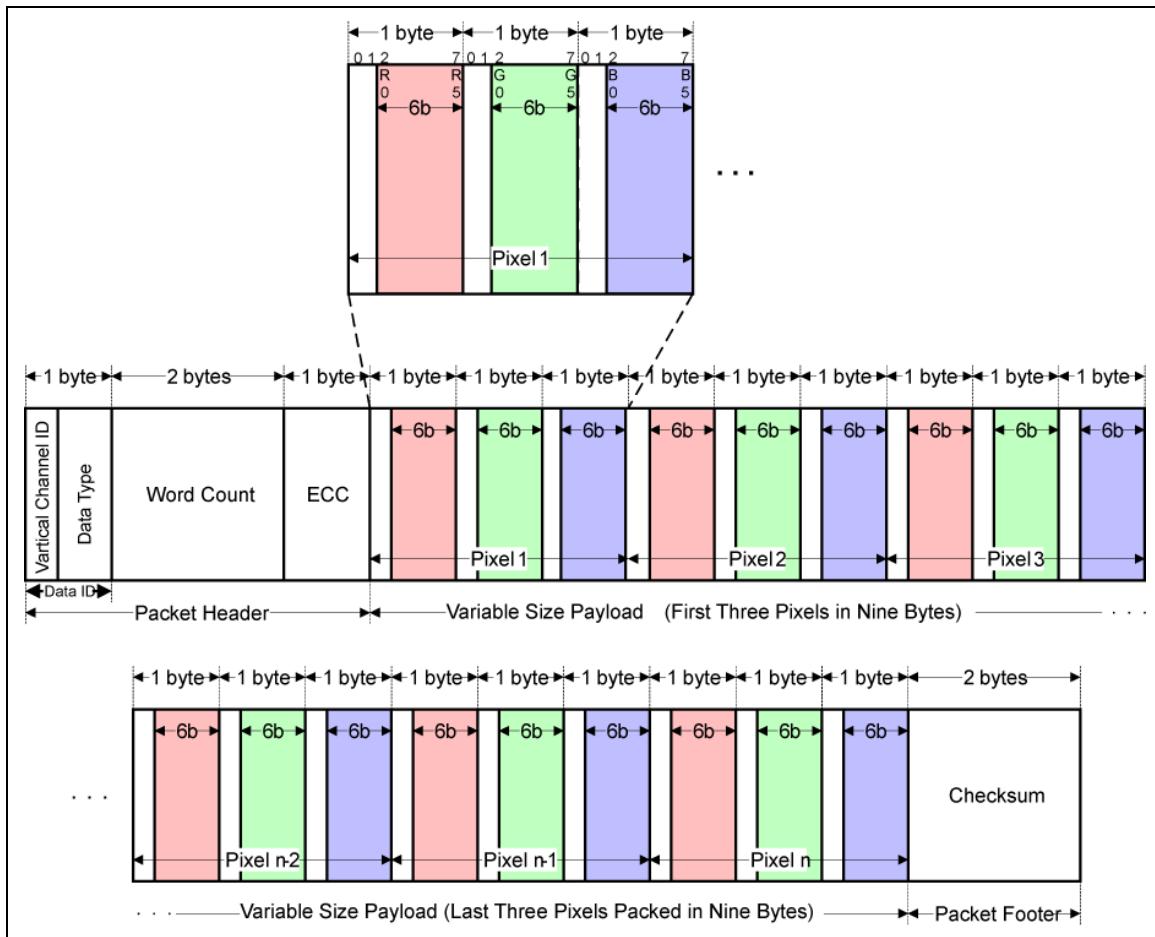


Figure 78 18bpp (Loosely Packed) – RGB Color Format (Long Packet)

7) Acknowledge with Error Report (AwER)

Table 28

Byte	Bit	Description	R61529 implementation	Note
Byte1 (Data0)	0	SoT Error	'0' fixed	No
	1	SoT Sync Error	'0' fixed	No
	2	EoT Sync Error	'0' fixed	No
	3	Escape Mode Entry Command Error	1: Error, 0: No Error	Yes
	4	Low-Power Transmit Sync Error	1: Error, 0: No Error	Yes
	5	HS Receive Timeout Error	'0' fixed	No
	6	False Control Error	'0' fixed	No
	7	Reserved	'0' fixed	-
Byte2 (Data1)	8	ECC Error, single-bit (detected, and corrected)	1: Error, 0: No Error	Yes
	9	ECC Error, multi-bit (detected, not corrected)	1: Error, 0: No Error	Yes
	10	Checksum Error (Long packet only)	1: Error, 0: No Error	Yes
	11	DSI Data Type Not Recognized	1: Error, 0: No Error	Yes
	12	DSI VC ID Invalid	1: Error, 0: No Error	Yes
	13	Invalid Transmission Length	'0' fixed	No
	14	Reserved	'0' fixed	-
	15	DSI Protocol Violation	'0' fixed	No

Note: Detailed error report condition is defined by R61529 (based on MIPI description).

8) DCS, MCS, and Data Type List

The following tables show available data type of each command (DCS and MCS).

Table 29 DCS and Data Type List

Command/Parameter		W/R	Host to R61529 Data Type (RX)									
			Write Type						Read Type			Other
		Data Type	05'h	15'h	39'h	13'h	23'h	29'h	14'h	24'h	06'h	37'h
		Packet	Short	Short	Long	Short	Short	Long	Short	Short	Short	Short
		DCS no para	DCS 1 para	DCS	Generic 1 para	Generic 2 para	Generic -	Generic 1 para	Generic 2 para	DCS no para	Set max. return packet size	
00h	nop	C	Yes	No	Yes	No	No	No	No	No	-	-
01h	soft_reset	C	Yes	No	Yes	No	No	No	No	No	No	-
04h	read_DDB_start	6	No	No	No	No	No	No	No	No	Yes	16'h6
0Ah	get_power_mode	1	No	No	No	No	No	No	No	No	Yes	16'h1
0Bh	get_address_mode	1	No	No	No	No	No	No	No	No	Yes	16'h1
0Ch	get_pixel_format	1	No	No	No	No	No	No	No	No	Yes	16'h1
0Dh	get_display_mode	1	No	No	No	No	No	No	No	No	Yes	16'h1
0Eh	get_signal_mode	1	No	No	No	No	No	No	No	No	Yes	16'h1
0Fh	get_diagnostic_mode	1	No	No	No	No	No	No	No	No	Yes	16'h1
10h	enter_sleep_mode	C	Yes	No	Yes	No	No	No	No	No	No	-
11h	exit_sleep_mode	C	Yes	No	Yes	No	No	No	No	No	No	-
12h	enter_partial_mode	C	Yes	No	Yes	No	No	No	No	No	No	-
13h	enter_normal_mode		Yes	No	Yes	No	No	No	No	No	No	-
20h	exit_invert_mode	C	Yes	No	Yes	No	No	No	No	No	No	-
21h	enter_invert_mode	C	Yes	No	Yes	No	No	No	No	No	No	-
28h	set_display_off	C	Yes	No	Yes	No	No	No	No	No	No	-
29h	set_display_on	C	Yes	No	Yes	No	No	No	No	No	No	-
2Ah	set_column_address	4	No	No	Yes	No	No	No	No	No	No	16'h4
2Bh	set_page_address	4	No	No	Yes	No	No	No	No	No	No	16'h4
2Ch	write_memory_start	N	No	No	Yes	No	No	No	No	No	No	N byte
2Eh	read_memory_start	N	No	No	No	No	No	No	No	No	Yes	N byte

Note: When each data type packet is sent, it is necessary to write all parameters of each DCS and MCS.

Table 30 DCS and Data Type List (continued)

DCS Command/Parameter		W/R	Host to R61529 Data Type (RX)									
			Write Type						Read Type			Other
		Data Type	05'h	15'h	39'h	13'h	23'h	29'h	14'h	24'h	06'h	37'h
		Packet	Short	Short	Long	Short	Short	Long	Short	Short	Short	Short
		DCS no para	DCS 1 para	DCS	Generic 1 para	Generic 2 para	Generic -	Generic 1 para	Generic 2 para	DCS no para	Set max. return packet size	
30h	set_partial_area	4	No	No	Yes	No	No	No	No	No	No	16'h4
34h	set_tear_off	C	Yes	No	Yes	No	No	No	No	No	No	-
35h	set_tear_on (type 1)	1	No	Yes	Yes	No	No	No	No	No	No	16'h1
36h	set_address_mode	1	No	Yes	Yes	No	No	No	No	No	No	16'h1
38h	exit_idle_mode	C	Yes	No	Yes	No	No	No	No	No	No	-
39h	enter_idle_mode	C	Yes	No	Yes	No	No	No	No	No	No	-
3Ah	set_pixel_format	1	No	Yes	Yes	No	No	No	No	No	No	16'h1
3Ch	write_memory_continue	N	No	No	Yes	No	No	No	No	No	No	N byte
3Eh	read_memory_continue	N	No	No	No	No	No	No	No	No	Yes	N byte
44h	set_tear_scanline	2	No	Yes	Yes	No	No	No	No	No	No	16'h2
45h	get_scanline	2	No	No	No	No	No	No	No	No	Yes	16'h2
A1h	read_DDB_start	6	No	No	No	No	No	No	No	No	Yes	16'h6

Note: When each data type packet is sent, it is necessary to write all parameters of each DCS and MCS.

Table 31 MCS and Data Type List (TBD)

MCS Command / Parameter		W/R	HOST→R61529 Data Type(RX)									
			Write Type						Read Type			
		Data Type	05'h	15'h	39'h	13'h	23'h	29'h	14'h	24'h	06'h	
		Packet	Short	Short	Long	Short	Short	Long	Short	Short	Short	
			DCS no para	DCS 1 para	DCS -	Generic 1 para	Generic 2 para	Generic -	Generic 1 para	Generic 2 para	DCS no para	set maximum return packet
B0h	Manufacturer Command Access Protect	1	No	No	No	No	Yes	Yes	Yes	No	No	16'h1
B1h	Low Power Mode Control	1	No	No	No	No	Yes	Yes	Yes	No	No	16'h1
B3h	Frame Memory Access and Interface Setting	4	No	No	No	No	No	Yes	Yes	No	No	16'h4
B4h	Display Mode	1	No	No	No	No	Yes	Yes	Yes	No	No	16'h1
B5h	Read Checksum and ECC Error Count	3	No	No	No	No	No	No	Yes	No	No	16'h3
B6h	DSI Control	2	No	No	No	No	No	Yes	Yes	No	No	16'h2
B7h	MDDI Control	4	No	No	No	No	No	Yes	Yes	No	No	16'h4
B8h	Backlight Control (1)	20	No	No	No	No	No	Yes	Yes	No	No	16'h14
B9h	Backlight Control (2)	4	No	No	No	No	No	Yes	Yes	No	No	16'h4
BAh	Backlight Control (3)	1	No	No	No	No	No	No	Yes	No	No	16'h1
BFh	Device Code Read	5	No	No	No	No	No	No	Yes	No	No	16'h5
C0h	Panel Driving Setting	8	No	No	No	No	No	Yes	Yes	No	No	16'h8
C1h	Display Timing Setting for Normal Mode	5	No	No	No	No	No	Yes	Yes	No	No	16'h5
C3h	Test Mode 1	1	No	No	No	No	No	Yes	Yes	No	No	16'h1
C4h	Source / Gate Driving Timing Setting	4	No	No	No	No	No	Yes	Yes	No	No	16'h4
C6h	DPI polarity Control	1	No	No	No	No	Yes	Yes	Yes	No	No	16'h1
C7h	Test Mode 2	2	No	No	No	No	No	Yes	Yes	No	No	16'h2
C8h	Gamma Setting A Set	24	No	No	No	No	No	Yes	Yes	No	No	16'h18
C9h	Gamma Setting B Set	24	No	No	No	No	No	Yes	Yes	No	No	16'h18
CAh	Gamma Setting C Set	24	No	No	No	No	No	Yes	Yes	No	No	16'h18
CCh	Test Mode 3	1	No	No	No	No	Yes	Yes	Yes	No	No	16'h1
D0h	Power Setting (Charge Pump Setting)	16	No	No	No	No	No	Yes	Yes	No	No	16'h10
D1h	VCOM Setting	4	No	No	No	No	No	Yes	Yes	No	No	16'h4

Table 32 MCS and Data Type List (TBD) (continued)

MCS Command / Parameter		W/R	HOST→R61529 Data Type(RX)									
			Write Type						Read Type			
		Data Type	05'h	15'h	39'h	13'h	23'h	29'h	14'h	24'h	06'h	
		Packet	Short	Short	Long	Short	Short	Long	Short	Short	Short	
			DCS no para	DCS 1 para	DCS -	Generic 1 para	Generic 2 para	Generic -	Generic 1 para	Generic 2 para	DCS no para	set maximum return packet
D6h	Test Mode 4	1	No	No	No	No	Yes	Yes	Yes	No	No	16'h1
D7h	Test Mode 5	15	No	No	No	No	No	Yes	Yes	No	No	16'hF
D8h	Test Mode 6	9	No	No	No	No	No	Yes	Yes	No	No	16'h9
D9h	Test Mode 7	3	No	No	No	No	No	Yes	Yes	No	No	16'h3
DAh	Test Mode 8	1	No	No	No	No	Yes	Yes	Yes	No	No	16'h1
E0h	NVM Access Control	4	No	No	No	No	No	Yes	Yes	No	No	16'h4
E1h	set_DDB_write_control	6	No	No	No	No	No	Yes	Yes	No	No	16'h6
E2h	NVM Load Control	1	No	No	No	No	Yes	Yes	Yes	No	No	16'h1
E4h	Test Mode 9	5	No	No	No	No	No	Yes	Yes	No	No	16'h5
E5h	Test Mode 10	1	No	No	No	No	Yes	Yes	Yes	No	No	16'h1
E6h	Test Mode 11	1	No	No	No	No	Yes	Yes	Yes	No	No	16'h1
E7h	Test Mode 12	5	No	No	No	No	No	Yes	Yes	No	No	16'h5
F3h	Test Mode 13	5	No	No	No	No	No	Yes	Yes	No	No	16'h5
F5h	Read Mode In for DBI only	0	No	No	No	No	No	No	No	No	No	-
F6h	Read Mode Out for DBI only	0	No	No	No	No	No	No	No	No	No	-
F8h	Test Mode 14	1	No	No	No	No	Yes	Yes	Yes	No	No	16'h1
FAh	Test Mode 15	1	No	No	No	No	Yes	Yes	Yes	No	No	16'h1
FCh	Test Mode 16	5	No	No	No	No	No	Yes	Yes	No	No	16'h5
FDh	Test Mode 17	13	No	No	No	No	No	Yes	Yes	No	No	16'hD
FEh	Test Mode 18	8	No	No	No	No	No	Yes	Yes	No	No	16'h8

9) DSI Data Format

The R61529 supports color formats shown below.

Table 33

Type	IM3-0	Data pin	Color format	R61529 implementation	
				Command Mode	Video Mode
DSI	0011, 1011	DATA0P,DATA0N	16bpp	Yes	No
			18bpp (Loosely packed)	Yes	Yes
			18bpp (Packed)	Yes	No
			24bpp	Yes	Yes

Yes: Supported

No: Unsupported

MDDI (Mobile Display Digital Interface)

MDDI (Mobile Display Digital Interface) is a differential small amplitude serial interface for high-speed data transfer via Stb+/- (STB_CLKP and STB_CLKN) and Data0+/- (DATA0P and DATA0N). High-speed data can be also transferred via only by Stb+/- and Data0+/. The specifications of MDDI supported by the R61529 are compatible to the MDDI specifications disclosed by VESA, Video Electronics Standards Association. The following are the specifications particular to the R61529's MDDI. See the MDDI specifications by VESA for details on the MDDI Link Protocol.

R61529's MDDI Specifications

- MDDI Type 1 (1 data lane)
- High-speed, differential, small-amplitude data transfer via Stb+/- and Data0+/- lines
- MDDI client: the R61529 enables direct connection to the base band (BB) chip without bridge chip
- Active Refresh Mode
 - Video data received via MDDI is directly output as display data without being written to internal RAM.
- Cost-performance optimized interface for mobile display systems
 1. Internal mode (one client), Forward Link (Type 1), and Reverse Link (Type 1) are supported
 2. Hibernation mode to save power consumption
 3. Tearing-free moving picture display via TE interface
 4. Moving picture display with low power consumption, realized by the features 2 and 3
 5. Shutdown mode for saving power consumption in the standby state
 6. Providing one-chip solution for MDDI mobile display systems

Note: In the specification for MDDI, shutdown refers to DSTB (deep standby mode).

- B5 of set_address_mode command (36h): Setting to only 0 (horizontal direction) is supported
- RAM window address setting
 - set_column_address (2Ah)
 - SC[9:0] = 2n (n = 0, 1, 2, ...159)
 - EC[9:0] = 2m - 1 (m = 1, 2, ...160)
 - EC - SC > 2 pixels

Example of MDDI Connection of the R61529

The R61529 incorporates terminal resistors for differential input pins (DATA0P, DATA0N, STB_CLKP, and STB_CLKN).

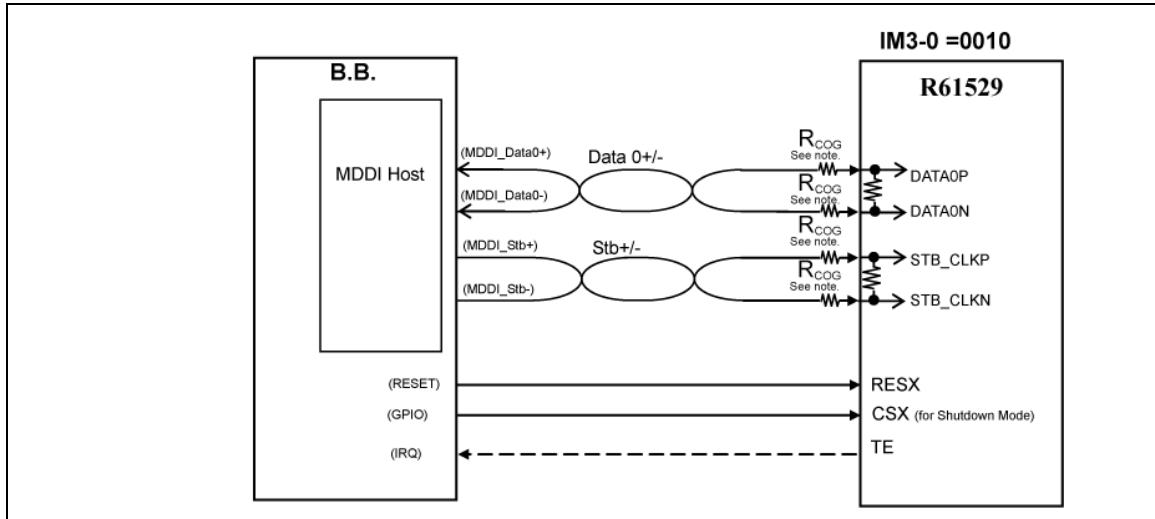


Figure 79

Note: Make the COG wiring resistances of Data0+/-, and Stb+/- lines as small as possible ($R_{COG} < 10$ ohm).

MDDI Link Protocol (Packets Supported by the R61529)

The MDDI packets supported by the R61529 are as follows. Do not send packets not supported by the R61529 in the system incorporating the R61529.

- Sub-Frame Header Packet
- Filler Packet
- Reverse Link Encapsulation Packet
- Link Shutdown Packet
- Perform Type Handoff Packet
- Round-Trip Delay Measurement Packet
- Forward Link Skew Calibration Packet
- Video Stream Packet
- Windowless Video Stream Packet
- Client Capability Packet
- Client Request and Status Packet
- Register Access Packet

Sub-Frame Header Packet

The Sub-Frame Header Packet is the first packet of every sub-frame. The Sub-Frame Header Packet is required for host-client synchronization.

	0	1	2	3	4	5	6	7			
1	Packet Length (0x14)								2 bytes	←	Specifies the number of bytes in the packet not including the packet length field.
2	Packet Type (0x3bff)								2 bytes	←	Specifies the format of this packet.
3	Unique Word (0x5a)								2 bytes	←	Specifies 32-bit Unique Word by the combination of Packet Type and Unique Word.
4	Reserved 1 (0x00)								2 bytes	←	Reserved for future use. Must be set to 0x00.
5	Sub-frame Length								4 bytes	←	Specifies the number of bytes per sub-frame.
6											
7											
8											
9											
10											
11											
12											
13	Protocol Version								2 bytes	←	Specifies the protocol version used by the host.
14											
15	Sub-frame Count								2 bytes	←	Specifies the number of sub-frames that have been transmitted. (0 ~ +1)
16											
17	Media-frame Count								4 bytes	←	
18											Specifies the number of media-frames that have been transmitted. (0 ~ +1)
19											
20											
21	CRC								2 bytes	←	CRC. Used to detect errors.
22											

Figure 80 Sub-Frame Header Packet

Protocol Version[15:0]

[15:2] – Reserved for future use. These must be set to 0x0.

[1:0] – Specifies sub-frame length

00 – Sub-frame lengths are fixed (not flexible). Packet longer than a sub-frame boundary cannot be sent.
Split large data to be sent into packets at the Sub-Frame Header Packet boundary.

01 – Sub-frame lengths are flexible. Sub-frame length specified by Sub-Frame Header Packet is enabled.
Packet longer than a sub-frame boundary cannot be sent. Adjust the next sub-frame length so that an average length is a target sub-frame length.

10 – Sub-frame length is unlimited. No more Sub-Frame Header Packets are required to be transmitted following the first Sub-Frame Header Packet after an exit from a hibernation state (length = 0).

Filler Packet

The Filler Packet is sent when no other information is available to be sent on the forward or reverse link. It is recommended to send Filler Packets with minimum length to allow maximum flexibility to send other packets when required.

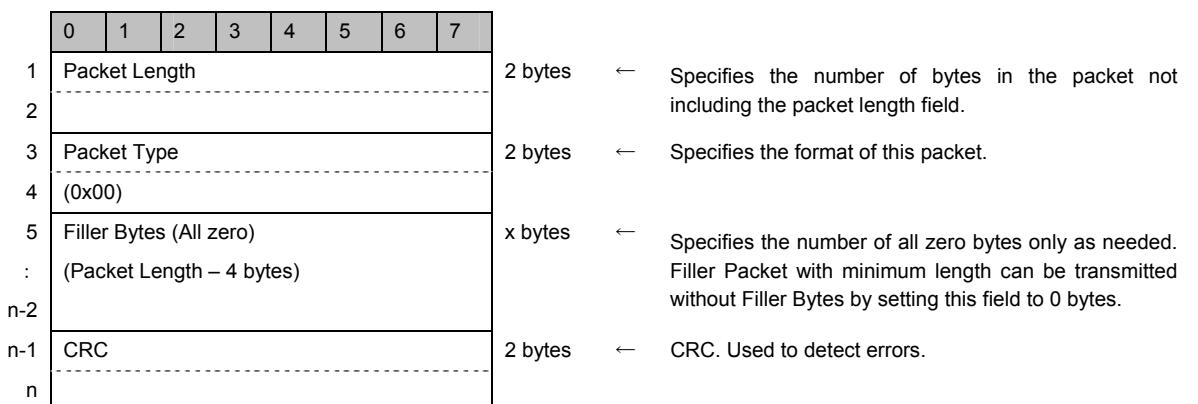


Figure 81 Filler Packet

Link Shutdown Packet

The Link Shutdown Packet is sent from the host to the client to indicate that the MDDI data and strobe will be shut down and go into a hibernation state. Normal operation is resumed when the link is restarted and the host sends packets to the client that is in a hibernation state.

	0	1	2	3	4	5	6	7	
1	Packet Length								2 bytes ← Specifies the number of bytes in the packet not including the packet length field.
2	(0x14)								
3	Packet Type								2 bytes ← Specifies the format of this packet.
4	(0x45)								
5	CRC								2 bytes ← Used to detect byte errors in the Packet Length to the Client ID.
6									
7	All zero								16 bytes ← Data bytes equal to zero.
:	(0x00)								
22									

Figure 82 Link Shutdown Packet

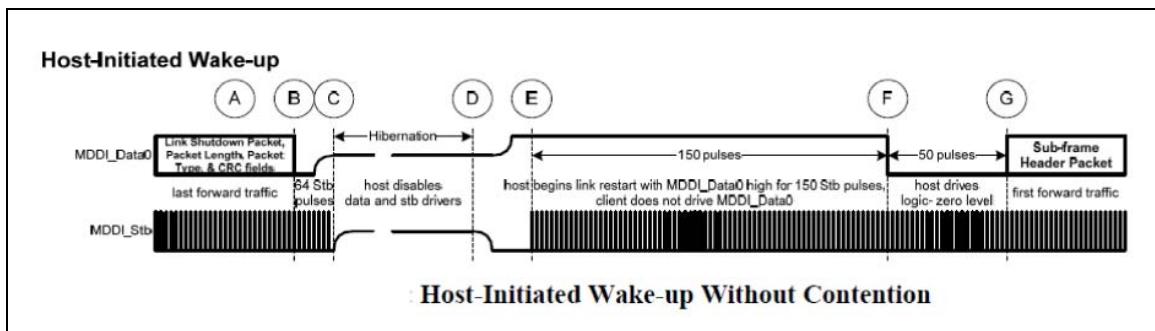


Figure 83

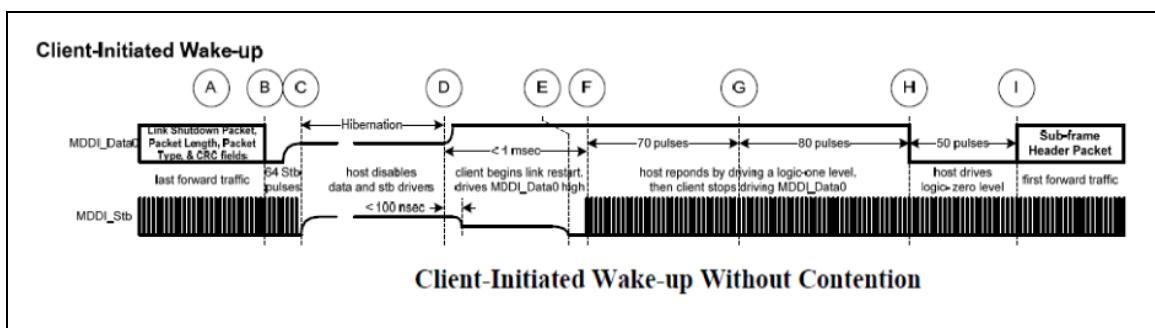


Figure 84

Round-Trip Delay Measurement Packet

The Round-Trip Delay Measurement Packet is used to measure the propagation delay from the host to the client plus the delay from the client back to the host. This measurement inherently includes all of the delays that exist in the line drivers and receivers and the interconnect subsystem. This measurement is used to set the turnaround delay and reverse link rate divisor parameters in the Reverse Link Encapsulation Packet.

	0	1	2	3	4	5	6	7	
1	Packet Length								2 bytes ← Specifies the number of bytes in the packet not including the packet length field.
2	(0xC8)								
3	Packet Type								2 bytes ← Specifies the format of this packet.
4	(0x52)								
5	hClient ID								2 bytes ← Reserved for the Client ID. Must be set to 0x00.
6	(0x00)								
7	Parameter CRC								2 bytes ← Used to detect byte errors in the Packet Length to the Client ID.
8									
9	Guard Time 1								64bytes
:									
72									
73	Measurement Period								64bytes ← Identifies the round trip delay of the link plus logic delay after the first bit of Measurement Period.
:									
136									
137	All Zero								2 bytes ← Enables MDDI_Data Line Drivers during bit 0 of the All Zero field.
138	(0x00)								
139	Guard Time 2								64bytes
:									
202									

Figure 85 Round-Trip Delay Measurement Packet

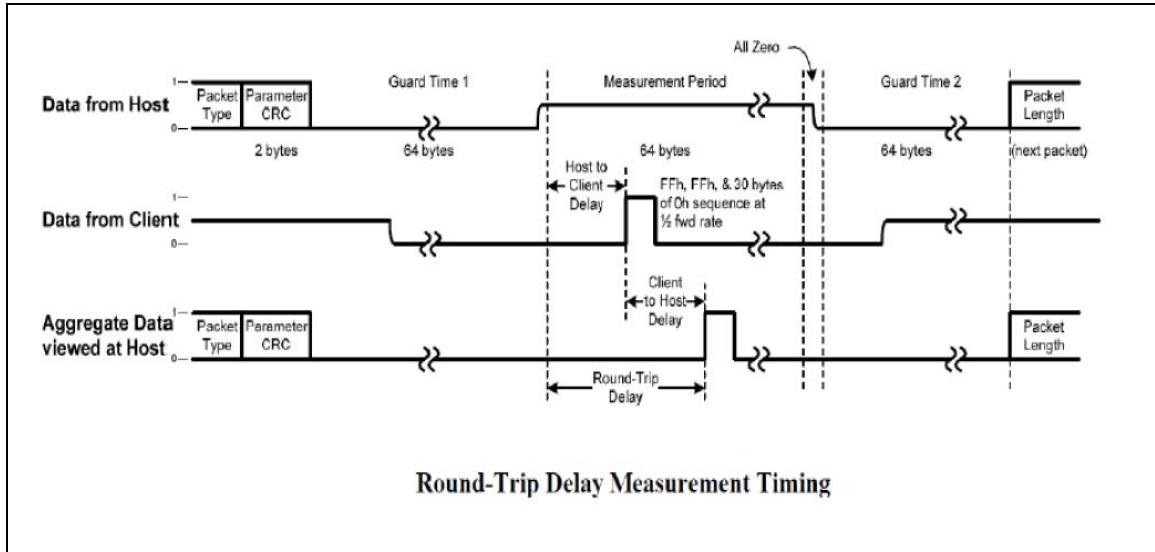


Figure 86

Forward Link Skew Calibration Packet

This packet allows the client to calibrate itself for differences in the propagation delay of the MDDI_Data signals with respect to the MDDI_Stb signal.

Figure 87 Forward Link Skew Calibration Packet

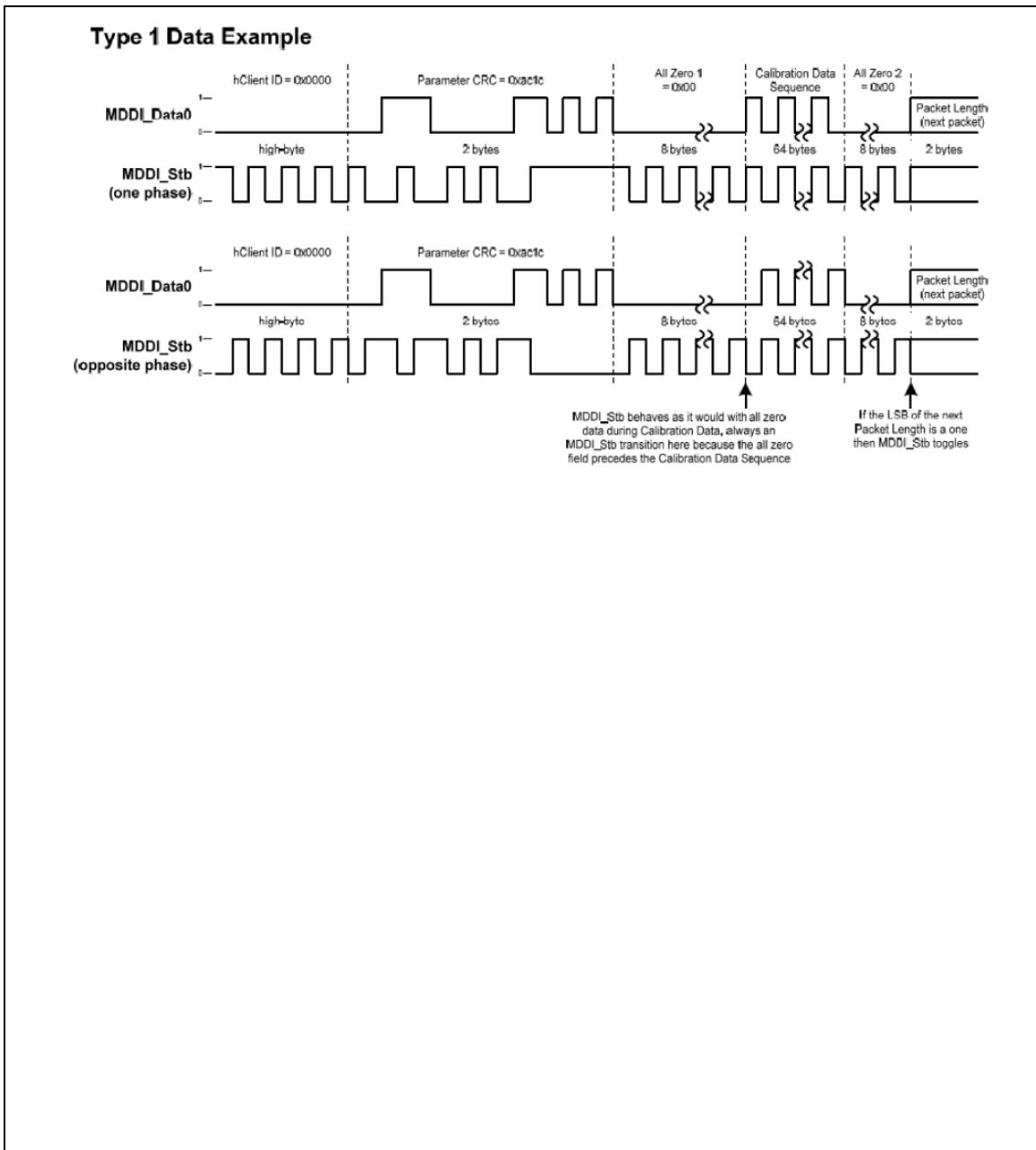


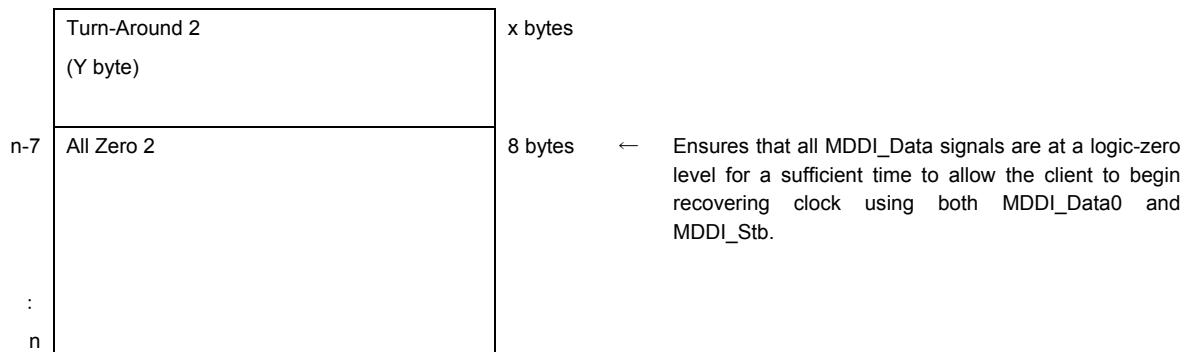
Figure 88

Reverse Link Encapsulation Packet

Data is transferred in the reverse direction using the Reverse Link Encapsulation Packet. When a forward link packet is sent, MDDI link is turned around in the middle of this packet so that packets can be sent in the reverse direction.

	0	1	2	3	4	5	6	7		
1	Packet Length								2 bytes	← Specifies the number of bytes in the packet not including the packet length field.
2										
3	Packet Type								2 bytes	← Specifies the format of this packet.
4	(0x41)									
5	hClient ID								2 bytes	← Reserved for the Client ID. Must be set to 0x00.
6	(0x00)									
7	Reverse Link Flags								1 byte	← Specifies kinds of data output to the Reverse Link Data Packets field.
8	Reverse Rate Divisor								1 byte	← Specifies Reverse Link Data transfer rate.
9	Turn-Around 1 Length								1 byte	← Specifies the total number of bytes that are allocated for Turn-Around 1 (X).
10	Turn-Around 2 Length								1 byte	← Specifies the total number of bytes that are allocated for Turn-Around 2 (Y).
11	Parameter CRC								2 bytes	← Used to detect byte errors in the Packet Length to the Turn-Around 2.
12										
13	All Zero 1								8 bytes	← Ensures that all MDDI_Data signals are at a logic-zero level for a sufficient time to allow the client to begin recovering clock using only MDDI_Stb.
14										
15										
16										
17										
18										
19										
20										
	Turn-Around 1 (X byte)								x bytes	← First turnaround period. The number of bytes specified by the Turn-Around 1 Length parameter is allocated to allow the MDDI_Data line drivers in the client to enable before the line drivers in the host are disabled.
	Reverse Data Packets (Packet Length - X - Y - 26 bytes)								x bytes	← A series of data packets transferred from the client to host. The client sends Filler Packets as if it drove MDDI_Data lines at a logic-zero level when it has no data to send to the host.

Figure 89 Reverse Link Encapsulation Packet

**Figure 90 Reverse Link Encapsulation Packet (continued)****Reverse Link Flags[7:0]**

[7:2]: Reserved for future use. These must be set to 0x0.

[1:0]: The host requests the client to transfer the Client Request and Status Packet or the Client Capability Packet in the Reverse Data Packets Field.

00: Register Read Response

01: Client Capability Packet (+ Register Read Response)

10: (Register Read response +) Client Request and Status Packet

11: Client Capability Packet (+ Register Read Response) + Client Request and Status Packet

If request to read Register Access Packet and this Reverse Link Encapsulation Packet requests Client Capability Packet or Client Request Status Packet, Client Capability Packet, Register Access Packet, and Client Request and Status Packet are read in that order.

Reverse Rate Divisor[7:0]

Specifies the number of MDDI_Stb cycles per Reverse Link Data Clock. The R61529 supports the following setting values.

[7:0]

8'h02: Reverse Data Rate / 2 (Forward Link Data Rate / 4)

8'h04: Reverse Data Rate / 4 (Forward Link Data Rate / 8)

8'h08: Reverse Data Rate / 8 (Forward Link Data Rate / 16)

8'h10: Reverse Data Rate / 16 (Forward Link Data Rate / 32)

Unlike Forward Link, Reverse Link Data Clock operates at Single Data Rate (SDR: used only on a rising edge). Reverse Link Data Clock is two times as many as Reverse Rate Divisor[7:0]. Reverse Link Data Rate depends on Reverse Link Data Clock and the following Interface Types.

Interface Type 1 – reverse data rate = reverse link data clock

Turn-Around 1 Length[7:0]

Specifies the number of bytes required for the MDDI_Data drivers in the host to disable their outputs.

Turn-Around 2 Length[7:0]

Specifies the number of bytes required for the MDDI_Data drivers in the host to enable their outputs.

Register Access Packet

Client registers in the client are accessed via the Register Access Packet.

	0	1	2	3	4	5	6	7			
1	Packet Length								2 bytes	←	Specifies the number of bytes in the packet not including the packet length field.
2										←	Specifies the format of this packet.
3	Packet Type									←	
4	(0x92)									←	
5	hClient ID								2 bytes	←	Reserved for the Client ID. Must be set to 0x00.
6	(0x00)									←	
7	Read/Write Info								2 bytes	←	Specifies the specific packet as either a write, or a read, or a response to a read.
8										←	
9	Register Address								4 bytes	←	Register address.
10										←	
11										←	
12										←	
13	Parameter CRC								2 bytes	←	CRC. Used to detect errors.
14										←	
	Register Data List (Packet Length - 14bytes)								x bytes	←	4-byte data that are written to or read from client registers.
										←	
	Register Data CRC								2 bytes	←	CRC. Used to detect errors.
										←	

Figure 91 Register Access Packet

Read/Write Info[15:0]

Specifies the specific packet as either a write, or a read, or a response to a read.

[13:0]: Specifies the number of 32-bit Register Data List items to be transferred in the Register Data List field.

[15:14]: Read/Write Flag

00: Writes Register Data List field value (32 bits) to registers specified by Register Address field.

Bits[13:0] specify the number of 32-bit register data items that are contained in the Register Data List field to be written to registers starting at the register specified by the Register Address field.

10: Requests registers of addresses specified by Register Address field. Bits[13:0] indicate the number of items register read is requested according to Register Address field. Register Data List field should be set to 0 bytes.

11: Indicates that the packet is data read according to request that [15:14] = 0. The Register Data List field contains addresses and read data of registers corresponding to the first Register Data List item. Bits[13:0] indicate the number of 32-bit register data items that have been read from registers specified by the Register Address field.

01: Reserved for future use. Setting inhibited.

Video Stream Packet

The R61529 writes image data to Frame memory via Video Stream Packet. The window and Frame memory addresses are set via Video Stream Packet.

	0	1	2	3	4	5	6	7			
1	Packet Length								2 bytes	←	Specifies the number of bytes in the packet not including the packet length field.
2											
3	Packet Type								2 bytes	←	Specifies the format of this packet.
4	(0x10)										
5	bClient ID								2 bytes	←	Reserved for the Client ID. Must be set to 0x00.
6	(0x00)										
7	Video Data Format Descriptor								2 bytes	←	Specifies the format of pixel data sent via this packet.
8											
9	Pixel Data Attributes								2 bytes	←	Specifies where pixel data is transferred.
10											
11	X Left Edge								2 bytes	←	Specifies a column start address in frame memory access area.
12											
13	Y Top Edge								2 bytes	←	Specifies a row start address in frame memory access area.
14											
15	X Right Edge								2 bytes	←	Specifies a column end address in frame memory access area.
16											
17	Y Bottom Edge								2 bytes	←	Specifies a row end address in frame memory access area.
18											
19	X Start								2 bytes	←	Specifies a column start address that Pixel Data is written. Not used. Must be set to 0x00.
20											
21	Y Start								2 bytes	←	Specifies a row start address that Pixel Data is written. Not used. Must be set to 0x00.
22											
23	Pixel Count								2 bytes	←	Specifies the number of pixels in the Pixel Data Field. Not used. Must be set to 0x00.
24											
25	Parameter CRC								2 bytes	←	Used to detect byte errors in the Packet Length to Pixel Count.
26											
27	Pixel Data								x bytes	←	Pixel Data
:	(Packet Length - 26 bytes)										
n-2											
n-1	Pixel Data CRC								2 bytes	←	CRC. Used to detect errors.
n											

Figure 92 Video Stream Packet

Video Data Format Descriptor[15:0]

[15:13]: Specifies the format of each Pixel Data.

[12]: Specifies whether the Pixel Data is packed or unpacked (how redundant bits are packed in bytes in Pixel Data transfer).

0: Each pixel in the Pixel Data field is byte-aligned with an MDDI byte boundary. (The Pixel Data is unpacked)

1: Each pixel in the Pixel Data is packed up against the previous pixel leaving no unused. (The Pixel Data is packed)

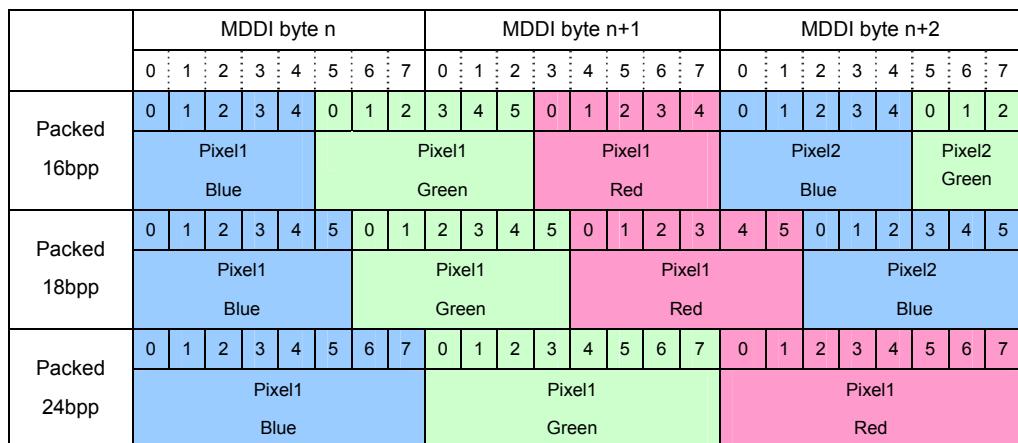
[11:0]: Specifies the number of bits per R pixel (by [11:8]), the number of bits per G pixel (by [7:4]), and the number of bits per B pixel (by [3:0]).

Table 34

[15:13]	[12]	[11:8]	[7:4]	[3:0]	Format
000	—	—	—	—	Monochrome format (Setting inhibited)
001	—	—	—	—	Color map format (Setting inhibited)
010	1	0x5	0x6	0x5	16bpp (Packed) RGB format (R:G:B=5:6:5)
	1	0x6	0x6	0x6	18bpp (Packed) RGB format (R:G:B=6:6:6)
	1	0x8	0x8	0x8	24bpp RGB format (R:G:B=8:8:8)
011	—	—	—	—	YUV422 format (Setting inhibited)
100	—	—	—	—	Bayer format (Setting inhibited)

Notes:

1. Video Stream Packet of the R61529 supports Forward Link, not Reverse Link. Read data from frame memory via Register Access Packet.
2. Do not send YUV data in RGB format.

**Figure 93**

Pixel Data Attributes[15:0]

- [15]: Indicates that the pixel in the Pixel Data field is the last pixel in a frame of data when bit 15 is set to 1.
- [14]: Reserved for future use and must be set to 0.
- [13:12]: Specifies a method for writing transparent data. (This is not used. Set to 00)
- [11:8]: Specifies an alternate display number. (This not used. Set to 00)
- [7:6]: Specifies the destination locations to which the Pixel Data is written. (The data is written to frame memory. Set to 00)
- [5]: Specifies that the Pixel Data is consecutive Frame Data of the Pixel Data that has been transferred.
- 0: X Left Edge, Y Top Edge, X Right Edge, Y Bottom Edge, X Start, and Y Start are enabled.
- 1: X Left Edge, Y Top Edge, X Right Edge, Y Bottom Edge, X Start, and Y Start are disregarded.
- [4]: Specifies whether the Pixel Data is camera data or display data. (The data is display data. Set to 0)
- [3]: Specifies whether the Pixel Data is Alternate Pixel Format or not. (Usual format is used. Set to 0)
- [2]: Specifies whether the Pixel Data supports an interlace format or not. (Interlace format is not supported. Set to 0)
- [1:0]: Specifies a method for transferring the Pixel Data. (Stereo image is not supported. Set to 11)

Windowless Video Stream Packet

The Windowless Video Stream Packet is a modification of the standard Video Stream Packet, however it removes the X and Y coordinates from the packet. This packet type assumes that full screen updates are always occurring and therefore there is no need for the window information. Bits[15:14] in the Pixel Data Attributes field are used to indicate the vertical synchronization of data (VSYNC) and each packet is assumed to be the width of the update region (HSYNC).

	0	1	2	3	4	5	6	7		
1	Packet Length								2 bytes	← Specifies the number of bytes in the packet not including the packet length field.
2									2 bytes	← Specifies the format of this packet.
3	Packet Type (0x16)								2 bytes	← Reserved for the Client ID. Must be set to 0x00.
4	(0x00)								2 bytes	← Specifies the format of pixel data sent via this packet.
5	bClient ID								2 bytes	← Specifies where pixel data is transferred.
6	(0x00)								2 bytes	← Specifies the number of pixels in the Pixel Data Field.
7	Video Data Format Descriptor								2 bytes	← Used to detect byte errors in the Packet Length to Pixel Count.
8									x bytes	← Pixel Data
9	Pixel Data Attributes								2 bytes	← CRC. Used to detect errors.
10										
11	Pixel Count									
12										
13	Parameter CRC									
14										
	Pixel Data (Packet Length - 14 bytes)									
	Pixel Data CRC									

Figure 94

Video Data Format Descriptor[15:0]

[15:13]: Specifies the format of each Pixel Data.

[12]: Specifies whether the Pixel Data is packed or unpacked (how redundant bits are packed in bytes in Pixel Data transfer).

0: Each pixel in the Pixel Data field is byte-aligned with an MDDI byte boundary. (The Pixel Data is unpacked)

1: Each pixel in the Pixel Data is packed up against the previous pixel leaving no unused. (The Pixel Data is packed)

[11:0]: Specifies the number of bits per R pixel (by [11:8]), the number of bits per G pixel (by [7:4]), and the number of bits per B pixel (by [3:0]).

Table 35

[15:13]	[12]	[11:8]	[7:4]	[3:0]	Format
000	—	—	—	—	Monochrome format (Setting inhibited)
001	—	—	—	—	Color map format (Setting inhibited)
010	1	0x5	0x6	0x5	16bpp (Packed) RGB format (R:G:B=5:6:5)
	1	0x6	0x6	0x6	18bpp (Packed) RGB format (R:G:B=6:6:6)
	1	0x8	0x8	0x8	24bpp RGB format (R:G:B=8:8:8)
011	—	—	—	—	YUV422 format (Setting inhibited)
100	—	—	—	—	Bayer format (Setting inhibited)

Note: Video Stream Packet of the R61529 supports Forward Link, not Reverse Link. Read data from frame memory via Register Access Packet.

Pixel Data Attributes[15:0]

[15:14]: Toggles VSYNC and HSYNC.

10: Changes VSYNC from non-active level to active level. HSYNC is toggled from non-active level for a certain period.

01: Returns VSYNC to non-active level if it is active level. VSYNC is returned to non-active level. HSYNC is toggled from non-active level for a certain period.

00: Not changes VSYNC and HSYNC.

11: Setting inhibited.

[13:12]: Specifies a method for writing transparent data. (This is not used. Set to 00)

[11:8]: Specifies an alternate display number. (This not used. Set to 00)

[7:6]: Specifies the destination locations to which the Pixel Data is written. (The data is written to frame memory. Set to 00)

[5]: Specifies that the Pixel Data is consecutive Frame Data of the Pixel Data that has been transferred.

0: X Left Edge, Y Top Edge, X Right Edge, Y Bottom Edge, X Start, and Y Start are enabled. (Setting inhibited)

1: X Left Edge, Y Top Edge, X Right Edge, Y Bottom Edge, X Start, and Y Start are disregarded. (Set bit[5] to 1)

[4]: Specifies whether the Pixel Data is camera data or display data. (The data is display data. Set to 0)

[3]: Specifies whether the Pixel Data is Alternate Pixel Format or not. (Usual format is used. Set to 0)

[2]: Specifies whether the Pixel Data supports an interlace format or not. (Interlace format is not supported. Set to 0)

[1:0]: Specifies a method for transferring the Pixel Data. (Stereo image is not supported. Set to 11)

	MDDI byte n								MDDI byte n+1								MDDI byte n+2							
	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
Packed 16bpp	0	1	2	3	4	0	1	2	3	4	5	0	1	2	3	4	0	1	2	3	4	0	1	2
	Pixel1 Blue					Pixel1 Green					Pixel1 Red					Pixel2 Blue					Pixel2 Green			
Packed 18bpp	0	1	2	3	4	5	0	1	2	3	4	5	0	1	2	3	4	5	0	1	2	3	4	5
	Pixel1 Blue					Pixel1 Green					Pixel1 Red					Pixel2 Blue					Pixel2 Blue			
Packed 24bpp	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
	Pixel1 Blue								Pixel1 Green								Pixel1 Red							

Figure 95

Client Capability Packet

The Client Capability Packet informs the host of the capabilities of the client so it can configure the host-to-client link in an optimum manner. The host can request the client to transmit this packet to the host client via the Reverse Link Flags in the Reverse Link Encapsulation Packet.

	0	1	2	3	4	5	6	7		
1	Packet Length (0x4A)								2 bytes	← Specifies the number of bytes in the packet not including the packet length field.
2									2 bytes	← Specifies the format of this packet.
3	Packet Type (0x42)								2 bytes	← Reserved for the Client ID. Not used. Returns 0x00.
4									2 bytes	← Specifies the minimum protocol version used by the client. Must be set to 1 or more.
5	hClient ID (0x00)								2 bytes	← Specifies the minimum protocol version that the client can use.
6									2 bytes	← Specifies the maximum data rate the client can receive on each data pair on the forward MDDI link prior to performing forward link skew calibration. The rate is specified as the number of million bits per second (Mbps).
7	Protocol Version (0x02)								1 byte	← Specifies the interface types that are supported on the forward and reverse links.
8									1 byte	← Specifies the number of alternate displays supported by the client. Not used. Returns 0x00.
9	Min Protocol Version (0x01)								2 bytes	← Specifies the maximum data rate the client can receive on each data pair on the forward MDDI link after performing forward link skew calibration. The rate is specified as the number of million bits per second (Mbps).
10									2 bytes	← Specifies the width of the bitmap of frame memory in the client expressed as the number of pixels.
11	Pre-calibration Data Rate Capability (0x32) (TBD)								2 bytes	← Specifies the height of the bitmap of frame memory in the client expressed as the number of pixels.
12									2 bytes	← Specifies the width of the display window in the client as the number of pixels.
13	Interface Type Capability (0x01)								2 bytes	← Specifies the height of the display window in the client expressed as the number of pixels.
14	Number of All Displays (0x00)								4 bytes	← Specifies the number of available color map tables in the client. Not used. Returns 0x00.
15										
16	Post-calibration Data Rate Capability (0x17C) (TBD)									
17										
18	Bitmap Width (0x13F)									
19										
20	Bitmap Height (0x1DF)									
21										
22	Display Window Width (0x13F)									
23										
24	Display Window Height (0x1DF)									
25										
26	Color Map Size (0x0000)									

Figure 96 Client Capability Packet

27			
28			
29	Color Map RGB Width (0x00)	2 bytes	← Specifies the number of bits of the red, green, and blue color components that is used in the color map display mode. Not used. Returns 0x00.
30			
31	RGB Capability (0x8888)	2 bytes	← Specifies the number of bits of resolution that can be displayed in RGB format.
32			
33	Monochrome Capability (0x00)	1 byte	← Specifies the number of bits of resolution that can be displayed in monochrome format. Not used. Returns 0x00.
34	Reserved 1(0x00)	1 byte	← Reserved for future use. Not used. Returns 0x00.
35	Y Cb Cr Capability (0x00)	2 bytes	← Specifies the number of bits of resolution that can be displayed in Y Cb Cr format. Not used. Returns 0x00.
36			
37	Bayer Capability (0x00)	2 bytes	← Specifies the number of bits of resolution, pixel group, and pixel order that can be displayed in Bayer format. Not used. Returns 0x00.
38			
39	Reserved 2 (0x00)	2 bytes	← Reserved for future use. Not used. Returns 0x00.
40			
41	Client Feature Capability (0x4C0100)	4 bytes	← Capabilities supported by the client.
42			
43			
44			
45	Max Video Frame Rate (0x3C) (TBD.)	1 byte	← Specifies the maximum video frame update capability of the client in frames per second. The host needs to update the image at a rate less than or equal to the value specified in this field. .
46	Min Video Frame Rate (0x00)	1 byte	← Specifies the minimum video frame update capability of the client in frames per second. The host needs to update the image at a rate greater than or equal to the value specified in this field. .
47			
48	Min Sub-frame Rate (0x01)	2 bytes	← Specifies the minimum sub-frame rate in frames per second.
49			
50	Audio Buffer Depth (0x00)	2 bytes	← Specifies the depth of the elastic buffer in the client dedicated to each audio stream. Not used. Returns 0x00.
51			
52	Audio Channel Capability (0x00)	2 bytes	← Audio channels are supported by the client. Not used. Returns 0x00.

Figure 97 Client Capability Packet (continued)

53	Audio Sample Rate Capability (0x00)	2 bytes	← Contains a set of flags that indicate the audio sample rate capability of the client. Not used. Returns 0x00.
55	Audio Sample Resolution (0x00)	1 byte	← Specifies the number of bits per audio sample that must be sent to the client in an Audio Stream Packet. Not used. Returns 0x00.
56	Mic Audio Sample Resolution (0x00)	1 byte	← Specifies the number of bits per audio sample that the Mic must send to the host in an Audio Stream Packet. Not used. Returns 0x00.
57	Mic Sample Rate Capability (0x00)	2 bytes	← Specifies the number of bits per audio sample that the Mic must send to the host in an Audio Stream Packet. Not used. Returns 0x00.
58			
59	Keyboard Data Format (0x00)	1 byte	← Specifies whether a keyboard is connected to the client system and the type of keyboard that is connected. Not used. Returns 0x00.
60	Pointing Device Data Format (0x00)	1 byte	← Specifies whether a pointing device is connected to the client system and the type of keyboard pointing device that is connected. Not used. Returns 0x00.
61	Content Protection Type (0x00)	2 bytes	← A set of flags to indicate the type of digital content protection that is supported by the client. Not used. Returns 0x00.
62			
63	Mfr Name	2 bytes	← 3-character ID of manufacturer. Not used. Returns 0x00.
64	(0x00)		
65	Product Code	2 bytes	← Product code assigned by the display manufacturer.
66	(0x1529)		
67	Reserved 3	2 bytes	← Reserved for future use. Not used. Returns 0x00.
68	(0x00)		
69	Serial Number	4 bytes	← Specifies the serial number of the display. Not used. Returns 0x00.
70	(0x0000)		
71			
72			
73	Week of Mfr (0x00)	1 byte	← Defines the week of manufacture of the display. Not used. Returns 0x00.
74	Year of Mfr (0x00)	1 byte	← Defines the year of manufacture of the display. Not used. Returns 0x00.
75	CRC	2 bytes	← CRC. Used to detect errors.
76			

Figure 98 Client Capability Packet (continued)

Interface Type Capability[7:0]

A bit set to 1 indicates that the specified interface type is supported, and a bit set to 0 indicates that the specified interface type is not supported. All hosts and clients must support at least Type 1 on the forward and reverse links.

[0]: Type 2 is supported on the forward link. (Not used. Returns 0)

[1]: Type 3 is supported on the forward link. (Not used. Returns 0)

[2]: Type 4 is supported on the forward link. (Not used. Returns 0)

[3]: Type 2 is supported on the reverse link. (Not used. Returns 0)

[4]: Type 3 is supported on the reverse link. (Not used. Returns 0)

[5]: Type 4 is supported on the reverse link. (Not used. Returns 0)

[7:6]: Reserved for future use. Returns 0.

RGB Capability[15:0]

The number of bits of resolution that can be displayed in RGB format is specified. A bit set to 1 indicates that the specified resolution is supported, and a bit set to 0 indicates that the specified resolution is not supported.

[3:0]: Specifies the maximum number of bits of blue in each pixel.

[7:4]: Specifies the maximum number of bits of green in each pixel.

[11:8]: Specifies the maximum number of bits of red in each pixel.

[13:12]: Reserved for future use. Returns 0x0.

[14]: Specifies whether the client supports unpacked RGB format.

1: The client supports unpacked RGB format.

0: The client does not support unpacked RGB format.

[15]: Specifies whether the client supports packed RGB format.

1: The client supports packed RGB format.

0: The client does not support packed RGB format.

In unpacked format, each pixel in the Pixel Data field is transferred with unused bits that occur in Pixel Data transfer left. In packed format, each pixel in the Pixel Data is transferred without leaving unused bits.

Client Feature Capability[31:0]

Whether specific features in the client are supported is specified. A bit set to 1 indicates the capability is supported, and a bit set to 0 indicates the capability is not supported.

Whether specific features in the client are supported is specified. A bit set to 1 indicates the capability is supported, and a bit set to 0 indicates the capability is not supported.

[0]: The Bitmap Block Transfer Packet. (Not used. Returns 0)

[1]: The Bitmap Area Fill Packet. (Not used. Returns 0)

[2]: The Bitmap Pattern Fill Packet. (Not used. Returns 0)

[3]: The Read Frame Buffer Packet. (Not used. Returns 0)

[4]: The Transparent Color and Mask Setup Packet. (Not used. Returns 0)

[5]: Audio data in unpacked format. (Not used. Returns 0)

[6]: Audio data in packed format. (Not used. Returns 0)

[7]: Reverse-link video stream data from a camera. (Not used. Returns 0)

[8]: The client has the ability to receive a full line of pixel data and ignore display addressing as specified by bit 5 of the Pixel Data Attributes field of the Video Stream Packet, and the client can also detect frame sync or end of video frame data via bit 15 of the Pixel Data Attributes field.

[9]: The Display Power State Packet. (Not used. Returns 0)

[10]: Display power state 01 defined by the Power State field of the Display Power State Packet. (Not used. Returns 0)

[11]: The client is connected to a pointing device and can send the Pointing Device Data Packet. (Not used. Returns 0)

[12]: The client is connected to a keyboard device and can send the Keyboard Data Packet. (Not used. Returns 0)

[13]: The client can set audio or video parameters supported by the VCP Feature Packets. (Not used. Returns 0)

[14]: The client can write pixel data to the offline display frame buffer. (Not used. Returns 0)

[15]: The client can write pixel data to the display frame buffer currently being used to refresh the display image. (Not used. Returns 0)

[16]: The client can write pixel data to all display frame buffers via a single Video Stream Packet. (Not used. Returns 0)

- [17]: The Request Specific Status Packet. (Not used. Returns 0)
- [18]: The Round-Trip Delay Measurement Packet. (Not used. Returns 0)
- [19]: The Forward Link Skew Calibration Packet. (Available. Returns 1)
- [20]: The client can respond to Valid Status Reply List Packet according to Request Specific Status Packet. (Not used. Returns 0)
- [21]: The client can use the Bitmap Block Transfer Packet, Bitmap Area Fill Packet, and Bitmap Pattern Fill Packet. (Not used. Returns 0)
- [22]: The Register Access Packet. (Available. Returns 1)
- [23]: The client can decode enhanced Video Stream Packets. (Not used. Returns 0) This packet includes the Windowless Video Packet as well as the Flexible Video Stream Packet.
- [24]: The Enhanced Reverse Encapsulation Packet. (Not used. Returns 0)
- [25]: The client can freeze a state. (Not used. Returns 0)
- [31:26]: Reserved for future use. Returns 0x0.

Client Request and Status Packet

This packet contains the minimum information including error and status needed so that the host can configure the host-to-client link in an optimum manner. The client sends this packet as the first packet when the host requests the Reverse Link Encapsulation Packet or Enhanced Reverse Link Encapsulation Packet. This packet is required by the host via the Reverse Link Flags in the Reverse Link Encapsulation Packet.

	0	1	2	3	4	5	6	7			
1	Packet Length								2 bytes	←	Specifies the number of bytes in the packet not including the packet length field.
2											
3	Packet Type								2 bytes	←	Specifies the format of this packet.
4	(0x46)										
5	hClient ID								2 bytes	←	Reserved for the Client ID. Not used. Returns 0x00.
6	(0x00)										
7	Reverse Link Request								2 bytes	←	Specifies the number of bytes the client needs in the reverse link in the next sub-frame to send information to the host.
8											
9	CRC Error Count								1bytes	←	Indicates the number of CRC errors that have occurred since the last Client Request and Status Packet is sent. The number is reset to 0 each time this packet is sent. Returns 255 if the number of CRC errors exceeds 255.
10	Client Status (0x00)								1bytes	←	A group of flags that indicates the current status of the client device. Not used. Returns 0x00.
11	Client Busy Flags (0xFFFF)								2 bytes	←	A set of busy flags to indicate that the client is performing a specific function and is not ready to accept another packet related to that function. Not used. Returns 0xFFFF.
12											
13	CRC								2 bytes	←	CRC. Used to detect errors.
14											

Figure 99

Client Status[7:0]

[0]: Indicates that there has been a change in the capability of the client. This could be due to the user connecting a peripheral device such as a microphone, keyboard, or display, or some other reason.

1: Capability has changed. Examine the Client Capability Packet to determine the new client characteristics.

0: Capability has not changed since the last Client Capability Packet was sent.

[1]: Indicates that the client device has detected an error in processing a packet since the last Client Capability Packet was sent.

[7:2]: Reserved for future use. Returns 0x0.

Client Busy Flags[15:0]

A set of busy flags to indicate that the client is performing a specific function and is not ready to accept another packet related to that function. A bit set to 1 indicates that the particular function is currently being performed by the client and the related function in the client is busy and returns 1. A bit set to 0 indicates that the related function in the client is ready and returns 0. The client must always return a busy status (bit set to 1) for all functions that are not supported in the client.

[0]: Bitmap block transfer function is busy.

[1]: Bitmap area fill function is busy.

[2]: Bitmap pattern fill function is busy.

[3]: The graphic subsystem is busy performing an operation that requires use of the frame buffer in the client.

[15:4]: Reserved for future use. Returns 0xFFFF.

Perform Type Handoff Packet

The Perform Type Handoff Packet is a means for the host to command the client to handoff interface type on forward link and reverse link. The host and the client must switch to the specified interface type on forward link and reverse link immediately after this packet is sent. Then, a new interface setting is enabled from a packet to be sent next.

	0	1	2	3	4	5	6	7		
1	Packet Length								2 bytes	← Specifies the number of bytes in the packet not including the packet length field. (Type 1: 16h)
2										
3	Packet Type								2 bytes	← Specifies the format of this packet.
4	(0x4D)									
5	Interface Type (0x9)								1 byte	← Confirms the new interface type to use.
6	Reversed 1								1 byte	← Reserved for future use. Not used. Returns 0x00.
7	Delay Filler								16 bytes	← Allow sufficient time for the client to prepare to switch over to use the new interface type setting. Set data to 0x00.
:	(0x00)									
23	CRC								2 bytes	← CRC. Used to detect errors.
24										

Figure 100

Interface Type[7:0]

[2:0]: Defines the interface type to be used on the forward link:

001: Handoff to Interface Type 1.

010: Handoff to Interface Type 2. (Not supported. Do not use)

011: Handoff to Interface Type 3. (Not supported. Do not use)

100: Handoff to Interface Type 4. (Not supported. Do not use)

[5:3]: Defines the interface type to be used on the reverse link.

001: Handoff to Interface Type 1.

010: Handoff to Interface Type 2. (Not supported. Do not use)

011: Handoff to Interface Type 3. (Not supported. Do not use)

100: Handoff to Interface Type 4. (Not supported. Do not use)

[7:6]: Reserved for future use. Must be set to 0x00.

Delay Filler

The purpose of this field is to allow sufficient time for the client to prepare to switch over to use the new interface type setting. The number of bytes in this field always results in it being 64 MDDI_Stb cycles in length. The length of the Delay Filler field is based on the interface type setting of the forward link as follows:

Forward Link Interface Type 1 – Delay Filler is 16 bytes.

MDDI Command Setting

When transferring a MIPI command that does not include a parameter, follow the setting below.

Table 36

Register Access Packet Parameter	Register Setting
Read/Write Info[15:0]	0 x 0000
Register Address[31:0]	24'h000000+CMD[7:0]
Register Data (1)[31:0]	32'h00000000

When transferring a MIPI command that includes a parameter, follow the setting below. When transferring MIPI commands, Register Access Packet is needed to send several times.

Table 37

Register Access Packet Parameter	Register Setting
Read/Write Info[15:0]	0 x 000n
Register Address[31:0]	24'h000000+CMD[7:0]
Register Data(1)[31:0]	24'h000000+PRM(1)[7:0]
:	:
Register Data(n)[31:0]	24'h000000+PRM(n)[7:0]

Shutdown Mode Setting

The R61529's Client MDDI supports Shutdown setting to bring the R61529 to the standby state to save power consumption during Hibernation.

By setting DSTB = 1 and sending Shutdown Packet, MDDI enters the Hibernation state. The Client MDDI's standby power requirement can be reduced while MDDI Link is maintained in the Hibernation state.

In Shutdown mode, the R61529 halts operation other than maintaining Hibernation state. In canceling Shutdown mode, execute HWRESET or input "Low" pulse 6 times from CSX pin. After canceling Shutdown mode, cancel the Hibernation state by Host-initiated Wake up.

For Shutdown Mode setting sequence, see "Deep Standby Mode / Shutdown Mode (MDDI) On/Off Sequence."

In Shutdown mode, command setting and Frame memory data are not retained and they must be reset after canceling the Hibernation state.

When setting and canceling the Hibernation state, follow the sequence as specified in the MDDI specifications by VESA.

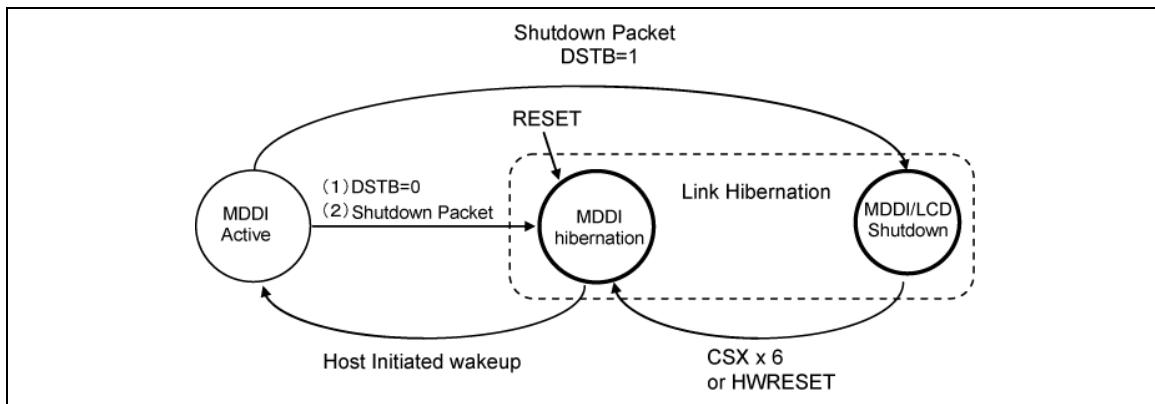


Figure 101 State Transitions in Shutdown Mode

CRC Error Detection Mode Setting

CRC error detection mode can be set by command. When this mode is set, CRC error is detected and an output level of the DOUT pin is set to "High."

Table 38 CRC Error Detection Mode Setting

Command	Description
MDCRC	Enables CRC error detection mode.
CRCSTP	Detection is temporarily halted. Setting CRCSTP sets an output level of the DOUT pin to "Low". CRCSTP is used to clear detection signal.

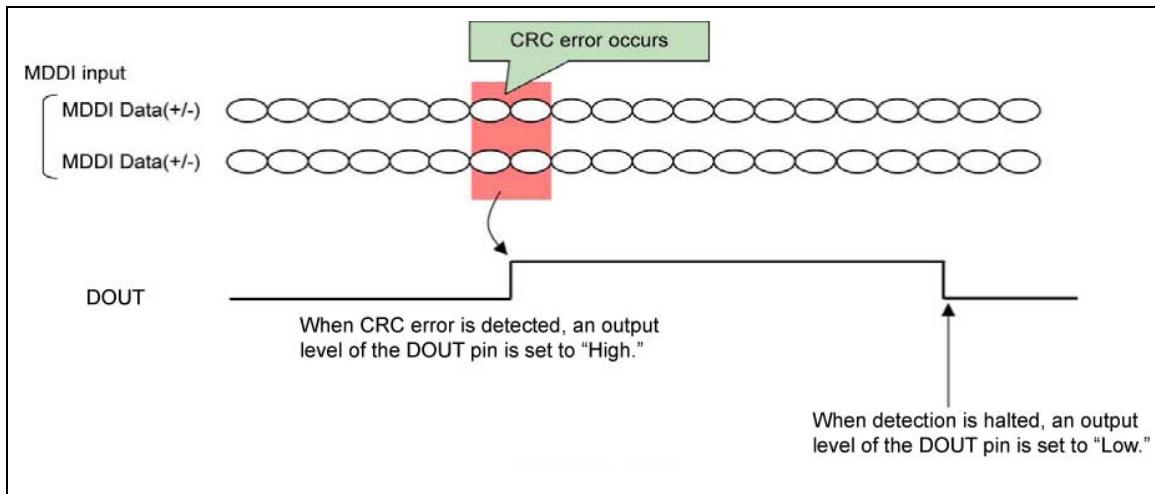


Figure 102

MDDI Moving Picture Interface

The R61529 supports TE interface to display moving picture in MDDI operation. Select either one according to the configuration of the system. By transferring data according to the following sequences, the R61529 can display moving picture via MDDI without tearing.

The Client MDDI supported by the R61529 adopts 2-frame data transfer format when writing moving picture data. By synchronizing the moving picture data rewrite operation via MDDI with the frame mark signal from the R61529 (TE), the R61529 can display moving picture via MDDI without tearing.

The output position of TE signal can be changed in units of lines. The output cycle of TE signal can also be changed in units of frames. Make these settings according to the MDDI transfer speed and data rewrite cycle.

In combination with the Hibernation setting, moving picture can be displayed via MDDI-TE with low power consumption.

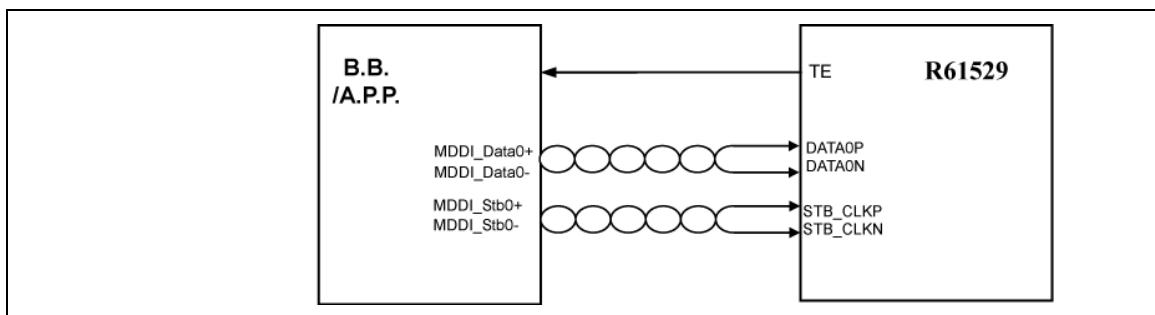


Figure 103

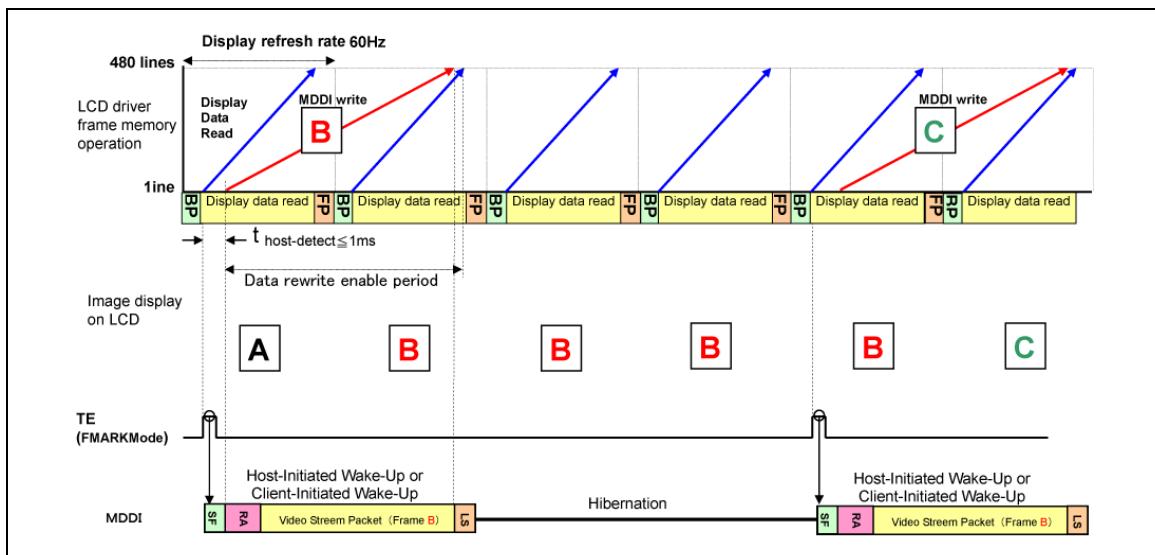


Figure 104

MDDI Mobile Display System

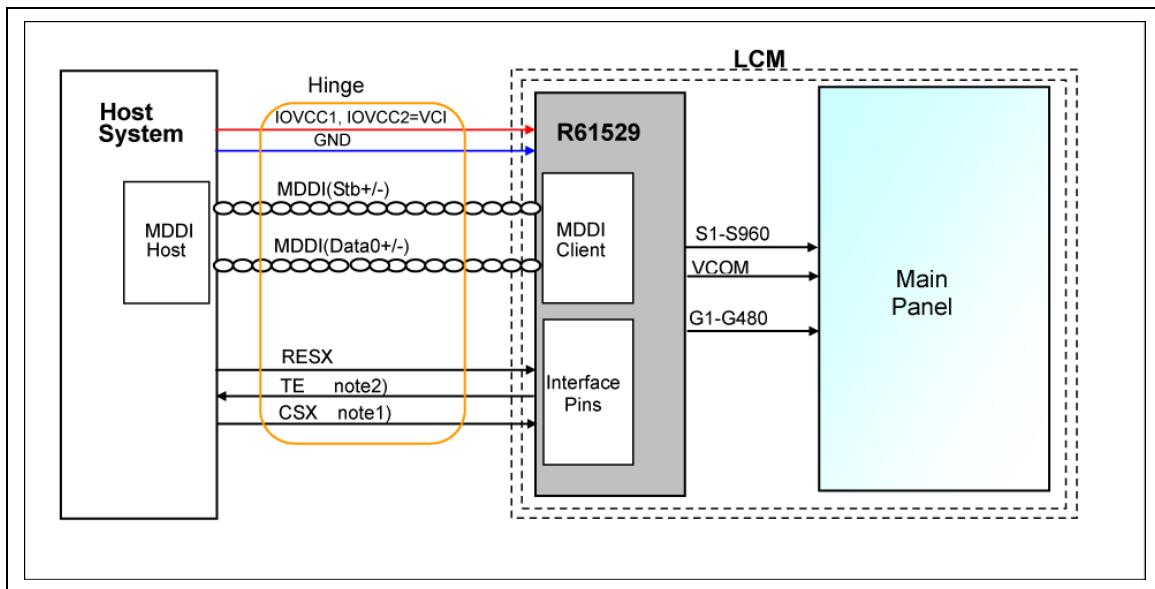


Figure 105 R61529 MDDI Mobile Display System Configuration Example

- Notes:
1. The CSX pin is used exclusively for the signal to cancel shutdown mode in MDDI operation. While not using Shutdown mode, the CSX pin does not have to be connected to the Host System.
 2. Use TE signal as the reference signal for moving picture display according to the configuration of system.
 3. The R61529 does not support the logic output ports to control peripheral devices and sub-display interface.

Method for Switching between MDDI and System Interface

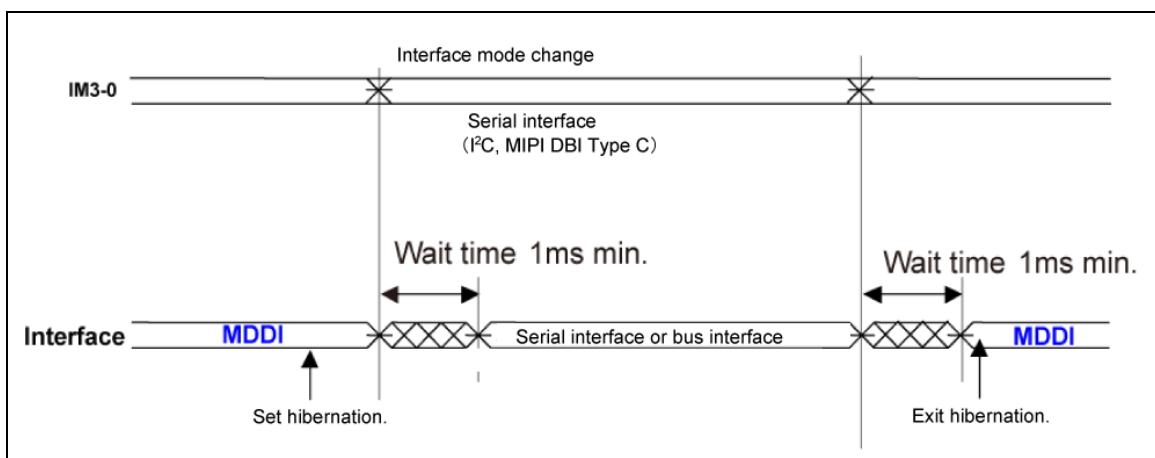


Figure 106

Forward Link Synchronization

The client must synchronize with the forward link in order to reliably receive all packets sent by the host. The following figure is a state diagram of the process the client must perform to achieve synchronization.

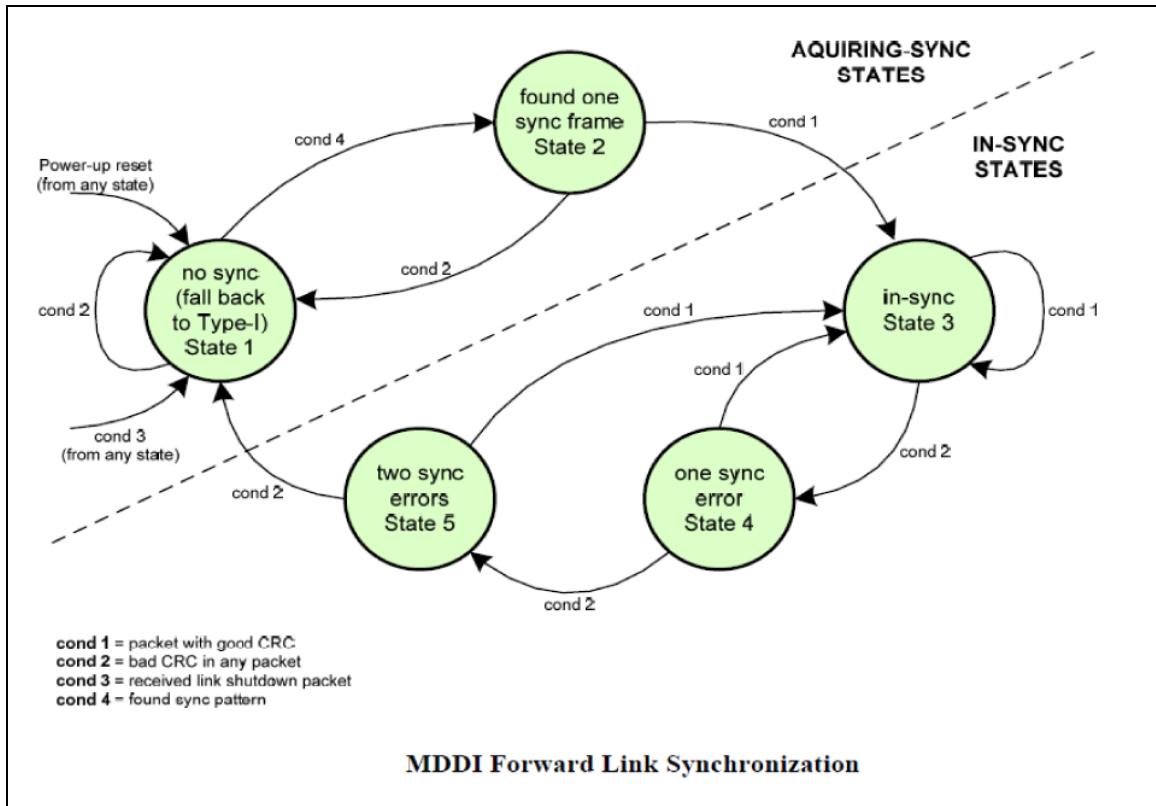


Figure 107

1. State 1: no sync

- (1) The client starts in the “no sync” state after power-up reset or Link Shutdown Packet.
- (2) The client searches for the unique word in the Sub-frame Header Packet.
- (3) When the unique word is found, the client saves the Sub-frame Length field.

* The client does not check the CRC on the first sub-frame header packet that was detected.

- (4) The sync state progresses to “found one sync sub-frame.”

2. State 2: found one sync frame

- (1) From all states other than “no sync”, if a packet with a good CRC is detected then the state progresses to the “in-sync” state.
- (2) If the CRC in any packet is not correct, then the state progresses to the “no sync” state along the appropriate path indicated in the state diagram.

3. State 3: in-sync

- (1) If a packet with a good CRC is detected, the state progresses to the “in-sync” state.
- (2) If the CRC in any packet is not correct, the state progresses to the “one sync error” state.

4. State 4: one sync error

- (1) If a packet with a good CRC is detected, the state progresses to the “in-sync” state.
- (2) If the CRC in any packet is not correct, the state progresses to the “two sync error” state.

5. State 5: two sync error

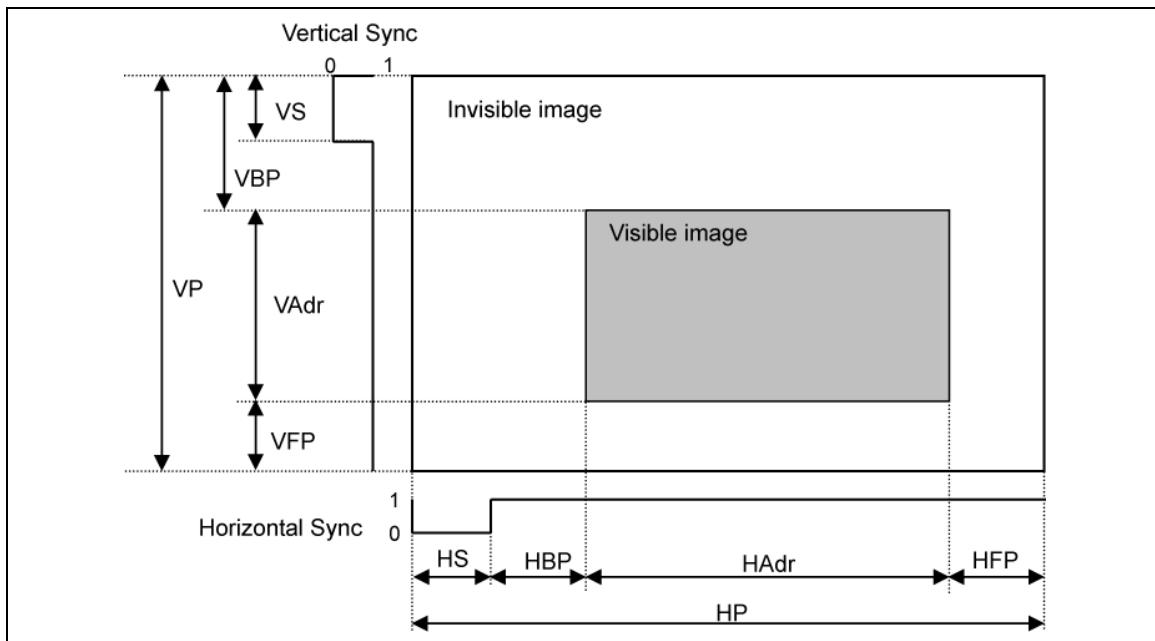
- (1) If a packet with a good CRC is detected, the state progresses to the “in-sync” state.
- (2) If the CRC in any packet is not correct, the state progresses to the “no sync” state.

* From all state other than “no sync”, if a packet with a good CRC is detected then the state progresses to the “in-sync” state.

* If the CRC in any packet is not correct, then the state progresses to the “no sync” state along the appropriate path indicated in the state diagram.

* In the “no sync” state, all packets others than Sub-frame Header Packet are disregarded.

* Client Request and Status Packet can read the number of CRC errors and counts up to 255. The error count is reset after the Client Status and Request Packet reads.

Active Refresh Mode**Figure 108****Table 39 Example of Vertical Display Timing Setting**

Item	Symbol	Condition	Unit	Min.	Typ.	Max.	Notes
Vertical cycle	VP		line	408	496	736	
Vertical low pulse width	VS		line	1	2	4	
Vertical front porch	VFP		line	4	8	128	
Vertical back porch	VBP		line	4	8	128	
Vertical data start point	-	VBP	line	4	8	128	
Vertical blanking period	VBL	VBP+VFP	line	8	16	256	
Vertical active area	Vadr		line	240	480	480	

Table 40 Example of Horizontal Display Timing Setting

Item	Symbol	Condition	Unit	Min.	Typ.	Max.	Notes
Horizontal front porch	HFP		ByteClock	600	—	—	
Horizontal data start point	-	HS+HBP	ByteClock	3	—	—	
Horizontal active area	Hadr		Pixel	320	320	320	

Note: $f_{\text{ByteClock}} = (1/2) * f_{\text{MDDICLK}}$. $f_{\text{ByteClock}}$ = frequency of ByteClock

Display Pixel Interface (DPI)

DPI

In Display Pixel Interface (DPI) operation, display operation is in synchronization with synchronous signals VSYNC, HSYNC, and PCLK. Video data is directly output as display data without being written to frame memory. In DPI operation, front porch period (FP), back porch period (BP), and display period (NL) must be made. Command must be transferred via DBI Type C serial interface. DPI and DSI/MDDI cannot be selected simultaneously.

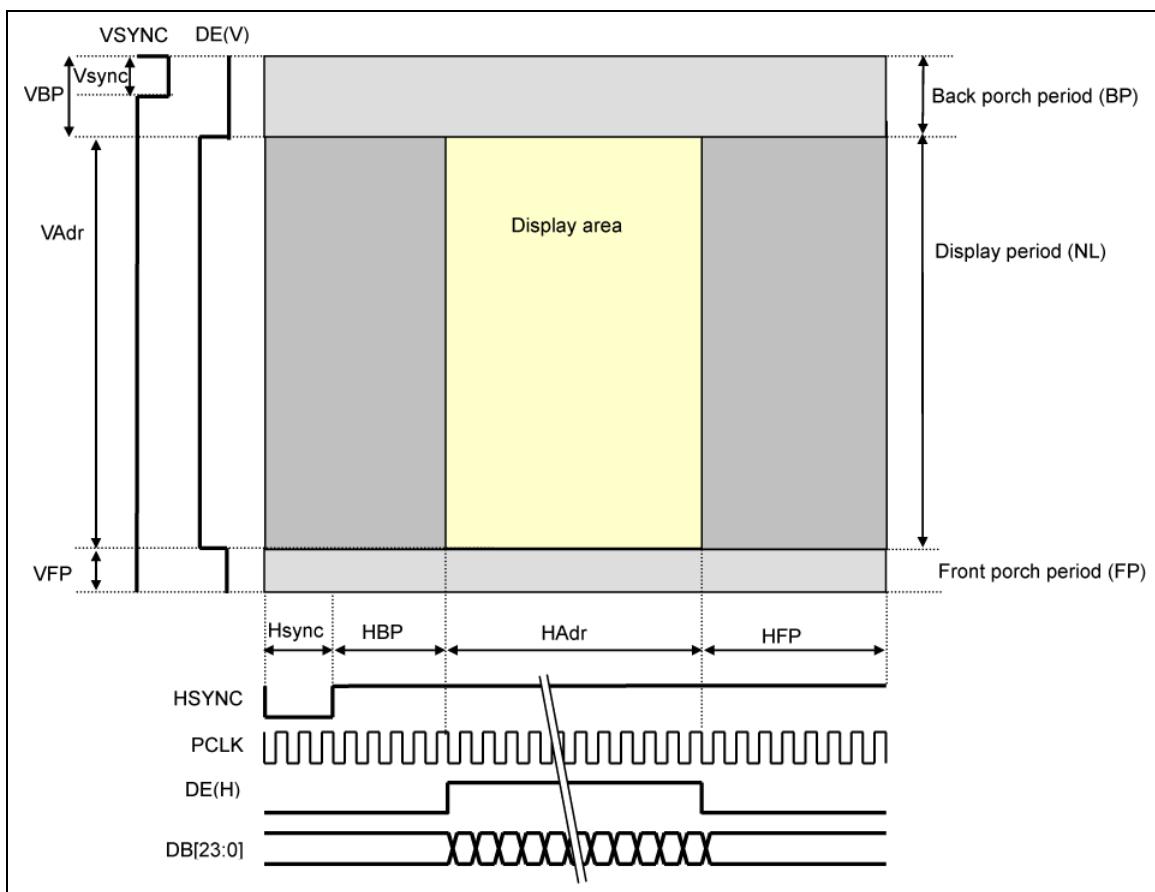


Figure 109

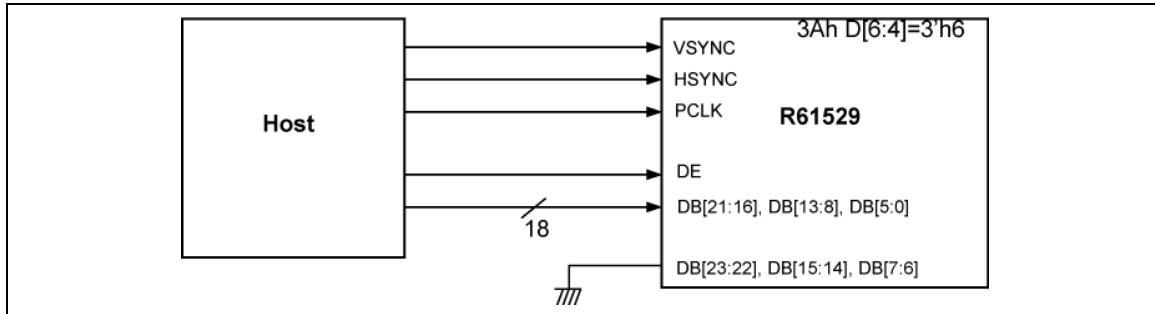
Table 41 Display Timing Setting Example (TBD)

Parameters	Symbols	Min.	Typ.	Max.	Step	Unit
Horizontal Synchronization	Hsync	2	10	16	1	PCLKCYC
Horizontal Back Porch	HBP	2	20	-	1	PCLKCYC
Horizontal Address	HAdr	-	320	-	1	PCLKCYC
Horizontal Front Porch	HFP	2	10	-	1	PCLKCYC
Vertical Synchronization	Vsync	1	2	4	1	Line
Vertical Back Porch	BP	4	8	128	1	Line
Vertical Address	VAdr	400	480	480	1	Line
Vertical Front Porch	VFP	4	8	128	1	Line

Note: Typical values are setting example when used with panel resolution QVGA (320RGB x 480), clock frequency 10.7 MHz and frame frequency about 60 Hz.

18-Bit DPI

18-bit DPI can be used when set_pixel_format (3Ah) D[6:4]=3'h6. Images are displayed in synchronization with synchronous signals VSYNC, HSYNC, and PCLK. 18-bit RGB data (DB[21:16], DB[13:8], and DB[5:0]) are transferred in synchronization with data enable signal (DE) and display operation. Only system interface (DBI Type C or I²C) can be used to set commands.

**Figure 110**

24-Bit DPI

24-bit DPI can be used when set_pixel_format (3Ah) D[6:4]=3'h7. Images are displayed in synchronization with synchronous signals VSYNC, HSYNC, and PCLK. 24-bit RGB data (DB[23:0]) are transferred in synchronization with data enable signal (DE) and display operation. Only system interface (DBI Type C or I²C) can be used to set commands.

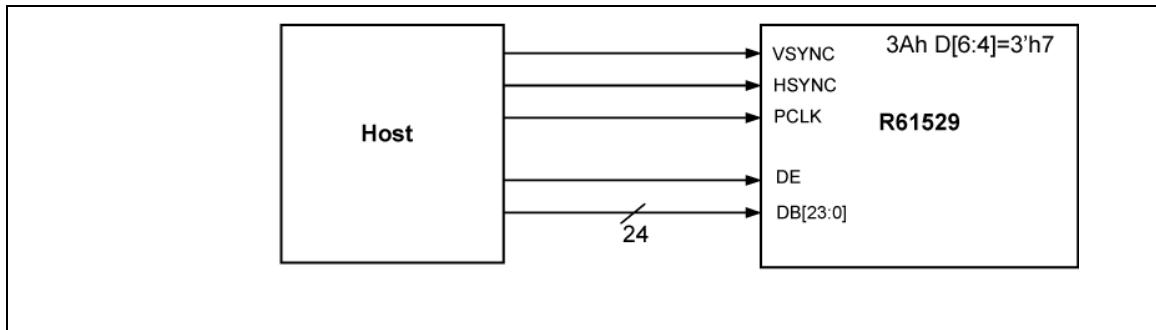


Figure 111

Setting Example for Display Control Clock in DPI Operation

The R61529 performs display operation using DPI by internal clock (PCLKD) generated by dividing PCLK frequency input from system. Set the PCLKD frequency as approximate as possible to frequency of OSC clock that is a reference clock. OSC clock is generated by dividing oscillation clock ($f_{osc} = 14$ MHz) according to DIV[3:0] setting (See description of C1h command). OSC clock equals a reference clock (clk).

PCLKD high period is specified by PCDIVH[3:0] (C0h command). PCLKD low period is specified by PCDIVL[3:0] (C0h command). Then, PCLKD frequency is specified.

PCDIVH [3:0]: Specifies the number of PCLK during internal clock PCLKD's high period in units of 1 clock.

PCDIVL [3:0]: Specifies the number of PCLK during internal clock PCLKD's low period in units of 1 clock.

Notes: 1. Make sure (PCDIVL = PCDIVH) or (PCDIVL = PCDIVH - 1).

2. Follow a restriction (Number of PCLK in 1H) \geq (Number of clocks set by RTN) \times (PCDIVL + PCDIVH).

A setting example is shown below. (Frame frequency is 60 Hz)

Resolution

320RGB \times 480 lines

Hsync = 10, HFP = 10, HBP = 20

VFP = 8, VBP = 8

Internal Clock

Internal Oscillation Clock: 14MHz

DIVn[3:0] = 4'h7 (x 1/12)

RTN[6:0] = 7'h27 (39 clocks)

BP[4:0] = 5'h8

FP[4:0] = 5'h8

NL[5:0] = 6'h3B

PCLK

60Hz \times (8 + 480 + 8) lines \times (10 + 20 + 320 + 10) clocks = 10.72 MHz

OSC clock = f_{osc} /12

10.72 MHz/(14 MHz/12) = 9.19

Set PCDIVH and PCDIVL so that PCLK frequency is divided into 9.

Judging from note 1, PCDIVH[3:0] is 4'h5 and PCDIVL[3:0] = 4'h4.

DPI Data Format

The R61529 supports 24bpp and 18bpp color formats shown below.

Table 42

DPI color format	MIPI Spec.	R61529	3Ah (set_pixel_format) D[6:4]
24bpp (16,777,216-color)	Yes	Yes	3'h7
18bpp (262,144-color Configuration 1)	Yes	No	-
18bpp (262,144-color Configuration 2)	Yes	Yes	3'h6
16bpp (65,536-color Configuration 1)	Yes	No	-
16bpp (65,536-color Configuration 2)	Yes	No	-
16bpp (65,536-color Configuration 3)	Yes	No	-

Yes: Supported

No: Unsupported

See tables in the next page for connection between host pins and the R61529's pins.

(a) 24-Bit Interface

When 24bpp format is selected by set_pixel_format (3Ah) ($D[6:4] = 3'h7$), connection between host pins and the R61529's pins is shown below.

Host pin	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
R61529 pin	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0

Figure 112

(b) 18-Bit Interface

When 18bpp format is selected by set_pixel_format (3Ah) ($D[6:4] = 3'h6$), connection between host pins and the R61529's pins is shown below.

Host pin	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	Not used	Not used	R5	R4	R3	R2	R1	R0	Not used	G5	G4	G3	G2	G1	G0	Not used	B5	B4	B3	B2	B1	B0	Not used	Not used
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
R61529 pin	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	Not used	Not used	R5	R4	R3	R2	R1	R0	Not used	G5	G4	G3	G2	G1	G0	Not used	B5	B4	B3	B2	B1	B0	Not used	Not used

Figure 113

Extended Format for 24 Bits/Pixel Data in 18-Bit Interface Operation

The R61529 supports a format extended from 18bpp to 24bpp as shown below. A method for extending a format is set by EPF.

	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
24bpp	R[5]	R[5]	R[7]	R[6]	R[6]	R[5]	R[4]	R[4]	R[3]	R[3]	R[3]	R[2]	R[2]	R[1]	R[1]	R[0]	R[2]	R[2]	R[1]	R[1]	R[0]	R[1]	R[0]	R[1]
18bpp EPF=2'h0 <u>(Note 1)</u>	R[4]	R[4]	R[4]	R[3]	R[3]	R[3]	R[2]	R[2]	R[1]	R[1]	R[1]	R[0]												
18bpp EPF=2'h1 <u>(Note 2)</u>	R[3]	R[3]	R[3]	R[2]	R[2]	R[2]	R[1]	R[1]	R[1]	R[1]	R[1]	R[0]												
18bpp EPF=2'h2	R[5]	R[5]	R[5]	R[4]	R[4]	R[4]	R[3]	R[3]	R[3]	R[3]	R[3]	R[2]												

Figure 114

- Notes:
1. Special processing: R[5:0], G[5:0], B[5:0] = 6'h3F → 8'hFF
 2. Special processing: R[5:0], G[5:0], B[5:0] = 6'h00 → 8'h00
 3. Setting EPF to 2'h3 is prohibited.

VSYNC Interface

The R61529 supports VSYNC interface, which enables displaying a moving picture without tearing by synchronizing MIPI DBI Type B interface (8/16/18/24 bits) with frame synchronous signal (VSYNC).

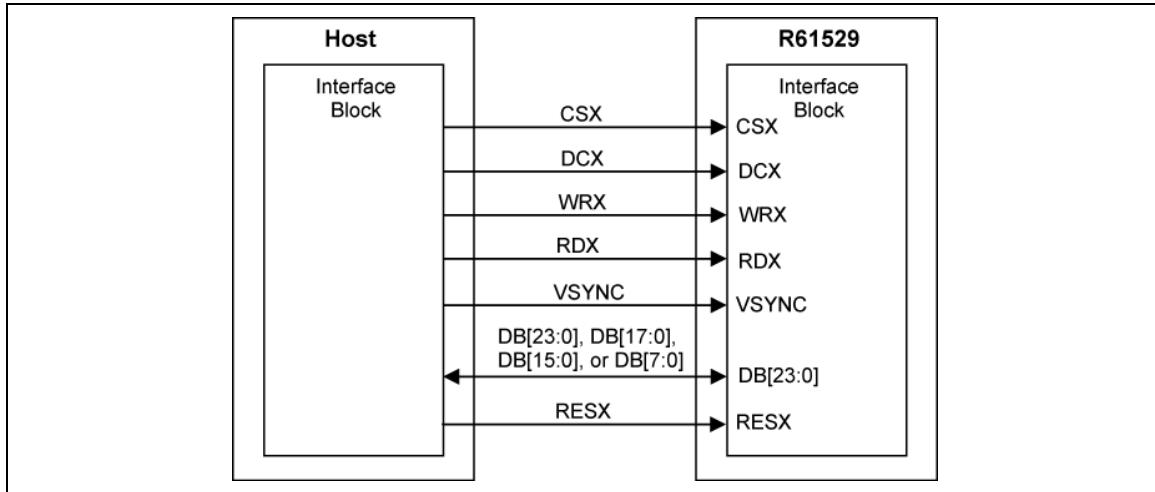


Figure 115

The VSYNC interface is selected by setting DM[1:0] = 10. In VSYNC interface operation, the internal display operation is synchronized with the VSYNC signal. By writing data to the internal RAM at faster than the calculated minimum speed, it becomes possible to rewrite the moving picture data without flickering the display and display a moving picture via MIPI DBI Type B interface.

The display operation is performed in synchronization with the internal clock signal generated from the internal oscillator and the VSYNC signal. The display data is written in the internal RAM so that the R61529 rewrites the data only within the moving picture area and minimize the number of data transfer required for moving picture display.

The VSYNC interface has the minimum for RAM data write speed and internal clock frequency, which must be more than the values calculated from the following formulas, respectively.

OSC clock frequency (fosc) [Hz]

$$= \text{Frame frequency} \times (\text{Display lines (NL)} + \text{Front porch (FP)} + \text{Back porch (BP)}) \times 26 \text{ clocks} \times \text{variance}$$

Minimum speed for RAM writing [Hz]

$$> 320 \times (\text{display lines (NL)} / \{(\text{Back porch (BP)} + \text{Display lines (NL)} - \text{margin}) \times 26 \text{ clocks}\} \times 1/\text{fOSC clock frequency})$$

Note: When RAM write operation is not started right after the falling edge of VSYNC, the time from the falling edge of VSYNC until the start of RAM write operation must also be taken into account.

An example of calculating minimum RAM writing speed and internal clock frequency in VSYNC interface operation is as follows.

[Example]: Base video image display via VSYNC interface

Panel size	320 RGB × 480 lines (NL = 8'hEF: 480 lines)
Total number of lines (NL)	480 lines
Back/front porch	12/4 lines (BP = 4'hC, FP = 4'h4)
Frame frequency	60 Hz

Internal clock frequency (fosc) [Hz]

$$= 60\text{Hz} \times (480 + 12 + 4) \text{ lines} \times 26 \text{ clocks} \times 1.1 / 0.9 = 945.7\text{kHz}$$

- Notes:
1. When setting the internal clock frequency, possible causes of fluctuation must also be taken into consideration. In this example, the internal clock frequency allows for a margin of ±10% for variances and guarantee that display operation is completed within one VSYNC cycle.
 2. This example includes variances attributed to LSI fabrication process and room temperature. Other possible causes of variances, such as differences in external resistors and voltage change are not considered in this example. It is necessary to include a margin for these factors.

Minimum speed for RAM writing [Hz]

$$> 320 \times 480 / \{(12 + 480 - 2) \text{ lines} \times 26 \text{ clocks}\} \times 1/945.7\text{MHz} = 11.4\text{MHz}$$

- Notes:
1. In this example, it is assumed that the R61529 starts writing data in the internal RAM on the falling edge of VSYNC.
 2. There must be at least a margin of 2 lines between the line to which the R61529 has just written data and the line where display operation on the LCD is performed.

In this example, the RAM write operation at a speed of 11.4MHz or more, which starts on the falling edge of VSYNC, guarantees the completion of data write operation in a certain line address before the R61529 starts the display operation of the data written in that line and can write video image data without causing flicker on the display.

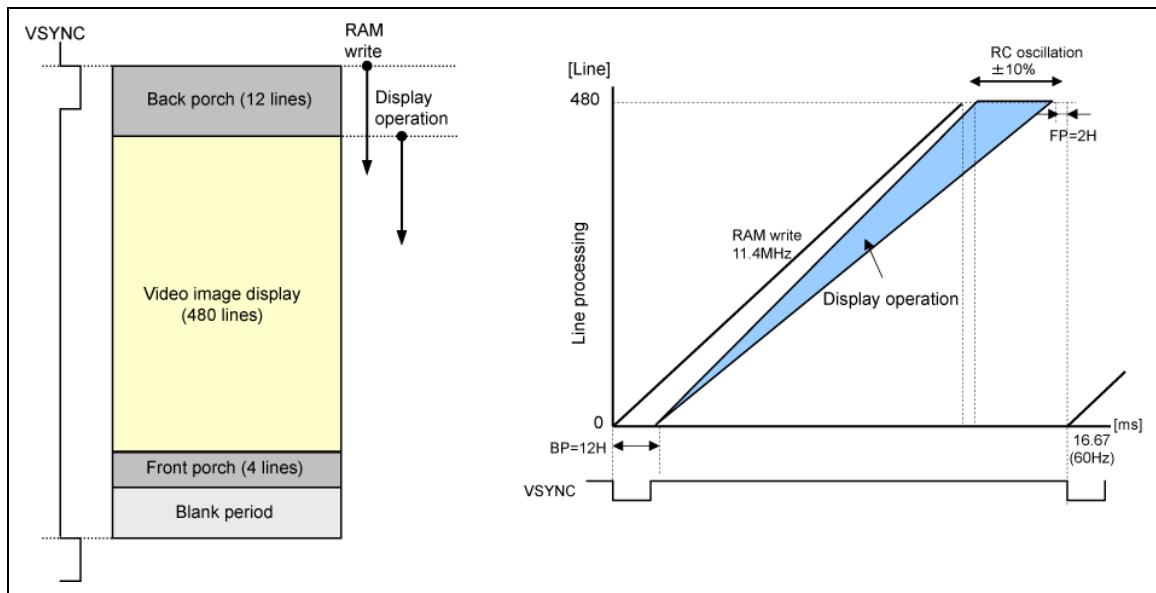


Figure 116 Write Operation via VSYNC Interface

Command List

Table 43 User Command

Operational Code (Hex)	Command	Command (C) /Read (R) /Write(W)	Number Of Parameter	MIPI DCS Type 1 Requirement	R61529 Implementation	Note
00h	nop	C	0	Yes	Yes	
01h	soft_reset	C	0	Yes	Yes	
04h	read_DDB_start	R	5	No	Yes	
06h	get_red_channel	R	1	No	No	
07h	get_green_channel	R	1	No	No	
08h	get_blue_channel	R	1	No	No	
0Ah	get_power_mode	R	1	Yes	Yes (Bits 6/5/4/2 Only)	
0Bh	get_address_mode	R	1	Yes	Yes (Bits 7/6/5/3/0 Only)	
0Ch	get_pixel_format	R	1	Yes	Yes	
0Dh	get_display_mode	R	1	Yes	Yes (Bit 5 Only)	
0Eh	get_signal_mode	R	1	Yes	Yes	
0Fh	get_diagnostic_result	R	1	Bits 7/6: Yes Bits 5/4: Optional	Yes (Bit6 Only)	
10h	enter_sleep_mode	C	0	Yes	Yes	
11h	exit_sleep_mode	C	0	Yes	Yes	
12h	enter_partial_mode	C	0	Yes	Yes	
13h	enter_normal_mode	C	0	Yes	Yes	
20h	exit_invert_mode	C	0	Yes	Yes	
21h	enter_invert_mode	C	0	Yes	Yes	
26h	set_gamma_curve	W	1	Yes	No	
28h	set_display_off	C	0	Yes	Yes	
29h	set_display_on	C	0	Yes	Yes	
2Ah	set_column_address	W	4	Yes	Yes	
2Bh	set_page_address	W	4	Yes	Yes	
2Ch	write_memory_start	W	Variable	Yes	Yes	
2Dh	wite_LUT	W	Variable	Optional	No	
2Eh	read_memory_start	R	Variable	Yes	Yes	

Table 44 User Command (Continued)

Operational Code (Hex)	Command	Command (C) /Read (R) /Write(W)	Number Of Parameter	MIPI DCS Type 1 Requirement	R61529 Implementation	Note
30h	set_partial_area	W	4	Yes	Yes	
33h	set_scroll_area	W	6	Yes	No	
34h	set_tear_off	C	0	Yes	Yes	
35h	set_tear_on	W	1	Yes	Yes	
36h	set_address_mode	W	1	Yes (Bits 7-0)	Yes (Bits 7/6/5/3/0 Only)	
37h	set_scroll_start	W	2	Yes	No	
38h	exit_idle_mode	C	0	Yes	Yes	
39h	enter_idle_mode	C	0	Yes	Yes	
3Ah	set_pixel_format	W	1	Yes	Yes	
3Ch	write_memory_continue	W	Variable	Yes	Yes	
3Eh	read_memory_continue	R	Variable	Yes	Yes	
44h	set_tear_scanline	W	2	Yes	Yes	
45h	get_scanline	R	2	Yes	Yes	
A1h	read_DDB_start	R	5	Yes	Yes (5 th parameter)	
A8h	read_DDB_continue	R	Variable	Yes	No	

Table 45 Manufacturer Command (TBD)

Operational Code (Hex)	Function	Command(C) /Read(R) /Write(W)	Number Of Parameter	Category
B0h	Manufacturer Command Access Protect	W/R	1	Additional User Command
B1h	Low Power Mode Control	W/R	1	Additional User Command
B3h	Frame Memory Access and Interface Setting	W/R	4	Additional User Command
B4h	Display Mode	W/R	1	
B5h	Read Checksum and ECC Error Count	W/R	3	
B6h	DSI Control	W/R	2	
B7h	MDDI Control	W/R	4	
B8h	Backlight Control (1)	W/R	20	
B9h	Backlight Control (2)	W/R	4	
BAh	Backlight Control (3)	R	1	
BFh	Device Code Read	R	5	
C0h	Panel Driving Setting	W/R	8	
C1h	Display V-Timing Setting for Normal Mode	W/R	5	
C3h	Test Mode 1	R	1	
C4h	Source / Gate Driving Timing Control Setting	W/R	4	
C6h	DPI polarity Control	W/R	1	
C7h	Test Mode 2	R	2	
C8h	Gamma Setting A Set	W/R	24	
C9h	Gamma Setting B Set	W/R	24	
CAh	Gamma Setting C Set	W/R	24	
CCh	Test Mode 3	R	1	
D0h	Power Setting (Charge Pump Setting)	W/R	16	
D1h	VCOM Setting	W/R	4	
D6h	Test Mode 4	R	1	
D7h	Test Mode 5	R	15	
D8h	Test Mode 6	R	9	
D9h	Test Mode 7	R	3	
DAh	Test Mode 8	R	1	

Table 46 Manufacturer Command (continued) (TBD)

Operational Code (Hex)	Function	Command(C) /Read(R) /Write(W)	Number Of Parameter	Category
E0h	NVM Access Control	W/R	4	
E1h	set_DDB_write_control	W/R	6	
E2h	NVM Load Control	W/R	1	
E4h	Test Mode 9	R	5	
E5h	Test Mode 10	R	1	
E6h	Test Mode 11	R	1	
E7h	Test Mode 12	R	5	
F3h	Test Mode 13	R	5	
F5h	Read Mode In for DBI Only	C	0	
F6h	Read Mode Out for DBI Only	C	0	
F8h	Test Mode 14	R	1	
FAh	Test Mode 15	R	1	
FCh	Test Mode 16	R	5	
FDh	Test Mode 17	R	13	
FEh	Test Mode 18	R	8	

Command Accessibility

In the default status, only User Commands and Manufacturer Command Access Protect (B0h) can be accessed. Other commands are recognized as “nop”.

Manufacturer Commands except B0h command are accessible by releasing Access Protect. See Command B0h description for details.

Table 47 User Command

Operational Code (Hex) Command		Command Accessibility				
		Normal Mode On Idle Mode Off Sleep Mode Off	Normal Mode On Idle Mode On Sleep Mode Off	Partial Mode On Idle Mode Off Sleep Mode Off	Partial Mode On Idle Mode On Sleep Mode Off	Sleep Mode On
00h	nop	Yes	Yes	Yes	Yes	Yes
01h	soft_reset	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
04h	read_DDB_start	Yes	Yes	Yes	Yes	Yes
0Ah	get_power_mode	Yes	Yes	Yes	Yes	Yes
0Bh	get_address_mode	Yes	Yes	Yes	Yes	Yes
0Ch	get_pixel_format	Yes	Yes	Yes	Yes	Yes
0Dh	get_display_mode	Yes	Yes	Yes	Yes	Yes
0Eh	get_signal_mode	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
0Fh	get_diagnostic_result	Yes	Yes	Yes	Yes	Yes
10h	enter_sleep_mode	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
11h	exit_sleep_mode	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
12h	enter_partial_mode	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
13h	enter_normal_mode	Yes	Yes	Yes	Yes	Yes
20h	exit_invert_mode	Yes	Yes	Yes	Yes	Yes
21h	enter_invert_mode	Yes	Yes	Yes	Yes	Yes
28h	set_display_off	Yes	Yes	Yes	Yes	Yes
29h	set_display_on	Yes	Yes	Yes	Yes	Yes
2Ah	set_column_address	Yes	Yes	Yes	Yes	Yes
2Bh	set_page_address	Yes	Yes	Yes	Yes	Yes
2Ch	write_memory_start	Yes	Yes	Yes	Yes	Yes
2Eh	read_memory_start	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes

Table 48 User Command (continued)

Operational Code (Hex) Command		Command Accessibility				
		Normal Mode On Idle Mode Off Sleep Mode Off	Normal Mode On Idle Mode On Sleep Mode Off	Partial Mode On Idle Mode Off Sleep Mode Off	Partial Mode On Idle Mode On Sleep Mode Off	Sleep Mode On
30h	set_partial_area	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
34h	set_tear_off	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
35h	set_tear_on	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
36h	set_address_mode	Yes	Yes	Yes	Yes	Yes
38h	exit_idle_mode	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
39h	enter_idle_mode	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
3Ah	set_pixel_format	Yes	Yes	Yes	Yes	Yes
3Ch	write_memory_continue	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
3Eh	read_memory_continue	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
44h	set_tear_scanline	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	Yes
45h	get_scanline	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	DM=0 (Note)	No
A1h	read_DDB_start	Yes	Yes	Yes	Yes	Yes

Note: Command may be accessed only when DM = 0 (display operation is in synchronization with internal oscillation clock). To access these commands is disabled when DM = 1 and DPI is selected.

Table 49 Manufacturer Command (TBD)

Operational Code (Hex) Command		Command Accessibility				
		Normal Mode On Idle Mode Off Sleep Mode Off	Normal Mode On Idle Mode On Sleep Mode Off	Partial Mode On Idle Mode Off Sleep Mode Off	Partial Mode On Idle Mode On Sleep Mode Off	Sleep Mode On
B0h	Manufacturer Command Access Protect	Yes	Yes	Yes	Yes	Yes
B1h	Low Power Mode Control	No	No	No	No	Yes
B3h	Frame Memory Access and Interface Setting	Yes	Yes	Yes	Yes	Yes
B4h	Display Mode	Yes	Yes	Yes	Yes	Yes
B5h	Read Checksum and ECC Error Count	Yes	Yes	Yes	Yes	Yes
B6h	DSI Control	Yes	Yes	Yes	Yes	Yes
B7h	MDDI Control	Yes	Yes	Yes	Yes	Yes
B8h	Backlight Control (1)	Yes	Yes	Yes	Yes	Yes
B9h	Backlight Control (2)	Yes	Yes	Yes	Yes	Yes
BAh	Backlight Control (3)	Yes	Yes	Yes	Yes	No
BFh	Device Code Read	Yes	Yes	Yes	Yes	Yes
C0h	Panel Driving Setting	Yes	Yes	Yes	Yes	Yes
C1h	Display V-Timing Setting for Normal Mode	Yes	Yes	Yes	Yes	Yes
C3h	Test Mode 1	No	No	No	No	No
C4h	Source / Gate Driving Timing Control Setting	Yes	Yes	Yes	Yes	Yes
C6h	DPI Polarity Control	Yes	Yes	Yes	Yes	Yes
C7h	Test Mode 2	Yes	Yes	Yes	Yes	Yes
C8h	Gamma Setting A Set	Yes	Yes	Yes	Yes	Yes
C9h	Gamma Setting B Set	Yes	Yes	Yes	Yes	Yes
CAh	Gamma Setting C Set	Yes	Yes	Yes	Yes	Yes
D0h	Power Setting (Charge Pump Setting)	Yes	Yes	Yes	Yes	Yes
D1h	VCOM Setting	Yes	Yes	Yes	Yes	Yes
D6h	Test Mode 4	No	No	No	No	No
D7h	Test Mode 5	No	No	No	No	No
D8h	Test Mode 6	No	No	No	No	No
D9h	Test Mode 7	No	No	No	No	No
DAh	Test Mode 8	No	No	No	No	No

Table 50 Manufacturer Command (continued) (TBD)

Operational Code (Hex) Command		Command Accessibility				
		Normal Mode On Idle Mode Off Sleep Mode Off	Normal Mode On Idle Mode On Sleep Mode Off	Partial Mode On Idle Mode Off Sleep Mode Off	Partial Mode On Idle Mode On Sleep Mode Off	Sleep Mode On
E0h	NVM Access Control	Yes	Yes	Yes	Yes	No
E1h	set_DDB_write_control	Yes	Yes	Yes	Yes	Yes
E2h	NVM Load Control	Yes	Yes	Yes	Yes	Yes
E4h	Test Mode 9	No	No	No	No	No
E5h	Test Mode 10	No	No	No	No	No
E6h	Test Mode 11	No	No	No	No	No
E7h	Test Mode 12	No	No	No	No	No
F3h	Test Mode 13	No	No	No	No	No
F5h	Read Mode In for DBI Only	Yes (Note)	Yes (Note)	Yes (Note)	Yes (Note)	Yes (Note)
F6h	Read Mode Out for DBI Only	Yes (Note)	Yes (Note)	Yes (Note)	Yes (Note)	Yes (Note)
F8h	Test Mode 14	No	No	No	No	No
FAh	Test Mode 15	No	No	No	No	No
FCh	Test Mode 16	No	No	No	No	No
FDh	Test Mode 17	No	No	No	No	No
FEh	Test Mode 18	No	No	No	No	No

Note: F5h and F6h commands can be used only in DBI Type C operation.

Default Modes and Values

Table 51 User Command

Operational Code (Hex)	Command	Parameters	Default Modes and Values(Hex)		
			After Power-on	After SW Reset	After HW Reset
00h	nop	None	N/A	N/A	N/A
01h	soft_reset	None	N/A	N/A	N/A
04h	read_DDB_start	1st	MS byte of Supplier ID (Note2)	MS byte of Supplier ID (Note2)	MS byte of Supplier ID (Note2)
		2nd	LS byte of Supplier ID (Note2)	LS byte of Supplier ID (Note2)	LS byte of Supplier ID (Note2)
		3rd	MS byte of Supplier Elective Data (Note2)	MS byte of Supplier Elective Data (Note2)	MS byte of Supplier Elective Data (Note2)
		4th	LS byte of Supplier Elective Data (Note2)	LS byte of Supplier Elective Data (Note2)	MS byte of Supplier Elective Data (Note2)
		5th	IFID (Note 2)	IFID (Note 2)	IFID (Note 2)
		6th	FFh	FFh	FFh
0Ah	get_power_mode	1st	08h	08h	08h
0Bh	get_address_mode	1st	00h	No Change (Note1)	00h
0Ch	get_pixel_format	1st	77h	77h	77h
0Dh	get_display_mode	1st	00h	00h	00h
0Eh	get_signal_mode	1st	00h	00h	00h
0Fh	get_diagnostic_result	1st	00h	00h	00h
10h	enter_sleep_mode	None	Sleep Mode On	Sleep Mode On	Sleep Mode On
11h	exit_sleep_mode	None	Sleep Mode On	Sleep Mode On	Sleep Mode On
12h	enter_partial_mode	None	Normal Display Mode On	Normal Display Mode On	Normal Display Mode On
13h	enter_normal_mode	None	Normal Display Mode On	Normal Display Mode On	Normal Display Mode On
20h	exit_invert_mode	None	Invert Mode Off	Invert Mode Off	Invert Mode Off
21h	enter_invert_mode	None	Invert Mode Off	Invert Mode Off	Invert Mode Off
28h	set_display_off	None	Display Off	Display Off	Display Off
29h	set_display_on	None	Display Off	Display Off	Display Off

Table 52 User Command (continued)

Operational Code (Hex)	Command	Parameters	Default Modes and Values(Hex)		
			After Power-on	After SW Reset	After HW Reset
2Ah	set_column_address	1st/2nd SC[9:0]	000h	000h	000h
		3rd/4th EC[9:0]	13F	If set_address_mode B5=0: 13F B5=1: 1DF	13F
2Bh	set_page_address	1st/2nd SP[9:0]	000h	000h	000h
		3rd/4th EP[9:0]	1DF	If set_address_mode B5=0 : 1DF B5=1 : 13F	1DF
2Ch	write_memory_start	All	Random Values	Not Cleared	Not Cleared
2Eh	read_memory_start	All	Random Values	Not Cleared	Not Cleared
30h	set_partial_area	1st/2nd SR[9:0]	000h	000h	000h
		3rd/4th ER[9:0]	1DF	1DF	1DF
34h	set_tear_off	6	TE line output Off	TE line output Off	TE line output Off
35h	set_tear_on	1st	TE line output Off	TE line output Off	TE line output Off
36h	set_address_mode	1st	00h	No Change (Note1)	00h
38h	exit_idle_mode	None	Idle Mode Off	Idle Mode Off	Idle Mode Off
39h	enter_idle_mode	None	Idle Mode Off	Idle Mode Off	Idle Mode Off
3Ah	set_pixel_format	1st	77h	77h	77h
3Ch	write_memory_continue	All	Random Values	Not Cleared	Not Cleared
3Eh	read_memory_continue	All	Random Values	Not Cleared	Not Cleared
44h	set_tear_scanline	1st/2nd STS[9:0]	000h	000h	000h
45h	get_scanline	1st/2nd GTS[9:0]	000h (invalid)	000h (invalid)	000h (invalid)

Table 53 User Command (continued)

Operational Code (Hex)	Command	Parameters	Default Modes and Values(Hex)		
			After Power-on	After SW Reset	After HW Reset
A1h	read_DDB_start	1st	MS byte of Supplier ID (Note2)	MS byte of Supplier ID (Note2)	MS byte of Supplier ID (Note2)
		2nd	LS byte of Supplier ID (Note2)	LS byte of Supplier ID (Note2)	LS byte of Supplier ID (Note2)
		3rd	MS byte of Supplier Elective Data (Note2)	MS byte of Supplier Elective Data (Note2)	MS byte of Supplier Elective Data (Note2)
		4th	LS byte of Supplier Elective Data (Note2)	LS byte of Supplier Elective Data (Note2)	MS byte of Supplier Elective Data (Note2)
		5th	IFID (Note 2)	IFID (Note 2)	IFID (Note 2)
		6th	FFh	FFh	FFh

Notes:

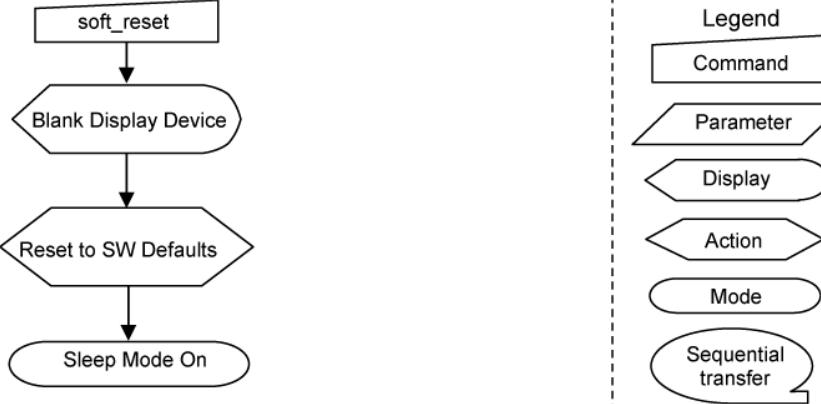
1. No change from the value before soft_reset command.

2. Data are loaded from internal NVM. If user writes VCM register value, Supplier ID, and Supplier Elective Data to the NVM, the values are set to default.

User Command**nop: 00h**

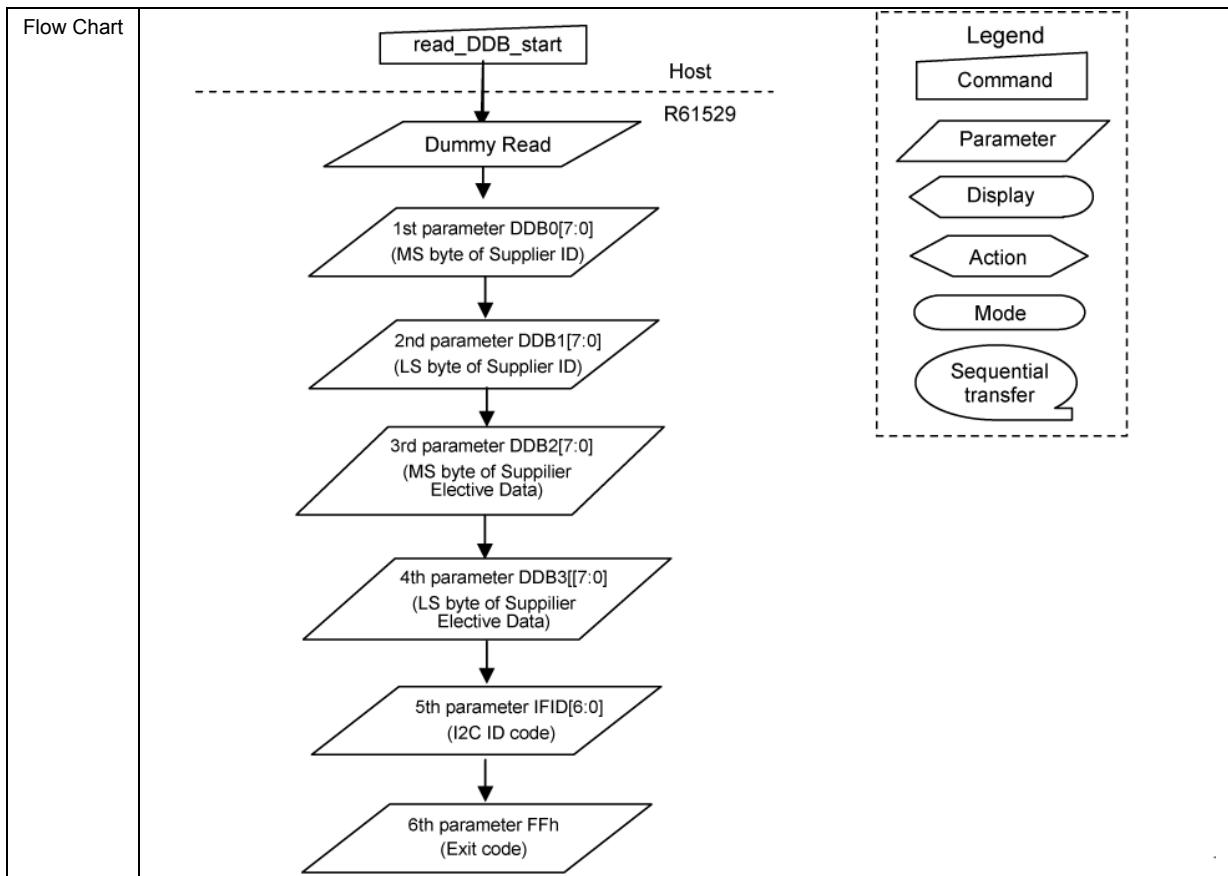
nop												
00h	Direction	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	H→D	0	X	0	0	0	0	0	0	0	0	00h
Parameter	None											
Description	This command is an empty command. It has no effect on the display module. It can be used to terminate frame memory write or read. X = Don't care											
Restriction	-											
Flow Chart	-											

soft_reset: 01h

01h		soft_reset										
	Direction	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	H→D	0	X	0	0	0	0	0	0	0	1	01h
Parameter	None											
Description	When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values (See "Default Modes and Values") X = Don't care											
Restriction	If a soft_reset is sent when the display module is not in Sleep Mode, the host processor must wait 5 frames before sending an exit_sleep_mode command. soft_reset shall not be sent during exit_sleep_mode sequence. No new command setting is allowed until the R61529 enters the Sleep Mode. See "State Transition Diagram" for the sequence to enter Sleep Mode.											
Flow Chart	 <pre> graph TD Start[soft_reset] --> Blank{Blank Display Device} Blank --> Reset{Reset to SW Defaults} Reset --> Sleep{Sleep Mode On} </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 											

read_DDB_start: 04h

04h		read_DDB_start											
		Direction	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command		H→D	0	X	0	0	0	0	0	1	0	0	04h
Dummy parameter		D→H	1	X	X	X	X	X	X	X	X	X	XXh
1 st parameter		D→H	1	X	DDB0 [7]	DDB0 [6]	DDB0 [5]	DDB0 [4]	DDB0 [3]	DDB0 [2]	DDB0 [1]	DDB0 [0]	XXh
2 nd parameter		D→H	1	X	DDB1 [7]	DDB1 [6]	DDB1 [5]	DDB1 [4]	DDB1 [3]	DDB1 [2]	DDB1 [1]	DDB1 [0]	XXh
3 rd parameter		D→H	1	X	DDB2 [7]	DDB2 [6]	DDB2 [5]	DDB2 [4]	DDB2 [3]	DDB2 [2]	DDB2 [1]	DDB2 [0]	XXh
4 th parameter		D→H	1	X	DDB3 [7]	DDB3 [6]	DDB3 [5]	DDB3 [4]	DDB3 [3]	DDB3 [2]	DDB3 [1]	DDB3 [0]	XXh
5 th parameter		D→H	1	X	0	IFID [6]	IFID [5]	IFID [4]	IFID [3]	IFID [2]	IFID [1]	IFID [0]	XXh
6 th parameter		D→H	1	X	1	1	1	1	1	1	1	1	FFh
Description	The command returns information from the display module as follows: 1st parameter (DDB0[7:0]): MS byte of Supplier ID (ID1[15:8]) 2nd parameter (DDB1[7:0]): LS byte of Supplier ID (ID1[7:0]) 3rd parameter (DDB2[7:0]): Supplier Elective Data (ID2[15:8]) 4th parameter (DDB3[7:0]): Supplier Elective Data (ID2[7:0]) 5th parameter: IFID[6:0]: I ² C ID code 6th parameter: FFh Supplier ID and Supplier Elective Data stored in internal NVM are read. X=Don't care												
Restriction	Note: When this command is read via DSI or MDDI, dummy read operation is not performed.												



get_power_mode: 0Ah

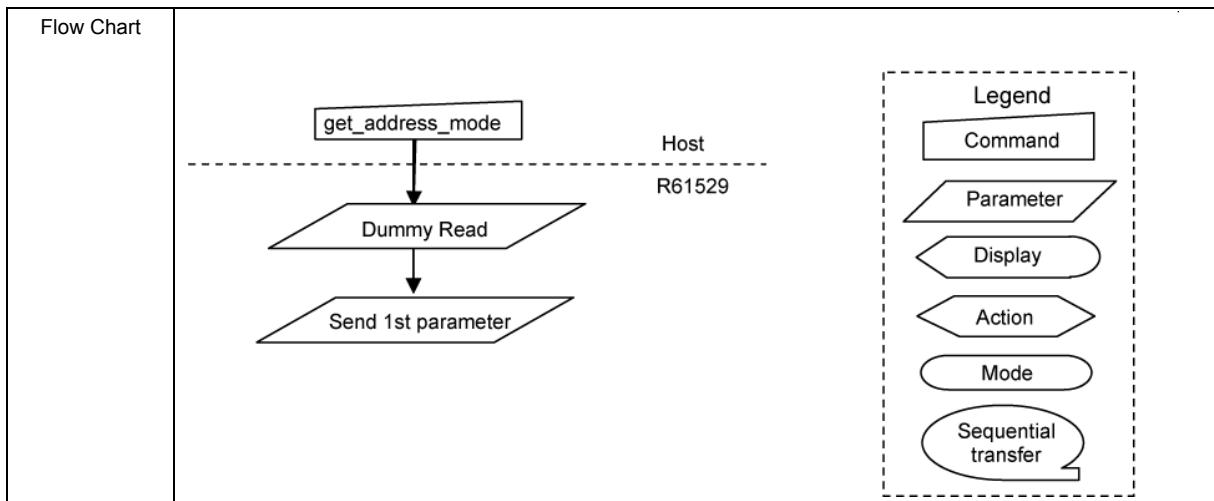
get_power_mode																			
0Ah	Direction	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex							
Command	H→D	0	X	0	0	0	0	1	0	1	0	0Ah							
Dummy parameter	D→H	1	X	X	X	X	X	X	X	X	X	XXh							
1 st parameter	D→H	1	X	0	IDMON	PTLON	SLPOUT	1	DSPON	0	0	XXh							
Description	The display module returns the current power mode as listed below.																		
Bit	Description				Comment		Command list symbol												
D7	Reserved				Set to '0'.		—												
D6	Idle Mode On/Off				-		IDMON												
D5	Partial Mode On/Off				-		PTLON												
D4	Sleep Mode On/Off				-		SLPOUT												
D3	Display Normal Mode On/Off				Set to '1'.		—												
D2	Display On/Off				-		DSPON												
D1	Reserved				Set to '0'.		—												
D0	Reserved				Set to '0'.		—												
• Bit D7 – Reserved	This bit is not applicable. Set to '0'. (Not supported)																		
• Bit D6 – Idle Mode On/Off	'0' = Idle Mode Off '1' = Idle Mode On																		
• Bit D5 – Partial Mode On/Off	'0' = Partial Mode Off '1' = Partial Mode On																		
• Bit D4 – Sleep Mode On/Off	'0' = Sleep Mode On '1' = Sleep Mode Off																		
• Bit D3 – Display Normal Mode On/Off	This bit is not applicable. Set to '1'. (Not supported)																		
• Bit D2 – Display On/Off	'0' = Display is Off. '1' = Display is On.																		
• Bit D1 – Reserved	This bit is not applicable. Set to '0'. (Not supported)																		
• Bit D0 – Reserved	This bit is not applicable. Set to '0'. (Not supported) X = Don't care																		

Restriction	Note: When this command is read via DSI or MDDI, dummy read operation is not performed.	
Flow Chart	<pre> graph TD A[get_power_mode] --> B{Dummy Read} B --> C[Send 1st parameter] style A fill:#fff,stroke:#000 style B fill:#fff,stroke:#000 style C fill:#fff,stroke:#000 style Host fill:#fff,stroke:#000 style Legend fill:#fff,stroke:#000 style Command fill:#fff,stroke:#000 style Parameter fill:#fff,stroke:#000 style Display fill:#fff,stroke:#000 style Action fill:#fff,stroke:#000 style Mode fill:#fff,stroke:#000 style SequentialTransfer fill:#fff,stroke:#000 Host --- B Host --- C Legend --- Command Legend --- Parameter Legend --- Display Legend --- Action Legend --- Mode Legend --- SequentialTransfer </pre>	

get_address_mode: 0Bh

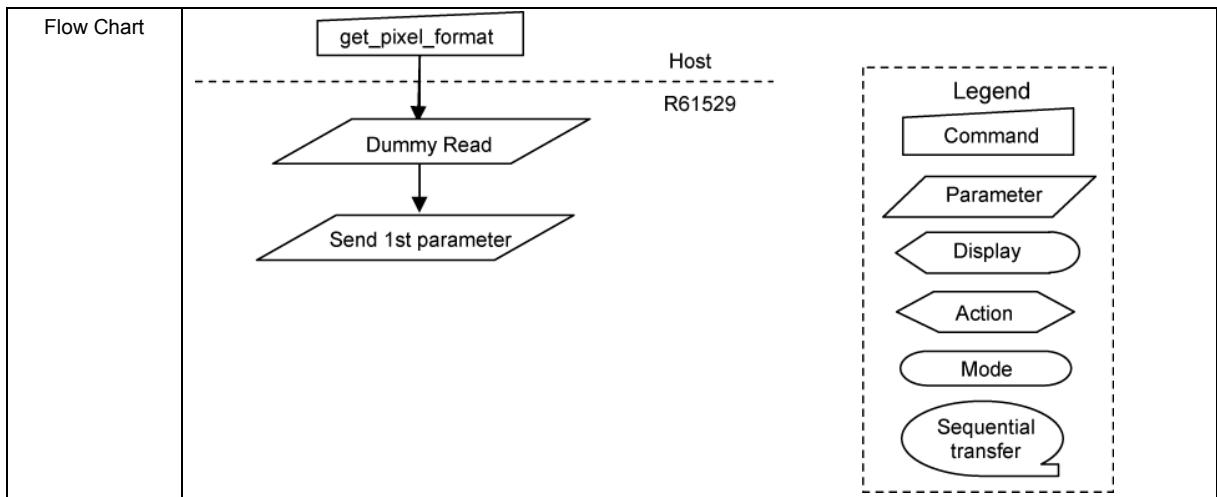
0Bh	get_address_mode											
	Direction	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	H→D	0	X	0	0	0	0	1	0	1	1	0Bh
Dummy parameter	D→H	1	X	X	X	X	X	X	X	X	X	XXh
1 st parameter	D→H	1	X	B7	B6	B5	0	B3	0	0	B0	XXh

Description	<p>The display module returns the current status of the display as described in the table below. This command setting depends on set_address_mode (36h). See "State Transition Diagram" for display mode transition.</p> <table border="1"> <thead> <tr> <th rowspan="2">Bit</th><th rowspan="2">Description</th><th rowspan="2">Comment</th><th colspan="2">Command list symbol</th></tr> <tr> <th>Command mode</th><th>Video mode</th></tr> </thead> <tbody> <tr> <td>D7</td><td>Page Address Order</td><td>-</td><td>B7</td><td>-</td></tr> <tr> <td>D6</td><td>Column Address Order</td><td>-</td><td>B6</td><td>B6</td></tr> <tr> <td>D5</td><td>Page/Column Addressing Order</td><td>-</td><td>B5</td><td>-</td></tr> <tr> <td>D4</td><td>Display Device Line Refresh Order</td><td>Set to '0'.</td><td>-</td><td>-</td></tr> <tr> <td>D3</td><td>RGB/BGR Order</td><td>-</td><td>B3</td><td>B3</td></tr> <tr> <td>D2</td><td>Display Data Latch Data Order</td><td>Set to '0'.</td><td>-</td><td>-</td></tr> <tr> <td>D1</td><td>Flip Horizontal</td><td>Set to '0'.</td><td>-</td><td>-</td></tr> <tr> <td>D0</td><td>Flip Vertical</td><td>-</td><td>B0</td><td>-</td></tr> </tbody> </table> <ul style="list-style-type: none"> Bit D7 – Page Address Order '0' = Top to Bottom (When set_address_mode D7 = '0') '1' = Bottom to Top (When set_address_mode D7 = '1') Bit D6 – Column Address Order '0' = Left to Right (When set_address_mode D6 = '0') '1' = Right to Left (When set_address_mode D6 = '1') Bit D5 – Page/Column Order '0' = Normal Mode '1' = Reverse Mode Bit D4 – Line Address Order This bit is not applicable. Set to '0'. (Not supported) Bit D3 – RGB/BGR Order '0' = RGB (When set_address_mode D3 = '0') '1' = BGR (When set_address_mode D3 = '1') Bit D2 – Display Data Latch Order This bit is not applicable. Set to '0'. (Not supported) Bit D1 – Flip Horizontal This bit is not applicable. Set to '0'. (Not supported) Bit D0 – Flip Vertical '0' = Normal (When set_address_mode D0 = '0') '1' = Flipped (When set_address_mode D0 = '1') <p>X = Don't care</p>					Bit	Description	Comment	Command list symbol		Command mode	Video mode	D7	Page Address Order	-	B7	-	D6	Column Address Order	-	B6	B6	D5	Page/Column Addressing Order	-	B5	-	D4	Display Device Line Refresh Order	Set to '0'.	-	-	D3	RGB/BGR Order	-	B3	B3	D2	Display Data Latch Data Order	Set to '0'.	-	-	D1	Flip Horizontal	Set to '0'.	-	-	D0	Flip Vertical	-	B0	-
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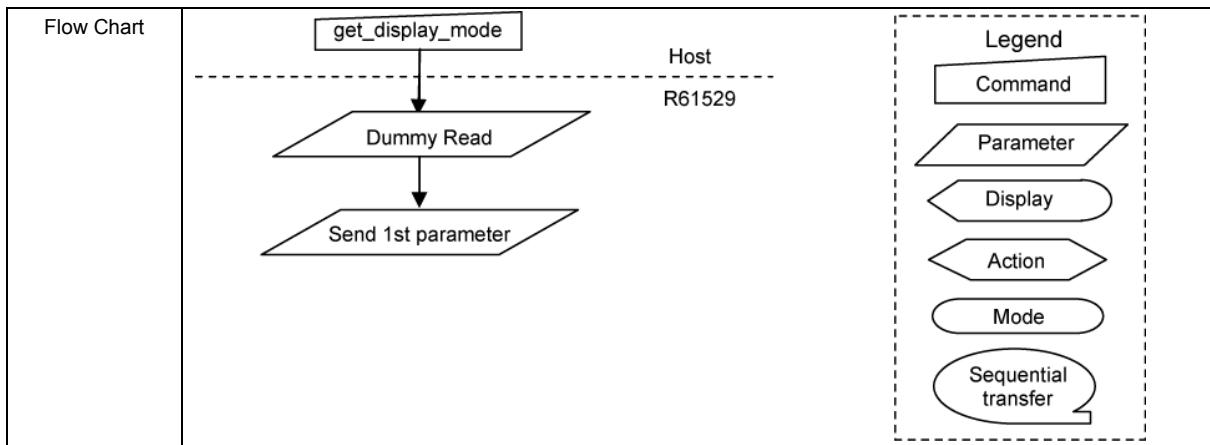
get_pixel_format: 0Ch

get_pixel_format																																																																												
0Ch	Direction	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex																																																																
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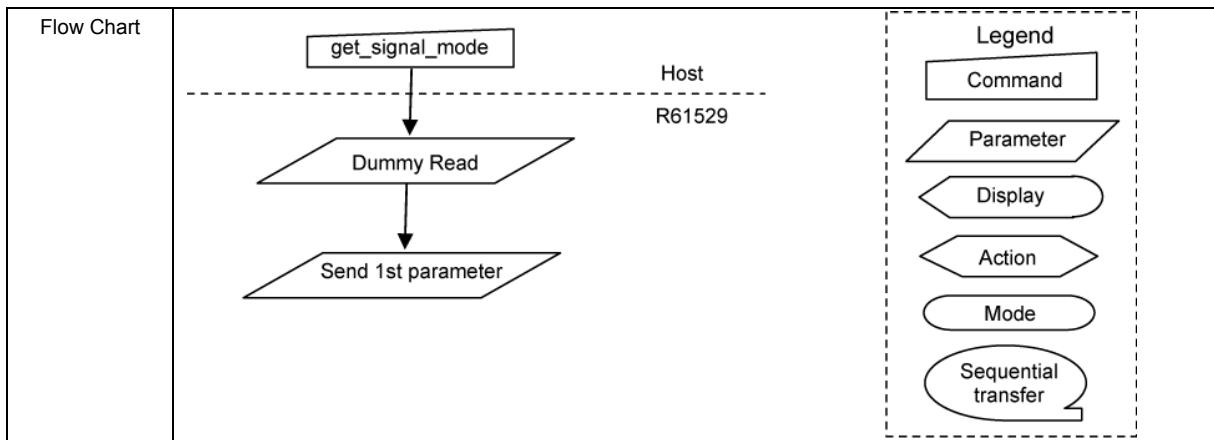
get_display_mode: 0Dh

get_display_mode																																															
0Dh	Direction	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex																																			
Command	H→D	0	X	0	0	0	0	1	1	0	1	0Dh																																			
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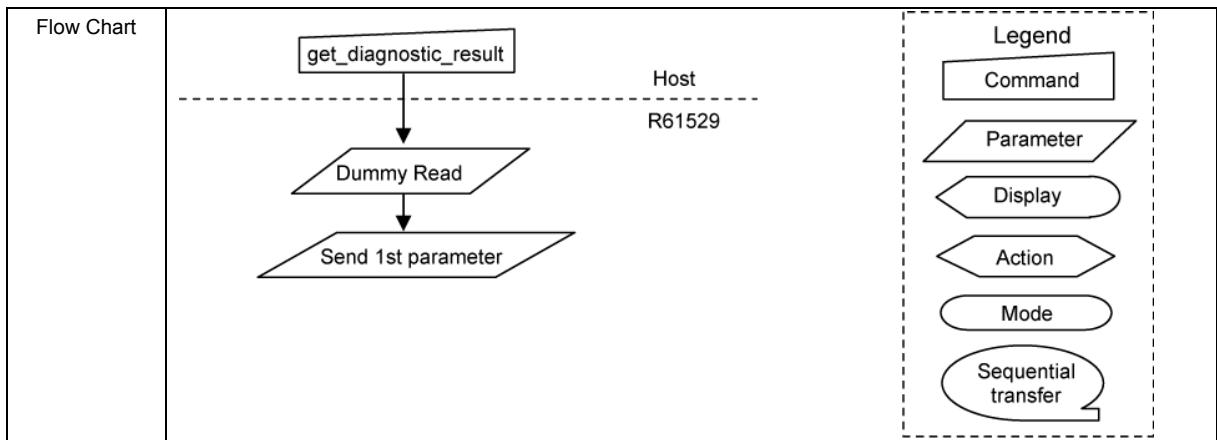
get_signal_mode: 0Eh

0Eh		get_signal_mode																																																																																																																																
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get_diagnostic_result: 0Fh

get_diagnostic_result																																																																																					
0Fh	Direction	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex																																																																									
Command	H→D	0	X	0	0	0	0	1	1	1	1	0Fh																																																																									
Dummy parameter	D→H	1	X	X	X	X	X	X	X	X	X	XXh																																																																									
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enter_sleep_mode: 10h

enter_sleep_mode												Hex
10h	Direction	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	H→D	0	X	0	0	0	1	0	0	0	0	10h
Parameter	None											
Description	<p>This command causes the LCD module to enter the Sleep mode. In this mode, the step-up circuit, internal oscillator and panel scanning stop. In Sleep mode, the frame memory contents remain unchanged.</p> <p>See State Transition Diagram for each stage of transition.</p> <p>X = Don't care</p>											
Restriction	<p>This command has no effect when the module is already in Sleep mode. Sleep mode can be exited only when the exit_sleep_mode (11h) is transmitted.</p> <p>Sending a new command is prohibited while the R61529 performs either display off sequence or power off sequence. Using DSI Data Type (22h and 32h) with DCS commands (10h, 11h, 28h, or 29h) is prohibited.</p>											
Flow Chart	<pre> graph TD AnyMode([Any Mode]) --> EnterSleepMode[enter_sleep_mode] EnterSleepMode --> BlankDisplayDevice{Blank Display Device} BlankDisplayDevice --> PowerOffDisplayDevice{Power Off Display Device} PowerOffDisplayDevice --> SleepMode([Sleep Mode]) EnterSleepMode --> StopPowerSupply{Stop Power Supply} StopPowerSupply --> StopInternalOscillator{Stop Internal Oscillator} StopInternalOscillator --> SleepMode subgraph Legend [Legend] Command[Command] Parameter[Parameter] Display[Display] Action[Action] Mode[Mode] SequentialTransfer[Sequential transfer] end </pre>											

exit_sleep_mode: 11h

11h		exit_sleep_mode										
	Direction	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	H→D	0	X	0	0	0	1	0	0	0	1	11h
Parameter	None											
Description	<p>This command causes the display module to exit Sleep mode. The step-up circuit, internal oscillator, and panel scanning start.</p> <p>See State Transition Diagram for each stage of transition.</p> <p>X = Don't care</p>											
Restriction	<p>This command shall not cause any visual effect on display device when the display module is not in Sleep mode.</p> <p>No new command setting is allowed during power ON sequence. Operation may continue for more than 6 frame periods due to power ON sequence setting. Do not send any command either in this case.</p> <p>The host processor must wait 5 frame periods after sending an enter_sleep_mode command before sending an exit_sleep_mode command.</p> <p>The display runs the self-diagnostic function after this command is received.</p> <p>Using DSI Data Type (22h and 32h) with DCS commands (10h, 11h, 28h, or 29h) is prohibited.</p>											
Flow Chart	<pre> graph TD Start((Sleep Mode)) --> Exit[exit_sleep_mode] Exit --> PowerOn{Power On Display Device} PowerOn --> Blank[Blank Display Device] Blank --> Display[Display Memory contents] Display --> End((Sleep Mode Off)) </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 											

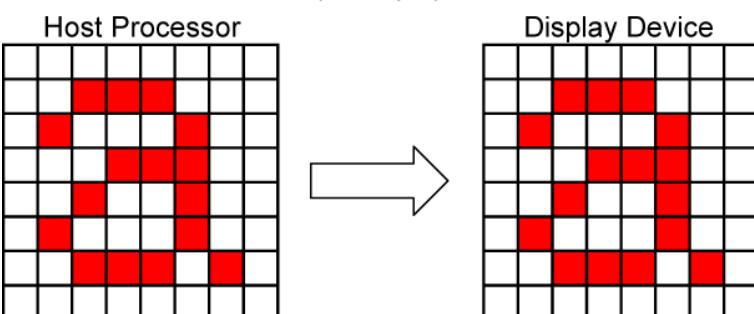
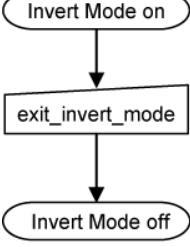
enter_partial_mode: 12h

enter_partial_mode												
12h	Direction	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	H→D	0	x	0	0	0	1	0	0	1	0	12h
Parameter	None											
Description	<p>This command causes the display module to enter the Partial Display Mode. The Partial Display Mode window is described by the set_partial_area command (30h). To leave Partial Display Mode, the enter_normal_mode (13h) should be written.</p> <p>X = Don't care</p> <p>Note: When a command breaks in the middle of frame period in Normal mode, the command is enabled from the next frame period.</p>											
Restriction	This command has no effect when the module is already in Partial mode.											
Flow Chart	See "set_partial_area (30h)".											

enter_normal_mode: 13h

enter_normal_mode												
13h	Direction	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	H→D	0	x	0	0	0	1	0	0	1	1	13h
Parameter	None											
Description	This command causes the display module to enter the Normal mode. Normal Mode means Partial mode is off. X = Don't care Note: When a command breaks in the middle of frame period in Partial mode, that command becomes valid from the next frame period.											
Restriction	This command has no effect when Normal mode is already active.											
Flow Chart	See the description of command set_partial_area (30h) when using this command.											

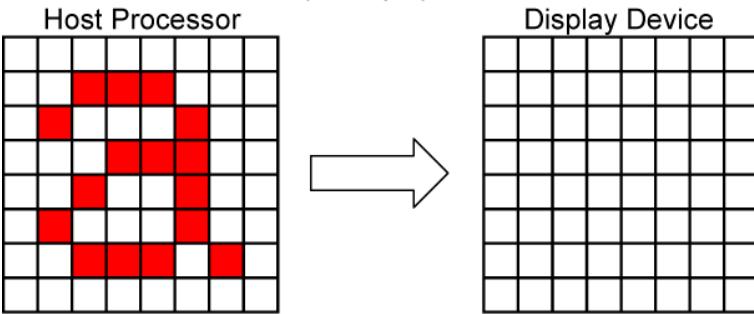
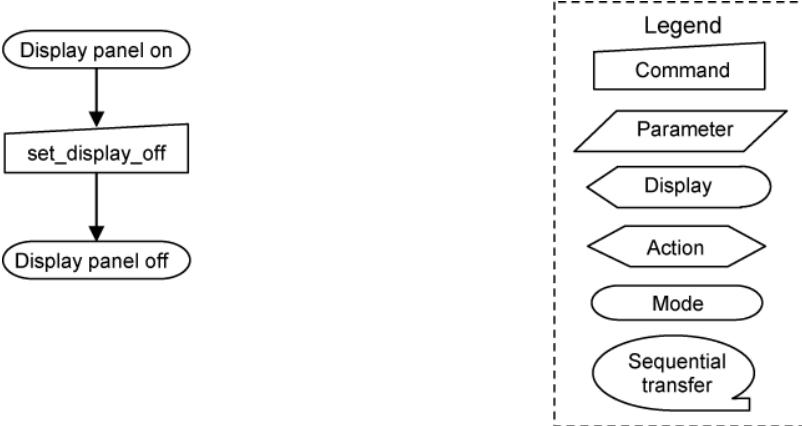
exit_invert_mode: 20h

20h		exit_invert_mode										
	Direction	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	H→D	0	X	0	0	1	0	0	0	0	0	20h
Parameter	None											
Description	This command causes the display module to stop inverting the image data on the display device. The frame memory contents remain unchanged. No status bits are changed. (Example)											
	 <p>X = Don't care</p>											
Restriction	This command has no effect when the module is already in inversion off mode.											
Flow Chart	 <pre> graph TD A([Invert Mode on]) --> B[exit_invert_mode] B --> C([Invert Mode off]) </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 											

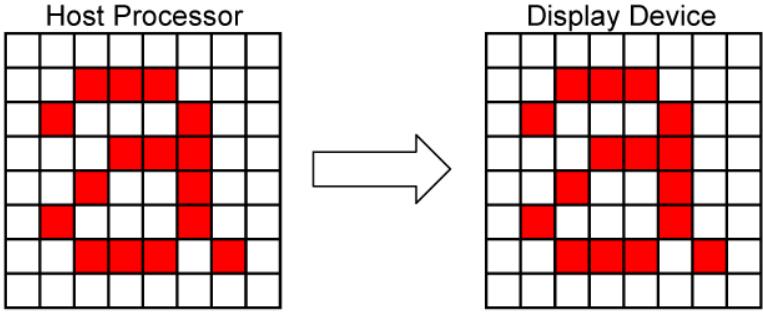
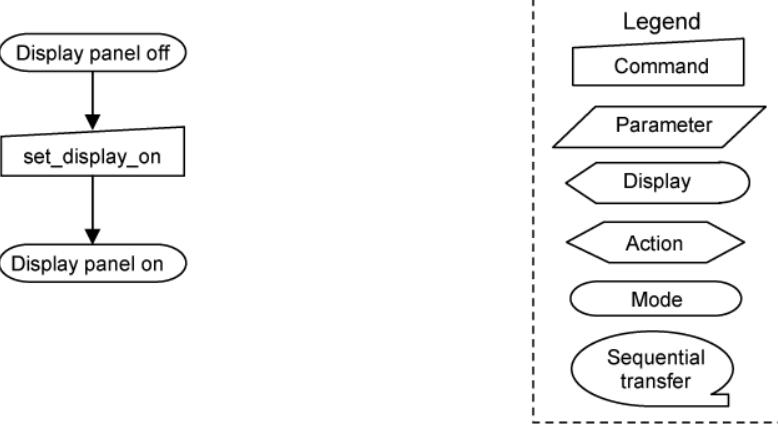
enter_invert_mode: 21h

enter_invert_mode												
21h	Direction	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	H→D	0	X	0	0	1	0	0	0	0	1	21h
Parameter	None											
Description	This command causes the display module to invert image data only on the display device. The frame memory contents remain unchanged. No status bits are changed.											
	(Example)											
	<p>X = Don't care</p>											
Restriction	This command has no effect when the display module is already inverting the display image. This command disables BLC functions.											
Flow Chart	<pre> graph TD A([Invert Mode off]) --> B[enter_invert_mode] B --> C([Invert Mode on]) </pre> <div style="border: 1px dashed black; padding: 5px; margin-top: 10px;"> Legend <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer </div>											

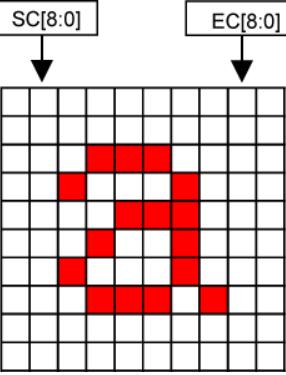
set_display_off: 28h

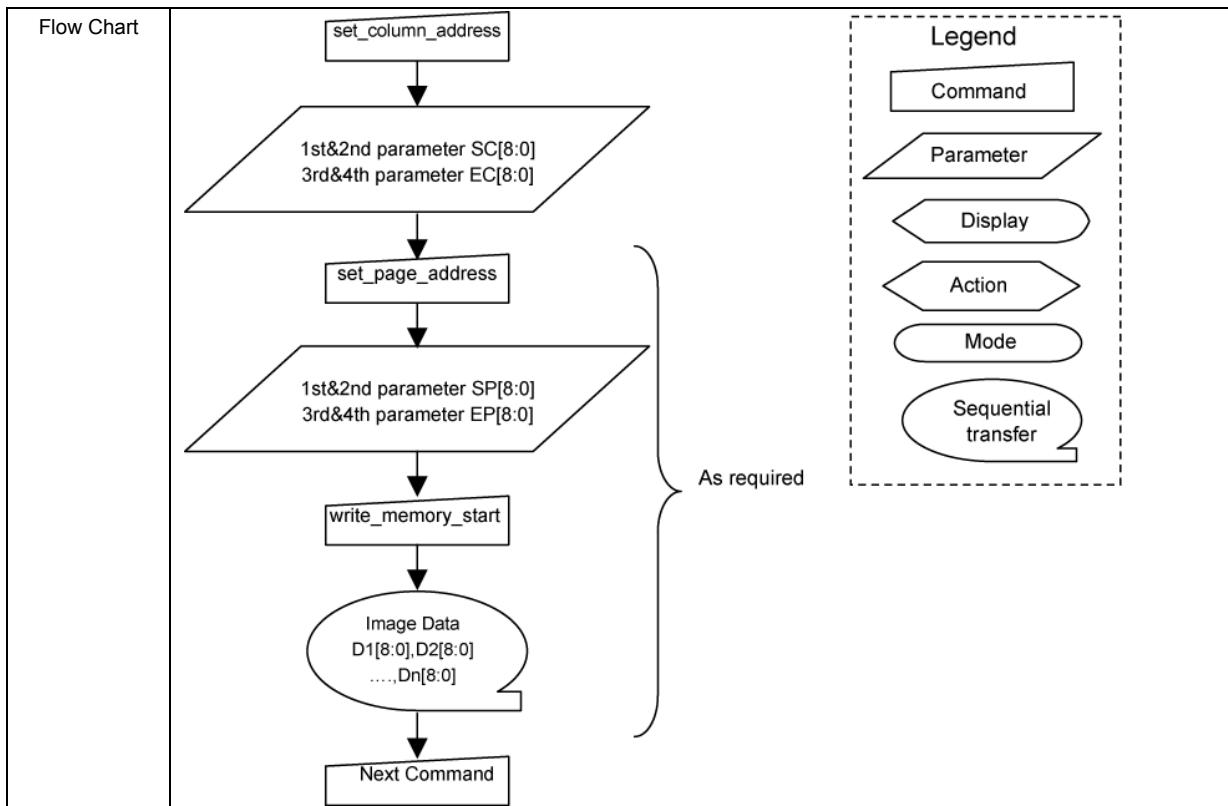
28h	set_display_off											
	Direction	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	H→D	0	X	0	0	1	0	1	0	0	0	28h
Parameter	None											
Description	This command causes the display module to stop displaying image data on the display device. The frame memory contents remain unchanged. No status bits are changed.											
	(Example)											
	 <p style="text-align: center;">Host Processor</p> <p style="text-align: center;">Display Device</p> <p style="text-align: center;">X = Don't care</p>											
Restriction	This command has no effect when the display panel is already off. Do not use this command with DSI Data Type (22h and 32h) and DCS commands (10h, 11h, 28h, and 29h).											
Flow Chart	 <pre> graph TD A([Display panel on]) --> B[/set_display_off/] B --> C([Display panel off]) </pre> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 											

set_display_on: 29h

set_display_on												
29h	Direction	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	H→D	0	X	0	0	1	0	1	0	0	1	29h
Parameter	None											
Description	This command causes the display module to start displaying the image data on the display device. The frame memory contents remain unchanged. No status bits are changed.											
	(Example)											
	 <p style="text-align: center;">Host Processor</p> <p style="text-align: center;">Display Device</p> <p style="text-align: center;">X = Don't care</p>											
Restriction	This command has no effect when the display panel is already on. Do not use this command with DSI Data Type (22h and 32h) and DCS commands (10h, 11h, 28h, and 29h).											
Flow Chart	 <pre> graph TD A([Display panel off]) --> B[set_display_on] B --> C([Display panel on]) </pre> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 											

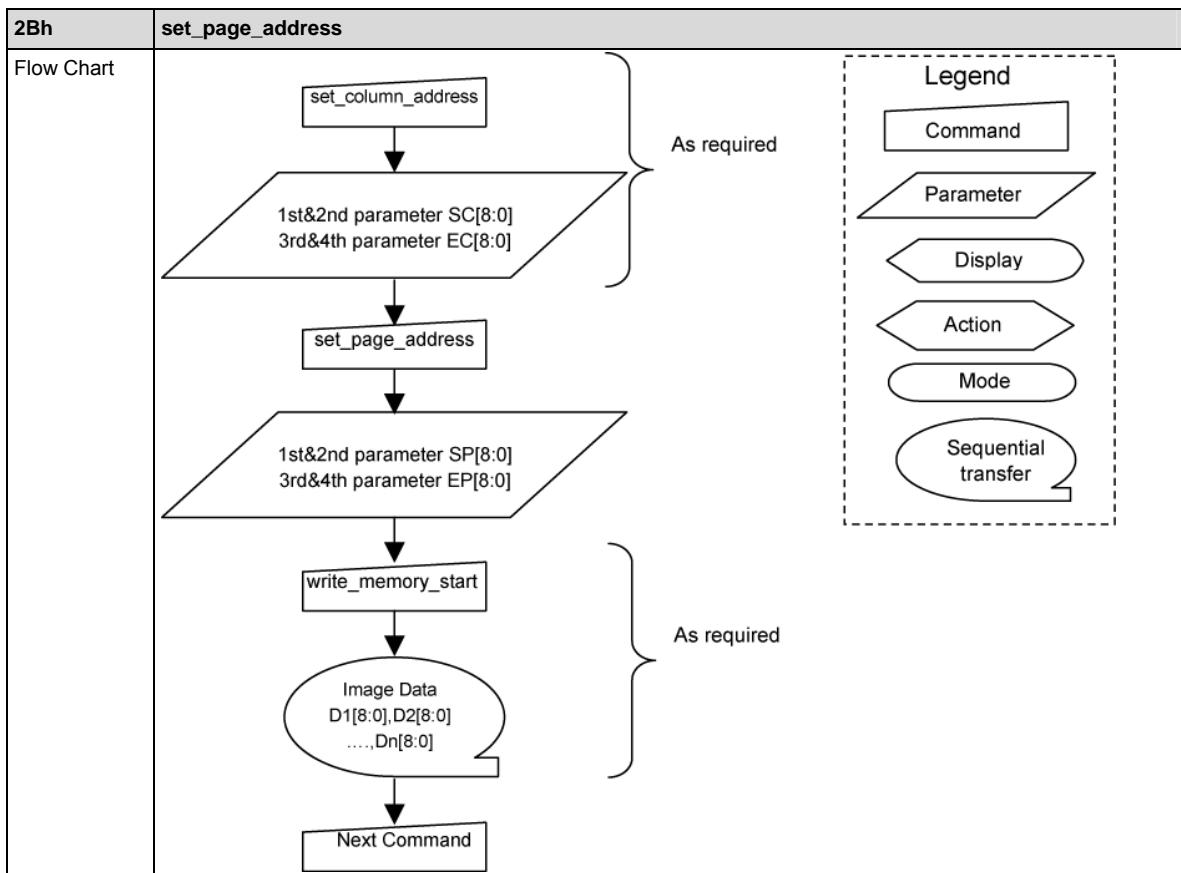
set_column_address: 2Ah

set_column_address												
2Ah	Direction	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	H→D	0	X	0	0	1	0	1	0	1	0	2Ah
1 st parameter	H→D	1	X	0	0	0	0	0	0	0	SC[8]	0Xh
2 nd parameter	H→D	1	X	SC[7]	SC[6]	SC[5]	SC[4]	SC[3]	SC[2]	SC[1]	SC[0]	XXh
3 rd parameter	H→D	1	X	0	0	0	0	0	0	0	EC[8]	0Xh
4 th parameter	H→D	1	X	EC[7]	EC[6]	EC[5]	EC[4]	EC[3]	EC[2]	EC[1]	EC[0]	XXh
Description	<p>This command defines the column extent of the frame memory accessed by the host processor. The values of SC[9:0] and EC[9:0] are referred when write_memory_start (2Ch) and read_memory_start (2Eh) commands are written. No status bits are changed.</p>  <p>X=Don't care</p>											
Restriction	<p>SC [8:0] must be equal to or less than EC[8:0]. Set the 1st parameter B5 in set_address_mode (36h) in advance.</p> <p>Note: The parameters are disregarded in following cases.</p> <ul style="list-style-type: none"> • If set_address_mode B5 = 0: SC[8:0] or EC[8:0] > 13Fh • If set_address_mode B5 = 1: SC[8:0] or EC[8:0] > 1DFh 											



set_page_address: 2Bh

2Bh	set_page_address											
	Direction	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	H→D	0	X	0	0	1	0	1	0	1	1	2Bh
1st parameter	H→D	1	X	0	0	0	0	0	0	0	SP[8]	0Xh
2nd parameter	H→D	1	X	SP[7]	SP[6]	SP[5]	SP[4]	SP[3]	SP[2]	SP[1]	SP[0]	XXh
3rd parameter	H→D	1	X	0	0	0	0	0	0	0	EP[8]	0Xh
4th parameter	H→D	1	X	EP[7]	EP[6]	EP[5]	EP[4]	EP[3]	EP[2]	EP[1]	EP[0]	XXh
Description	<p>This command defines the page extent of the frame memory accessed by the host processor. No status bits are changed.</p> <p>The values of SP[8:0] and EP[8:0] are referred when write_memory_start (2Ch) and read_memory_start (2Eh) commands are written.</p> <p>Example</p> <p>X = Don't care</p>											
Restriction	<p>SP[8:0] must always be equal to or less than EP[8:0]. Set the 1st parameter B5 in set_address_mode (36h) in advance.</p> <p>Note: The parameters are disregarded in following cases.</p> <ul style="list-style-type: none"> • If set_address_mode B5 = 0: SP[8:0] or EP[8:0] > 1DFh • If set_address_mode B5 = 1: SP[8:0] or EP[8:0] > 13Fh 											



write_memory_start: 2Ch

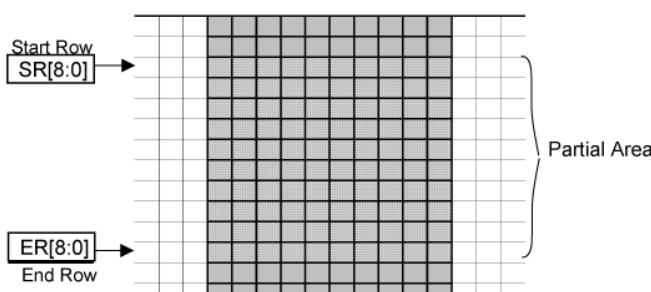
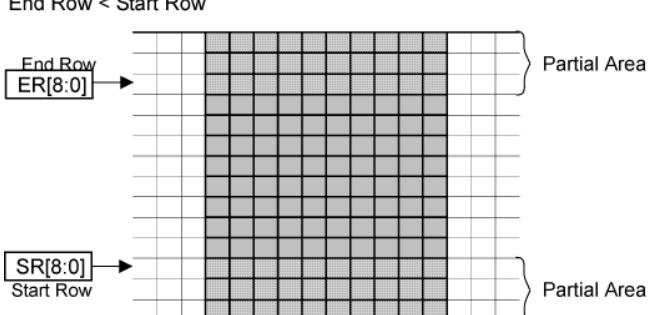
2Ch	write_memory_start											
	Direction	RDX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	H→D	1	X	0	0	1	0	1	1	0	0	2Ch
1st parameter	H→D	1	D1 [23:8]	D1 [7]	D1 [6]	D1 [5]	D1 [4]	D1 [3]	D1 [2]	D1 [1]	D1 [0]	XXXh
:	H→D	1	Dx [23:8]	Dx [7]	Dx [6]	Dx [5]	Dx [4]	Dx [3]	Dx [2]	Dx [1]	Dx [0]	XXXh
Nth parameter	H→D	1	Dn [23:8]	Dn [7]	Dn [6]	Dn [5]	Dn [4]	Dn [3]	Dn [2]	Dn [1]	Dn [0]	XXXh
Description	<p>This command transfers image data from the host processor to the display module's frame memory.</p> <p>No status bits are changed.</p> <p>If this command is received, the column and page registers are set to the Start Column (SC) and Start Page (SP) respectively.</p> <p>After pixel data 1 is stored in frame memory at (SC, SP), address counter's direction differs depending on Bits 5, 6, 7 of set_address_mode (36h). See "Host Processor to Memory Write/Read Direction".</p> <p>If Frame Memory Access and Interface setting (B3h) WEMODE = 0:</p> <p>If the number of pixels in transfer data exceed (EC-SC+1)*(EP-SP+1), the extra pixels are ignored.</p> <p>If Frame Memory Access and Interface setting (B3h) WEMODE = 1</p> <p>When the number of pixels in transfer data exceed (EC-SC+1)*(EP-SP+1), the column register and the page register are set to the Start Column and Start Page respectively. Then subsequent data are written to the frame memory.</p> <p>Sending any other command will stop writing to the frame memory.</p> <p>See DBI Data Format and DSI Data Format for write data formats in DBI Type B 24-/18-/16-/8-bit bus interface and DSI.</p> <p>X=Don't care.</p>											
Restriction	In all color modes, there are no restrictions on the length of parameters. If data is not transferred in units of pixels, the extra data is regarded as invalid.											

2Ch	write_memory_start
Flow Chart	<p>The flowchart illustrates the process of starting memory writes. It begins with a rectangular box labeled "Write_memory_start". An arrow points down to an oval labeled "Image Data" containing the text "D1[23:0], D2[23:0] ... , Dn[23:0]". Another arrow points down from the oval to a rectangular box labeled "Next Command".</p> <p>Legend:</p> <ul style="list-style-type: none">Command (rectangle)Parameter (trapezoid)Display (arrow pointing left)Action (arrow pointing right)Mode (rectangle)Sequential transfer (oval)

read_memory_start: 2Eh

2Eh	read_memory_start											
	Direction	RDX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	H→D	1	X	0	0	1	0	1	1	1	0	2Eh
Dummy parameter	D→H	1	X	X	X	X	X	X	X	X	X	XXh
1st parameter	D→H	1	D1 [23:8]	D1 [7]	D1 [6]	D1 [5]	D1 [4]	D1 [3]	D1 [2]	D1 [1]	D1 [0]	XXXh
:	D→H	1	Dx [23:8]	Dx [7]	Dx [6]	Dx [5]	Dx [4]	Dx [3]	Dx [2]	Dx [1]	Dx [0]	XXXh
Nth parameter	D→H	1	Dn [23:8]	Dn [7]	Dn [6]	Dn [5]	Dn [4]	Dn [3]	Dn [2]	Dn [1]	Dn [0]	XXXh
Description	<p>This command transfers image data from the frame memory to the host processor. No status bits are changed.</p> <p>If this command is received, the column and page registers are set to the Start Column (SC) and Start Page (SP) respectively.</p> <p>After pixel data is read from the frame memory at (SC, SP), address counter's direction differs depending on Bits 5, 6, 7 of set_address_mode (36h). See "Host Processor to Memory Write/Read Direction".</p> <p>If read operation continued after (EP, EC) data are read, the last data (EP, EC) continue to be read.</p> <p>Any other written command stops frame memory read.</p> <p>See DBI Data Format and DSI Data Format for read data formats in DBI Type B 24-/18-/16-/8-bit bus interface and DSI, respectively.</p> <p>X = Don't care.</p>											
Restriction	<p>In all color modes, the Frame read is always 24 bits so there is no restriction on the length of parameters. If data is not transferred in units of pixels, the extra data is regarded as invalid.</p> <p>Note: When this command is read via DSI or MDDI, dummy read operation is not performed.</p>											
Flow Chart	<pre> graph TD A[read_memory_start] --> B{Dummy Read} B --> C([Image Data D1[23:0], D2[23:0], Dn[23:0]]) C --> D[Next Command] style C fill:none,stroke:none style D fill:none,stroke:none %% Legend E[Command] --- F[Parameter] E --- G{Display} E --- H{Action} E --- I[Mode] E --- J([Sequential transfer]) %% Legend </pre>											

set_partial_area: 30h

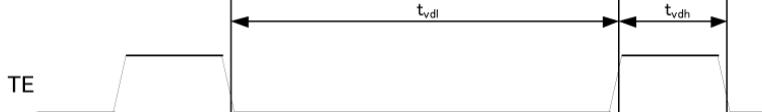
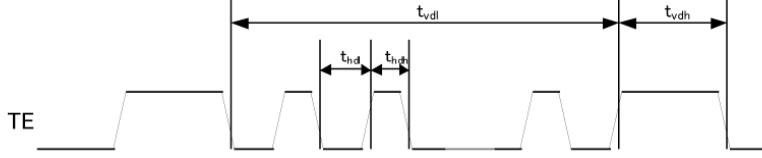
30h	set_partial_area											
	Direction	RDX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	H→D	1	X	0	0	1	1	0	0	0	0	30h
1st parameter	H→D	1	X	0	0	0	0	0	0	0	SR[8]	00h
2nd parameter	H→D	1	X	SR[7]	SR[6]	SR[5]	SR[4]	SR[3]	SR[2]	SR[1]	SR[0]	00h
3rd parameter	H→D	1	X	0	0	0	0	0	0	0	ER[8]	01h
4th parameter	H→D	RDX	X	ER[7]	ER[6]	ER[5]	ER[4]	ER[3]	ER[2]	ER[1]	ER[0]	DFh
Description	<p>This command defines the partial mode's display area. There are 2 parameters associated with this command, the first defines the Start Row (SR) and the second the End Row (ER), as illustrated in the figures below. SR and ER refer to the Frame Memory Line Pointer.</p> <p>End Row > Start Row</p>  <p>End Row < Start Row</p>  <p>If End Row = Start Row, the partial area will be one row deep. X = Don't care.</p>											
Restriction	SR[8:0] and ER[8:0] must not be greater than a value set by NL. The bits other than SR[8:0] and ER[8:0] are "Don't care".											

30h	set_partial_area
Flow Chart	<p>1. To enter partial mode</p> <pre> graph TD AnyMode((Any Mode)) --> SetPartialArea[set_partial_area] SetPartialArea --> SRER{SR[8:0] and ER[8:0]} SRER --> EnterPartialMode[enter_partial_mode] EnterPartialMode --> PartialModeOn((Partial Mode On)) </pre> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer <p>2. To exit partial mode</p> <pre> graph TD PartialModeOn((Partial Mode On)) --> SetDisplayOff[set_display_off] SetDisplayOff --> EnterNormalMode[enter_normal_mode] EnterNormalMode --> NormalModeOn((Normal Mode On)) NormalModeOn --> WriteMemoryStart[write_memory_start] WriteMemoryStart --> ImageData{Image Data D1[23:0], D2[23:0], Dn[23:0]} ImageData --> SetDisplayOn[set_display_on] </pre> <p>Optional (To avoid tearing effect)</p> <p>Enter Normal Mode turns Partial Mode off</p>

set_tear_off: 34h

34h	set_tear_off											
	Direction	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	H→D	0	X	0	0	1	1	0	1	0	0	34h
Parameter	None											
Description	This command turns off the Tearing Effect output signal from the TE signal line. X = Don't care											
Restriction	This command has no effect when Tearing Effect output is already off.											
Flow Chart	<pre> graph TD A([TE output On or Off]) --> B[/set_tear_off/] B --> C([TE output off]) </pre> <p>The flowchart illustrates the sequence of operations. It starts with an oval labeled "TE output On or Off", which points down to a rounded rectangle labeled "set_tear_off". This leads down to another oval labeled "TE output off". To the right of the flowchart is a legend enclosed in a dashed box:</p> <ul style="list-style-type: none"> Legend Command: Box Parameter: Box Display: Parallelogram Action: Double-headed arrow Mode: Oval Sequential transfer: Ellipse 											

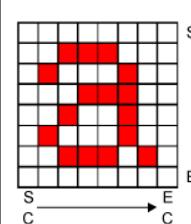
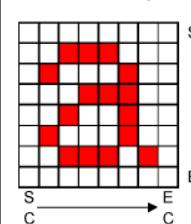
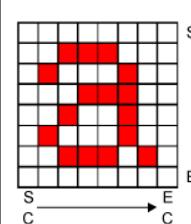
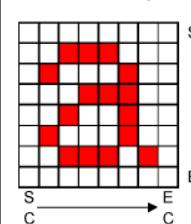
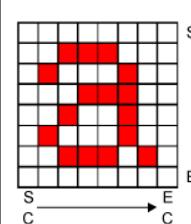
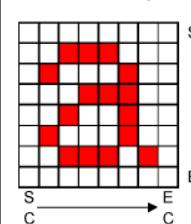
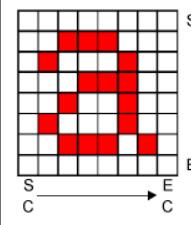
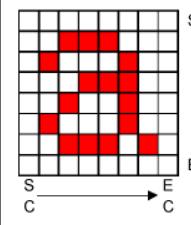
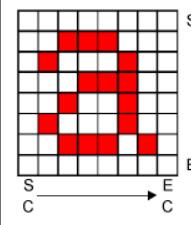
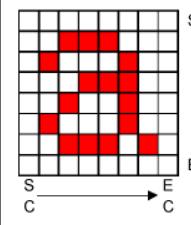
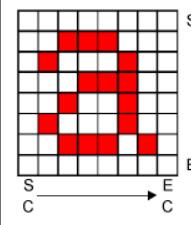
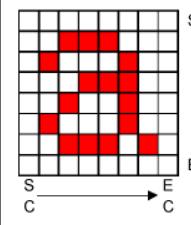
set_tear_on: 35h

35h	set_tear_on											
	Direction	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	H→D	0	X	0	0	1	1	0	1	0	1	35h
Parameter	H→D	1	X	X	X	X	X	X	X	X	TELO M	00h
Description	<p>This command turns on the display module's Tearing Effect output signal on the TE signal line.</p> <p>The Tearing Effect Line On has one parameter, TELON, which describes the Tearing Effect Output Line mode.</p> <p>See TE Pin Output Signal for detail.</p> <p>TELOM = 0: The Tearing Effect Output line consists of V-Blanking information only. The Tearing Effect Output line shall be high during vertical blanking period.</p>  <p>TELOM = 1: The Tearing Effect Output line consists of both V-blanking and H-blanking information.</p>  <p>Vertical blanking period: BP + FP</p> <p>Note 1: The Tearing Effect Output line shall be active low when the display module is in Sleep mode.</p> <p>Note 2: To use DSI TE-report, set TELOM to 0,</p> <p>X = Don't care</p>											
Restriction	This command has no effect when Tearing Effect output is already ON. Changes in parameter TELOM is enabled from the next frame period.											

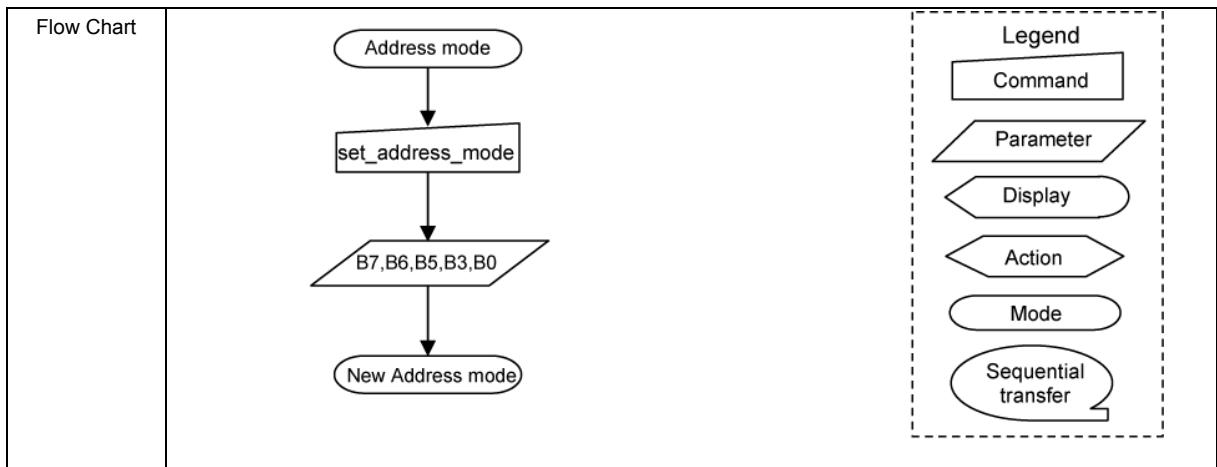
35h	set_tear_on
Flow Chart	<pre> graph TD A([TE output On or Off]) --> B[set_tear_on] B --> C{TEOM} C --> D([TE output On]) </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer

set_address_mode: 36h

set_address_mode																																																													
36h	Direction	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex																																																	
Command	H→D	0	X	0	0	1	1	0	1	1	0	36h																																																	
1st parameter	H→D	1	X	B7	B6	B5	0	B3	0	0	B0	00h																																																	
Description	This command sets read/write scanning direction of frame memory. No status bits are changed.																																																												
	<table border="1"> <thead> <tr> <th>Bit</th> <th>Description</th> <th>Comment</th> <th colspan="2">Symbol</th> </tr> <tr> <th></th> <th></th> <th></th> <th>Command mode</th> <th>Video mode</th> </tr> </thead> <tbody> <tr> <td>D7</td> <td>Page Address Order</td> <td>-</td> <td>B7</td> <td>B7</td> </tr> <tr> <td>D6</td> <td>Column Address Order</td> <td>-</td> <td>B6</td> <td>B6</td> </tr> <tr> <td>D5</td> <td>Page/Column Addressing Order</td> <td>-</td> <td>B5</td> <td>-</td> </tr> <tr> <td>D4</td> <td>Display Device Line Refresh Order</td> <td>Set to '0'.</td> <td>-</td> <td>-</td> </tr> <tr> <td>D3</td> <td>RGB/BGR Order</td> <td>-</td> <td>B3</td> <td>B3</td> </tr> <tr> <td>D2</td> <td>Display Data Latch Data Order</td> <td>Set to '0'.</td> <td>-</td> <td>-</td> </tr> <tr> <td>D1</td> <td>Flip Horizontal</td> <td>Set to '0'.</td> <td>-</td> <td>-</td> </tr> <tr> <td>D0</td> <td>Flip Vertical</td> <td>-</td> <td>B0</td> <td>-</td> </tr> </tbody> </table>			Bit	Description	Comment	Symbol					Command mode	Video mode	D7	Page Address Order	-	B7	B7	D6	Column Address Order	-	B6	B6	D5	Page/Column Addressing Order	-	B5	-	D4	Display Device Line Refresh Order	Set to '0'.	-	-	D3	RGB/BGR Order	-	B3	B3	D2	Display Data Latch Data Order	Set to '0'.	-	-	D1	Flip Horizontal	Set to '0'.	-	-	D0	Flip Vertical	-	B0	-								
Bit	Description	Comment	Symbol																																																										
			Command mode	Video mode																																																									
D7	Page Address Order	-	B7	B7																																																									
D6	Column Address Order	-	B6	B6																																																									
D5	Page/Column Addressing Order	-	B5	-																																																									
D4	Display Device Line Refresh Order	Set to '0'.	-	-																																																									
D3	RGB/BGR Order	-	B3	B3																																																									
D2	Display Data Latch Data Order	Set to '0'.	-	-																																																									
D1	Flip Horizontal	Set to '0'.	-	-																																																									
D0	Flip Vertical	-	B0	-																																																									
	<ul style="list-style-type: none"> Bit D7 – Page Address Order '0' = Top to Bottom. '1' = Bottom to Top. <p>A figure below shows a relationship between frame memory data and display data. For a relationship between input data and display data in Video mode, see "Relationship between Input Data and Display Data."</p>																																																												
	<table border="1"> <thead> <tr> <th></th> <th colspan="2">B7=0</th> <th colspan="2">B7=1</th> </tr> </thead> <tbody> <tr> <td>B6=0 B5=0 B3=X</td> <td></td> <td></td> <td></td> <td></td> </tr> </tbody> </table>													B7=0		B7=1		B6=0 B5=0 B3=X																																											
	B7=0		B7=1																																																										
B6=0 B5=0 B3=X																																																													

Description	<ul style="list-style-type: none"> Bit D6 – Column Address Order <p>'0' = Left to Right. '1' = Right to Left.</p> <p>A figure below shows a relationship between frame memory data and display data. For a relationship between input data and display data in Video mode, see "Relationship between Input Data and Display Data."</p> 						
<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center; width: 25%;">B6=0</th> <th style="text-align: center; width: 25%;">B6=1</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;"> Host Processor B7=0 B5=0 B3=X  </td> <td style="text-align: center;"> Host Processor Frame Memory  </td> </tr> </tbody> </table>				B6=0	B6=1	Host Processor B7=0 B5=0 B3=X 	Host Processor Frame Memory 
B6=0	B6=1						
Host Processor B7=0 B5=0 B3=X 	Host Processor Frame Memory 						
<ul style="list-style-type: none"> Bit D5 – Page/Column Addressing Order <p>'0' = Normal Mode. '1' = Reverse Mode.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center; width: 25%;">B5=0</th> <th style="text-align: center; width: 25%;">B5=1</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;"> Host Processor B7=0 B6=0 B3=X  </td> <td style="text-align: center;"> Host Processor Frame Memory  </td> </tr> </tbody> </table> <p>For bits B7 to B5, see "Frame Memory." Set B5 to 0 when DSI is used (B5 set to 1 is not supported).</p> <ul style="list-style-type: none"> Bit D4 – Display Device Line Refresh Order <p>This bit is not applicable. Set to '0'. (Not supported)</p> 				B5=0	B5=1	Host Processor B7=0 B6=0 B3=X 	Host Processor Frame Memory 
B5=0	B5=1						
Host Processor B7=0 B6=0 B3=X 	Host Processor Frame Memory 						

Description	<ul style="list-style-type: none"> Bit D3 – RGB/BGR Order <p>'0' = RGB. '1' = BGR.</p> <p>A figure below shows a relationship between frame memory data and display data. For a relationship between input data and display data in Video mode, see "Relationship between Input Data and Display Data."</p> <table border="1" data-bbox="393 505 1410 797"> <thead> <tr> <th></th><th>B3=0</th><th>B3=1</th></tr> </thead> <tbody> <tr> <td></td><td> Frame Memory </td><td> Display Device </td></tr> <tr> <td></td><td> Frame Memory </td><td> Display Device </td></tr> </tbody> </table> Bit D2 – Display Data Latch Order <p>This bit is not applicable. Set to '0'. (Not supported)</p> Bit D1 – Flip Horizontal <p>This bit is not applicable. Set to '0'. (Not supported)</p> Bit D0 – Flip Vertical <p>'0' = Normal. '1' = Flipped (Gate scanning direction inverts.).</p> <table border="1" data-bbox="393 1134 1410 1426"> <thead> <tr> <th></th><th>B0=0</th><th>B0=1</th></tr> </thead> <tbody> <tr> <td>B4=0</td><td> Frame Memory </td><td> Display Device </td></tr> <tr> <td></td><td> Frame Memory </td><td> Display Device </td></tr> </tbody> </table> 		B3=0	B3=1		Frame Memory 	Display Device 		Frame Memory 	Display Device 		B0=0	B0=1	B4=0	Frame Memory 	Display Device 		Frame Memory 	Display Device
	B3=0	B3=1																	
	Frame Memory 	Display Device 																	
	Frame Memory 	Display Device 																	
	B0=0	B0=1																	
B4=0	Frame Memory 	Display Device 																	
	Frame Memory 	Display Device 																	
Restriction	-																		



Relationship between Input Data and Display Data

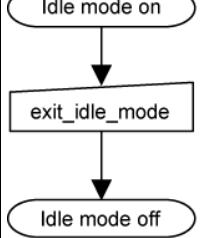
(1) D7 = 0, D6 = 0, D3 = 0 (C0h command: BGR = 0, SS = 0)														
Data input →														→ Data input (End)
R_x1y1	G_x1y1	B_x1y1	R_x2y1	G_x2y1	B_x2y1	R_x319y1	G_x319y1	B_x319y1	R_x320y1	G_x320y1	B_x320y1	
R_x1y2	G_x1y2	B_x1y2	R_x2y2	G_x2y2	B_x2y2	R_x319y2	G_x319y2	B_x319y2	R_x320y2	G_x320y2	B_x320y2	
:	:	:	:	:	:	:	:	:	:	:	:	
R_x1y480	G_x1y480	B_x1y480	R_x2y480	G_x2y480	B_x2y480	R_x319y480	G_x319y480	B_x319y480	R_x320y480	G_x320y480	B_x320y480	
Display panel 1st line														→ Data input (End)
R_x1y1	G_x1y1	B_x1y1	R_x2y1	G_x2y1	B_x2y1	R_x319y1	G_x319y1	B_x319y1	R_x320y1	G_x320y1	B_x320y1	
R_x1y2	G_x1y2	B_x1y2	R_x2y2	G_x2y2	B_x2y2	R_x319y2	G_x319y2	B_x319y2	R_x320y2	G_x320y2	B_x320y2	
:	:	:	:	:	:	:	:	:	:	:	:	
R_x1y480	G_x1y480	B_x1y480	R_x2y480	G_x2y480	B_x2y480	R_x319y480	G_x319y480	B_x319y480	R_x320y480	G_x320y480	B_x320y480	
S1	S2	S3	S4	S5	S6	S955	S956	S957	S958	S959	S960	
480th line														
(2) D7 = 0, D6 = 0, D3 = 1 (C0h command: BGR = 0, SS = 0)														
Data input →														→ Data input (End)
R_x1y1	G_x1y1	B_x1y1	R_x2y1	G_x2y1	B_x2y1	R_x319y1	G_x319y1	B_x319y1	R_x320y1	G_x320y1	B_x320y1	
R_x1y2	G_x1y2	B_x1y2	R_x2y2	G_x2y2	B_x2y2	R_x319y2	G_x319y2	B_x319y2	R_x320y2	G_x320y2	B_x320y2	
:	:	:	:	:	:	:	:	:	:	:	:	
R_x1y480	G_x1y480	B_x1y480	R_x2y480	G_x2y480	B_x2y480	R_x319y480	G_x319y480	B_x319y480	R_x320y480	G_x320y480	B_x320y480	
Display panel 1st line														→ Data input (End)
B_x1y1	G_x1y1	R_x1y1	B_x2y1	G_x2y1	R_x2y1	B_x319y1	G_x319y1	R_x319y1	B_x320y1	G_x320y1	R_x320y1	
B_x1y2	G_x1y2	R_x1y2	B_x2y2	G_x2y2	R_x2y2	B_x319y2	G_x319y2	R_x319y2	B_x320y2	G_x320y2	R_x320y2	
:	:	:	:	:	:	:	:	:	:	:	:	
B_x1y480	G_x1y480	R_x1y480	B_x2y480	G_x2y480	R_x2y480	B_x319y480	G_x319y480	R_x319y480	B_x320y480	G_x320y480	R_x320y480	
S1	S2	S3	S4	S5	S6	S955	S956	S957	S958	S959	S960	
480th line														
(3) D7 = 0, D6 = 1, D3 = 0 (C0h command: BGR = 0, SS = 0)														
Data input →														→ Data input (End)
R_x1y1	G_x1y1	B_x1y1	R_x2y1	G_x2y1	B_x2y1	R_x319y1	G_x319y1	B_x319y1	R_x320y1	G_x320y1	B_x320y1	
R_x1y2	G_x1y2	B_x1y2	R_x2y2	G_x2y2	B_x2y2	R_x319y2	G_x319y2	B_x319y2	R_x320y2	G_x320y2	B_x320y2	
:	:	:	:	:	:	:	:	:	:	:	:	
R_x1y480	G_x1y480	B_x1y480	R_x2y480	G_x2y480	B_x2y480	R_x319y480	G_x319y480	B_x319y480	R_x320y480	G_x320y480	B_x320y480	
Display panel 1st line														→ Data input (End)
R_x320y1	G_x320y1	B_x320y1	R_x319y1	G_x319y1	B_x319y1	R_x2y1	G_x2y1	B_x2y1	R_x1y1	G_x1y1	B_x1y1	
R_x320y2	G_x320y2	B_x320y2	R_x319y2	G_x319y2	B_x319y2	R_x2y2	G_x2y2	B_x2y2	R_x1y2	G_x1y2	B_x1y2	
:	:	:	:	:	:	:	:	:	:	:	:	
R_x320y480	G_x320y480	B_x320y480	R_x319y480	G_x319y480	B_x319y480	R_x2y480	G_x2y480	B_x2y480	R_x1y480	G_x1y480	B_x1y480	
S1	S2	S3	S4	S5	S6	S955	S956	S957	S958	S959	S960	
480th line														
(4) D7 = 0, D6 = 1, D3 = 1 (C0h command: BGR = 0, SS = 0)														
Data input →														→ Data input (End)
R_x1y1	G_x1y1	B_x1y1	R_x2y1	G_x2y1	B_x2y1	R_x319y1	G_x319y1	B_x319y1	R_x320y1	G_x320y1	B_x320y1	
R_x1y2	G_x1y2	B_x1y2	R_x2y2	G_x2y2	B_x2y2	R_x319y2	G_x319y2	B_x319y2	R_x320y2	G_x320y2	B_x320y2	
:	:	:	:	:	:	:	:	:	:	:	:	
R_x1y480	G_x1y480	B_x1y480	R_x2y480	G_x2y480	B_x2y480	R_x319y480	G_x319y480	B_x319y480	R_x320y480	G_x320y480	B_x320y480	
Display panel 1st line														→ Data input (End)
B_x320y1	G_x320y1	R_x320y1	B_x319y1	G_x319y1	R_x319y1	B_x2y1	G_x2y1	R_x2y1	B_x1y1	G_x1y1	R_x1y1	
B_x320y2	G_x320y2	R_x320y2	B_x319y2	G_x319y2	R_x319y2	B_x2y2	G_x2y2	R_x2y2	B_x1y2	G_x1y2	R_x1y2	
:	:	:	:	:	:	:	:	:	:	:	:	
B_x320y480	G_x320y480	R_x320y480	B_x319y480	G_x319y480	R_x319y480	B_x2y480	G_x2y480	R_x2y480	B_x1y480	G_x1y480	R_x1y480	
S1	S2	S3	S4	S5	S6	S955	S956	S957	S958	S959	S960	
480th line														

Figure 117

(5) D7 = 1, D6 = 0, D3 = 0 (C0h command: BGR = 0, SS = 0)												
Data input (Start)						Data input (End)						
R,x1y1	G,x1y1	B,x1y1	R,x2y1	G,x2y1	B,x2y1	R,x319y1	G,x319y1	B,x319y1	R,x320y1	G,x320y1	
R,x1y2	G,x1y2	B,x1y2	R,x2y2	G,x2y2	B,x2y2	R,x319y2	G,x319y2	B,x319y2	R,x320y2	G,x320y2	
:	:	:	:	:	:	:	:	:	:	:	
R,x1y480	G,x1y480	B,x1y480	R,x2y480	G,x2y480	B,x2y480	R,x319y480	G,x319y480	B,x319y480	R,x320y480	G,x320y480	
Data input (End)												
Display panel	1st line						R,x1y480	G,x1y480	B,x1y480	R,x2y480	G,x2y480	B,x2y480
	:	:	:	:	:	:
480th line	R,x1y2	G,x1y2	B,x1y2	R,x2y2	G,x2y2	B,x2y2	R,x319y2	G,x319y2	B,x319y2	R,x320y2	G,x320y2
	R,x1y1	G,x1y1	B,x1y1	R,x2y1	G,x2y1	B,x2y1	R,x319y1	G,x319y1	B,x319y1	R,x320y1	G,x320y1
S1	S2	S3	S4	S5	S6	S955	S956	S957	S958	S959	S960
(6) D7 = 1, D6 = 0, D3 = 1 (C0h command: BGR = 0, SS = 0)												
Data input (Start)						Data input (End)						
R,x1y1	G,x1y1	B,x1y1	R,x2y1	G,x2y1	B,x2y1	R,x319y1	G,x319y1	B,x319y1	R,x320y1	G,x320y1	B,x320y1
R,x1y2	G,x1y2	B,x1y2	R,x2y2	G,x2y2	B,x2y2	R,x319y2	G,x319y2	B,x319y2	R,x320y2	G,x320y2	B,x320y2
:	:	:	:	:	:	:	:	:	:	:	:
R,x1y480	G,x1y480	B,x1y480	R,x2y480	G,x2y480	B,x2y480	R,x319y480	G,x319y480	B,x319y480	R,x320y480	G,x320y480	B,x320y480
Data input (End)												
Display panel	1st line						R,x1y480	G,x1y480	B,x1y480	R,x2y480	G,x2y480	B,x2y480
	:	:	:	:	:	:
480th line	B,x1y2	G,x1y2	R,x1y2	B,x2y2	G,x2y2	R,x2y2	B,x319y2	G,x319y2	R,x319y2	B,x320y2	G,x320y2
	B,x1y1	G,x1y1	R,x1y1	B,x2y1	G,x2y1	R,x2y1	B,x319y1	G,x319y1	R,x319y1	B,x320y1	G,x320y1
S1	S2	S3	S4	S5	S6	S955	S956	S957	S958	S959	S960
(7) D7 = 1, D6 = 1, D3 = 0 (C0h command: BGR = 0, SS = 0)												
Data input (Start)						Data input (End)						
R,x1y1	G,x1y1	B,x1y1	R,x2y1	G,x2y1	B,x2y1	R,x319y1	G,x319y1	B,x319y1	R,x320y1	G,x320y1	B,x320y1
R,x1y2	G,x1y2	B,x1y2	R,x2y2	G,x2y2	B,x2y2	R,x319y2	G,x319y2	B,x319y2	R,x320y2	G,x320y2	B,x320y2
:	:	:	:	:	:	:	:	:	:	:	:
R,x1y480	G,x1y480	B,x1y480	R,x2y480	G,x2y480	B,x2y480	R,x319y480	G,x319y480	B,x319y480	R,x320y480	G,x320y480	B,x320y480
Data input (End)												
Display panel	1st line						R,x320y480	G,x320y480	B,x320y480	R,x319y480	G,x319y480	B,x319y480
	:	:	:	:	:	:
480th line	R,x320y2	G,x320y2	B,x320y2	R,x319y2	G,x319y2	B,x319y2	R,x2y2	G,x2y2	B,x2y2	R,x1y2	G,x1y2
	R,x320y1	G,x320y1	B,x320y1	R,x319y1	G,x319y1	B,x319y1	R,x2y1	G,x2y1	B,x2y1	R,x1y1	G,x1y1
S1	S2	S3	S4	S5	S6	S955	S956	S957	S958	S959	S960
(8) D7 = 1, D6 = 1, D3 = 1 (C0h command: BGR = 0, SS = 0)												
Data input (Start)						Data input (End)						
R,x1y1	G,x1y1	B,x1y1	R,x2y1	G,x2y1	B,x2y1	R,x319y1	G,x319y1	B,x319y1	R,x320y1	G,x320y1	B,x320y1
R,x1y2	G,x1y2	B,x1y2	R,x2y2	G,x2y2	B,x2y2	R,x319y2	G,x319y2	B,x319y2	R,x320y2	G,x320y2	B,x320y2
:	:	:	:	:	:	:	:	:	:	:	:
R,x1y480	G,x1y480	B,x1y480	R,x2y480	G,x2y480	B,x2y480	R,x319y480	G,x319y480	B,x319y480	R,x320y480	G,x320y480	B,x320y480
Data input (End)												
Display panel	1st line						R,x320y480	G,x320y480	B,x320y480	R,x319y480	G,x319y480	B,x319y480
	:	:	:	:	:	:
480th line	R,x320y2	G,x320y2	B,x320y2	R,x319y2	G,x319y2	B,x319y2	R,x2y2	G,x2y2	B,x2y2	R,x1y2	G,x1y2
	R,x320y1	G,x320y1	B,x320y1	R,x319y1	G,x319y1	B,x319y1	R,x2y1	G,x2y1	B,x2y1	R,x1y1	G,x1y1
S1	S2	S3	S4	S5	S6	S955	S956	S957	S958	S959	S960

Figure 118

exit_idle_mode: 38h

38h	exit_idle_mode											
	Direction	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	H→D	0	X	0	0	1	1	1	0	0	0	38h
Parameter	None											
Description	This command causes the display module to exit Idle mode. LCD can display up to maximum 16,777,216 colors. X = Don't care											
Restriction	This command has no effect when the display module is not in Idle mode.											
Flow Chart	 <pre> graph TD A([Idle mode on]) --> B[exit_idle_mode] B --> C([Idle mode off]) </pre> <div style="border: 1px dashed black; padding: 5px; margin-top: 10px;"> Legend <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer </div>											

enter_idle_mode: 39h

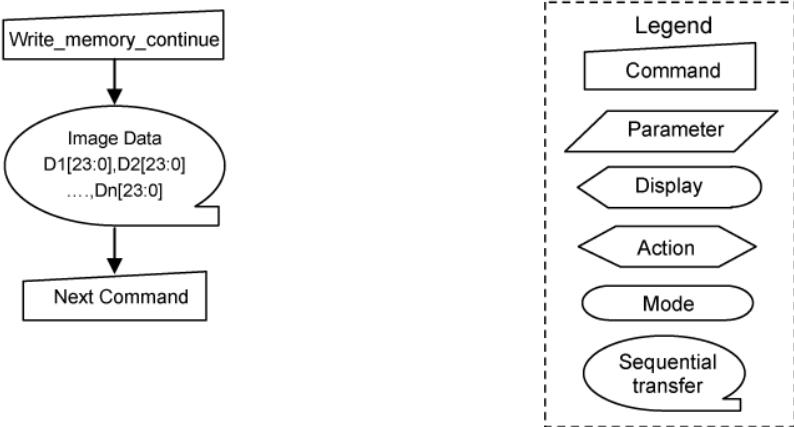
39h	enter_idle_mode																																																																																																																																																																																																				
	Direction	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex																																																																																																																																																																																									
Command	H→D	0	X	0	0	1	1	1	0	0	1	39h																																																																																																																																																																																									
Parameter	None																																																																																																																																																																																																				
Description	This command causes the display module to enter Idle mode. In Idle mode, color expression is reduced. Eight color depth data are displayed using MSB of each R, G and B color components in the Frame Memory. Gamma settings (Gamma Set A-B (C8-Ah)) for each R, G, B are enabled when Idle Mode is On.																																																																																																																																																																																																				
	<p style="text-align: center;">Memory Display Panel</p> <table border="1" style="margin-top: 10px; width: 100%; text-align: center;"> <thead> <tr> <th colspan="13">Memory Contents vs. Display Color</th> </tr> <tr> <th></th> <th colspan="6">R[7:0]</th> <th colspan="6">G[7:0]</th> <th colspan="6">B[7:0]</th> </tr> </thead> <tbody> <tr> <td>Black</td> <td>0</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td> <td>0</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td> <td>0</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td> </tr> <tr> <td>Blue</td> <td>0</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td> <td>0</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td> <td>1</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td> </tr> <tr> <td>Red</td> <td>1</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td> <td>0</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td> <td>0</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td> </tr> <tr> <td>Magenta</td> <td>1</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td> <td>0</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td> <td>1</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td> </tr> <tr> <td>Green</td> <td>0</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td> <td>1</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td> <td>0</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td> </tr> <tr> <td>Cyan</td> <td>0</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td> <td>1</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td> <td>1</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td> </tr> <tr> <td>Yellow</td> <td>1</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td> <td>1</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td> <td>0</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td> </tr> <tr> <td>White</td> <td>1</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td> <td>1</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td> <td>1</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td> </tr> </tbody> </table> <p style="text-align: center;">X = Don't care</p>													Memory Contents vs. Display Color														R[7:0]						G[7:0]						B[7:0]						Black	0	X	X	X	X	X	0	X	X	X	X	X	0	X	X	X	X	X	Blue	0	X	X	X	X	X	0	X	X	X	X	X	1	X	X	X	X	X	Red	1	X	X	X	X	X	0	X	X	X	X	X	0	X	X	X	X	X	Magenta	1	X	X	X	X	X	0	X	X	X	X	X	1	X	X	X	X	X	Green	0	X	X	X	X	X	1	X	X	X	X	X	0	X	X	X	X	X	Cyan	0	X	X	X	X	X	1	X	X	X	X	X	1	X	X	X	X	X	Yellow	1	X	X	X	X	X	1	X	X	X	X	X	0	X	X	X	X	X	White	1	X	X	X	X	X	1	X	X	X	X	X	1	X	X	X	X	X
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Blue	0	X	X	X	X	X	0	X	X	X	X	X	1	X	X	X	X	X																																																																																																																																																																																			
Red	1	X	X	X	X	X	0	X	X	X	X	X	0	X	X	X	X	X																																																																																																																																																																																			
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Green	0	X	X	X	X	X	1	X	X	X	X	X	0	X	X	X	X	X																																																																																																																																																																																			
Cyan	0	X	X	X	X	X	1	X	X	X	X	X	1	X	X	X	X	X																																																																																																																																																																																			
Yellow	1	X	X	X	X	X	1	X	X	X	X	X	0	X	X	X	X	X																																																																																																																																																																																			
White	1	X	X	X	X	X	1	X	X	X	X	X	1	X	X	X	X	X																																																																																																																																																																																			
Restriction	This command has no effect when module is already in Idle mode.																																																																																																																																																																																																				

39h	enter_idle_mode
Flow Chart	<p>The flowchart illustrates the sequence of events for entering idle mode. It begins with an oval labeled "Idle mode off", which points down to a rectangle labeled "enter_idle_mode". This leads to another oval labeled "Idle mode on". To the right of the flowchart is a legend enclosed in a dashed box, defining symbols used in the chart.</p> <p>Legend:</p> <ul style="list-style-type: none">Command (rectangle)Parameter (trapezoid)Display (left-pointing arrow)Action (right-pointing arrow)Mode (oval)Sequential transfer (oval with a curved arrow)

set_pixel_format: 3Ah

3Ah	set_pixel_format																																																
	Direction	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex																																					
Command	H→D	0	X	0	0	1	1	1	0	1	0	3Ah																																					
1 st parameter	H→D	1	X	0	D6	D5	D4	0	D2	D1	D0	XXh																																					
Description	<p>This command is used to define the format of RGB picture data, which are to be transferred via the DPI/DSI/MDDI.</p> <p>Bits D6, D5, and D4 are used in MIPI DPI operation, MIPI DSI Video Mode, and MDDI Active Refresh Mode. Bits D2, D1, and D0 are used in MIPI DBI operation, MIPI DSI Command Mode, MDDI Command Mode, and I²C operation.</p> <p>The formats are shown in the following table. Set Bits D7 and D3 to 0.</p> <table border="1"> <thead> <tr> <th>Control Interface Color Format</th> <th>D6/D2</th> <th>D5/D1</th> <th>D4/D0</th> </tr> </thead> <tbody> <tr> <td>Setting inhibited</td> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>Setting inhibited</td> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>Setting inhibited</td> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>Setting inhibited</td> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>Setting inhibited</td> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>16 bits/pixel (65,536 colors)</td> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>18 bits/pixel (262,144 colors)</td> <td>1</td> <td>1</td> <td>0</td> </tr> <tr> <td>24 bits/pixel (16,777,216 colors)</td> <td>1</td> <td>1</td> <td>1</td> </tr> </tbody> </table> <p>For each data format, see the corresponding section.</p> <p>Note: When "Setting inhibited" is set, undesirable image will be displayed on the panel.</p> <p>X = Don't care</p>													Control Interface Color Format	D6/D2	D5/D1	D4/D0	Setting inhibited	0	0	0	Setting inhibited	0	0	1	Setting inhibited	0	1	0	Setting inhibited	0	1	1	Setting inhibited	1	0	0	16 bits/pixel (65,536 colors)	1	0	1	18 bits/pixel (262,144 colors)	1	1	0	24 bits/pixel (16,777,216 colors)	1	1	1
Control Interface Color Format	D6/D2	D5/D1	D4/D0																																														
Setting inhibited	0	0	0																																														
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24 bits/pixel (16,777,216 colors)	1	1	1																																														
Restriction	-																																																
Flow Chart	<pre> graph TD A[set_pixel_format] --> B{set_pixel_format} B --> C(New Pixel Mode) style A fill:#fff,stroke:#000,stroke-width:1px style B fill:#fff,stroke:#000,stroke-width:1px style C fill:#fff,stroke:#000,stroke-width:1px style Legend fill:#fff,stroke:#000,stroke-width:1px style LegendText fill:#fff,stroke:#000,stroke-width:1px </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																																																

write_memory_continue: 3Ch

3Ch		write_memory_continue											
		Direction	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command		H→D	0	X	0	0	1	1	1	1	0	0	3Ch
1st pixel data		H→D	1	D1 [23:8]	D1 [7]	D1 [6]	D1 [5]	D1 [4]	D1 [3]	D1 [2]	D1 [1]	D1 [0]	000h ... FFFh
:		H→D	1	Dx [23:8]	Dx [7]	Dx [6]	Dx [5]	Dx [4]	Dx [3]	Dx [2]	Dx [1]	Dx [0]	000h ... FFFh
Nth pixel data		H→D	1	Dn [23:8]	Dn [7]	Dn [6]	Dn [5]	Dn [4]	Dn [3]	Dn [2]	Dn [1]	Dn [0]	000h ... FFFh
Description	<p>This command transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous write_memory_continue or write_memory_start command.</p> <p>Frame Memory Access and Interface Setting (B3h): WEMODE = 0</p> <p>If the number of pixels in the transfer data exceed (EC-SC+1)*(EP-SP+1), the extra pixels are ignored.</p> <p>Frame Memory Access and Interface Setting (B3h): WEMODE = 1</p> <p>When the number of pixels in the transfer data exceed (EC-SC+1)*(EP-SP+1), the column register and the page register are reset to the Start Column/Start Page positions, and the subsequent data are written to the frame memory.</p> <p>X=Don't care</p>												
Restriction	<p>If write_memory_continue command is executed without setting set_column_address (2Ah), set_page_address (2Bh), and set_address_mode (36h), there is no guarantee that data are correctly written to the frame memory. If data is not transferred in units of pixels, the extra data is regarded as invalid.</p>												
Flow Chart	 <pre> graph TD A[Write_memory_continue] --> B((Image Data D1[23:0], D2[23:0] ..., Dn[23:0])) B --> C[Next Command] style B fill:none,stroke:none style C fill:none,stroke:none %% Legend subgraph Legend direction TB L1[Command] L2[Parameter] L3[Display] L4[Action] L5[Mode] L6[Sequential transfer] end </pre>												

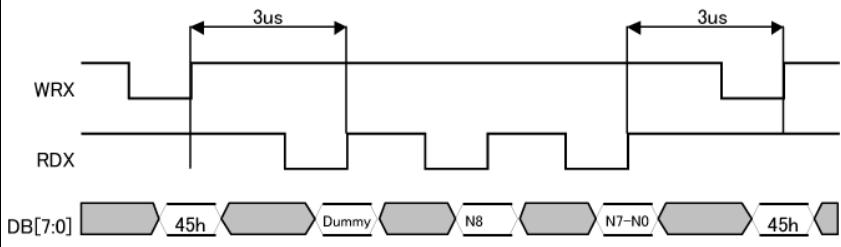
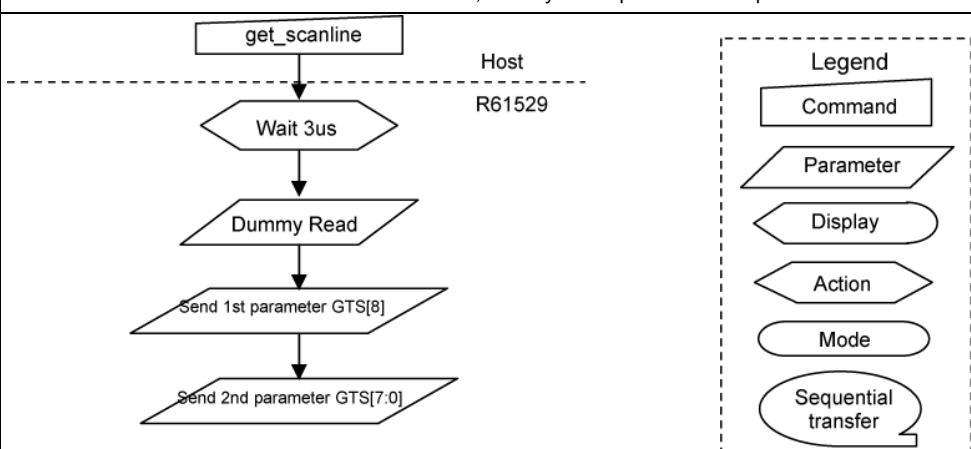
read_memory_continue: 3Eh

3Eh		read_memory_continue											
		Direction	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	H→D	0	X	0	0	1	1	1	1	1	1	0	3Eh
Dummy parameter	D→H	1	X	X	X	X	X	X	X	X	X	X	XXh
1 st pixel data	D→H	1	D1 [23:8]	D1 [7]	D1 [6]	D1 [5]	D1 [4]	D1 [3]	D1 [2]	D1 [1]	D1 [0]	000h...FFFh	
:	D→H	1	Dx [23:8]	Dx [7]	Dx [6]	Dx [5]	Dx [4]	Dx [3]	Dx [2]	Dx [1]	Dx [0]	000h...FFFh	
Nth pixel data	D→H	1	Dn [23:8]	Dn [7]	Dn [6]	Dn [5]	Dn [4]	Dn [3]	Dn [2]	Dn [1]	Dn [0]	000h...FFFh	
Description	<p>This command transfers image data from the host processor to the display module's frame memory continuing from the location following the previous read_memory_continue or read_memory_start command.</p> <p>If read operation is executed after (EP, EC) is read, the last data (EP, EC) continue to output.</p> <p>After pixel data 1 are written to frame memory (SC, SP), address counter's direction differs depending on setting of set_address_mode (36h)'s Bits 5, 6, 7. See "Host Processor to Memory Write/Read Direction".</p> <p>X = Don't care</p>												
Restriction	<p>In any color mode, format returned by read_memory_continue is always 24 bits so there is no restriction on the length of parameter. If data is not transferred in units of pixels, the extra data is regarded as invalid.</p> <p>Note: When this command is read via DSI or MDDI, dummy read operation is not performed.</p>												
Flow Chart	<pre> graph TD A[read_memory_continue] --> B{Dummy Read} B --> C([Image Data D1[23:0], D2[23:0] ..., Dn[23:0]]) C --> D[Next Command] style C fill:#f0f0f0,stroke:#000,stroke-width:1px style D fill:#f0f0f0,stroke:#000,stroke-width:1px style A fill:#f0f0f0,stroke:#000,stroke-width:1px style B fill:#f0f0f0,stroke:#000,stroke-width:1px style D fill:#f0f0f0,stroke:#000,stroke-width:1px %% Legend subgraph Legend LegendTitle[Legend] LegendCommand[Command] LegendParameter[Parameter] LegendDisplay[Display] LegendAction[Action] LegendMode[Mode] LegendSequential[Sequential transfer] end %% Legend styling LegendCommand fill:#f0f0f0,stroke:#000,stroke-width:1px LegendParameter fill:#f0f0f0,stroke:#000,stroke-width:1px LegendDisplay fill:#f0f0f0,stroke:#000,stroke-width:1px LegendAction fill:#f0f0f0,stroke:#000,stroke-width:1px LegendMode fill:#f0f0f0,stroke:#000,stroke-width:1px LegendSequential fill:#f0f0f0,stroke:#000,stroke-width:1px </pre>												

set_tear_scanline:44h

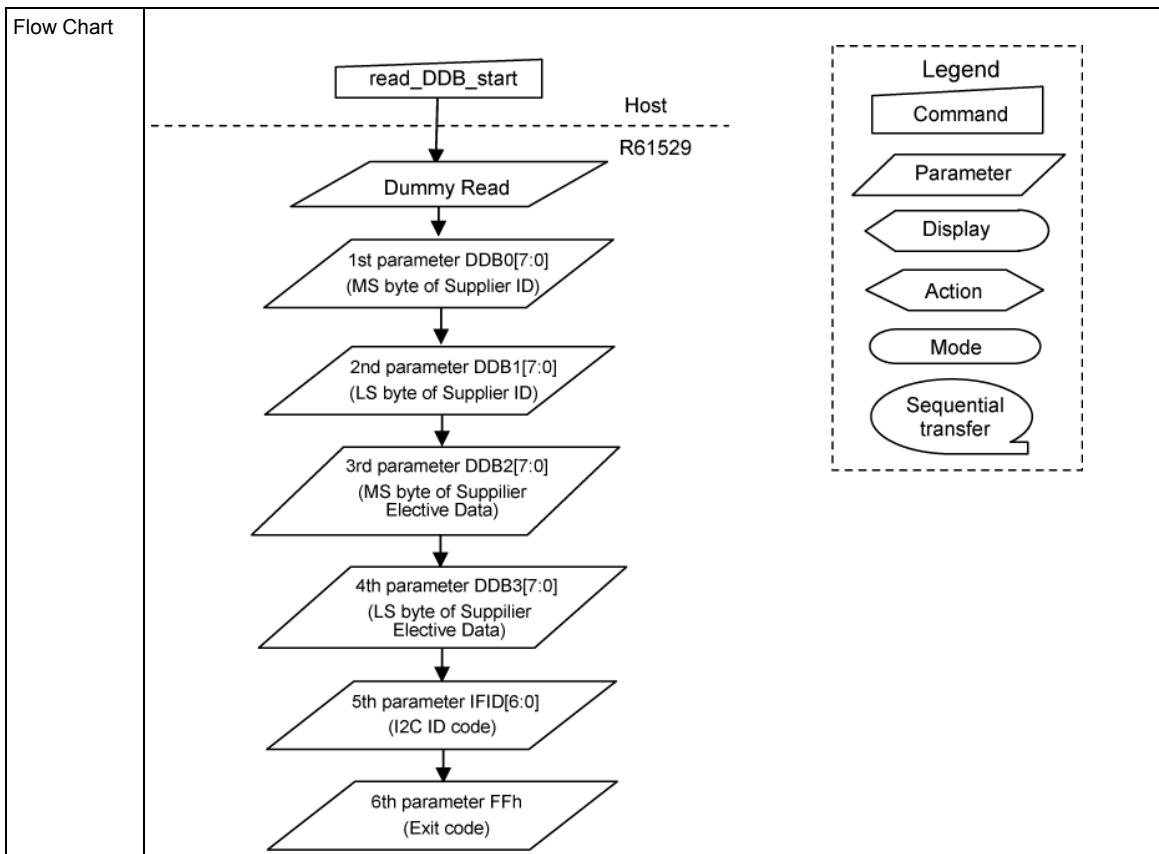
44h		set_tear_scanline											
		Direction	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command		H→D	0	X	0	1	0	0	0	1	0	0	44h
1 st Parameter		H→D	1	X	0	0	0	0	0	0	0	STS [8]	0Xh
2 nd Parameter		H→D	1	X	STS [7]	STS [6]	STS [5]	STS [4]	STS [3]	STS [2]	STS [1]	STS [0]	XXh
Description	<p>This command turns on the display module's Tearing Effect output signal on the TE signal line when the display module reaches one line before a line N defined by STS [8:0].</p> <p>TE line is unaffected by change in B4 bit of set_address_mode command.</p> <p>See figure in "TE Pin Output Signal".</p> <p>X =don't care.</p>												
Restriction	<p>The command takes affect on the frame following the current frame. Therefore, if the TE signal is already ON, TE signal is output according to the old set_tear_on and set_tear_scanline commands until the end of currently scanned frame.</p> <p>Setting is disabled when TELOM=1 of set_tear_on (35h).</p> <p>Make sure that STS [8:0] ≤ NL (number of line) + 1.</p>												
Flow Chart	<pre> graph TD A([TE Output On or Off]) --> B[/set_tear_scanline/] B --> C[/Send 1st parameter STS[8]/] C --> D[/Send 2nd parameter STS[7:0]/] D --> E([TE Output On the Nth line]) </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 												

get_scanline: 45h

45h	get_scanline											
	Direction	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	H→D	0	X	0	1	0	0	0	1	0	1	45h
Dummy parameter	D→H	1	X	X	X	X	X	X	X	X	X	XXh
1 st parameter	D→H	1	X	0	0	0	0	0	0	0	GTS [8]	0Xh
2 nd parameter	D→H	1	x	GTS [7]	GTS [6]	GTS [5]	GTS [4]	GTS [3]	GTS [2]	GTS [1]	GTS [0]	XXh
Description	<p>The display module returns the current scan line. The total number of scan lines is defined as (BP + NL + FP). The first scan line of back porch period is defined as line 0. In sleep mode, the value returned by get_scanline is undefined.</p> <p>X = Don't care</p>											
Restriction	<p>After get_line command is input, it takes 3μs or more to read it. After parameters are read, wait 3μs or more to input this command again.</p>  <p>Note: When this command is read via DSI or MDDI, dummy read operation is not performed.</p>											
Flow Chart												

read_DDB_start: A1h

A1h	read_DDB_start												
	Direction	DCX	DB23-DB8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	
Command	H → D	0	X	1	0	1	0	0	0	0	1	A1h	
Dummy parameter	D → H	1	X	X	X	X	X	X	X	X	X	XXh	
1 st parameter	D → H	1	X	DDB0 [7]	DDB0 [6]	DDB0 [5]	DDB0 [4]	DDB0 [3]	DDB0 [2]	DDB0 [1]	DDB0 [0]	XXh	
2 nd parameter	D → H	1	X	DDB1 [7]	DDB1 [6]	DDB1 [5]	DDB1 [4]	DDB1 [3]	DDB1 [2]	DDB1 [1]	DDB1 [0]	XXh	
3 rd parameter	D → H	1	X	DDB2 [7]	DDB2 [6]	DDB2 [5]	DDB2 [4]	DDB2 [3]	DDB2 [2]	DDB2 [1]	DDB2 [0]	XXh	
4 th parameter	D → H	1	X	DDB3 [7]	DDB3 [6]	DDB3 [5]	DDB3 [4]	DDB3 [3]	DDB3 [2]	DDB3 [1]	DDB3 [0]	XXh	
5 th parameter	D → H	1	X	0	IFID [6]	IFID [5]	IFID [4]	IFID [3]	IFID [2]	IFID [1]	IFID [0]	XXh	
6 th parameter	D → H	1	X	1	1	1	1	1	1	1	1	FFh	
Description	The command returns information from the display module as follows: 1 st parameter DDB0[7:0]: MS byte of Supplier ID (ID1[15:8]) 2 nd parameter DDB1[7:0]: LS byte of Supplier ID (ID1[7:0]) 3 rd parameter DDB2[7:0]: Supplier Elective Data (ID2[15:8]) 4 th parameter DDB3[7:0]: Supplier Elective Data (ID2[7:0]) 5 th parameter: IFID[6:0]: I ² C ID code 6 th parameter: EEC[7:0]: FFh Supplier ID and Supplier Elective Data stored in internal NVM are read. X = Don't care												
Restriction	Note: When this command is read via DS1 or MDDI, dummy read operation is not performed.												



Manufacturer Command

Additional User Command

MCAP: Manufacturer Command Access Protect (B0h)

MCAP(Manufacturer Command Access Protect)												Hex																																																																																			
B0h	W / R	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex																																																																																			
Command	—	0	X	1	0	1	1	0	0	0	0	B0h																																																																																			
1st parameter	W / R	1	X	0	0	0	0	0	MCAP [2]	MCAP [1]	MCAP [0]	0Xh																																																																																			
Description	MCAP[2:0] The R61529 is required to release Access Packet before inputting a Manufacturer Command. This command releases parameters so that Manufacturer Command inputs are enabled. When the conditions to release Protect, as shown in the table above, are met, Manufacturer Command inputs are enabled.																																																																																														
	<table border="1"> <thead> <tr> <th colspan="2"></th> <th colspan="6">MCAP[1:0]</th> <th colspan="4"></th> </tr> <tr> <th colspan="2">Command</th> <th>3'b000</th> <th>3'b001</th> <th>3'b010</th> <th>3'b011 (default)</th> <th>3'b100</th> <th>3'b101-3'b111</th> <th colspan="4"></th> </tr> </thead> <tbody> <tr> <td>B0h</td> <td>Yes</td> <td rowspan="8">Setting inhibited</td> <td>Yes</td> <td>Yes</td> <td rowspan="8">Yes</td> <td rowspan="8">Setting inhibited</td> <td colspan="4"></td> </tr> <tr> <td>B1h</td> <td>Yes</td> <td>Yes</td> <td>No</td> <td colspan="4"></td> </tr> <tr> <td>B3h-BFh</td> <td>Yes</td> <td>No</td> <td>No</td> <td colspan="4"></td> </tr> <tr> <td>C0h-D3h</td> <td>Yes</td> <td>No</td> <td>No</td> <td colspan="4"></td> </tr> <tr> <td>D6h-F3h</td> <td>No</td> <td>No</td> <td>No</td> <td colspan="4"></td> </tr> <tr> <td>F5h-F6h</td> <td>Yes</td> <td>Yes</td> <td>No</td> <td colspan="4"></td> </tr> <tr> <td>F8h-FEh</td> <td>No</td> <td>No</td> <td>No</td> <td colspan="4" rowspan="2"></td> </tr> </tbody> </table> <p>Yes : Access Possible(Protect Off) No : Access impossible(Protect On) Once the R61529 enables Manufacturer Command inputs, it keeps the state until MCAP[2:0] is written so that the R61529 enters Protect ON state again. X = Don't care</p>														MCAP[1:0]										Command		3'b000	3'b001	3'b010	3'b011 (default)	3'b100	3'b101-3'b111					B0h	Yes	Setting inhibited	Yes	Yes	Yes	Setting inhibited					B1h	Yes	Yes	No					B3h-BFh	Yes	No	No					C0h-D3h	Yes	No	No					D6h-F3h	No	No	No					F5h-F6h	Yes	Yes	No					F8h-FEh	No	No	No				
		MCAP[1:0]																																																																																													
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C0h-D3h	Yes		No	No																																																																																											
D6h-F3h	No		No	No																																																																																											
F5h-F6h	Yes		Yes	No																																																																																											
F8h-FEh	No		No	No																																																																																											
Restriction	In case of H/W Reset or soft_reset, accessing a Manufacturer Command is restricted so that Manufacturer Commands B1h-FEh inputs are identified as nop command. Note: When this command is read via DSI or MDDI, dummy read operation is not performed.																																																																																														

Low Power Mode Control (B1h)

Low Power Mode Control												
B1h	W / R	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	—	0	X	1	0	1	1	0	0	0	1	B1h
1 st parameter	W / R	1	X	0	0	0	0	0	0	0	DSTB	0Xh
Description	<p>This command is used to enter the Deep Standby Mode.</p> <p>DSTB</p> <p>The driver enters the Deep Standby Mode when DSTB=1. Internal logic power supply circuit (VDD) is turned down enabling low power consumption. In the Deep Standby mode, data stored in the frame memory and the instructions are not retained. Rewrite them after the Deep Standby mode is exited.</p> <p>Do not input soft_reset command and other commands in deep standby mode.</p> <p>X = Don't care</p>											
Restriction	<p>Deep standby mode can be set in only Sleep Mode On. Accessing DSTB in Sleep Mode Off is regarded (treated as nop command). DSTB is accessed after enter_sleep_mode.</p> <p>When this command is read via DSI or MDDI, dummy read operation is not performed.</p>											
Flow Chart	<pre> graph TD A([Sleep Mode]) --> B[Low Power Mode Control] B --> C{DSTB=1} C --> D([Deep Standby Mode]) style B fill:#e0e0ff,stroke:#000,stroke-width:1px style C fill:#ffffcc,stroke:#000,stroke-width:1px style D fill:#e0e0ff,stroke:#000,stroke-width:1px </pre> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 											

Frame Memory Access and Interface Setting (B3h)

B3h	Frame Memory Access and Interface Setting																										
	W / R	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex															
Command	—	0	X	1	0	1	1	0	0	1	1	B3h															
1 st parameter	W / R	1	X	0	0	0	0	0	0	WE MODE	0	0Xh															
2 nd parameter	W / R	1	X	0	0	IN_T EON	0	0	TEI [2]	TEI [1]	TEI [0]	XXh															
3 rd parameter	W / R	1	X	0	0	0	0	0	0	0	0	00h															
4 th parameter	W / R	1	X	0	0	EPF [1]	EPF [0]	0	0	DFM [1]	DFM [0]	XXh															
Description	WEMODE <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center; padding: 2px;">WEMODE</th> <th style="text-align: center; padding: 2px;">Window group setting for memory write</th> </tr> </thead> <tbody> <tr> <td style="text-align: center; padding: 2px;">0</td> <td style="padding: 2px;">The write start position is not reset to the start of window address, and the subsequent data are disregarded.</td> </tr> <tr> <td style="text-align: center; padding: 2px;">1</td> <td style="padding: 2px;">The write start position is reset to the start of window address area to overwrite the subsequent data to the previous data.</td> </tr> </tbody> </table>												WEMODE	Window group setting for memory write	0	The write start position is not reset to the start of window address, and the subsequent data are disregarded.	1	The write start position is reset to the start of window address area to overwrite the subsequent data to the previous data.									
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	EPF[1:0] This bit is used to set data format when 16/18bpp (R,G,B) data are converted to 24bpp (r,g,b) stored in internal frame memory (24bpp). <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center; padding: 2px;">EPF[1:0]</th> <th style="text-align: center; padding: 2px;">18bpp (R, G, B) → 24bpp (r, g, b)</th> <th style="text-align: center; padding: 2px;">16bpp (R, G, B) → 24bpp (r, g, b)</th> </tr> </thead> <tbody> <tr> <td style="text-align: center; padding: 2px;">2'h0</td> <td style="padding: 2px;"> <p>"0" is written to the LSB.</p> <p>r[7:0]={ R[5:0], 2'h0 } g[7:0]={ G[5:0], 2'h0 } b[7:0]={ B[5:0], 2'h0 }</p> <p>Note that the data are converted as follows: R[5:0], B[5:0]=6'h3F → r, b[7:0]=8'hFF G[5:0]=6'h3F → g[7:0]=8'hFF</p> </td> <td style="padding: 2px;"> <p>"0" is written to the LSB.</p> <p>r[7:0]={ R[5:0], 2'h0 } g[7:0]={ G[5:0], 2'h0 } b[7:0]={ B[5:0], 2'h0 }</p> <p>Note that the data are converted as follows: R[4:0], B[4:0]=5'h1F → r, b[7:0]=8'hFF G[5:0]=6'h3F → g[7:0]=8'hFF</p> </td> </tr> <tr> <td style="text-align: center; padding: 2px;">2'h1</td> <td style="padding: 2px;"> <p>"1" is written to the LSB.</p> <p>r[7:0]={ R[5:0], 2'h3 } g[7:0]={ G[5:0], 2'h3 } b[7:0]={ B[5:0], 2'h3 }</p> <p>Note that the data are converted as follows: R[5:0], B[5:0]=6'h0 → r, b[7:0]=8'h00 G[5:0]=6'h0 → g[7:0]=8'h00</p> </td> <td style="padding: 2px;"> <p>"1" is written to the LSB.</p> <p>r[7:0]={ R[5:0], 2'h3 } g[7:0]={ G[5:0], 2'h3 } b[7:0]={ B[5:0], 2'h3 }</p> <p>Note that the data are converted as follows: R[4:0], B[4:0]=5'h0 → r, b[7:0]=8'h00 G[5:0]=6'h0 → g[7:0]=8'h00</p> </td> </tr> <tr> <td style="text-align: center; padding: 2px;">2'h2</td> <td style="padding: 2px;"> <p>The MSB value is written to the LSB.</p> <p>r[7:0]={ R[5:0], R[5:4] } g[7:0]={ G[5:0], G[5:4] } b[7:0]={ B[5:0], B[5:4] }</p> </td> <td style="padding: 2px;"> <p>The MSB value is written to the LSB.</p> <p>r[7:0]={ R[4:0], R[4:2] } g[7:0]={ G[5:0], G[5:4] } b[7:0]={ B[4:0], B[4:2] }</p> </td> </tr> <tr> <td style="text-align: center; padding: 2px;">2'h3</td> <td style="padding: 2px;">Setting inhibited</td> <td style="padding: 2px;"></td> </tr> </tbody> </table>												EPF[1:0]	18bpp (R, G, B) → 24bpp (r, g, b)	16bpp (R, G, B) → 24bpp (r, g, b)	2'h0	<p>"0" is written to the LSB.</p> <p>r[7:0]={ R[5:0], 2'h0 } g[7:0]={ G[5:0], 2'h0 } b[7:0]={ B[5:0], 2'h0 }</p> <p>Note that the data are converted as follows: R[5:0], B[5:0]=6'h3F → r, b[7:0]=8'hFF G[5:0]=6'h3F → g[7:0]=8'hFF</p>	<p>"0" is written to the LSB.</p> <p>r[7:0]={ R[5:0], 2'h0 } g[7:0]={ G[5:0], 2'h0 } b[7:0]={ B[5:0], 2'h0 }</p> <p>Note that the data are converted as follows: R[4:0], B[4:0]=5'h1F → r, b[7:0]=8'hFF G[5:0]=6'h3F → g[7:0]=8'hFF</p>	2'h1	<p>"1" is written to the LSB.</p> <p>r[7:0]={ R[5:0], 2'h3 } g[7:0]={ G[5:0], 2'h3 } b[7:0]={ B[5:0], 2'h3 }</p> <p>Note that the data are converted as follows: R[5:0], B[5:0]=6'h0 → r, b[7:0]=8'h00 G[5:0]=6'h0 → g[7:0]=8'h00</p>	<p>"1" is written to the LSB.</p> <p>r[7:0]={ R[5:0], 2'h3 } g[7:0]={ G[5:0], 2'h3 } b[7:0]={ B[5:0], 2'h3 }</p> <p>Note that the data are converted as follows: R[4:0], B[4:0]=5'h0 → r, b[7:0]=8'h00 G[5:0]=6'h0 → g[7:0]=8'h00</p>	2'h2	<p>The MSB value is written to the LSB.</p> <p>r[7:0]={ R[5:0], R[5:4] } g[7:0]={ G[5:0], G[5:4] } b[7:0]={ B[5:0], B[5:4] }</p>	<p>The MSB value is written to the LSB.</p> <p>r[7:0]={ R[4:0], R[4:2] } g[7:0]={ G[5:0], G[5:4] } b[7:0]={ B[4:0], B[4:2] }</p>	2'h3	Setting inhibited	
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2'h2	<p>The MSB value is written to the LSB.</p> <p>r[7:0]={ R[5:0], R[5:4] } g[7:0]={ G[5:0], G[5:4] } b[7:0]={ B[5:0], B[5:4] }</p>	<p>The MSB value is written to the LSB.</p> <p>r[7:0]={ R[4:0], R[4:2] } g[7:0]={ G[5:0], G[5:4] } b[7:0]={ B[4:0], B[4:2] }</p>																									
2'h3	Setting inhibited																										

Description	DFM[1:0]												
Description	The bit is used to define image data write/read format to the Frame Memory. For details, see a section of each data format.												
	TEI[2:0]												
	The bit is used to define interval between outputs of TE signal. Set in accordance with update cycle and transfer rate of the display data.												
	<table border="1"> <thead> <tr> <th>TEI[2:0]</th><th>Interval</th></tr> </thead> <tbody> <tr> <td>0</td><td>Every frame</td></tr> <tr> <td>1</td><td>2 frames</td></tr> <tr> <td>3</td><td>4 frames</td></tr> <tr> <td>5</td><td>6 frames</td></tr> <tr> <td>Other than above</td><td>Setting inhibited</td></tr> </tbody> </table>	TEI[2:0]	Interval	0	Every frame	1	2 frames	3	4 frames	5	6 frames	Other than above	Setting inhibited
TEI[2:0]	Interval												
0	Every frame												
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Other than above	Setting inhibited												
	IN_TEON												
	The bit specifies whether TE pin is used or TER (TE Report) is used in MIPI DSI operation, and specifies whether TE pin is used or Client initiated wake up is used in MDDI operation.												
	<table border="1"> <thead> <tr> <th>IN_TEON</th><th>Setting</th></tr> </thead> <tbody> <tr> <td>0</td><td>TE pin is used.</td></tr> <tr> <td>1</td><td>TE pin is not used. Set TELOM (35h command) to 0.</td></tr> </tbody> </table>	IN_TEON	Setting	0	TE pin is used.	1	TE pin is not used. Set TELOM (35h command) to 0.						
IN_TEON	Setting												
0	TE pin is used.												
1	TE pin is not used. Set TELOM (35h command) to 0.												
	X = Don't care												
Restriction	Note: When this command is read via DSI or MDDI, dummy read operation is not performed.												

Display Mode (B4h)

B4h	Display Mode																																	
	W / R	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex																						
Command	—	0	X	1	0	1	1	0	1	0	0	B4h																						
1 st parameter	R	1	X	0	0	0	0	0	0	DM[1]	DM[0]	0Xh																						
Description	DM[1:0] These bits are used to select display operation when I ² C or DBI Type B is selected. The R61529 allows switching display operation between internal clock operation and external display operation by DM[1:0] setting. Switching from MIPI DPI operation to VSYNC interface operation and vice versa is prohibited. Setting of these bits can be changed in Sleep mode only and not guaranteed in other modes. <table border="1" style="margin-top: 10px;"> <thead> <tr> <th>DM[1:0]</th> <th>Display mode</th> </tr> </thead> <tbody> <tr> <td rowspan="4">I²C Modes 1 and 2</td> <td>2'h0</td> <td>Internal oscillation clock</td> </tr> <tr> <td>2'h1</td> <td>MIPI DPI</td> </tr> <tr> <td>2'h2</td> <td>Setting inhibited</td> </tr> <tr> <td>2'h3</td> <td>Setting inhibited</td> </tr> </tbody> </table> <table border="1" style="margin-top: 10px;"> <thead> <tr> <th>DM[1:0]</th> <th>Display mode</th> </tr> </thead> <tbody> <tr> <td rowspan="4">MIPI DBI Type B 8, 16, 18, 24 bits</td> <td>2'h0</td> <td>Internal oscillation clock</td> </tr> <tr> <td>2'h1</td> <td>Setting inhibited</td> </tr> <tr> <td>2'h2</td> <td>VSYNC interface</td> </tr> <tr> <td>2'h3</td> <td>Setting inhibited</td> </tr> </tbody> </table> X = Don't care												DM[1:0]	Display mode	I ² C Modes 1 and 2	2'h0	Internal oscillation clock	2'h1	MIPI DPI	2'h2	Setting inhibited	2'h3	Setting inhibited	DM[1:0]	Display mode	MIPI DBI Type B 8, 16, 18, 24 bits	2'h0	Internal oscillation clock	2'h1	Setting inhibited	2'h2	VSYNC interface	2'h3	Setting inhibited
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Restriction	Note: When this command is read via DSI or MDDI, dummy read operation is not performed.																																	

Read Checksum and ECC Error Count (B5h)

B5h	Read Checksum and ECC Error Count											
	W / R	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	—	0	X	1	0	1	1	0	1	0	1	B5h
Dummy Parameter	R	1	X	X	X	X	X	X	X	X	X	XXh
1st parameter	R	1	X	CSOU T[7]	CSOU T[6]	CSOU T[5]	CSOU T[4]	CSOU T[3]	CSOU T[2]	CSOU T[1]	CSOU T[0]	XXh
2nd parameter	R	1	X	DSIEC P[7]	DSIEC P[6]	DSIEC P[5]	DSIEC P[4]	DSIEC P[3]	DSIEC P[2]	DSIEC P[1]	DSIEC P[0]	XXh
3rd parameter	R	1	X	DSIEC E[7]	DSIEC E[6]	DSIEC E[5]	DSIEC E[4]	DSIEC E[3]	DSIEC E[2]	DSIEC E[1]	DSIEC E[0]	XXh
Description	<p>CSOUT[7:0] These bits read checksum error count values. When checksum error occurs in DSI Long Packet reception, the value is counted up. When these bits are read, they are cleared to 8'h00.</p> <p>DSIECP[7:0] These bits read single-bit ECC error count values. When 1-bit ECC error occurs in DSI Packet Header reception, the value is counted up. When these bits are read, they are cleared to 8'h00.</p> <p>DSIECE[7:0] These bits read multi-bit ECC error count values. When 2-bit-or-more ECC error occurs in DSI Packet Header reception, the value is counted up. When these bits are read, they are cleared to 8'h00.</p> <p>X = Don't care</p>											
Restriction	Note: When this command is read via DSI, dummy read operation is not performed.											

DSI Control (B6h)

B6h	DSI Control																																																																										
	W / R	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex																																																															
Command	—	0	X	1	0	1	1	0	1	1	0	B6h																																																															
1 st parameter	W / R	1	X	0	1	0	1	0	0	DSITX DIV[1]	DSITX DIV[0]	5Xh																																																															
2 nd parameter	W / R	1	X	DSI_THS SET[1]	DSI_THS SET [0]	0	0	0	0	1	1	X3h																																																															
Description	DSITXDIV[1:0] These bits are used to define the division ratio to generate transmit clock in LP mode. If DSICLK stops, data is transmitted by using the internal oscillator (14MHz). <table border="1" style="margin-left: 20px;"> <tr> <th>DSITXDIV[1:0]</th> <th>DSICLK division ratio</th> </tr> <tr> <td>2'b00</td> <td>fDSICLK/4</td> </tr> <tr> <td>2'b01</td> <td>fDSICLK/8</td> </tr> <tr> <td>2'b10</td> <td>fDSICLK/16</td> </tr> <tr> <td>2'b11</td> <td>fDSICLK/32</td> </tr> </table> DSITXDIV setting example <table border="1" style="margin-left: 20px;"> <thead> <tr> <th rowspan="2">Status of Clock Lane</th> <th colspan="2">Host to R61529</th> <th colspan="3">R61529 to Host</th> </tr> <tr> <th>Bit Rate [Mbps]</th> <th>fDSICLK [MHz]</th> <th>Setting of DSITXDIV [1:0]</th> <th>fTXCLK [MHz]</th> <th>Bit rate [Mbps]</th> </tr> </thead> <tbody> <tr> <td rowspan="8">Active</td> <td>480</td> <td>240</td> <td rowspan="4">2'b10</td> <td>15.0</td> <td>7.50</td> </tr> <tr> <td>440</td> <td>220</td> <td>13.8</td> <td>6.88</td> </tr> <tr> <td>400</td> <td>200</td> <td>12.5</td> <td>6.25</td> </tr> <tr> <td>320</td> <td>160</td> <td rowspan="4">2'b01</td> <td>20.0</td> <td>10.0</td> </tr> <tr> <td>300</td> <td>150</td> <td>18.8</td> <td>4.69</td> </tr> <tr> <td>200</td> <td>100</td> <td>12.5</td> <td>6.25</td> </tr> <tr> <td>160</td> <td>80</td> <td rowspan="2">2'b00</td> <td>20</td> <td>10.0</td> </tr> <tr> <td>100</td> <td>50</td> <td>12.5</td> <td>6.25</td> </tr> <tr> <td>Inactive (Stop)</td> <td>-</td> <td>-</td> <td>-</td> <td>14.0 (fosc)</td> <td>0.3925</td> </tr> </tbody> </table> <p>X = Don't care</p>												DSITXDIV[1:0]	DSICLK division ratio	2'b00	fDSICLK/4	2'b01	fDSICLK/8	2'b10	fDSICLK/16	2'b11	fDSICLK/32	Status of Clock Lane	Host to R61529		R61529 to Host			Bit Rate [Mbps]	fDSICLK [MHz]	Setting of DSITXDIV [1:0]	fTXCLK [MHz]	Bit rate [Mbps]	Active	480	240	2'b10	15.0	7.50	440	220	13.8	6.88	400	200	12.5	6.25	320	160	2'b01	20.0	10.0	300	150	18.8	4.69	200	100	12.5	6.25	160	80	2'b00	20	10.0	100	50	12.5	6.25	Inactive (Stop)	-	-	-	14.0 (fosc)	0.3925
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Description	<p>DSI_THSSET[1:0]</p> <p>These bits are used to change operation frequency according to DSI clock when MIPI DSI is selected.</p> <table border="1"><thead><tr><th rowspan="2">DSI_THSSET[1:0]</th><th colspan="2">Operating frequency (MHz)</th></tr><tr><th>Min</th><th>Max</th></tr></thead><tbody><tr><td>00</td><td>50</td><td>90</td></tr><tr><td>01</td><td>90</td><td>140</td></tr><tr><td>10</td><td>140</td><td>210</td></tr><tr><td>11</td><td>210</td><td>250</td></tr></tbody></table> <p>X = Don't care</p>	DSI_THSSET[1:0]	Operating frequency (MHz)		Min	Max	00	50	90	01	90	140	10	140	210	11	210	250
DSI_THSSET[1:0]	Operating frequency (MHz)																	
	Min	Max																
00	50	90																
01	90	140																
10	140	210																
11	210	250																
Restriction	Note: When this command is read via DSI or MDDI, dummy read operation is not performed.																	

MDDI Control (B7h)

MDDI Control																																				
B7h	W / R	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex																								
Command	—	0	X	1	0	1	1	0	1	1	1	B7h																								
1st parameter	W / R	1	X	0	0	0	0	0	0	CRCSTP	MDCRC	0Xh																								
2nd parameter	W / R	1	X	0	0	0	0	0	0	0	0	00h																								
3rd parameter	W / R	1	X	0	0	0	1	0	MDDI_ICONT_TX[2]	MDDI_ICONT_TX[1]	MDDI_ICONT_TX[0]	1Xh																								
4th parameter	W / R	1	X	0	0	1	0	0	0	0	1	21h																								
Description	MDCRC When MDDI error detection mode is enabled, an output level of the DOUT pin is set to "High" if an error is detected. For details, see "CRC Error Detection Mode Setting" in "MDDI (Mobile Display Digital Interface)." <table border="1"> <thead> <tr> <th>MDCRC</th> <th>CRC error detection mode</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Halt</td> </tr> <tr> <td>1</td> <td>Enable</td> </tr> </tbody> </table> CRCSTP While CRCSTP is set to 1, detection is temporarily disabled. When the DOUT pin returns to "Low" level, CRCSTP is set to 0. CRCSTP is used as an error detection signal. For details, see "CRC Error Detection Mode Setting" in "MDDI (Mobile Display Digital Interface)." MDDI_ICONT_TX[2:0] They are used to adjust bias current for MDDI reverse link. They decide TX output differential signal level. <table border="1"> <thead> <tr> <th>MDDI_ICONT_TX[2:0]</th> <th>Theoretical value of differential output current from Reverse Transmitter.</th> </tr> </thead> <tbody> <tr> <td>3'h0</td> <td>50%</td> </tr> <tr> <td>3'h 1</td> <td>60% Center of values specified by MDDI standard (ver.1.2)</td> </tr> <tr> <td>3'h 2</td> <td>70%</td> </tr> <tr> <td>3'h 3</td> <td>80%</td> </tr> <tr> <td>3'h 4</td> <td>90%</td> </tr> <tr> <td>3'h 5</td> <td>100% Center of values specified by MDDI standard (ver.1.0)</td> </tr> <tr> <td>3'h 6</td> <td>110%</td> </tr> <tr> <td>3'h 7</td> <td>120%</td> </tr> </tbody> </table> X = Don't care												MDCRC	CRC error detection mode	0	Halt	1	Enable	MDDI_ICONT_TX[2:0]	Theoretical value of differential output current from Reverse Transmitter.	3'h0	50%	3'h 1	60% Center of values specified by MDDI standard (ver.1.2)	3'h 2	70%	3'h 3	80%	3'h 4	90%	3'h 5	100% Center of values specified by MDDI standard (ver.1.0)	3'h 6	110%	3'h 7	120%
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Restriction	Note: When this command is read via DSI or MDDI, dummy read operation is not performed.																																			

Backlight Control (1) (B8h)

B8h	Backlight Control (1)											
	W / R	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	—	0	X	1	0	1	1	1	0	0	0	B8h
1 st parameter	W / R	1	X	0	0	0	0	0	0	BLCM	BLCO N	0Xh
2 nd parameter	W / R	1	X	0	0	0	THRE W0[4]	THRE W0[3]	THRE W0[2]	THRE W0[1]	THRE W0[0]	XXh
3 rd parameter	W / R	1	X	0	0	0	THRE W1[4]	THRE W1[3]	THRE W1[2]	THRE W1[1]	THRE W1[0]	XXh
4 th parameter	W / R	1	X	ULMT W0[7]	ULMT W0[6]	ULMT W0[5]	ULMT W0[4]	ULMT W0[3]	ULMT W0[2]	ULMT W0[1]	ULMT W0[0]	XXh
5 th parameter	W / R	1	X	ULMT W1[7]	ULMT W1[6]	ULMT W1[5]	ULMT W1[4]	ULMT W1[3]	ULMT W1[2]	ULMT W1[1]	ULMT W1[0]	XXh
6 th parameter	W / R	1	X	LLMT W0[7]	LLMT W0[6]	LLMT W0[5]	LLMT W0[4]	LLMT W0[3]	LLMT W0[2]	LLMT W0[1]	LLMT W0[0]	XXh
7 th parameter	W / R	1	X	LLMT W1[7]	LLMT W1[6]	LLMT W1[5]	LLMT W1[4]	LLMT W1[3]	LLMT W1[2]	LLMT W1[1]	LLMT W1[0]	XXh
8 th parameter	W / R	1	X	0	0	0	0	PITCH W[3]	PITCH W[2]	PITCH W[1]	PITCH W[0]	0Xh
9 th parameter	W / R	1	X	0	0	0	CGAP W [4]	CGAP W [3]	CGAP W [2]	CGAP W [1]	CGAP W [0]	XXh
10 th parameter	W / R	1	X	LNCO M0	0	0	COEF K0[4]	COEF K0[3]	COEF K0[2]	COEF K0[1]	COEF K0[0]	XXh
11 th parameter	W / R	1	X	LNCO M1	0	0	COEF K1[4]	COEF K1[3]	COEF K1[2]	COEF K1[1]	COEF K1[0]	XXh
12 th parameter	W / R	1	X	TBL3 [7]	TBL3 [6]	TBL3 [5]	TBL3 [4]	TBL3 [3]	TBL3 [2]	TBL3 [1]	TBL3 [0]	XXh
13 th parameter	W / R	1	X	TBL4 [7]	TBL4 [6]	TBL4 [5]	TBL4 [4]	TBL4 [3]	TBL4 [2]	TBL4 [1]	TBL4 [0]	XXh
14 th parameter	W / R	1	X	TBL5 [7]	TBL5 [6]	TBL5 [5]	TBL5 [4]	TBL5 [3]	TBL5 [2]	TBL5 [1]	TBL5 [0]	XXh
15 th parameter	W / R	1	X	TBL6 [7]	TBL6 [6]	TBL6 [5]	TBL6 [4]	TBL6 [3]	TBL6 [2]	TBL6 [1]	TBL6 [0]	XXh
16 th parameter	W / R	1	X	TBL7 [7]	TBL7 [6]	TBL7 [5]	TBL7 [4]	TBL7 [3]	TBL7 [2]	TBL7 [1]	TBL7 [0]	XXh

17 th parameter	W / R	1	X	0	0	0	0	0	0	0	0	00h																																		
18 th parameter	W / R	1	X	0	0	0	0	0	0	0	0	00h																																		
19 th parameter	W / R	1	X	0	0	0	0	0	0	0	0	00h																																		
20 th parameter	W / R	1	X	0	0	0	0	0	0	0	0	00h																																		
Description	<p>Note: Make sure that BLC function is turned off (D0 (the 1st parameter): BLCON=0) when changing parameter values of B8h and switching BLC modes (D1 (the 1st parameter: BLCM)).</p> <p>Write 00h in the 16th parameter.</p> <p>BLCM</p> <p>The bit is used to select BLC mode. There are two sets of bits for each of THREW, ULMTW, LLMTW, COEFK, and LNCOM registers, enabling different settings for different display images.</p> <table border="1"> <thead> <tr> <th>BLCM</th> <th>BLC mode</th> <th colspan="8">Enabled register</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Mode 0</td> <td>THREW0</td> <td>ULMTW0</td> <td>LLMTW0</td> <td>PITCHW</td> <td>CGAPW</td> <td>LNCOM0</td> <td>COEFK0</td> </tr> <tr> <td>1</td> <td>Mode 1</td> <td>THREW1</td> <td>ULMTW1</td> <td>LLMTW1</td> <td></td> <td></td> <td>LNCOM1</td> <td>COEFK1</td> </tr> </tbody> </table> <p>BLCON</p> <p>The bit is used to turn the BLC function ON/OFF.</p> <table border="1"> <thead> <tr> <th>BLCON</th> <th>BLC function</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>OFF</td> </tr> <tr> <td>1</td> <td>ON</td> </tr> </tbody> </table> <p>The BLC function is disabled in Display Invert Mode On. Use BLC function (BLCON = 1) in Normal Mode On and Display Invert Mode Off.</p>												BLCM	BLC mode	Enabled register								0	Mode 0	THREW0	ULMTW0	LLMTW0	PITCHW	CGAPW	LNCOM0	COEFK0	1	Mode 1	THREW1	ULMTW1	LLMTW1			LNCOM1	COEFK1	BLCON	BLC function	0	OFF	1	ON
BLCM	BLC mode	Enabled register																																												
0	Mode 0	THREW0	ULMTW0	LLMTW0	PITCHW	CGAPW	LNCOM0	COEFK0																																						
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Description	<p>THREW0[4:0], THREW1[4:0]</p> <p>The bits are used to specify percentage from the threshold to grayscale number 63 in the total of grayscale data. This is the ratio (percentage) of the maximum number of pixels that makes display image white (= data "63") to the total of pixels by image processing.</p> <p>Percentage of pixels =</p> <p>Number of pixels with the grayscale from the threshold to grayscale No. 63 / Number of all pixels</p> <p>THREW0 is enabled when BLCM=0. THREW1 is enabled when BLCM=1.</p> <table border="1" data-bbox="382 804 711 1522"> <thead> <tr> <th>THREW0[4:0] THREW1[4:0]</th><th>Percentage of pixels</th></tr> </thead> <tbody> <tr><td>5'h00</td><td>0%</td></tr> <tr><td>5'h01</td><td>2%</td></tr> <tr><td>5'h02</td><td>4%</td></tr> <tr><td>5'h03</td><td>6%</td></tr> <tr><td>5'h04</td><td>8%</td></tr> <tr><td>5'h05</td><td>10%</td></tr> <tr><td>5'h06</td><td>12%</td></tr> <tr><td>5'h07</td><td>14%</td></tr> <tr><td>5'h08</td><td>16%</td></tr> <tr><td>5'h09</td><td>18%</td></tr> <tr><td>5'h0A</td><td>20%</td></tr> <tr><td>5'h0B</td><td>22%</td></tr> <tr><td>5'h0C</td><td>24%</td></tr> <tr><td>5'h0D</td><td>26%</td></tr> <tr><td>5'h0E</td><td>28%</td></tr> <tr><td>5'h0F</td><td>30%</td></tr> </tbody> </table> <table border="1" data-bbox="747 804 1076 1522"> <thead> <tr> <th>THREW0[4:0] THREW1[4:0]</th><th>Percentage of pixels</th></tr> </thead> <tbody> <tr><td>5'h10</td><td>32%</td></tr> <tr><td>5'h11</td><td>34%</td></tr> <tr><td>5'h12</td><td>36%</td></tr> <tr><td>5'h13</td><td>38%</td></tr> <tr><td>5'h14</td><td>40%</td></tr> <tr><td>5'h15</td><td>42%</td></tr> <tr><td>5'h16</td><td>44%</td></tr> <tr><td>5'h17</td><td>46%</td></tr> <tr><td>5'h18</td><td>48%</td></tr> <tr><td>5'h19</td><td>50%</td></tr> <tr><td>5'h1A</td><td>52%</td></tr> <tr><td>5'h1B</td><td>54%</td></tr> <tr><td>5'h1C</td><td>56%</td></tr> <tr><td>5'h1D</td><td>58%</td></tr> <tr><td>5'h1E</td><td>60%</td></tr> <tr><td>5'h1F</td><td>62%</td></tr> </tbody> </table>	THREW0[4:0] THREW1[4:0]	Percentage of pixels	5'h00	0%	5'h01	2%	5'h02	4%	5'h03	6%	5'h04	8%	5'h05	10%	5'h06	12%	5'h07	14%	5'h08	16%	5'h09	18%	5'h0A	20%	5'h0B	22%	5'h0C	24%	5'h0D	26%	5'h0E	28%	5'h0F	30%	THREW0[4:0] THREW1[4:0]	Percentage of pixels	5'h10	32%	5'h11	34%	5'h12	36%	5'h13	38%	5'h14	40%	5'h15	42%	5'h16	44%	5'h17	46%	5'h18	48%	5'h19	50%	5'h1A	52%	5'h1B	54%	5'h1C	56%	5'h1D	58%	5'h1E	60%	5'h1F	62%
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Description	ULMTW0[7:0], ULMTW1[7:0]						
The possible maximum value of the threshold grayscale value (Dth) that makes display image white is set in units of 1 grayscale. ULMTW0 is enabled when BLCM=0. ULMTW1 is enabled when BLCM=1.							
ULMTW0[7:0] ULMTW1[7:0]	Maximum scale (Frame memory data)	ULMTW0[7:0] ULMTW1[7:0]	Maximum scale (Frame memory data)	ULMTW0[7:0] ULMTW1[7:0]	Maximum scale (Frame memory data)	ULMTW0[7:0] ULMTW1[7:0]	Maximum scale (Frame memory data)
8'h00	0	8'h10	16	8'h20	32	8'h30	48
8'h01	1	8'h11	17	8'h21	33	8'h31	49
8'h02	2	8'h12	18	8'h22	34	8'h32	50
8'h03	3	8'h13	19	8'h23	35	8'h33	51
8'h04	4	8'h14	20	8'h24	36	8'h34	52
8'h05	5	8'h15	21	8'h25	37	8'h35	53
8'h06	6	8'h16	22	8'h26	38	8'h36	54
8'h07	7	8'h17	23	8'h27	39	8'h37	55
8'h08	8	8'h18	24	8'h28	40	8'h38	56
8'h09	9	8'h19	25	8'h29	41	8'h39	57
8'h0A	10	8'h1A	26	8'h2A	42	8'h3A	58
8'h0B	11	8'h1B	27	8'h2B	43	8'h3B	59
8'h0C	12	8'h1C	28	8'h2C	44	8'h3C	60
8'h0D	13	8'h1D	29	8'h2D	45	8'h3D	61
8'h0E	14	8'h1E	30	8'h2E	46	8'h3E	62
8'h0F	15	8'h1F	31	8'h2F	47	8'h3F	63

Description	ULMTW0[7:0] ULMTW1[7:0]	Maximum scale (Frame memory data)						
8'h40	64		8'h50	80		8'h60	96	
8'h41	65		8'h51	81		8'h61	97	
8'h42	66		8'h52	82		8'h62	98	
8'h43	67		8'h53	83		8'h63	99	
8'h44	68		8'h54	84		8'h64	100	
8'h45	69		8'h55	85		8'h65	101	
8'h46	70		8'h56	86		8'h66	102	
8'h47	71		8'h57	87		8'h67	103	
8'h48	72		8'h58	88		8'h68	104	
8'h49	73		8'h59	89		8'h69	105	
8'h4A	74		8'h5A	90		8'h6A	106	
8'h4B	75		8'h5B	91		8'h6B	107	
8'h4C	76		8'h5C	92		8'h6C	108	
8'h4D	77		8'h5D	93		8'h6D	109	
8'h4E	78		8'h5E	94		8'h6E	110	
8'h4F	79		8'h5F	95		8'h6F	111	

Description	ULMTW0[7:0] ULMTW1[7:0]	Maximum scale (Frame memory data)						
8'h80	128		8'h90	144		8'hA0	160	
8'h81	129		8'h91	145		8'hA1	161	
8'h82	130		8'h92	146		8'hA2	162	
8'h83	131		8'h93	147		8'hA3	163	
8'h84	132		8'h94	148		8'hA4	164	
8'h85	133		8'h95	149		8'hA5	165	
8'h86	134		8'h96	150		8'hA6	166	
8'h87	135		8'h97	151		8'hA7	167	
8'h88	136		8'h98	152		8'hA8	168	
8'h89	137		8'h99	153		8'hA9	169	
8'h8A	138		8'h9A	154		8'hAA	170	
8'h8B	139		8'h9B	155		8'hAB	171	
8'h8C	140		8'h9C	156		8'hAC	172	
8'h8D	141		8'h9D	157		8'hAD	173	
8'h8E	142		8'h9E	158		8'hAE	174	
8'h8F	143		8'h9F	159		8'hAF	175	

Description	ULMTW0[7:0] ULMTW1[7:0]	Maximum scale (Frame memory data)						
8'hC0	192		8'hD0	208		8'hE0	224	
8'hC1	193		8'hD1	209		8'hE1	225	
8'hC2	194		8'hD2	210		8'hE2	226	
8'hC3	195		8'hD3	211		8'hE3	227	
8'hC4	196		8'hD4	212		8'hE4	228	
8'hC5	197		8'hD5	213		8'hE5	229	
8'hC6	198		8'hD6	214		8'hE6	230	
8'hC7	199		8'hD7	215		8'hE7	231	
8'hC8	200		8'hD8	216		8'hE8	232	
8'hC9	201		8'hD9	217		8'hE9	233	
8'hCA	202		8'hDA	218		8'hEA	234	
8'hCB	203		8'hDB	219		8'hEB	235	
8'hCC	204		8'hDC	220		8'hEC	236	
8'hCD	205		8'hDD	221		8'hED	237	
8'hCE	206		8'hDE	222		8'hEE	238	
8'hCF	207		8'hDF	223		8'hEF	239	

Description	LLMTW0[7:0], LLMTW1[7:0]						
The possible minimum value of the threshold grayscale value (Dth) that makes display image white is set in units of 1 grayscale. LLMTW0 is enabled when BLCM=0. LLMTW1 is enabled when BLCM=1.							
LLMTW0[7:0] LLMTW1[7:0]	Minimum scale (Frame memory data)	LLMTW0[7:0] LLMTW1[7:0]	Minimum scale (Frame memory data)	LLMTW0[7:0] LLMTW1[7:0]	Minimum scale (Frame memory data)	LLMTW0[7:0] LLMTW1[7:0]	Minimum scale (Frame memory data)
8'h00	0	8'h10	16	8'h20	32	8'h30	48
8'h01	1	8'h11	17	8'h21	33	8'h31	49
8'h02	2	8'h12	18	8'h22	34	8'h32	50
8'h03	3	8'h13	19	8'h23	35	8'h33	51
8'h04	4	8'h14	20	8'h24	36	8'h34	52
8'h05	5	8'h15	21	8'h25	37	8'h35	53
8'h06	6	8'h16	22	8'h26	38	8'h36	54
8'h07	7	8'h17	23	8'h27	39	8'h37	55
8'h08	8	8'h18	24	8'h28	40	8'h38	56
8'h09	9	8'h19	25	8'h29	41	8'h39	57
8'h0A	10	8'h1A	26	8'h2A	42	8'h3A	58
8'h0B	11	8'h1B	27	8'h2B	43	8'h3B	59
8'h0C	12	8'h1C	28	8'h2C	44	8'h3C	60
8'h0D	13	8'h1D	29	8'h2D	45	8'h3D	61
8'h0E	14	8'h1E	30	8'h2E	46	8'h3E	62
8'h0F	15	8'h1F	31	8'h2F	47	8'h3F	63

Description	LLMTW0[7:0] LLMTW1[7:0]	Minimum scale (Frame memory data)						
8'h40	64		8'h50	80		8'h60	96	
8'h41	65		8'h51	81		8'h61	97	
8'h42	66		8'h52	82		8'h62	98	
8'h43	67		8'h53	83		8'h63	99	
8'h44	68		8'h54	84		8'h64	100	
8'h45	69		8'h55	85		8'h65	101	
8'h46	70		8'h56	86		8'h66	102	
8'h47	71		8'h57	87		8'h67	103	
8'h48	72		8'h58	88		8'h68	104	
8'h49	73		8'h59	89		8'h69	105	
8'h4A	74		8'h5A	90		8'h6A	106	
8'h4B	75		8'h5B	91		8'h6B	107	
8'h4C	76		8'h5C	92		8'h6C	108	
8'h4D	77		8'h5D	93		8'h6D	109	
8'h4E	78		8'h5E	94		8'h6E	110	
8'h4F	79		8'h5F	95		8'h6F	111	

Description	LLMTW0[7:0] LLMTW1[7:0]	Minimum scale (Frame memory data)						
8'h80	128		8'h90	144		8'hA0	160	
8'h81	129		8'h91	145		8'hA1	161	
8'h82	130		8'h92	146		8'hA2	162	
8'h83	131		8'h93	147		8'hA3	163	
8'h84	132		8'h94	148		8'hA4	164	
8'h85	133		8'h95	149		8'hA5	165	
8'h86	134		8'h96	150		8'hA6	166	
8'h87	135		8'h97	151		8'hA7	167	
8'h88	136		8'h98	152		8'hA8	168	
8'h89	137		8'h99	153		8'hA9	169	
8'h8A	138		8'h9A	154		8'hAA	170	
8'h8B	139		8'h9B	155		8'hAB	171	
8'h8C	140		8'h9C	156		8'hAC	172	
8'h8D	141		8'h9D	157		8'hAD	173	
8'h8E	142		8'h9E	158		8'hAE	174	
8'h8F	143		8'h9F	159		8'hAF	175	

Description	LLMTW0[7:0] LLMTW1[7:0]	Minimum scale (Frame memory data)						
8'hC0	192		8'hD0	208		8'hE0	224	
8'hC1	193		8'hD1	209		8'hE1	225	
8'hC2	194		8'hD2	210		8'hE2	226	
8'hC3	195		8'hD3	211		8'hE3	227	
8'hC4	196		8'hD4	212		8'hE4	228	
8'hC5	197		8'hD5	213		8'hE5	229	
8'hC6	198		8'hD6	214		8'hE6	230	
8'hC7	199		8'hD7	215		8'hE7	231	
8'hC8	200		8'hD8	216		8'hE8	232	
8'hC9	201		8'hD9	217		8'hE9	233	
8'hCA	202		8'hDA	218		8'hEA	234	
8'hCB	203		8'hDB	219		8'hEB	235	
8'hCC	204		8'hDC	220		8'hEC	236	
8'hCD	205		8'hDD	221		8'hED	237	
8'hCE	206		8'hDE	222		8'hEE	238	
8'hCF	207		8'hDF	223		8'hEF	239	
Note: LLMTW0[7:0] and LLMTW1[7:0] values are restricted as above table according to COEFK0[4:0] and COEFK1[4:0] values. Make sure to follow the above minimum LLMTW*[7:0] setting to each COEFK*[4:0] value.								

<p>Description</p> <p>PITCHW0[3:0], PITCHW1[3:0]</p> <p>This parameter sets the amount of change of threshold grayscale value (Dth) that makes display image white per frame in units of one half of the grayscale.</p> <table border="1" style="width: 100%; border-collapse: collapse; text-align: center;"> <thead> <tr> <th style="background-color: #cccccc;">PITCHW[3:0]</th><th style="background-color: #cccccc;">Amount of change (grayscale)</th></tr> </thead> <tbody> <tr><td>4'h0</td><td>Setting inhibited</td></tr> <tr><td>4'h1</td><td>1/2 grayscale</td></tr> <tr><td>4'h2</td><td>1 grayscale</td></tr> <tr><td>4'h3</td><td>3/2 grayscales</td></tr> <tr><td>4'h4</td><td>2 grayscales</td></tr> <tr><td>4'h5</td><td>5/2 grayscales</td></tr> <tr><td>4'h6</td><td>3 grayscales</td></tr> <tr><td>4'h7</td><td>7/2 grayscales</td></tr> <tr><td>4'h8</td><td>4 grayscales</td></tr> <tr><td>4'h9</td><td>9/2 grayscales</td></tr> <tr><td>4'hA</td><td>5 grayscales</td></tr> <tr><td>4'hB</td><td>11/2 grayscales</td></tr> <tr><td>4'hC</td><td>6 grayscales</td></tr> <tr><td>4'hD</td><td>13/2 grayscales</td></tr> <tr><td>4'hE</td><td>7 grayscales</td></tr> <tr><td>4'hF</td><td>15/2 grayscales</td></tr> </tbody> </table>	PITCHW[3:0]	Amount of change (grayscale)	4'h0	Setting inhibited	4'h1	1/2 grayscale	4'h2	1 grayscale	4'h3	3/2 grayscales	4'h4	2 grayscales	4'h5	5/2 grayscales	4'h6	3 grayscales	4'h7	7/2 grayscales	4'h8	4 grayscales	4'h9	9/2 grayscales	4'hA	5 grayscales	4'hB	11/2 grayscales	4'hC	6 grayscales	4'hD	13/2 grayscales	4'hE	7 grayscales	4'hF	15/2 grayscales	<p>LNCOM0, LNCOM1</p> <p>LNCOM0, LNCOM1: Used to select 2- or 4-point interpolation when BLC function is used. When BLCM is set to 0, LNCOM0 is enabled. When BLCM is set to 1, LNCOM1 is enabled.</p> <p>BLCM=0</p> <table border="1" style="width: 100%; border-collapse: collapse; text-align: center;"> <thead> <tr> <th style="background-color: #cccccc;">LNCOM0</th><th style="background-color: #cccccc;">Interpolation</th></tr> </thead> <tbody> <tr><td>0</td><td>4-point interpolation</td></tr> <tr><td>1</td><td>2-point interpolation</td></tr> </tbody> </table> <p>BLCM=1</p> <table border="1" style="width: 100%; border-collapse: collapse; text-align: center;"> <thead> <tr> <th style="background-color: #cccccc;">LNCOM1</th><th style="background-color: #cccccc;">Interpolation</th></tr> </thead> <tbody> <tr><td>0</td><td>4-point interpolation</td></tr> <tr><td>1</td><td>2-point interpolation</td></tr> </tbody> </table>	LNCOM0	Interpolation	0	4-point interpolation	1	2-point interpolation	LNCOM1	Interpolation	0	4-point interpolation	1	2-point interpolation
PITCHW[3:0]	Amount of change (grayscale)																																														
4'h0	Setting inhibited																																														
4'h1	1/2 grayscale																																														
4'h2	1 grayscale																																														
4'h3	3/2 grayscales																																														
4'h4	2 grayscales																																														
4'h5	5/2 grayscales																																														
4'h6	3 grayscales																																														
4'h7	7/2 grayscales																																														
4'h8	4 grayscales																																														
4'h9	9/2 grayscales																																														
4'hA	5 grayscales																																														
4'hB	11/2 grayscales																																														
4'hC	6 grayscales																																														
4'hD	13/2 grayscales																																														
4'hE	7 grayscales																																														
4'hF	15/2 grayscales																																														
LNCOM0	Interpolation																																														
0	4-point interpolation																																														
1	2-point interpolation																																														
LNCOM1	Interpolation																																														
0	4-point interpolation																																														
1	2-point interpolation																																														

Description	CGAPW0[4:0], CGAPW1[4:0]		
The difference of the two grayscales counted by the threshold counter is set in units of one half of the grayscale.			
CGAPW[4:0]	Grayscale difference	CGAPW[4:0]	
5'h00	Setting inhibited	5'h10	2 grayscales
5'h01	1/2 grayscale	5'h11	17/2 grayscales
5'h02	1 grayscale	5'h12	9 grayscales
5'h03	3/2 grayscale	5'h13	19/2 grayscales
5'h04	2 grayscales	5'h14	10 grayscales
5'h05	5/2 grayscales	5'h15	21/2 grayscales
5'h06	3 grayscales	5'h16	11 grayscales
5'h07	7/2 grayscales	5'h17	23/2 grayscales
5'h08	4 grayscales	5'h18	12 grayscales
5'h09	9/2 grayscales	5'h19	25/2 grayscales
5'h0A	5 grayscales	5'h1A	13 grayscales
5'h0B	11/2 grayscales	5'h1B	27/2 grayscales
5'h0C	6 grayscales	5'h1C	14 grayscales
5'h0D	13/2 grayscales	5'h1D	29/2 grayscales
5'h0E	7 grayscales	5'h1E	15 grayscales
5'h0F	15/2 grayscales	5'h1F	31/2 grayscales

Description	COEFK0[4:0] , COEFK1[4:0]	
This register sets the range of the grayscale that prevents display image from being white, according to the ratio of the grayscale mentioned here to the grayscale number that makes data white.		
	COEFK0[4:0] COEFK1[4:0]	Range of grayscale preventing image from being white
	5'h00	0%
	5'h01	6.25%
	5'h02	12.50%
	5'h03	18.75%
	5'h04	25.00%
	5'h05	31.25%
	5'h06	37.50%
	5'h07	43.75%
	5'h08	50.00%
	5'h09	56.25%
	5'h0A	62.50%
	5'h0B	68.75%
	5'h0C	75.00%
	5'h0D	81.25%
	5'h0E	87.50%
	5'h0F	93.75%
	COEFK0[4:0] COEFK1[4:0]	Range of grayscale preventing image from being white
	5'h10	100.00%
	5'h11	Setting inhibited
	5'h12	Setting inhibited
	5'h13	Setting inhibited
	5'h14	Setting inhibited
	5'h15	Setting inhibited
	5'h16	Setting inhibited
	5'h17	Setting inhibited
	5'h18	Setting inhibited
	5'h19	Setting inhibited
	5'h1A	Setting inhibited
	5'h1B	Setting inhibited
	5'h1C	Setting inhibited
	5'h1D	Setting inhibited
	5'h1E	Setting inhibited
	5'h1F	Setting inhibited

Description	TBL_MIN[7:0], TBL3[7:0], TBL4[7:0], TBL5[7:0], TBL6[7:0], TBL7[7:0]
The reference value used for interpolation calculation in gamma table are set by TBL_*.	
TBL_* [7:0]	8-bit reference value
8'h00	8'h00
8'h01	8'h01
8'h02	8'h02
8'h03	8'h03
8'h04	8'h04
8'h05	8'h05
8'h06	8'h06
8'h07	8'h07
8'h08	8'h08
8'h09	8'h09
8'h0A	8'h0A
8'h0B	8'h0B
8'h0C	8'h0C
8'h0D	8'h0D
8'h0E	8'h0E
8'h0F	8'h0F
8'h10	8'h10
8'h11	8'h11
8'h12	8'h12
8'h13	8'h13
8'h14	8'h14
8'h15	8'h15
8'h16	8'h16
8'h17	8'h17
8'h18	8'h18
8'h19	8'h19
8'h1A	8'h1A
8'h1B	8'h1B
8'h1C	8'h1C
8'h1D	8'h1D
8'h1E	8'h1E
8'h1F	8'h1F
TBL_* [7:0]	8-bit reference value
8'h20	8'h20
8'h21	8'h21
8'h22	8'h22
8'h23	8'h23
8'h24	8'h24
8'h25	8'h25
8'h26	8'h26
8'h27	8'h27
8'h28	8'h28
8'h29	8'h29
8'h2A	8'h2A
8'h2B	8'h2B
8'h2C	8'h2C
8'h2D	8'h2D
8'h2E	8'h2E
8'h2F	8'h2F
8'h30	8'h30
8'h31	8'h31
8'h32	8'h32
8'h33	8'h33
8'h34	8'h34
8'h35	8'h35
8'h36	8'h36
8'h37	8'h37
8'h38	8'h38
8'h39	8'h39
8'h3A	8'h3A
8'h3B	8'h3B
8'h3C	8'h3C
8'h3D	8'h3D
8'h3E	8'h3E
8'h3F	8'h3F
TBL_* [7:0]	8-bit reference value
8'h40	8'h40
8'h41	8'h41
8'h42	8'h42
8'h43	8'h43
8'h44	8'h44
8'h45	8'h45
8'h46	8'h46
8'h47	8'h47
8'h48	8'h48
8'h49	8'h49
8'h4A	8'h4A
8'h4B	8'h4B
8'h4C	8'h4C
8'h4D	8'h4D
8'h4E	8'h4E
8'h4F	8'h4F
8'h50	8'h50
8'h51	8'h51
8'h52	8'h52
8'h53	8'h53
8'h54	8'h54
8'h55	8'h55
8'h56	8'h56
8'h57	8'h57
8'h58	8'h58
8'h59	8'h59
8'h5A	8'h5A
8'h5B	8'h5B
8'h5C	8'h5C
8'h5D	8'h5D
8'h5E	8'h5E
8'h5F	8'h5F
TBL_* [7:0]	8-bit reference value
8'h60	8'h60
8'h61	8'h61
8'h62	8'h62
8'h63	8'h63
8'h64	8'h64
8'h65	8'h65
8'h66	8'h66
8'h67	8'h67
8'h68	8'h68
8'h69	8'h69
8'h6A	8'h6A
8'h6B	8'h6B
8'h6C	8'h6C
8'h6D	8'h6D
8'h6E	8'h6E
8'h6F	8'h6F
8'h70	8'h70
8'h71	8'h71
8'h72	8'h72
8'h73	8'h73
8'h74	8'h74
8'h75	8'h75
8'h76	8'h76
8'h77	8'h77
8'h78	8'h78
8'h79	8'h79
8'h7A	8'h7A
8'h7B	8'h7B
8'h7C	8'h7C
8'h7D	8'h7D
8'h7E	8'h7E
8'h7F	8'h7F

Description	TBL_* [7:0]	8-bit reference value	TBL_* [7:0]	8-bit reference value	TBL_* [7:0]	8-bit reference value	TBL_* [7:0]	8-bit reference value
	8'h80	8'h80	8'hA0	8'hA0	8'hC0	8'hC0	8'hE0	8'hE0
	8'h81	8'h81	8'hA1	8'hA1	8'hC1	8'hC1	8'hE1	8'hE1
	8'h82	8'h82	8'hA2	8'hA2	8'hC2	8'hC2	8'hE2	8'hE2
	8'h83	8'h83	8'hA3	8'hA3	8'hC3	8'hC3	8'hE3	8'hE3
	8'h84	8'h84	8'hA4	8'hA4	8'hC4	8'hC4	8'hE4	8'hE4
	8'h85	8'h85	8'hA5	8'hA5	8'hC5	8'hC5	8'hE5	8'hE5
	8'h86	8'h86	8'hA6	8'hA6	8'hC6	8'hC6	8'hE6	8'hE6
	8'h87	8'h87	8'hA7	8'hA7	8'hC7	8'hC7	8'hE7	8'hE7
	8'h88	8'h88	8'hA8	8'hA8	8'hC8	8'hC8	8'hE8	8'hE8
	8'h89	8'h89	8'hA9	8'hA9	8'hC9	8'hC9	8'hE9	8'hE9
	8'h8A	8'h8A	8'hAA	8'hAA	8'hCA	8'hCA	8'hEA	8'hEA
	8'h8B	8'h8B	8'hAB	8'hAB	8'hCB	8'hCB	8'hEB	8'hEB
	8'h8C	8'h8C	8'hAC	8'hAC	8'hCC	8'hCC	8'hEC	8'hEC
	8'h8D	8'h8D	8'hAD	8'hAD	8'hCD	8'hCD	8'hED	8'hED
	8'h8E	8'h8E	8'hAE	8'hAE	8'hCE	8'hCE	8'hEE	8'hEE
	8'h8F	8'h8F	8'hAF	8'hAF	8'hCF	8'hCF	8'hEF	8'hEF
	8'h90	8'h90	8'hB0	8'hB0	8'hD0	8'hD0	8'hF0	8'hF0
	8'h91	8'h91	8'hB1	8'hB1	8'hD1	8'hD1	8'hF1	8'hF1
	8'h92	8'h92	8'hB2	8'hB2	8'hD2	8'hD2	8'hF2	8'hF2
	8'h93	8'h93	8'hB3	8'hB3	8'hD3	8'hD3	8'hF3	8'hF3
	8'h94	8'h94	8'hB4	8'hB4	8'hD4	8'hD4	8'hF4	8'hF4
	8'h95	8'h95	8'hB5	8'hB5	8'hD5	8'hD5	8'hF5	8'hF5
	8'h96	8'h96	8'hB6	8'hB6	8'hD6	8'hD6	8'hF6	8'hF6
	8'h97	8'h97	8'hB7	8'hB7	8'hD7	8'hD7	8'hF7	8'hF7
	8'h98	8'h98	8'hB8	8'hB8	8'hD8	8'hD8	8'hF8	8'hF8
	8'h99	8'h99	8'hB9	8'hB9	8'hD9	8'hD9	8'hF9	8'hF9
	8'h9A	8'h9A	8'hBA	8'hBA	8'hDA	8'hDA	8'hFA	8'hFA
	8'h9B	8'h9B	8'hBB	8'hBB	8'hDB	8'hDB	8'hFB	8'hFB
	8'h9C	8'h9C	8'hBC	8'hBC	8'hDC	8'hDC	8'hFC	8'hFC
	8'h9D	8'h9D	8'hBD	8'hBD	8'hDD	8'hDD	8'hFD	8'hFD
	8'h9E	8'h9E	8'hBE	8'hBE	8'hDE	8'hDE	8'hFE	8'hFE
	8'h9F	8'h9F	8'hBF	8'hBF	8'hDF	8'hDF	8'hFF	8'hFF
	X = Don't care							
Restriction	Note: When this command is read via DSI or MDDI, dummy read operation is not performed.							

Backlight Control (2) (B9h)

B9h	Backlight Control (2)											
	W / R	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	—	0	X	1	0	1	1	1	0	0	1	B9h
1 st parameter	W / R	1	X	0	0	0	0	0	0	0	PWM ON	0Xh
2 nd parameter	W / R	1	X	BDCV [7]	BDCV [6]	BDCV [5]	BDCV [4]	BDCV [3]	BDCV [2]	BDCV [1]	BDCV [0]	XXh
3 rd parameter	W / R	1	X	PWMDI V [7]	PWMDI V [6]	PWMDI V [5]	PWMDI V [4]	PWMDI V [3]	PWMDI V [2]	PWMDI V [1]	PWMDI V [0]	XXh
4 th parameter	W / R	1	X	0	0	0	PWMW M	LEDP WME	0	0	0	XXh
Description	PWMON, PWMWM PWMWM = 0: Controls On/Off of the PWM output according to Display On/Off state. PWMWM = 1: Controls On/Off of the PWM output according to PWMON setting. Note that LEDPWM is OFF when in Sleep Mode regardless of PWMON value. LEDPWME LEDPWME pin output enable bit. In the system configuration using no LEDPWM pin, set the bit to 0. In the system configuration using LEDPWM pin, set the bit to 1. This setting can be changed only in Sleep Mode On. Do not change setting when the R61529 is operating.											
LEDPWME	PWMWM	PWMON	BLCON	RDPWM		LEDPWM output	Note					
0	0	*	0	BDCV		0%						
			1	BLC*BDCV		0%						
	1	0	0	0%		0%						
			1	Setting inhibited		Setting inhibited						
		1	0	BDCV		0%						
			1	BLC*BDCV		0%	*2					
1	0	*	0	BDCV		BDCV	*1					
			1	BLC*BDCV		BLC*BDCV	*1					
	1	0	0	0%		0%						
			1	Setting inhibited		Setting inhibited						
		1	0	BDCV		BDCV						
			1	BLC*BDCV		BLC*BDCV	*2					

Notes:

- If PWMWM = 0, On/Off of the PWM output is automatically controlled according to display ON/Off state.
 Display Off: Sleep Mode On or set_display_off
 Display On: sleep Mode Off and set_display_on
- If PWMWM = 1, RDPWM and LEDPWM outputs cause BDCV value to be read during Display Off.

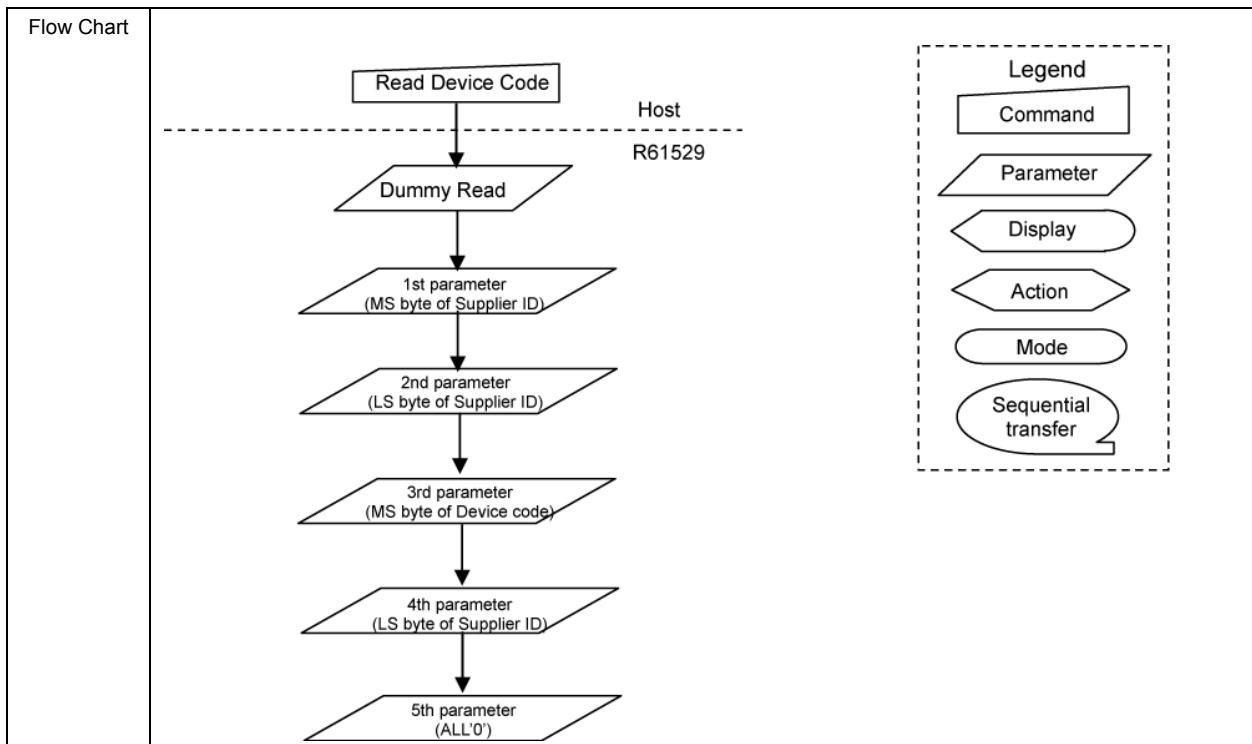
Description	<p>BDCV[7:0]</p> <p>PWM signal's width is selected from 256 values between 8'hFF and 8'h00 when LED is adjusted externally.</p> <p>BLCON=0: PWM signal whose width is determined by BDCV[7:0] is output.</p> <p>BLCON=1: PWM signal whose width is determined by (BDCV*BLC).</p> <table border="1"> <thead> <tr> <th>BDCV[7:0]</th> <th>Amount of light</th> </tr> </thead> <tbody> <tr> <td>8'h00</td> <td>None (0%)</td> </tr> <tr> <td>8'h01</td> <td>1/255</td> </tr> <tr> <td>8'h02</td> <td>2/255</td> </tr> <tr> <td>8'h03</td> <td>3/255</td> </tr> <tr> <td>:</td> <td>:</td> </tr> <tr> <td>8'hFE</td> <td>254/255</td> </tr> <tr> <td>8'hFF</td> <td>255/255 (100%)</td> </tr> </tbody> </table> <p>PWMDIV[7:0]</p> <p>The bit is used to define frequency of PWM signal that is output from LEDPWM pin.</p> <table border="1"> <thead> <tr> <th>PWMDIV[7:0]</th> <th>LEDPWM frequency</th> </tr> </thead> <tbody> <tr> <td>8'h00</td> <td>54.9KHz</td> </tr> <tr> <td>8'h01</td> <td>27.4KHz</td> </tr> <tr> <td>8'h02</td> <td>18.3KHz</td> </tr> <tr> <td>8'h03</td> <td>13.7KHz</td> </tr> <tr> <td>8'h04 – 8'h06</td> <td>Setting inhibited</td> </tr> <tr> <td>8'h07</td> <td>6.86KHz</td> </tr> <tr> <td>8'h08 – 8'h0E</td> <td>Setting inhibited</td> </tr> <tr> <td>8'h0F</td> <td>3.43KHz</td> </tr> </tbody> </table> <table border="1"> <thead> <tr> <th>PWMDIV[7:0]</th> <th>LEDPWM frequency</th> </tr> </thead> <tbody> <tr> <td>8'h10-8'h1E</td> <td>Setting inhibited</td> </tr> <tr> <td>8'h1F</td> <td>1.72KHz</td> </tr> <tr> <td>8'h20-8'h3E</td> <td>Setting inhibited</td> </tr> <tr> <td>8'h3F</td> <td>0.86KHz</td> </tr> <tr> <td>8'h40-8'h7E</td> <td>Setting inhibited</td> </tr> <tr> <td>8'h7F</td> <td>0.43KHz</td> </tr> <tr> <td>8'h80-8'hFE</td> <td>Setting inhibited</td> </tr> <tr> <td>8'hFF</td> <td>0.21KHz</td> </tr> </tbody> </table> <p>Note: These values are typical values. The maximum variance is ±7%.</p> <pre> graph TD PWMON[PWMON] --> BLC[BLC] PWMMWM[PWMMWM] --> BLC BLC --> BLC_out(()) BDCV[BDCV] --> BLC_out BLC_out --> Multiplier(()) Multiplier --> PWM[PWM] LEDPWME[LEDPWME] --> PWM PWM --> LEDPWM[LEDPWM] RDPWM[RDPWM] --> PWM </pre> <p>X = Don't care</p>	BDCV[7:0]	Amount of light	8'h00	None (0%)	8'h01	1/255	8'h02	2/255	8'h03	3/255	:	:	8'hFE	254/255	8'hFF	255/255 (100%)	PWMDIV[7:0]	LEDPWM frequency	8'h00	54.9KHz	8'h01	27.4KHz	8'h02	18.3KHz	8'h03	13.7KHz	8'h04 – 8'h06	Setting inhibited	8'h07	6.86KHz	8'h08 – 8'h0E	Setting inhibited	8'h0F	3.43KHz	PWMDIV[7:0]	LEDPWM frequency	8'h10-8'h1E	Setting inhibited	8'h1F	1.72KHz	8'h20-8'h3E	Setting inhibited	8'h3F	0.86KHz	8'h40-8'h7E	Setting inhibited	8'h7F	0.43KHz	8'h80-8'hFE	Setting inhibited	8'hFF	0.21KHz
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Restriction	Note: When this command is read via DSI or MDDI, dummy read operation is not performed.																																																				

Backlight Control (3) (BAh)

Backlight Control (3) (Read PWM Data)												
BAh	W / R	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	—	0	x	1	0	1	1	1	0	1	0	BAh
Dummy Parameter	R	1	X	X	X	X	X	X	X	X	X	XXh
1 st parameter	R	1	x	RDPWM[7]	RDPWM[6]	RDPWM[5]	RDPWM[4]	RDPWM[3]	RDPWM[2]	RDPWM[1]	RDPWM[0]	XXh
Description	RDPWM[7:0] The command is used to read LED brightness data for LEDPWM signal. X = Don't care											
Restriction	Read data is invalid in Sleep Mode On. Note: When this command is read via DSI or MDDI, dummy read operation is not performed.											
Flow Chart	<pre> graph TD A[Read PWM Data] --> B{Dummy Read} B --> C[/Send 1st parameter RDPWM[7:0]/] style A fill:#fff,stroke:#000,stroke-width:1px style B fill:#fff,stroke:#000,stroke-width:1px style C fill:#fff,stroke:#000,stroke-width:1px </pre> <p>The flowchart illustrates the sequence of operations. It starts with a rectangular box labeled "Read PWM Data". An arrow points down to a diamond-shaped box labeled "Dummy Read". Another arrow points down to a trapezoidal box labeled "Send 1st parameter RDPWM[7:0]". To the right of the flowchart is a legend enclosed in a dashed box:</p> <ul style="list-style-type: none"> Command (rectangle) Parameter (trapezoid) Display (diamond) Action (parallelogram) Mode (oval) Sequential transfer (bubble) 											

Device Code Read (BFh)

BFh	Device Code Read											
	W / R	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	—	0	X	1	0	1	1	1	1	1	1	BFh
Dummy parameter	R	1	X	X	X	X	X	X	X	X	X	XXh
1 st parameter	R	1	X	0	0	0	0	0	0	0	1	01h
2 nd parameter	R	1	X	0	0	1	0	0	0	1	0	22h
3 rd parameter	R	1	X	0	0	0	1	0	1	0	1	15h
4 th parameter	R	1	X	0	0	1	0	1	0	0	1	29h
5 th parameter	R	1	X	0	0	0	0	0	0	0	0	00h
Description	The parameters are used to read the information as follows. 1 st parameter: Returns the upper byte "01h" of Renesas Technology's Supplier ID decided by MIPI Alliance. 2 nd parameter: Returns the lower byte "22h" of Renesas Technology's Supplier ID decided by MIPI Alliance. 3 rd parameter: Returns the upper byte "15h" of product code of this LSI. 4 th parameter: Returns the lower byte "29h" of product code of this LSI. X = Don't care											
Restriction	Note: When this command is read via DSI or MDDI, dummy read operation is not performed.											



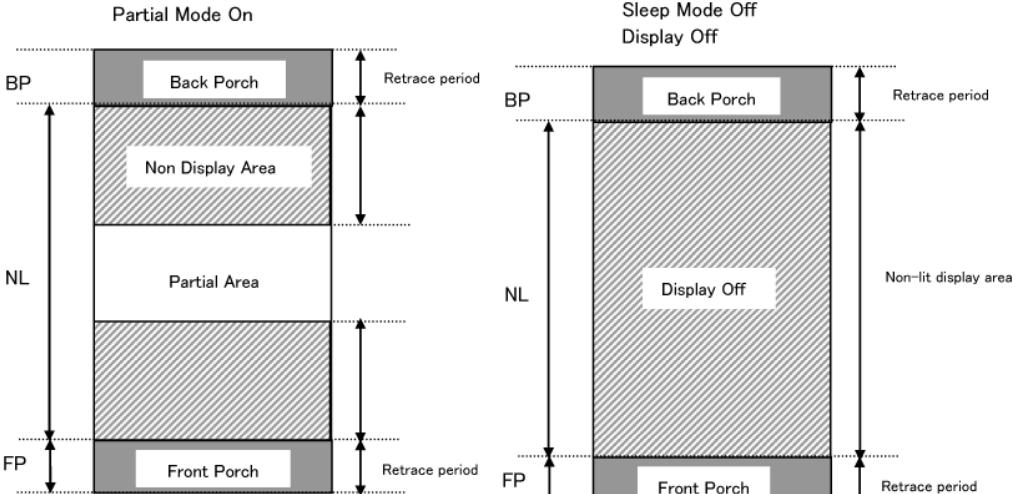
Panel Control Command**Panel Driving Setting (C0h)**

C0h	Panel Driving Setting											
	W / R	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	—	0	X	1	1	0	0	0	0	0	0	C0h
1 st parameter	W / R	1	X	0	0	0	REV	SM	GS	BGR	SS	XXh
2 nd parameter	W / R	1	X	NL[7]	NL[6]	NL[5]	NL[4]	NL[3]	NL[2]	NL[1]	1	XXh
3 rd parameter	W / R	1	X	0	NL[8]	SCN [5]	SCN [4]	SCN [3]	SCN [2]	SCN [1]	SCN [0]	XXh
4 th parameter	W / R	1	X	0	0	0	1	0	0	BLV	PTV	1Xh
5 th parameter	W / R	1	X	0	0	0	NDL	PTDC	0	0	0	XXh
6 th parameter	W / R	1	X	0	0	0	PTG	ISC[3]	ISC[2]	ISC[1]	ISC[0]	XXh
7 th parameter	W / R	1	X	0	0	0	0	BLS	0	0	0	0Xh
8 th parameter	W / R	1	X	PCDIV H[3]	PCDIV H[2]	PCDIV H[1]	PCDIV H[0]	PCDIV L[3]	PCDIV L[2]	PCDIV L[1]	PCDIV L[0]	XXh

Description	REV	Source output level in display period.																				
	REV	Input Data	Source output level in display area																			
			Positive polarity	Positive polarity																		
	0	24'h000000 : 24'hFFFFFF	V255 : V0	V255 : V0																		
	1	24'h000000 : 24'hFFFFFF	V0 : V255	V0 : V255																		
	SM																					
	SM=0: Left/right interchanging scan SM=1: Left/right one-side scan																					
	GS																					
	GS=0: Forward scan GS=1: Reverse scan																					
	The R61529 allows changing gate driver assignment and the scan mode by combination of SM and GS bits. Set these bits in accordance with the configuration of the module. For details, see "Scan Mode Setting".																					
BGR																						
The bit is used to switch RGB/BGR. (See description of B6 bit in 36h command) Relationships between BGR setting and gamma correction registers are shown below.																						
<table border="1"> <thead> <tr> <th>36h(B3)</th><th>BGR</th><th>Host processor</th><th>Display Device</th></tr> </thead> <tbody> <tr> <td rowspan="2">0</td><td>0</td><td>RGB</td><td>RGB</td></tr> <tr><td>1</td><td>RGB</td><td>BGR</td></tr> <tr> <td rowspan="2">1</td><td>0</td><td>RGB</td><td>BGR</td></tr> <tr><td>1</td><td>RGB</td><td>RGB</td></tr> </tbody> </table>					36h(B3)	BGR	Host processor	Display Device	0	0	RGB	RGB	1	RGB	BGR	1	0	RGB	BGR	1	RGB	RGB
36h(B3)	BGR	Host processor	Display Device																			
0	0	RGB	RGB																			
	1	RGB	BGR																			
1	0	RGB	BGR																			
	1	RGB	RGB																			
SS																						
The bit is used to set the shift direction of output from the source driver. (See description of B6 bit in 36h command)																						
<table border="1"> <thead> <tr> <th>36h(B6)</th><th>SS</th><th>Source Output</th></tr> </thead> <tbody> <tr> <td rowspan="2">0</td><td>0</td><td>S1 → S960</td></tr> <tr><td>1</td><td>S960 → S1</td></tr> </tbody> </table> <table border="1"> <thead> <tr> <th>36h(B6)</th><th>SS</th><th>Source Output</th></tr> </thead> <tbody> <tr> <td rowspan="2">1</td><td>0</td><td>S960 → S1</td></tr> <tr><td>1</td><td>S1 → S960</td></tr> </tbody> </table>					36h(B6)	SS	Source Output	0	0	S1 → S960	1	S960 → S1	36h(B6)	SS	Source Output	1	0	S960 → S1	1	S1 → S960		
36h(B6)	SS	Source Output																				
0	0	S1 → S960																				
	1	S960 → S1																				
36h(B6)	SS	Source Output																				
1	0	S960 → S1																				
	1	S1 → S960																				
To change the RGB order, set SS and BGR bit in accordance with mounting position.																						

Description	NL[8:1]																																																																								
	These bits set the number of lines to drive the LCD to in units of 2 lines in the range from 240 lines to 480 lines. The frame memory address mapping is not affected by the number of NL[8:1]. The number of lines should be set according to the panel size.																																																																								
	<table border="1"> <thead> <tr> <th>NL[8:1]</th><th>Number of drive line</th></tr> </thead> <tbody> <tr><td>8'h00-8'h76</td><td>Setting inhibited</td></tr> <tr><td>8'h77</td><td>240 lines</td></tr> <tr><td>8'h78</td><td>242 lines</td></tr> <tr><td>8'h79</td><td>244 lines</td></tr> <tr><td>:</td><td>:</td></tr> <tr><td>:</td><td>:</td></tr> <tr><td>:</td><td>:</td></tr> <tr><td>:</td><td>:</td></tr> <tr><td>8'hEC</td><td>474 lines</td></tr> <tr><td>8'hED</td><td>476 lines</td></tr> <tr><td>8'hEE</td><td>478 lines</td></tr> <tr><td>8'hEF</td><td>480 lines</td></tr> <tr><td>8'hF0-8'hFF</td><td>Setting inhibited</td></tr> </tbody> </table>	NL[8:1]	Number of drive line	8'h00-8'h76	Setting inhibited	8'h77	240 lines	8'h78	242 lines	8'h79	244 lines	:	:	:	:	:	:	:	:	8'hEC	474 lines	8'hED	476 lines	8'hEE	478 lines	8'hEF	480 lines	8'hF0-8'hFF	Setting inhibited																																												
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		SM=0		SM=1																																																																					
	GS=0	GS=1	GS=0	GS=1																																																																					
6'h00	G[1]	G[(N)]	G[1]	G[N]																																																																					
6'h01	G[9]	G[(N+8)]	G[16]	G[N+4]																																																																					
6'h02	G[17]	G[(N+16)]	G[33]	G[N+8]																																																																					
6'h03	G[25]	G[(N+24)]	G[49]	G[N+12]																																																																					
6'h04	G[33]	G[(N+32)]	G[65]	G[N+16]																																																																					
6'h05	G[41]	G[(N+40)]	G[81]	G[N+20]																																																																					
6'h06	G[49]	G[(N+48)]	G[97]	G[N+24]																																																																					
6'h07	G[57]	G[(N+56)]	G[113]	G[N+28]																																																																					
6'h08	G[65]	G[(N+64)]	G[129]	G[N+32]																																																																					
6'h09	G[73]	G[(N+72)]	G[145]	G[N+36]																																																																					
6'h0A	G[81]	G[(N+80)]	G[161]	G[N+40]																																																																					
6'h0B-6'h2F	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited																																																																					

Description	To set SCN, follow the restriction below:																			
	SM	GS	Restriction																	
	0	0	(Scanning start position -1) + (Number of line (NL bit)) ≤ 480																	
	0	1	Scanning start position ≤ 480																	
	1	0	(Scanning start position -1) + (Number of line (NL bit)) ≤ 480																	
	1	1	Scanning start position ≤ 480																	
	BLV																			
The bit selects inversion operation during the retrace period.																				
<table border="1"> <thead> <tr> <th>BLV</th><th colspan="2">Inversion operation during retrace period</th></tr> </thead> <tbody> <tr> <td>0</td><td colspan="2">Dot inversion</td></tr> <tr> <td>1</td><td colspan="2" rowspan="4">Column inversion</td></tr> </tbody> </table>				BLV	Inversion operation during retrace period		0	Dot inversion		1	Column inversion									
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1	Column inversion																			
BLS																				
The bit is used to define source output level in the Retrace Period.																				
<table border="1"> <thead> <tr> <th>BLS</th><th>Positive polarity</th><th>Negative polarity</th></tr> </thead> <tbody> <tr> <td>0</td><td>V255</td><td>V255</td></tr> <tr> <td>1</td><td>V0</td><td>V20</td></tr> </tbody> </table>				BLS	Positive polarity	Negative polarity	0	V255	V255	1	V0	V20								
BLS	Positive polarity	Negative polarity																		
0	V255	V255																		
1	V0	V20																		
PTV																				
The bit is used to define inversion in a non-lit display area.																				
<table border="1"> <thead> <tr> <th>PTV</th><th colspan="2">Inverting operation in non-lit display area</th></tr> </thead> <tbody> <tr> <td>0</td><td colspan="2">Dot inversion</td></tr> <tr> <td>1</td><td colspan="2" rowspan="4">Column inversion</td></tr> </tbody> </table>				PTV	Inverting operation in non-lit display area		0	Dot inversion		1	Column inversion									
PTV	Inverting operation in non-lit display area																			
0	Dot inversion																			
1	Column inversion																			
NDL																				
The bit is used to define source output level (PTV=1) in the non-lit display area.																				
<table border="1"> <thead> <tr> <th rowspan="2">NDL</th><th colspan="2">Source output level in non-lit display area</th></tr> <tr> <th>Positive polarity</th><th>Negative polarity</th></tr> </thead> <tbody> <tr> <td>2'h0</td><td>V255</td><td>V255</td></tr> <tr> <td>2'h1</td><td>V0</td><td>V0</td></tr> <tr> <td>2'h2</td><td>GND</td><td>GND</td></tr> <tr> <td>2'h3</td><td colspan="2">Setting inhibited</td></tr> </tbody> </table>				NDL	Source output level in non-lit display area		Positive polarity	Negative polarity	2'h0	V255	V255	2'h1	V0	V0	2'h2	GND	GND	2'h3	Setting inhibited	
NDL	Source output level in non-lit display area																			
	Positive polarity	Negative polarity																		
2'h0	V255	V255																		
2'h1	V0	V0																		
2'h2	GND	GND																		
2'h3	Setting inhibited																			

Description	<p>"Retrace period" means back and front porches.</p> <p>"Non-lit display area" means:</p> <ul style="list-style-type: none"> Non-display area other than the Partial Area defined by SR[8:0] and ER[8:0]. Display area when Sleep mode is off and the display operation is off.  <p>PTG</p> <p>The bit is used to select gate scan mode in non-lit display area.</p> <table border="1" data-bbox="349 1145 825 1280"> <thead> <tr> <th>PTG</th><th>gate output in non-lit display area</th></tr> </thead> <tbody> <tr> <td>0</td><td>Normal scan</td></tr> <tr> <td>1</td><td>Interval scan</td></tr> </tbody> </table> <p>Note: Selects the frame-n inversion liquid crystal drive waveform (B/C = 0) when selecting interval scan.</p>	PTG	gate output in non-lit display area	0	Normal scan	1	Interval scan
PTG	gate output in non-lit display area						
0	Normal scan						
1	Interval scan						

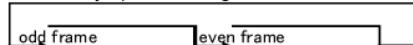
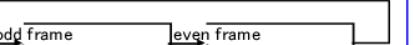
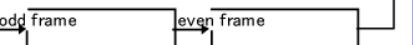
Description	<p>ISC[3:0]</p> <p>The bit is used to set the scan cycle when PTG selects interval scan in non-display area drive period. The scan cycle is defined by n frame periods, where n is an odd number from 3 to 31. The polarity of liquid crystal drive voltage from the gate driver is inverted in the same timing as the interval scan cycle.</p> <table border="1"> <thead> <tr> <th>ISC[3:0]</th><th>Scan interval</th><th>ISC[3:0]</th><th>Scan interval</th></tr> </thead> <tbody> <tr> <td>4'h0</td><td>Setting inhibited</td><td>4'h8</td><td>17 frames</td></tr> <tr> <td>4'h1</td><td>3 frames</td><td>4'h9</td><td>19 frames</td></tr> <tr> <td>4'h2</td><td>5 frames</td><td>4'hA</td><td>21 frames</td></tr> <tr> <td>4'h3</td><td>7 frames</td><td>4'hB</td><td>23 frames</td></tr> <tr> <td>4'h4</td><td>9 frames</td><td>4'hC</td><td>25 frames</td></tr> <tr> <td>4'h5</td><td>11 frames</td><td>4'hD</td><td>27 frames</td></tr> <tr> <td>4'h6</td><td>13 frames</td><td>4'hE</td><td>29 frames</td></tr> <tr> <td>4'h7</td><td>15 frames</td><td>4'hF</td><td>31 frames</td></tr> </tbody> </table> <p>PCDIVH[3:0]/PCDIVL[3:0]</p> <p>When the R61529's display operation is synchronized with PCLK during DPI operation, internal clock for display operation switches from internal oscillation clock to PCLKD. The bits are used to define the division ratio of PCLKD to PCLK.</p> <p>PCDIVH specifies the number of PCLK during PCLKD high period in units of 1 clock. PCDIVL specifies the number of PCLK during PCLKD low period in units of 1 clock.</p> <table border="1"> <thead> <tr> <th>PCDIVH[3:0] PCDIVL[3:0]</th><th>Number of clocks</th><th>PCDIVH[3:0] PCDIVL[3:0]</th><th>Number of clocks</th></tr> </thead> <tbody> <tr> <td>4'h0</td><td>Setting inhibited</td><td>4'h8</td><td>8 clocks</td></tr> <tr> <td>4'h1</td><td>1 clock</td><td>4'h9</td><td>9 clocks</td></tr> <tr> <td>4'h2</td><td>2 clocks</td><td>4'hA</td><td>10 clocks</td></tr> <tr> <td>4'h3</td><td>3 clocks</td><td>4'hB</td><td>11 clocks</td></tr> <tr> <td>4'h4</td><td>4 clocks</td><td>4'hC</td><td>12 clocks</td></tr> <tr> <td>4'h5</td><td>5 clocks</td><td>4'hD</td><td>13 clocks</td></tr> <tr> <td>4'h6</td><td>6 clocks</td><td>4'hE</td><td>14 clocks</td></tr> <tr> <td>4'h7</td><td>7 clocks</td><td>4'hF</td><td>15 clocks</td></tr> </tbody> </table> <p>Set PCDIVL=PCDIVH or PCDIVH-1. Also, set PCDIVH and PCDIVL so that PCLKD frequency becomes the closest to internal oscillation clock frequency. X = Don't care</p>	ISC[3:0]	Scan interval	ISC[3:0]	Scan interval	4'h0	Setting inhibited	4'h8	17 frames	4'h1	3 frames	4'h9	19 frames	4'h2	5 frames	4'hA	21 frames	4'h3	7 frames	4'hB	23 frames	4'h4	9 frames	4'hC	25 frames	4'h5	11 frames	4'hD	27 frames	4'h6	13 frames	4'hE	29 frames	4'h7	15 frames	4'hF	31 frames	PCDIVH[3:0] PCDIVL[3:0]	Number of clocks	PCDIVH[3:0] PCDIVL[3:0]	Number of clocks	4'h0	Setting inhibited	4'h8	8 clocks	4'h1	1 clock	4'h9	9 clocks	4'h2	2 clocks	4'hA	10 clocks	4'h3	3 clocks	4'hB	11 clocks	4'h4	4 clocks	4'hC	12 clocks	4'h5	5 clocks	4'hD	13 clocks	4'h6	6 clocks	4'hE	14 clocks	4'h7	7 clocks	4'hF	15 clocks
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Restriction	Note: When this command is read via DSI or MDDI, dummy read operation is not performed.																																																																								

Display Timing Setting for Normal Mode (C1h)

C1h	Display Timing Setting for Normal Mode																																																					
	W / R	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex																																										
Command	—	0	X	1	1	0	0	0	0	0	1	C1h																																										
1st parameter	W / R	1	X	0	0	0	0	DIV[3]	DIV[2]	DIV[1]	DIV[0]	0Xh																																										
2nd parameter	W / R	1	X	0	0	RTN [5]	RTN [4]	RTN [3]	RTN [2]	RTN [1]	RTN [0]	XXh																																										
3rd parameter	W / R	1	X	BP [7]	BP [6]	BP [5]	BP [4]	BP [3]	BP [2]	BP [1]	BP [0]	XXh																																										
4th parameter	W / R	1	X	FP [7]	FP [6]	FP [5]	FP [4]	FP [3]	FP [2]	FP [1]	FP [0]	XXh																																										
5th parameter	W / R	1	X	0	LINEIN V0[2]	LINEIN V0[1]	LINEIN V0[0]	0	0	0	PNSET	XXh																																										
Description	DIV[3:0] These bits set the division ratio of the internal clock frequency. A clock whose frequency is divided is a reference clock (unit: clk) for a display circuit and step-up circuit. One clock width equals 1 clk. Set DIV[3:0] before use according to use conditions. fOSC=14MHz(Typ.). If a division ratio is set to 1/12 (4'h7), $1/(14\text{MHz}/12) = 0.85\mu\text{s} = 1\text{clk}$.																																																					
	<table border="1"> <thead> <tr> <th>DIV[3:0]</th> <th>Setting</th> </tr> </thead> <tbody> <tr> <td>4'h0-3</td> <td>Setting inhibited</td> </tr> <tr> <td>4'h4</td> <td>fOSC/9</td> </tr> <tr> <td>4'h5</td> <td>fOSC/10</td> </tr> <tr> <td>4'h6</td> <td>Setting inhibited</td> </tr> <tr> <td>4'h7</td> <td>fOSC/12</td> </tr> <tr> <td>Other than the above</td> <td>Setting inhibited</td> </tr> </tbody> </table> RTN[5:0] These bits set the number of clocks in 1 line period.												DIV[3:0]	Setting	4'h0-3	Setting inhibited	4'h4	fOSC/9	4'h5	fOSC/10	4'h6	Setting inhibited	4'h7	fOSC/12	Other than the above	Setting inhibited																												
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Description	FP[7:0], BP[7:0]	Number of front porch lines	Number of back porch lines
<p>These parameters define the retrace period (i.e. front and back porches) which appears before and after the display area. FP bits define number of front porch lines while BP bits define number of back porch lines.</p>			
FP[7:0], BP[7:0]	Number of front porch lines	Number of back porch lines	
8'h00	Setting inhibited	Setting inhibited	
8'h01	Setting inhibited	Setting inhibited	
8'h02	Setting inhibited	Setting inhibited	
8'h03	Setting inhibited	Setting inhibited	
8'h04	4 lines	4 lines	
8'h05	5 lines	5 lines	
8'h06	6 lines	6 lines	
8'h07	7 lines	7 lines	
8'h08	8 lines	8 lines	
8'h09	9 lines	9 lines	
8'h0A	10 lines	10 lines	
8'h0B	11 lines	11 lines	
8'h0C	12 lines	12 lines	
8'h0D	13 lines	13 lines	
8'h0E	14 lines	14 lines	
8'h0F	15 lines	15 lines	
:	:	:	
8'h7F	127 lines	127 lines	
8'h80	128 lines	128 lines	
8'h81	Setting inhibited	Setting inhibited	
:	:	:	
8'hFF	Setting inhibited	Setting inhibited	

Description	<p>PNSET</p> <p>Sets a dot inversion method.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #cccccc;"> <th style="text-align: center;">PNSET</th><th style="text-align: center;">Setting</th></tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td><td>Spatial configuration mode 1</td></tr> <tr> <td style="text-align: center;">1</td><td>Spatial configuration mode 2</td></tr> </tbody> </table> <p>LINEINV0[2:0]</p> <p>Sets a line inversion cycle of a dot inversion method.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #cccccc;"> <th style="text-align: center;">LINEINV0[2:0]</th><th colspan="2" style="text-align: center;">Setting</th></tr> </thead> <tbody> <tr> <td style="text-align: center;">3'h0</td><td>1-line inversion</td><td>Only spatial configuration mode 1</td></tr> <tr> <td style="text-align: center;">3'h1</td><td>2-line inversion</td><td></td></tr> <tr> <td style="text-align: center;">3'h2</td><td>3-line inversion</td><td>Only spatial configuration mode 1</td></tr> <tr> <td style="text-align: center;">3'h3</td><td>4-line inversion</td><td></td></tr> <tr> <td style="text-align: center;">3'h4</td><td>8-line inversion</td><td></td></tr> <tr> <td style="text-align: center;">3'h5</td><td>Column inversion</td><td>Only spatial configuration mode 1</td></tr> <tr> <td style="text-align: center;">2'h6</td><td>Setting inhibited</td><td></td></tr> <tr> <td style="text-align: center;">3'h7</td><td>Setting inhibited</td><td></td></tr> </tbody> </table> <p>Source output operation performed by combined setting of PNSET0 and LINEINV0 are as follows:</p>	PNSET	Setting	0	Spatial configuration mode 1	1	Spatial configuration mode 2	LINEINV0[2:0]	Setting		3'h0	1-line inversion	Only spatial configuration mode 1	3'h1	2-line inversion		3'h2	3-line inversion	Only spatial configuration mode 1	3'h3	4-line inversion		3'h4	8-line inversion		3'h5	Column inversion	Only spatial configuration mode 1	2'h6	Setting inhibited		3'h7	Setting inhibited	
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3'h7	Setting inhibited																																	

<p>Description</p> <ul style="list-style-type: none"> ● 1-line inversion Only spatial configuration mode 1 <div style="border: 1px solid black; padding: 10px; margin-top: 10px;">  <p>odd frame → even frame</p> <p>Line ↓</p> <table border="1" style="border-collapse: collapse; text-align: center;"> <tr><td>+</td><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td></tr> <tr><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td><td>+</td></tr> <tr><td>+</td><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td></tr> <tr><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td><td>+</td></tr> </table> </div> <ul style="list-style-type: none"> ● 2-line inversion <div style="display: flex; justify-content: space-around; margin-top: 10px;"> <div style="width: 45%;"> <p>Spatial configuration mode 1</p>  <p>odd frame → even frame</p> <table border="1" style="border-collapse: collapse; text-align: center;"> <tr><td>+</td><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td></tr> <tr><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td><td>+</td></tr> <tr><td>+</td><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td></tr> <tr><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td><td>+</td></tr> <tr><td>+</td><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td></tr> <tr><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td><td>+</td></tr> <tr><td>+</td><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td></tr> <tr><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td><td>+</td><td>-</td><td>+</td></tr> </table> </div> <div style="width: 45%;"> <p>Spatial configuration mode 2</p>  <p>odd frame → even frame</p> <table border="1" style="border-collapse: collapse; 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<p>Description</p>	<p>● 8-line inversion</p> <p>Spatial configuration mode 1</p> <p>Spatial configuration mode 2</p>
<p>Restriction</p>	<p>Make sure that the total of lines set by the BP and FP bits is an even number.</p>

X = Don't care

Test Mode 1 (C3h)

C3h	Test Mode 1											
	W / R	DCX	DB23- DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	—	0	X	1	1	0	0	0	0	1	1	C3h
Dummy Parameter	R	1	X	X	X	X	X	X	X	X	X	XXh
1st parameter	R	1	X	0	0	1	0	0	0	0	1	21h
Description	Test mode command. Do not access this command and its parameters. X = Don't care											

Source/Gate Driving Timing Setting (C4h)

C4h	Panel Driving Setting																													
	W / R	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex																		
Command	—	0	X	1	1	0	0	0	1	0	0	C4h																		
1st parameter	W / R	1	X	0	NOW B[2]	NOW B[1]	NOW B[0]	0	NOW [2]	NOW [1]	NOW [0]	XXh																		
2nd parameter	W / R	1	X	0	0	0	0	0	0	0	0	00h																		
3rd parameter	W / R	1	X	0	0	0	0	SEQG ND[3]	SEQG ND[2]	SEQG ND[1]	SEQG ND[0]	0Xh																		
4th parameter	W / R	1	X	0	0	0	0	SEQV CIL3]	SEQV CIL[2]	SEQV CIL[1]	SEQV CIL[0]	0Xh																		
Description	NOWB[2:0] These bits are used to set a falling position of gate output. <table border="1" style="margin-left: 20px; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #cccccc;">NOWB[2:0]</th> <th style="background-color: #cccccc;">Falling position of gate output</th> </tr> </thead> <tbody> <tr><td>3'h0</td><td>Setting inhibited</td></tr> <tr><td>3'h1</td><td>Setting inhibited</td></tr> <tr><td>3'h2</td><td>1 clock</td></tr> <tr><td>3'h3</td><td>2 clocks</td></tr> <tr><td>3'h4</td><td>3 clocks</td></tr> <tr><td>3'h5</td><td>4 clocks</td></tr> <tr><td>3'h6</td><td>5 clocks</td></tr> <tr><td>3'h7</td><td>6 clocks</td></tr> </tbody> </table> <p>Note: The unit clock here is the frequency divided clock, which is set according to the division ratio set by DIV (C1h).</p>												NOWB[2:0]	Falling position of gate output	3'h0	Setting inhibited	3'h1	Setting inhibited	3'h2	1 clock	3'h3	2 clocks	3'h4	3 clocks	3'h5	4 clocks	3'h6	5 clocks	3'h7	6 clocks
NOWB[2:0]	Falling position of gate output																													
3'h0	Setting inhibited																													
3'h1	Setting inhibited																													
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3'h3	2 clocks																													
3'h4	3 clocks																													
3'h5	4 clocks																													
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Description	<p>NOW[2:0]</p> <p>These bits are used to set a gate output start position (non-overlap period) in 1-line period.</p> <table border="1"> <thead> <tr> <th>NOW[2:0]</th><th>Falling position of gate output</th></tr> </thead> <tbody> <tr> <td>3'h0</td><td>1 clock</td></tr> <tr> <td>3'h1</td><td>2 clocks</td></tr> <tr> <td>3'h2</td><td>3 clocks</td></tr> <tr> <td>3'h3</td><td>4 clocks</td></tr> <tr> <td>3'h4</td><td>5 clocks</td></tr> <tr> <td>3'h5</td><td>6 clocks</td></tr> <tr> <td>3'h6</td><td>7 clocks</td></tr> <tr> <td>3'h7</td><td>8 clocks</td></tr> </tbody> </table> <p>Note: The unit clock here is the frequency divided clock, which is set according to the division ratio set by DIV (C1h).</p>	NOW[2:0]	Falling position of gate output	3'h0	1 clock	3'h1	2 clocks	3'h2	3 clocks	3'h3	4 clocks	3'h4	5 clocks	3'h5	6 clocks	3'h6	7 clocks	3'h7	8 clocks
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3'h2	3 clocks																		
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3'h4	5 clocks																		
3'h5	6 clocks																		
3'h6	7 clocks																		
3'h7	8 clocks																		

Description	SEQGND[3:0] Sets a source pre-charge period. (GND pre-charge) "clk" equals a reference clock (clk) set by DIV[3:0] (C1h command) or set by PCDIVH[3:0] and PCDIVL[3:0] (C0h command). <table border="1"> <thead> <tr> <th>SEQGND[3:0]</th><th>Period</th></tr> </thead> <tbody> <tr><td>4'h0</td><td>Setting inhibited</td></tr> <tr><td>4'h1</td><td>Setting inhibited</td></tr> <tr><td>4'h2</td><td>Setting inhibited</td></tr> <tr><td>4'h3</td><td>3clks</td></tr> <tr><td>4'h4</td><td>4clks</td></tr> <tr><td>4'h5</td><td>5clks</td></tr> <tr><td>4'h6</td><td>6clks</td></tr> <tr><td>:</td><td>:</td></tr> <tr><td>4'h9</td><td>9clks</td></tr> <tr><td>4'hA</td><td>10clks</td></tr> <tr><td>4'hB</td><td>11clks</td></tr> <tr><td>4'hC</td><td>12clks</td></tr> <tr><td>4'hD</td><td>13clks</td></tr> <tr><td>4'hE</td><td>14clks</td></tr> <tr><td>4'hF</td><td>15clks</td></tr> </tbody> </table>	SEQGND[3:0]	Period	4'h0	Setting inhibited	4'h1	Setting inhibited	4'h2	Setting inhibited	4'h3	3clks	4'h4	4clks	4'h5	5clks	4'h6	6clks	:	:	4'h9	9clks	4'hA	10clks	4'hB	11clks	4'hC	12clks	4'hD	13clks	4'hE	14clks	4'hF	15clks	SEQVCIL[3:0] Sets a source pre-charge period. (VCI and VCL pre-charge) "clk" equals a reference clock (clk) set by DIV[3:0] (C1h command) or set by PCDIVH[3:0] and PCDIVL[3:0] (C0h command). <table border="1"> <thead> <tr> <th>SEQVCIL[3:0]</th><th>Period</th></tr> </thead> <tbody> <tr><td>4'h0</td><td>Setting inhibited</td></tr> <tr><td>4'h1</td><td>1clk</td></tr> <tr><td>4'h2</td><td>2clks</td></tr> <tr><td>4'h3</td><td>3clks</td></tr> <tr><td>4'h4</td><td>4clks</td></tr> <tr><td>4'h5</td><td>5clks</td></tr> <tr><td>4'h6</td><td>6clks</td></tr> <tr><td>:</td><td>:</td></tr> <tr><td>4'h9</td><td>9clks</td></tr> <tr><td>4'hA</td><td>10clks</td></tr> <tr><td>4'hB</td><td>11clks</td></tr> <tr><td>4'hC</td><td>12clks</td></tr> <tr><td>4'hD</td><td>13clks</td></tr> <tr><td>4'hE</td><td>14clks</td></tr> <tr><td>4'hF</td><td>15clks</td></tr> </tbody> </table>	SEQVCIL[3:0]	Period	4'h0	Setting inhibited	4'h1	1clk	4'h2	2clks	4'h3	3clks	4'h4	4clks	4'h5	5clks	4'h6	6clks	:	:	4'h9	9clks	4'hA	10clks	4'hB	11clks	4'hC	12clks	4'hD	13clks	4'hE	14clks	4'hF	15clks
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Basic operation of source output 1 (polarity inversion)	<p>An example of a source output waveform (pre-charge) is shown below.</p> <p>(n = 0,1,2,3.....255)</p> <p>X = Don't care</p>																																																																	
Restriction	Note: When this command is read via DSI or MDDI, dummy read operation is not performed.																																																																	

DPI Polarity Control

DPI Polarity Control (C6h)												
C6h	W / R	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	—	0	X	1	1	0	0	0	1	1	0	C6h
1st parameter	W / R	1	X	0	0	0	VSPL	HSPL	EPL	0	DPL	00h
Description	<p>VSPL Sets the signal polarity of the VSYNC pin. VSPL=0 Low active VSPL=1 High active</p> <p>HSPL Sets the signal polarity of the HSYNC pin HSPL=0 Low active HSPL=1 High active</p> <p>EPL Sets the signal polarity of the DE pin EPL=0 DE=0: Writing DB[23:0] data is enabled. DE=1: Writing DB[23:0] is disabled. EPL=1 DE=0: Writing DB[23:0] data is disabled. DE=1: Writing DB[23:0] is enabled.</p> <p>DPL Sets the signal polarity of the PCLK pin. DPL=0 Reads data on the rising edge of the PCLK signal. DPL=1 Reads data on the falling edge of the PCLK signal.</p> <p>X = Don't care</p>											
Restriction	Note: When this command is read via DSI or MDDI, dummy read operation is not performed.											

Test Mode 2 (C7h)

C7h	Test Mode 2											
	W / R	DCX	DB23- DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	—	0	X	1	1	0	0	0	1	1	1	C7h
Dummy Parameter	R	1	X	X	X	X	X	X	X	X	X	XXh
1st parameter	R	1	X	0	0	0	0	0	0	0	0	00h
2nd parameter	R	1	X	0	0	0	0	0	0	0	0	00h
Description	Test mode command. Do not access this command and its parameters. X = Don't care											

Gamma Control Command**Gamma Setting A Set (C8h)**

C8h	Gamma Setting A Set											
	W / R	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	—	0	X	1	1	0	0	1	0	0	0	C8h
1st parameter	W / R	1	X	0	GSELA P0[6]	GSELA P0[5]	GSELA P0[4]	GSELA P0[3]	GSELA P0[2]	GSELA P0[1]	GSELA P0[0]	XXh
2nd parameter	W / R	1	X	0	GSELA P1[6]	GSELA P1[5]	GSELA P1[4]	GSELA P1[3]	GSELA P1[2]	GSELA P1[1]	GSELA P1[0]	XXh
3rd parameter	W / R	1	X	0	GSELA P2[6]	GSELA P2[5]	GSELA P2[4]	GSELA P2[3]	GSELA P2[2]	GSELA P2[1]	GSELA P2[0]	XXh
4th parameter	W / R	1	X	0	GSELA P3[6]	GSELA P3[5]	GSELA P3[4]	GSELA P3[3]	GSELA P3[2]	GSELA P3[1]	GSELA P3[0]	XXh
5th parameter	W / R	1	X	0	GSELA P4[6]	GSELA P4[5]	GSELA P4[4]	GSELA P4[3]	GSELA P4[2]	GSELA P4[1]	GSELA P4[0]	XXh
6th parameter	W / R	1	X	0	GSELA P5[6]	GSELA P5[5]	GSELA P5[4]	GSELA P5[3]	GSELA P5[2]	GSELA P5[1]	GSELA P5[0]	XXh
7th parameter	W / R	1	X	0	GSELA P6[6]	GSELA P6[5]	GSELA P6[4]	GSELA P6[3]	GSELA P6[2]	GSELA P6[1]	GSELA P6[0]	XXh
8th parameter	W / R	1	X	0	GSELA P7[6]	GSELA P7[5]	GSELA P7[4]	GSELA P7[3]	GSELA P7[2]	GSELA P7[1]	GSELA P7[0]	XXh
9th parameter	W / R	1	X	0	GSELA P8[6]	GSELA P8[5]	GSELA P8[4]	GSELA P8[3]	GSELA P8[2]	GSELA P8[1]	GSELA P8[0]	XXh
10th parameter	W / R	1	X	0	GSELA P9[6]	GSELA P9[5]	GSELA P9[4]	GSELA P9[3]	GSELA P9[2]	GSELA P9[1]	GSELA P9[0]	XXh
11th parameter	W / R	1	X	0	GSELA P10[6]	GSELA P10[5]	GSELA P10[4]	GSELA P10[3]	GSELA P10[2]	GSELA P10[1]	GSELA P10[0]	XXh
12th parameter	W / R	1	X	0	GSELA P11[6]	GSELA P11[5]	GSELA P11[4]	GSELA P11[3]	GSELA P11[2]	GSELA P11[1]	GSELA P11[0]	XXh
13th parameter	W / R	1	X	0	GSELA N0[6]	GSELA N0[5]	GSELA N0[4]	GSELA N0[3]	GSELA N0[2]	GSELA N0[1]	GSELA N0[0]	XXh
14th parameter	W / R	1	X	0	GSELA N1[6]	GSELA N1[5]	GSELA N1[4]	GSELA N1[3]	GSELA N1[2]	GSELA N1[1]	GSELA N1[0]	XXh
15th parameter	W / R	1	X	0	GSELA N2[6]	GSELA N2[5]	GSELA N2[4]	GSELA N2[3]	GSELA N2[2]	GSELA N2[1]	GSELA N2[0]	XXh
16th parameter	W / R	1	X	0	GSELA N3[6]	GSELA N3[5]	GSELA N3[4]	GSELA N3[3]	GSELA N3[2]	GSELA N3[1]	GSELA N3[0]	XXh

17th parameter	W / R	1	X	0	GSELA N4[6]	GSELA N4[5]	GSELA N4[4]	GSELA N4[3]	GSELA N4[2]	GSELA N4[1]	GSELA N4[0]	XXh
18th parameter	W / R	1	X	0	GSELA N5[6]	GSELA N5[5]	GSELA N5[4]	GSELA N5[3]	GSELA N5[2]	GSELA N5[1]	GSELA N5[0]	XXh
19th parameter	W / R	1	X	0	GSELA N6[6]	GSELA N6[5]	GSELA N6[4]	GSELA N6[3]	GSELA N6[2]	GSELA N6[1]	GSELA N6[0]	XXh
20th parameter	W / R	1	X	0	GSELA N7[6]	GSELA N7[5]	GSELA N7[4]	GSELA N7[3]	GSELA N7[2]	GSELA N7[1]	GSELA N7[0]	XXh
21st parameter	W / R	1	X	0	GSELA N8[6]	GSELA N8[5]	GSELA N8[4]	GSELA N8[3]	GSELA N8[2]	GSELA N8[1]	GSELA N8[0]	XXh
22nd parameter	W / R	1	X	0	GSELA N9[6]	GSELA N9[5]	GSELA N9[4]	GSELA N9[3]	GSELA N9[2]	GSELA N9[1]	GSELA N9[0]	XXh
23rd parameter	W / R	1	X	0	GSELA N10[6]	GSELA N10[5]	GSELA N10[4]	GSELA N10[3]	GSELA N10[2]	GSELA N10[1]	GSELA N10[0]	XXh
24th parameter	W / R	1	X	0	GSELA N11[6]	GSELA N11[5]	GSELA N11[4]	GSELA N11[3]	GSELA N11[2]	GSELA N11[1]	GSELA N11[0]	XXh
Description	Grayscale (red or blue) that Gamma Setting A Set registers are applied depends on settings of C0h command (BGR bit) and 36h command (B3 bit). See description of C0h command for details. See "Gamma Correction Function" for detailed description of the parameters. X = Don't care											
Restriction	Note: When this command is read via DSI or MDDI, dummy read operation is not performed.											

Gamma Setting B Set (C9h)

C9h	Gamma Setting B Set											
	W / R	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	—	0	X	1	1	0	0	1	0	0	1	C9h
1st parameter	W / R	1	X	0	GSELB P0[6]	GSELB P0[5]	GSELB P0[4]	GSELB P0[3]	GSELB P0[2]	GSELB P0[1]	GSELB P0[0]	XXh
2nd parameter	W / R	1	X	0	GSELB P1[6]	GSELB P1[5]	GSELB P1[4]	GSELB P1[3]	GSELB P1[2]	GSELB P1[1]	GSELB P1[0]	XXh
3rd parameter	W / R	1	X	0	GSELB P2[6]	GSELB P2[5]	GSELB P2[4]	GSELB P2[3]	GSELB P2[2]	GSELB P2[1]	GSELB P2[0]	XXh
4th parameter	W / R	1	X	0	GSELB P3[6]	GSELB P3[5]	GSELB P3[4]	GSELB P3[3]	GSELB P3[2]	GSELB P3[1]	GSELB P3[0]	XXh
5th parameter	W / R	1	X	0	GSELB P4[6]	GSELB P4[5]	GSELB P4[4]	GSELB P4[3]	GSELB P4[2]	GSELB P4[1]	GSELB P4[0]	XXh
6th parameter	W / R	1	X	0	GSELB P5[6]	GSELB P5[5]	GSELB P5[4]	GSELB P5[3]	GSELB P5[2]	GSELB P5[1]	GSELB P5[0]	XXh
7th parameter	W / R	1	X	0	GSELB P6[6]	GSELB P6[5]	GSELB P6[4]	GSELB P6[3]	GSELB P6[2]	GSELB P6[1]	GSELB P6[0]	XXh
8th parameter	W / R	1	X	0	GSELB P7[6]	GSELB P7[5]	GSELB P7[4]	GSELB P7[3]	GSELB P7[2]	GSELB P7[1]	GSELB P7[0]	XXh
9th parameter	W / R	1	X	0	GSELB P8[6]	GSELB P8[5]	GSELB P8[4]	GSELB P8[3]	GSELB P8[2]	GSELB P8[1]	GSELB P8[0]	XXh
10th parameter	W / R	1	X	0	GSELB P9[6]	GSELB P9[5]	GSELB P9[4]	GSELB P9[3]	GSELB P9[2]	GSELB P9[1]	GSELB P9[0]	XXh
11th parameter	W / R	1	X	0	GSELB P10[6]	GSELB P10[5]	GSELB P10[4]	GSELB P10[3]	GSELB P10[2]	GSELB P10[1]	GSELB P10[0]	XXh
12th parameter	W / R	1	X	0	GSELB P11[6]	GSELB P11[5]	GSELB P11[4]	GSELB P11[3]	GSELB P11[2]	GSELB P11[1]	GSELB P11[0]	XXh
13th parameter	W / R	1	X	0	GSELB N0[6]	GSELB N0[5]	GSELB N0[4]	GSELB N0[3]	GSELB N0[2]	GSELB N0[1]	GSELB N0[0]	XXh
14th parameter	W / R	1	X	0	GSELB N1[6]	GSELB N1[5]	GSELB N1[4]	GSELB N1[3]	GSELB N1[2]	GSELB N1[1]	GSELB N1[0]	XXh
15th parameter	W / R	1	X	0	GSELB N2[6]	GSELB N2[5]	GSELB N2[4]	GSELB N2[3]	GSELB N2[2]	GSELB N2[1]	GSELB N2[0]	XXh
16th parameter	W / R	1	X	0	GSELB N3[6]	GSELB N3[5]	GSELB N3[4]	GSELB N3[3]	GSELB N3[2]	GSELB N3[1]	GSELB N3[0]	XXh

17th parameter	W / R	1	X	0	GSELB N4[6]	GSELB N4[5]	GSELB N4[4]	GSELB N4[3]	GSELB N4[2]	GSELB N4[1]	GSELB N4[0]	XXh
18th parameter	W / R	1	X	0	GSELB N5[6]	GSELB N5[5]	GSELB N5[4]	GSELB N5[3]	GSELB N5[2]	GSELB N5[1]	GSELB N5[0]	XXh
19th parameter	W / R	1	X	0	GSELB N6[6]	GSELB N6[5]	GSELB N6[4]	GSELB N6[3]	GSELB N6[2]	GSELB N6[1]	GSELB N6[0]	XXh
20th parameter	W / R	1	X	0	GSELB N7[6]	GSELB N7[5]	GSELB N7[4]	GSELB N7[3]	GSELB N7[2]	GSELB N7[1]	GSELB N7[0]	XXh
21st parameter	W / R	1	X	0	GSELB N8[6]	GSELB N8[5]	GSELB N8[4]	GSELB N8[3]	GSELB N8[2]	GSELB N8[1]	GSELB N8[0]	XXh
22nd parameter	W / R	1	X	0	GSELB N9[6]	GSELB N9[5]	GSELB N9[4]	GSELB N9[3]	GSELB N9[2]	GSELB N9[1]	GSELB N9[0]	XXh
23rd parameter	W / R	1	X	0	GSELB N10[6]	GSELB N10[5]	GSELB N10[4]	GSELB N10[3]	GSELB N10[2]	GSELB N10[1]	GSELB N10[0]	XXh
24th parameter	W / R	1	X	0	GSELB N11[6]	GSELB N11[5]	GSELB N11[4]	GSELB N11[3]	GSELB N11[2]	GSELB N11[1]	GSELB N11[0]	XXh
Description	Gamma Setting B Set registers are applied to green grayscale. See "Gamma Correction Function" for detailed description of the parameters. X = Don't care											
Restriction	Note: When this command is read via DSI or MDDI, dummy read operation is not performed.											

Gamma Setting C Set (CAh)

CAh	Gamma Setting C Set											
	W / R	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	—	0	X	1	1	0	0	1	0	1	0	CAh
1st parameter	W / R	1	X	0	GSELC P0[6]	GSELC P0[5]	GSELC P0[4]	GSELC P0[3]	GSELC P0[2]	GSELC P0[1]	GSELC P0[0]	XXh
2nd parameter	W / R	1	X	0	GSELC P1[6]	GSELC P1[5]	GSELC P1[4]	GSELC P1[3]	GSELC P1[2]	GSELC P1[1]	GSELC P1[0]	XXh
3rd parameter	W / R	1	X	0	GSELC P2[6]	GSELC P2[5]	GSELC P2[4]	GSELC P2[3]	GSELC P2[2]	GSELC P2[1]	GSELC P2[0]	XXh
4th parameter	W / R	1	X	0	GSELC P3[6]	GSELC P3[5]	GSELC P3[4]	GSELC P3[3]	GSELC P3[2]	GSELC P3[1]	GSELC P3[0]	XXh
5th parameter	W / R	1	X	0	GSELC P4[6]	GSELC P4[5]	GSELC P4[4]	GSELC P4[3]	GSELC P4[2]	GSELC P4[1]	GSELC P4[0]	XXh
6th parameter	W / R	1	X	0	GSELC P5[6]	GSELC P5[5]	GSELC P5[4]	GSELC P5[3]	GSELC P5[2]	GSELC P5[1]	GSELC P5[0]	XXh
7th parameter	W / R	1	X	0	GSELC P6[6]	GSELC P6[5]	GSELC P6[4]	GSELC P6[3]	GSELC P6[2]	GSELC P6[1]	GSELC P6[0]	XXh
8th parameter	W / R	1	X	0	GSELC P7[6]	GSELC P7[5]	GSELC P7[4]	GSELC P7[3]	GSELC P7[2]	GSELC P7[1]	GSELC P7[0]	XXh
9th parameter	W / R	1	X	0	GSELC P8[6]	GSELC P8[5]	GSELC P8[4]	GSELC P8[3]	GSELC P8[2]	GSELC P8[1]	GSELC P8[0]	XXh
10th parameter	W / R	1	X	0	GSELC P9[6]	GSELC P9[5]	GSELC P9[4]	GSELC P9[3]	GSELC P9[2]	GSELC P9[1]	GSELC P9[0]	XXh
11th parameter	W / R	1	X	0	GSELC P10[6]	GSELC P10[5]	GSELC P10[4]	GSELC P10[3]	GSELC P10[2]	GSELC P10[1]	GSELC P10[0]	XXh
12th parameter	W / R	1	X	0	GSELC P11[6]	GSELC P11[5]	GSELC P11[4]	GSELC P11[3]	GSELC P11[2]	GSELC P11[1]	GSELC P11[0]	XXh
13th parameter	W / R	1	X	0	GSELC N0[6]	GSELC N0[5]	GSELC N0[4]	GSELC N0[3]	GSELC N0[2]	GSELC N0[1]	GSELC N0[0]	XXh
14th parameter	W / R	1	X	0	GSELC N1[6]	GSELC N1[5]	GSELC N1[4]	GSELC N1[3]	GSELC N1[2]	GSELC N1[1]	GSELC N1[0]	XXh
15th parameter	W / R	1	X	0	GSELC N2[6]	GSELC N2[5]	GSELC N2[4]	GSELC N2[3]	GSELC N2[2]	GSELC N2[1]	GSELC N2[0]	XXh
16th parameter	W / R	1	X	0	GSELC N3[6]	GSELC N3[5]	GSELC N3[4]	GSELC N3[3]	GSELC N3[2]	GSELC N3[1]	GSELC N3[0]	XXh

17th parameter	W / R	1	X	0	GSELC N4[6]	GSELC N4[5]	GSELC N4[4]	GSELC N4[3]	GSELC N4[2]	GSELC N4[1]	GSELC N4[0]	XXh
18th parameter	W / R	1	X	0	GSELC N5[6]	GSELC N5[5]	GSELC N5[4]	GSELC N5[3]	GSELC N5[2]	GSELC N5[1]	GSELC N5[0]	XXh
19th parameter	W / R	1	X	0	GSELC N6[6]	GSELC N6[5]	GSELC N6[4]	GSELC N6[3]	GSELC N6[2]	GSELC N6[1]	GSELC N6[0]	XXh
20th parameter	W / R	1	X	0	GSELC N7[6]	GSELC N7[5]	GSELC N7[4]	GSELC N7[3]	GSELC N7[2]	GSELC N7[1]	GSELC N7[0]	XXh
21st parameter	W / R	1	X	0	GSELC N8[6]	GSELC N8[5]	GSELC N8[4]	GSELC N8[3]	GSELC N8[2]	GSELC N8[1]	GSELC N8[0]	XXh
22nd parameter	W / R	1	X	0	GSELC N9[6]	GSELC N9[5]	GSELC N9[4]	GSELC N9[3]	GSELC N9[2]	GSELC N9[1]	GSELC N9[0]	XXh
23rd parameter	W / R	1	X	0	GSELC N10[6]	GSELC N10[5]	GSELC N10[4]	GSELC N10[3]	GSELC N10[2]	GSELC N10[1]	GSELC N10[0]	XXh
24th parameter	W / R	1	X	0	GSELC N11[6]	GSELC N11[5]	GSELC N11[4]	GSELC N11[3]	GSELC N11[2]	GSELC N11[1]	GSELC N11[0]	XXh
Description	Grayscale (red or blue) that Gamma Setting C Set registers are applied depends on settings of C0h command (BGR bit) and 36h command (B3 bit). See description of C0h command for details. See "Gamma Correction Function" for detailed description of the parameters. X = Don't care											
Restriction	Note: When this command is read via DSI or MDDI, dummy read operation is not performed.											

Test Mode 3 (CCh)

CCh	Test Mode 3											
	W / R	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	—	0	X	1	1	0	0	1	1	0	0	CCh
Dummy Parameter	R	1	X	X	X	X	X	X	X	X	X	XXh
1st parameter	R	1	X	0	0	0	0	0	0	0	0	00h
Description	Test mode command. Do not access this command and its parameters. X = Don't care											

Power Control Command**Power Setting (Charge Pump Setting) (D0h)**

Power Setting (Charge Pump Setting)												
D0h	W / R	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	—	0	X	1	1	0	1	0	0	0	0	D0h
1st parameter	W / R	1	X	1	0	DC4 [1]	DC4 [0]	DC1 [1]	DC1 [0]	DC2 [1]	DC2 [0]	XXh
2nd parameter	W / R	1	X	0	0	0	0	BT [1]	BT [0]	1	0	0Xh
3rd parameter	W / R	1	X	0	0	0	0	1	0	0	0	08h
4th parameter	W / R	1	X	0	0	DC1M [1]	DC1M [0]	0	0	0	0	X0h
5th parameter	W / R	1	X	0	0	VC1 [2]	VC1 [1]	VC1 [0]	VC2 [2]	VC2 [1]	VC2 [0]	0Bh
6th parameter	W / R	1	X	0	0	0	0	0	1	0	0	04h
7th parameter	W / R	1	X	0	0	0	0	0	0	0	1	01h
8th parameter	W / R	1	X	0	0	0	0	0	0	0	0	00h
9th parameter	W / R	1	X	0	0	0	0	1	0	0	0	08h
10th parameter	W / R	1	X	0	0	0	0	0	0	0	1	01h
11th parameter	W / R	1	X	0	0	0	0	0	0	0	0	00h
12th parameter	W / R	1	X	0	0	0	0	0	1	1	0	06h
13th parameter	W / R	1	X	0	0	0	0	0	0	0	1	01h
14th parameter	W / R	1	X	0	0	0	0	0	0	0	0	00h
15th parameter	W / R	1	X	0	0	0	0	0	0	0	0	00h
16th parameter	W / R	1	X	0	0	1	0	0	0	0	0	20h

Description	<p>DC1[1:0]</p> <p>Sets a step-up clock cycle of the internal step-up circuit generating VSP. 1H equals 1 horizontal (line) period.</p> <table border="1"> <thead> <tr> <th>DC1[1:0]</th><th>Step-up clock cycle</th></tr> </thead> <tbody> <tr> <td>2'h0</td><td>Halt</td></tr> <tr> <td>2'h1</td><td>1H</td></tr> <tr> <td>2'h2</td><td>1/2H</td></tr> <tr> <td>2'h3</td><td>Setting inhibited</td></tr> </tbody> </table> <p>DC2[1:0]</p> <p>Sets a step-up clock cycle of the internal step-up circuit generating VGH and VGL. 1H equals 1 horizontal (line) period. 2H equals 2 horizontal (2-line) periods.</p> <table border="1"> <thead> <tr> <th>DC2[1:0]</th><th>Step-up clock cycle</th></tr> </thead> <tbody> <tr> <td>2'h0</td><td>Halt</td></tr> <tr> <td>2'h1</td><td>2H</td></tr> <tr> <td>2'h2</td><td>4H</td></tr> <tr> <td>2'h3</td><td>8H</td></tr> </tbody> </table> <p>DC4[1:0]</p> <p>Sets a step-up clock cycle of the internal step-up circuit generating VCL. 1H equals 1 horizontal (line) period.</p> <table border="1"> <thead> <tr> <th>DC4[1:0]</th><th>Step-up clock cycle</th></tr> </thead> <tbody> <tr> <td>2'h0</td><td>Halt</td></tr> <tr> <td>2'h1</td><td>1H</td></tr> <tr> <td>2'h2</td><td>1/2H</td></tr> <tr> <td>2'h3</td><td>Setting inhibited</td></tr> </tbody> </table> <p>DC1M[1:0]</p> <p>Sets a step-up clock cycle of the internal step-up circuit generating VSN.</p> <table border="1"> <thead> <tr> <th>DC1M[1:0]</th><th>Step-up clock cycle</th></tr> </thead> <tbody> <tr> <td>2'h0</td><td>Halt</td></tr> <tr> <td>2'h1</td><td>1H</td></tr> <tr> <td>2'h2</td><td>1/2H</td></tr> <tr> <td>2'h3</td><td>Setting inhibited</td></tr> </tbody> </table>	DC1[1:0]	Step-up clock cycle	2'h0	Halt	2'h1	1H	2'h2	1/2H	2'h3	Setting inhibited	DC2[1:0]	Step-up clock cycle	2'h0	Halt	2'h1	2H	2'h2	4H	2'h3	8H	DC4[1:0]	Step-up clock cycle	2'h0	Halt	2'h1	1H	2'h2	1/2H	2'h3	Setting inhibited	DC1M[1:0]	Step-up clock cycle	2'h0	Halt	2'h1	1H	2'h2	1/2H	2'h3	Setting inhibited
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VCOM Setting (D1h)

D1h		VCOM Setting																																																																																																											
		W / R	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex																																																																																																
Command	—	0	X		1	1	0	1	0	0	0	1	D1h																																																																																																
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4th parameter	W / R	1	X	VDC [7]	VDC [6]	VDC [5]	VDC [4]	VDC [3]	VDC [2]	VDC [1]	VDC [0]	VDC [0]	XXh																																																																																																
Description	WCVDC WCVDC=1: Used to enable write to VDC[7:0]. To set NVM write data, write 1 in WCVDC. WCVDC=0: Used to disable write to VDC[7:0]. Values loaded from NVM are retained even if this parameter is written. PVH[6:0] Sets VPLVL that is reference voltage of γ correction registers for positive polarity. Make sure that VSP – VPLVL ≥ 0.3V.																																																																																																												
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7'h12	5.250V																																																																																																												
7'h13	5.225V																																																																																																												
7'h14	5.200V																																																																																																												
7'h15	5.175V																																																																																																												
7'h16	5.150V																																																																																																												
7'h17	5.125V																																																																																																												
7'h18	5.100V																																																																																																												
7'h19	5.075V																																																																																																												
7'h1A	5.050V																																																																																																												
7'h1B	5.025V																																																																																																												
7'h1C	5.000V																																																																																																												
7'h1D	4.975V																																																																																																												
7'h1E	4.950V																																																																																																												
7'h1F	4.925V																																																																																																												
PVH [6:0]	VPLVL																																																																																																												
7'h20	4.900V																																																																																																												
7'h21	4.875V																																																																																																												
7'h22	4.850V																																																																																																												
7'h23	4.825V																																																																																																												
7'h24	4.800V																																																																																																												
7'h25	4.775V																																																																																																												
7'h26	4.750V																																																																																																												
7'h27	4.725V																																																																																																												
7'h28	4.700V																																																																																																												
7'h29	4.675V																																																																																																												
7'h2A	4.650V																																																																																																												
7'h2B	4.625V																																																																																																												
7'h2C	4.600V																																																																																																												
7'h2D	4.575V																																																																																																												
7'h2E	4.550V																																																																																																												
7'h2F	4.525V																																																																																																												

Description	PVH [6:0]	VPLVL	PVH [6:0]	VPLVL	PVH [6:0]	VPLVL
	7'h30	4.500V	7'h48	3.900V	7'h60	3.300V
	7'h31	4.475V	7'h49	3.875V	7'h61	3.275V
	7'h32	4.450V	7'h4A	3.850V	7'h62	3.250V
	7'h33	4.425V	7'h4B	3.825V	7'h63	3.225V
	7'h34	4.400V	7'h4C	3.800V	7'h64	3.200V
	7'h35	4.375V	7'h4D	3.775V	7'h65	3.175V
	7'h36	4.350V	7'h4E	3.750V	7'h66	3.150V
	7'h37	4.325V	7'h4F	3.725V	7'h67	3.125V
	7'h38	4.300V	7'h50	3.700V	7'h68	3.100V
	7'h39	4.275V	7'h51	3.675V	7'h69	3.075V
	7'h3A	4.250V	7'h52	3.650V	7'h6A	3.050V
	7'h3B	4.225V	7'h53	3.625V	7'h6B	3.025V
	7'h3C	4.200V	7'h54	3.600V	7'h6C	3.000V
	7'h3D	4.175V	7'h55	3.575V	7'h6D	Setting inhibited
	7'h3E	4.150V	7'h56	3.550V	7'h6E	Setting inhibited
	7'h3F	4.125V	7'h57	3.525V	7'h6F	Setting inhibited
	7'h40	4.100V	7'h58	3.500V	7'h70	Setting inhibited
	7'h41	4.075V	7'h59	3.475V	7'h71	Setting inhibited
	7'h42	4.050V	7'h5A	3.450V	7'h72	Setting inhibited
	7'h43	4.025V	7'h5B	3.425V	:	:
	7'h44	4.000V	7'h5C	3.400V	7'h7C	Setting inhibited
	7'h45	3.975V	7'h5D	3.375V	7'h7D	Setting inhibited
	7'h46	3.950V	7'h5E	3.350V	7'h7E	Setting inhibited
	7'h47	3.925V	7'h5F	3.325V	7'h7F	Setting inhibited

NVH[6:0]

Sets VNLVL that is reference voltage of γ correction registers for negative polarity.

Make sure that VSP – VPLVL ≤ -0.3V

NVH [6:0]	VNLVL
7'h00	-5.700V
7'h01	-5.675V
7'h02	-5.650V
7'h03	-5.625V
7'h04	-5.600V
7'h05	-5.575V
7'h06	-5.550V
7'h07	-5.525V
7'h08	-5.500V
7'h09	-5.475V
7'h0A	-5.450V
7'h0B	-5.425V
7'h0C	-5.400V
7'h0D	-5.375V
7'h0E	-5.350V
7'h0F	-5.325V
7'h10	-5.300V
7'h11	-5.275V
7'h12	-5.250V
7'h13	-5.225V
7'h14	-5.200V
7'h15	-5.175V
7'h16	-5.150V
7'h17	-5.125V
7'h18	-5.100V
7'h19	-5.075V
7'h1A	-5.050V
7'h1B	-5.025V
7'h1C	-5.000V
7'h1D	-4.975V
7'h1E	-4.950V
7'h1F	-4.925V

NVH [6:0]	VNLVL
7'h20	-4.900V
7'h21	-4.875V
7'h22	-4.850V
7'h23	-4.825V
7'h24	-4.800V
7'h25	-4.775V
7'h26	-4.750V
7'h27	-4.725V
7'h28	-4.700V
7'h29	-4.675V
7'h2A	-4.650V
7'h2B	-4.625V
7'h2C	-4.600V
7'h2D	-4.575V
7'h2E	-4.550V
7'h2F	-4.525V
7'h30	-4.500V
7'h31	-4.475V
7'h32	-4.450V
7'h33	-4.425V
7'h34	-4.400V
7'h35	-4.375V
7'h36	-4.350V
7'h37	-4.325V
7'h38	-4.300V
7'h39	-4.275V
7'h3A	-4.250V
7'h3B	-4.225V
7'h3C	-4.200V
7'h3D	-4.175V
7'h3E	-4.150V
7'h3F	-4.125V

NVH [6:0]	VNLVL
7'h40	-4.100V
7'h41	-4.075V
7'h42	-4.050V
7'h43	-4.025V
7'h44	-4.000V
7'h45	-3.975V
7'h46	-3.950V
7'h47	-3.925V
7'h48	-3.900V
7'h49	-3.875V
7'h4A	-3.850V
7'h4B	-3.825V
7'h4C	-3.800V
7'h4D	-3.775V
7'h4E	-3.750V
7'h4F	-3.725V
7'h50	-3.700V
7'h51	-3.675V
7'h52	-3.650V
7'h53	-3.625V
7'h54	-3.600V
7'h55	-3.575V
7'h56	-3.550V
7'h57	-3.525V
7'h58	-3.500V
7'h59	-3.475V
7'h5A	-3.450V
7'h5B	-3.425V
7'h5C	-3.400V
7'h5D	-3.375V
7'h5E	-3.350V
7'h5F	-3.325V

Description	NVH [6:0]	VNLVL	NVH [6:0]	VNLVL	NVH [6:0]	VNLVL
	7'h60	-3.300V	7'h68	-3.100V	7'h70	Setting inhibited
	7'h61	-3.275V	7'h69	-3.075V	7'h71	Setting inhibited
	7'h62	-3.250V	7'h6A	-3.050V	7'h72	Setting inhibited
	7'h63	-3.225V	7'h6B	-3.025V	:	:
	7'h64	-3.200V	7'h6C	-3.000V	7'h7C	Setting inhibited
	7'h65	-3.175V	7'h6D	Setting inhibited	7'h7D	Setting inhibited
	7'h66	-3.150V	7'h6E	Setting inhibited	7'h7E	Setting inhibited
	7'h67	-3.125V	7'h6F	Setting inhibited	7'h7F	Setting inhibited

VDC[7:0]		VDC[7:0]		VDC[7:0]	
The bit is used to set VCOMDC output voltage. VCOMDC = -0.3V ~ -3.0V.					
VDC[7:0]	VCOMDC	VDC[7:0]	VCOMDC	VDC[7:0]	VCOMDC
8'h00	Setting inhibited	8'h20	VNLVL x 0.096	8'h40	VNLVL x 0.193
8'h01	Setting inhibited	8'h21	VNLVL x 0.099	8'h41	VNLVL x 0.196
8'h02	Setting inhibited	8'h22	VNLVL x 0.102	8'h42	VNLVL x 0.199
8'h03	Setting inhibited	8'h23	VNLVL x 0.105	8'h43	VNLVL x 0.202
8'h04	Setting inhibited	8'h24	VNLVL x 0.108	8'h44	VNLVL x 0.205
8'h05	Setting inhibited	8'h25	VNLVL x 0.111	8'h45	VNLVL x 0.208
8'h06	Setting inhibited	8'h26	VNLVL x 0.114	8'h46	VNLVL x 0.211
8'h07	Setting inhibited	8'h27	VNLVL x 0.117	8'h47	VNLVL x 0.214
8'h08	Setting inhibited	8'h28	VNLVL x 0.120	8'h48	VNLVL x 0.217
8'h09	Setting inhibited	8'h29	VNLVL x 0.123	8'h49	VNLVL x 0.220
8'h0A	Setting inhibited	8'h2A	VNLVL x 0.127	8'h4A	VNLVL x 0.223
8'h0B	Setting inhibited	8'h2B	VNLVL x 0.130	8'h4B	VNLVL x 0.226
8'h0C	Setting inhibited	8'h2C	VNLVL x 0.133	8'h4C	VNLVL x 0.229
8'h0D	Setting inhibited	8'h2D	VNLVL x 0.136	8'h4D	VNLVL x 0.232
8'h0E	Setting inhibited	8'h2E	VNLVL x 0.139	8'h4E	VNLVL x 0.235
8'h0F	Setting inhibited	8'h2F	VNLVL x 0.142	8'h4F	VNLVL x 0.238
8'h10	VNLVL x 0.048	8'h30	VNLVL x 0.145	8'h50	VNLVL x 0.241
8'h11	VNLVL x 0.051	8'h31	VNLVL x 0.148	8'h51	VNLVL x 0.244
8'h12	VNLVL x 0.054	8'h32	VNLVL x 0.151	8'h52	VNLVL x 0.247
8'h13	VNLVL x 0.057	8'h33	VNLVL x 0.154	8'h53	VNLVL x 0.250
8'h14	VNLVL x 0.060	8'h34	VNLVL x 0.157	8'h54	VNLVL x 0.253
8'h15	VNLVL x 0.063	8'h35	VNLVL x 0.160	8'h55	VNLVL x 0.256
8'h16	VNLVL x 0.066	8'h36	VNLVL x 0.163	8'h56	VNLVL x 0.259
8'h17	VNLVL x 0.069	8'h37	VNLVL x 0.166	8'h57	VNLVL x 0.262
8'h18	VNLVL x 0.072	8'h38	VNLVL x 0.169	8'h58	VNLVL x 0.265
8'h19	VNLVL x 0.075	8'h39	VNLVL x 0.172	8'h59	VNLVL x 0.268
8'h1A	VNLVL x 0.078	8'h3A	VNLVL x 0.175	8'h5A	VNLVL x 0.271
8'h1B	VNLVL x 0.081	8'h3B	VNLVL x 0.178	8'h5B	VNLVL x 0.274
8'h1C	VNLVL x 0.084	8'h3C	VNLVL x 0.181	8'h5C	VNLVL x 0.277
8'h1D	VNLVL x 0.087	8'h3D	VNLVL x 0.184	8'h5D	VNLVL x 0.280
8'h1E	VNLVL x 0.090	8'h3E	VNLVL x 0.187	8'h5E	VNLVL x 0.283
8'h1F	VNLVL x 0.093	8'h3F	VNLVL x 0.190	8'h5F	VNLVL x 0.286

Description	VDC[7:0]	VCOMDC	VDC[7:0]	VCOMDC	VDC[7:0]	VCOMDC
	8'h60	VNLVL x 0.289		8'h80	VNLVL x 0.386	
	8'h61	VNLVL x 0.292		8'h81	VNLVL x 0.389	
	8'h62	VNLVL x 0.295		8'h82	VNLVL x 0.392	
	8'h63	VNLVL x 0.298		8'h83	VNLVL x 0.395	
	8'h64	VNLVL x 0.301		8'h84	VNLVL x 0.398	
	8'h65	VNLVL x 0.304		8'h85	VNLVL x 0.401	
	8'h66	VNLVL x 0.307		8'h86	VNLVL x 0.404	
	8'h67	VNLVL x 0.310		8'h87	VNLVL x 0.407	
	8'h68	VNLVL x 0.313		8'h88	VNLVL x 0.410	
	8'h69	VNLVL x 0.316		8'h89	VNLVL x 0.413	
	8'h6A	VNLVL x 0.319		8'h8A	VNLVL x 0.416	
	8'h6B	VNLVL x 0.322		8'h8B	VNLVL x 0.419	
	8'h6C	VNLVL x 0.325		8'h8C	VNLVL x 0.422	
	8'h6D	VNLVL x 0.328		8'h8D	VNLVL x 0.425	
	8'h6E	VNLVL x 0.331		8'h8E	VNLVL x 0.428	
	8'h6F	VNLVL x 0.334		8'h8F	VNLVL x 0.431	
	8'h70	VNLVL x 0.337		8'h90	VNLVL x 0.434	
	8'h71	VNLVL x 0.340		8'h91	VNLVL x 0.437	
	8'h72	VNLVL x 0.343		8'h92	VNLVL x 0.440	
	8'h73	VNLVL x 0.346		8'h93	VNLVL x 0.443	
	8'h74	VNLVL x 0.349		8'h94	VNLVL x 0.446	
	8'h75	VNLVL x 0.352		8'h95	VNLVL x 0.449	
	8'h76	VNLVL x 0.355		8'h96	VNLVL x 0.452	
	8'h77	VNLVL x 0.358		8'h97	VNLVL x 0.455	
	8'h78	VNLVL x 0.361		8'h98	VNLVL x 0.458	
	8'h79	VNLVL x 0.364		8'h99	VNLVL x 0.461	
	8'h7A	VNLVL x 0.367		8'h9A	VNLVL x 0.464	
	8'h7B	VNLVL x 0.370		8'h9B	VNLVL x 0.467	
	8'h7C	VNLVL x 0.373		8'h9C	VNLVL x 0.470	
	8'h7D	VNLVL x 0.377		8'h9D	VNLVL x 0.473	
	8'h7E	VNLVL x 0.380		8'h9E	VNLVL x 0.476	
	8'h7F	VNLVL x 0.383		8'h9F	VNLVL x 0.479	

Description	VDC[7:0]	VCOMDC	VDC[7:0]	VCOMDC	VDC[7:0]	VCOMDC
	8'hC0	VNLVL x 0.578	8'hD6	VNLVL x 0.645	8'hEC	VNLVL x 0.711
	8'hC1	VNLVL x 0.581	8'hD7	VNLVL x 0.648	8'hED	VNLVL x 0.714
	8'hC2	VNLVL x 0.584	8'hD8	VNLVL x 0.651	8'hEE	VNLVL x 0.717
	8'hC3	VNLVL x 0.587	8'hD9	VNLVL x 0.654	8'hEF	VNLVL x 0.720
	8'hC4	VNLVL x 0.590	8'hDA	VNLVL x 0.657	8'hF0	Setting inhibited
	8'hC5	VNLVL x 0.593	8'hDB	VNLVL x 0.660	8'hF1	Setting inhibited
	8'hC6	VNLVL x 0.596	8'hDC	VNLVL x 0.663	8'hF2	Setting inhibited
	8'hC7	VNLVL x 0.599	8'hDD	VNLVL x 0.666	8'hF3	Setting inhibited
	8'hC8	VNLVL x 0.602	8'hDE	VNLVL x 0.669	8'hF4	Setting inhibited
	8'hC9	VNLVL x 0.605	8'hDF	VNLVL x 0.672	8'hF5	Setting inhibited
	8'hCA	VNLVL x 0.608	8'hE0	VNLVL x 0.675	8'hF6	Setting inhibited
	8'hCB	VNLVL x 0.611	8'hE1	VNLVL x 0.678	8'hF7	Setting inhibited
	8'hCC	VNLVL x 0.614	8'hE2	VNLVL x 0.681	8'hF8	Setting inhibited
	8'hCD	VNLVL x 0.617	8'hE3	VNLVL x 0.684	8'hF9	Setting inhibited
	8'hCE	VNLVL x 0.620	8'hE4	VNLVL x 0.687	8'hFA	Setting inhibited
	8'hCF	VNLVL x 0.623	8'hE5	VNLVL x 0.690	8'hFB	Setting inhibited
	8'hD0	VNLVL x 0.627	8'hE6	VNLVL x 0.693	8'hFC	Setting inhibited
	8'hD1	VNLVL x 0.630	8'hE7	VNLVL x 0.696	8'hFD	Setting inhibited
	8'hD2	VNLVL x 0.633	8'hE8	VNLVL x 0.699	8'hFE	Setting inhibited
	8'hD3	VNLVL x 0.636	8'hE9	VNLVL x 0.702	8'hFF	Setting inhibited
	8'hD4	VNLVL x 0.639	8'hEA	VNLVL x 0.705		
	8'hD5	VNLVL x 0.642	8'hEB	VNLVL x 0.708		

X = Don't care

Restriction	Note: When this command is read via DSI or MDDI, dummy read operation is not performed.
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Test Mode 4 (D6h)

D6h		Test Mode 4										
	W / R	DCX	DB23- DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	—	0	X	1	1	0	1	0	1	1	0	D6h
Dummy Parameter	R	1	X	X	X	X	X	X	X	X	X	XXh
1st parameter	R	1	X	1	0	1	0	1	0	0	0	A8h
Description	Test mode command. Do not access this command and its parameters. X = Don't care											

Test Mode 5 (D7h)

D7h	Test Mode 5											
	W / R	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	—	0	X	1	1	0	1	0	1	1	1	D7h
Dummy Parameter	R	1	X	X	X	X	X	X	X	X	X	XXh
1st parameter	R	1	X	0	0	0	0	0	0	0	0	00h
2nd parameter	R	1	X	0	0	0	0	0	0	0	0	00h
3rd parameter	R	1	X	1	0	0	0	1	0	0	0	88h
4th parameter	R	1	X	1	0	1	0	0	0	0	0	A0h
5th parameter	R	1	X	0	0	1	0	1	0	0	0	28h
6th parameter	R	1	X	0	0	1	0	1	0	1	0	2Ah
7th parameter	R	1	X	0	0	1	0	0	0	1	0	22h
8th parameter	R	1	X	0	0	0	0	0	0	0	1	01h
9th parameter	R	1	X	0	1	1	1	0	0	0	1	71h
10th parameter	R	1	X	0	0	0	0	1	0	0	0	08h
11th parameter	R	1	X	0	1	0	0	0	0	1	0	42h
12th parameter	R	1	X	0	0	0	0	0	0	0	0	00h
13th parameter	R	1	X	1	0	0	0	0	0	0	0	80h
14th parameter	R	1	X	1	0	0	0	0	0	0	0	80h
15th parameter	R	1	X	0	0	0	0	0	0	1	1	03h
Description	Test mode command. Do not access this command and its parameters. X = Don't care.											

Test Mode 6 (D8h)

D8h	Test Mode 6											
	W / R	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	—	0	X	1	1	0	1	1	0	0	0	D8h
Dummy Parameter	R	1	X	X	X	X	X	X	X	X	X	XXh
1st parameter	R	1	X	0	1	1	0	0	1	1	0	66h
2nd parameter	R	1	X	0	1	1	0	0	1	1	0	66h
3rd parameter	R	1	X	0	0	1	0	0	0	1	0	22h
4th parameter	R	1	X	0	1	1	0	0	1	1	0	66h
5th parameter	R	1	X	0	0	1	0	0	0	0	1	21h
6th parameter	R	1	X	0	1	1	0	1	0	0	0	68h
7th parameter	R	1	X	0	0	1	0	0	0	1	0	22h
8th parameter	R	1	X	0	1	1	0	0	0	1	0	62h
9th parameter	R	1	X	0	0	0	0	0	1	0	1	05h
Description	Test mode command. Do not access this command and its parameters. X = Don't care											

Test Mode 7 (D9h)

D9h	Test Mode 7											
	W / R	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	—	0	X	1	1	0	1	1	0	0	1	D9h
Dummy Parameter	R	1	X	X	X	X	X	X	X	X	X	XXh
1st parameter	R	1	X	1	1	0	0	1	1	1	1	Cfh
2nd parameter	R	1	X	0	1	1	0	1	1	0	1	6Dh
3rd parameter	R	1	X	1	1	0	1	0	0	1	1	D3h
Description	Test mode command. Do not access this command and its parameters. X = Don't care											

Test Mode 8 (DAh)

DAh	Test Mode 8											
	W / R	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	—	0	X	1	1	0	1	1	0	1	0	DAh
Dummy Parameter	R	1	X	X	X	X	X	X	X	X	X	XXh
1st parameter	R	1	X	0	0	0	0	0	0	0	1	01h
Description	Test mode command. Do not access this command and its parameters. X = Don't care											

NVM Control Command**NVM Access Control (E0h)**

NVM Access Control												
E0h	W / R	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	—	0	X	1	1	1	0	0	0	0	0	E0h
1st parameter	W / R	1	X	0	0	0	0	0	0	0	NVAE	0Xh
2nd parameter	W / R	1	X	0	FTT	0	0	0	0	0	0	X0h
3rd parameter	W / R	1	X	0	0	0	TEM [0]	0	0	VERIF LGWR	VERIF LGER	XXh
4th parameter	W / R	1	X	0	0	0	0	0	0	0	0	00h
Description	NVAE NVM access enable register. NVM access is enabled when NVAE=1. FTT NVM access control register. When FTT=1, NVM write operation or NVM erase operation starts. After NVM write and verify operations, FTT is returned to 0. VERIFLGER When data is written to NVM, this bit returns erase-verify result after erase-erase verify operation. This bit is read-only bit. The data written to this bit is disregarded. Erase-verify operation passes: VERIFLGER = 1. Erase verify operation fails: VERIFLGER = 0. VERIFLGWR After data is erased from NVM, this bit returns write verify result after write-write verify operation. This bit is read-only bit. The data written to this bit is disregarded. Write-verify operation passes: VERIFLGWR = 1. Write verify operation fails: VERIFLGWR = 0.											

```

graph TD
    S0((0  
Fail)) -- "Verify Fail" --> S0
    S0 -- "FTT = 0 → 1" --> S1((1  
Pass))
    S1 -- "Verify Pass" --> S0
    HWRESET[HWRESET] --> S0
  
```

Description	TEM[0] Sets the data output from the TE pin. <table border="1"><thead><tr><th>TEM[0]</th><th>TE output</th></tr></thead><tbody><tr><td>0</td><td>Tearing Effect</td></tr><tr><td>1</td><td>Data automatically written to NVM is verified. (VERIFLGER & VERIFLGWR) TE = 0: Verification result is NG. TE = 1: Verification result is OK.</td></tr></tbody></table> X = Don't care	TEM[0]	TE output	0	Tearing Effect	1	Data automatically written to NVM is verified. (VERIFLGER & VERIFLGWR) TE = 0: Verification result is NG. TE = 1: Verification result is OK.
TEM[0]	TE output						
0	Tearing Effect						
1	Data automatically written to NVM is verified. (VERIFLGER & VERIFLGWR) TE = 0: Verification result is NG. TE = 1: Verification result is OK.						
Restriction	Note: When this command is read via DSI or MDDI, dummy read operation is not performed.						

set_DDB_write_control (E1h)

set_DDB write_control												
E1h	W / R	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	—	0	X	1	1	1	0	0	0	0	1	E1h
1st parameter	W / R	1	X	0	0	0	0	0	0	WCIFI D	WCD DB	0Xh
2nd parameter	W / R	1	X	DDB0 [7]	DDB0 [6]	DDB0 [5]	DDB0 [4]	DDB0 [3]	DDB0 [2]	DDB0 [1]	DDB0 [0]	XXh
3rd parameter	W / R	1	X	DDB1 [7]	DDB1 [6]	DDB1 [5]	DDB1 [4]	DDB1 [3]	DDB1 [2]	DDB1 [1]	DDB1 [0]	XXh
4th parameter	W / R	1	X	DDB2 [7]	DDB2 [6]	DDB2 [5]	DDB2 [4]	DDB2 [3]	DDB2 [2]	DDB2 [1]	DDB2 [0]	XXh
5th parameter	W / R	1	X	DDB3 [7]	DDB3 [6]	DDB3 [5]	DDB3 [4]	DDB3 [3]	DDB3 [2]	DDB3 [1]	DDB3 [0]	XXh
6th parameter	W / R	1	X	0	IFID [6]	IFID [5]	IFID [4]	IFID [3]	IFID [2]	IFID [1]	IFID [0]	XXh
Description	<p>The command writes information from the display module as follows:</p> <p>2nd parameter (DDB0[7:0]): MS byte of Supplier ID (ID1[15:8])</p> <p>3rd parameter (DDB1[7:0]): LS byte of Supplier ID (ID1[7:0])</p> <p>4th parameter (DDB2[7:0]): Supplier Elective Data (ID2[15:8])</p> <p>5th parameter (DDB3[7:0]): Supplier Elective Data (ID2[7:0])</p> <p>6th parameter: IFID[6:0]</p> <p>WCDDDB</p> <p>WCDDDB = 1: This bit enables to write data to ID1[15:0] and ID2[15:0] (A1h). Data that is set in ID1[15:0] and ID2[15:0] can be written to NVM.</p> <p>WCDDDB = 0: This bit disables to write data to ID1[15:0] and ID2[15:0] (A1h). Set WCDDDB = 0 except when data is written to NVM.</p> <p>WCIFID</p> <p>WCIFID = 1: This bit enables to write data to IFID[6:0] (A1h). Data that is set in IFID[6:0] (A1h) can be written to NVM.</p> <p>WCDDDB = 0: This bit disables to write data to IFID[6:0] (A1h). Set WCIFID = 0 except when data is written to NVM.</p> <p>X = Don't care</p>											
Restriction	Note: When this command is read via DSI or MDDI, dummy read operation is not performed.											

NVM Load Control (E2h)

NVM Load Control												
E2h	W / R	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	—	0	X	1	1	1	0	0	0	1	0	E2h
1st parameter	W / R	1	X	1	LD[6]	LD[5]	LD[4]	LD[3]	LD[2]	LD[1]	LD[0]	XXh
Description	LD[7:0] Sets command to execute data load from the NVM during each sequence. LD[x] = 0 does not execute data load from the NVM to each command. In this case, a setting value before data load is not overwritten. LD[x] = 1 executes data load from the NVM to each command. In this case, a setting value before data load is overwritten.											
	Load control commands in NVM Load operation Unconditional Manufacturer Command: E2h LD[0] Manufacturer Command: E1h (parameters 1~6) LD[1] Manufacturer Command: B3h (parameters 1~4), B4h (parameter 1), B6h (parameters 1~2), B7h (parameters 1~4) LD[2] Manufacturer Command: B8h (parameters 1~20), B9h (parameters 1~4) LD[3] Manufacturer Command: C0h (parameters 1~8), C1h (parameters 1~5), C3h (parameter 1), C4h (parameters 1~4), C6h (parameter 1), C7h (parameters 1~2), C8h (parameters 1~6) LD[4] Manufacturer Command: C8h (parameters 7~24), C9h (parameters 1~24), CAh (parameters 1~24) LD[5] Manufacturer Command: D0h (parameters 1~16), D1h (parameters 1~4), D3h (parameter 1), D7h (parameters 1~15), D8h (parameters 1~9), D9h (parameters 1~3), DAh (parameter 1) LD[6] Manufacturer Command: CCh (parameter 1), D6h (parameter 1), E6h (parameter 1), F3h (parameters 1~5), F8h (parameter 1), FAh (parameter 1), FCCh (parameters 1~5), FDh (parameters 1~13), FEh (parameters 1~8)											
	X = Don't care											
Restriction	Note: When this command is read via DSI or MDDI, dummy read operation is not performed.											

Test Mode 9 (E4h)

E4h		Test Mode 9											
		W / R	DCX	DB23- DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	-	0	X	1	1	1	0	0	1	0	0	E4h	
1st parameter	R	1	X	0	0	0	0	0	0	0	0	00h	
2nd parameter	R	1	X	0	0	0	0	0	0	0	0	00h	
3rd parameter	R	1	X	0	0	1	0	0	0	1	0	22h	
4th parameter	R	1	X	1	0	1	0	1	0	1	0	AAh	
5th parameter	R	1	X	0	0	0	0	0	0	0	0	00h	
Description	Test mode command. Do not access this command and its parameters. X = Don't care												

Test Mode 10 (E5h)

E5h		Test Mode 10											
		W / R	DCX	DB23- DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	-	0	X	1	1	1	0	0	1	0	1	E5h	
1st parameter	R	1	X	0	0	0	0	0	0	0	0	00h	
Description	Test mode command. Do not access this command and its parameters. X = Don't care												

Test Mode 11 (E6h)

E6h		Test Mode 11											
		W / R	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	-	0	X	1	1	1	0	0	1	1	0	E6h	
1st parameter	R	1	X	0	0	0	0	0	0	0	0	00h	
Description	Test mode command. Do not access this command and its parameters. X = Don't care												

Test Mode 12 (E7h)

E7h		Test Mode 12											
		W / R	DCX	DB23-DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	-	0	X	1	1	1	0	0	1	1	1	E7h	
1st parameter	R	1	X	0	0	0	0	0	0	0	0	00h	
2nd parameter	R	1	X	0	0	0	0	0	0	0	0	00h	
3rd parameter	R	1	X	0	0	0	0	0	0	0	0	00h	
4th parameter	R	1	X	0	0	0	0	0	0	0	0	00h	
5th parameter	R	1	X	0	0	0	0	0	0	0	0	00h	
Description	Test mode command. Do not access this command and its parameters. X = Don't care												

Test Mode 13 (F3h)

F3h		Test Mode 13											
		W / R	DCX	DB23- DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	-	0	X	1	1	1	1	0	0	1	1	1	F3h
1st parameter	R	1	X	0	0	0	0	0	1	1	0	06h	
2nd parameter	R	1	X	0	0	0	0	0	0	0	0	00h	
3rd parameter	R	1	X	0	0	0	0	0	0	0	0	00h	
4th parameter	R	1	X	0	0	1	0	0	1	0	0	24h	
5th parameter	R	1	X	0	0	0	0	0	0	0	0	00h	
Description	Test mode command. Do not access this command and its parameters. X = Don't care												

Read Mode In for DBI Only (F5h)

F5h		Read Mode In for DBI Only										
		W / R	DCX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	-	0	1	1	1	1	1	0	1	0	1	F5h
Description	When MIPI DBI Type C is selected, Manufacturer Command read mode is entered. When Manufacturer command is input after this command, a parameter is output in synchronization with a falling edge of SCL. To exit the read mode, input the F6h command. In read sequence, CSX should not be raised between read command and read parameter, and between read parameters before all parameters are read. If a pause is invoked between read command and read parameter, write sequence is executed and data is overwritten. X = Don't care											
Restriction	This command can be used only when MIPI DBI Type C is selected.											

Read Mode Out for DBI Only (F6h)

F6h		Read Mode Out for DBI only									
	W / R	DCX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	-	0	1	1	1	1	0	1	1	0	F6h
Description	Input this command to execute the read mode entered by the F5h command. X = Don't care										
Restriction	This command can be used only when MIPI DBI Type C is selected.										

Test Mode 14 (F8h)

F8h		Test Mode 14										
	W / R	DCX	DB23- DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	-	0	X	1	1	1	1	1	0	0	0	F8h
1st parameter	R	1	X	0	0	0	0	0	0	0	0	00h
Description	Test mode command. Do not access this command and its parameters. X = Don't care											

Test Mode 15 (FAh)

FAh		Test Mode 15										
	W / R	DCX	DB23- DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	-	0	X	1	1	1	1	1	0	1	0	FAh
1st parameter	R	1	X	0	0	0	0	1	0	0	1	09h
Description	Test mode command. Do not access this command and its parameters. X = Don't care											

Test Mode 16 (FCh)

FCh	Test Mode 16											
	W / R	DCX	DB23- DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	-	0	X	1	1	1	1	1	1	0	0	FCh
1st parameter	R	1	X	0	0	0	0	0	0	0	0	00h
2nd parameter	R	1	X	0	0	0	0	0	0	0	0	00h
3rd parameter	R	1	X	0	0	0	0	0	0	0	0	00h
4th parameter	R	1	X	0	0	0	0	0	0	0	0	00h
5th parameter	R	1	X	0	0	0	0	0	0	0	0	00h
Description	Test mode command. Do not access this command and its parameters. X = Don't care											

Test Mode 17 (FDh)

FDh	Test Mode 17											
	W / R	DCX	DB23- DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	-	0	X	1	1	1	1	1	1	0	1	FDh
1st parameter	R	1	X	0	0	0	0	0	0	0	0	00h
2nd parameter	R	1	X	0	0	0	0	0	0	0	0	00h
3rd parameter	R	1	X	0	1	1	1	0	0	0	0	70h
4th parameter	R	1	X	0	0	0	0	0	0	0	0	00h
5th parameter	R	1	X	0	0	1	1	0	0	1	0	32h
6th parameter	R	1	X	0	0	1	1	0	0	0	1	31h
7th parameter	R	1	X	0	0	1	1	0	1	0	0	34h
8th parameter	R	1	X	0	0	1	1	0	0	0	0	30h
9th parameter	R	1	X	0	0	1	1	0	0	1	0	32h
10th parameter	R	1	X	0	0	1	1	0	0	0	1	31h
11th parameter	R	1	X	0	0	0	0	0	1	0	0	04h
12th parameter	R	1	X	0	0	0	0	0	0	0	0	00h
13th parameter	R	1	X	0	0	0	0	0	0	0	0	00h
Description	Test mode command. Do not access this command and its parameters. X = Don't care											

Test Mode 18 (FEh)

FEh	Test Mode 18											
	W / R	DCX	DB23- DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex
Command	-	0	X	1	1	1	1	1	1	1	0	FEh
1st parameter	R	1	X	1	0	0	0	0	0	0	0	00h
2nd parameter	R	1	X	1	0	0	0	0	0	0	0	00h
3rd parameter	R	1	X	1	0	0	0	0	0	0	0	00h
4th parameter	R	1	X	1	0	1	0	0	0	0	0	20h
5th parameter	R	1	X	0	0	0	0	0	0	0	0	00h
6th parameter	R	1	X	0	0	0	0	0	0	0	0	00h
7th parameter	R	1	X	1	1	1	1	0	0	0	0	F0h
8th parameter	R	1	X	1	1	1	1	1	1	1	1	FFh
Description	Test mode command. Do not access this command and its parameters. X = Don't care											

Reset

The R61529 is set to its internal initial setting during a reset period initiated by a RESET input. During the RESET period, no command is accepted from the host processor. The source driver unit and the power supply circuit unit are also reset to the respective initial states when RESET signal is input to the R61529.

Command Default Values

The default values of commands are shown in the “Default Modes and Values” table in Command List. The command setting is initialized to the default value when a Hardware Reset is executed. A table below shows initial states of input/output pins after reset.

Table 54 Initial State of Input/Output pins (T.B.D.)

Pin name	Input/Output Pin Initial State	Pin name	Input/Output Pin Initial State
VDD	1.5V	C11P	VCI
VSP	VCI	C11M	GND
VSN	GND	C12P	VCI
VPLVL	Hi-Z	C12M	GND
VNLVL	Hi-Z	C13P	VCI
VCL	GND	C13M	GND
VGH	GND	C14P	VCI
VGL	GND	C14M	GND
		C21P	GND
		C21M	GND
		C22P	GND
		C22M	GND
VGS	GND	C23P	GND
VCOMDC	GND	C23M	GND
VCOM	GND	C41P	VCI
S1-S960	GND	C41M	GND
G1-G480	GND	C42P	VCI
		C42M	GND
DB23-DB0	Hi-Z		
DIN	Hi-Z		
DOUT (Note)	IOVCC1		
TE	GND		
LEDPWM	GND		

Note: When RESETX is low, an output state of DOUT is GND during reset. After RESETX is set to high, an output state of this pin is IOVCC1 during reset.

Frame Memory

The frame memory retains image data of up to 3,686,400 bits (480 x 320 x 24 bits).

Address Mapping from Memory to Display

Normal Display On or Partial Mode On

In this mode, a content of the frame memory within an area where column pointer is 0000h to 013Fh and page pointer is 0000h to 01DFh is displayed.

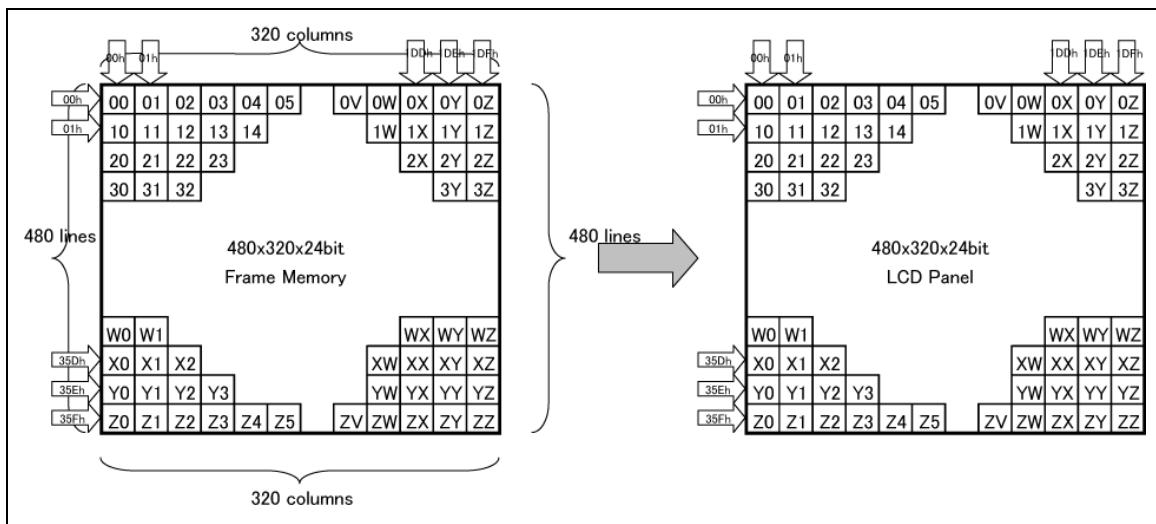


Figure 119

Write/Read Direction from/to Host Processor

Below figure illustrates data stream from the host processor.

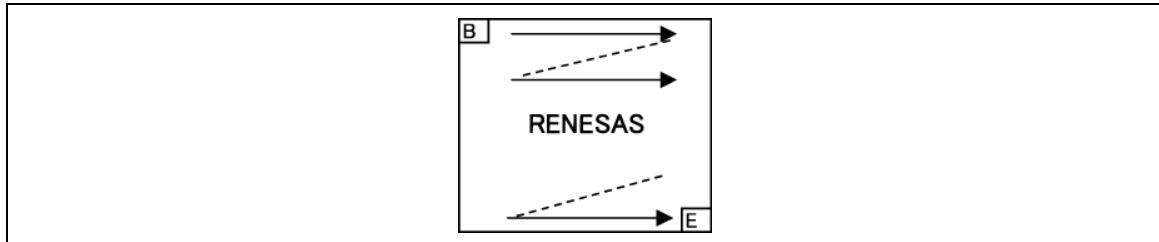


Figure 120

The data is written in the order illustrated above. The Counter which dictates write position on the physical memory is controlled by “set_address_mode (36h)” command Bits B5, B6, B7 as illustrated below.

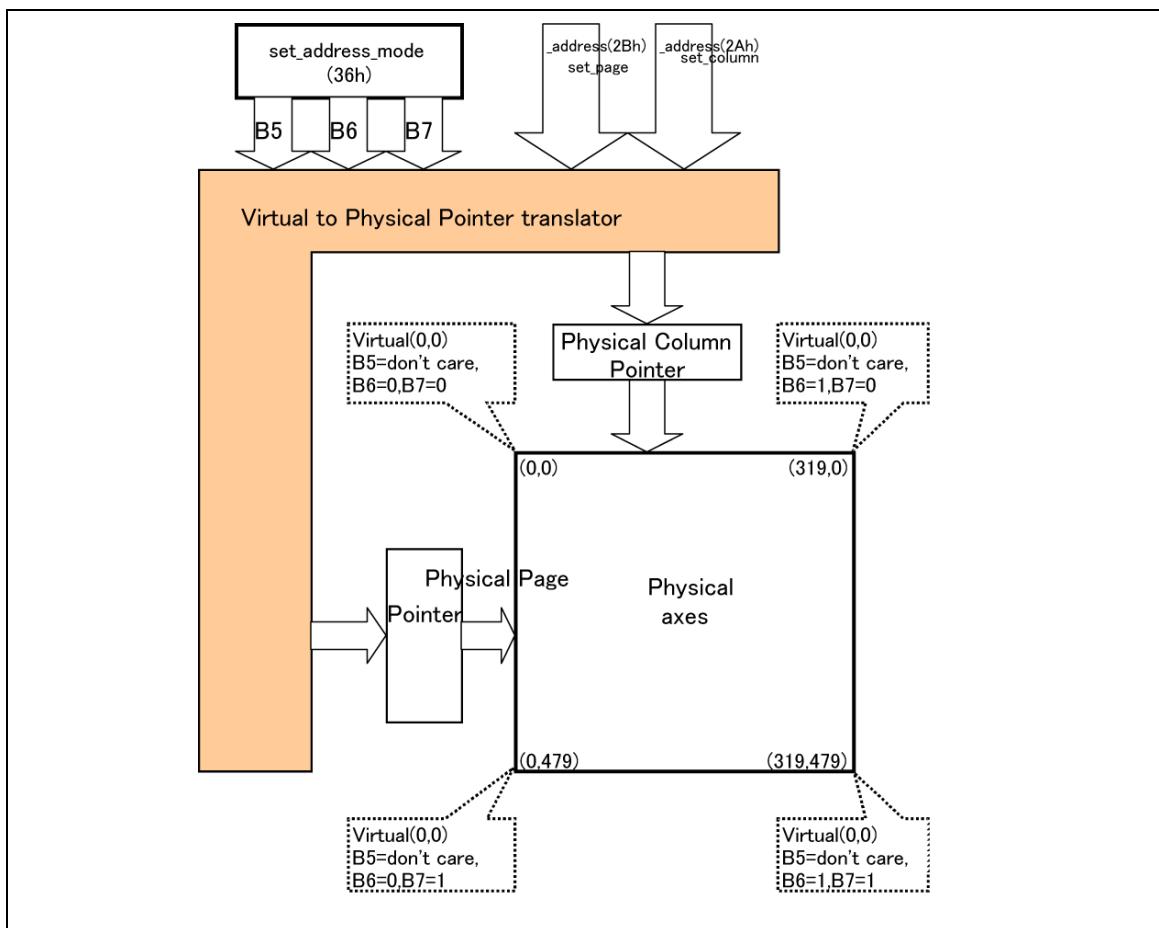


Figure 121

Table 55

B5	B6	B7	Column Address	Page Address
0	0	0	Direct to Physical Column Pointer	Direct to Physical Page Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (479-Physical Page Pointer)
0	1	0	Direct to (319-Physical Column Pointer)	Direct to Physical Page Pointer
0	1	1	Direct to (319-Physical Column Pointer)	Direct to (479-Physical Page Pointer)
1	0	0	Direct to Physical Page Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (479-Physical Page Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Page Pointer	Direct to (319-Physical Column Pointer)
1	1	1	Direct to (479-Physical Column Pointer)	Direct to (319-Physical Page Pointer)

For each image orientation, the controls on the column and page counters apply as below.

Note: Data is always written to the Frame Memory in the same order, regardless of the Memory Write Direction set by set_address_mode (36h) bits B7, B6 and B5. The write order for each pixel unit is as follows.

Table 56

D23	D22	D21	D20	D19	D18	D17	D16
R7	R6	R5	R4	R3	R2	R1	R0

D15	D14	D13	D12	D11	D10	D9	D8
G7	G6	G5	G4	G3	G2	G1	G0

D7	D6	D5	D4	D3	D2	D1	D0
B7	B6	B5	B4	B3	B2	B1	B0

Table 57 Address pointer (counter) operation

Condition	Column counter	Page counter	Note
When commands write_memory_start (2Ch) and read_memory_start (2Eh) are received.	Back to Start Column	Back to Start Page	
Execute Pixel Read/Write	Increment by 1	No change	
When column counter value is larger than "End Column"	Back to Start Column	Increment by 1	
When column counter value is larger than "End Column" and page counter value is larger than "End Page"	STOP	STOP	Entry Mode(B3h) WEMODE=0
	Back to Start Column	Back to Start Page	Entry Mode(B3h) WEMODE=1

One pixel unit represents 1 column and 1 page counter value on the Frame Memory. See the next page for the resultant image for each orientation setting.

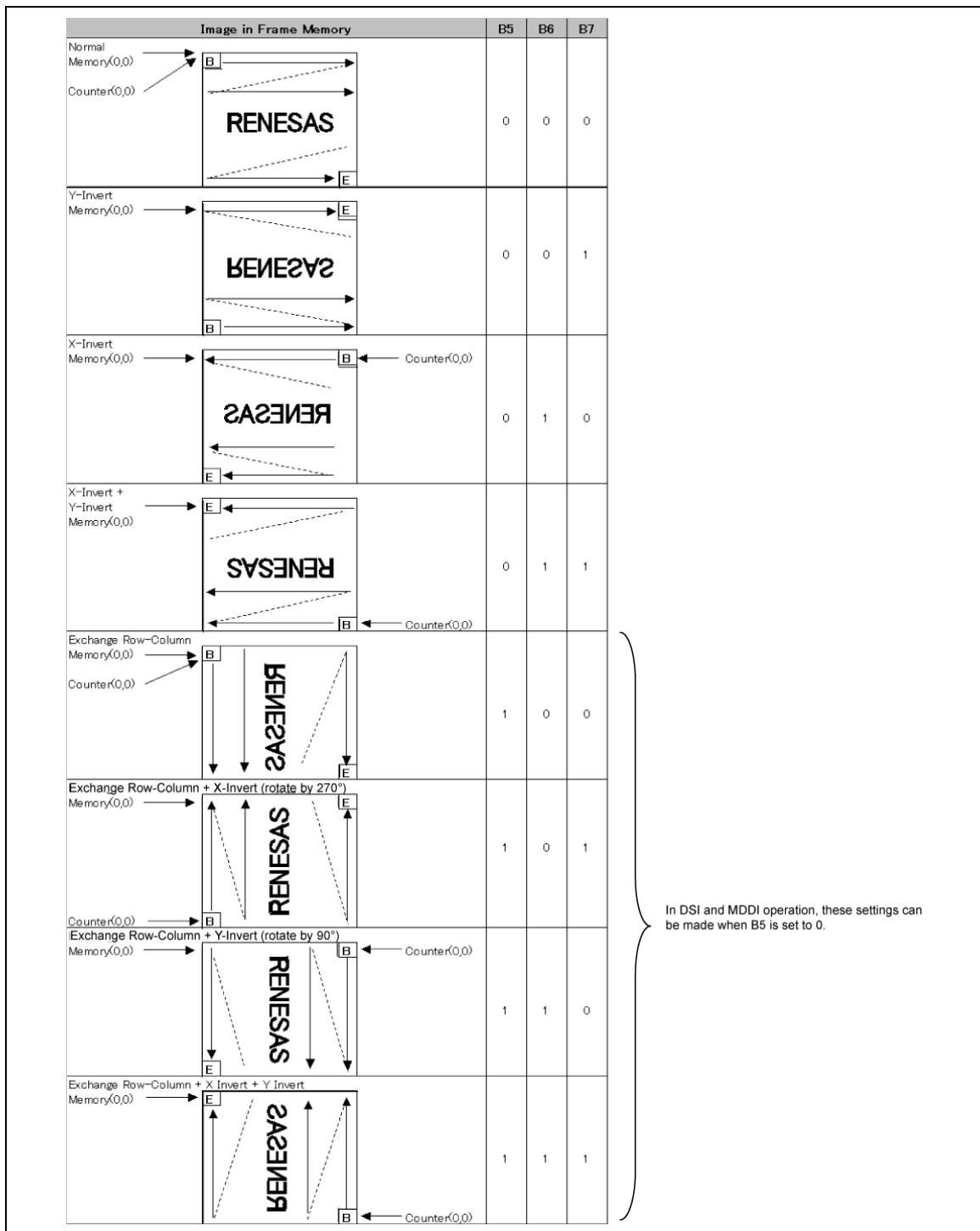


Figure 122

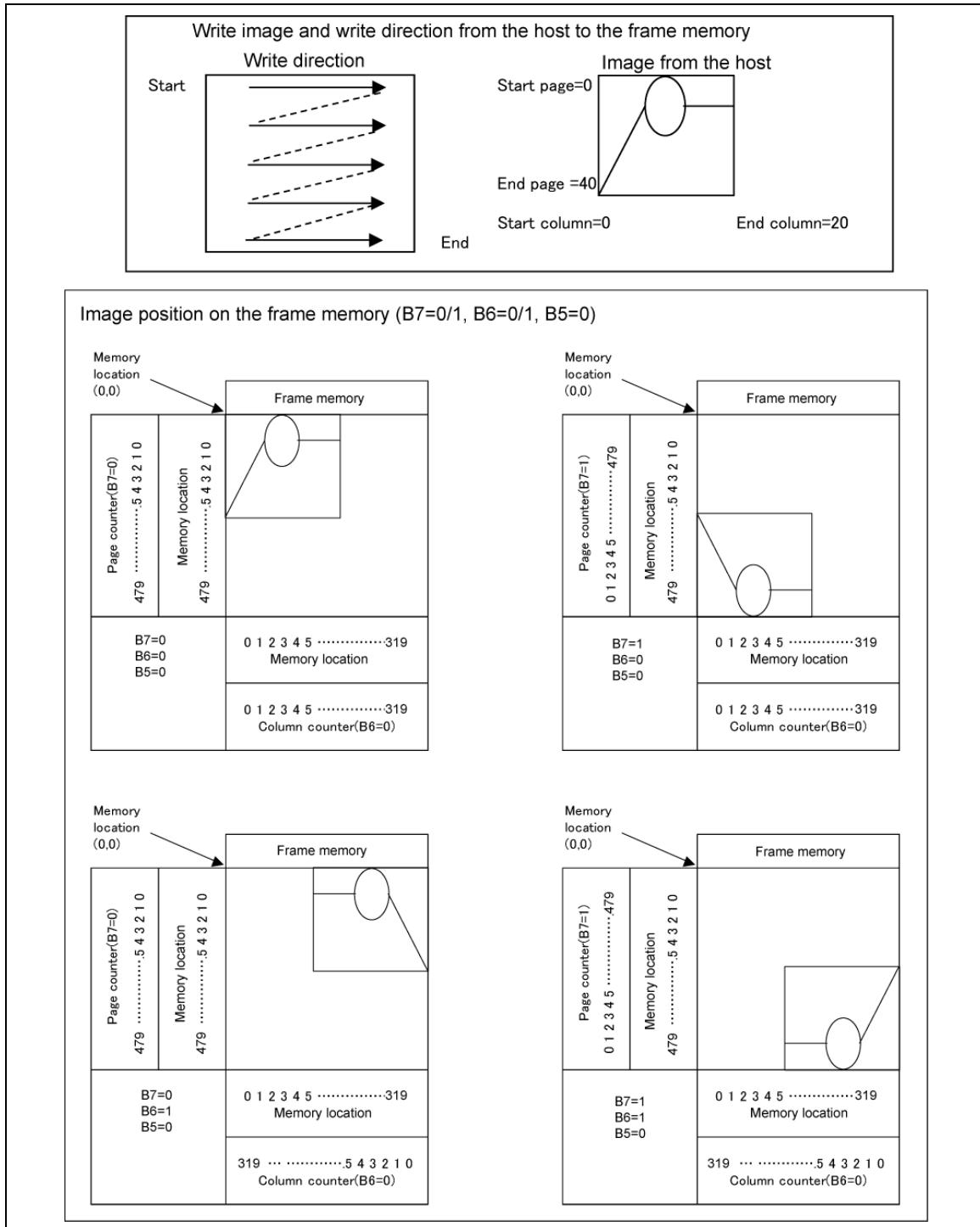


Figure 123

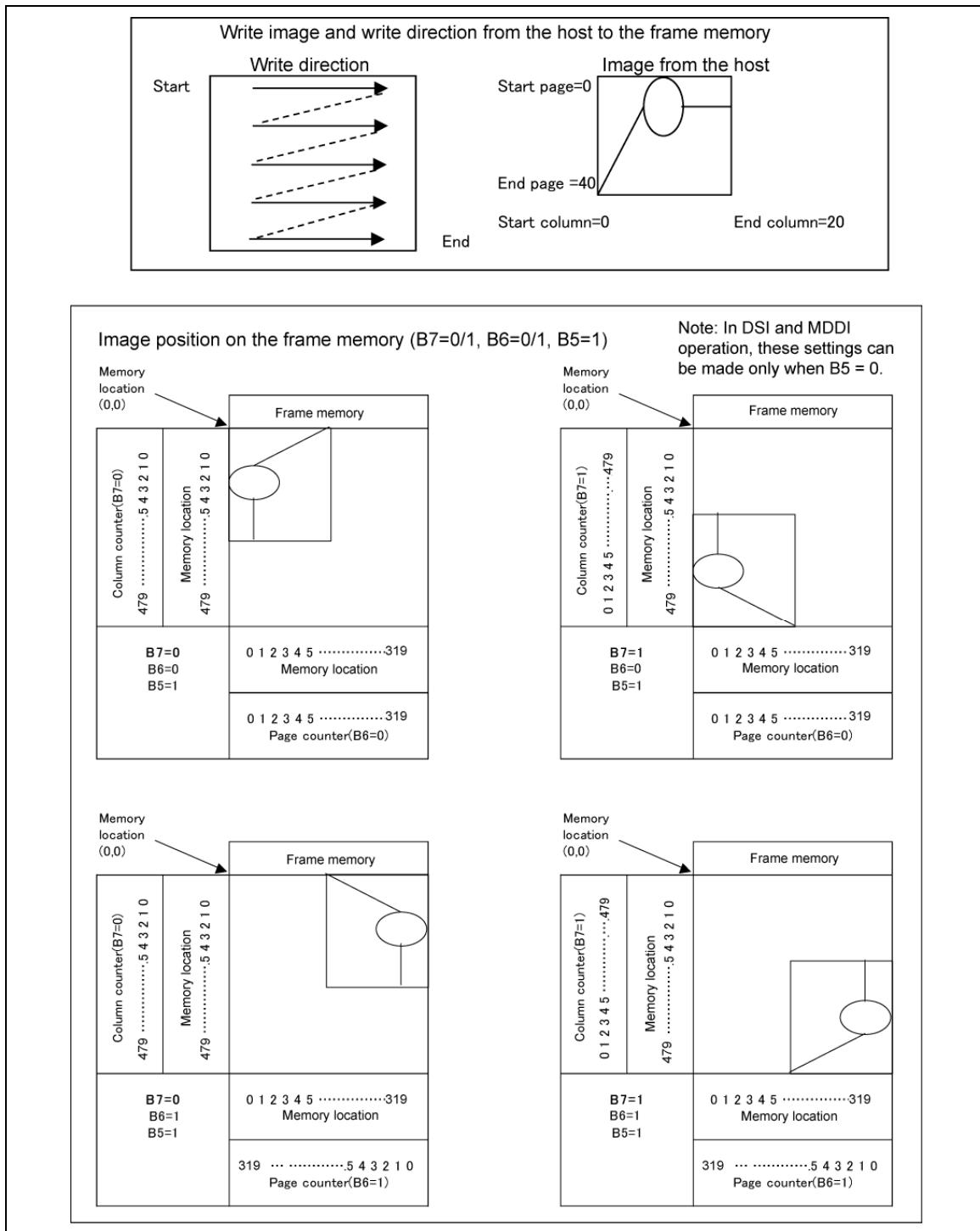


Figure 124

Internal Reference Clock Generating Function (TBD)

A figure below is a diagram of reference clock used in the R61529. A ‘reference clock (clk)’ is a minimum unit of a clock used for register setting. In MIPI DPI mode, a clock whose frequency is divided by PCLK input from system is chosen as a reference clock (clk). In other modes, a clock that divides frequency of the internal oscillation clock is chosen as a reference clock (clk).

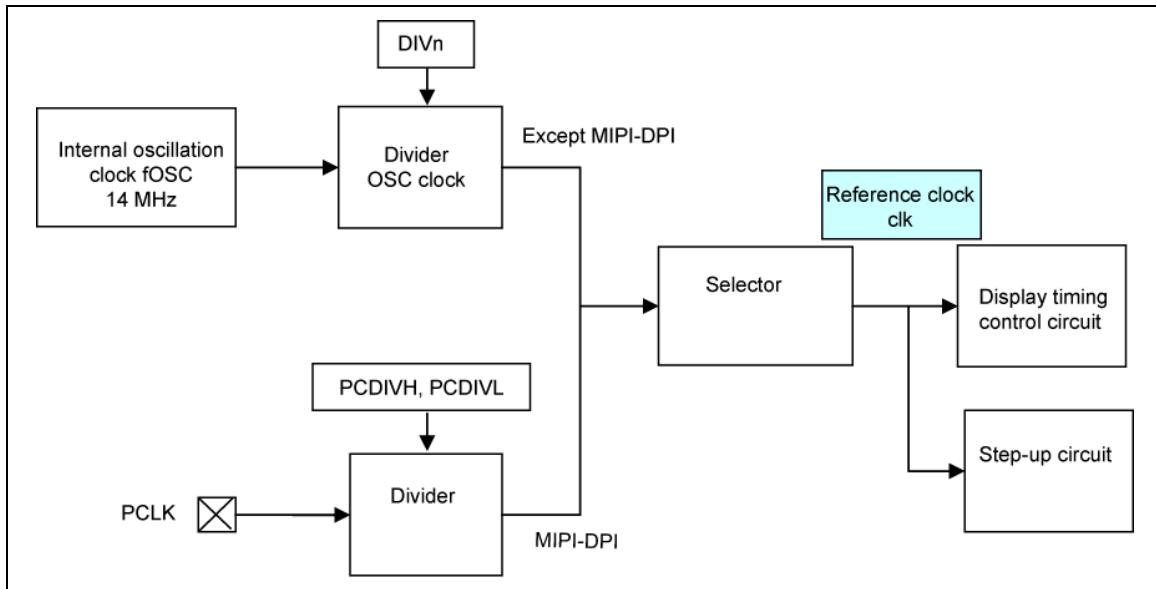
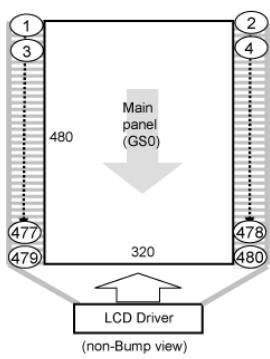
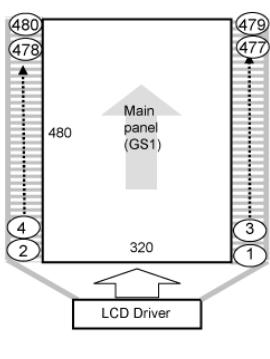
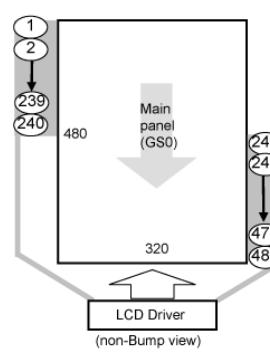
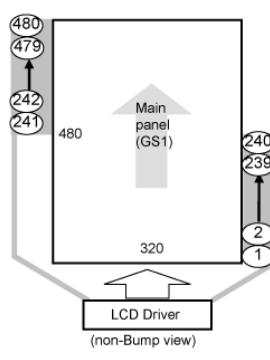


Figure 125 Diagram of Internal Reference Clock

Scan Mode Setting

The R61529 allows for changing the gate-line/gate driver assignment and the shift direction of gate line scan in the following 4 different ways by combination of SM and GS bit settings. These combinations allow various connections between the R61529 and the LCD panel.

SM	Scan direction	
	Left/right interchanging forward scan (GS = 0)	Left/right interchanging reverse scan (GS = 1)
0	 <p>Scan order G[1]→G[2]→G[3]→………→G[478]→G[479]→G[480]</p>	 <p>Scan order G[480]→G[479]→G[478]→………→G[3]→G[2]→G[1]</p>
1	 <p>Scan order G[1]→G[3]→……G[477]→G[479]→G[2]→G[4]→……G[478]→G[480]</p>	 <p>Scan order G[480]→G[478]→……→G[4]→G[2]→G[479]→G[477]→……G[3]→G[1]</p>

Note: The numbers in the circles in the figure show the order of scan.

Figure 126

Frame Frequency Adjustment Function

The R61529 supports a function to adjust frame frequency. The frame frequency for driving the LCD can be adjusted by setting Display Timing Setting (RTN bits) without changing the oscillation frequency.

It is possible to set a low frame frequency for saving power consumption when displaying a still picture and set a high frame frequency when displaying video image.

Relationship between the Liquid Crystal Drive Duty and the Frame Frequency

The relationship between the liquid crystal drive duty and the frame frequency is calculated from the following equation. The frame frequency can be changed by setting the number of clocks per 1 line period (RTN) of Display Timing Setting command.

Equation for calculating frame frequency

$$\text{FrameFrequency} = \frac{\text{osc}}{\text{Number of Clocks/line} \times (\text{NL} + \text{FP} + \text{BP})} [\text{Hz}]$$

fosc: Internal operation clock frequency (14MHz)

Number of clocks per line: RTN

Line: number of lines to drive the LCD: NL

Number of lines for front porch: FP

Number of lines for back porch: BP

Example of Calculation: when Maximum Frame Frequency = 60 Hz

OSC : fosc / 12 = 1.16Hz (DIV[3:0] = 4'h7 (an example of Divider setting: 1/12))

Number of lines: 480 lines

1H period: 39 clock cycles (RTN = 6'h27)

Front porch: 8 lines

Back porch: 8 lines

$$\therefore f_{FLM} = \frac{14\text{MHz}}{39\text{clocks} \times \frac{1}{12} \times (480 + 8 + 8)} \approx 60\text{Hz}$$

TE Pin Output Signal

Tearing Effect Line signal can be output from TE pin as frame memory data transfer synchronous signals. TE signal is trigger for frame memory write operation to enable data transfer in synchronization with the scanning operation. Tearing Effect Output signal is turned on/off by set_tear_off (34h) and set_tear_on (35h) commands.

Table 58

TEON (represents status of 35h command)	TELOM (35h1st parameter)	TE pin output
0	*	GND
1	0	TE (Mode1)
1	1	TE (Mode2)

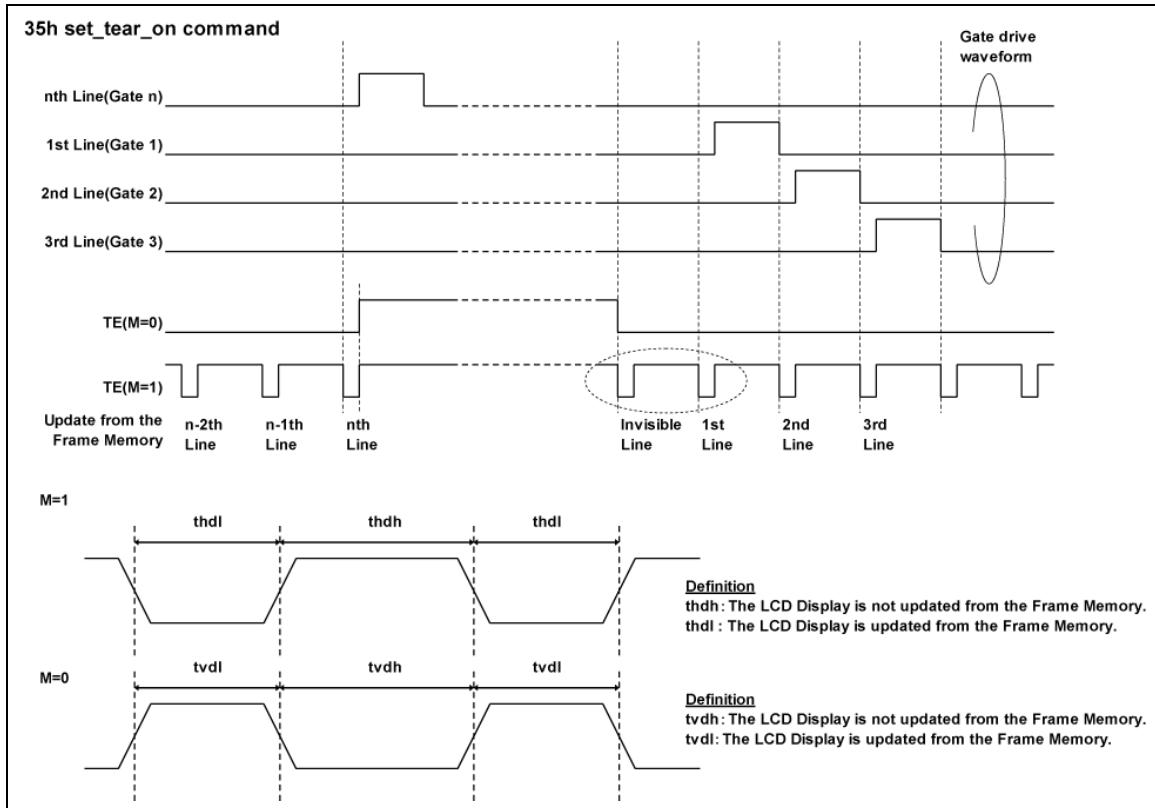


Figure 127

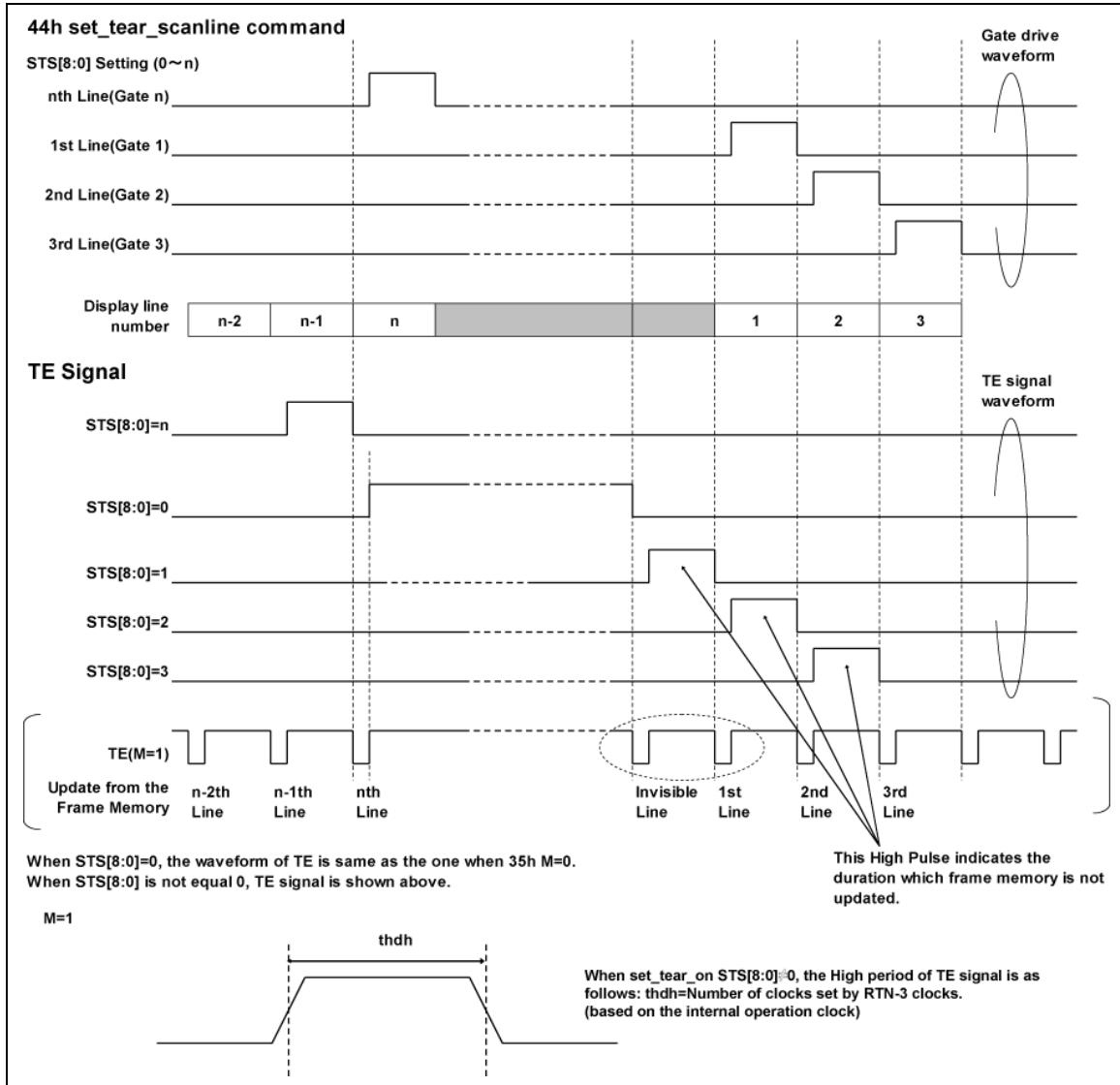


Figure 128

Self-Diagnostic Functions (TBD)

The R61529 supports the self-diagnostic functions. Set get_diagnostic_result (0Fh) 1st parameter's D6 bit according to the following flow chart.

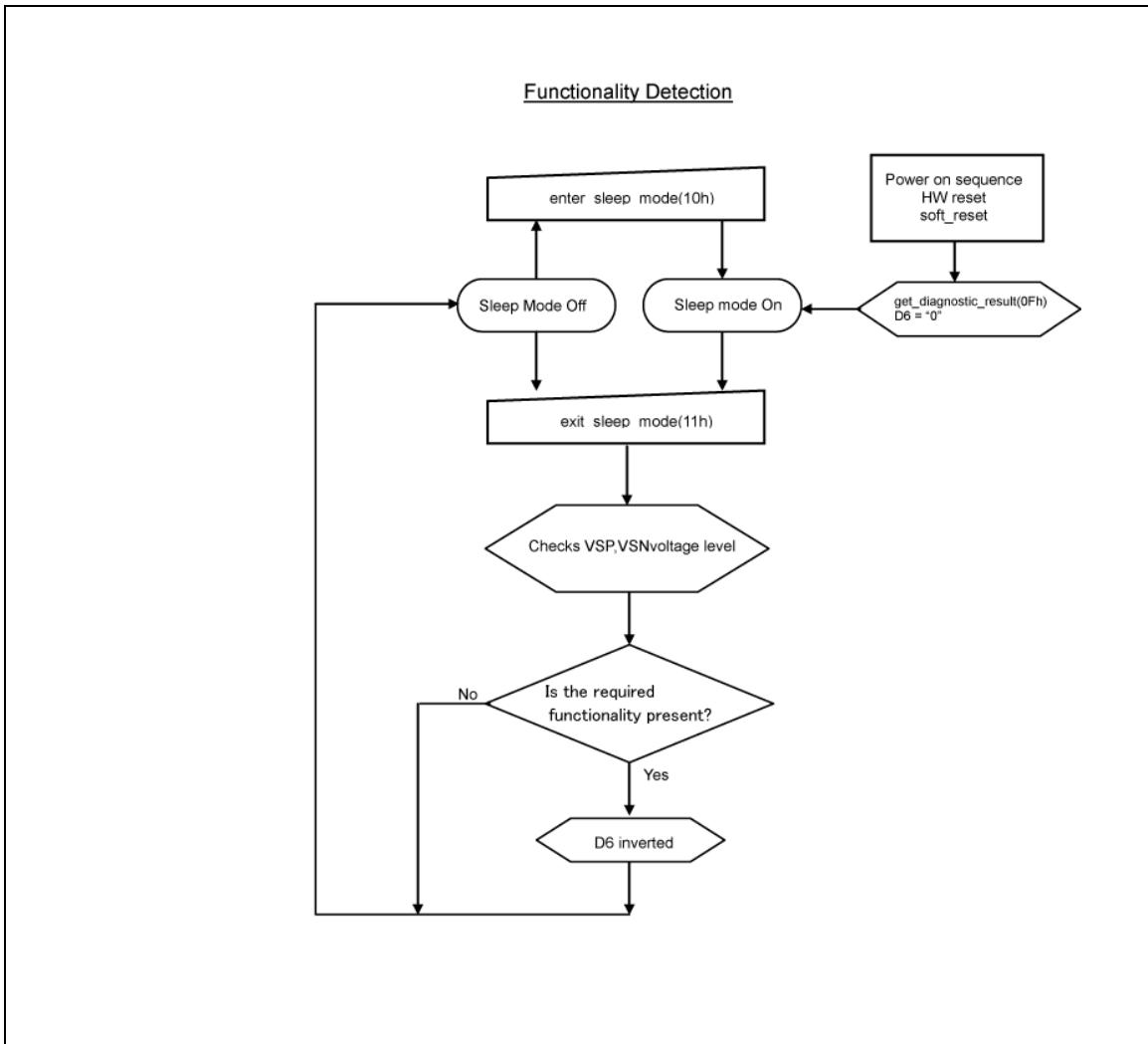


Figure 129 Functionality Detection

Dynamic Backlight Control Function (TBD)

The R61529 supports BLC (backlight control) function to control backlight brightness and process image dynamically. This function enables to reduce backlight power and minimize the effect of reduced power on the display image.

The display image is dynamically controlled by the BLC function. The availability of this function ranges from moving pictures such as TV image to still pictures such as menu. The histogram of display data is analyzed by BLC function, according to the brightness range of backlight set by parameters. The brightness of backlight and image processing coefficient are calculated so that image data is optimized. Backlight power is reduced without changing display image.

- Notes:
1. The BLC setting is enabled by BLCON bit setting (B8h).
 2. The effects of BLC function on power efficiency and display quality depend on image data and the setting. Check display quality on the panel.

- Control backlight dynamically according to the image histogram.
- PWM pin for LED backlight adjustment
- PWM signal control register set by the host processor. Backlight dimmer is adjusted by calculating internally-decided PWM value and maximum PWM value from the host processor.

System Configuration

1. The PWM signal is used to directly control the R61529 and LED driver IC. The LED driver IC is controlled entirely via the R61529.

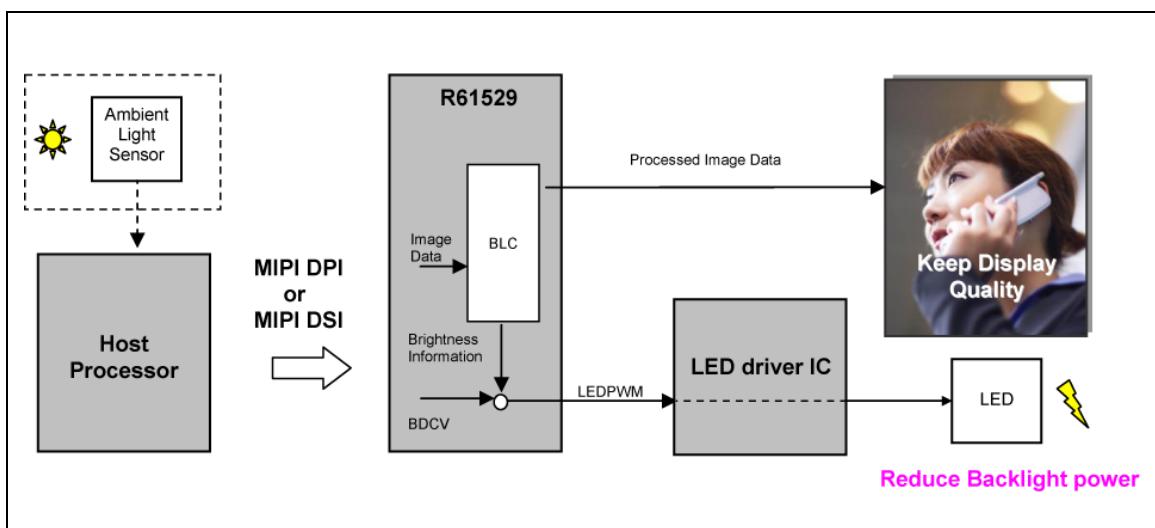


Figure 130

2. The host processor reads LED brightness information internally generated by BLC processing from the R61529 via MIPI DSI. Then, the LED driver IC is controlled from the host processor. There is the time difference between brightness adjustment by PWM and displaying data processed from the R61529. Check the effect on the image.

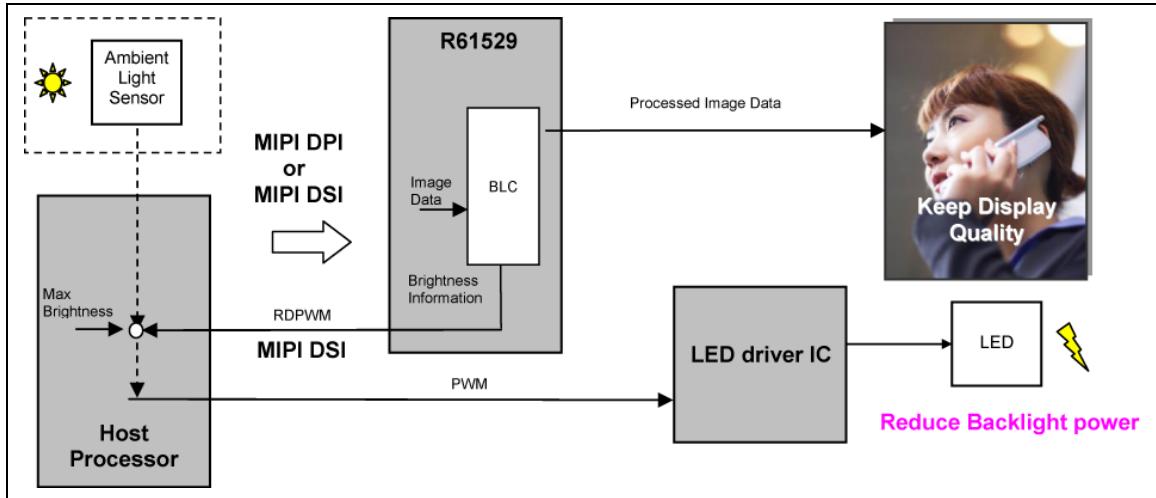


Figure 131

BLC Parameter Setting

The backlight control function has the following two functions:

- Image processing and backlight control processing
- Retain the grayscale of the display image that has turned white

These functions are set by the following registers:

- (1) BLC operating threshold (THREW)
- (2) Amount of change of threshold grayscale value per frame (PITCHW)
- (3) Difference between two grayscale values counted by the histogram counter (CGAPW)
- (4) Backlight brightness adjustment range (ULMTW and LLMTW)
- (5) Gamma conversion table (TBL_MIN and TBLx[7:0])
- (6) Interpolation to prevent display image from turning white (COEFK)

(1) THREWx[4:0]

This parameter sets the ratio (percentage) of the maximum number of pixels that makes display image white (= data 255) to the total of pixels by image processing. The ratio can be set from zero percent to sixty two percent in units of two percent. After this parameter sets the number of pixels that makes display image white, threshold grayscale value (Dth) that makes display image white is set so that the number of the pixels set by this parameter does not change.

To reduce the power by about 30 percent, set the above ratio to thirty percent (THREW = 5'h0F). When the value set by this parameter exceeds the range of Dth to be mentioned later, the priority is given to the range of threshold grayscale value (Dth).

According to the relationship between threshold grayscale value (Dth) and gamma conversion table (see (5)), the rate of backlight brightness reduction (= the rate of power reduction) and image correction factor are set.

- The larger THREW value tends to enhance the effect of reducing backlight power, and increases the image correction factor. In this case, the effect on display image increases (See note 1).
- The smaller THREW value tends to reduce the effect of reducing backlight power, and decreases the image correction factor. In this case, the effect on display image decreases (See note 1).

Notes: 1. The tendency for backlight power reduction and the effect on image by BLC function depend on image data. Check display quality on the panel.
2. The result of the histogram analysis is enabled from the next frame.

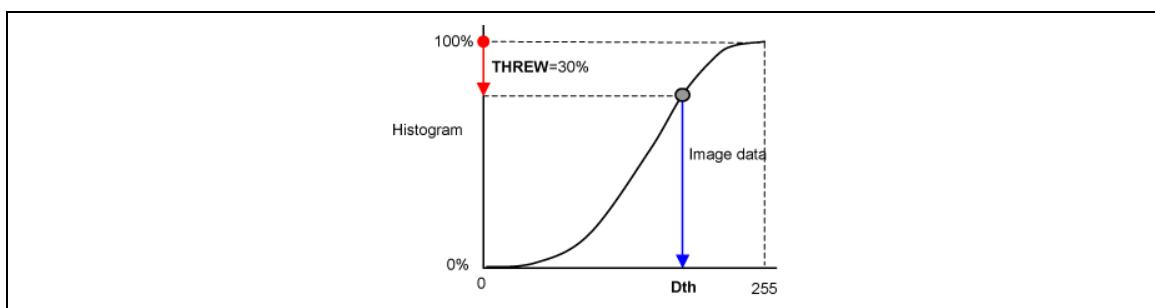
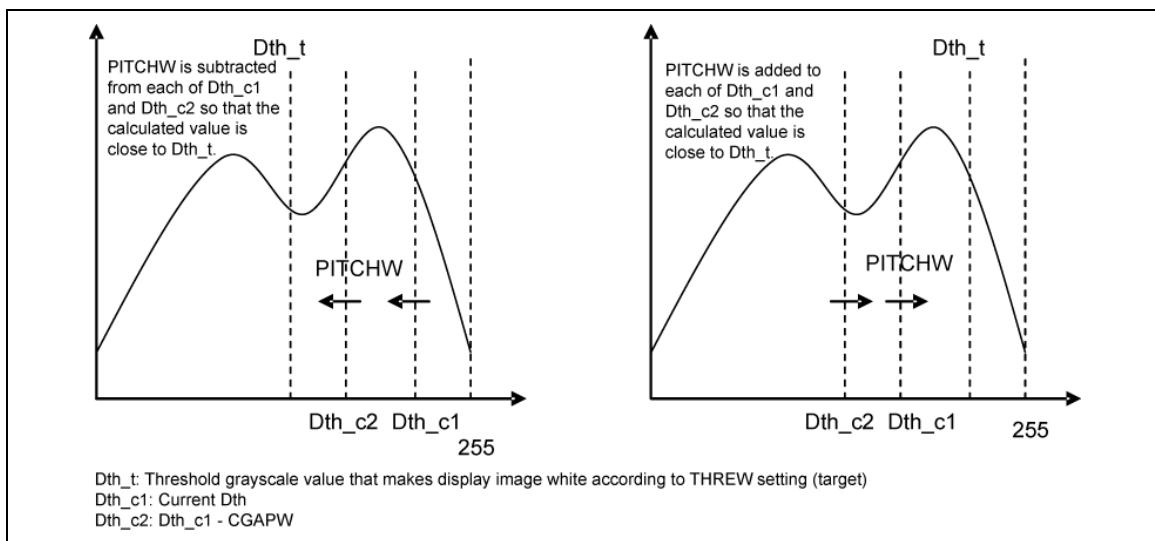


Figure 132

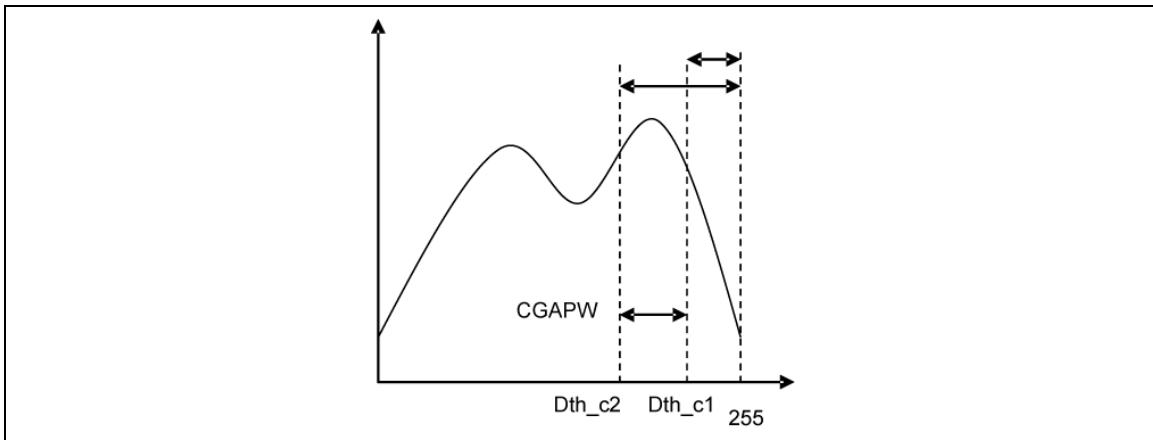
(2) PITCHWx[3:0]

This parameter sets the amount of change of threshold grayscale value (Dth) that makes display image white per frame in units of one half of the grayscale. When the target (Dth) is changed by the histogram change of input image including video image, this parameter can adjust the amount of changing threshold grayscale value (Dth). Therefore, this parameter is effective in reducing sharp change of backlight brightness. Make sure that CGAPWx[4:0] ≥ PITCHWx[3:0].



(3) CGAPWx[4:0]

The difference of the two grayscales (Dth_c1 and Dth_c2) counted by the present threshold counter is set in units of one eighth of the grayscale. This parameter is effective in slowing the change of threshold grayscale value (Dth). So, the speed of the change of Dth is adjusted to reduce subtle changes and flickers. Make sure that $CGAPWx[4:0] \geq PITCHWx[3:0]$.

**Figure 134**

(4) ULMTWx[7:0], LLMTWx[7:0]

The possible range of the threshold grayscale value (Dth) that makes display image white is set in units of 1 grayscale. ULMTW and LLMTW set the maximum grayscale and the minimum grayscale, respectively. Dth can be changed within the range set by ULMTW and LLMTW.

When there is no effect on saving power consumption due to a large number of pixels displaying white color, that is, in cases such as GUI, the R61529 can save power consumption by setting ULMTW lower than the maximum grayscale if saving power consumption precedes the display quality.

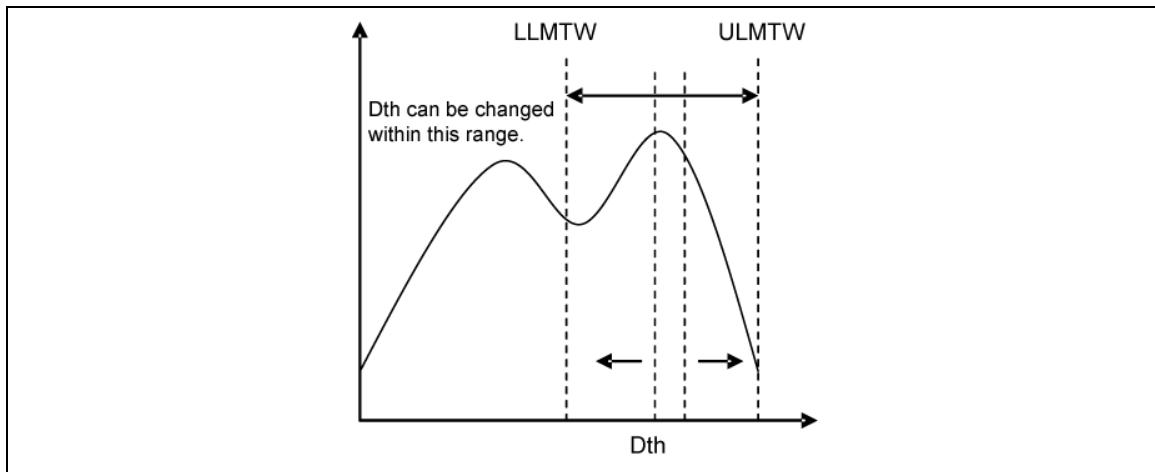
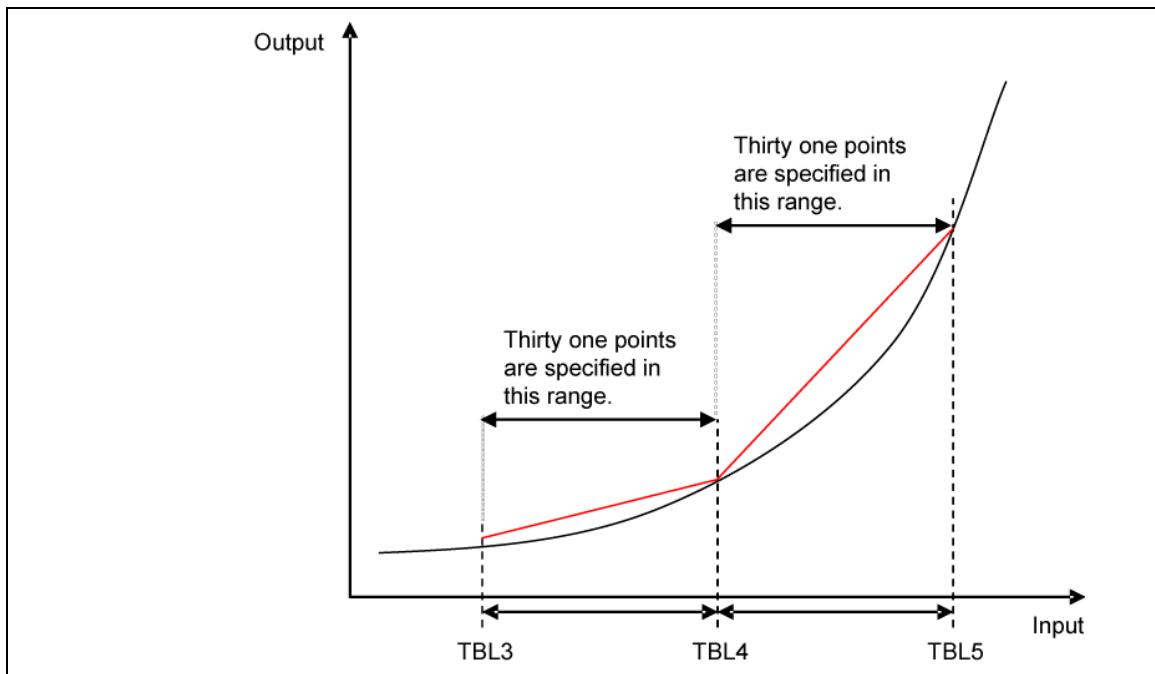


Figure 135

(5) TBL_*[7:0]

The reference values used for interpolation calculation in the gamma conversion table are set by 8-bit TBL_*[7:0]. Interpolation is performed as follows: First, four grayscale values are specified by TBL_*[7:0]. Then, the output data corresponding to the input data to thirty one grayscale values specified at even interval between the adjacent two grayscale values of the four grayscale values specified by TBL_*[7:0] is calculated by linear interpolation.

**Figure 136**

The table setting value is calculated by the following formula according to panel gamma value.

$$\text{Table setting value} = 255 \times (\text{table input grayscale} / 255)^{\gamma}$$

As the input table grayscale, the above calculation formula is applied to grayscales 127, 159, 191, 223, and 255 to calculate the table values. The values are set as TBL*. The following table is applied to the case that gamma is set to 2.2.

Table 59

Register	TBL3	TBL4	TBL5	TBL6	TBL7
Table input grayscale	127	159	191	223	255
Table setting value	55	90	135	190	255

(6) COEFKx[4:0]

This register sets the range of the grayscale that prevents display image from turning white, according to the ratio of the grayscale to the grayscale number that makes data white. The ratio can be set from 0 percent to 100 percent. The first grayscale (S) that starts grayscale interpolation to prevent display image from turning white is calculated by this register and Dth. Then, the number of grayscales between this grayscale (S) and the maximum grayscale is calculated by interpolation function, and it is used as image processing pixel value.

The larger COEFK[4:0] setting value increases the number of grayscales available for interpolation and relatively decreases the contrast between interpolation sections. As a result, the gamma value changes and the brightness decreases. Also, the color of the section changes. In the interpolation factor, there is a trade-off between contrast between interpolation section and the interpolation that the gamma value changes.

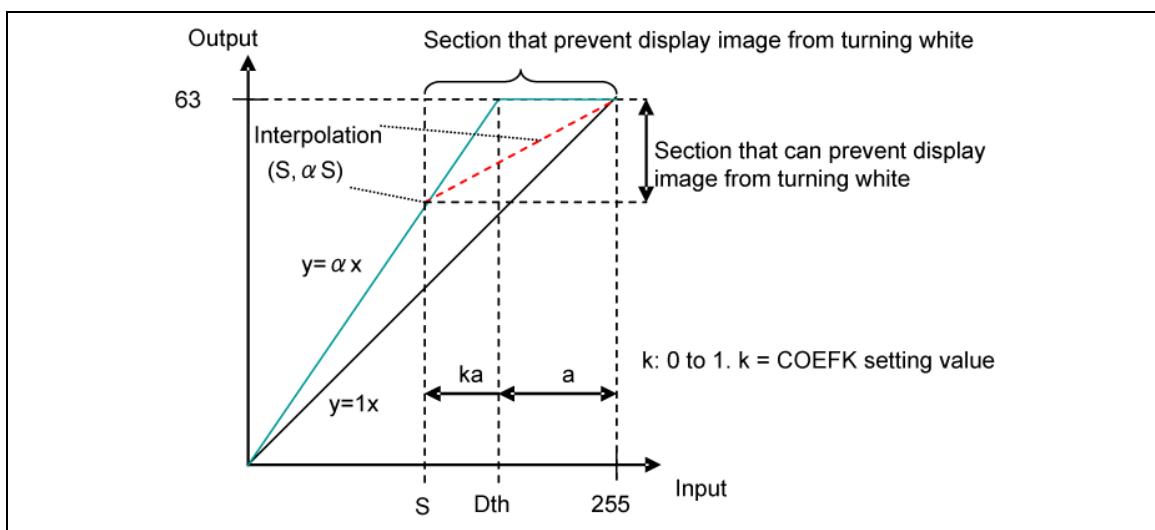


Figure 137

PWM Signal Setting

The PWM signal is output from the LEDPWM pin according to BDCV[7:0] bit settings and brightness information (8 bits) output from BLC control circuit.

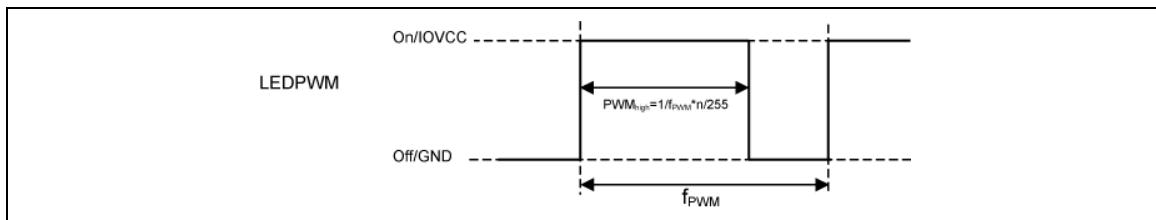


Figure 138 PWM output

Setting below is applied to interfaces except MIPI DPI.

Table 60

PWMDIV[7:0]	LEDPWM frequency	PWMDIV[7:0]	LEDPWM frequency
8'h00	54.9KHz	8'h10-8'h1E	Setting inhibited
8'h01	27.4KHz	8'h1F	1.72KHz
8'h02	18.3KHz	8'h20-8'h3E	Setting inhibited
8'h03	13.7KHz	8'h3F	0.86KHz
8'h04-8'h06	Setting inhibited	8'h40-8'h7E	Setting inhibited
8'h07	6.86KHz	8'h7F	0.43KHz
8'h08-8'h0E	Setting inhibited	8'h80-8'hFE	Setting inhibited
8'h0F	3.43KHz	8'hFF	0.21KHz

Note: The values in the table above show the typical. There shall be variance of maximum +/-5% in the actual operation.

Table 61

Dimming data	Duty _{PWM}
8'h00	0(fixed Low)
8'h01	1/255
8'h02	2/255
8'h03	3/255
:	:
:	:
8'h0D	253/255
8'h0E	254/255
8'hFF	1(fixed High)

State Transition Diagram (Display Mode)

Definition of Display Modes

The state transition of the R61529 (display modes) compliant with MIPI DCS is as follows:

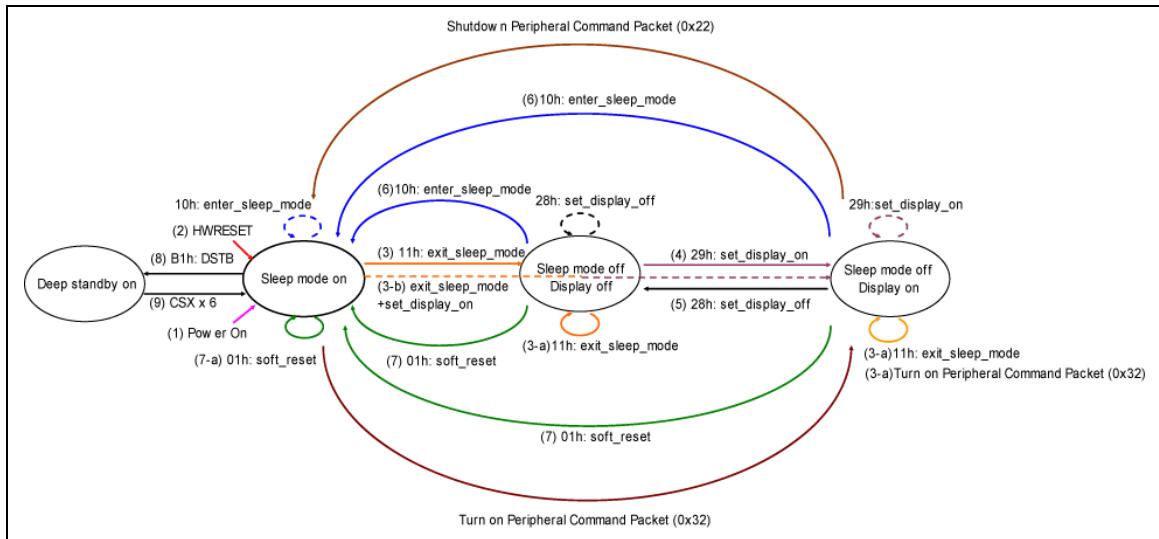


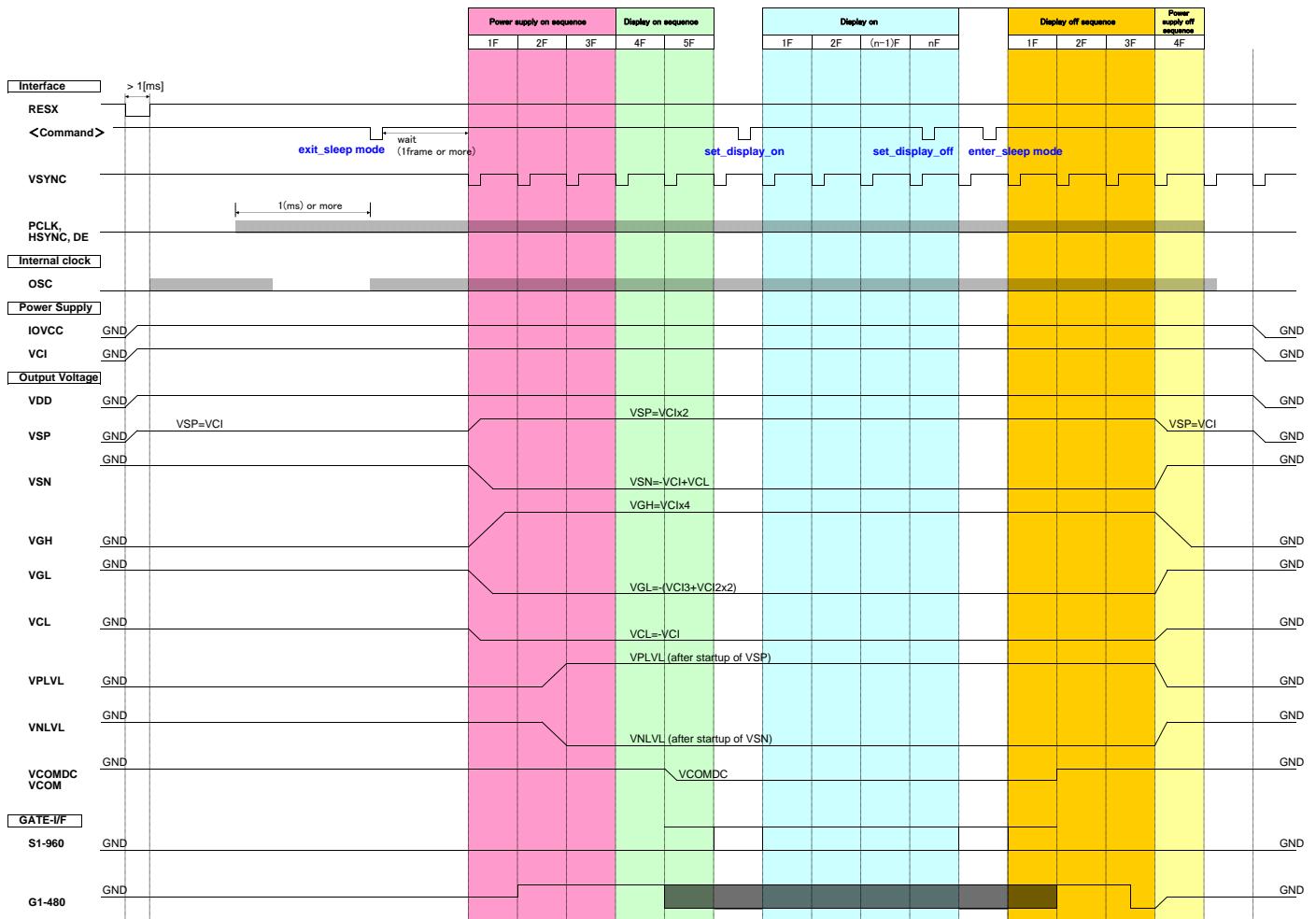
Figure 139

Table 62 Operation Mode Transition Sequence

Sequence	Command	State	
		From	To
(1)	Power On sequence	-	- Sleep mode on
(2)	HWRESET sequence	-	- Sleep mode on
(3)	exit_sleep_mode sequence	11h:exit_sleep_mode	Sleep mode on Sleep out Display off
			Sleep mode off Sleep mode off Display off/on Display off/on
(3-a)	exit_sleep_mode + display_on sequence	11h:exit_sleep_mode	Sleep mode on Sleep mode off Display on
(3-b)	set_display_on sequence	29h:set_display_on	Sleep mode off Sleep mode off Display off Display on
(4)	set_display_off sequence	28h:set_display_off	Sleep mode off Sleep mode off Display on Display off
(5)	enter_sleep_mode sequence	10h:enter_sleep_mode	Sleep mode off Sleep mode on Display off/on
(7)	soft_reset sequence	01h:soft_reset	Sleep out Sleep mode on Display off/on
			Sleep mode on Sleep mode on
(8)	Deep standby mode sequence	Manufacturer Command B1h: Deep standby mode	Sleep mode on -
(9)	Exit_Deep standby mode_sequence	CSX x6, HWRESET-	- Sleep mode on

■ Power On/Off Sequence

- *1 The state transition (display mode) of the R61529 complies with MIPI DCS.
- *2 Input Sync Event, Vsync Start (Data Type 01h), Sync Event, H Sync Start (Data Type 21h) in MIPI DSI operation. Input DSI clock according to PCLK input timing in this figure.
- *3 Start inputting DE, PCLK, VSYNC, and HSYNC clocks at least 1ms before inputting exit_sleep_mode command (11h).
- *4 Data written in MIPI DPI, MIPI DSI Video Mode and MDDI Active Refresh Mode is directly output as display data without being written to internal RAM. At this time, the power supply on/off sequence is executed by PCLK. Start inputting clock at least 1ms before inputting exit_sleep_mode command (11h). Also, continue to input the clocks until an end of the power supply off sequence after inputting exit_sleep_mode command (11h).
- Data written in modes except MIPI DPI, MIPI DSI Video Mode and MDDI Active Refresh Mode is not directly output as display data without being written to internal RAM. At this time, the power supply on/off sequence is executed by the internal OSC clock.



Power/Display On/Off Sequence

The power/display on/off sequence is shown below.

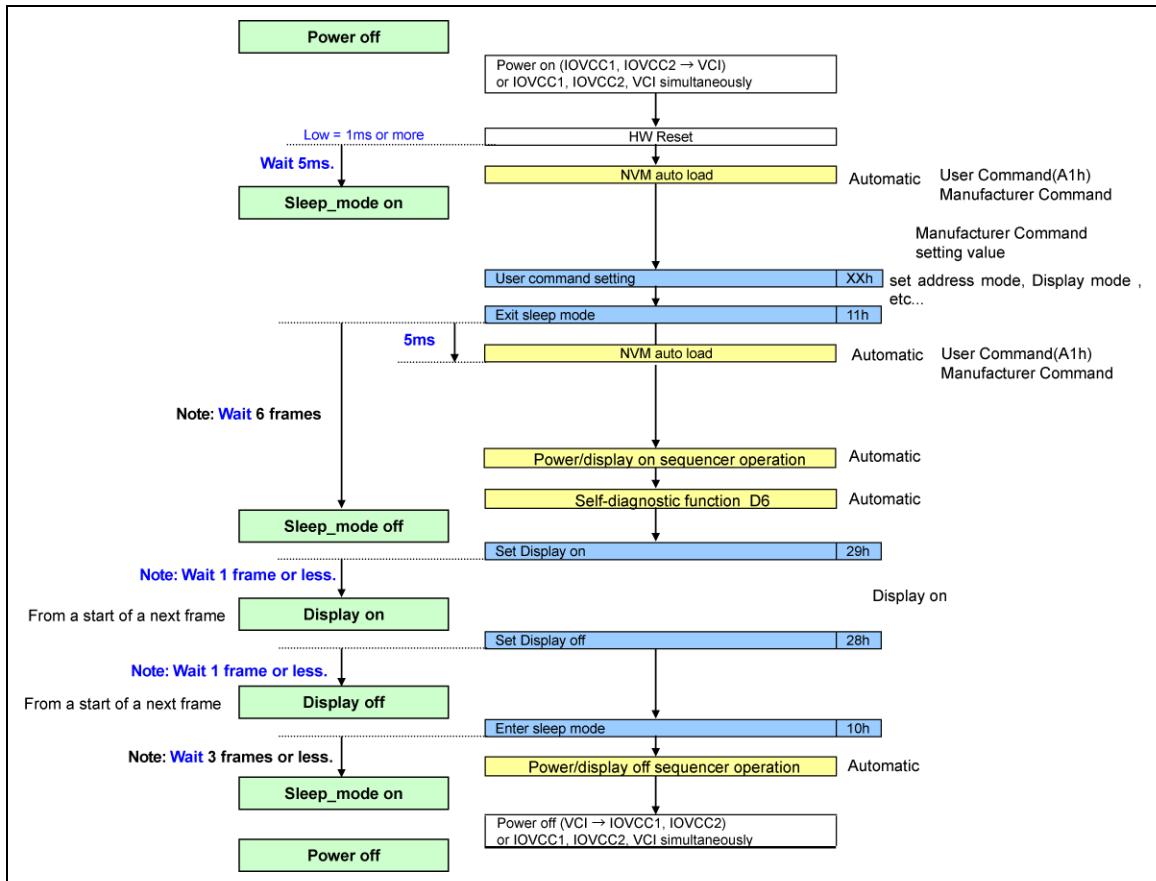


Figure 140

Note: Calculation example of wait time

$1/60\text{Hz} = 16.6\text{ms}$ when the driver is used at frame frequency of 60Hz.

- (1) If display operation is synchronized with an internal oscillation clock, one frame period depends on user setting of DIV[3:0], RTN[3:0], FP[7:0], BP[7:0], and NL[8:1]. If display operation is synchronized with VSYNC interface or MIPI, one frame period is a VSYNC cycle.
- (2) If display operation is synchronized with an internal oscillation clock, exit sleep mode is executed after issue of command. If display operation is synchronized with VSYNC interface or MIPI, exit sleep mode is not executed until next input of VSYNC.
- (3) If display operation is synchronized with an internal oscillation clock, enter sleep mode is not executed until next input of internal frame signal after command is issued. Enter sleep mode is executed in synchronization with an internal frame signal. If display operation is synchronized with VSYNC interface or MIPI, enter sleep mode is not executed until next input of VSYNC.

Secure the above wait time.

Power/Display On/Off Sequence when using MDDI

The power/display on sequence when using MDDI is shown below.

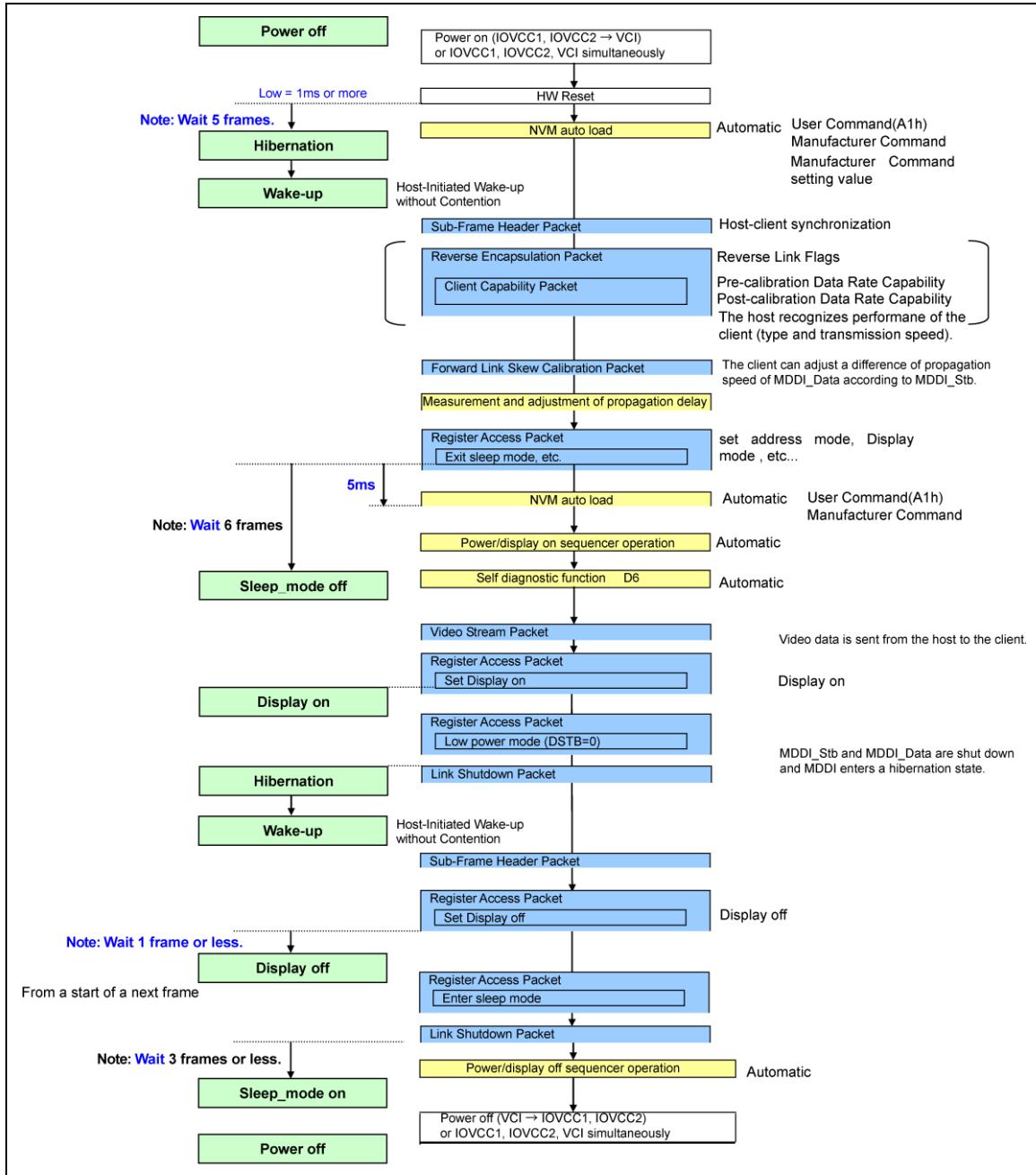


Figure 141

Note: Calculation example of wait time

$1/60\text{Hz} = 16.6\text{ms}$ when the driver is used at frame frequency of 60Hz.

- (1) If display operation is synchronized with an internal oscillation clock, one frame period depends on user setting of DIV[3:0], RTN[3:0], FP[7:0], BP[7:0], and NL[8:1]. If display operation is synchronized with VSYNC interface or MIPI, one frame period is a VSYNC cycle.
- (2) If display operation is synchronized with an internal oscillation clock, exit sleep mode is executed after issue of command. If display operation is synchronized with VSYNC interface or MIPI, exit sleep mode is not executed until next input of VSYNC.
- (3) If display operation is synchronized with an internal oscillation clock, enter sleep mode is not executed until next input of internal frame signal after command is issued. Enter sleep mode is executed in synchronization with an internal frame signal. If display operation is synchronized with VSYNC interface or MIPI, enter sleep mode is not executed until next input of VSYNC.

Secure the above wait time.

Gamma Correction Function

The R61529 supports γ -correction function to make the optimal colors according to the characteristics of the panel. The R61529 has registers for positive and negative polarities (Gamma Setting A Set, Gamma Setting B Set, and Gamma Setting C Set) to allow different settings for R, G, and B dots.

γ Correction Circuit

The following figure shows a gamma correction circuit. Two ends of the 168-step ladder resistors for positive grayscale are connected to VPLVL and VGS. Those for negative grayscale are connected to VGS (GND) and VNLVL.

V0P/N, V4P/N, V8P/N, V15P/N, V31P/N, V79P/N, V176P/N, V224P/N, V240P/N, V247P/N, V251P/N, and V255P/N are grayscale reference levels. The reference levels can be adjusted by register. Voltage between VPLVL and VGS (GND), and voltage between VGS (GND) and VNLVL is divided by ladder resistors. The divided voltage is selected by selectors, and then, grayscale reference levels are output. For other grayscale levels, see “Grayscale Voltage Calculation Formula.”

The R61529 incorporates RGB separate gamma correction function. There are three circuits of R, G and B in parallel behind selectors.

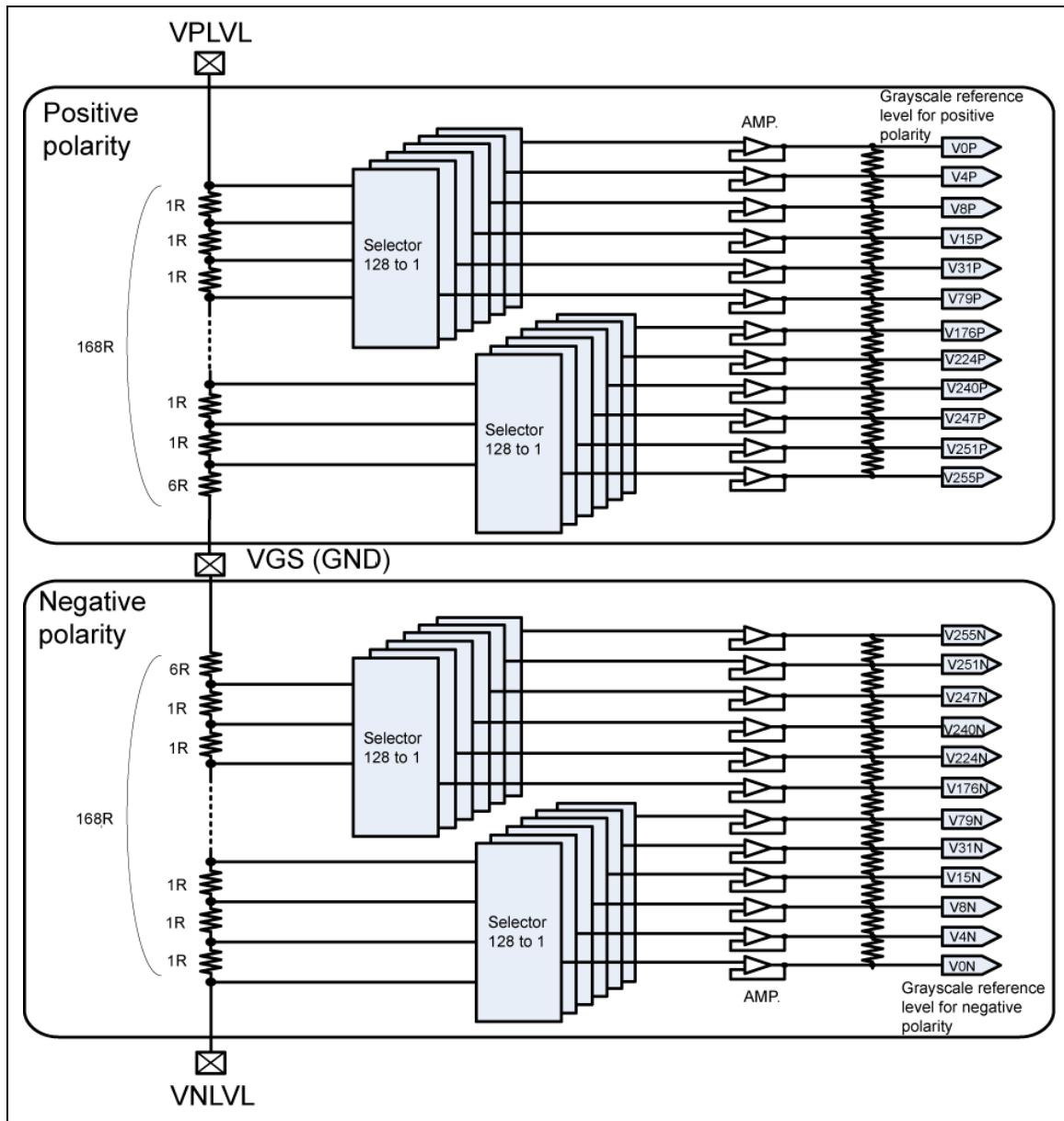


Figure 142

γ Correction Register

The following table shows the γ -correction register and grayscale reference level. Each reference level is set by a 7-bit gamma correction register that generates a grayscale reference level. Each of the gamma correction registers for positive polarity and negative polarity consists of twelve 7-bit registers (total: 84 bits).

Table 63

Grayscale reference level	γ correction register	
	Positive polarity	Negative polarity
V0	GSELxP0[6:0]	GSELxN0[6:0]
V4	GSELxP1[6:0]	GSELxN1[6:0]
V8	GSELxP2[6:0]	GSELxN2[6:0]
V15	GSELxP3[6:0]	GSELxN3[6:0]
V31	GSELxP4[6:0]	GSELxN4[6:0]
V79	GSELxP5[6:0]	GSELxN5[6:0]
V176	GSELxP6[6:0]	GSELxN6[6:0]
V224	GSELxP7[6:0]	GSELxN7[6:0]
V240	GSELxP8[6:0]	GSELxN8[6:0]
V247	GSELxP9[6:0]	GSELxN9[6:0]
V251	GSELxP10[6:0]	GSELxN10[6:0]
V255	GSELxP11[6:0]	GSELxN11[6:0]

Note: 'X' in register name indicates 'A' of "Gamma Setting A Set", 'B' of "Gamma Setting B Set," or 'C' of "Gamma Setting C Set."

Relationship between Gamma Correction Register and Voltage (Reference Level Select Table)

Tables below shows relationships between values set in gamma correction registers and voltage.

Table 64

Register	Value	Voltage
GSELxP0[6:0]	7'h00	$\Delta V \times (1-0/168)$
GSELxP1[6:0]	7'h01	$\Delta V \times (1-1/168)$
GSELxP2[6:0]	7'h02	$\Delta V \times (1-2/168)$
GSELxP3[6:0]	7'h03	$\Delta V \times (1-3/168)$
GSELxP4[6:0]	7'h04	$\Delta V \times (1-4/168)$
GSELxP5[6:0]	7'h05	$\Delta V \times (1-5/168)$
	:	:
	:	:
GSELxN0[6:0]	7'h7A	$\Delta V \times (1-122/168)$
GSELxN1[6:0]	7'h7B	$\Delta V \times (1-123/168)$
GSELxN2[6:0]	7'h7C	$\Delta V \times (1-124/168)$
GSELxN3[6:0]	7'h7D	$\Delta V \times (1-125/168)$
GSELxN4[6:0]	7'h7E	$\Delta V \times (1-126/168)$
GSELxN5[6:0]	7'h7F	$\Delta V \times (1-127/168)$

Note: 'ΔV' indicates VPLVL-VGS (positive polarity) or VGS-VNLVL (negative polarity).

Table 65

Register	Value	Voltage
GSELxP6[6:0]	7'h00	$\Delta V \times (0+6/168)$
GSELxP7[6:0]	7'h01	$\Delta V \times (1+6/168)$
GSELxP8[6:0]	7'h02	$\Delta V \times (2+6/168)$
GSELxP9[6:0]	7'h03	$\Delta V \times (3+6/168)$
GSELxP10[6:0]	7'h04	$\Delta V \times (4+6/168)$
GSELxP11[6:0]	7'h05	$\Delta V \times (5+6/168)$
	:	:
	:	:
GSELxN6[6:0]	7'h7A	$\Delta V \times (122+6/168)$
GSELxN7[6:0]	7'h7B	$\Delta V \times (123+6/168)$
GSELxN8[6:0]	7'h7C	$\Delta V \times (124+6/168)$
GSELxN9[6:0]	7'h7D	$\Delta V \times (125+6/168)$
GSELxN10[6:0]	7'h7E	$\Delta V \times (126+6/168)$
GSELxN11[6:0]	7'h7F	$\Delta V \times (127+6/168)$

Note: 'ΔV' indicates VPLVL-VGS (positive polarity) or VGS-VNLVL (negative polarity).

Grayscale Voltage Calculation Formula

Table 66

Grayscale voltage	Formula	Grayscale voltage	Formula
V0	See reference level select tables.	V33	(V31*2+V35*2)/4
V1	(V0-V4)*18/26+V4	V34	(V31+V35*3)/4
V2	(V0-V4)*11/26+V4	V35	(V31-V79)*24/27+V79
V3	(V0-V4)*5/26+V4	V36	(V35*3+V39)/4
V4	See reference level select tables.	V37	(V35*2+V39*2)/4
V5	(V4-V8)*10/14+V8	V38	(V35+V39*3)/4
V6	(V4-V8)*6/14+V8	V39	(V31-V79)*21/27+V79
V7	(V4-V8)*3/14+V8	V40	(V39*3+V43)/4
V8	See reference level select tables.	V41	(V39*2+V43*2)/4
V9	(V8-V15)*13/16+V15	V42	(V39+V43*3)/4
V10	(V8-V15)*10/16+V15	V43	(V31-V79)*18/27+V79
V11	(V8-V15)*8/16+V15	V44	(V43*3+V47)/4
V12	(V8-V15)*6/16+V15	V45	(V43*2+V47*2)/4
V13	(V8-V15)*4/16+V15	V46	(V43+V47*3)/4
V14	(V8-V15)*2/16+V15	V47	(V31-V79)*15.5/27+V79
V15	See reference level select tables.	V48	(V47*3+V51)/4
V16	(V15*3+V19)/4	V49	(V47*2+V51*2)/4
V17	(V15*2+V19*2)/4	V50	(V47+V51*3)/4
V18	(V15+V19*3)/4	V51	(V31-V79)*13/27+V79
V19	(V15-V31)*12/17+V31	V52	(V51*3+V55)/4
V20	(V19*3+V23)/4	V53	(V51*2+V55*2)/4
V21	(V19*2+V23*2)/4	V54	(V51+V55*3)/4
V22	(V19+V23*3)/4	V55	(V31-V79)*10.5/27+V79
V23	(V15-V31)*7/17+V31	V56	(V55*3+V59)/4
V24	(V23*3+V27)/4	V57	(V55*2+V59*2)/4
V25	(V23*2+V27*2)/4	V58	(V55+V59*3)/4
V26	(V23+V27*3)/4	V59	(V31-V79)*8.5/27+V79
V27	(V15-V31)*3/17+V31	V60	(V59*3+V63)/4
V28	(V27*3+V31)/4	V61	(V59*2+V63*2)/4
V29	(V27*2+V31*2)/4	V62	(V59+V63*3)/4
V30	(V27+V31*3)/4	V63	(V31-V79)*6.5/27+V79
V31	See reference level select tables.	V64	(V63*3+V67)/4
V32	(V31*3+V35)/4	V65	(V63*2+V67*2)/4

Grayscale voltage	Formula	Grayscale voltage	Formula
V66	(V63+V67*3)/4	V99	(V79-V176)*19.25/24.25+V176
V67	(V31-V79)*4.5/27+V79	V100	(V99*3+V103)/4
V68	(V67*3+V71)/4	V101	(V99*2+V103*2)/4
V69	(V67*2+V71*2)/4	V102	(V99+V103*3)/4
V70	(V67+V71*3)/4	V103	(V79-V176)*18.25/24.25+V176
V71	(V31-V79)*3/27+V79	V104	(V103*3+V107)/4
V72	(V71*3+V75)/4	V105	(V103*2+V107*2)/4
V73	(V71*2+V75*2)/4	V106	(V103+V107*3)/4
V74	(V71+V75*3)/4	V107	(V79-V176)*17.25/24.25+V176
V75	(V31-V79)*1.5/27+V79	V108	(V107*3+V111)/4
V76	(V75*3+V79)/4	V109	(V107*2+V111*2)/4
V77	(V75*2+V79*2)/4	V110	(V107+V111*3)/4
V78	(V75+V79*3)/4	V111	(V79-V176)*16.25/24.25+V176
V79	See reference level select tables.	V112	(V111*3+V115)/4
V80	(V79*3+V83)/4	V113	(V111*2+V115*2)/4
V81	(V79*2+V83*2)/4	V114	(V111+V115*3)/4
V82	(V79+V83*3)/4	V115	(V79-V176)*15.25/24.25+V176
V83	(V79-V176)*23.25/24.25+V176	V116	(V115*3+V119)/4
V84	(V83*3+V87)/4	V117	(V115*2+V119*2)/4
V85	(V83*2+V87*2)/4	V118	(V115+V119*3)/4
V86	(V83+V87*3)/4	V119	(V79-V176)*14.25/24.25+V176
V87	(V79-V176)*22.25/24.25+V176	V120	(V119*3+V123)/4
V88	(V87*3+V91)/4	V121	(V119*2+V123*2)/4
V89	(V87*2+V91*2)/4	V122	(V119+V123*3)/4
V90	(V87+V91*3)/4	V123	(V79-V176)*13.25/24.25+V176
V91	(V79-V176)*21.25/24.25+V176	V124	(V123*3+V127)/4
V92	(V91*3+V95)/4	V125	(V123*2+V127*2)/4
V93	(V91*2+V95*2)/4	V126	(V123+V127*3)/4
V94	(V91+V95*3)/4	V127	(V79-V176)*12.25/24.25+V176
V95	(V79-V176)*20.25/24.25+V176	V128	(V79-176)*12/24.25+V176
V96	(V95*3+V99)/4	V129	(V128*3+V132)/4
V97	(V95*2+V99*2)/4	V130	(V128*2+V132*2)/4
V98	(V95+V99*3)/4	V131	(V128+V132*3)/4

Grayscale voltage	Formula	Grayscale voltage	Formula
V132	(V79-176)*11/24.25+V176	V165	(V164*3+V168)/4
V133	(V132*3+V136)/4	V166	(V164*2+V168*2)/4
V134	(V132*2+V136*2)/4	V167	(V164+V168*3)/4
V135	(V132+V136*3)/4	V168	(V79-176)*2/24.25+V176
V136	(V79-176)*10/24.25+V176	V169	(V168*3+V172)/4
V137	(V136*3+V140)/4	V170	(V168*2+V172*2)/4
V138	(V136*2+V140*2)/4	V171	(V168+V172*3)/4
V139	(V136+V140*3)/4	V172	(V79-176)*1/24.25+V176
V140	(V79-176)*9/24.25+V176	V173	(V172*3+V176)/4
V141	(V140*3+V144)/4	V174	(V172*2+V176*2)/4
V142	(V140*2+V144*2)/4	V175	(V172+V176*3)/4
V143	(V140+V144*3)/4	V176	See reference level select tables.
V144	(V79-176)*8/24.25+V176	V177	(V176*3+V180)/4
V145	(V144*3+V148)/4	V178	(V176*2+V180*2)/4
V146	(V144*2+V148*2)/4	V179	(V176+V180*3)/4
V147	(V144+V148*3)/4	V180	(V176-V224)*25.5/27+V224
V148	(V79-176)*7/24.25+V176	V181	(V180*3+V184)/4
V149	(V148*3+V152)/4	V182	(V180*2+V184*2)/4
V150	(V148*2+V152*2)/4	V183	(V180+V184*3)/4
V151	(V148+V152*3)/4	V184	(V176-V224)*24/27+V224
V152	(V79-176)*6/24.25+V176	V185	(V184*3+V188)/4
V153	(V152*3+V156)/4	V186	(V184*2+V188*2)/4
V154	(V152*2+V156*2)/4	V187	(V184+V188*3)/4
V155	(V152+V156*3)/4	V188	(V176-V224)*22.5/27+V224
V156	(V79-176)*5/24.25+V176	V189	(V188*3+V192)/4
V157	(V156*3+V160)/4	V190	(V188*2+V192*2)/4
V158	(V156*2+V160*2)/4	V191	(V188+V192*3)/4
V159	(V156+V160*3)/4	V192	(V176-V224)*20.5/27+V224
V160	(V79-176)*4/24.25+V176	V193	(V192*3+V196)/4
V161	(V160*3+V164)/4	V194	(V192*2+V196*2)/4
V162	(V160*2+V164*2)/4	V195	(V192+V196*3)/4
V163	(V160+V164*3)/4	V196	(V176-V224)*18.5/27+V224
V164	(V79-176)*3/24.25+V176	V197	(V197*3+V200)/4

Table 67

Grayscale voltage	Formula	Grayscale voltage	Formula
V198	$(V197*2+V200*2)/4$	V231	$(V228+V232*3)/4$
V199	$(V197+V200*3)/4$	V232	$(V224-V240)*10/17+V240$
V200	$(V176-V224)*16.5/27+V224$	V233	$(V232*3+V236)/4$
V201	$(V200*3+V204)/4$	V234	$(V232*2+V236*2)/4$
V202	$(V200*2+V204*2)/4$	V235	$(V232+V236*3)/4$
V203	$(V200+V204*3)/4$	V236	$(V224-V240)*5/17+V240$
V204	$(V176-V224)*14/27+V224$	V237	$(V236*3+V240)/4$
V205	$(V204*3+V208)/4$	V238	$(V236*2+V240*2)/4$
V206	$(V204*2+V208*2)/4$	V239	$(V236+V240*3)/4$
V207	$(V204+V208*3)/4$	V240	See reference level select tables.
V208	$(V176-V224)*11.5/27+V224$	V241	$(V240-V247)*14/16+V247$
V209	$(V208*3+V212)/4$	V242	$(V240-V247)*12/16+V247$
V210	$(V208*2+V212*2)/4$	V243	$(V240-V247)*10/16+V247$
V211	$(V208+V212*3)/4$	V244	$(V240-V247)*8/16+V247$
V212	$(V176-V224)*9/27+V224$	V245	$(V240-V247)*6/16+V247$
V213	$(V212*3+V216)/4$	V246	$(V240-V247)*3/16+V247$
V214	$(V212*2+V216*2)/4$	V247	See reference level select tables.
V215	$(V212+V216*3)/4$	V248	$(V247-V251)*11/14+V251$
V216	$(V176-V224)*6/27+V224$	V249	$(V247-V251)*8/14+V251$
V217	$(V216*3+V220)/4$	V250	$(V247-V251)*4/14+V251$
V218	$(V216*2+V220*2)/4$	V251	See reference level select tables.
V219	$(V216+V220*3)/4$	V252	$(V251-V255)*21/26+V255$
V220	$(V176-V224)*3/27+V224$	V253	$(V251-V255)*15/26+V255$
V221	$(V220*3+V224)/4$	V254	$(V251-V255)*8/26+V255$
V222	$(V220*2+V224*2)/4$	V255	See reference level select tables.
V223	$(V220+V224*3)/4$		
V224	See reference level select tables.		
V225	$(V224*3+V228)/4$		
V226	$(V224*2+V228*2)/4$		
V227	$(V224+V228*3)/4$		
V228	$(V224-V240)*14/17+V240$		
V229	$(V228*3+V232)/4$		
V230	$(V228*2+V232*2)/4$		

Gamma Correction Register Setting Example

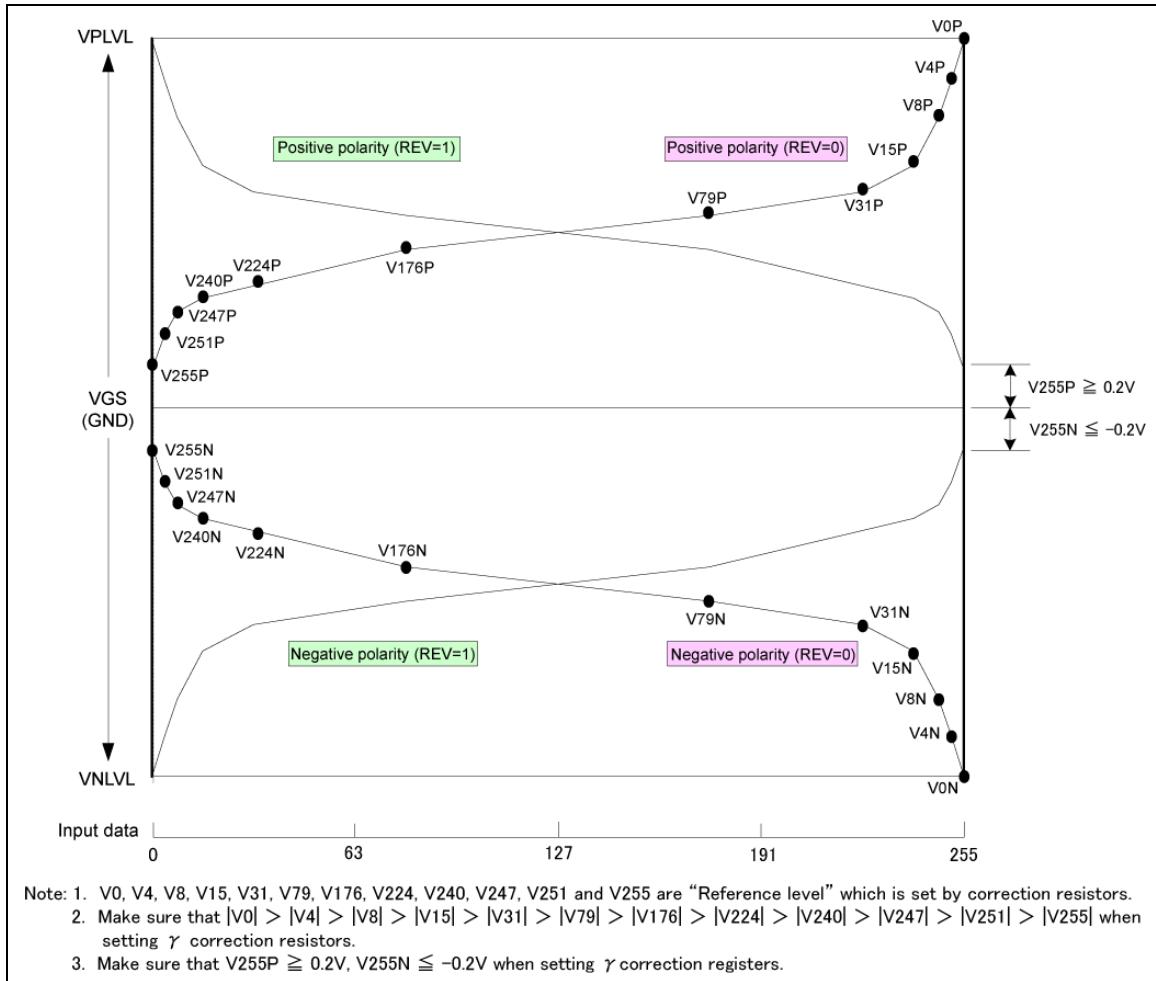


Figure 143

Relationship between Frame Memory Data and Grayscale Voltage (REV)**Table 68**

Frame memory data	REV = 1		REV = 0	
	Positive polarity (PRxPxx)	Negative Polarity (PRxNxx)	Positive Polarity (PRxPxx)	Negative Polarity (PRxNxx)
8'h00	V0	V0	V255	V255
8'h01	V1	V1	V254	V254
8'h02	V2	V2	V253	V253
8'h03	V3	V3	V252	V252
8'h04	V4	V4	V251	V251
8'h05	V5	V5	V250	V250
8'h06	V6	V6	V249	V249
8'h07	V7	V7	V248	V248
8'h08	V8	V8	V247	V247
8'h09	V9	V9	V246	V246
8'h0A	V10	V10	V245	V245
8'h0B	V11	V11	V244	V244
8'h0C	V12	V12	V243	V243
8'h0D	V13	V13	V242	V242
8'h0E	V14	V14	V241	V241
8'h0F	V15	V15	V240	V240
:	:	:	:	:
8'hF0	V240	V240	V15	V15
8'hF1	V241	V241	V14	V14
8'hF2	V242	V242	V13	V13
8'hF3	V243	V243	V12	V12
8'hF4	V244	V244	V11	V11
8'hF5	V245	V245	V10	V10
8'hF6	V246	V246	V9	V9
8'hF7	V247	V247	V8	V8
8'hF8	V248	V248	V7	V7
8'hF9	V249	V249	V6	V6
8'hFA	V250	V250	V5	V5
8'hFB	V251	V251	V4	V4
8'hFC	V252	V252	V3	V3
8'hFD	V253	V253	V2	V2
8'hFE	V254	V254	V1	V1
8'hFF	V255	V255	V0	V0

Power Supply Generating Circuit

The following figure shows the configurations of LCD drive voltage generating circuit of the R61529.

Power Supply Circuit Connection Example

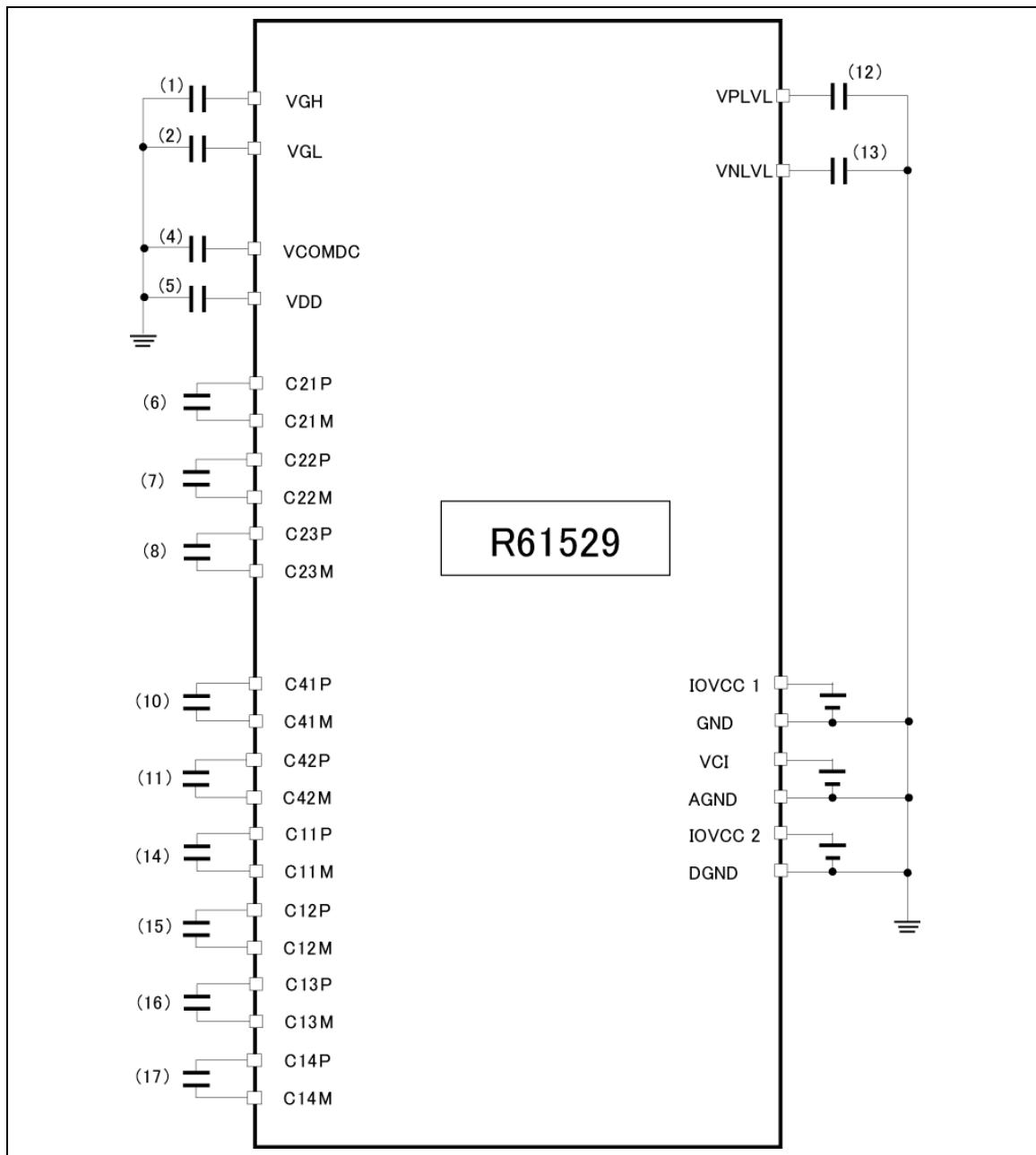


Figure 144

Specifications of External Elements Connected to the Power Supply Circuit

The specifications of external elements connected to the power-supply circuit of the R61529 are as follows. The numbers in the parentheses refer to the numbers in figure “Power Supply Circuit Connection Example”.

Table 69

Capacitor	Recommended tolerance of capacitor	Connected to
1μF (B characteristics) (TBD.)	3V	(5)VDD
	6V	(4)VCOMDC, (10)C41P/M, (11)C42P/M, (14)C11P/M, (15)C12P/M, (16)C13P/M, (17)C14P/M
	10V	(6)C21P/M, (7)C22P/M, (8)C23P/M, (12)VPLVL, (13)VLNL
	25V	(1)VGH, (2)VGL

Stabilizing capacitors connected to VCOMDC, VPLVL, and VLNL are unnecessary according to image quality.

Note: To place bypass capacitor at spots between each power supply (VCI, IOVCC1, and IOVCC2) and GND is recommended.

Voltage Setting Pattern Diagram

The following are the diagrams of voltage generation in the R61529 and the relationship between TFT display application voltage waveforms and electrical potential.

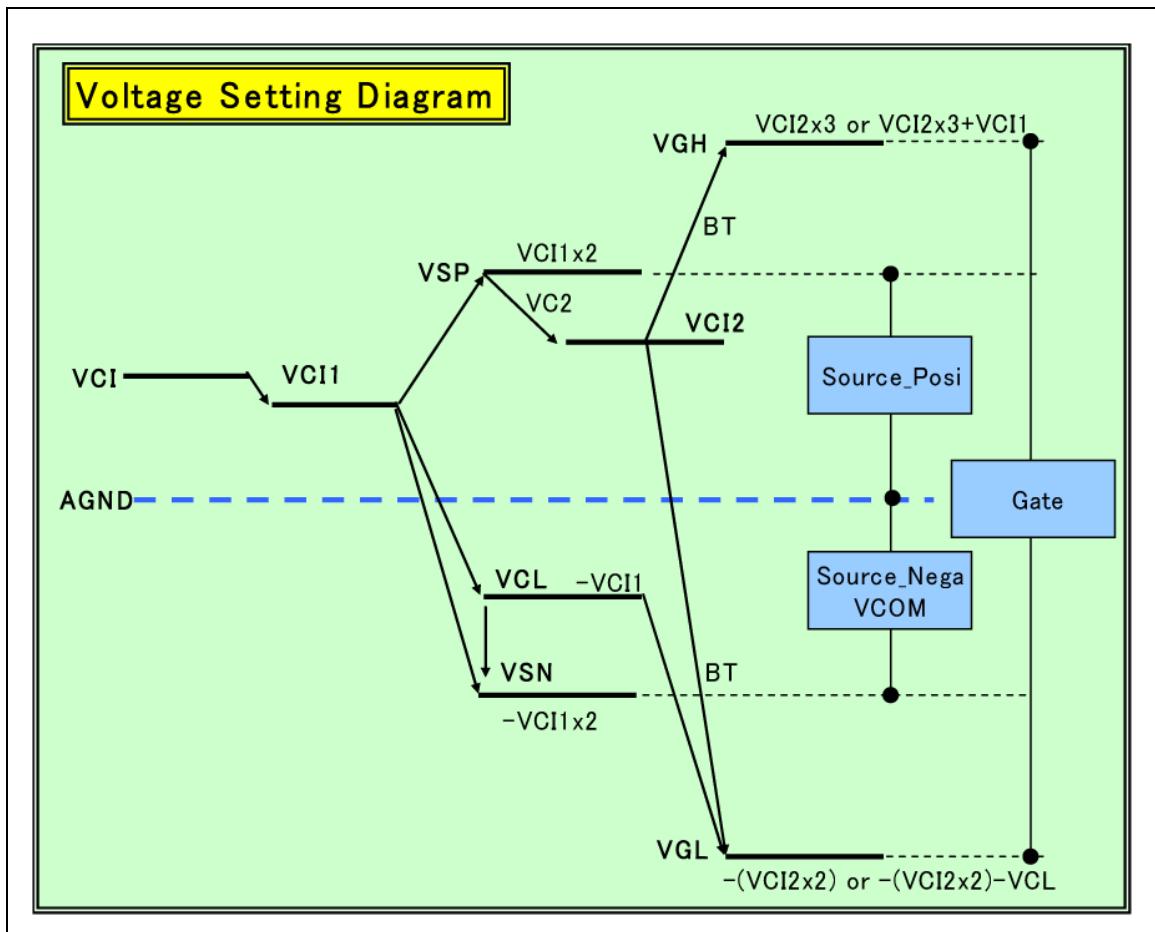


Figure 145

- Note:
1. Make sure that $(VSP-VPLVL) \geq 0.3V$, $(VSN-VNLVL) \leq -0.3V$. Please be careful that the VSP, VSN output voltages will become lower due to current consumption in display operation. Also, this VSP and VSN output voltage depression contributes to VGH and VGL voltages depression. It may lead amplitude reduction of the voltage from IC to the panel, and the gate line drive.
 2. In operation, setting voltages within the respective voltage ranges written above is recommended.
 3. Make sure that $VCI-VCL \leq 6V$.

Voltage setting tables for VGH and VGL are shown below.

Table 70 VGH Setting (VCI1 = 2.8V)

		VCI2						
		5.00V	4.80V	4.60V	4.40V	4.20V	4.00V	3.80V
BT[1:0]	2'h0	Setting inhibited						
	2'h1	17.8V	17.2V	16.6V	16.0V	15.4V	14.8V	14.2V
	2'h2	17.8V	17.2V	16.6V	16.0V	15.4V	14.8V	14.2V
	2'h3	15.0V	14.4V	13.8V	13.2V	12.6V	12.0V	11.4V

Table 71 VGL Setting

		VCI2						
		5.00V	4.80V	4.60V	4.40V	4.20V	4.00V	3.80V
BT[1:0]	2'h0	Setting inhibited						
	2'h1	-12.8V	-12.4V	-12.0V	-11.6V	-11.2V	-10.8V	-10.4V
	2'h2	-10.0V	-9.6V	-9.2V	-8.8V	-8.4V	-8.0V	-7.6V
	2'h3	-10.0V	-9.6V	-9.2V	-8.8V	-8.4V	-8.0V	-7.6V

Deep Standby Mode/Shutdown Mode (MDDI) On/Off Sequence

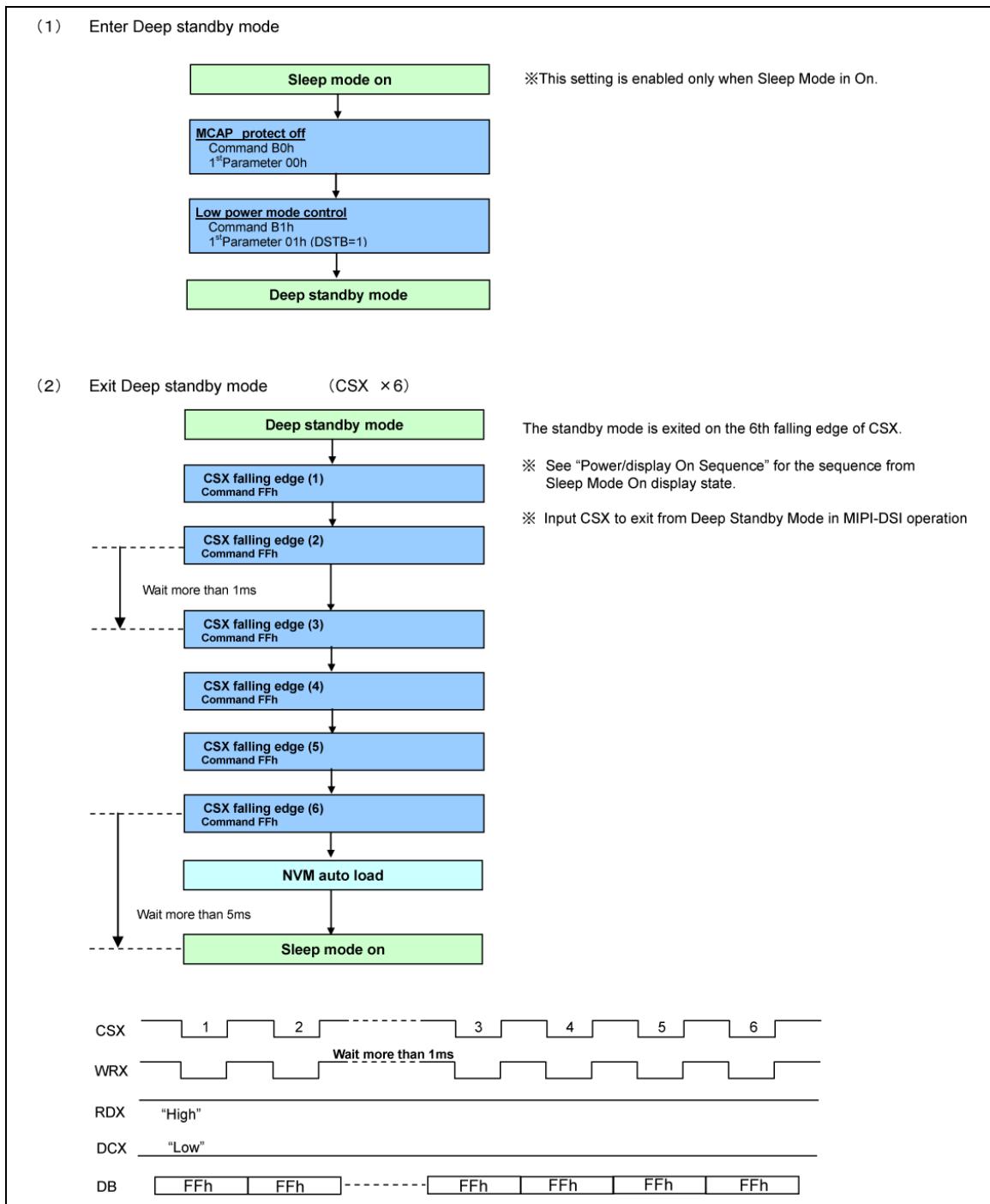


Figure 146

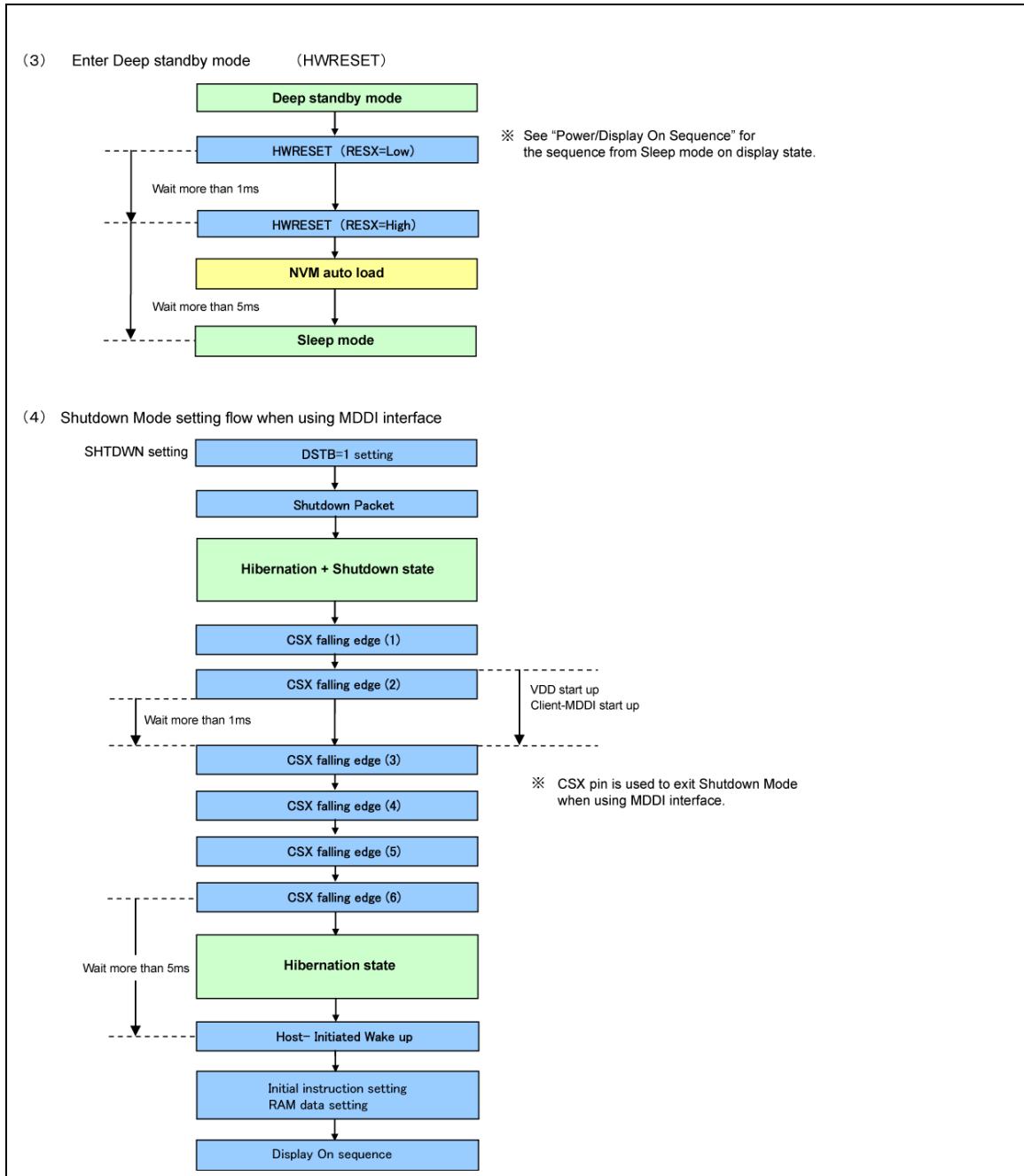


Figure 147

Hardware Reset during Display Operation

If any of the following two conditions occurs during normal display operation, the R61529 executes power supply off sequence.

- (1) Hardware reset (RESX = Low) is accepted during display operation.
- (2) VCI level falls abnormally (about 2.1V or less) during display operation.

In either (1) or (2), as shown below, each of gate output pins G1 to G480 is sequentially set to high level (VGH). After setting them to high level for about 1ms, set each of them to GND level.



Figure 148

NVM Control (TBD)

The R61529 incorporates 2k-bit NVM for user's use.

- 16 bits are for Supplier ID (read by read_DDB_start command)
- 16 bits are for Supplier Elective Data (read by read_DDB_start command)
- Manufacturer Command is stored

To write, read and erase data from/to the NVM, follow the sequence below. Data on the NVM is loaded to internal registers automatically when the sequences are performed.

Power On sequence

HW RESET sequence

exit_sleep_mode command

Data stored in the NVM is retained permanently even if power supply is turned off.

Table 72 NVM Operating Conditions

Operation	Power supply voltage (T.B.D.)		Time	Temperature
Write/Erase	VCI	2.40~3.30V	900ms or more, after E0h: FTT=1setting	+20°C~+30°C
	IOVCC1	1.65~3.30V		

Note: NVM data rewrite (erase-write) operation should be performed up to 5 times per address.

The following commands below are stored in the NVM.

List of Command stored into NVM	
E2h : P1	
B3h : P1~P4	
B4h : P1	
B6h : P1~P2	
B7h : P1~P4	
B8h : P1~P20	
B9h : P1~P4	
C0h : P1~P8	
C1h : P1~P5	
C3h : P1	
C4h : P1~P4	
C6h : P1	
C7h : P1~P2	
C8h : P1~P24	
C9h : P1~P24	
CAh : P1~P24	
CCh : P1	
D0h : P1~P16	
D1h : P1~P4	
D3h : P1	
D6h : P1	
D7h : P1~P15	
D8h : P1~P9	
D9h : P1~P3	
DAh : P1	
E1h : P1~P6	
E6h : P1	
F3h : P1~P5	
F8h : P1	
FAh : P1	
FCh : P1~P5	
FDh : P1~P13	
FEh : P1~P8	

LDx (E2h command) sets command to execute data load from NVM.

Table 73

Unconditional	Manufacturer Command:	E2h
LD[0]	Manufacturer Command:	E1h (parameters 1 ~ 6)
LD[1]	Manufacturer Command:	B3h (parameters 1~4), B4h (parameter 1), B6h (parameters 1~2), B7h (parameters 1~4)
LD[2]	Manufacturer Command:	B8h (parameters 1~20), B9h (parameters 1~4)
LD[3]	Manufacturer Command:	C0h (parameters 1~8), C1h (parameters 1~5), C3h (parameter 1), C4h (parameters 1~4), C6h (parameter 1), C7h (parameters 1~2), C8h (parameters 1~6)
LD[4]	Manufacturer Command:	C8h (parameters 7~24), C9h (parameters 1~24), CAh (parameters 1~24)
LD[5]	Manufacturer Command:	D0h (parameters 1~16), D1h (parameters 1~4), D3h (parameter 1), D7h (parameters 1~15), D8h (parameters 1~9), D9h (parameters 1~3), DAh (parameter 1)
LD[6]	Manufacturer Command:	CCh (parameter 1), D6h (parameter 1), E6h (parameter 1), F3h (parameters 1~5), F8h (parameter 1), FAh (parameter 1), FCh (parameters 1~5), FDh (parameters 1~13), FEh (parameters 1~8)

NVM Write Sequence

The register values of User/Manufacturer Commands supposed to be stored in NVM are written to NVM. When “1” is written to an address, the bit of the address is set to “1”. The default status is “0”.

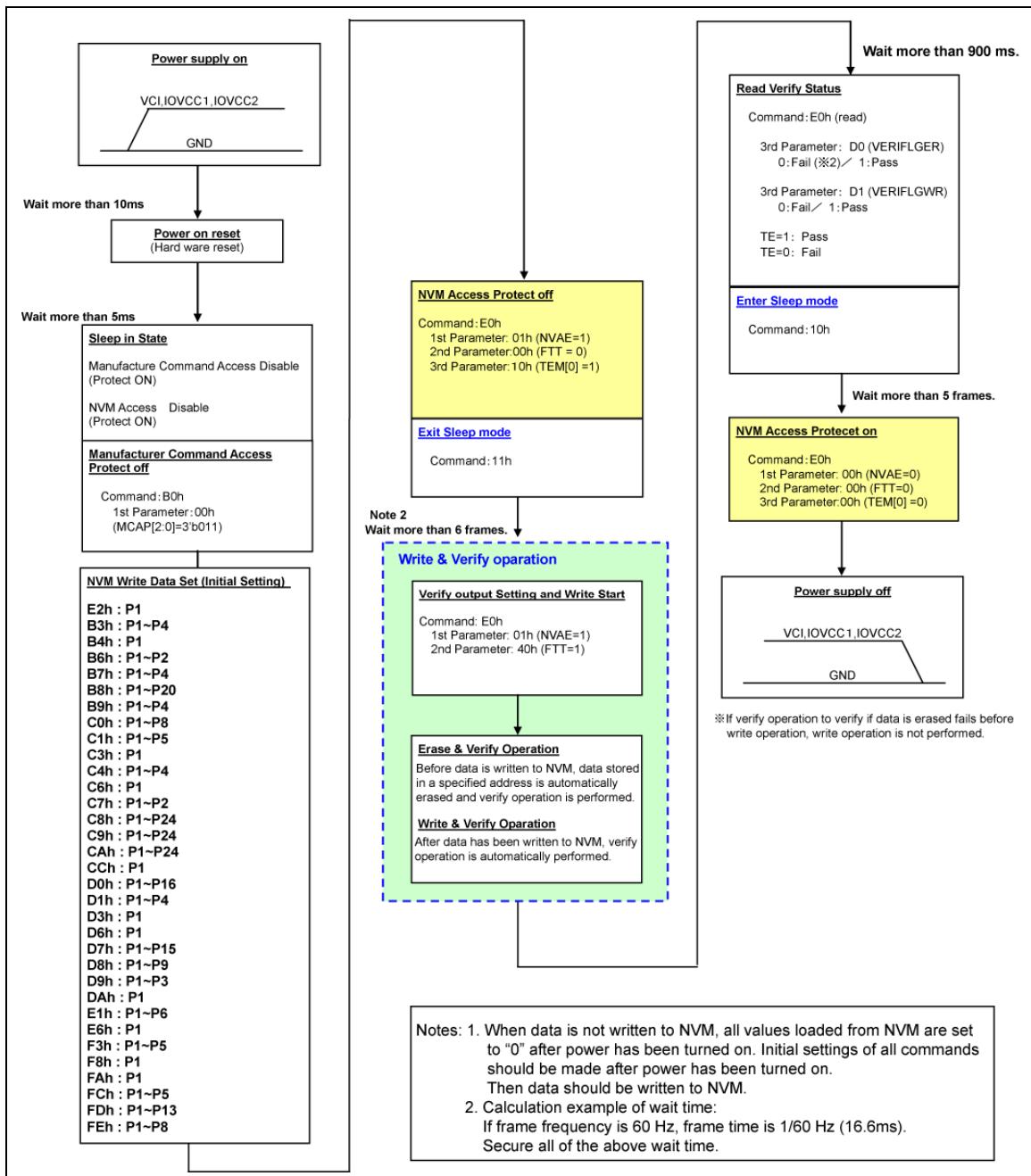


Figure 149

Absolute Maximum Rating

Table 74

Item	Symbol	Unit	Value	Notes
Power supply voltage (1)	IOVCC1, IOVCC2	V	-0.3 ~ +4.6	1, 2
Power supply voltage (2)	VCI – AGND	V	-0.3 ~ +4.6	1, 3
Power supply voltage (3)	VCI – VCL	V	-0.3 ~ +6.5	1, 4
Power supply voltage (4)	VSP – AGND	V	-0.3 ~ +6.5	1, 4
Power supply voltage (5)	AGND – VSN	V	-0.3 ~ +6.5	1, 4
Power supply voltage (6)	AGND – VGL	V	-0.3 ~ +20.0	1, 5
Power supply voltage (7)	VGH – AGND	V	-0.3 ~ +22.0	1
Power supply voltage (8)	VGH – VGL	V	-0.3 ~ +30.0	1
Input voltage	Vt	V	-0.3 ~ IOVCC1,2 + 0.3	1
Operating temperature	Topr	°C	-40 ~ +85	1, 6
Storage temperature	Tstg	°C	-55 ~ +110	1

- Notes:
1. If used beyond the absolute maximum ratings, the LSI may be destroyed. It is strongly recommended to use the LSI within the limits of its electrical characteristics during normal operation. The reliability of LSI is not guaranteed if used in the conditions beyond the limits and it may lead to malfunction.
 2. Make sure (High) IOVCC1 \geq GND (Low), (High) IOVCC2 \geq GND (Low).
 3. Make sure (High) VCI \geq AGND (Low).
 4. Make sure (High) VSP \geq AGND (Low), (High) VSN \leq AGND (Low).
 5. Make sure (High) AGND \geq VGL (Low).
 6. The DC/AC characteristics of die and wafer products are guaranteed at 85°C.

Electrical Characteristics

DC Characteristics

Table 75 (VCI = IOVCC2= 2.8V, IOVCC1 = 1.8V, Ta = -40°C ~ +85°C) ^{see Note 1} (TBD.)

Item	Symbol	Unit	Test condition	Min.	Typ.	Max.	Note
Input "High" level voltage 1 (Except RESX)	V _{IH1}	V	IOVCC=1.650V~3.300V	0.80 x IOVCC1	—	IOVCC1	1, 2
Input "Low" level voltage 1 (RESX)	V _{IL1}	V	IOVCC=1.650V~3.300V	0	—	0.20 x IOVCC1	1, 2
Input "High" level voltage 2 (RESX)	V _{IH2}	V	IOVCC=1.650V~3.300V	0.90 x IOVCC1	—	IOVCC1	1, 2
Input "Low" level voltage 2 (RESX)	V _{IL2}	V	IOVCC=1.650V~3.300V	0	—	0.10 x IOVCC1	1, 2
Output "High" level voltage 1 (DB[15:0],TE,LEDPWM)	V _{OH1}	V	IOVCC=1.650V~3.300V, IOUT=-0.1mA	0.80 x IOVCC1	—	—	1
Output "Low" level voltage 1 (DB[15:0],TE,LEDPWM)	V _{OL1}	V	IOVCC=1.650V~3.300Vm, IOUT=0.1mA	—	—	0.20 x IOVCC1	1
Input "High" level current	I _{IH}	µA	Vin=IOVCC1	—	—	10	3
Input "Low" level current	I _{IL}	µA	Vin=0V	-10	—	—	3
Current consumption (IOVCC1-GND)	Normal Mode +Sleep out	I _{OPN}	480-line drive IOVCC1=1.80V IOVCC2=VCI=2.80V fFLM=60Hz, Ta=25°C BLCON=0, IM3-0='0111'	-	-	TBD	5
	Deep Standby mode	I _{DST1}	IOVCC1=1.80V IOVCC2=VCI=2.80V Ta=25°C	-	0.1	1.0	4

Table 76 (VCI = IOVCC2= 2.8V, IOVCC1 = 1.8V, Ta = -40°C ~ +85°C) ^{see Note 1} (TBD.) (Continued)

Item	Symbol	Unit	Test condition	Min.	Typ.	Max.	Note	
LCD power supply current (VCI-GND)	Normal Mode +Sleep out	I _{CIN}	480-line drive IOVCC1=1.80V IOVCC2=VCI=2.80V fFLM=60Hz, Ta=25°C RAM data: 24'h000000, REV=0, FP=5'h08, BP=5'h08, VC2=3'h3, VC3=3'h7, PVH=7'h30, NVH=7'h30, VDC=8'h4D, AP=3'h3, APN=3'h3, SWRON=0, SWRONM=0, DC1=2'h1, DC2=2'h2, DC4=2'h1, DC1M=2'h1, SEQGND=4'h4, SEQVCIL=4'h4, GEQ1W=3'h3, GSEL*P0=GSEL*N0=7'h00 GSEL*P1=GSEL*N1=7'h10 GSEL*P2=GSEL*N2=7'h20 GSEL*P3=GSEL*N3=7'h30 GSEL*P4=GSEL*N4=7'h40 GSEL*P5=GSEL*N5=7'h50 GSEL*P6=GSEL*N6=7'h48 GSEL*P7=GSEL*N7=7'h38 GSEL*P8=GSEL*N8=7'h28 GSEL*P9=GSEL*N9=7'h15 GSEL*P10=GSEL*N10=7'h 08 GSEL*P11=GSEL*N11=7'h 01 (*: A,B,C) No load on panel	-	-	TBD.	4	
	Deep Standby mode	I _{DST3}	μA	IOVCC1=1.80V IOVCC2=VCI=2.80V	-	0.1	1.0	5
Output voltage dispersion		ΔVo	mV	-	-	-	TBD.	5
Average output variance		ΔVΔ	mV	-	-35	-	+35	6

DC Characteristics (MIPI DSI)**Table 77 (VCI = IOVCC2= 2.8V, IOVCC1 = 1.8V, Ta = -40°C ~ +85°C) see Note 1 (TBD.)**

Item	Symbol	Unit	Test condition	Min.	Typ.	Max.	Note	
DSI current consumption (IOVCC2-DGND):	HS mode	I_{HS}	mA	IOVCC1=1.800V IOVCC2=VCI=2.800V DSI 1 lane, DSICLK=120MHz DSI Data:24'h000	-	-	TBD.	4
	LP mode	I_{LP}	μA	IOVCC1=1.800V IOVCC2=VCI=2.800V Clock lane=LP11 Data lane=LP11	-	-	TBD.	4
	Deep Standby mode	I_{DST2}	μA	IOVCC1=1.800V IOVCC2=VCI=2.800V Ta=25°C	-	0.1	1.0	4

Notes to Electrical Characteristics

- Notes:
1. DC/AC electrical characteristics of bare die and wafer are guaranteed at +85°C.
 2. The following figures illustrate the configurations of input, I/O, and output pins.

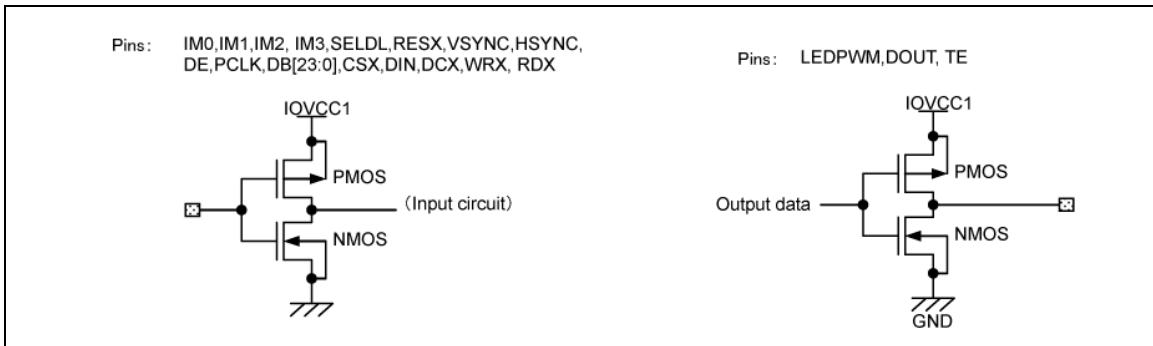


Figure 150 Pin Circuit Configuration

3. This excludes the current in the output drive MOS.
4. This excludes the current in the input/output units. Make sure that the input level is fixed because shoot-through current increases in the input circuit when the CMOS input is at a mid-level. The current consumption is unaffected by whether the CSX pin is “high” or “low” while not accessing via interface pins.
5. The output voltage deviation is the difference in voltages between output pins that are placed side by side in the same display mode. It is a reference value.
6. The average output voltage dispersion is the variance of average source-output voltage of different chips of the same product. The average source output voltage is measured for one chip with the same display data.

DC Characteristics (MIPI DSI DC Specifications)**Table 78 (IOVCC2= 2.40V~3.30V, Ta = -40°C ~ +85°C) (TBD.)**

Item		Symbol	Unit	Test Condition	Min.	Typ.	Max.	Notes
HS-RX	Differential input high threshold	VIDTH	mV		-	-	70	3
	Differential input low threshold	VIDTL	mV		-70	-	-	3
	Single-ended input low voltage	VILHS	mV		-40	-	-	
	Single-ended input high voltage	VIHHS	mV		-	-	460	
	Common-mode voltage HS receive mode	VCMRX(DC)	mV		70	-	330	1
	Differential input impedance	ZID	Ω		-	(90)	-	2
LP-RX	Logic 0 input voltage not in ULP State	VIL	mV		-50	-	550	
	Logic 1 input voltage	VIH	mV		880	-	1350	
	I/O leakage current	ILEAK	µA	Vin = -50mV - 1350mV	-10	-	10	
LP-TX	Thevenin output low level	VOL	mV		-50	-	50	
	Thevenin output high level	VOH	V		1.1	1.2	1.3	
	Output impedance of LP transmitter	ZOLP	Ω		(110)	-	-	2
CD-RX	Logic 0 contention threshold	VILCD	mV		-	-	200	
	Logic 1 contention threshold	VIHCD	mV		450	-	-	

- Notes:
1. VCMRX(DC) = (VDP+VDN)/2
 2. Excluding COG Resistance (Contact Resistance and ITO Wiring Resistance). The values are tentative.
 3. Minimum 110mV/-110mV HS differential swing is required for display data transfer.

DC Characteristics (MDDI)**Table 79 (VCI = IOVCC2= 2.8V, IOVCC1 = 1.8V, Ta = -40°C ~ +85°C) ^{see Note 1} (TBD.)**

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Notes
Standard receiver differential input “High” threshold voltage (DATA0P/N, STB_CLKP/N)	V _{IT+}	mV	(DATA0P) – (DATA0N) (STB_CLKP) – (STB_CLKN)	—	0	50	—
Standard receiver differential input “Low” threshold voltage (DATA0P/N, STB_CLKP/N)	V _{IT-}	mV	(DATA0P) – (DATA0N) (STB_CLKP) – (STB_CLK M)	-50	0	—	—
Offset receiver differential input “High” threshold voltage (DATA0P/N)	V _{IT+off}	mV		—	85	110	—
Offset receiver differential input “Low” threshold voltage (DATA0P/N)	V _{IT-off}	mV		60	85	—	—
Receiver differential input “High” Current (DATA0P/N, STB_CLKP/N)	I _{ID+}	mA		1.5	—	2.5	1
Receiver differential input “Low” Current (DATA0P/N, STB_CLKP/N)	I _{ID-}	mA		-2.5	—	-1.5	1
Input voltage range	V _{IRNG}	V		0.6	—	1.1	—
Driver differential output “High” Current (DATA0P/N)	I _{OD+}	mA		2.5	—	4.5	2
Driver differential output “Low” Current (DATA0P/N)	I _{OD-}	mA		-4.5	—	-2.5	2
Output voltage range	V _{ORNG}	V		0.11	—	1.60	2
Differential input impedance	ZID	Ω		80	100	125	—
Current consumption (IOVCC2-DGND)	I _{hib}	uA	IOVCC1=IOVCC2=VCI=2.85V, Ta=25°C	—	TBD.	TBD.	—
Current consumption (IOVCC2-DGND)	I _{trans}	mA	IOVCC1=IOVCC2= VCI =2.85V, 1/t _{BIT} =250Mbps, Ta=25°C	—	TBD.	TBD.	—

Note: The DC/AC characteristics of die and wafer products are guaranteed at 85°C.

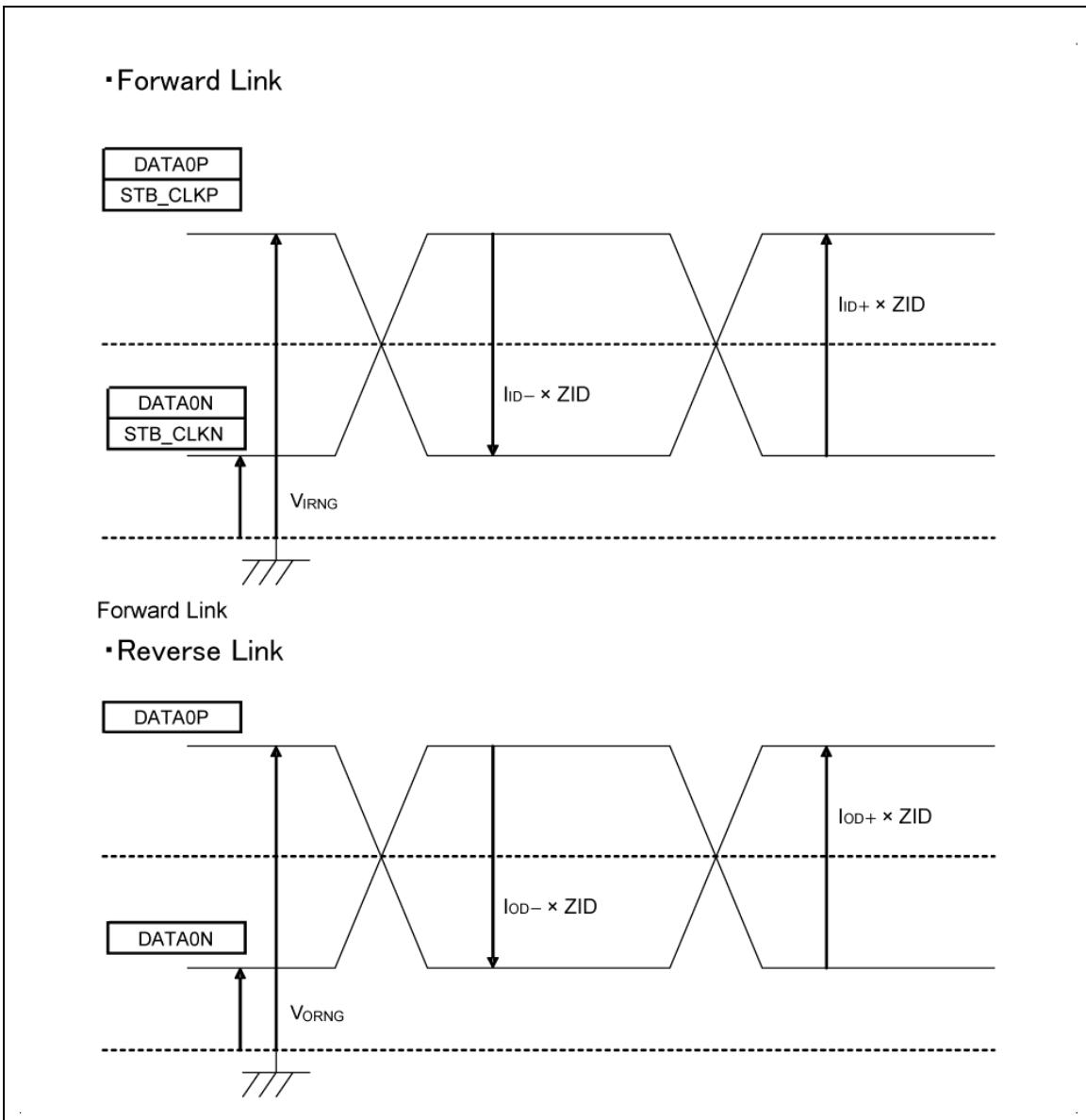


Figure 151 MDDI DC Characteristic Symbol

Step-up Circuit Characteristics

Table 80 (VCI = IOVCC2= 2.8V, IOVCC1 = 1.8V, Ta = -40°C ~ +85°C) see Note 1 (TBD.)

Item	Unit	Test Condition	Min.	Typ.	Max.
Step-up output voltage	VSP	V	TBD.	TBD.	TBD.
	VSN	V	TBD.	TBD.	TBD.
	VCL	V	TBD.	TBD.	TBD.
	VGH	V	TBD.	TBD.	TBD.
	VGL	V	TBD.	TBD.	TBD.

Note: The DC/AC characteristics of die and wafer products are guaranteed at 85°C.

Power Supply Voltage Range

Table 81 (VCI = IOVCC2= 2.8V, IOVCC1 = 1.8V, Ta = -40°C ~ +85°C) see Note 1

Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
Power supply voltage	IOVCC1	V	1.65	1.80	3.30	-
	IOVCC2	V	2.40	2.80	3.30	-
	VCI	V	2.40	2.80	3.30	-

Note: The DC/AC characteristics of die and wafer products are guaranteed at 85°C.

Output Voltage Range

Table 82 (VCI = IOVCC2= 2.8V, IOVCC1 = 1.8V, Ta = -40°C ~ +85°C) see Note 1

Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
Source driver	Positive polarity	V	VGS+0.2V	-	VSP-0.3	-
	Negative polarity	V	VSN+0.3	-	VGS-0.2V	
Grayscale reference voltage	VPLVL	V	3.0V	-	VSP-0.3V	-
	VNLVL	V	VSN+0.3V	-	-3.0V	-
Step-up output voltage	VSP	V	4.6V	-	6.0V	-
Step-up output voltage	VSN	V	-4.6V	-	-6.0V	-
Step-up output voltage	VGH	V	11.4V	-	17.8V	-
Step-up output voltage	VGL	V	-7.6V	-	-12.8V	-
Voltage between VGH and VGL		V		-	28.0V	-

Note: The DC/AC characteristics of die and wafer products are guaranteed at 85°C.

Clock Characteristics

Table 83 (VCI = IOVCC2= 2.8V, IOVCC1 = 1.8V, Ta = -40°C ~ +85°C) see Note 1

Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
RC oscillation clock	fosc	MHz	13.0	14.0	15.0	-

Note: The DC/AC characteristics of die and wafer products are guaranteed at 85°C.

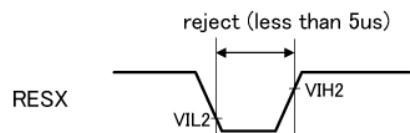
Reset Timing Characteristics

Table 84 (VCI = IOVCC2= 2.8V, IOVCC1 = 1.8V, Ta = -40°C ~ +85°C) see Note 1

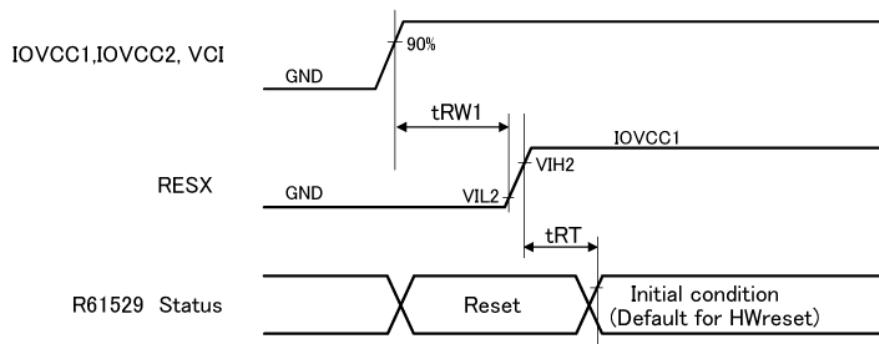
Item	Symbol	Unit	Test Condition	Min.	Max.
Reset "Low" level width 1	tRW1	ms	Power On	1	—
Reset "Low" level width 2	tRW2	us	Operation	10	—
Reset time	tRT	ms		—	5

Note: The DC/AC characteristics of die and wafer products are guaranteed at 85°C.

Reset reject



(1) Reset timing at Power supply ON



(2) Reset timing during operation

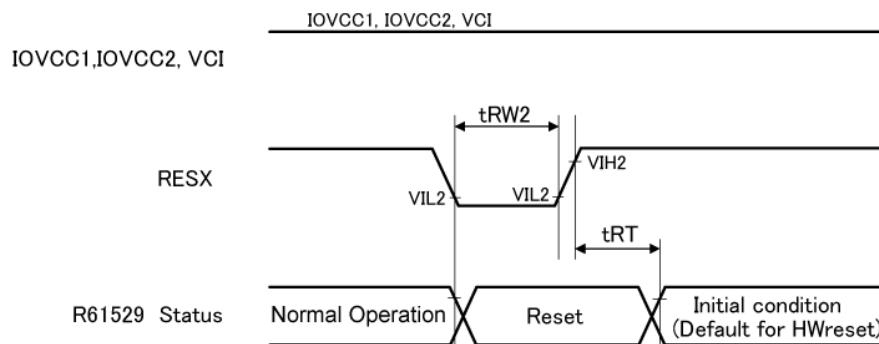


Figure 152 Reset Timing Characteristics

Liquid Crystal Driver Output Characteristics

Table 85 Source Driver (VCI = IOVCC2= 2.8V, IOVCC1 = 1.8V, Ta = -40°C ~ +85°C) see Note 1

Item	Symbol	Unit	Test condition	Min.	Typ.	Max.	Note
Source driver output delay time	tdds	us	VSP=5.6V,VSN=-5.6V, GNDpre-charge time =3.4us VCI/VCLpre-charge time =3.4us Amplitude : -5.2V~+5.2V Margin : Target grayscale voltage $\pm 35mV$	—	—	30	2

Notes: 1. The DC/AC characteristics of die and wafer products are guaranteed at 85°C.

2. LCD driver output delay time depends on the liquid crystal panel load. Therefore, frame frequency and one line cycle needs to be specified checking image quality on the panel to be used.

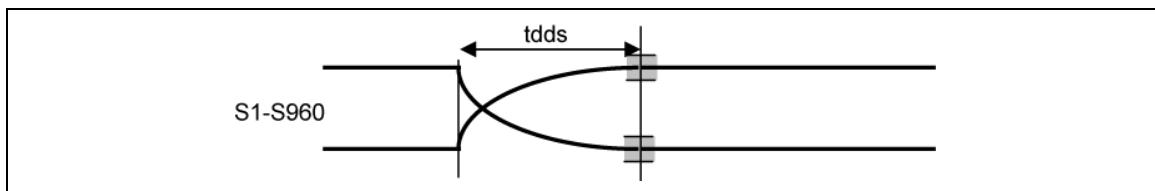


Figure 153 Liquid Crystal Driver Output Timing (TBD.)

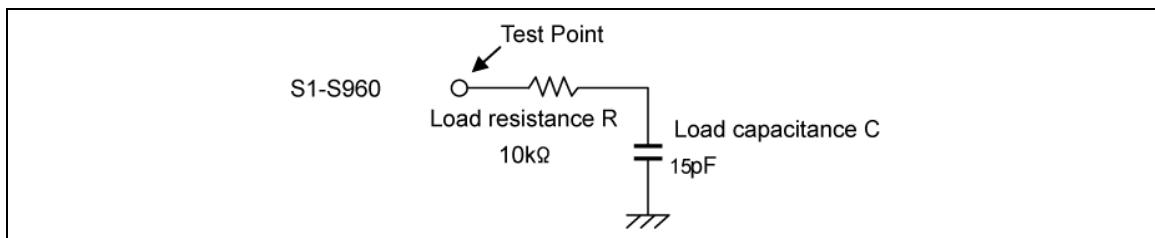


Figure 154 Load circuit for testing LCD driver output characteristics (TBD.)

MIPI DBI Type B Timing Characteristics(VCI=IOVCC2=2.8V, IOVCC1=1.8V, Ta=-40°C ~ +85°C)^{see Note 1}

Note: The DC/AC characteristics of die and wafer products are guaranteed at 85°C.

Table 86 3/2-Transfer (IOVCC1=1.650V ~ 3.3V, Ta=-40°C ~ +85°C) (TBD.)

Item	Symbol	Unit	Test Condition	Min.	Max.
Address setup time	DCX	tast	ns	0	-
Address hold time (Write/Read)		taht	ns	10	-
Chip select setup time (Write)	CSX	tcs	ns	20	-
Chip select setup time (Read)		trcs	ns	170	-
Chip select wait time (Write/Read)		tcsf	ns	15	-
Write cycle time	WRX	twc	ns	50	-
Write control pulse "High" period		twrh	ns	20	-
Write control pulse "Low" period		twrl	ns	20	-
Read cycle time	RDX	trc	ns	450	-
Read control pulse "High" period		trdh	ns	250	-
Read control pulse "Low" period		trdl	ns	170	-
Write data setup time	DB[23:0]	twds	ns	CL Max.30pF Min.8pF	15
Write data hold time		twdh	ns		15
Read access time		tracc	ns		10
Output disable time		trod	ns		10

Table 87 1-Transfer (IOVCC1=1.650V ~ 3.3V, Ta=-40°C ~ +85°C) (TBD.)

Item	Symbol	Unit	Test Condition	Min.	Max.
Address setup time	DCX	tast	ns	0	-
Address hold time (Write/Read)		taht	ns	10	-
Chip select setup time (Write)	CSX	tcs	ns	35	-
Chip select setup time (Read)		trcs	ns	170	-
Chip select wait time (Write/Read)		tcsf	ns	15	-
Write cycle time	WRX	twc	ns	80	-
Write control pulse "High" period		twrh	ns	35	-
Write control pulse "Low" period		twrl	ns	35	-
Read cycle time	RDX	trc	ns	450	-
Read control pulse "High" period		trdh	ns	250	-
Read control pulse "Low" period		trdl	ns	170	-
Write data setup time	DB[23:0]	twds	ns	CL Max.30pF Min.8pF	15
Write data hold time		twdh	ns		15
Read access time		tracc	ns		10
Output disable time		trod	ns		10
					150

Table 88 2-, 3- Transfer (IOVCC1=1.650V ~ 3.3V, Ta=-40°C ~ +85°C) (TBD.)

Item	Symbol	Unit	Test Condition	Min.	Max.
Address setup time	DCX	tast	ns	0	-
Address hold time (Write/Read)		taht	ns	10	-
Chip select setup time (Write)	CSX	tcs	ns	15	-
Chip select setup time (Read)		trcs	ns	170	-
Chip select wait time (Write/Read)		tcsf	ns	15	-
Write cycle time	WRX	twc	ns	40	-
Write control pulse "High" period		twrh	ns	15	-
Write control pulse "Low" period		twrl	ns	15	-
Read cycle time	RDX	trc	ns	450	-
Read control pulse "High" period		trdh	ns	250	-
Read control pulse "Low" period		trdl	ns	170	-
Write data setup time	DB[23:0]	twds	ns	CL Max.30pF Min.8pF	15
Write data hold time		twdh	ns		25
Read access time		tracc	ns		10
Output disable time		trod	ns		150
					10

Note: 1 transfer: (1) 16-bit I/F 16bpp

3/2 transfers: (1) 16-bit I/F 18bpp, (2) 16-bit I/F 24 bpp Option 1

2 transfers: (1) 8-bit I/F 16bpp, (2) 16-bit I/F 18bpp Options 2, 3, (3) 16-bit I/F 24bpp Option 2

3 transfers: (1) 8-bit I/F 18bpp, (2) 8-bit I/F 24bpp

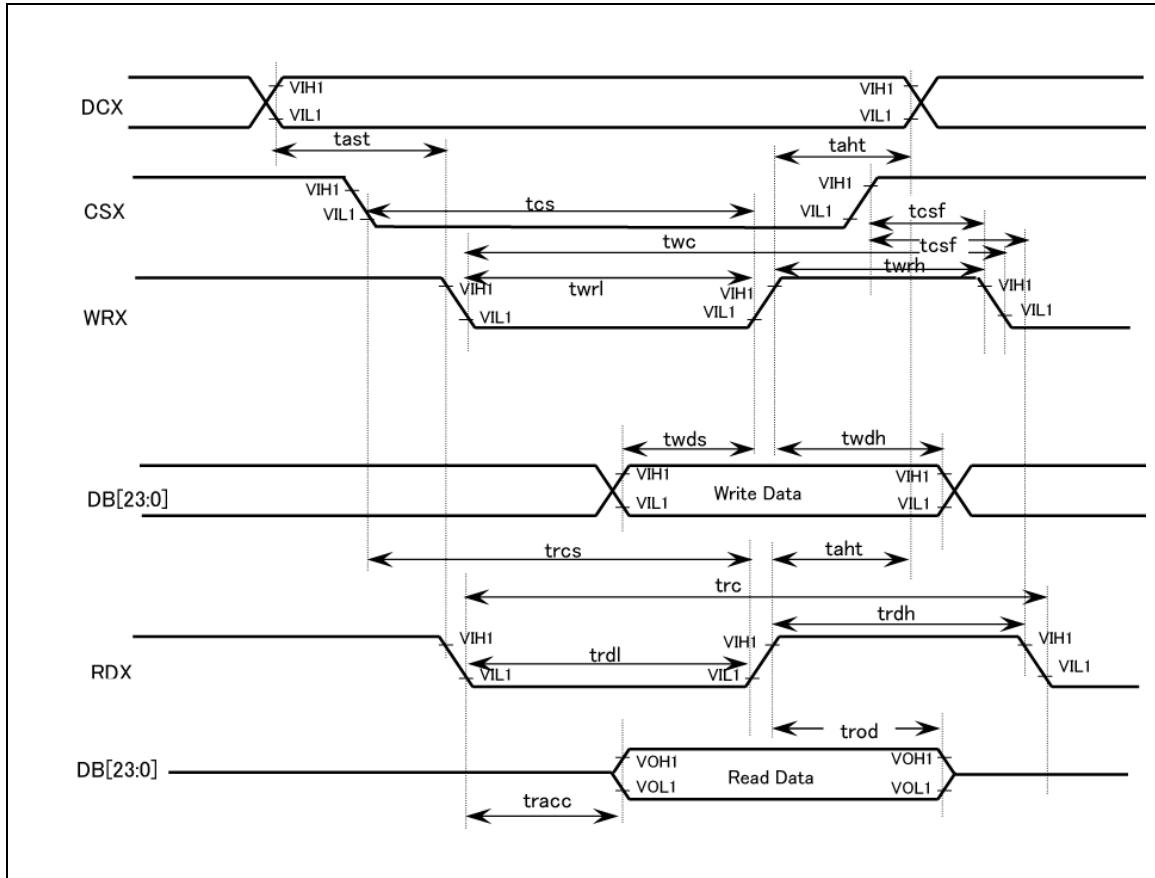
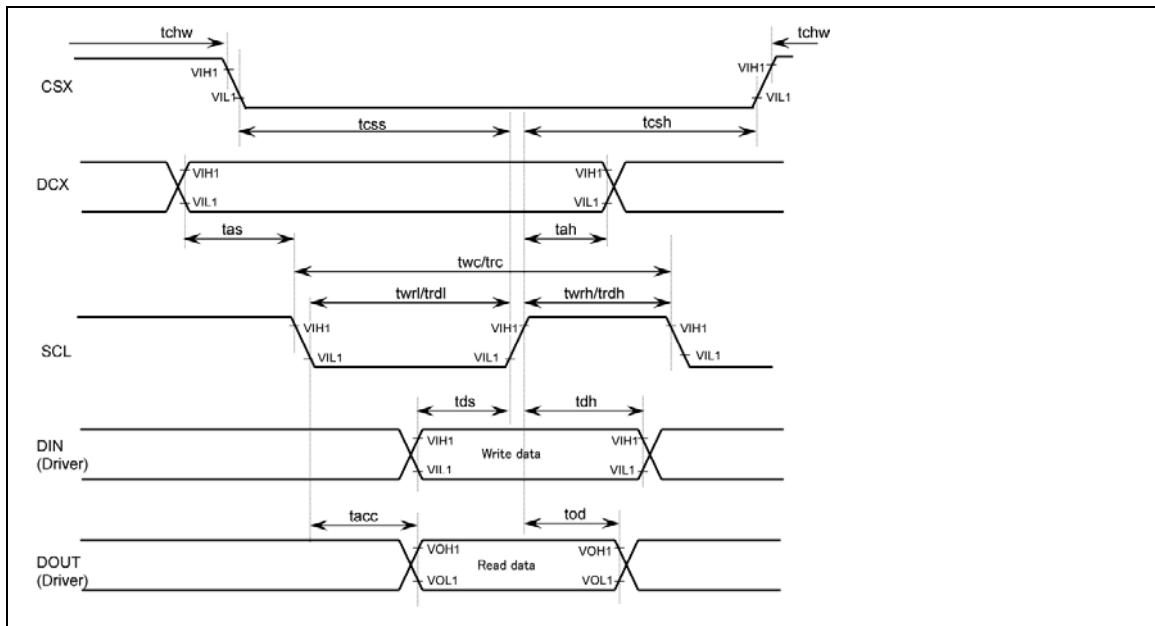


Figure 155 DBI Type B (24/18/16/8 Bits) Timing

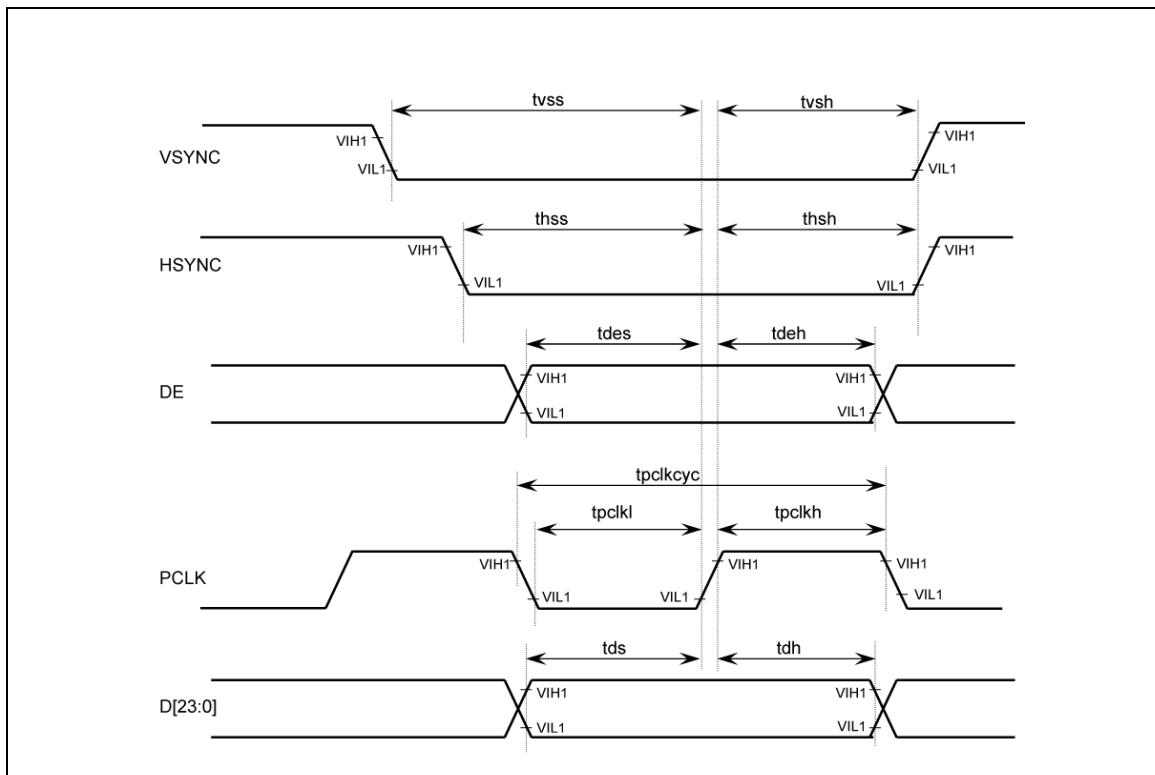
MIPI DBI Type C Timing Characteristics**Table 89 (IOVCC1=1.65V~3.30V, Ta=-40°C~+85°C) (TBD.)**

Item	Symbol	Unit	Test Condition	Min.	Max.
Chip Select Set Up Time	CSX	tcss	ns	40	-
Chip Select Hold Time		tcsH	ns	40	-
Chip Select High Pulse Width		tchw	ns	100	
Address setup time	DCX	tas	ns	10	
Address hold time (Write/Read)		tah	ns	10	
Write Cycle Time	SCL (Write)	twc	ns	100	-
SCL "High"Width(Write)		twrh	ns	40	-
SCL "Low"Width(Write)		twrl	ns	40	-
Read Cycle Time	SCL (Read)	trc	ns	300	-
SCL "High"Width (Read)		trdh	ns	120	-
SCL "Low"Width(Read)		trdl	ns	120	-
Data Set Up Time	DIN	tds	ns	30	-
Data Hold Time		tdh	ns	30	-
Access Time	DOUT	tacc	ns	CL Max.30pF Min.8pF	110
Output Disable Time		tod	ns		10
Rise/fall time	-	tr/tf	ns	-	15

**Figure 156 MIPI DBI Type C Timing**

MIPI DPI Timing Characteristics (IOVCC1=1.65V~3.30V, Ta=-40°C~+85°C) (TBD)**Table 90**

Item	Symbol	Unit	Test Condition	Min.	Max.
VSYNC setup time	VSYNC	tvss	ns	20	-
VSYNC hold time		tvsh	ns	20	-
Hsync setup time	Hsync	thss	ns	20	-
Hsync hold time		thsh	ns	20	-
DE setup time	DE	tdes	ns	20	-
DE hold time		tdeh	ns	20	-
Pixel clock cycle time	PCLK	tpclkcyc	ns	74	-
Pixel clock "Low" period		tpclkl	ns	32	-
Pixel clock "High" period		tpclkh	ns	32	-
Data setup time	DB[23:0]	tds	ns	20	-
Data hold time		tdh	ns	20	-

**Figure 157 MIPI DPI Timing**

Serial Interface Timing Characteristics (I^2C)

Table 91 (IOVCC1=1.650V ~ 3.3V, Ta=-40°C ~ +85°C) (TBD.)

Item	Symbol	Unit	Min.	Typ.	Max.
Serial clock cycle time	t_{SCL}	ns	2500	-	-
Serial clock "High" period	t_{SCLH}	ns	600	-	-
Serial clock "Low" period	t_{SCLL}	ns	1300	-	-
Bus free time	t_{BUF}	ns	300	-	-
Start condition Hold time	t_{STAH}	ns	600	-	-
Restart condition setup time	t_{STAS}	ns	600	-	-
Stop condition setup time	t_{STOPS}	ns	600	-	-
Data setup time	t_{SDAS}	ns	300	-	-
Data hold time	t_{SDAH}	ns	0	-	-

Notes: 1. The line connected to the SDA pin requires an external pull-up resistor in I^2C bus interface operation.

2. The output data delay time is based on the load condition compliant with I^2C .

Serial Interface Operation

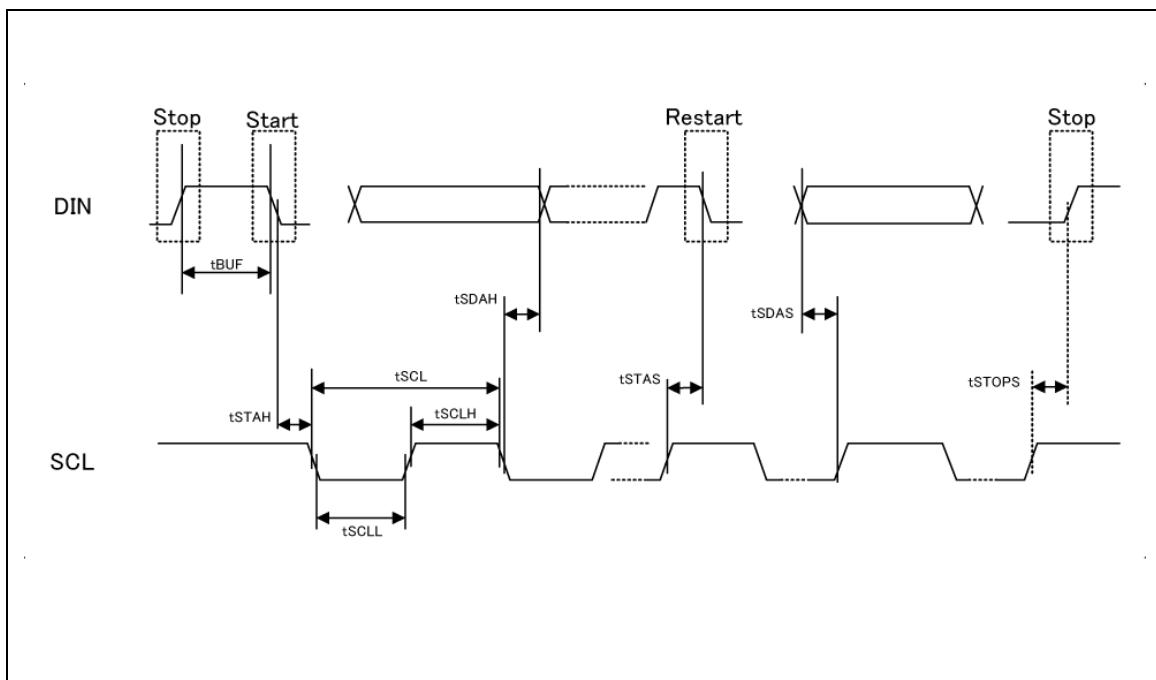


Figure 158 I^2C Timing

HS-RX Clock and Data-Clock Specifications (IOVCC2=2.40V~3.30V, Ta=-40°C ~+85°C) (TBD)**Table 92**

Item	Symbol	Unit	Min.	Typ.	Max.	Note
DSICLK Frequency	fDSICLK	MHz	100	-	250	4
DSICLK Cycle time	tCLKP	ns	4.0	-	10	
DSI Data Transfer Rate (Command mode)	tDSIR	Mbps	200	-	500	4
DSI Data Transfer Rate (Video mode)	tDSIR	Mbps	200	-	350	4
Data to Clock Setup Time	tSETUP	UI	0.15	-	-	
		ns	0.30	-	-	5
Clock to Data Hold Time	tHOLD	UI	0.15	-	-	
		ns	0.30	-	-	5

Note: 4. When $tDSICLK \leq 125\text{MHz}$, change auto load NV setting so that it is compliant with THS-PREPRare+THS-ZERO spec.

5. Minimum tSETUP/tHOLD Time is 0.15UI. This value may change according to DSI transfer rate.

LP-RX/TX Clock and Data-Clock Specifications (IOVCC2=2.40V~3.30V, Ta=-40°C ~+85°C) (TBD)**Table 93**

Parameter	Description	Min	Typ	Max	Unit	Notes
T _{HS-PREPARE}	Time to drive LP-00 to prepare for HS transmission	40 ns + 4*UI	-	85ns + 6*UI	ns	
T _{HS-PREPARE} + T _{HS-ZERO}	T _{HS-PREPARE} + Time to drive HS-0 before the Sync sequence	145ns + 10*UI	-	-	ns	
T _{HS-TRAIL}	Time to drive flipped differential state after last payload data bit of a HS transmission burst	max (n*8*UI, 60 ns + n*4*UI)	-	-	ns	1,2
T _{HS-EXIT}	Time to drive LP-11 after HS burst	100	-	-	ns	
T _{TA-GO}	Time to drive LP-00 after Turnaround Request	4*T _{LPTX}				
T _{TA-SURE}	Time-out before new TX side starts driving	1*T _{LPTX}	-	2*T _{LPTX}		
T _{TA-GET}	Time to drive LP-00 by new TX	5*T _{LPTX}				
T _{LPX}	Length of any Low-Power state period	50	-	-	ns	
Ratio T _{LPX}	Ratio of T _{LPX(MASTER)} /T _{LPX(SLAVE)} between Master and Slave side	2/3	-	3/2		
T _{CLK-POST}	Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	60 ns + 52UI	-	-	UI	3
T _{CLK-PREPARE} + T _{CLK-ZERO}	T _{CLK-PREPARE} + time for lead HS-0 drive period before starting Clock	300	-	-	ns	
T _{CLK-PRE}	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8	-	-	UI	
T _{CLK-PREPARE}	Time to drive LP-00 to prepare for HS clock transmission	38	-	95	ns	
T _{CLK-TRAIL}	Time to drive HS differential state after last payload clock bit of an HS transmission burst	60	-	-	ns	
T _{EOT}	Time from start of T _{HS-TRAIL} period to start of LP-11 state	-	-	105 ns + n*12*UI		2
T _{LPTX1}	Length of Low-Power TX period in case of using DSI clock	-	16/fDSICLK	-	UI	4
T _{LPTX2}	Length of Low-Power TX period in case of using internal OSC clock	-	1/fosc	-	ns	

- Notes:
1. If $a > b$ then $\max(a, b) = a$, otherwise $\max(a, b) = b$
 2. Where $n = 1$ for Forward-direction HS mode.
 3. The R61529 can work with this specification although the end part of internal process is remained when Clock Lane enter LP-11 and delay. Due to the R61529 can work without the remained process if tCLK-POST is more than 256 UI.
 4. The R61529 uses DSI clock from the Host processor if Clock Lane is active, and internal oscillator clock if Clock Lane is disabled. Here, "fosc" is the frequency of oscillator clock, typical 14MHz.

Timing Diagram

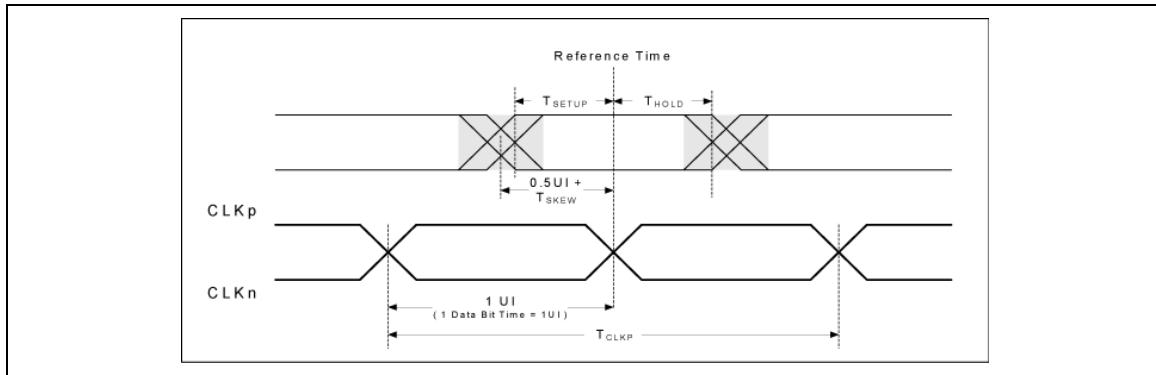


Figure 159 Data to Clock Timing Definitions

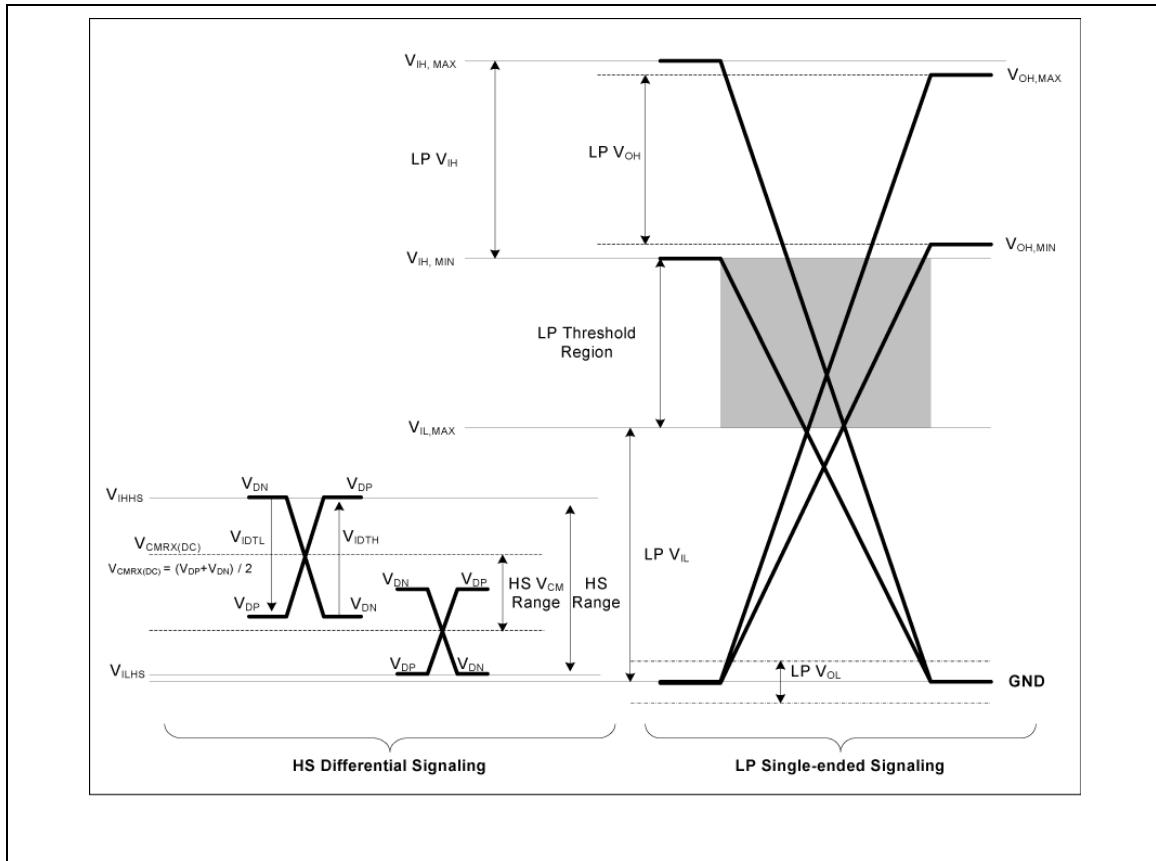


Figure 160 DSI LP mode

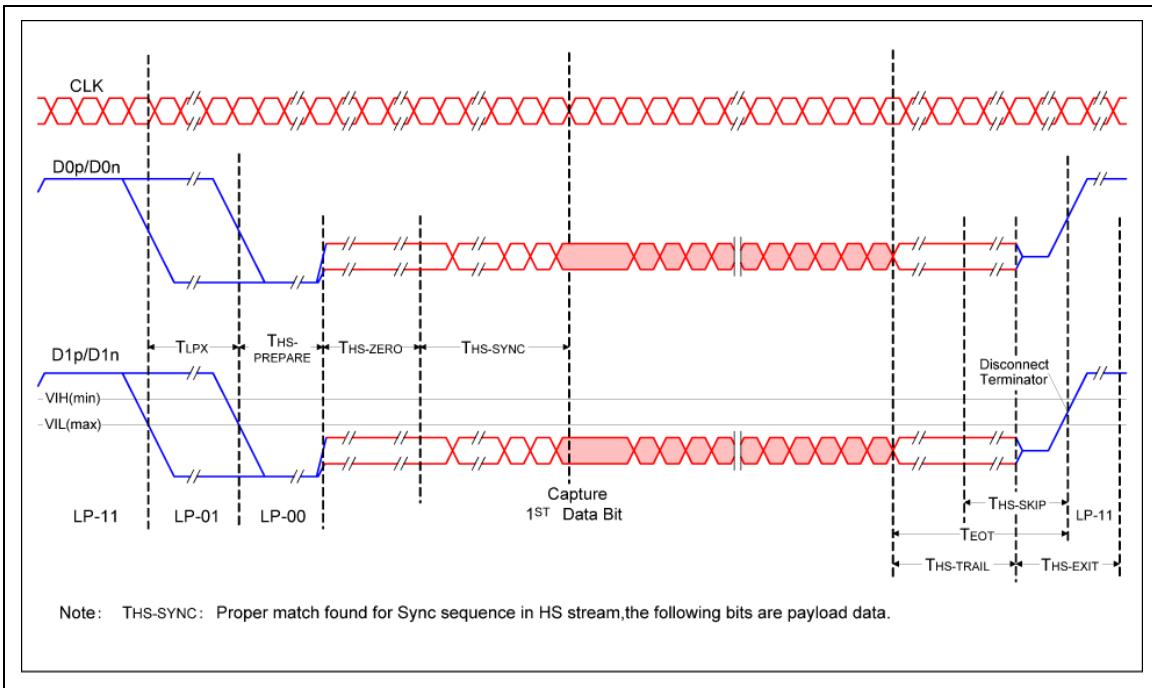


Figure 161 HS Data Transmission in Bursts

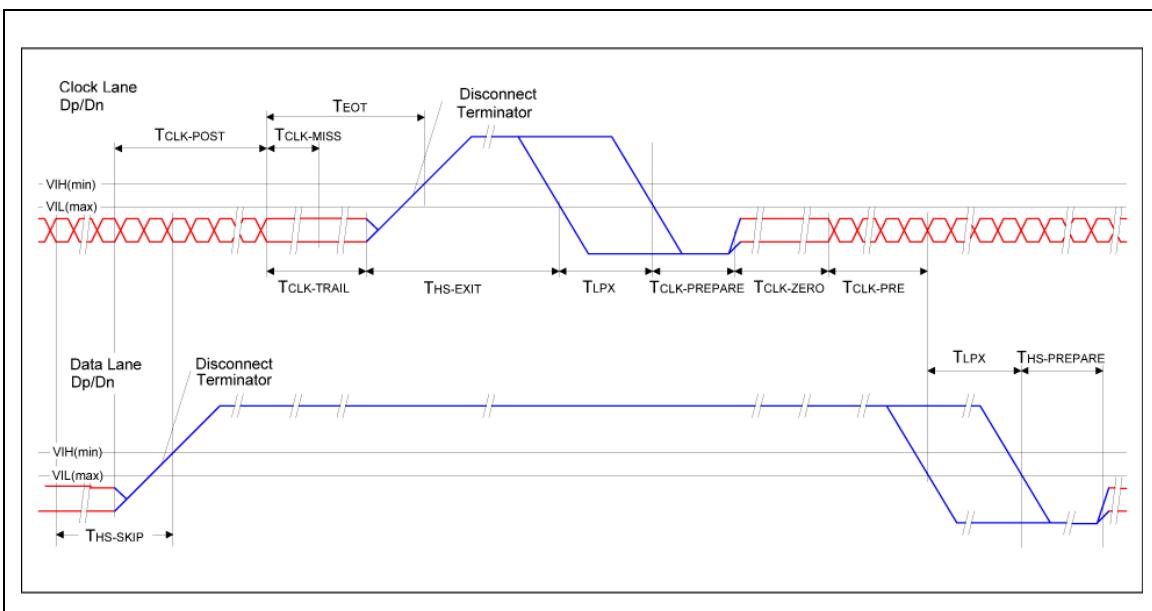


Figure 162 Switching the Clock Lane between Clock Transmission and LP mode

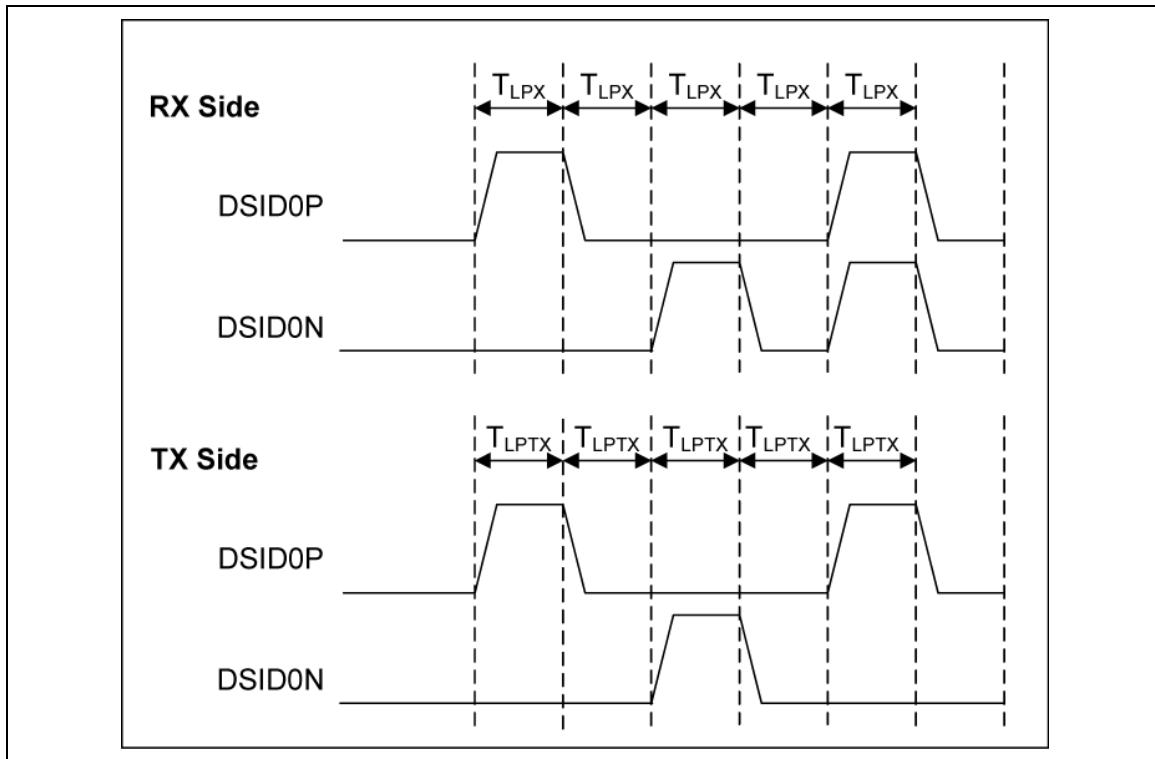


Figure 163 DSI LP mode

MDDI Timing Characteristics

MDDI Receiver Timing Characteristics

(VCI= IOVCC2 = 2.40V ~ 3.30V, IOVCC1= 1.65V ~ 3.30V Ta=-40°C~+85°C) (TBD.)

Table 94

Item	Symbol	Unit	Min.	Typ.	Max.
Data transfer rate (Command mode)	1/tBIT	Mbps	10	—	400
Data transfer rate (Active Refresh mode)	1/tBIT	Mbps	10	—	250
Differential transfer input skew	±tskew-pair-l	ns	—	—	0.05
Data_Stb input skew	±tdiff-skew-l	ns	—	—	0.45*tBIT

MDDI Input Operation

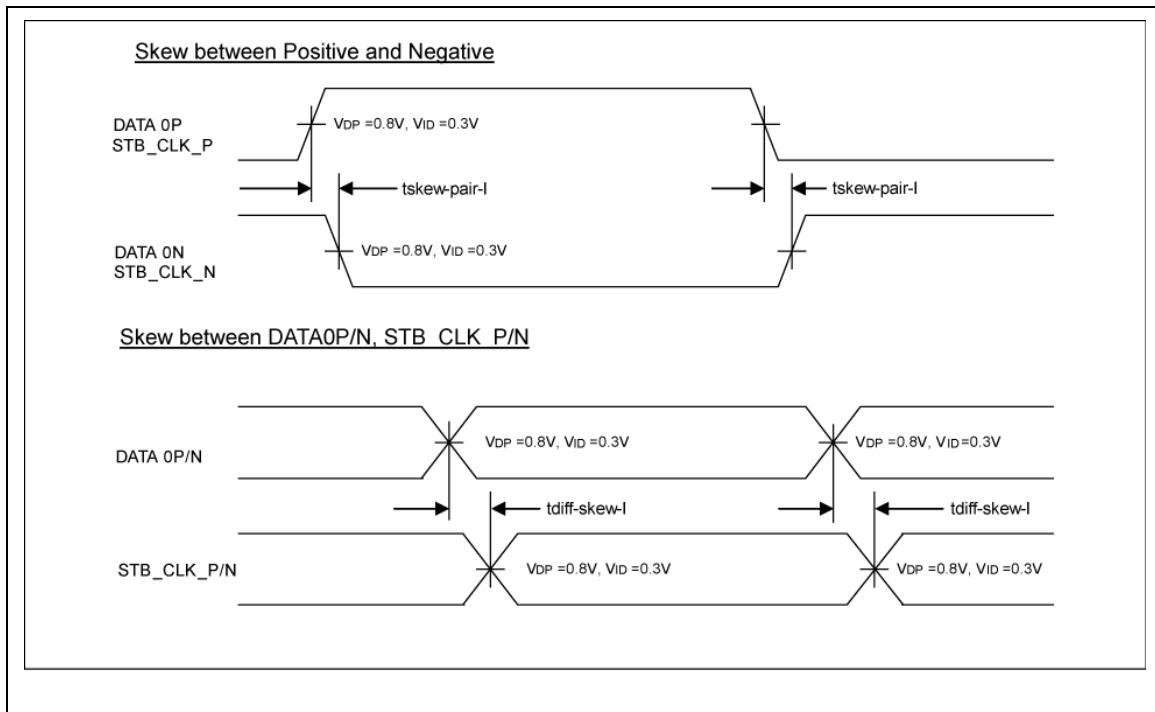


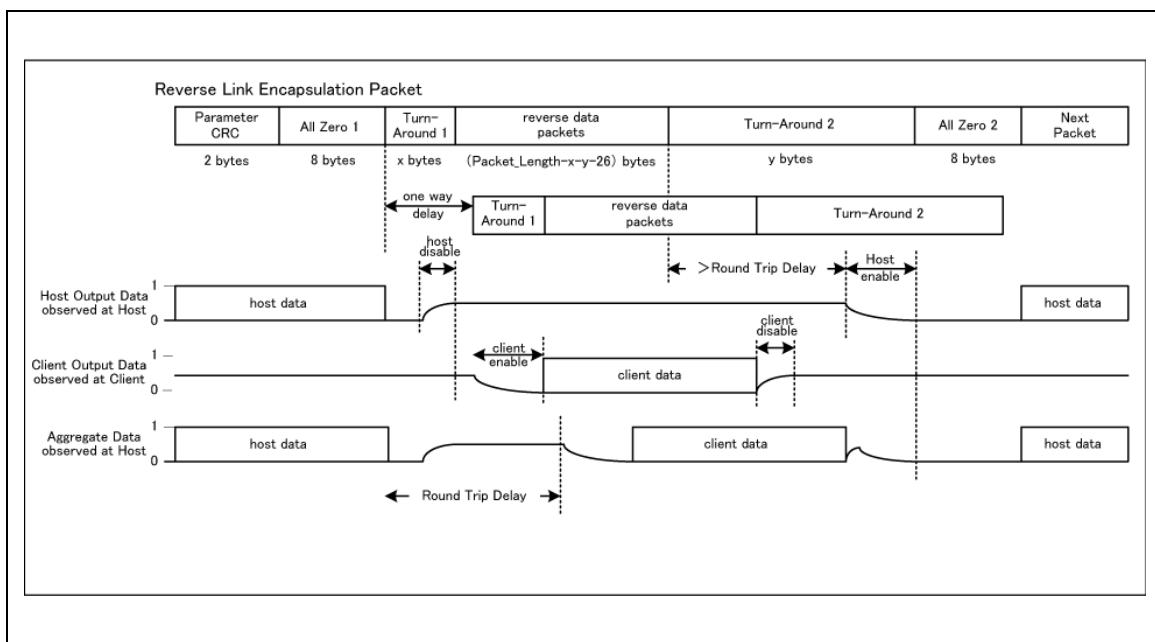
Figure 164 MDDI Input Operation

MDDI Transmitter Timing Characteristics

(VCI= IOVCC2 = 2.40V ~ 3.30V, IOVCC1= 1.65V ~ 3.30V Ta=-40°C~+85°C) (TBD.)

Table 95

Items	Symbol	Unit	Min.	Typ.	Max.
Data transfer rate(Reverse Link)	1/tBIT-Reverse	Mbps	0.15	—	12.5
Client output enable time (Turn Around 1 field)	tclient-enable	ns	0		$16 \times t\text{BIT-Reverse}$
Client output Disable time (Turn Around 2 field)	tclient-disable	ns	0		$16 \times t\text{BIT-Reverse}$

**Figure 165 MDDI Output Operation Overview image**

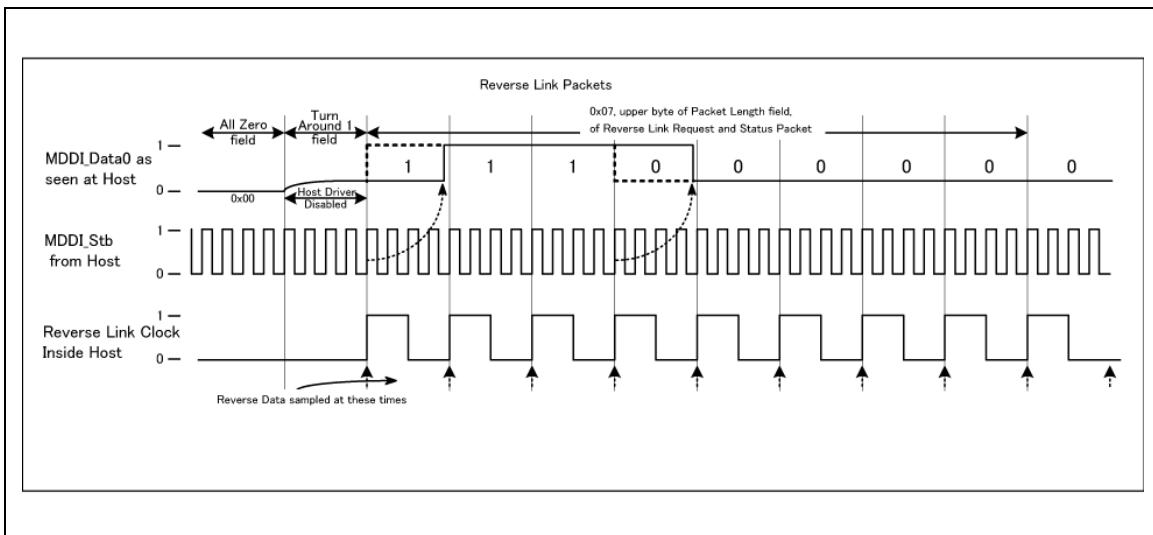


Figure 166 MDDI Output Operation Detail Image (Reverse rate Divisor[7:0]=4h case)

Revision Record

Rev.	Date	Page No	Contents of Modification
0.00	March 29, 2010		First issue
0.01	May 31, 2010	8	Changed: Description of privacy filter Added: "MDDI + TE synchronization signal output" Deleted: Description of outline sharpening function 9 Changed: Description of privacy filter, Interface power supply → Interface and logic power supply, Analog and logic power supply → Analog power supply, VSP-GND → VSP-AGND, VSN-GND → AGND-VSN
		10	Changed: "note 1" → "note 2" (IOVCC2), "13.0V - 20.0V" → "11.4V - 18.3V" (VGH), "-9.0V - -15.0V" → "-7.6V - -13.3V"(VGL)
		11	Changed: WRX/SCL → WRX Deleted: C24P/C24M Corrected: VG1-G480 → G1-G480
		12	Changed: Description of display data transfer, frame frequency, changing interface and mode, name and spec of I2C, number of colors (I2C (Mode 1), MIPI DBI Type C 9 bits (Option 1), MIPI DBI Type C 8 bits (Option 3), MDDI, MDDI Active Refresh Mode) Added: Note on reference chapter
		17	Added: Function of releasing shutdown mode Changed: WRX/SCL → WRX, MIPI DBI Type C and I2C operation → MIPI DBI Type C operation, connection of DOUT Deleted: Description of pin level (CSX, DCX, WRX, RDX)
		18	Deleted: Description of high level and low level (DE)
		19	Changed: Connection of C11P, C11M, C12P, C12M, C13P, C13M, C14P, C14M, "VC2[2:0] and VC3[2:0]" → "VC1[2:0] and VC2[2:0]" Deleted: C24P/C24M Added: "VC1[2:0] and"
		20	Added: Description of omitting stabilizing capacitor Changed: Stabilizing capacitor → Open, Liquid crystal panel → Stabilizing capacitor
		21	Changed: Description and connection of VREFC, VDDTEST, TEST1-4, TESTE, TSC, and VPP1 Added: "or leave open" and description of ITO wiring
		22	Added: Pad arrangement
		23-41	Added: Pad coordinates
		42	Changed: Section "BUMP Arrangement"
		43	Changed: Chip size and alignment mark Deleted: (TBD)
		44	Added: Recommended resistance and connection
		45	Changed: WRX/SCL → WRX
		47	Added: RDX and DB[7:0] (interface)
		49	Changed: DB[7:0] → DB[N:0] (parameter)
		50	Changed: DB[N:0] → DB[7:0] (command)

Rev.	Date	Page No	Contents of Modification
		52	Changed: No → Yes (IM[3:0] = 0100: R61529 implementation of 12bpp color format)
		53	Added: [IM3-0 = 0111]
		66	Added: Description of B3 bit and BGR bit
		69	Corrected: Description of read cycle sequence in figure Changed: Sequences Added: Description of dummy (in figures)
		70	Changed: Sequences Added: Description of get command and read command
		72	Deleted: Description of color formats
		77	Changed: MIPI D-PHY version Deleted: Redundant description of MIPI DCS
		79	Added: soft_reset (in figure)
		82	Added: soft_reset (in figure) and HWRESET (in table)
		83	Added: soft_reset
		95	Changed: 960 lines → 480 lines
		99	Changed: 5 → 6 (04h), 16'h5 → 16'h6 (04h), → 16'h4 (2'hA, 2'hB), - → N byte (2'hC)
		100	Changed: - → 16'h4 (30h), - → 16'h1 (35h and 36h), 5 → 6 (A1h), 16'h5 → 16'h6 (A1h) Deleted: A8h
		101-102	Defined: MCS and Data Type List
		104	Changed: Note 2 → note (in figure)
		105	Added: "Perform Type Handoff Packet" and "Windowless Video Stream Packet"
		107	Changed: Description of Protocol Version[1:0]
		108	Added: Figures of Host-Initiated Wakeup and Client-Initiated Wakeup
		110	Added: Figure of Round-Trip Delay Measurement Timing
		112	Added: Example waveforms of Forward Link Skew Calibration Packet
		114	Added: Description of Reverse Link Flags[7:0] Changed: Description of Reverse Rate Divisor[7:0]
		115	Changed: Description of Reverse Rate Divisor[7:0]
		116	Corrected: Read/Wrote Info[15:0] → Read/Write Info[15:0]
		117	Changed: hClient ID → bClient ID
		118	Added: "(The Pixel Data is packed)" (in [12]) Changed: Description of [11:0]
		119	Deleted: Definition of X Left Edge, Y Top Edge, X Right Edge, and Y Bottom Edge
		120-122	Added: Section "Windowless Video Stream Packet"
		123	Corrected: Protocol Version and Min Protocol Version Changed: (0x17C) → (0x32C) (Pre-calibration Data Rate Capability)

Rev.	Date	Page No	Contents of Modification
	126		Added: (Not used. Returns 0) (in [0] of Interface Type Capability[7:0])
	130		Changed: 0x00 → 0xFFFF
	131-132		Added: Section "Perform Type Handoff Packet"
	132		Changed: Description of "MIPI Command Setting"
	134		Changed: DIN → DOUT
	135		Deleted: Resistors (from figure)
	137-138		Added: Section "Synchronization with Forward Link (TBD)"
	139		Added: "front porch period (FP)" (in description)
			Changed: Table of display timing setting, note
	140		Deleted: Section "16-Bit DPI" Added: "(TBD)" (to title of table)
	142		Added: Section "Setting Example for Display Control Clock in DPI Operation"
	143		Added: Description of connection between host pins and the R61529 pins
	144		Deleted: Figure of 16-bit interface
	147		Changed: 6'h3B → 8'hEF (NL)
	149		Changed: (Bits 5/2/1 Only) → (Bit 5 Only) (0Dh)
	150		Changed: Yes → No (R61529 implementation of A8h)
	151		Changed: Number of parameters (B3h, B8h, C0h, C1h) Deleted: B5h, C2h, C3h, D5h Added: B4h, D1h
	153		Deleted: A8h
	154		Deleted: B5h, C2h, C3h, D5h
	155		Added: IFID (04h)
	157		Added: IFID (A1h) Deleted: A8h
	160		Changed: ID1[15:0] → DDB0[7:0], DDB1[7:0], ID2[15:0] → DDB2[7:0], DDB3[7:0], XXh → 00h (Hex of 1st to 4th parameters), description of 1st and 2nd parameters Added: 5th and 6th parameters, "IFID" Corrected: Dummy parameter Shifted: Note (from p.162) Deleted: Redundant row
	161		Changed: ID1[15:0] → DDB0[7:0], DDB1[7:0], ID2[15:0] → DDB2[7:0], DDB3[7:0], I2C IC → I2C ID Added: 6th parameter and "IFID" Shifted: Note (to p.161)
	162		Changed: XXh → 08h, PLTON → PTION
	163		Shifted: Note (from Flow Chart to Restriction)
	164		Changed: XXh → 00h
	165		Add: Description of reference chapter

Rev.	Date	Page No	Contents of Modification
			Changed: Table Shifted: Note (from p.167)
166			Shifted: Note (to p.166)
167			Changed: X0h → 77h Shifted: Note (from p.169)
168			Shifted: Note (to p.168)
169			Changed: X0h → 00h Shifted: Note (from p.171)
170			Shifted: Note (to p.170)
171			Shifted: Note (from p.173)
172			Shifted: Note (to p.172)
173			Changed: X0h → 00h Shifted: Note (from p.175)
174			Shifted: Note (to p.174)
180			Corrected: set_display_off → enter_invert_mode
183			Changed: Hex of 1st to 4th parameters, SC[9:0] → SC[8:0], EC[9:0] → EC[8:0], note
184			Changed: SC[9:0] → SC[8:0], EC[9:0] → EC[8:0], note
185			Changed: Hex of 1st to 4th parameters, SP[9:0] → SP[8:0], EP[9:0] → EP[8:0], note
186			Changed: SP[9:0] → SP[8:0], EP[9:0] → EP[8:0], note
189			Shifted: Note (from Flow Chart to Restriction)
190			Changed: Hex of 1st to 4th parameters, SR[9:0] → SR[8:0], ER[9:0] → ER[8:0], and figure
191			Added: Flow chart
193			Changed: Hex and formula for V-Blanking Corrected: Note 2
195			Changed: "-" → B7 (D7 in Video mode) Added: description of relationship between frame memory data and display data
196			Added: description of relationship between frame memory data and display data
197			Added: description of relationship between frame memory data and display data, row of restriction Changed: Host → Frame Memory (in figure of bit D3)
198			Added: B3
199-200			Changed: Figures
204			Changed: XXh → 77h
206			Shifted: Note (from Flow Chart to Restriction)
207			Changed: Hex of 1st and 2nd parameters, STS[9:0] → STS[8:0], description of Tearing Effect output signal
208			Changed: Hex of 1st and 2nd parameters, GTS[9:0] → GTS[8:0] Shifted: Note (from Flow Chart to Restriction)

Rev.	Date	Page No	Contents of Modification
			Changed: ID1[15:0] → DDB0[7:0], DDB1[7:0], ID2[15:0] → DDB2[7:0], DDB3[7:0], XXh → 00h (Hex of 1st to 6th parameters) Shifted: Note (from p.212)
209			
210			Changed: ID1[15:0] → DDB0[7:0], DDB1[7:0], ID2[15:0] → DDB2[7:0], DDB3[7:0] Added: (I2C ID Code) Shifted: Note (to p.211)
211			Deleted: Section "read_DDB_continue: A8h" Changed: MCAP[1:0] → MCAP[2:0], table, and restriction
212			Added: Description of accessing DSTB
213			Changed: Hex of 1st to 4th parameters Added: IN_TEON, DFM[1] Deleted: DENC[2:0]
214			Added: Description of IN_TEON, restriction
215			Added: "when DBI Type B is chosen" Changed: XXh → 00h, DPI signal → Setting inhibited (in table)
216			Deleted: Section "Read Checksum and ECC Error Count (B5h) Changed: Hex of 1st and 2nd parameters, DB0 of 2nd parameter
217			Added: Restriction
218			Deleted: Section "MDDI Control (B7h)" Changed: Hex of 1st to 15th parameters
219			Added: Rows of 17th to 20th parameters Changed: Note (D0 → DB0, D1 → DB1)
225			Corrected: LMTW → LLMTW
228			Corrected: LLMTW*[5:0] → LLMTW*[7:0]
233			Added: Restriction
234			Added: PWMON, description of change in LEDPWME Deleted: Description of change in PWMWM setting Changed: Note 1 ("+" → "or", "+" → "and")
235			Added: Description of PWMDIV[7:0] and restriction Deleted: LEDPWMPOL
236			Shifted: Note (from Flow Chart to Restriction)
237			Changed: Hex and DB0 of 3rd and 4th parameters and DB5 of 4th parameter Shifted: Note (from p.240)
238			Changed: Flow Chart Shifted: Note (to p.239)
239			Changed: Hex of 1st to 8th parameters, NL[0] → 1, 0 → 1 (DB4 of 4th parameter) Added: NL[8:6]
240			Added: Description of reference section (in SS)
241			Changed: NL[5:0] → NL[8:1], description of the number of lines to driver the LCD, table of NL[8:1], table of SCN[5:0] (SM=1, GS=1)

Rev.	Date	Page No	Contents of Modification
	242		Changed: Tables of SCN (SM=1, GS=0), BLV, BLS (negative polarity), and PTV
	243		Deleted: Description of PTDC
	244		Added: "during DPI operation" (in description of PCDIVH[3:0]/PCDIVL[3:0]), restriction
	245		Changed: Hex of 1st to 5th parameters, DIV0[3:0] → DIV[3:0], RTN0[5:0] → RTN[5:0], BP0[7:0] → BP[7:0], FP0[7:0] → FP[7:0], PNSET0[2:0] → PNSET, description of division ratio, tables of DIV[3:0] and RTN[5:0] Deleted: Display Timing for Partial Mode (C2h)", "Display Timing Setting for Idle Mode (C3h)", parameter tables of C2h and C3h commands, description of DPI_OFF
	246		Changed: FPn[7:0] → FP[7:0], BPn[7:0] → BP[7:0]
	247		Changed: PNSET0[1:0] → PNSET, tables of PNSET and LINEINV0
	249		Added: Note
	250		Deleted: Row of 5th parameter Changed: Row of 3rd and 4th parameters, Hex of 1st, 3rd, and 4th parameters Added: NOWB[2:0]
	251		Corrected: Note Added: Figure
	252		Deleted: Figure of basic operation of source output 2 Added: "and VCL" (in SEQVCIL[3:0]), description of clk (in SEQGND[3:0] and SEQVCIL[3:0]), restriction Changed: Figure of basic operation of source output 1
	253		Changed: Hex of 1st parameter Added: Restriction
	254		Changed: Hex of 1st to 16th parameters
	255		Changed: Hex of 17th to 24th parameters Added: Restriction
	256		Changed: Hex of 1st to 16th parameters
	257		Changed: Hex of 17th to 24th parameters Added: Restriction
	258		Changed: Hex of 1st to 16th parameters
	259		Changed: Hex of 17th to 24th parameters Added: Restriction
	260		Changed: Contents and/or hex of 1st-7th, 9th-10th, 12th-16th parameters
	261		Corrected: Description of DC1[1:0] and DC1M[1:0] Deleted: Description of VLMT4[2:0]
	262		Changed: VC3[2:0] → VC1[2:0], description and tables of VC1[2:0] (former VC3[2:0]) and VC2[2:0] Added: Description of BT[1:0] and restriction
	263		Shifted: Section "VCOM Setting (D1h)" (from p.272) Changed: D5h → D1h, 1 → 0 (DB2 of command), hex of 1st to 4th parameters Corrected: WCVCM → WCVDC
	269		Added: Table of VDC[7:0] (8'hC0-8'FF) Deleted: Description of inhibited setting

Rev.	Date	Page No	Contents of Modification
		270	Deleted: Section "Power Setting for Normal Mode (D3h)", Redundant description of VERIFLGER and VERIFLGWR
		271	Deleted: Note on TEM[0] Added: Restriction
		272	Changed: Hex of 1st to 4th parameters Added: Description of information from display module, restriction Deleted: Description of A8h.
		273	Changed: Hex of 1st parameter, description of LD[7:0], load control commands
		274	Deleted: Sections "Test Mode 13 (E3h)" to "Test Mode 21 (FEh)"
		276	Deleted: VREFM, C24P, C24M Changed: VPLVL, VNLVL, VGH, C21P, C22P, C23P
		277	Changed: 13F → 013Fh, 1DF → 01DFh
		280, 282	Added: "and MDDI"
		283	Added: Description and figure of internal reference clock generating function
		284	Changed: 320 → 480 (in the lower right box)
		285	Added: "of Display Timing Setting command"
		286	Deleted: Note on SDT register setting (in figure)
		291	Changed: THREW[4:0] → THREWx[4:0]
		292	Changed: PITCHW[3:0] → PITCHWx[3:0], one eighth → one half
		293	Changed: PITCHW[3:0] → PITCHWx[3:0], CGAPW[4:0] → CGAPWx[4:0]
		294	Changed: ULMTW[7:0] → ULMTWx[7:0], LLMTW[7:0] → LLMTWx[7:0]
		295	Added: TBL7 and 255
		296	Changed: COEFK[4:0] → COEFKx[4:0]
		297	Changed: Table of PWM DIV[7:0] (8'h00)
		298	Deleted: Description of clock cycle in MIPI DSI operation (using 2 lanes)
		302	Changed: Sequence and description
		303	Added: Description of NVM auto load (lower) Changed: Description of orders to turn on and off power
		304	Changed: Description of orders to turn on and off power
		305	Changed: Description of the 3rd paragraph
		306	Changed: Figure
		308	Changed: Tables
		314	Deleted: VCMREV (from section name)
		315	Deleted: (3) VCL, (9) C24P/M Changed: (12) VSP → (12) VPLVL, (13) VSN → (13) VNLVL
		316	Deleted: (3) VCL, (9) C24P/M, row of 16V Changed: (12) VSP → (12) VPLVL, (13) VSN → (13) VNLVL Shifted: 6)C21P/N, (7) C22P/M, (8) C23P/M (to row of 10V)

Rev.	Date	Page No	Contents of Modification
			Added: Description of stabilizing capacitors
317			Changed: Voltage setting diagram
318			Added: Voltage setting tables
321			Changed: xxkk-bit NVM → 2k-bit NVM
324			Changed: 864-line drive → 480-line drive, average output variance, note no. (3-6)
325			Changed: Note no.
326			Shifted: Section "Note to Electrical Characteristics" (from p.352) Deleted: Former note 3
328, 330			Added: Note
331			Added: Note Changed: Table of output voltage range
333			Added: Test condition of liquid crystal driver output characteristics, note on DC/AC characteristics Changed:- → 30 (in table), S1440 → S960, xxkΩ → 10kΩ, xxpF → 15pF (in figures)
334			Added: Note Changed: tcs, tcsf, twc, twrh, twrl, twds, twdh Deleted: Spec of rise/fall time
335			Changed: tcs, tcsf, twc, twrh, twrl, twdh Deleted: Spec of rise/fall time
336			Changed: tcs, tcsf, twc, twrh, twrl Deleted: Spec of rise/fall time
338			Changed: Chip select setup time → Rise/fall time
339			Changed: Min. of all items Deleted: Spec of rise/fall time
343			Changed: 14MHz → 14MHz
349			Changed: 2h case → 4h case Shifted: Section "Note to Electrical Characteristics" (to p.329)
0.02	August 4, 2010	8	Changed: I ² C → I ² C Deleted: Description of privacy filter function
		9	Changed: VGH-GND → VGH-AGND, GND-VGL → AGND-VGL (gate driver power supply) Deleted: Description of privacy filter function
		10	Changed: I ² C → I ² C, 18.3V → 17.8V (VGH), -13.3V → -12.8V (VGL)
		11	Changed: I ² C → I ² C Added: TSC, AGNDDUM1-56, VPP1, TESTO1-TESTO16, TESTE, TEST1-4, VDDTEST, VREFD, VREFM, VREF, VREFC, TSC Deleted: VCI (internal logic power supply regulator), GNDDUMxx, IOVCC1DUMx, AGNDDUMxx, DGNDDMYxx
		12	Changed: Number of available colors (IM[3:0] = 0000, 0001, 1001), I ² C → I ² C Added: Note numbers ("(Note 3)", "(Note 4)"), note of DPI (note 2), notes 3 and 4
		13	Changed: WRX/SCL → WRX

Rev.	Date	Page No	Contents of Modification
	14		Added: Description of MIPI DSI Video Mode and MDDI Active Refresh Mode
	15		Added: Description of gate driver circuit, gate output, scan
	16		Changed: I ² C → I ² C (IM0-3) Added: Description of TE
	17		Changed: I ² C → I ² C (DIN) Added: "and I ² C" (WRX)
	18		Changed: IOVCC1 → IOVCC1 or GND (VSYNC, HSYNC, DE) Added: Description of signal polarity and reference section (VSYNC, HSYNC, DE, PCLK) Deleted: Low active (VSYNC, HSYNC)
	19		Changed: VCI → GND (VGH)
	20		Added: TESTO1-TESTO16
	21		Changed: AGNDDUM1-xx → AGNDDUM1-56, - → Open (AGNDDUM1-56), GND → AGND (VPP1), description of connection with GND (TESTE) Deleted: DGNDDMY1-xx, DUMMYR1-4
	22-23		Added: Pad arrangement (TBD)
	44		Changed: 230 mm → 230 um (chip thickness) Deleted: "Alignment mark coordinate"
	45-46		Changed: Resistance, connection
	69		Changed: WRX/SCL → WRX
	70		Changed: DB0SDI → DIN, DB1SDO → DOUT (Option 1: R61529), Data → DOUT data (read cycle sequence) Deleted: "via DIN" (read cycle sequence)
	72		Changed: Sequences (Options 1 and 3) Deleted: Description of get command, read command, Read Mode In command (Option 1)
	76		Changed: I ² C → I ² C, WRX/SCL → WRX
	77-78		Changed: I ² C → I ² C
	79		Changed: I ² C → I ² C Added: 1000 (IM3-0)
	87		Added: Description and figure of Tearing Report
	95		Changed: Min., Typ., Max. (table) Deleted: Note 3 (table)
	96		Changed: Min. (table)
	102		Changed: - → 16'h1 (3Ah), - → N byte (3Ch), - → 16'h2 (44h)
	103		Changed: Low Power Mode Control → Display Mode (B4h), Source/Gate Driving Timing Control → Source/Gate Driving Timing Setting (C4h), Display Control Setting → Test Mode 2 (C7h), Power Setting → Power Setting (Charge Pump Setting (D0h) Added: B5h, C3h, CCh Deleted: D3h
	104		Changed: set_write_DDB_control → set_DDB_write_control (E1h), Yes → No (14'h of F5h and F6h)

Rev.	Date	Page No	Contents of Modification
			Added: D6h, D7h, D8h, D9h, DAh, E4h, E5h, E6h, E7h, F3h, F8h, FAh, FCh, FDh, FEh
105			Added: "Command Mode", "Video Mode" Deleted: "MIPI Spec."
112			Changed: Description of Measurement Period, All Zero (exchanged)
119			Added: "Read/Write Flag" ([15:14])
120			Added: Description of X Start, Y Start, Pixel Count
121			Added: Note 2 (table)
123			Changed: the display attributes field → the Pixel Data Attributes field
124			Changed: [15] → [15:14] (Pixel Data Attributes[15:0]) Deleted: Description of [14] (Pixel Data Attributes[15:0])
126			Changed: 0x01 → 0x02 (Protocol Version), 0x32C → 0x32 (Pre-calibration Data Rate Capability), 0x00 → 0x01 (Interface Type Capability)
127			Added: 0x4C0100 (Client Feature Capability) Deleted: TBD (Client Feature Capability)
130			Changed: keyboard → keyboard device ([12])
131			Changed: (Available. Returns 1) → (Not used. Returns 0) ([18])
139			Changed: 16-/8-bit bus interface → I ² C, MIPI DBI Type C
140			Deleted: "TBD" (section name)
141			Added: Description of disregard for packets (state 5)
142			Added: Section "Active Refresh Mode"
143			Changed: BP → VBP, VD → NL (figure)
144			Changed: - → 8 (table), 14 MHz → 10.7 MHz (note), 2'h6 → 3'h6, I2C → I2C
145			Changed: 2'h7 → 3'h7, I2C → I ² C
146			Changed: DIVl[3:0] → DIV[3:0], DIVl[3:0] → DIVn[3:0]
147			Changed: Yes → No, 3'h5 → - (16bpp (65,536-color Configuration 2)) Added: "24bpp and 18bpp"
149			Deleted: Description and note of 16bpp
150			Changed: WRX/SCL → WRX
153			Changed: (Bits 6/5/4/3/2 Only) → (Bits 6/5/4/2 Only) (0Ah)
155			Changed: Low Power Mode Control → Display Mode (B4h), Source/Gate Driving Timing Control → Source/Gate Driving Timing Setting (C4h), Display Control Setting → Test Mode 2 (C7h), Power Setting → Power Setting (Charge Pump Setting (D0h)) Added: B5h, C3h, CCh, D0h, D6h, D7h, D8h, D9h, DAh Deleted: D3h
156			Changed: set_write_DDB_control → set_DDB_write_control (E1h) Added: E4h, E5h, E6h, E7h, F3h, F8h, FAh, FCh, FDH, FEh
158			Deleted: Note of EFh command
159			Changed: Source/Gate Driving Timing Control → Source/Gate Driving Timing Setting (C4h), Display Control Setting → Test Mode 2 (C7h)

Rev.	Date	Page No	Contents of Modification
			Added: B4h, B5h, C3h, CCh, D1h, D6h, D7h, D8h, D9h, DAh Deleted: D3h
160			Changed: set_write_DDB_control → set_DDB_write_control (E1h) Added: E4h, E5h, E6h, E7h, F3h, F8h, FAh, FCh, FDh, FEh, "(Note)", note
164			Added: Description of frame memory
165			Changed: "State & Command Sequence" → "State Transition Diagram"
166			Changed: 00h → XXh (1st to 5th parameters) Added: I ² C ID code
168			Changed: 08h → XXh (1st parameter)
170			Changed: 00h → XXh (1st parameter)
173			Changed: 77h → XXh (1st parameter), MDDI-Video → MDDI Active Refresh, I ² C → I ² C
175, 177, 179			Changed: 00h → X0h (1st parameter)
181, 185-188			Added: Description of frame memory
189			Changed: 00h → 0Xh (1st, 3rd parameters), 00h → XXh (2nd parameter), 3Fh → XXh (4th parameter)
191			Changed: 00h → 0Xh (1st parameter), 00h → XXh (2nd parameter), 01h → 0Xh (3rd parameter), DFh → XXh (4th parameter)
193, 195			Changed: 000h…3FFh → XXXh (all parameters)
205-206			Added: Condition of C0h command
208			Deleted: Description of grayscale levels, power consumption reduction
210			Changed: 77h → XXh, MDDI Video Mode → MDDI Active Refresh Mode, I ² C → I ² C
211			Changed: 1st parameter → 1st pixel data, Nth parameter → Nth pixel data
213-214			Changed: 00h → 0Xh (1st parameter), 00h → XXh (2nd parameter)
215			Changed: 00h → XXh (Dummy parameter, 1st-5th parameters), EEC[7:0] → 1 (6th parameter) Added: I ² C ID code, FFh
216			Added: I ² C ID code
217			Changed: 03h → 0Xh, table of MCAP[2:0] (3'b100, 3'b101-111) Added: X = Don't care
218			Changed: 00h → 0Xh Added: X = Don't care
219			Changed: 00h → 0Xh (1st parameter), 00h → XXh (2nd, 4th parameters)
220			Added: X = Don't care
221			Changed: Display Mode and Frame Memory Write Mode → Display Mode, 1 → 0 (DB0), I ² C → I ² C, Standby mode → Sleep mode, tables of display mode Added: X = Don't care
222			Added: Section "Read Checksum and ECC Error Count (B5h)"

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	223		Changed: 51h → 5Xh (1st parameter), 83h → X3h (2nd parameter), 0.785 → 14.0 (table)
	224		Changed: All min. and max. Added: X = Don't care
	225		Added: Section "MDDI Control (B7h)"
	226		Changed: 00h → 0Xh (1st parameter), 0Fh → XXh (2nd-3rd parameters), FFh → XXh (4th, 5th parameters), C8h → XXh (6th-7th parameters), C2h → 0Xh (8th parameter), 18h → XXh (9th parameter), 10h → XXh (10th, 11th parameters), 37h → XXh (12th parameter), 5Ah → XXh (13th parameter), 87h → XXh (14th parameter), BEh → XXh (15th parameter), 00h → XXh, 0 → TBL[7:0] (16th parameter)
	227		Deleted: Description of change in BLCM value (BLCM)
	240		Added: TBL7[7:0]
	241		Added: X = Don't care
	242		Changed: 00h → 0Xh (1st parameter), 00h → XXh (2nd-4th parameters)
	243		Added: X = Don't care
	244		Changed: 00h → XXh (1st parameter)
	247		Changed: 00h → XXh (1st, 6th, 8th parameters), DFh → XXh (2nd parameter), 40h → XXh (3rd parameter), 10h → 1Xh (4th parameter), 00h → XXh (5th, 7th parameters)
	249		Changed: NL[5:0] → NL[8:1] (table of SCN[5:0])
	252		Changed: PCLK (DM=1, DPI) → PCLK Added: X = Don't care
	253		Changed: 07h → 0Xh (1st parameter), 27h → XXh (2nd parameter), 08h → XXh (3rd, 4th parameters), 00h → XXh (5th parameter), $1/(14\text{MHz}/12) \approx 0.85\mu\text{s} = 1 \text{ clk.} \rightarrow 1/(14\text{MHz}/12) = 0.85\mu\text{s} = 1 \text{ clk.}$
	257		Added: X = Don't care
	258		Added: Section "Test Mode 1 (C3h)"
	259		Changed: 11h → XXh (1st parameter), 04h → 0Xh (3rd, 4th parameters), table of NOWB[2:0] (3'h1 to 3'h7)
	260		Changed: Table of NOW[2:0] (3'h0 to 3'h7)
	261		Added: X = Don't care
	262		Changed: Panel Driving Setting → DPI Polarity Control (table) Added: X = Don't care
	263		Added: Section "Test Mode 2 (C7h)"
	264		Changed: 00h → XXh (1st, 13th parameters), 10h → XXh (2nd, 14th parameter), 20h → XXh (3rd, 15th parameters), 30h → XXh (4th, 16th parameter), 40h → XXh (5th parameter), 50h → XXh (6th parameter), 48h → XXh (7th parameter), 38h → XXh (8th parameter), 28h → XXh (9th parameter), 15h → XXh (10th parameter), 08h → XXh (11th parameter), 01h → XXh (12th parameter)
	265		Changed: 40h → XXh (17th parameter), 50h → XXh (18th parameter), 48h → XXh (19th parameter), 38h → XXh (20th parameter), 28h → XXh (21st parameter), 15h → XXh (22nd parameter), 08h → XXh (23rd parameter), 01h → XXh (24th parameter) Added: Description of C0h command and 36h command, X = Don't care

Rev.	Date	Page No	Contents of Modification
			Deleted: Description of red grayscale
266			Changed: 00h → XXh (1st, 13th parameters), 10h → XXh (2nd, 14th parameter), 20h → XXh (3rd, 15th parameters), 30h → XXh (4th, 16th parameter), 40h → XXh (5th parameter), 50h → XXh (6th parameter), 48h → XXh (7th parameter), 38h → XXh (8th parameter), 28h → XXh (9th parameter), 15h → XXh (10th parameter), 08h → XXh (11th parameter), 01h → XXh (12th parameter)
267			Changed: 40h → XXh (17th parameter), 50h → XXh (18th parameter), 48h → XXh (19th parameter), 38h → XXh (20th parameter), 28h → XXh (21st parameter), 15h → XXh (22nd parameter), 08h → XXh (23rd parameter), 01h → XXh (24th parameter) Added: X = Don't care
268			Changed: 00h → XXh (1st, 13th parameters), 10h → XXh (2nd, 14th parameter), 20h → XXh (3rd, 15th parameters), 30h → XXh (4th, 16th parameter), 40h → XXh (5th parameter), 50h → XXh (6th parameter), 48h → XXh (7th parameter), 38h → XXh (8th parameter), 28h → XXh (9th parameter), 15h → XXh (10th parameter), 08h → XXh (11th parameter), 01h → XXh (12th parameter)
269			Changed: 40h → XXh (17th parameter), 50h → XXh (18th parameter), 48h → XXh (19th parameter), 38h → XXh (20th parameter), 28h → XXh (21st parameter), 15h → XXh (22nd parameter), 08h → XXh (23rd parameter), 01h → XXh (24th parameter) Added: Description of C0h command and 36h command, X = Don't care, section "Test Mode 3 (CCh)" Deleted: Description of blue grayscale
270			Changed: 96h → XXh (1st parameter), 06h → 0Xh (2nd parameter), 10h → X0h (4th parameter), 0 → 1 (DB2 of 6th parameter), 1 → 0 (DB7 of 3rd, 4th parameters)
272			Changed: VCI3 → VCI1 (description of VC1[2:0]) Added: X = Don't care
273			Changed: 00h → 0Xh, 00h → XXh (2nd, 3rd parameters), 80h → XXh (4th parameter)
275			Changed: $\geq 0.3V$ → $\leq -0.3V$
279			Added: X = Don't care
280			Added: Section "Test Mode 4 (D6h)"
281			Added: Section "Test Mode 5 (D7h)"
282			Added: Section "Test Mode 6 (D8h)"
283			Added: Sections "Test Mode 7 (D9h)", "Test Mode 8 (DAh)"
284			Changed: 00h → 0Xh (1st parameter), 00h → X0h (2nd parameter), 00h → XXh (3rd parameter)
285			Added: X = Don't care
286			Changed: 00h → 0Xh (1st parameter), 00h → XXh (2nd-6th parameter) Added: X = Don't care
287			Changed: 1 → LD[6], C0h → XXh, load control commands in NVM load operation Added: X = Don't care, restriction
288			Added: Sections "Test Mode 9 (E4h)", "Test Mode 10 (E5h)"
289			Added: Sections "Test Mode 11 (E6h)", "Test Mode 12 (E7h)"
290			Changed: DBI → MIPI DBI Type C

Rev.	Date	Page No	Contents of Modification
			Added: Section "Test Mode 13 (F3h), X = Don't care, restriction (F5h)
291			Added: X = Don't care, restriction, sections "Test Mode 14 (F8h)", "Test Mode 15 (FAh)"
292			Added: Section "Test Mode 16 (FCh)"
293			Added: Section "Test Mode 17 (FDh)"
294			Added: Section "Test Mode 18 (FEh)"
296			Added: IOVCC1 (DOUT), note
315			Changed: (TBD) → 255 (table setting value)
317			Deleted: Description and table of setting applied to MIPI DPI, section "Privacy Filter (TBD)"
318			Changed: Definition of display modes (figure)
321			Changed: (IOVCC1, IOVCC2 → VCI) → (VCI → IOVCC1, IOVCC2) (power off) Added: Notes (1)-(3)
322			Changed: (IOVCC1, IOVCC2 → VCI) → (VCI → IOVCC1, IOVCC2) (power off)
323			Added: Notes on calculation of wait time
332			Changed: Figure
336			Changed: -(VCI2x2) + VCL → -(VCI2x2) - VCL
337			Changed: Setting inhibited (2'h0)
340			Added: Section "Hardware Reset during Display Operation"
342			Added: List of command stored into NVM
343			Added: Description and table of data load
344			Changed: (MCAP[1:0] = 2'b00) → (MCAP[2:0] = 3'b011), NVM write data set (initial setting)
346			Added: " I_{OPN} ", mA, "IM3-0='0111', "-", "TBD", "5" (I_{OPN}) Deleted: "when DPI is selected" (I_{OPN})
347			Changed: 4 → 5 (I_{DST3}) Added: Test conditions of I_{CIN}
349			Changed: WRX/SCL → WRX
351			Changed: Data0P/M → Data0P/N, STB_CLK_P/M → STB_CLKP/N
352			Changed: STB_CLK_P → STB_CLKP, STB_CLK_N → STB_CLKN Deleted: Data1P, DATA1N
354			Changed: 7.6V → 11.4V (VGH), 30.0V → 28.0V (voltage between VGH and VGL)
363			Changed: I2C → I ² C

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