Digital Circuits and Systems Lab

Laboratory report submitted for the partial fulfillment
of the requirements for the degree of

Bachelor of Technology
in
Communication and Computer Engineering

by

Anushrut - Roll No. 17UCC072

Course Coordinator
Dr. Kusum Lata

Department of Electronics and Communication Engineering
The LNM Institute of Information Technology, Jaipur

October 2018

Contents

Chapter *6*

Experiment - 6

6.1 Name of the Experiments

Design D latch, JK flip flop, RS flip flop and T flip flop using behavioral and structural modeling.

6.2 Theory

A D latch is one of the basic components of sequential circuits which can store a bit of data. It works on the principle of level trigger and works like an open gate for Enable = 1 and memory hold for Enable = 0.

A RS Flip Flop is a simple memory block based on the principle of edge trigger and activates only with either a rising or falling edge of the clock and can hold 1 bit of data.

A JK Flip Flop is an upgraded RS Flip Flop with an addition stage of gates to get around the invalid conditions of an RS Flip Flop.

A T Flip Flop is a special case of JK flip flop where the input is connected with both J and K and hence work as a toggle flip flip with clock.

6.3 Coding Techniques used

6.3.1 Data flow modeling

Dataflow Modeling includes declaration of a target signal using logical events occurring on the particular signal. Dataflow Modeling is primarily expressed using signal assignment statements. This modeling is shown by implementing a D Latch.

6.3.2 Structural modeling

Structural Modeling is the set of interconnected components. That is, it describes the structure. The visible components are instantiated in the declarative part of the architecture body while the declared components are instantiated with their respective interface ports in the statement part of the architecture body. This modeling is shown by implementing a JK Flip Flop.

6.3.3 Behavioral modeling by using If statement

Behavioral Modeling deals with the functionality of an entity. Here, the set of statements are executed sequentially in a specified order, mainly specified within a process statement. The process statement is itself a concurrent statement but inside it lies a set of statements which are all sequential in nature. This modeling is shown by implementing a D Flip Flop, RS Flip Flop and T Flip Flop.

6.4 Simulation and Results

6.4.1 Synchronous D latch using dataflow modeling.

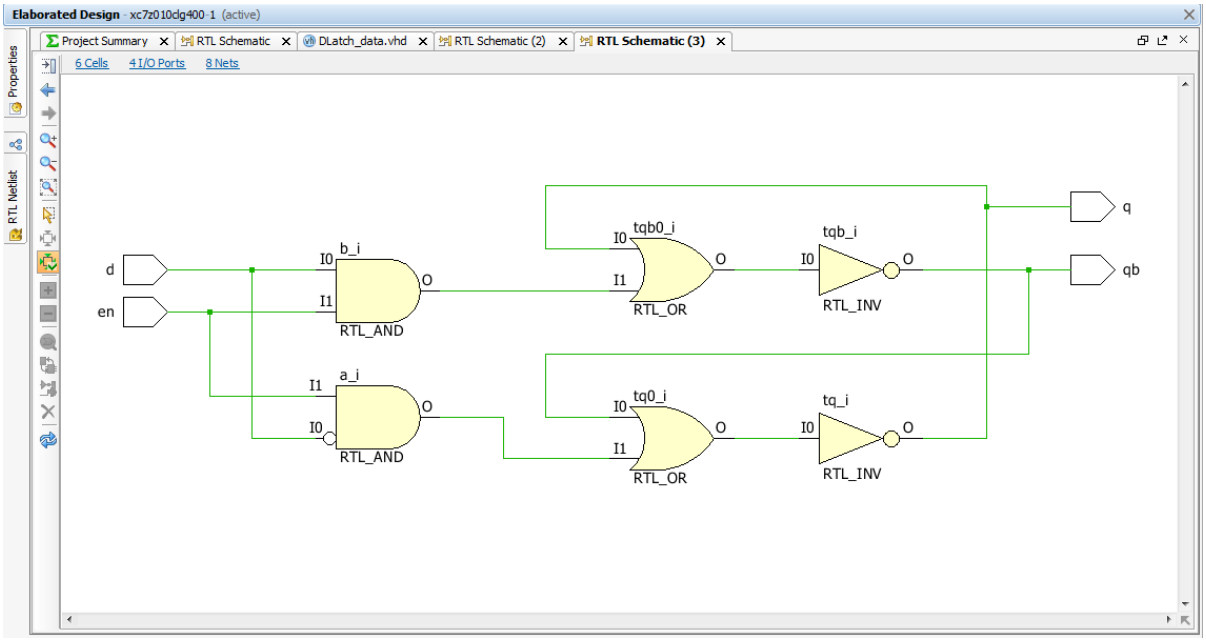

Figure 6.1 Schematic of implementing a synchronous D latch using dataflow modeling.

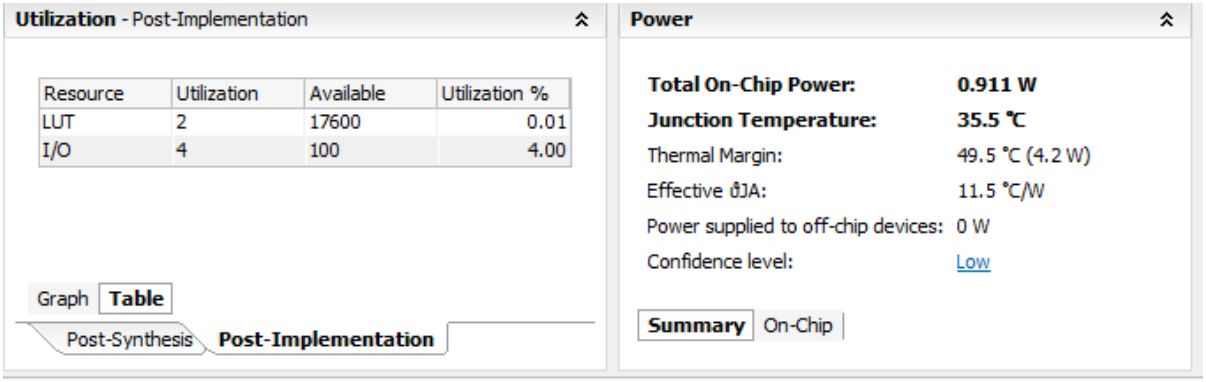

Figure 6.2 Project Summary of implementing a synchronous D latch using dataflow modeling.

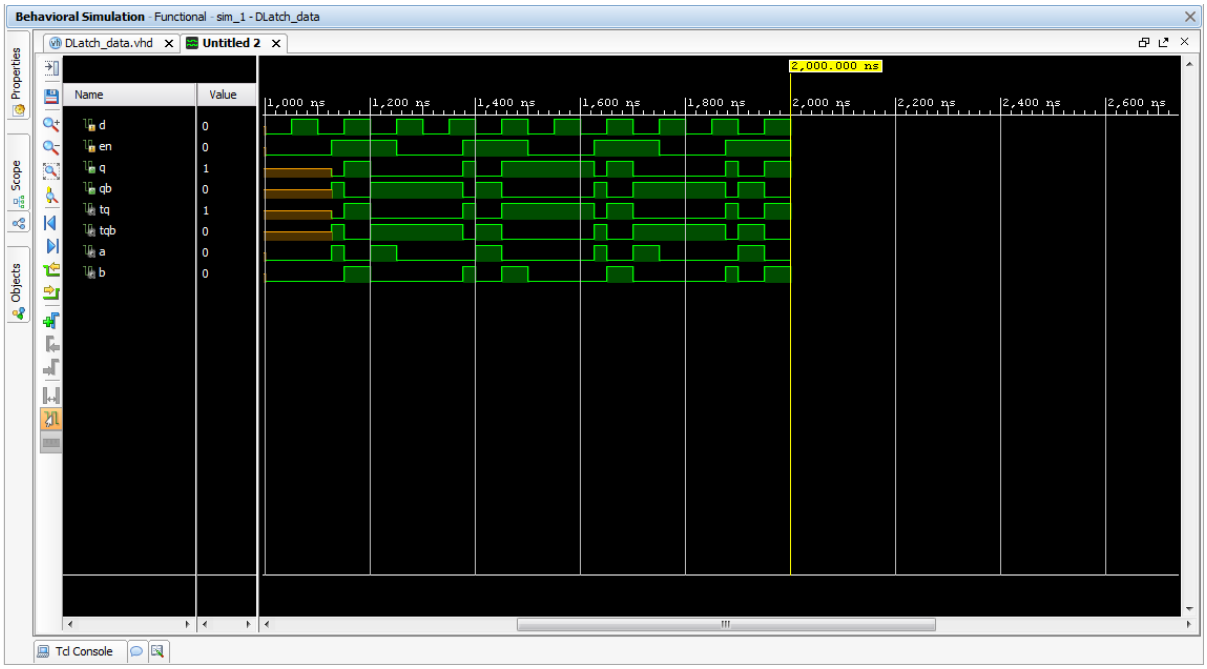

Figure 6.3 Simulation of implementing a synchronous D latch using dataflow modeling.

6.4.2 Synchronous D flip flop using behavioral modeling.

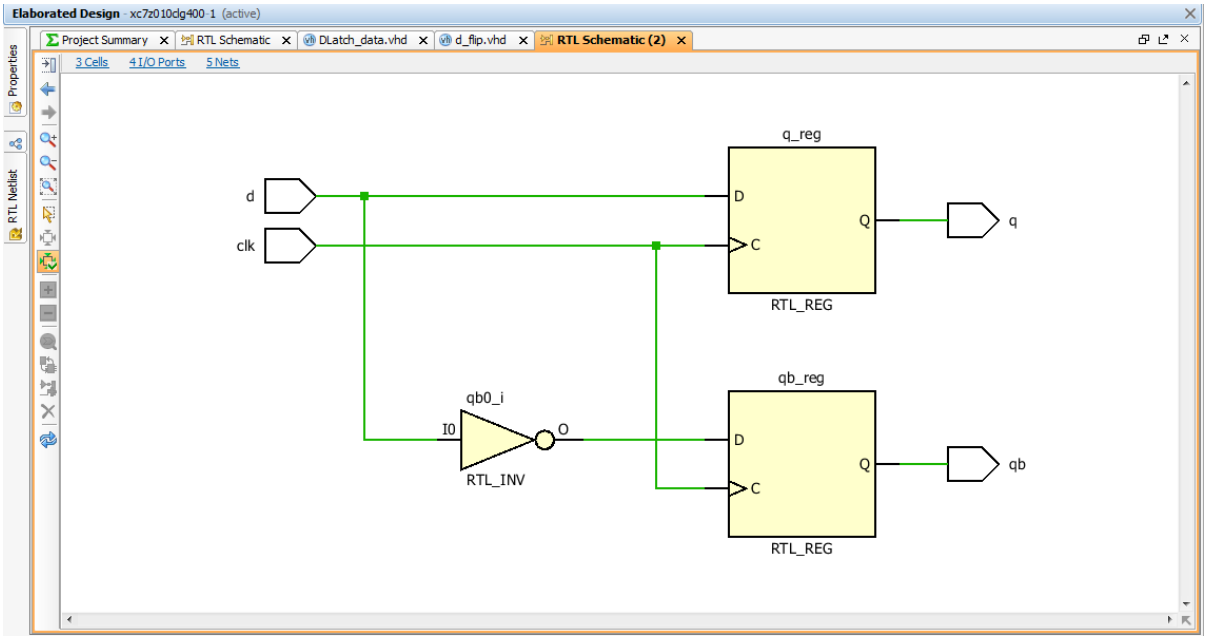

Figure 6.4 Schematic of implementing a synchronous D flip flop using behavioral modeling.

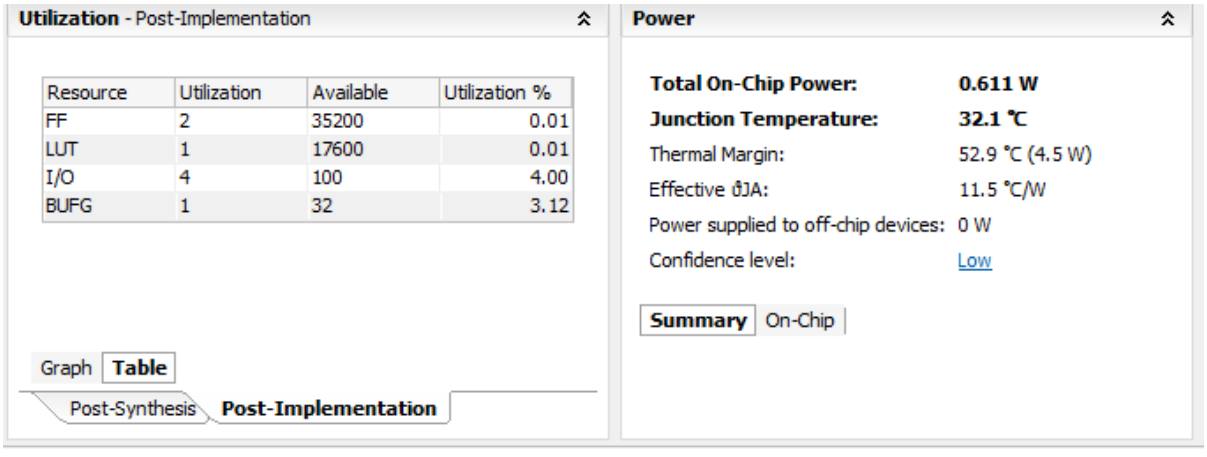

Figure 6.5 Project Summary of implementing a synchronous D flip flop using behavioral modeling.

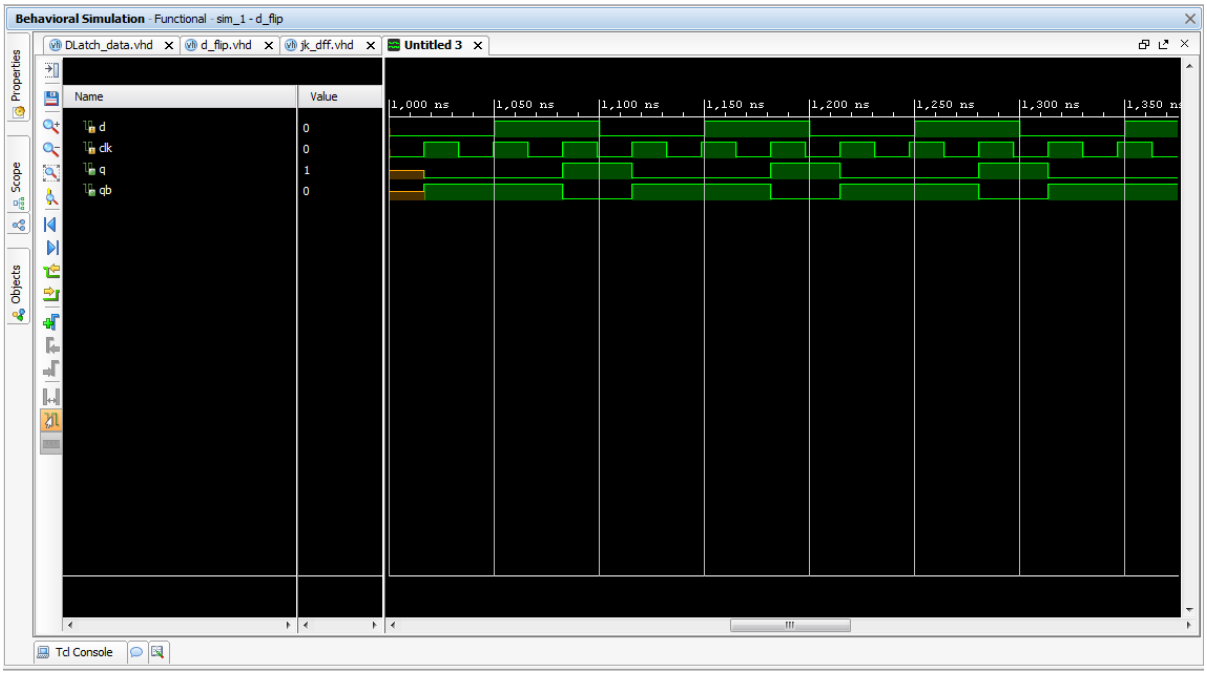

Figure 6.6 Simulation of implementing a synchronous D flip flop using behavioral modeling.

6.4.3 Synchronous JK flip flop using structural modeling.

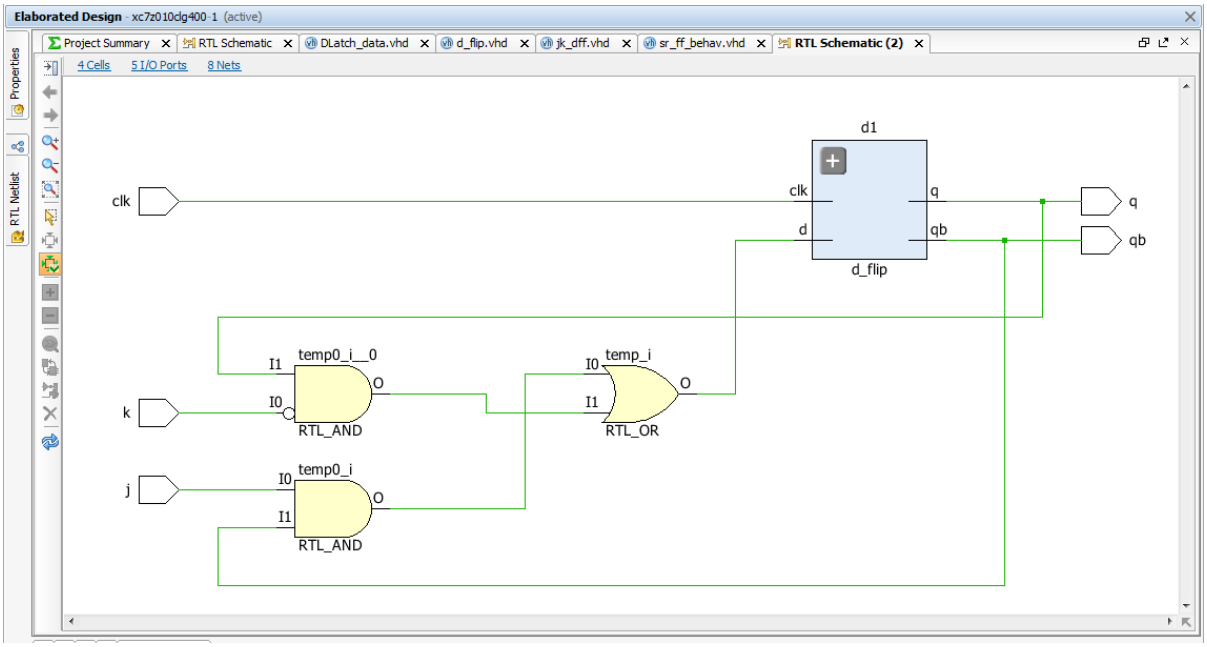

Figure 6.7 Schematic of Implementing a Synchronous JK flip flop using structural modeling.

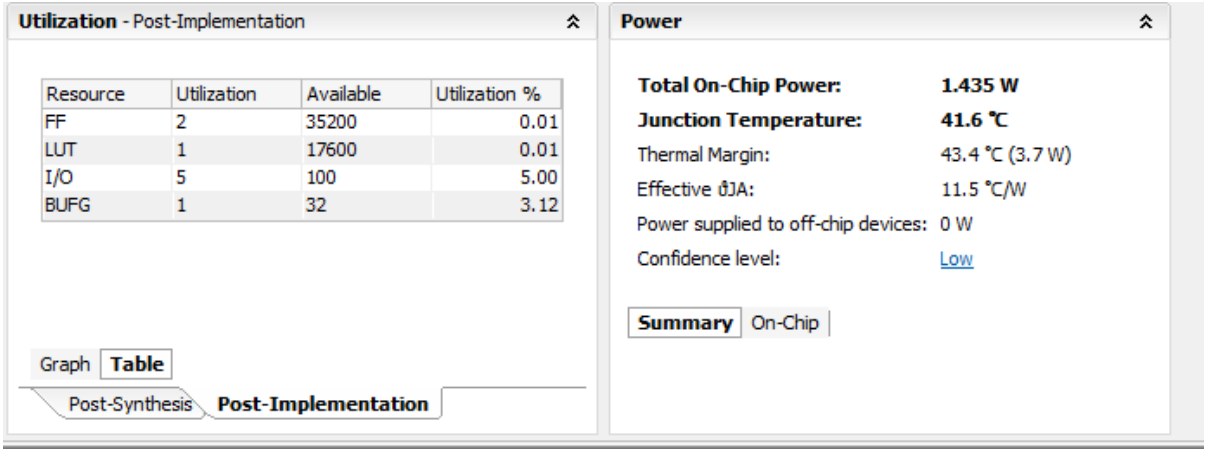

Figure 6.8 Project Summary of Implementing a Synchronous JK flip flop using structural modeling.

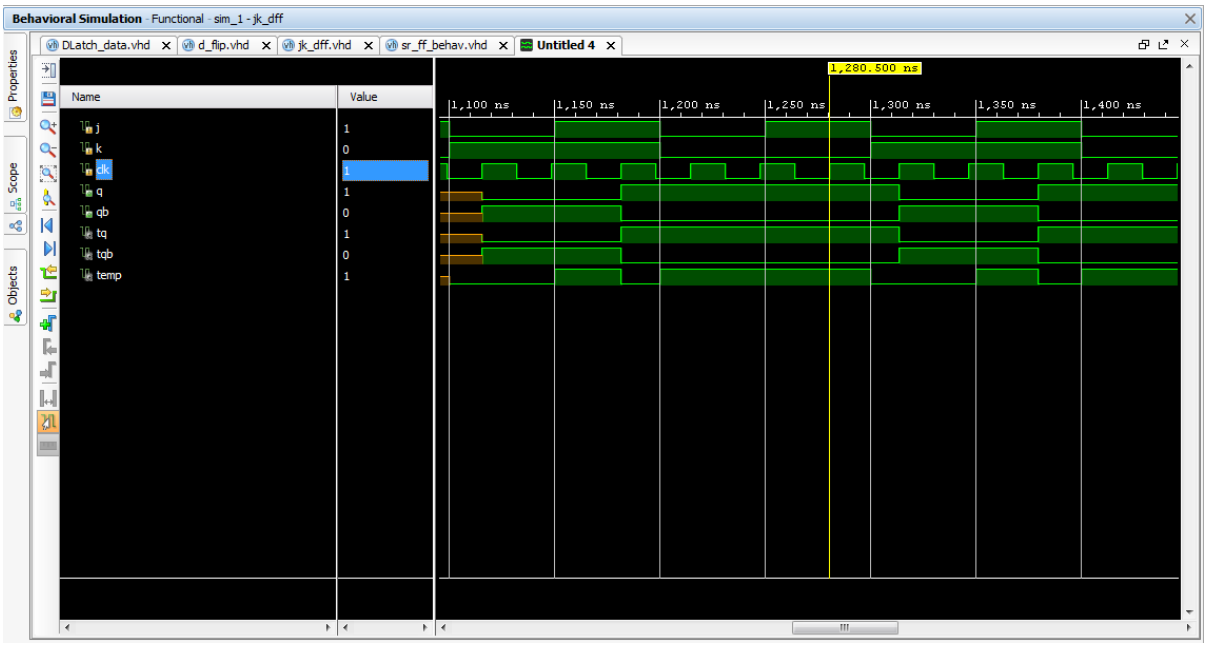

Figure 6.9 Simulation of Implementing a Synchronous JK flip flop using structural modeling.

6.4.4 Synchronous RS flip flop using behavioral modeling.

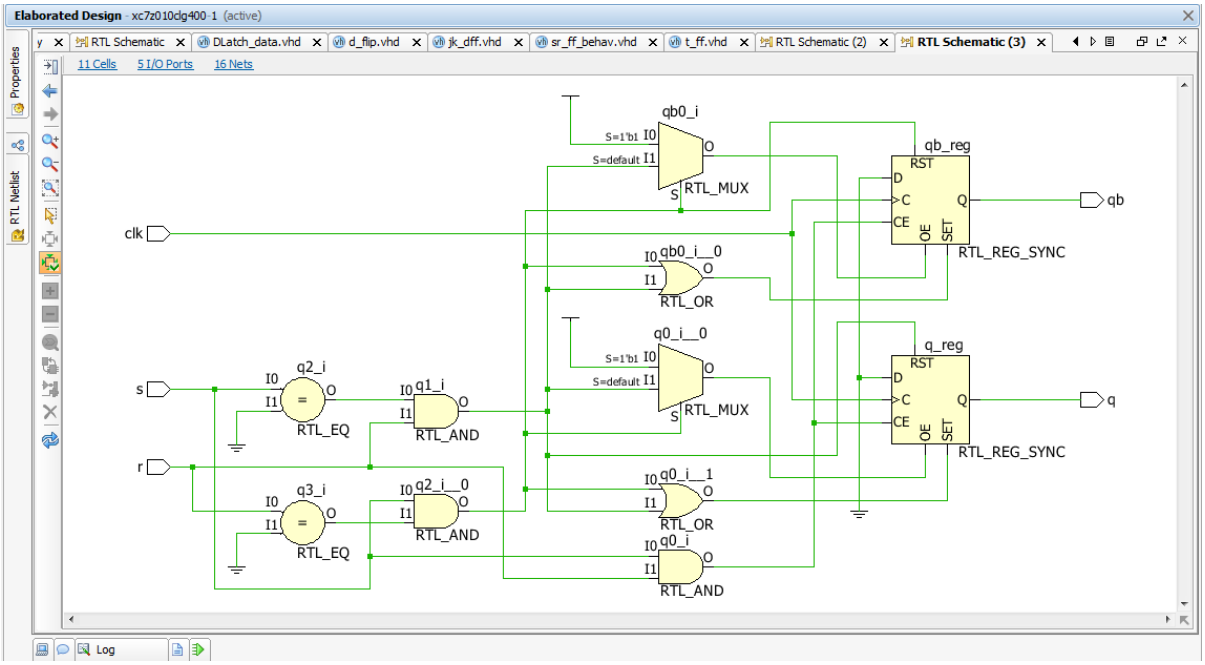

Figure 6.10 Schematic of Implementing a Synchronous RS flip flop using behavioral modeling.

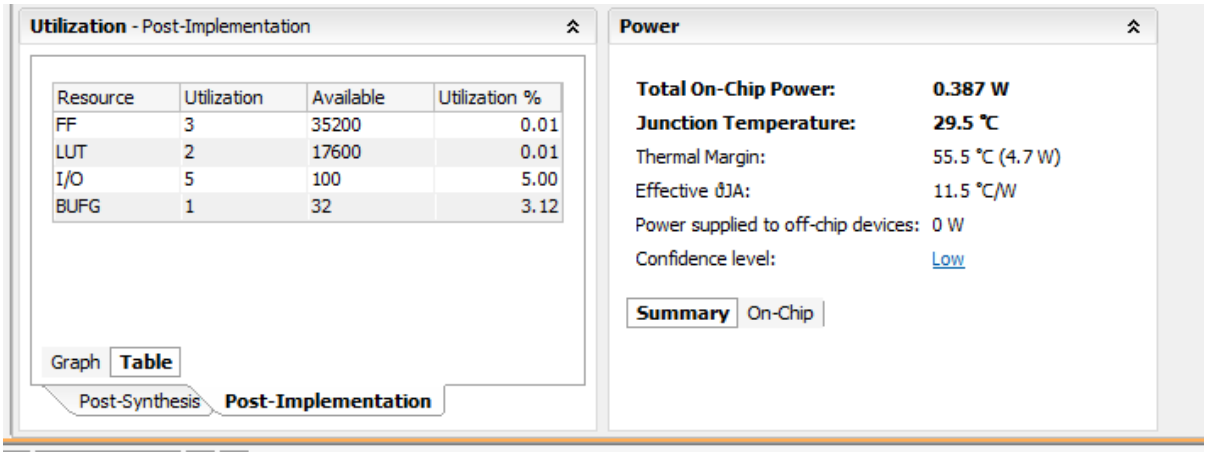

Figure 6.11 Project Summary of Implementing a Synchronous RS flip flop using behavioral modeling.

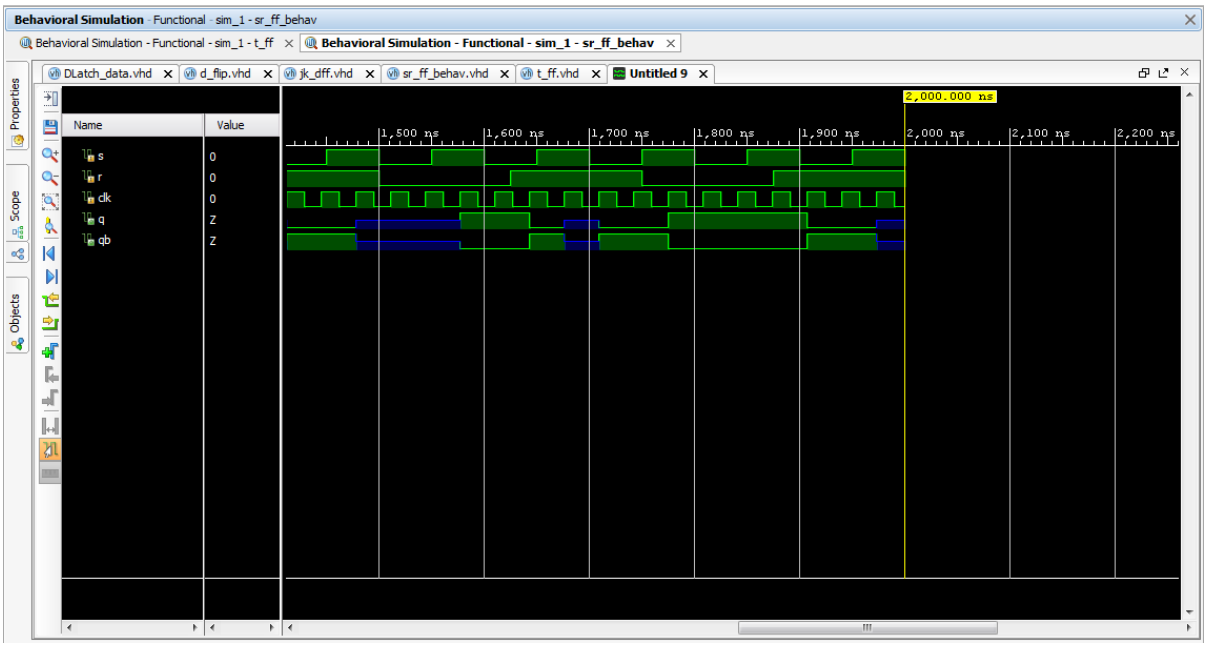

Figure 6.12 Simulation of Implementing a Synchronous RS flip flop using behavioral modeling.

6.4.5 Synchronous T flip flop using behavioral modeling.

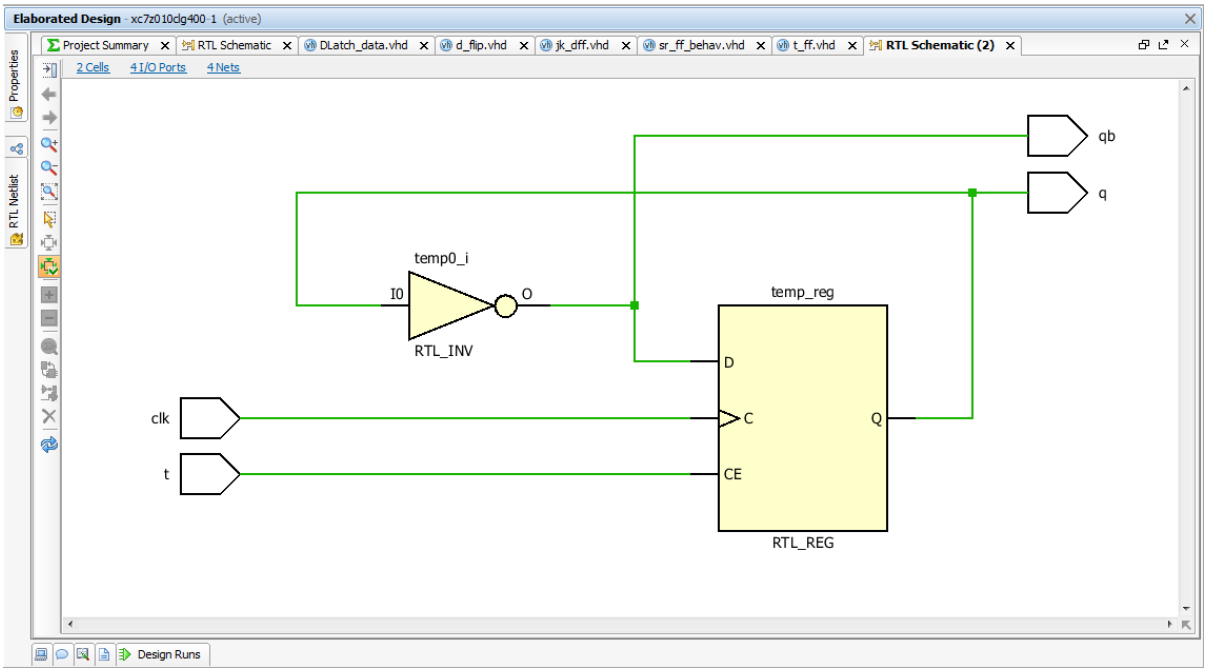

Figure 6.13 Schematic of Implementing a synchronous T flip flop using behavioral modeling.

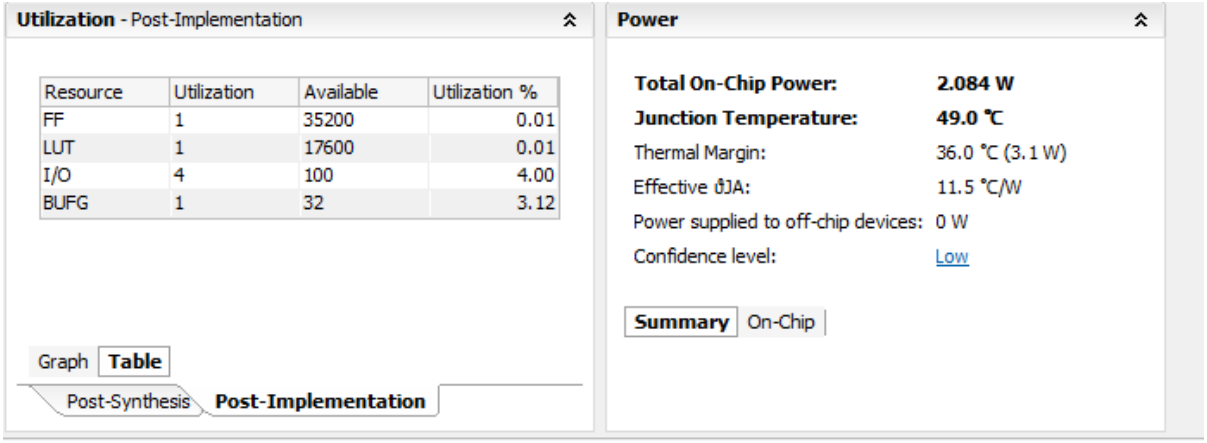

Figure 6.14 Project Summary of Implementing a synchronous T flip flop using behavioral modeling.

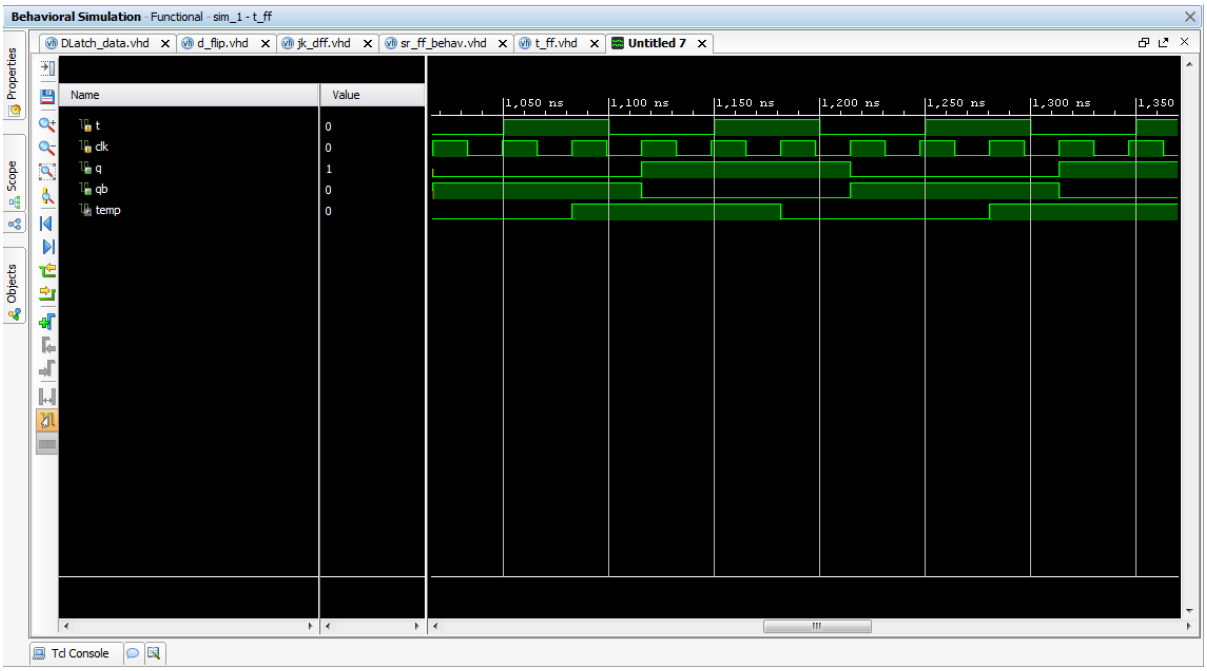

Figure 6.15 Simulation of Implementing a synchronous T flip flop using behavioral modeling.

6.5 Summary

Name of the Entity	No. of LUT used	Total On chip Power
Implementing a synchronous D latch using dataflow modeling.	2	0.911W
Implementing a synchronous D flip flop using behavioral modeling.	1	0.611W
Implementing a Synchronous JK flip flop using structural modeling.	1	1.435W
Implementing a Synchronous RS flip flop using behavioral modeling.	2	0.387w
Implementing a synchronous T flip flop using behavioral modeling.	1	2.084w

Table 6.1 comparision of Area and power requirements for different kinds of methods.