Digital Circuits and Systems Lab

Laboratory report submitted for the partial fulfillment
of the requirements for the degree of

Bachelor of Technology
in
Communication and Computer Engineering

by

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Contents

Chapter *4*

Experiment - 4

4.1 Name of the Experiments

Implement 2 to 4 and 3 to 8 line decoder using dataflow, behavioral and mixed modeling in VHDL. Implement Boolean functions using decoders.

4.2 Theory

A binary decoder is a combinational logic circuit that converts binary information from the n coded inputs to a maximum of 2^n unique decimal outputs.
A 2 to 4 decoder activates one of the 4 outputs for each input value from 0-3
A 3 to 8 decoder activates one of the 4 outputs for each input value from 0-7
A 4 to 16 decoder activates one of the 4 outputs for each input value from 0-15

A higher level of decoder can be derived using lower level decoders

4.3 Coding Techniques used

4.3.1 Data flow modeling

Dataflow Modeling includes declaration of a target signal using logical events occurring on the particular signal. Dataflow Modeling is primarily expressed using signal assignment statements. This modeling is shown by implementing a 3 to 8 line decoder.

4.3.2 Structural modeling

Structural Modeling is the set of interconnected components. That is, it describes the structure. The visible components are instantiated in the declarative part of the architecture body while the declared components are instantiated with their respective interface ports in the statement part of the architecture body. This modeling is shown by implementing a boolean function through 3 to 8 line decoder and implementing a 4 to 16 decoder using 2 to 4 decoder.

4.3.3 Behavioral modeling by using If statement

Behavioral Modeling deals with the functionality of an entity. Here, the set of statements are executed sequentially in a specified order, mainly specified within a process statement. The process statement is itself a concurrent statement but inside it lies a set of statements which are all sequential in nature. This modeling is shown by implementing a 2 to 4 line decoder.

4.4 Simulation and Results

4.4.1 Using behavioral architecture, implement a 2 to 4 line decoder.

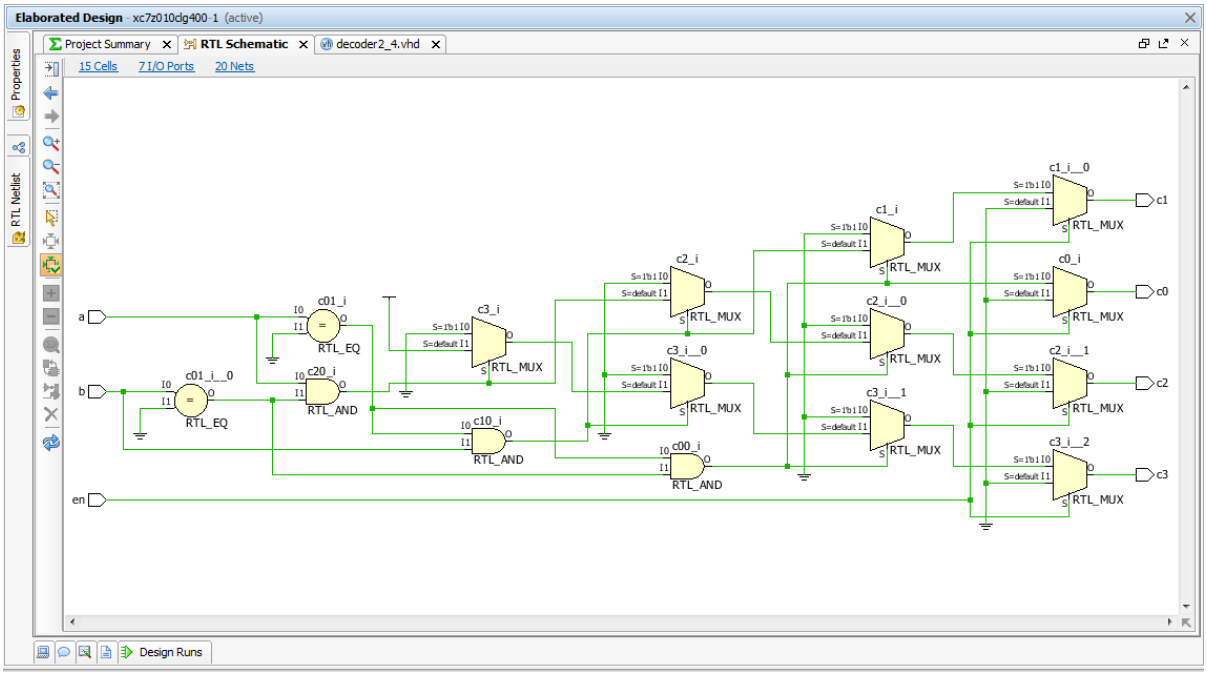

Figure 4.1 Schematic of implementing a 2 to 4 line decoder using behavioral

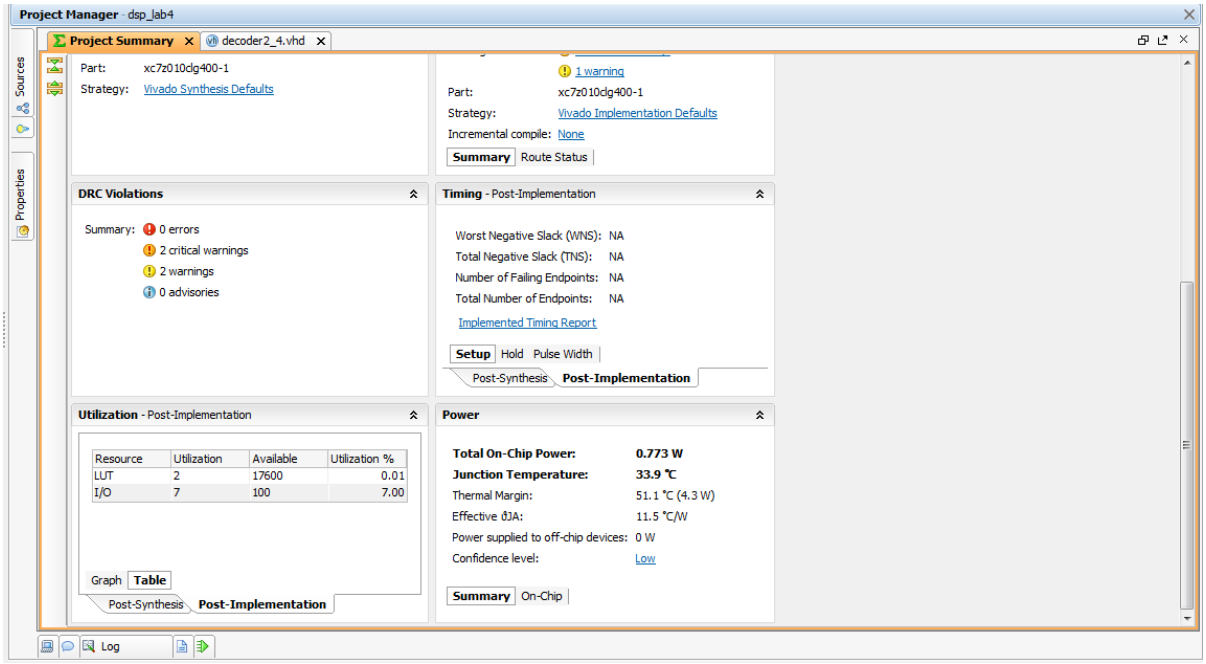

Figure 4.2 Project Summary of implementing a 2 to 4 line decoder using behavioral

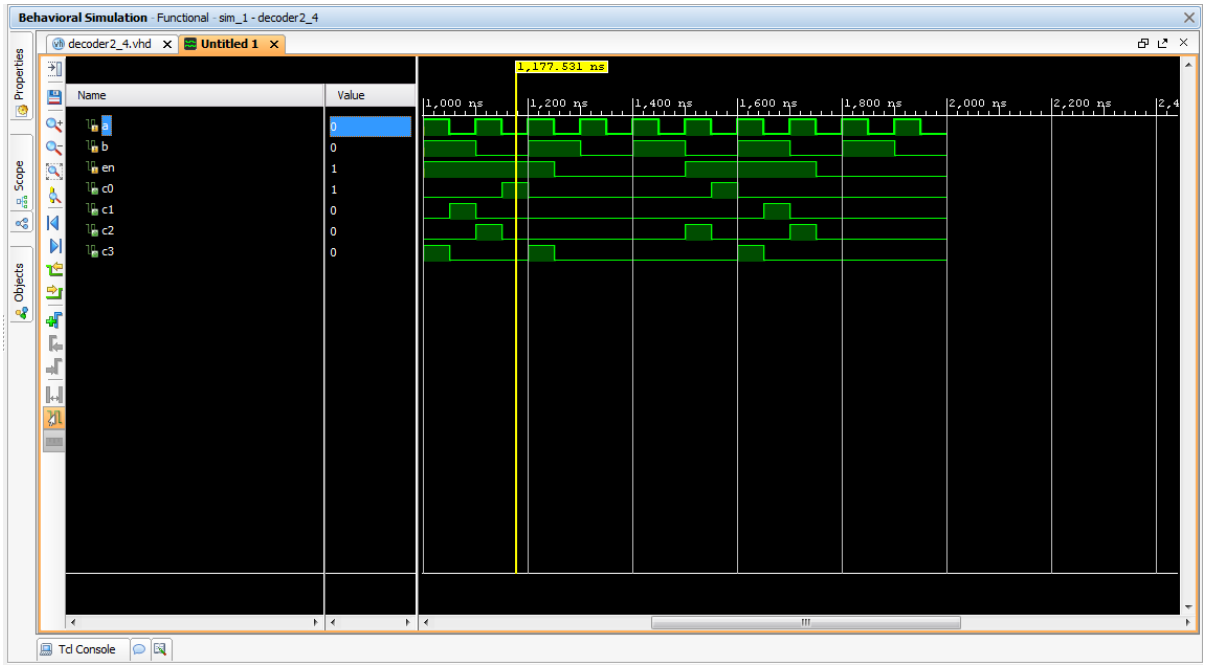

Figure 4.3 Simulation of implementing a 2 to 4 line decoder using behavioral

4.4.2 Using dataflow modeling, implement a 3 to 8 line decoder.

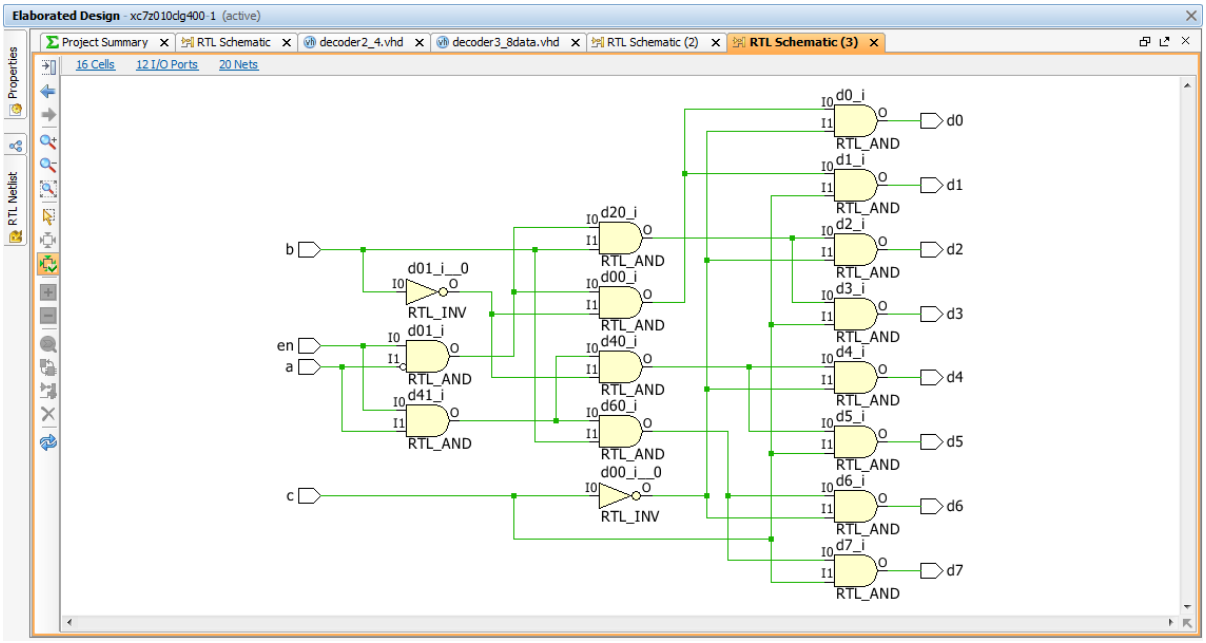

Figure 4.4 Schematic of implementing 3 to 8 decoder using dataflow.

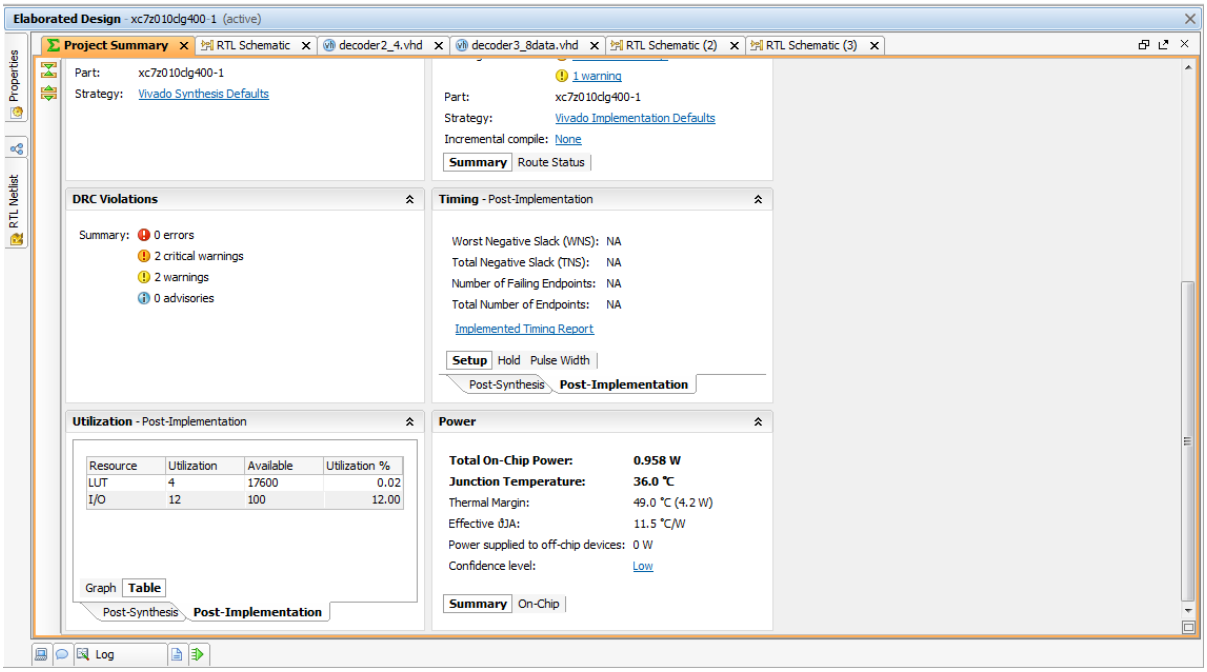

Figure 4.5 Project Summary of implementing 3 to 8 decoder using dataflow.

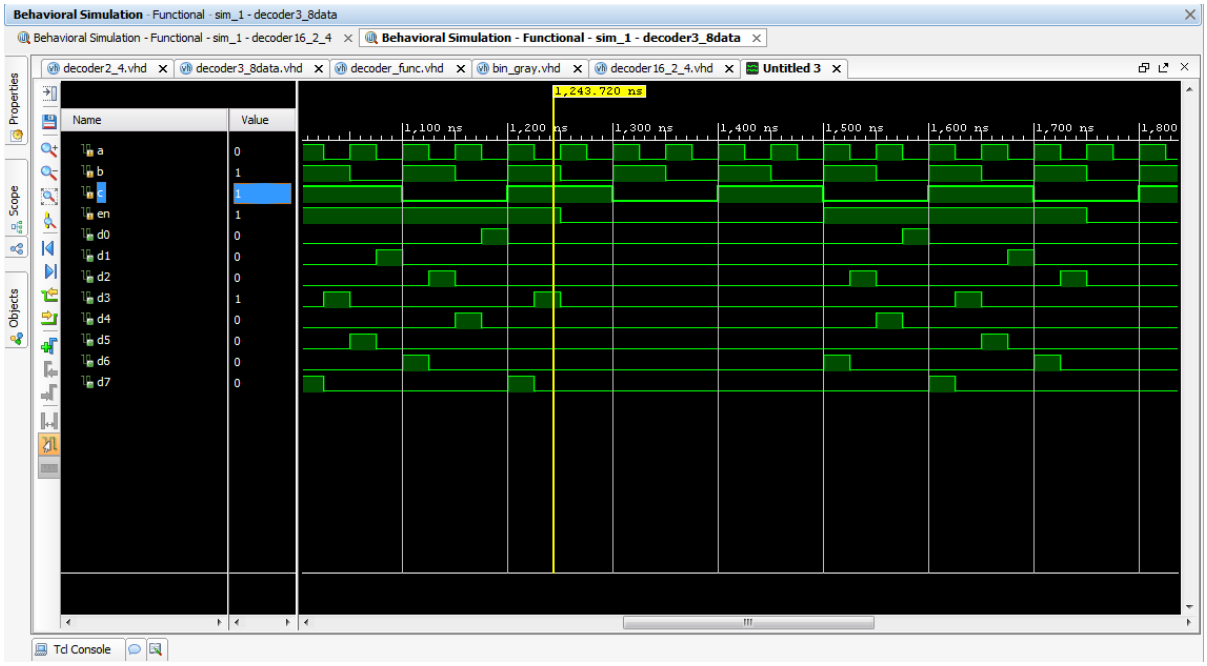

Figure 4.6 Simulation of implementing 3 to 8 decoder using dataflow.

4.4.3 Implement the following function using a 3 to 8 line decoder by using structural architecture.

F(A, B, C) = (1, 3, 4, 6)

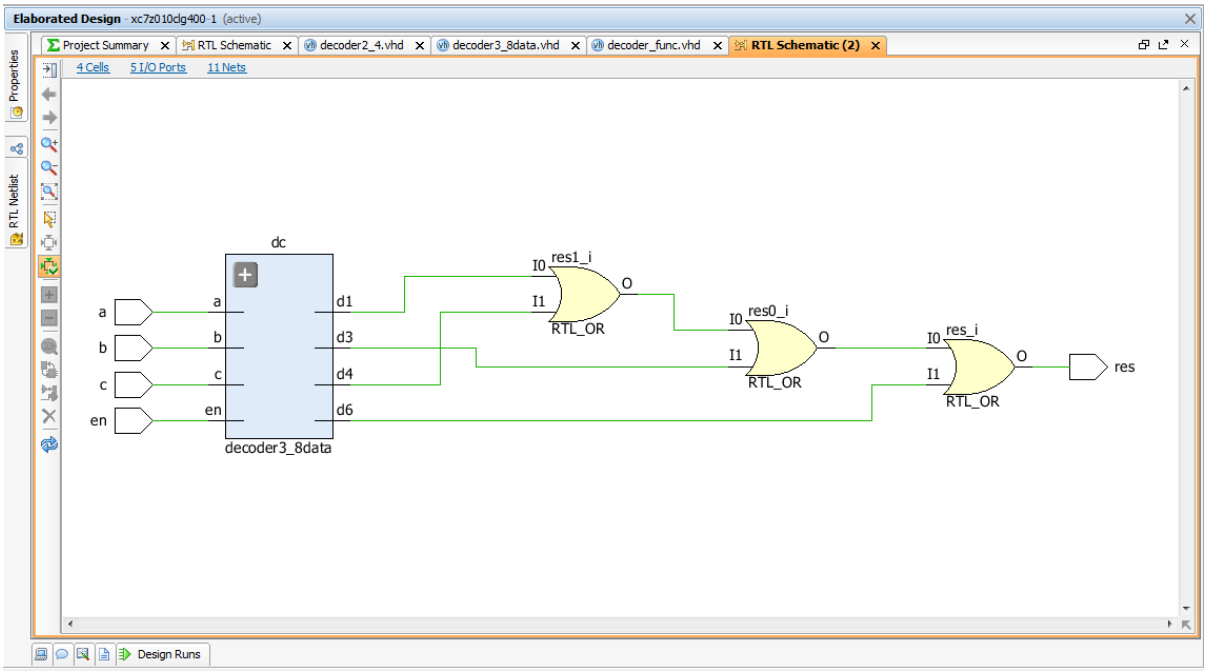

Figure 4.7 Schematic of Implementing a boolean function using decoder.

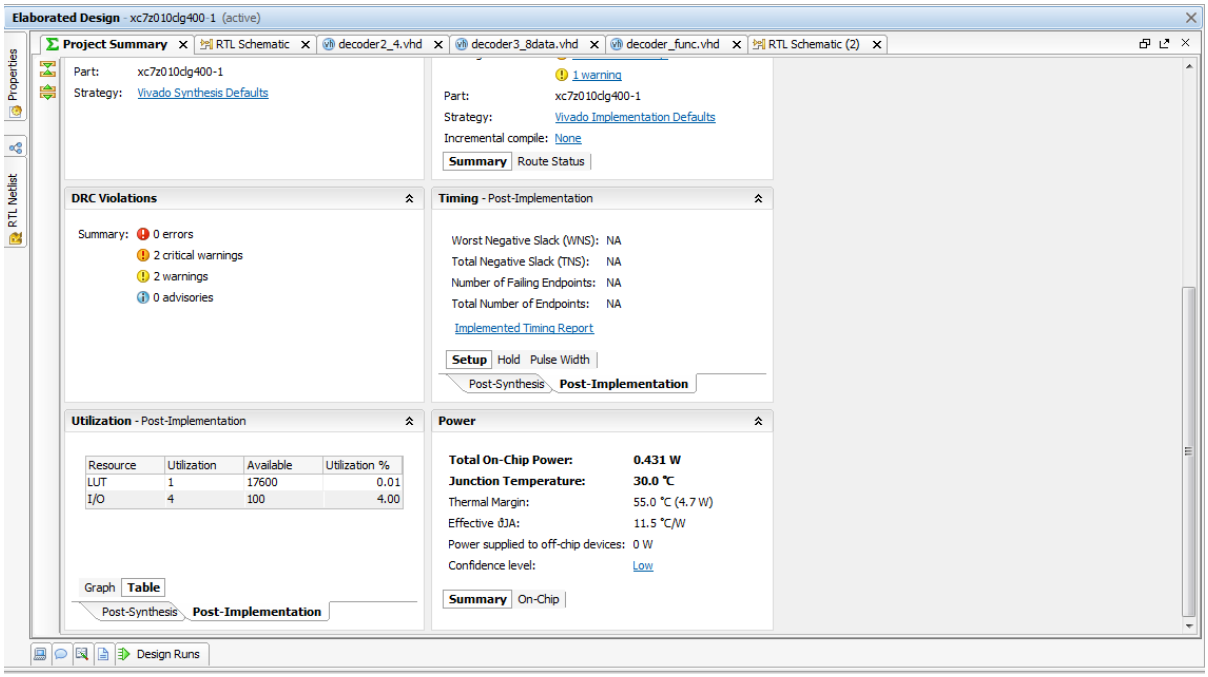

Figure 4.8 Project Summary of Implementing a boolean function using decoder.

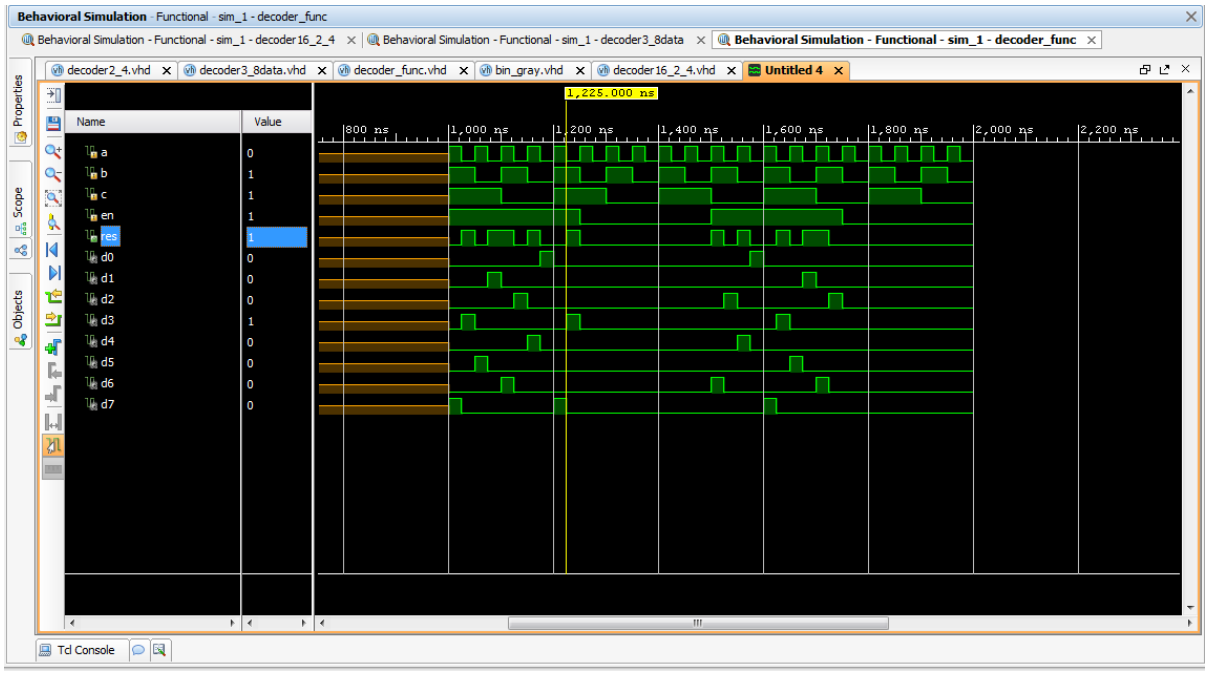

Figure 4.9 Simulation of Implementing a boolean function using decoder.

4.4.4 Encode a 4 bit array of binary number system to the corresponding 4 bit array of gray code.

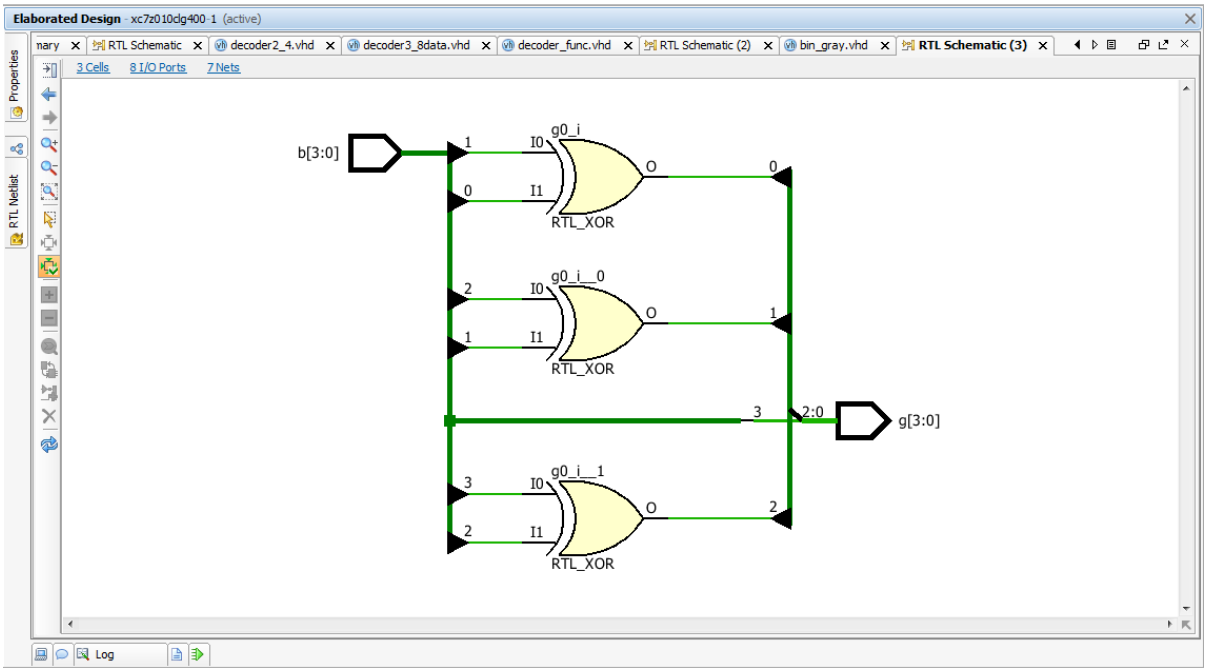

Figure 4.10 Schematic of Encoding 4 bit binary number to corresponding gray code

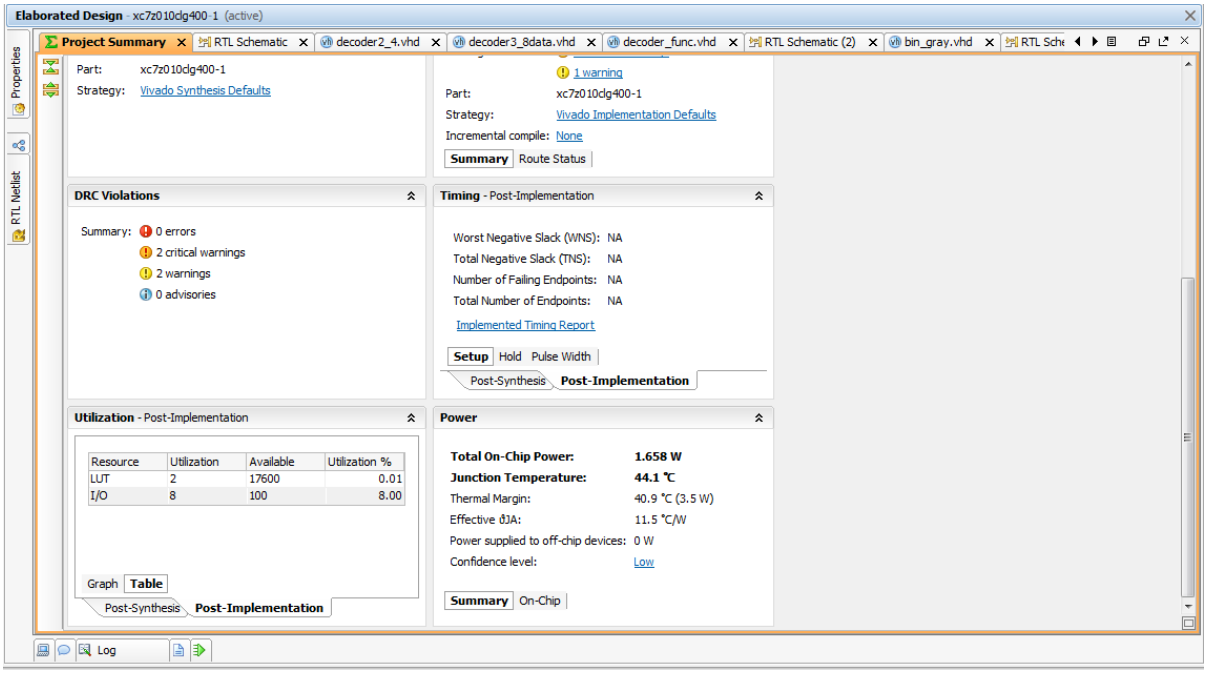

Figure 4.11 Project Summary of Encoding 4 bit binary number to corresponding gray code

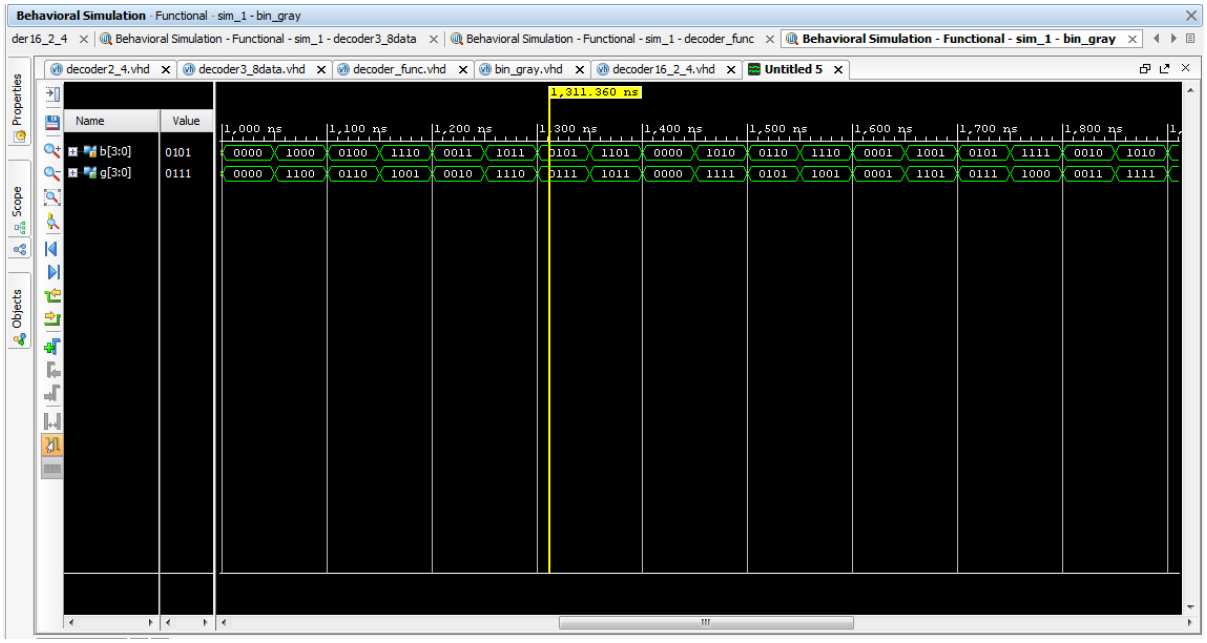

Figure 4.12 Simulation of Encoding 4 bit binary number to corresponding gray code

4.4.5 Implement a 4 to 16 line decoder using only 2 to 4 line decoders, using structural modeling.

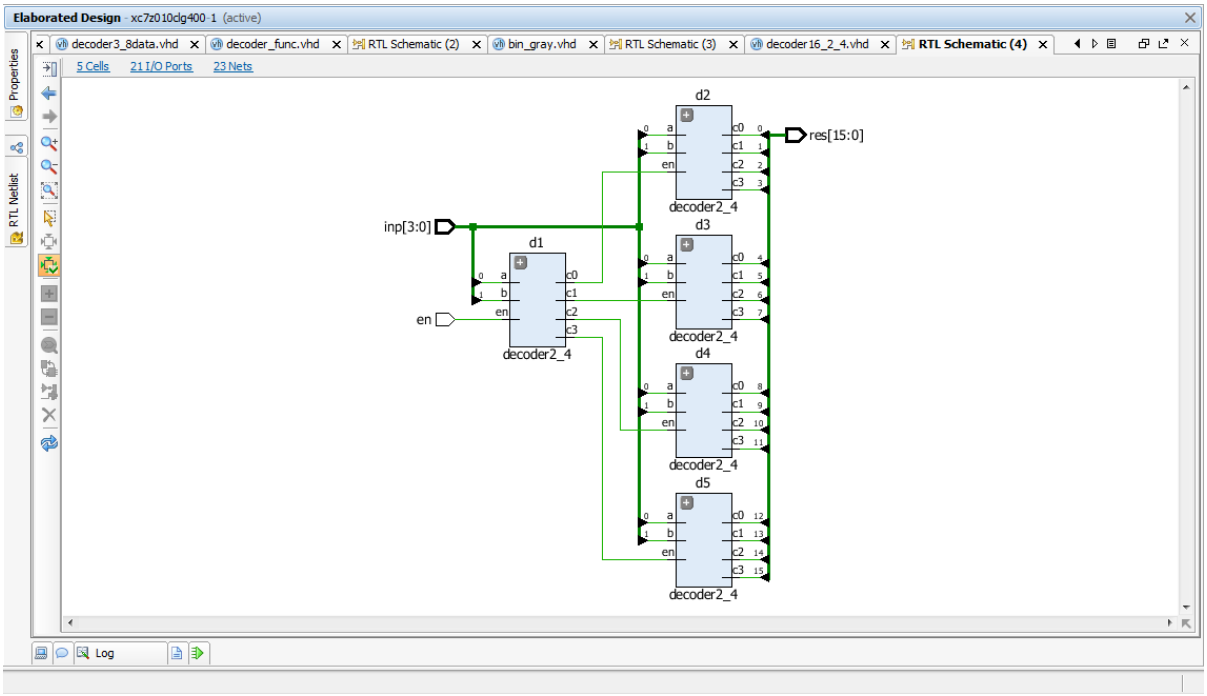

Figure 4.13 Schematic of Implementing 4 to 16 decoder using 2 to 4 decoder.

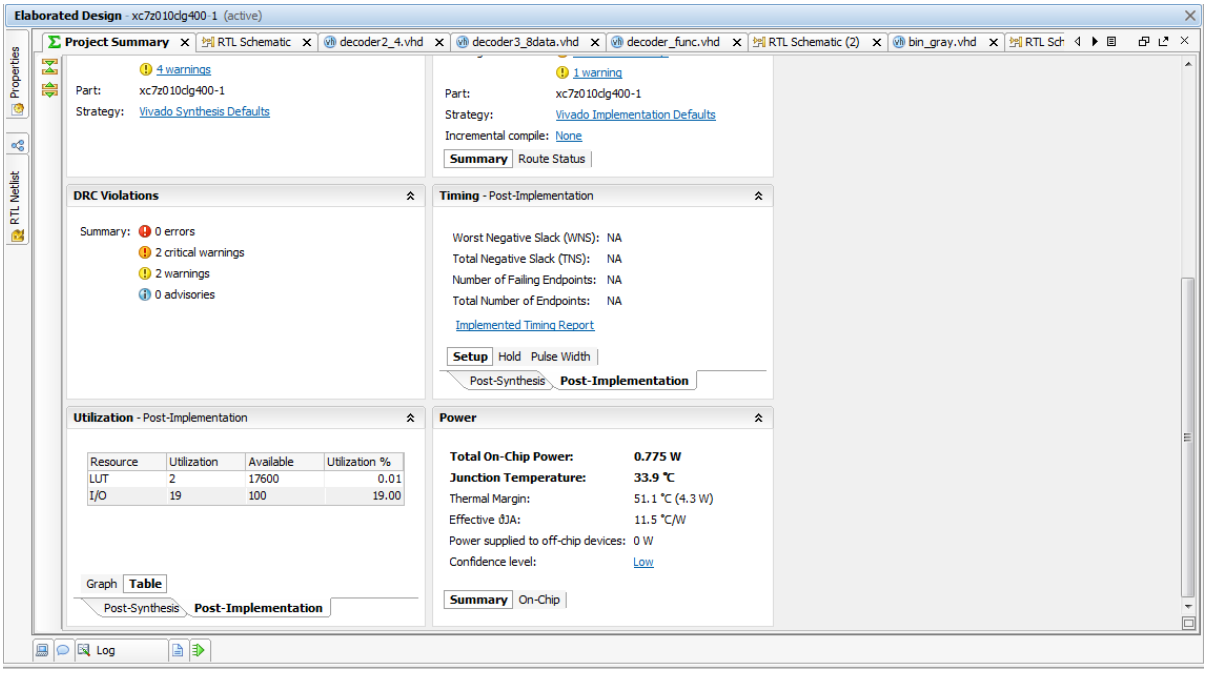

Figure 4.14 Project Summary of Implementing 4 to 16 decoder using 2 to 4 decoder.

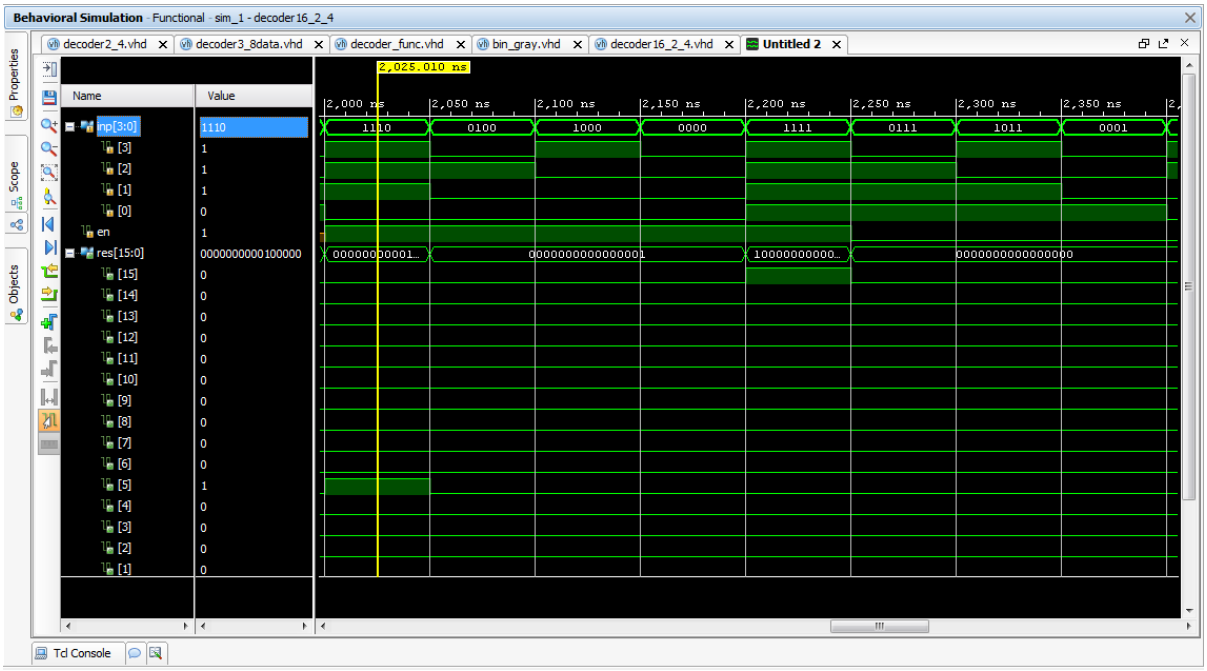

Figure 4.15 Simulation of Implementing 4 to 16 decoder using 2 to 4 decoder.

4.5 Summary

Name of the Entity	No. of LUT used	Total On chip Power
Simulation of implementing a 2 to 4 line decoder using behavioral	2	0.773W
Simulation of implementing 3 to 8 decoder using dataflow	4	0.958W
Implementing a boolean function using decoder	1	0.431W
Encoding 4 bit binary number to corresponding gray code	2	1.658w
Implementing 4 to 16 decoder using 2 to 4 decoder	2	0.775w

Table 4.1 comparision of Area and power requirements for different kinds of methods.