Digital Circuits and Systems Lab

Laboratory report submitted for the partial fulfillment
of the requirements for the degree of

Bachelor of Technology
in
Communication and Computer Engineering

by

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Chapter *3*

Experiment - 3

3.1 Name of the Experiments

Implementation of 2x1, 4x1 and 8x1 multiplexers using dataflow, behavioral and structural modeling in VHDL.

3.2 Theory

The multiplexer(also called MUX) is a combinational logic circuit designed to switch one of several input lines to a single common output line by the application of a control signal.
A 2x1 MUX takes in 2 input lines of signal and 1 control signal and outputs a single signal depending on the control signal.
A 4x1 MUX takes in 4 input lines of signal and 2 control signal and outputs a single signal depending on the combination of the control signals.
A 8x1 MUX takes in 8 input lines of signal and 3 control signal and outputs a single signal depending on the combination of the control signals.

3.3 Coding Techniques used

3.3.1 Data flow modeling

Dataflow Modeling includes declaration of a target signal using logical events occurring on the particular signal. Dataflow Modeling is primarily expressed using signal assignment statements.
Used in Experiments of Implementing a 2x1 multiplexer using dataflow modeling and Implementing a 4x1 multiplexer using dataflow modeling.

3.3.2 Behavioral modeling

By using If statement, Behavioral Modeling deals with the functionality of an entity. Here, the set of statements are executed sequentially in a specified order, mainly specified within a process statement. The process statement is itself a concurrent statement but inside it lies a set of statements which are all sequential in nature.
Used in Experiment of Implementing a 2x1 multiplexer using behavioral modeling

3.3.3 Structural modeling

Structural Modeling is the set of interconnected components. That is, it describes the structure. The visible components are instantiated in the declarative part of the architecture body while the declared components are instantiated with their respective interface ports in the statement part of the architecture body.
Used in Experiments of Implementing a 4x1 multiplexer using only 2x1 MUX and Implementing a 8x1 multiplexer using only 2x1 MUX

3.4 Simulation and Results

3.4.1 Implementing a 2x1 multiplexer using dataflow modeling.

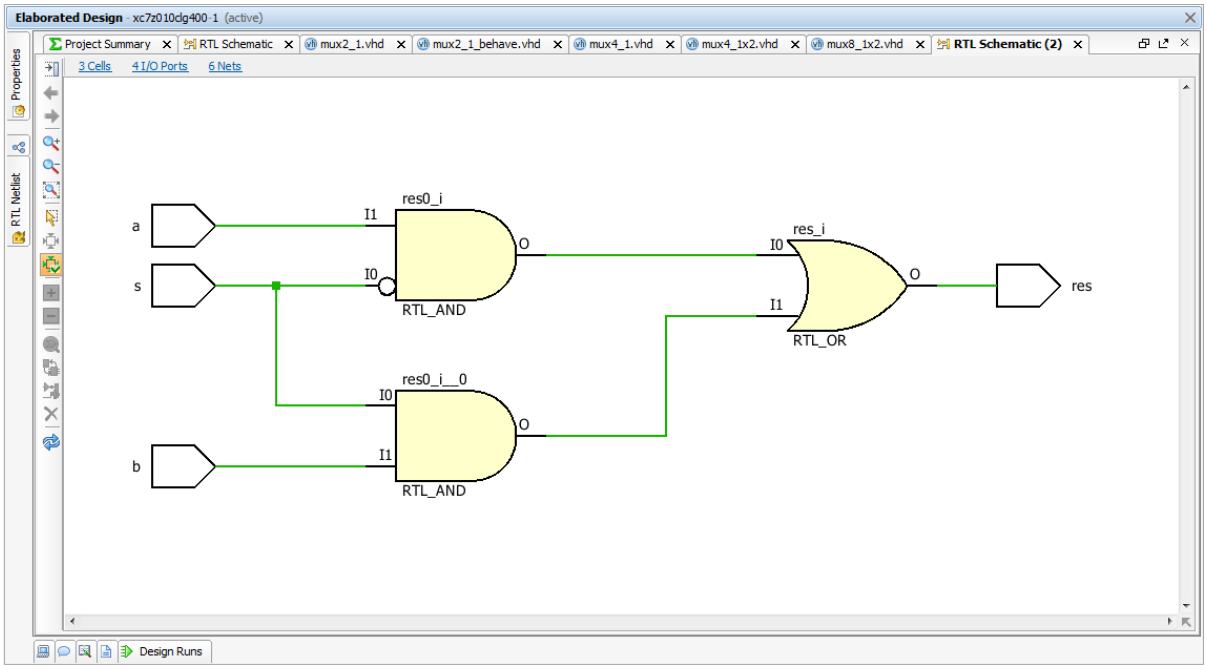

Figure 3.1 Schematic of Implementing a 2x1 multiplexer using dataflow modeling

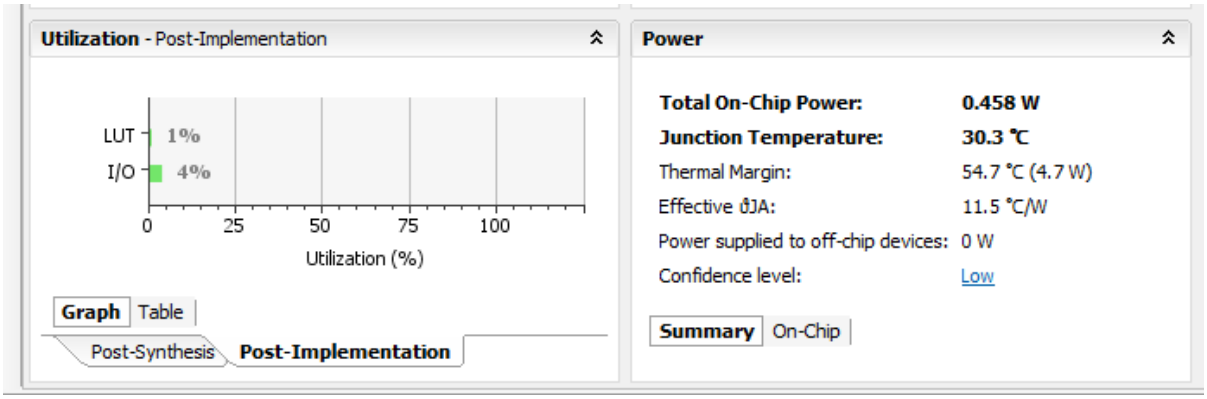

Figure 3.2 Project Summary of Implementing a 2x1 multiplexer using dataflow modeling

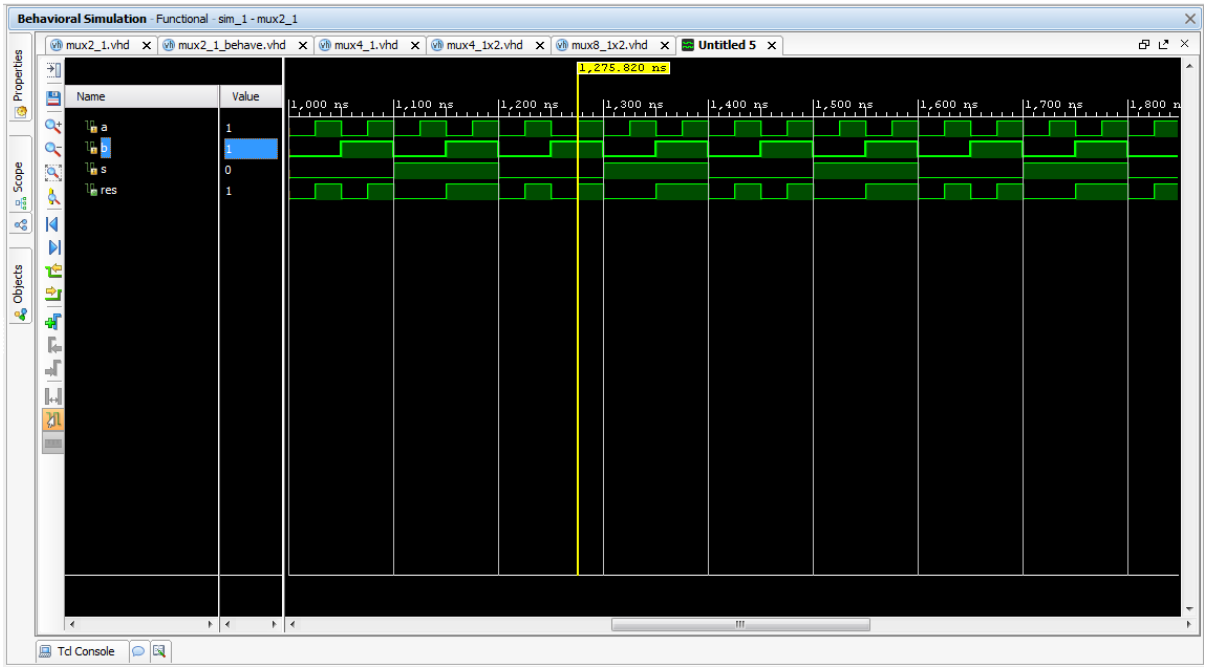

Figure 3.3 Simulation of Implementing a 2x1 multiplexer using dataflow modeling

3.4.2 Implementing a 2x1 multiplexer using behavioral modeling

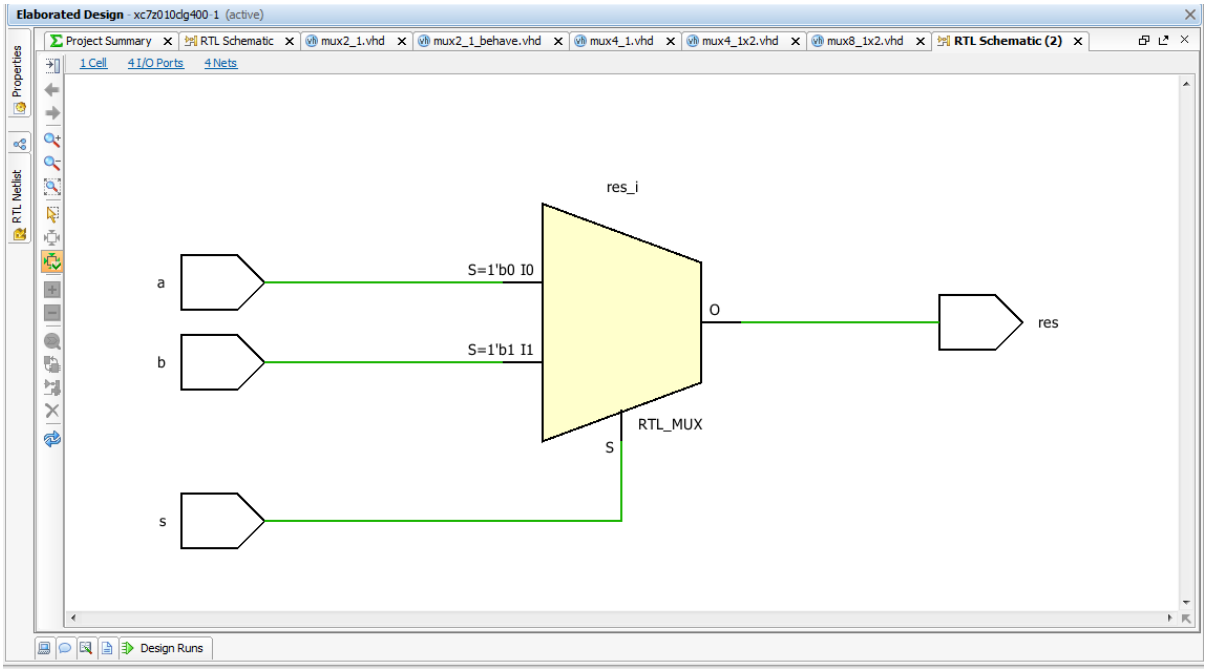

Figure 3.4 Schematic of Implementing a 2x1 multiplexer using behavioral modeling

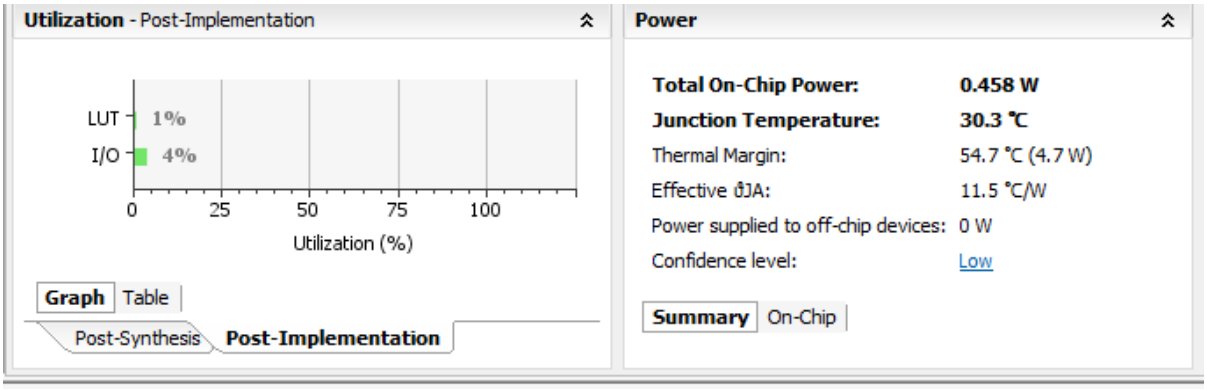

Figure 3.5 Project Summary of Implementing a 2x1 multiplexer using behavioral modeling

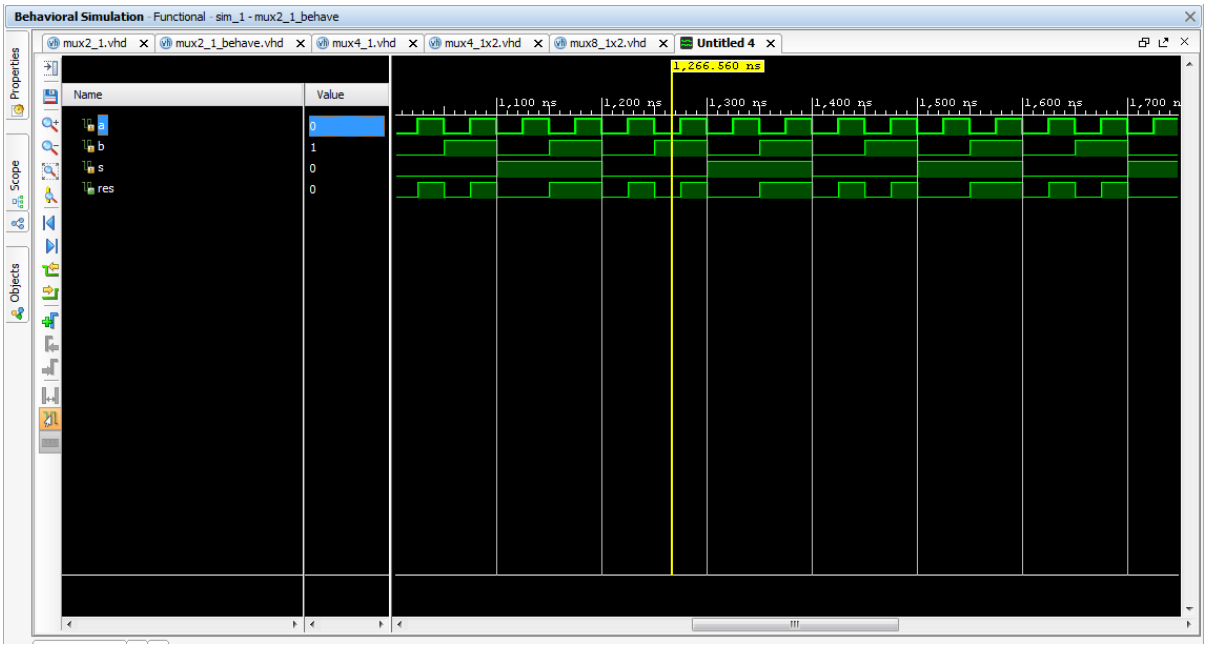

Figure 3.6 Simulation of Implementing a 2x1 multiplexer using behavioral modeling

3.4.3 Implementing a 4x1 multiplexer using dataflow modeling.

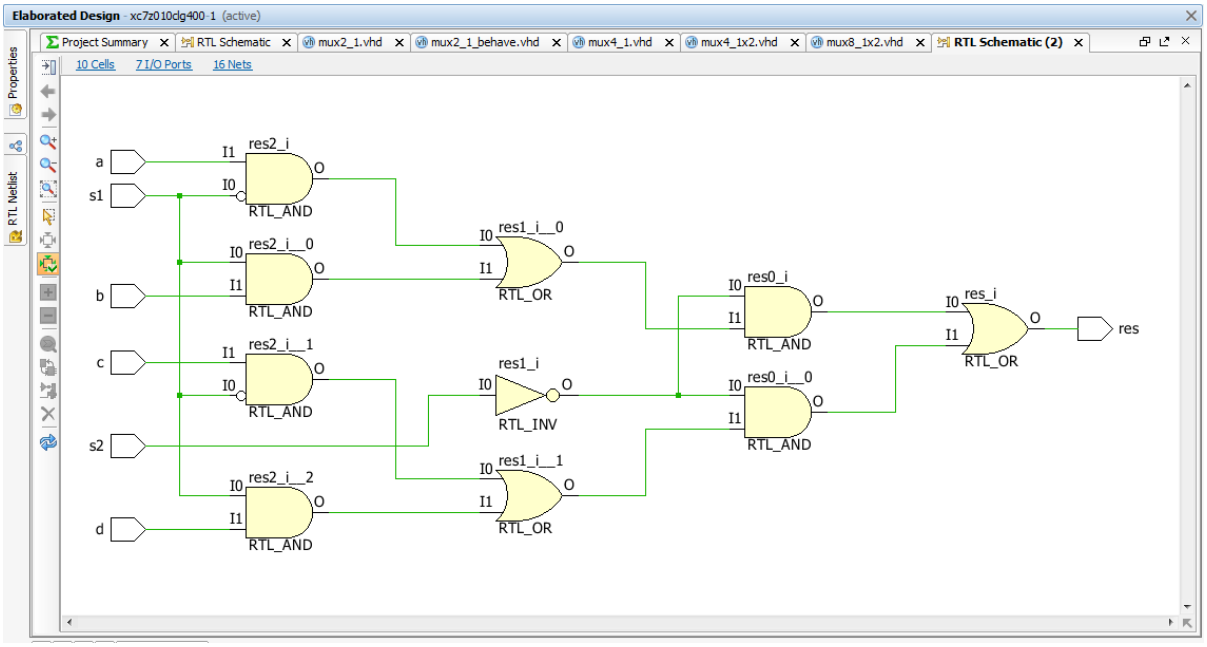

Figure 3.7 Schematic of Implementing a 4x1 multiplexer using dataflow modeling.

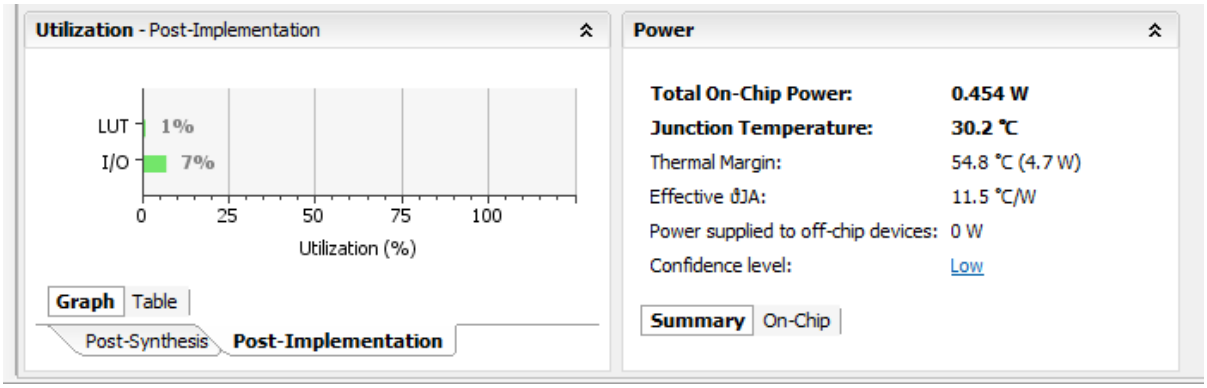

Figure 3.8 Project Summary of Implementing a 4x1 multiplexer using dataflow modeling.

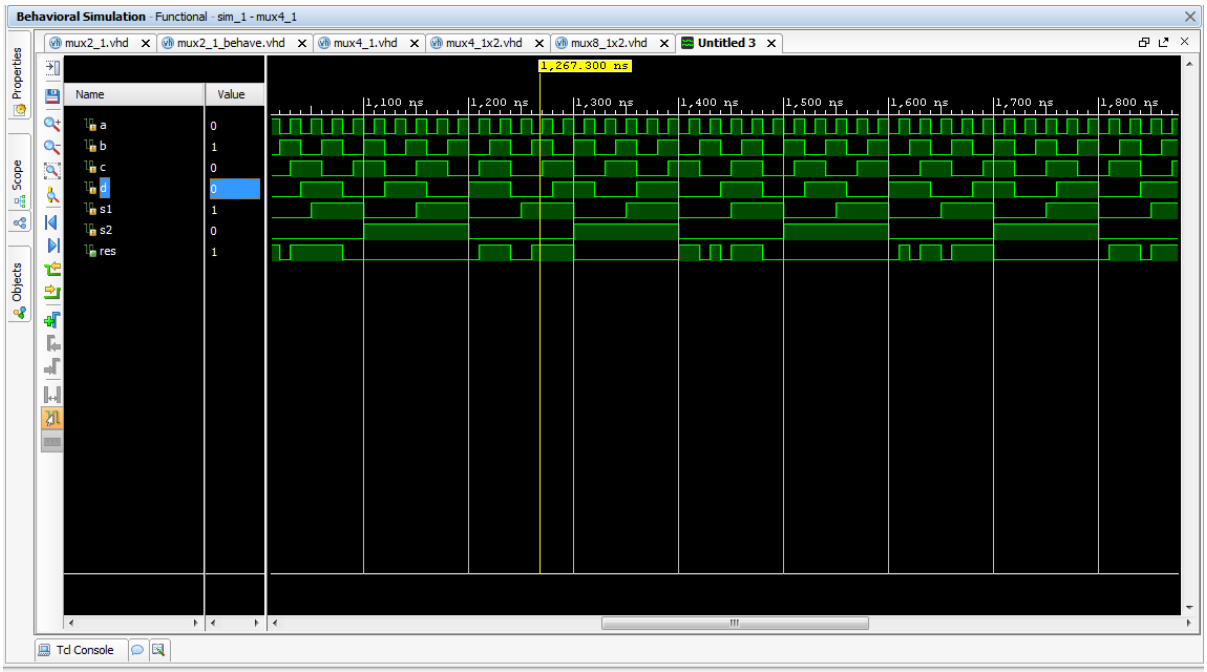

Figure 3.9 Simulation of Implementing a 4x1 multiplexer using dataflow modeling.

3.4.4 Implementing a 4x1 multiplexer using only 2x1 MUX

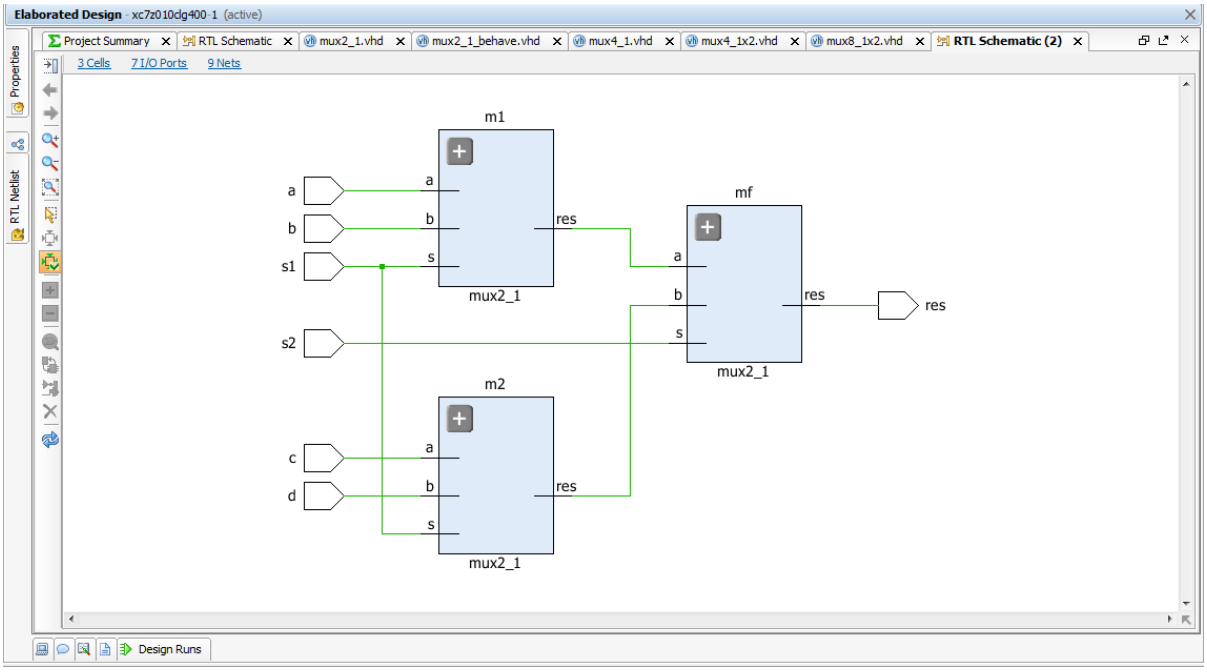

Figure 3.10 Schematic of Implementing a 4x1 multiplexer using only 2x1 MUX

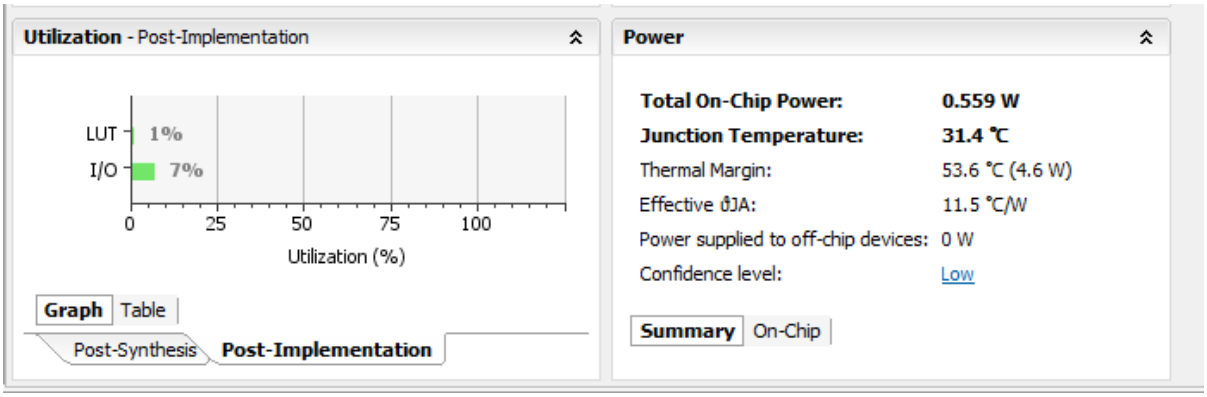

Figure 3.11 Project Summary of Implementing a 4x1 multiplexer using only 2x1 MUX

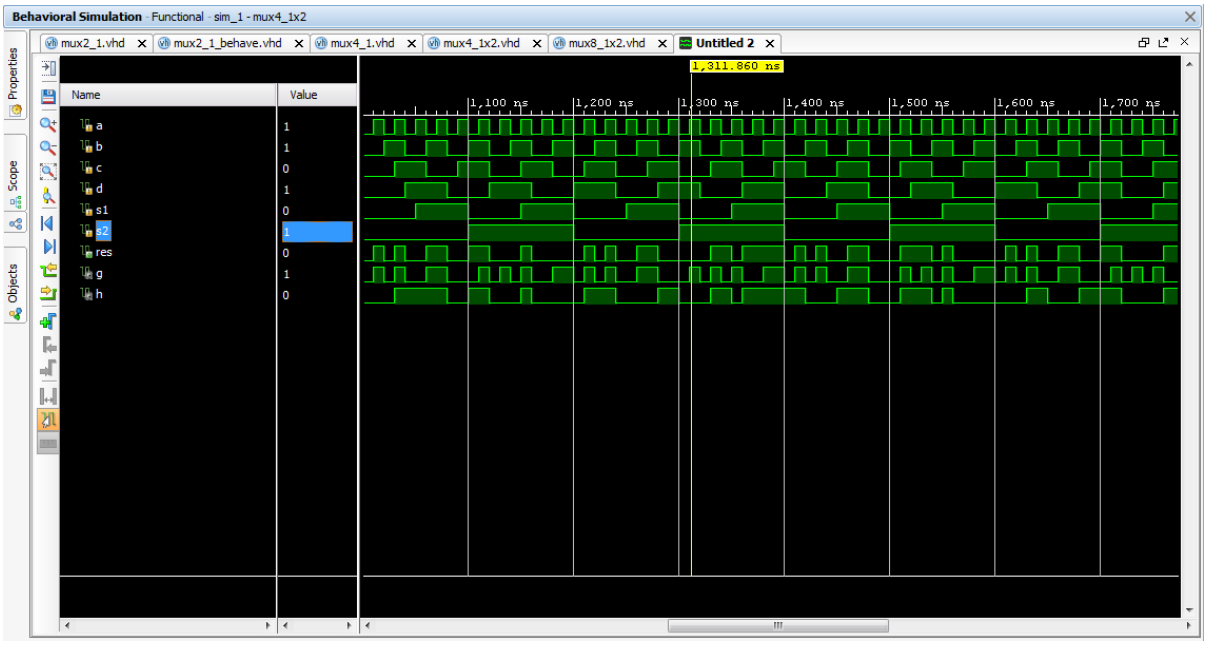

Figure 3.12 Simulation of Implementing a 4x1 multiplexer using only 2x1 MUX

3.4.5 Implementing a 8x1 multiplexer using only 2x1 MUX

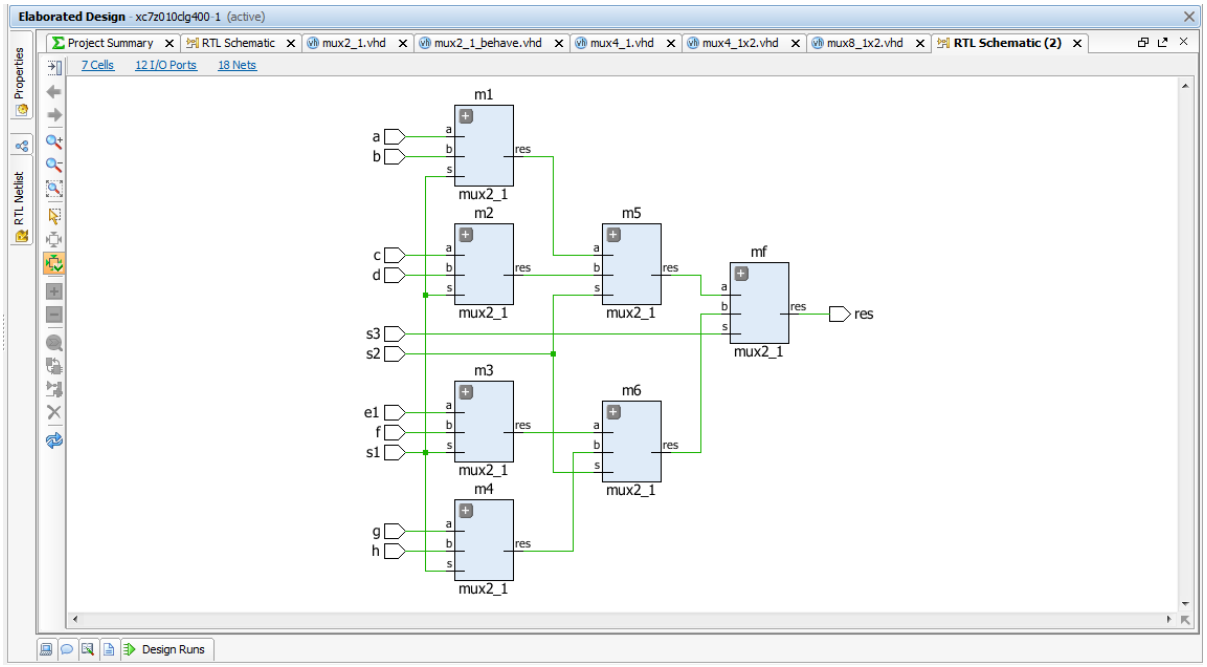

Figure 3.13 Schematic of Implementing a 8x1 multiplexer using only 2x1 MUX

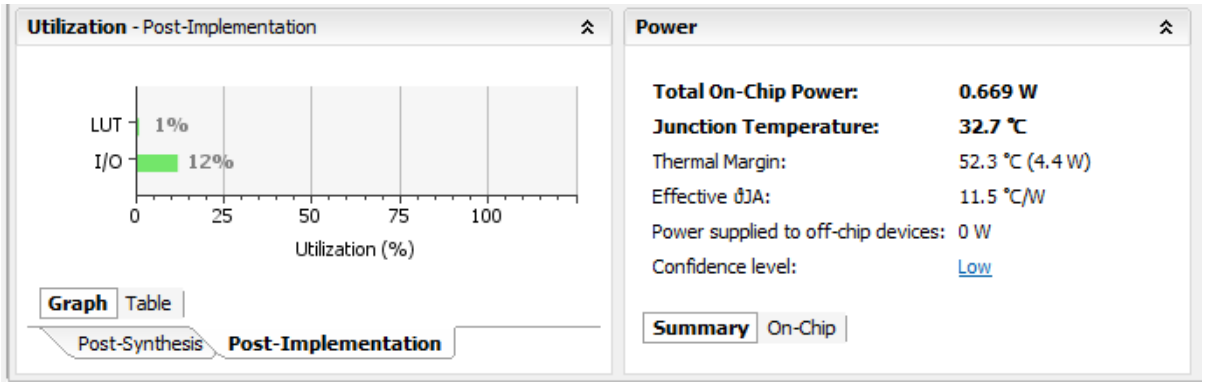

Figure 3.14 Project Summary of Implementing a 8x1 multiplexer using only 2x1 MUX

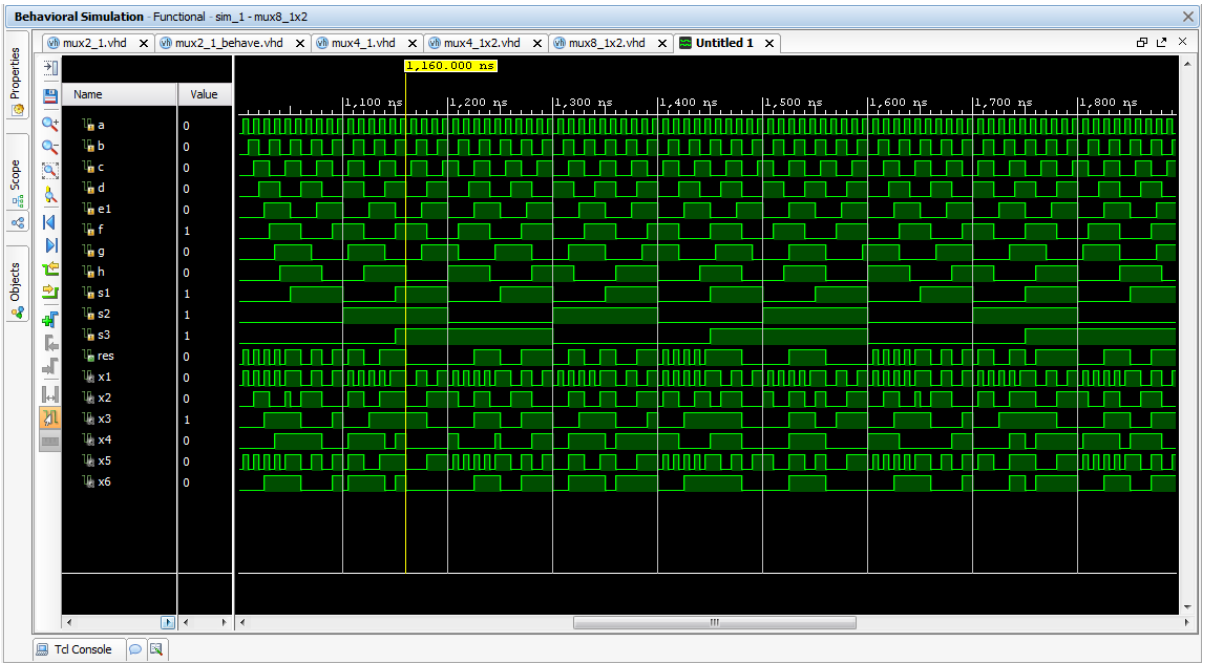

Figure 3.15 Simulation of Implementing a 8x1 multiplexer using only 2x1 MUX

3.5 Summary

Name of the Entity	No. of LUT used	Total On chip Power
Implementing a 2x1 multiplexer using dataflow modeling	1	0.458W
Implementing a 2x1 multiplexer using behavioral modeling	1	0.458W
Implementing a 4x1 multiplexer using dataflow modeling	1	0.454W
Implementing a 4x1 multiplexer using only 2x1 MUX	1	0.559W
Implementing a 8x1 multiplexer using only 2x1 MUX	2	0.669W

Table 3.1 comparision of Area and power requirements for different kinds of Multiplexers.