Digital Circuits and Systems Lab

Laboratory report submitted for the partial fulfillment
of the requirements for the degree of

Bachelor of Technology
in
Communication and Computer Engineering

by

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September 2018

Contents

Chapter *5*

Experiment - 5

5.1 Name of the Experiments

A. Implement 4 bit ripple carry adder using structural modeling.
B. Implement 4 bit adder/subtractor using structural modeling.

5.2 Theory

Addition of three bits result in two bits of sum and carry where
Sum = A XOR B XOR Cin
Carry = AB + BCin + CinA
In ripple carry addition, the previous carry bit is forwarded as the Cin for the addition of the next carry bit.
To implement subtraction using an adder, we use of the concept of 2's complement addition of a binary number,i.e, if we want to subtract a number, we can add its complement to gain the same result.
To implement this, we make use of the property of XOR gate to invert the output if one of the input is high. Hence if we want to subtract a number, we simply take its inverse and add it with an extra 1 to make its 2's complement. In doing so, we can get subtraction using the same ripple carry adder

5.3 Coding Techniques used

5.3.1 Structural modeling

Structural Modeling is the set of interconnected components. That is, it describes the structure. The visible components are instantiated in the declarative part of the architecture body while the declared components are instantiated with their respective interface ports in the statement part of the architecture body.
This method is used in both of the following experiments.

5.4 Simulation and Results

5.4.1 Using structural modeling, implement a 4 bit adder to add two 4 bit vectors

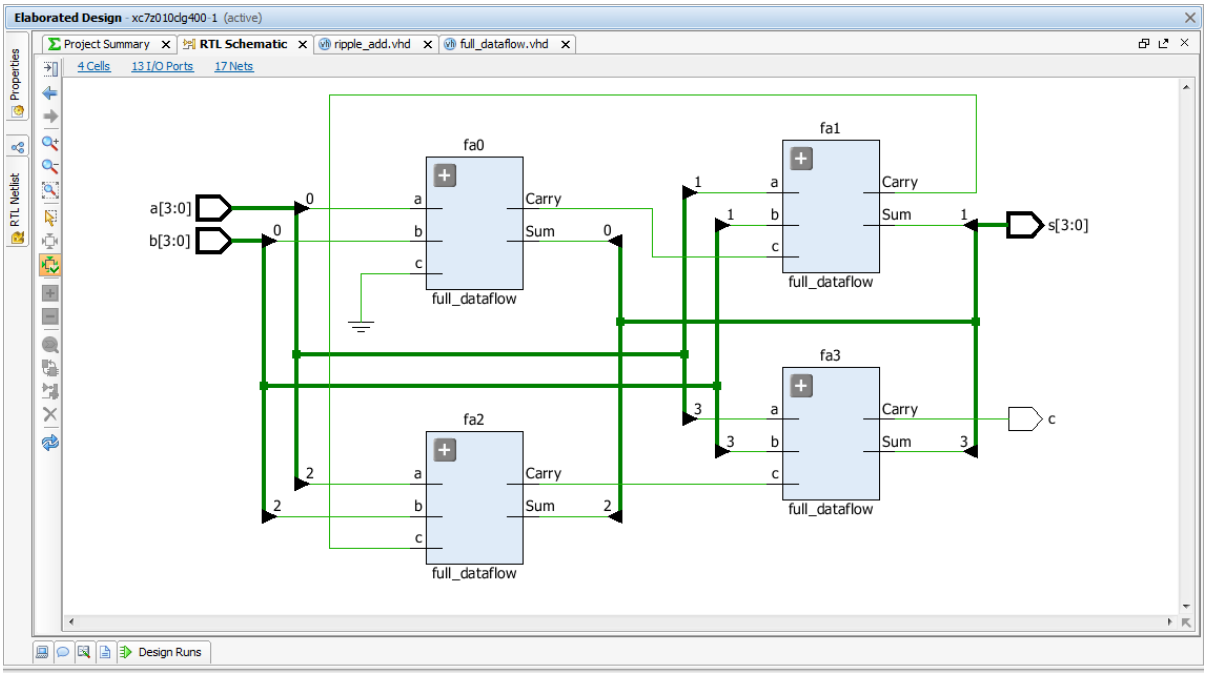

Figure 5.1 Schematic of implementing a 4 bit adder to add two 4 bit vectors

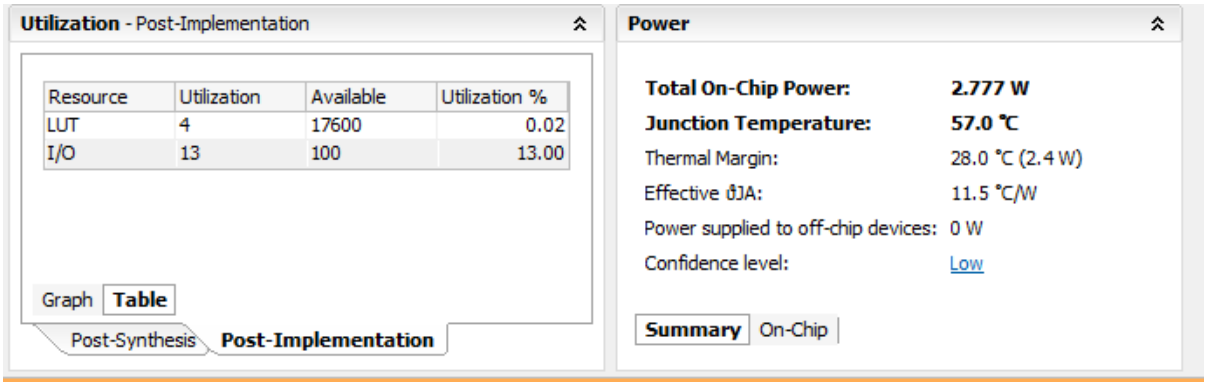

Figure 5.2 Project Summary of implementing a 4 bit adder to add two 4 bit vectors

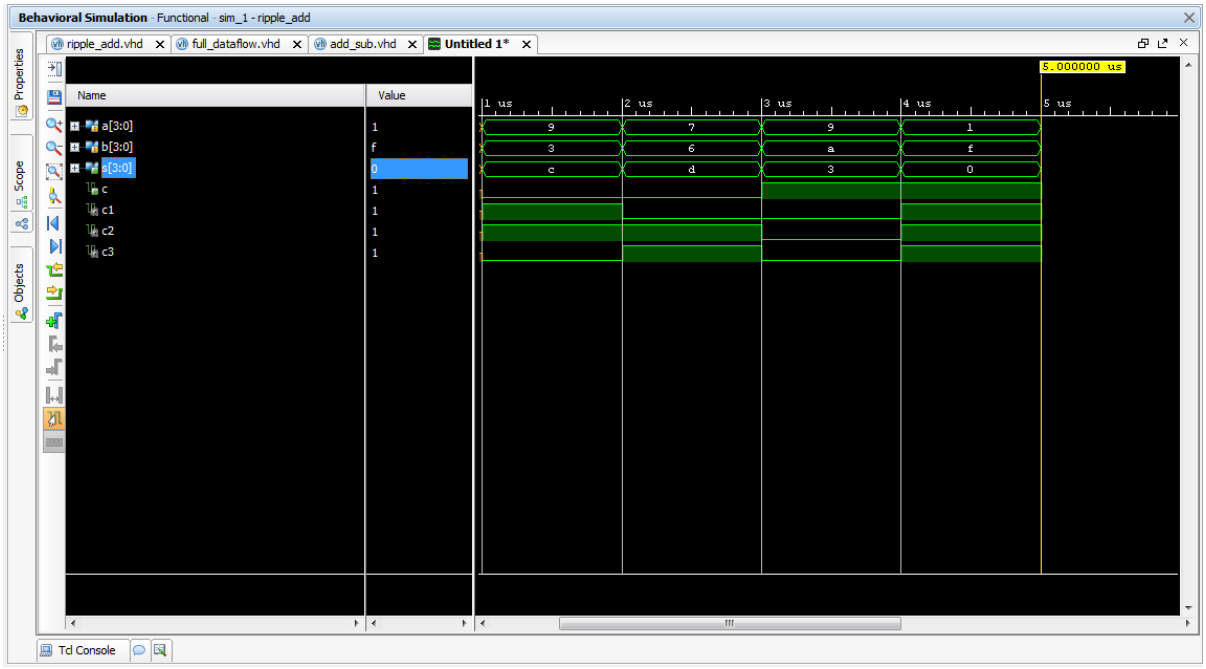

Figure 5.3 Simulation of implementing a 4 bit adder to add two 4 bit vectors

5.4.2 Using structural modeling, implement a 4 bit adder/ subtractor to add/subtract two 4 bit vectors A and B with Control input as M

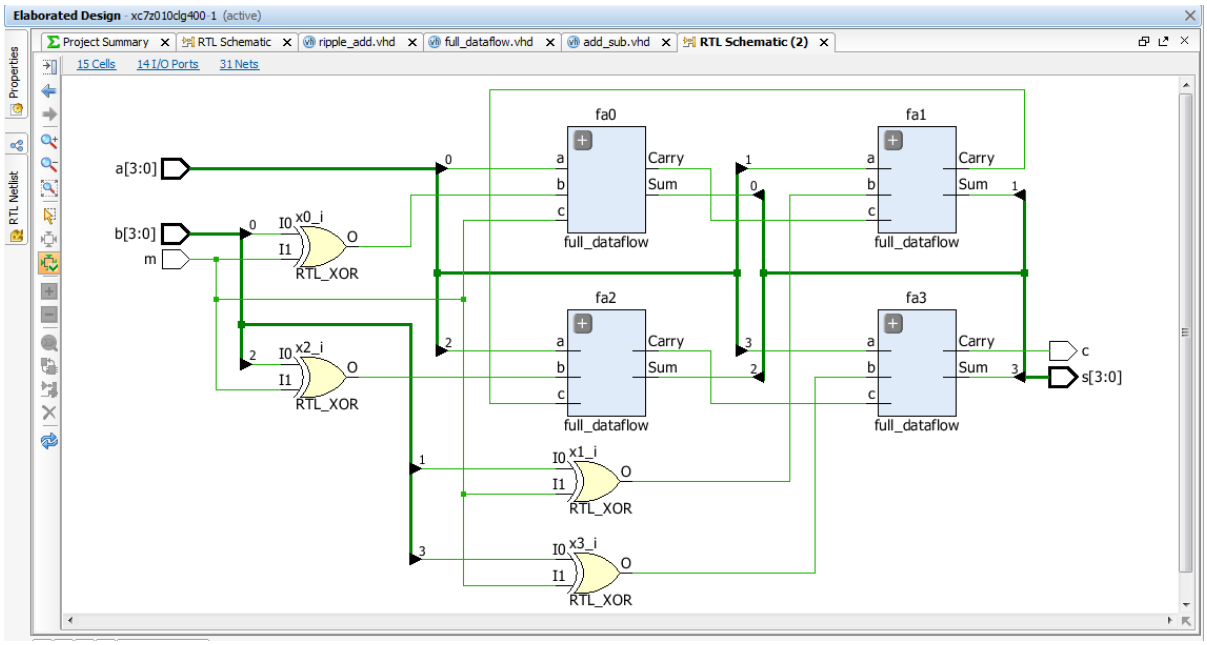

Figure 5.4 Schematic of implementing a 4 bit adder/ subtractor.

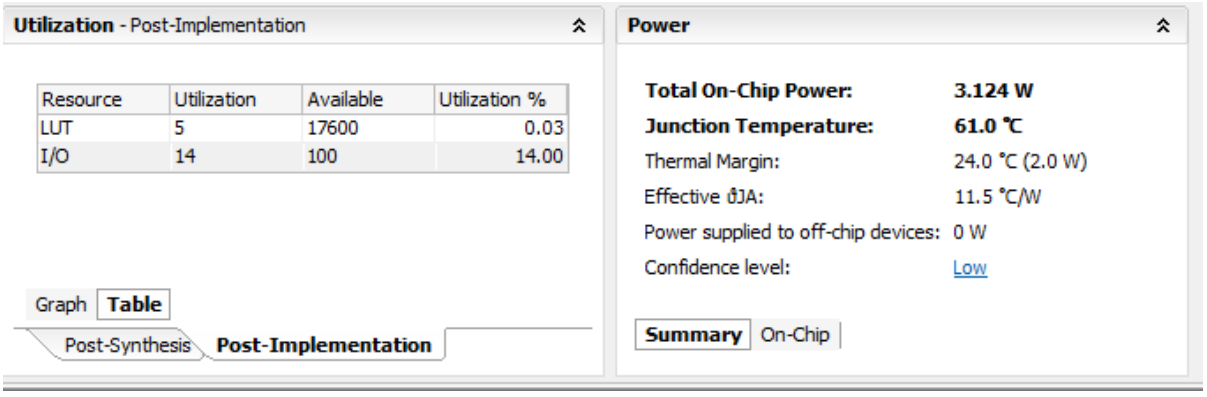

Figure 5.5 Project Summary of implementing a 4 bit adder/ subtractor.

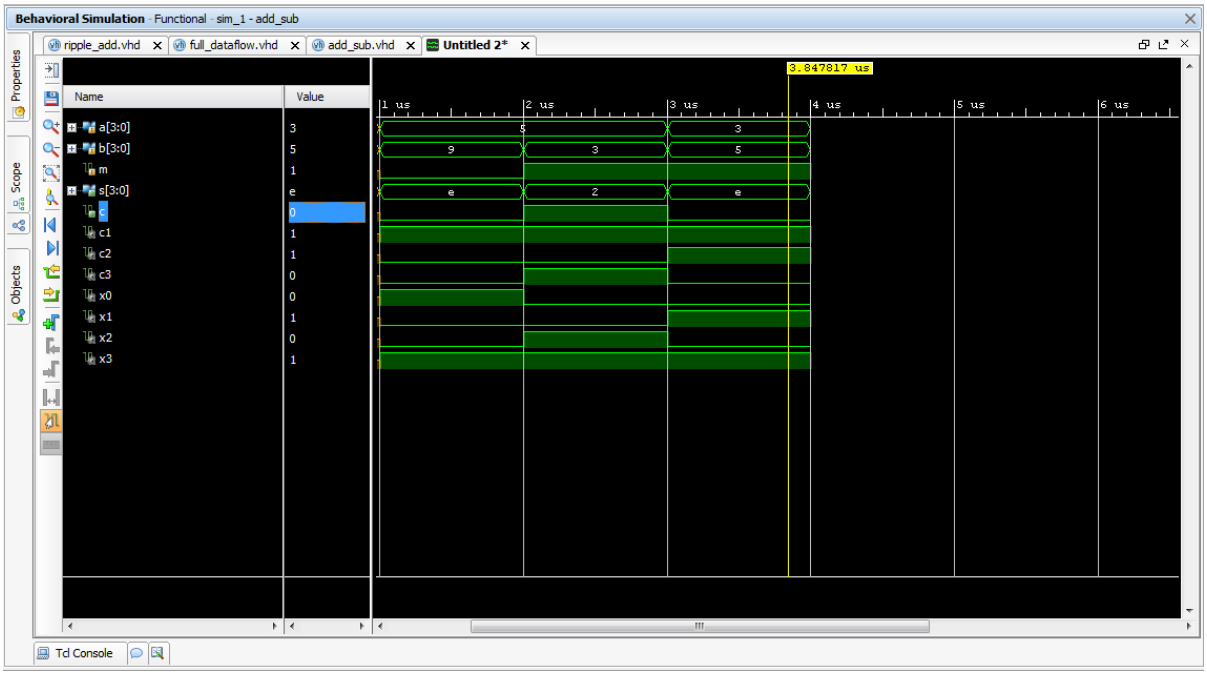

Figure 5.6 Simulation of implementing a 4 bit adder/ subtractor.

5.5 Summary

Name of the Entity	No. of LUT used	Total On chip Power
Implement a 4 bit adder to add two 4 bit vectors	4	2.777W
Implement a 4 bit adder/ subtractor with Control input as M	5	3.124W

Table 5.1 comparision of Area and power requirements for different kinds of methods.