Digital Circuits and Systems Lab

Laboratory report submitted for the partial fulfillment
of the requirements for the degree of

Bachelor of Technology
in
Communication and Computer Engineering

by

Anushrut - Roll No. 17UCC072

Course Coordinator
Dr. Kusum Lata

Department of Electronics and Communication Engineering
The LNM Institute of Information Technology, Jaipur

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Contents

Chapter *2*

Experiment - 2

2.1 Name of the Experiments

Realize the function, mentioned below in at least four different physical ways:
F(x) = x0 + x1 + x2 + x3 + x4 + x5 + x6 + x7 + x8 + x9

2.2 Theory

The '+' operator in boolean expression represents the "OR" operation which defines that if any of the given inputs are true then regardless of the other inputs of the expression,the resultant expression must be true.

2.3 Coding Techniques used

2.3.1 Data flow modeling

Dataflow Modeling includes declaration of a target signal using logical events occurring on the particular signal. Dataflow Modeling is primarily expressed using signal assignment statements.

2.3.2 Structural modeling

Structural Modeling is the set of interconnected components. That is, it describes the structure. The visible components are instantiated in the declarative part of the architecture body while the declared components are instantiated with their respective interface ports in the statement part of the architecture body.

2.4 Simulation and Results

2.4.1 Implement the Function F(x) using 8 stages of 2 input OR gates

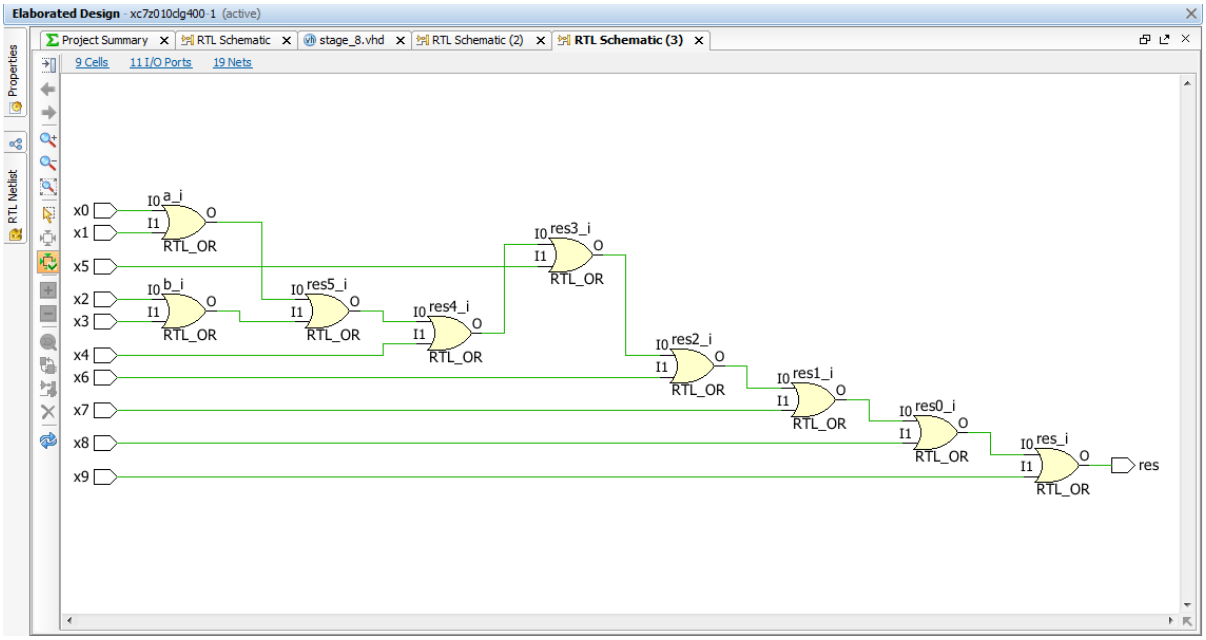

Figure 2.1 Schematic of Function F(x) using 8 stages of 2 input OR gates

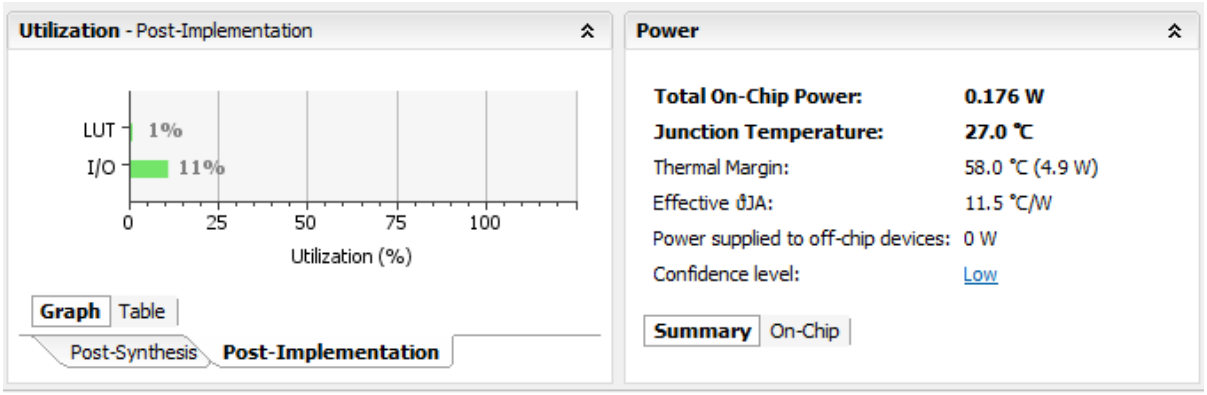

Figure 2.2 Project Summary of Function F(x) using 8 stages of 2 input OR gates

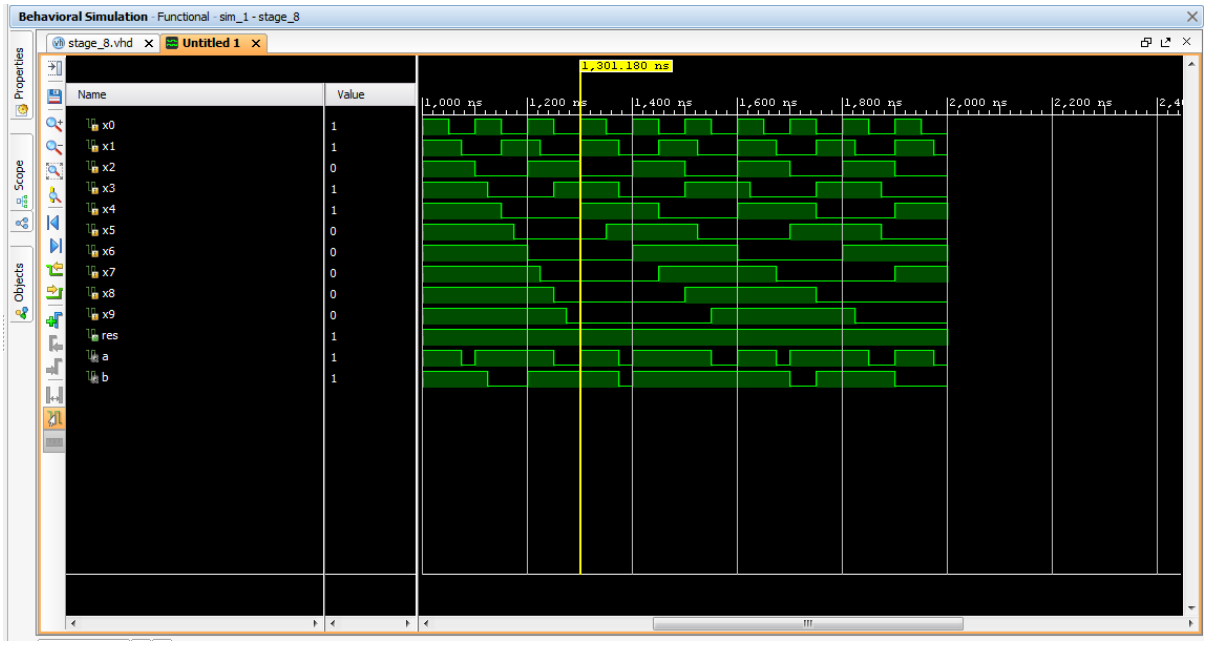

Figure 2.3 Simulation of Function F(x) using 8 stages of 2 input OR gates

2.4.2 Implement F(x) using three 4 different input OR gates

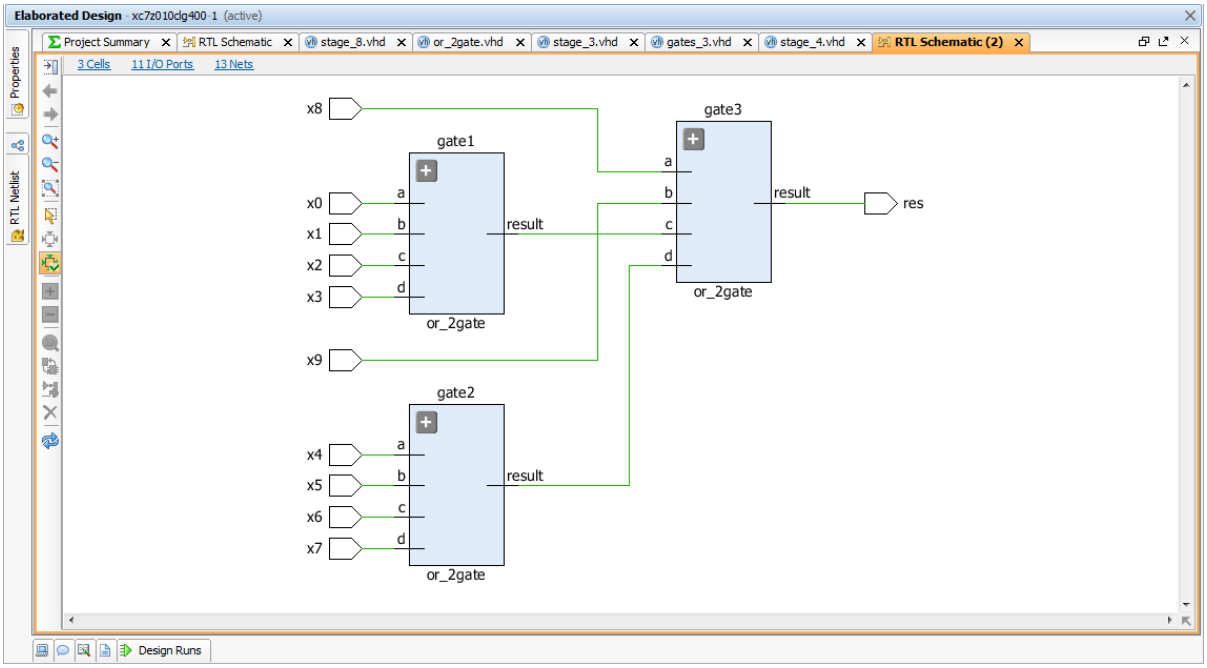

Figure 2.4 Schematic of F(x) using three 4 different input OR gates

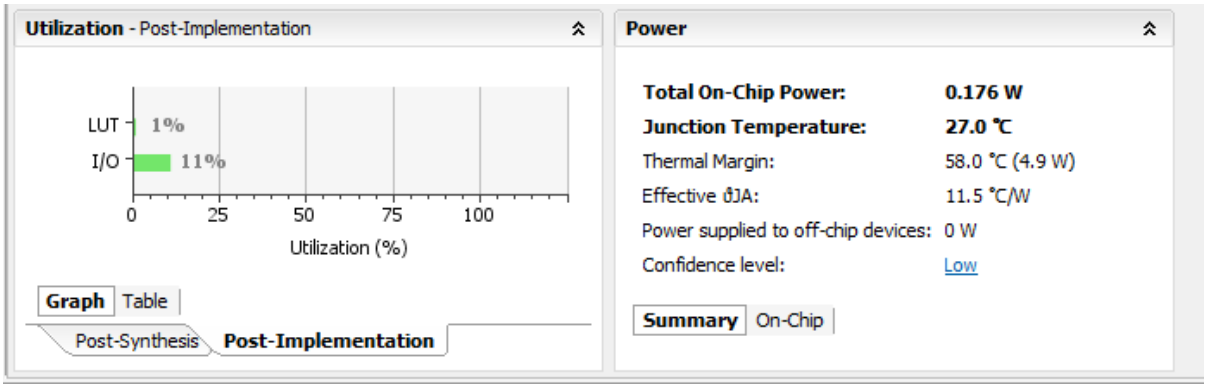

Figure 2.5 Project Summary of F(x) using three 4 different input OR gates

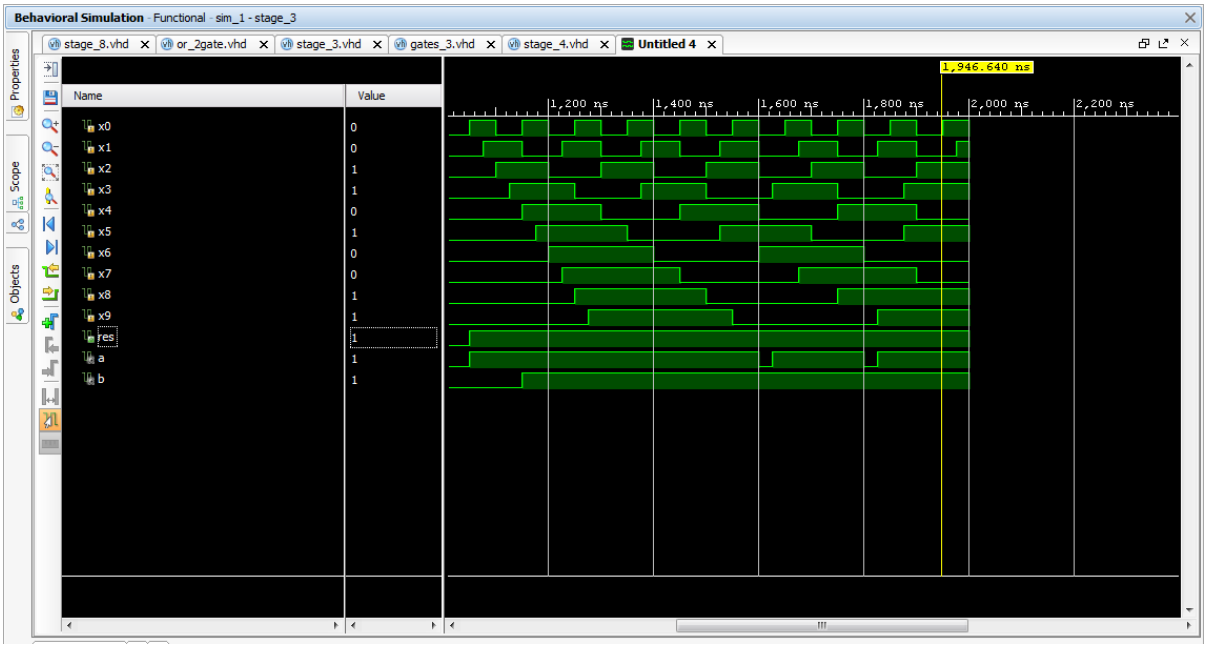

Figure 2.6 Simulation of F(x) using three 4 different input OR gates

2.4.3 Implement F(x) as a three stage network.

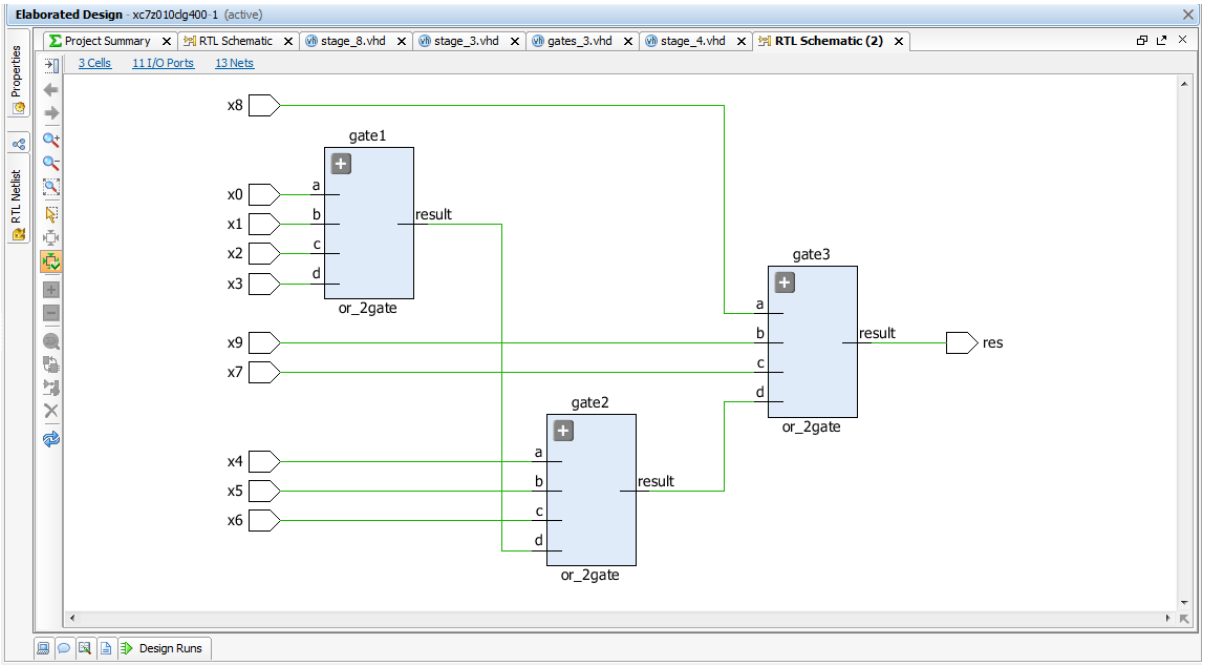

Figure 2.7 Schematic of F(x) as a three stage network.

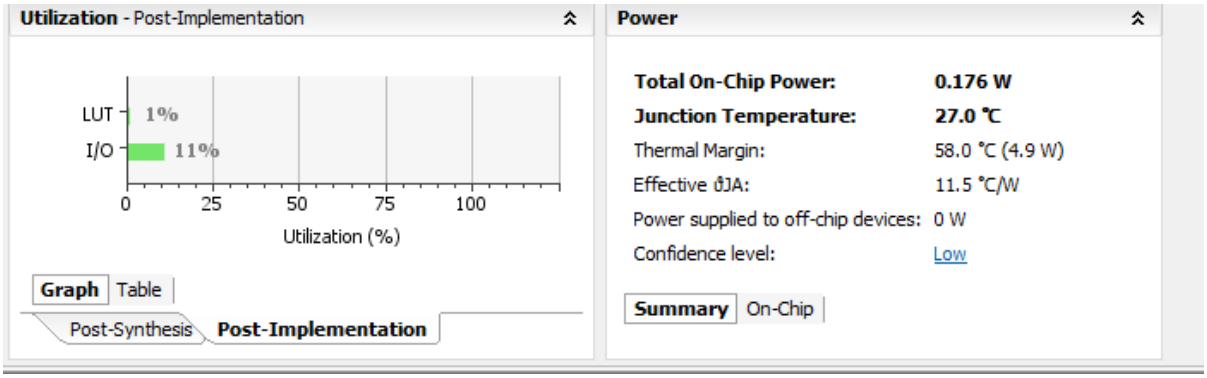

Figure 2.8 Project Summary of F(x) as a three stage network.

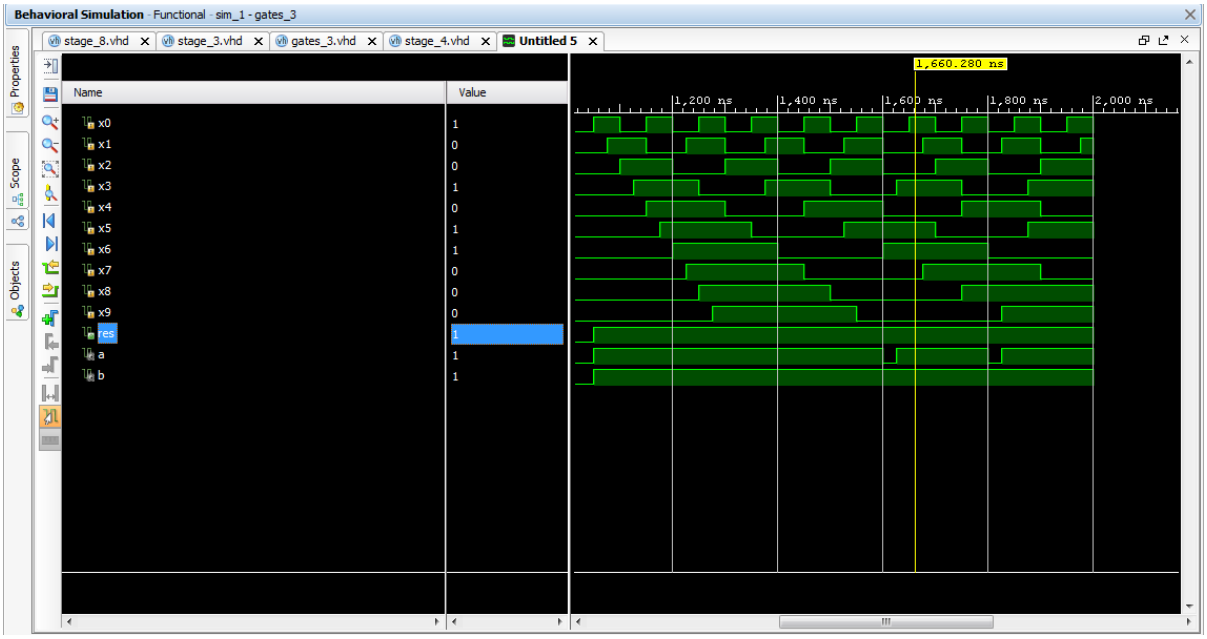

Figure 2.9 Simulation of F(x) as a three stage network.

2.4.4 Implement F(x) as a 4 stage network.

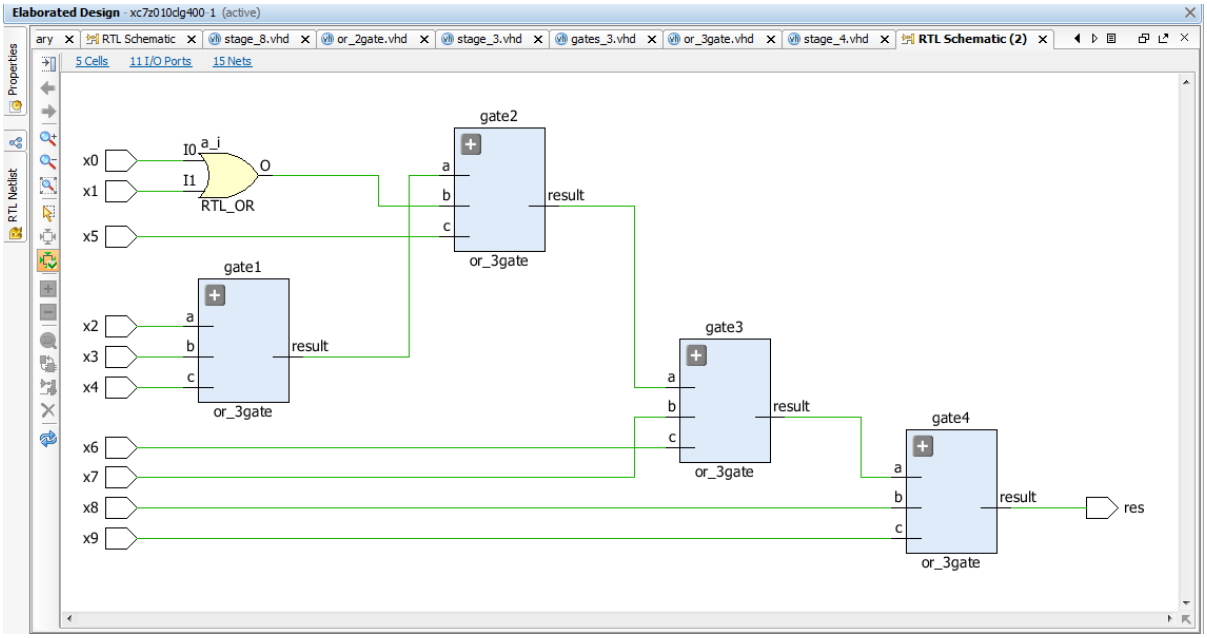

Figure 2.10 Schematic of F(x) as a 4 stage network

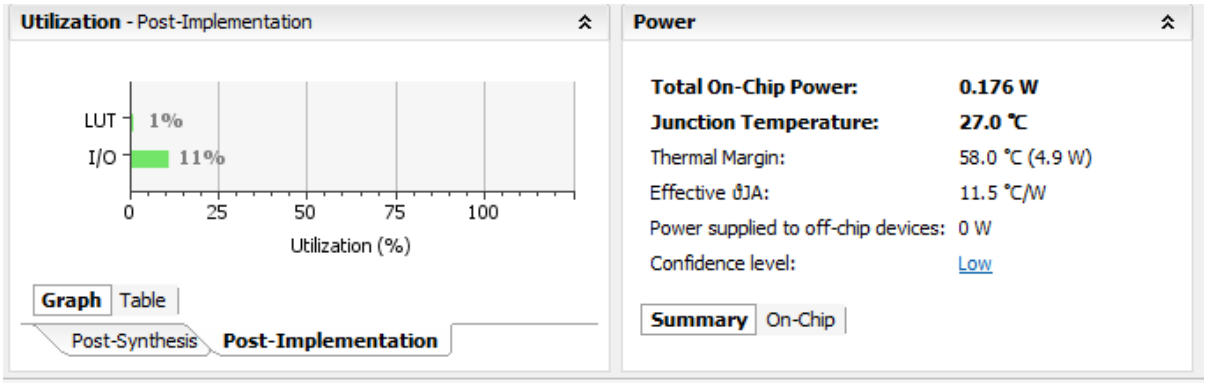

Figure 2.11 Project Summary of F(x) as a 4 stage network

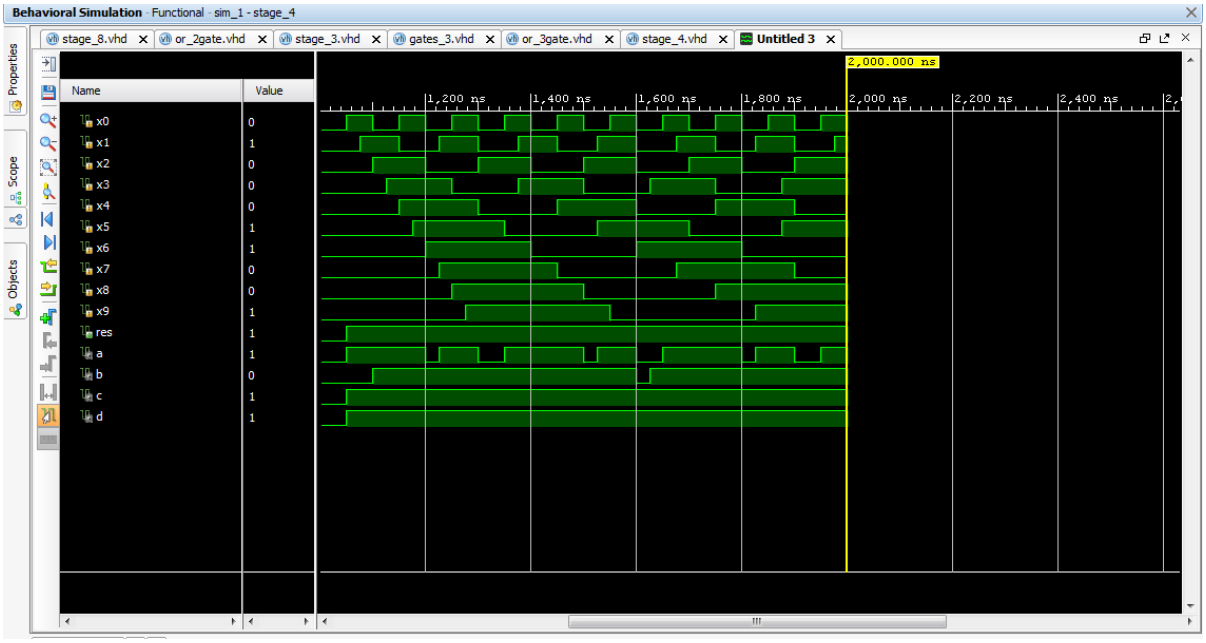

Figure 2.12 Simulation of F(x) as a 4 stage network

2.5 Summary

Name of the Entity	No. of LUT used	Total On chip Power
F(x) using 8 stages of 2 input OR gates	2	0.176W
F(x) using three 4 different inputs OR gate	2	0.176W
F(x) as 3 stage-network	2	0.176W
F(x) as 4 stage-network	2	0.176W

Table 2.1 comparision of Area and power requirements for different kinds of methods.