Digital Circuits and Systems Lab

Laboratory report submitted for the partial fulfillment
of the requirements for the degree of

Bachelor of Technology
in
Communication and Computer Engineering

by

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November 2018

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Chapter *8*

Experiment - 8

8.1 Name of the Experiments

Sequential system design using state Machines:
1. MOD 4 up/down counter with Reset and control signal Count using Finite state machines
2. Sequential System to detect pattern 1101 in a sequence of 0's and 1's.

8.2 Theory

A counter is a device to count by advancing the contents of the counter by one count with each clock pulse.
Counters which increase with a clock input are said to operate in a count-up mode. Likewise, counters which decrease their sequence with a clock input are said to operate in a count-down mode.
Counters that operate in both the UP and DOWN modes, are called bidirectional counters.
MOD counters, are defined based on the number of states that the counter will sequence through before returning back to its original value.

A sequence detector is a sequential state machine which takes an input of bits and generates an output 1 whenever the target sequence has been detected

8.3 Coding Techniques used

8.3.1 Behavioral modeling by using If statement

Behavioral Modeling deals with the functionality of an entity. Here, the set of statements are executed sequentially in a specified order, mainly specified within a process statement. The process statement is itself a concurrent statement but inside it lies a set of statements which are all sequential in nature. This modeling is shown by implementing the mod 4 counter and the Sequence detector.

8.4 Simulation and Results

8.4.1 MOD 4 up/down counter with Reset and control signal Count using Finite state machines

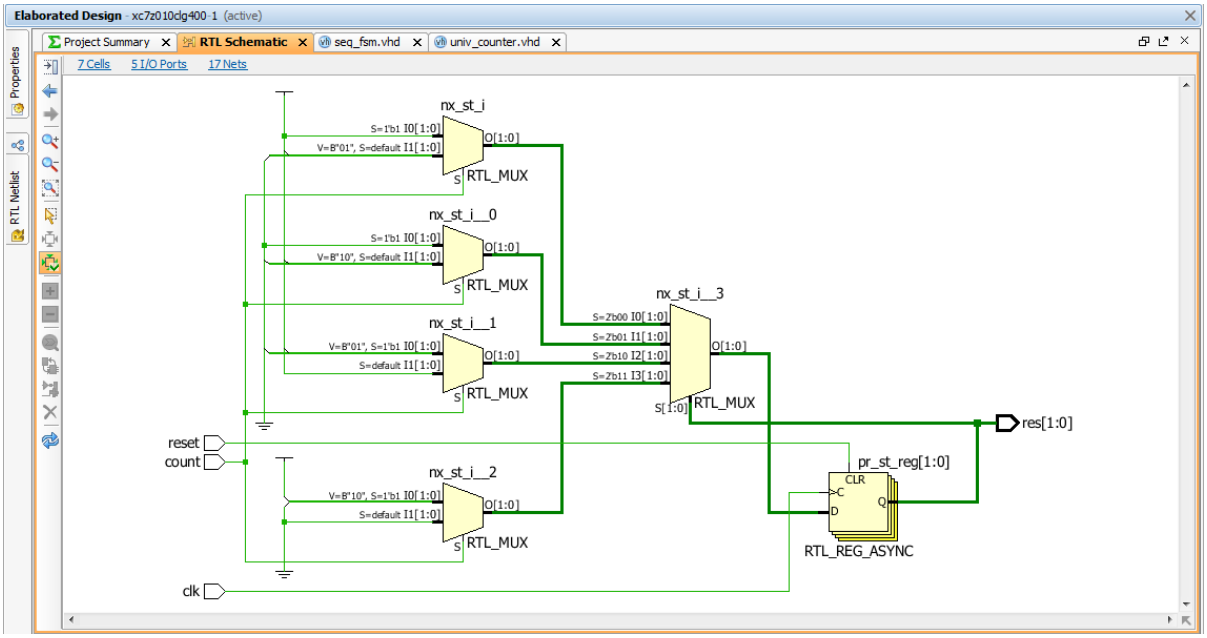

Figure 8.1 Schematic of implementing a MOD 4 up/down counter

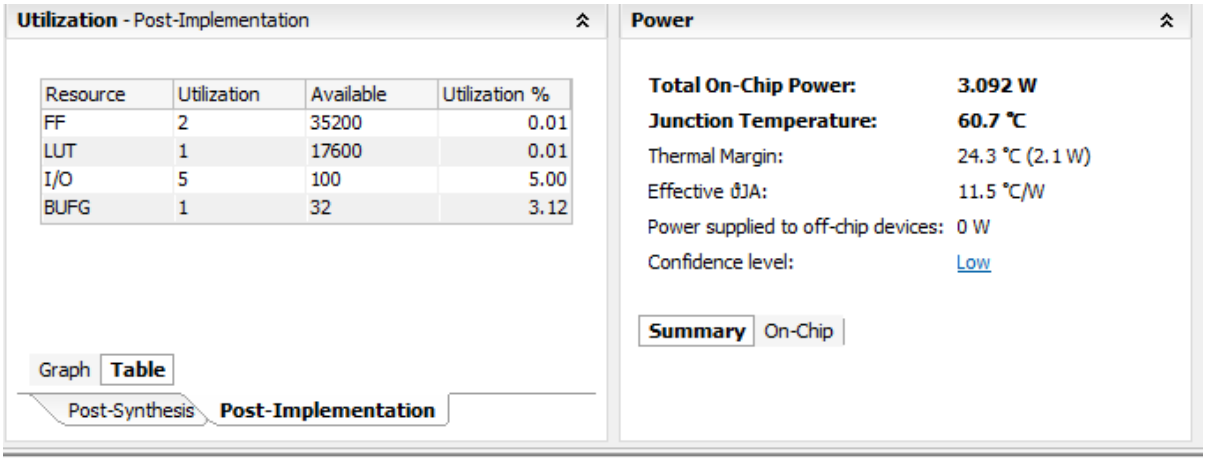

Figure 8.2 Project Summary of implementing a MOD 4 up/down counter

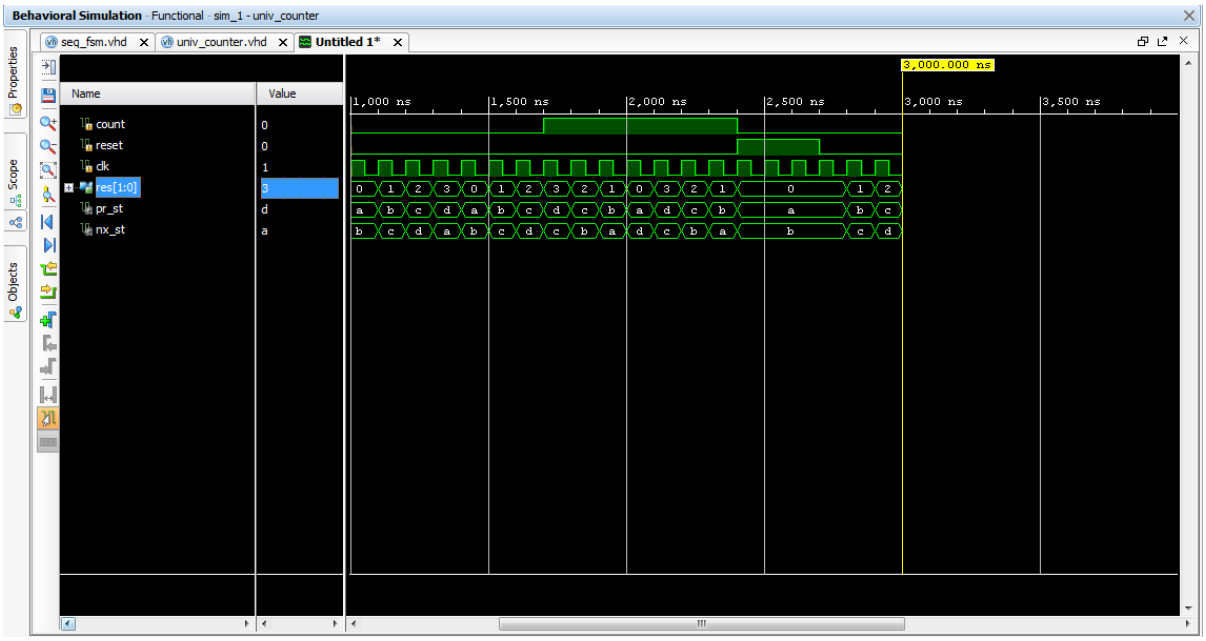

Figure 8.3 Simulation of implementing a MOD 4 up/down counter

8.4.2 Sequential System to detect pattern 1101 in a sequence of 0's and 1's.

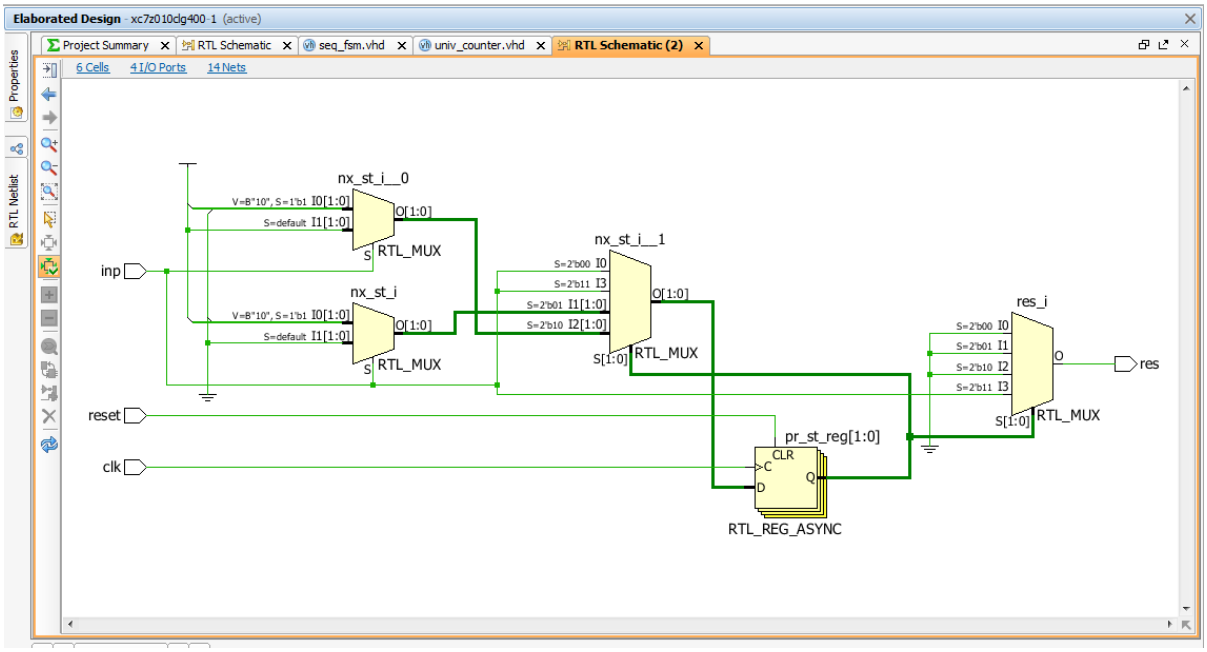

Figure 8.4 Schematic of implementing Sequential System to detect pattern.

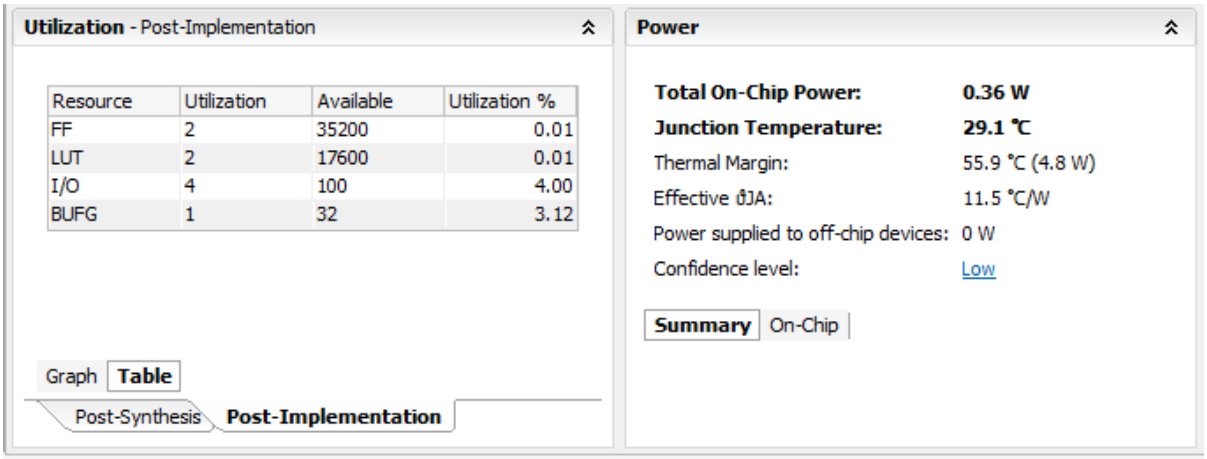

Figure 8.5 Project Summary of implementing Sequential System to detect pattern.

Figure 8.6 Simulation of implementing Sequential System to detect pattern.

8.5 Summary

Name of the Entity	No. of LUT used	Total On chip Power
Implementing a MOD 4 up/down counter	1	3.092W
Implementing Sequential System to detect pattern.	2	0.36W

Table 8.1 comparision of Area and power requirements for different kinds of methods.