Digital Circuits and Systems Lab

Laboratory report submitted for the partial fulfillment
of the requirements for the degree of

Bachelor of Technology
in
Communication and Computer Engineering

by

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Contents

Chapter *9*

Experiment - 9

9.1 Name of the Experiments

Counters and its applications:
1. Modulo 16 counter with 4 bit parallel input I, control signals clock, clear, count enable, load and 4 bit output S and one bit output Terminal count.
2. Using modulo 16 counter designing a 2 to 12 counter.

9.2 Theory

In Synchronous Counter, the external clock signal is connected to the clock input of EVERY individual flip-flop within the counter so that all of the flip-flops are clocked together simultaneously (in parallel) at the same time giving a fixed time relationship. In other words, changes in the output occur in synchronisation with the clock signal.
The result of this synchronisation is that all the individual output bits changing state at exactly the same time in response to the common clock signal with no ripple effect and therefore, no propagation delay.

9.3 Coding Techniques used

9.3.1 Structural modeling

Structural Modeling is the set of interconnected components. That is, it describes the structure. The visible components are instantiated in the declarative part of the architecture body while the declared components are instantiated with their respective interface ports in the statement part of the architecture body. This modeling is shown by implementing a 2 to 12 counter using modulo 16 counter

9.3.2 Behavioral modeling by using If statement

Behavioral Modeling deals with the functionality of an entity. Here, the set of statements are executed sequentially in a specified order, mainly specified within a process statement. The process statement is itself a concurrent statement but inside it lies a set of statements which are all sequential in nature.
This modeling is shown by implementing a modulo 16 counter

9.4 Simulation and Results

9.4.1 Modulo 16 counter with 4 bit parallel input I, control signals clock, clear, count enable, load and 4 bit output S and one bit output Terminal count.

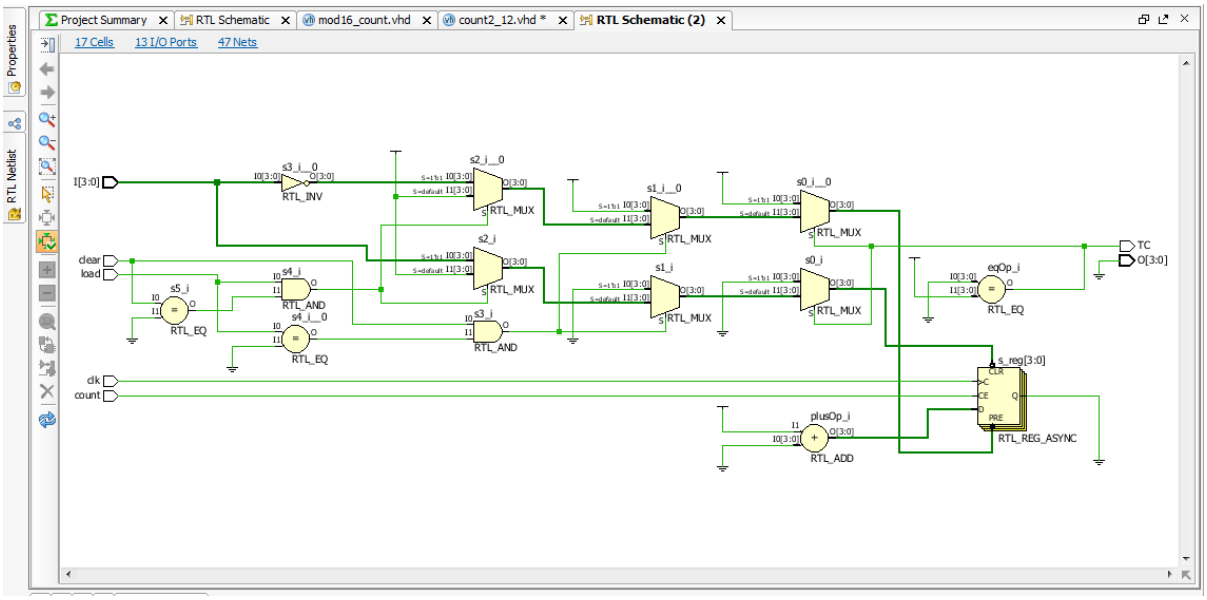

Figure 9.1 Schematic of implementing a Modulo 16 counter

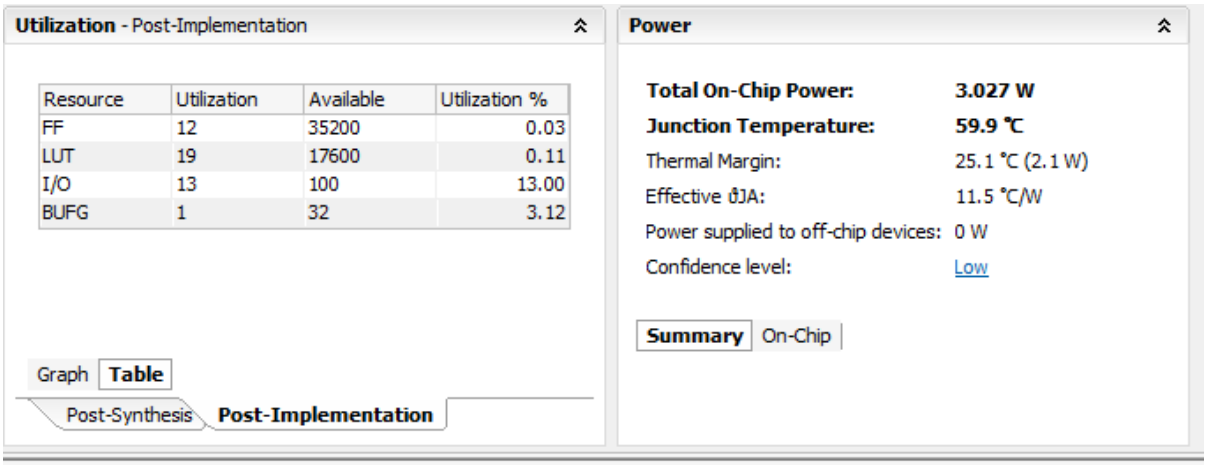

Figure 9.2 Project Summary of implementing a Modulo 16 counter

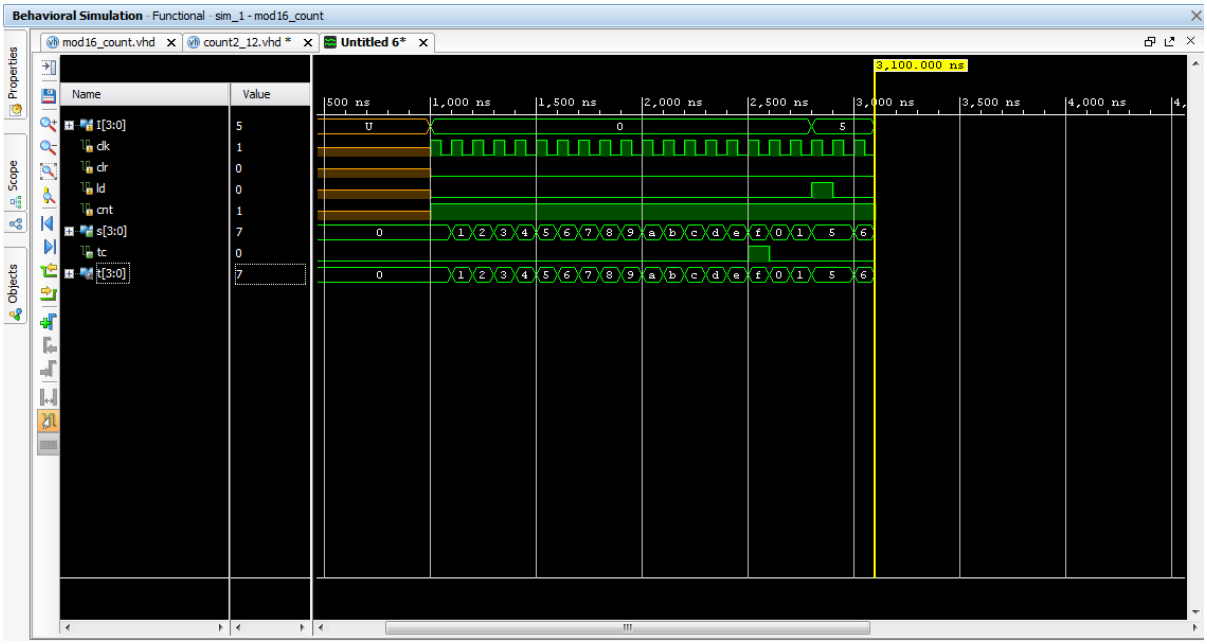

Figure 9.3 Simulation of implementing a Modulo 16 counter

9.4.2 Using modulo 16 counter designing a 2 to 12 counter.

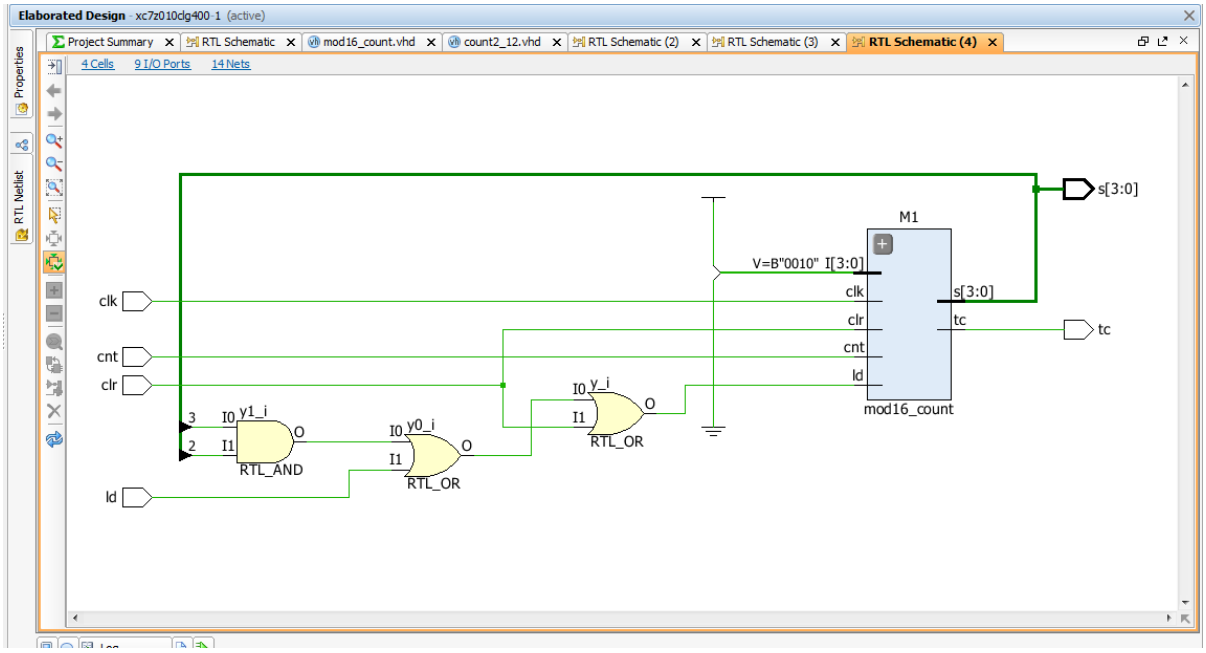

Figure 9.4 Schematic of implementing a 2 to 12 counter.

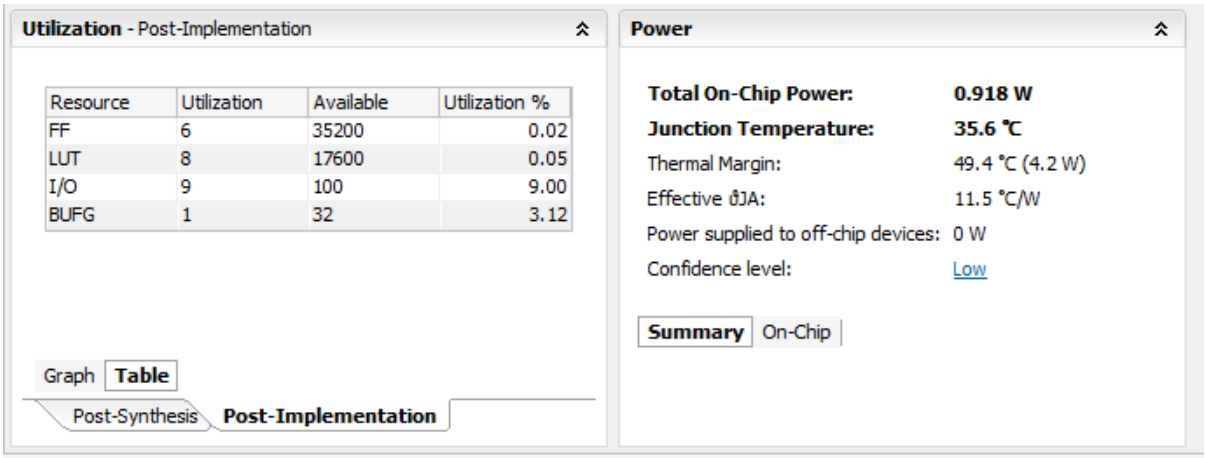

Figure 9.5 Project Summary of implementing a 2 to 12 counter.

Figure 9.6 Simulation of implementing a 2 to 12 counter.

9.5 Summary

Name of the Entity	No. of LUT used	Total On chip Power
Implementing a Modulo 16 counter	19	3.027W
Implementing a 2 to 12 counter	8	0.918w

Table 9.1 comparision of Area and power requirements for different kinds of methods.