Digital Circuits and Systems Lab

Laboratory report submitted for the partial fulfillment
of the requirements for the degree of

Bachelor of Technology
in
Communication and Computer Engineering

by

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Chapter *7*

Experiment - 7

7.1 Name of the Experiments

Shift Register Design Using VHDL:
1. 8-bit Shift-Left Register with Negative-Edge Clock, Clock Enable, Serial In, and Serial Out.
2. 8-bit shift Register with Reset,Serial In and Serial Out.
3. 8-bit Shift-Left Register with Positive-Edge Clock, Serial In, and Parallel Out.
4. 16 bit Shift-Left Register with Positive-Edge Clock, Serial In, and Parallel Out using 2 8-bit Shift Registers

7.2 Theory

The Shift Register is a type of sequential logic circuit that can be used for the storage or the transfer of binary data. It is a cascade of flip flops, in which the output of each flip-flop is connected to the 'data' input of the next flip-flop in a chain, resulting in a circuit that shifts by one position the 'bit array' stored in it, 'shifting in' the data present at its input and 'shifting out' the last bit in the array, at each transition of the clock input.
Shift Registers are used for data storage or for the movement of data. The individual data latches that make up a single shift register are all driven by a common clock signal making them synchronous devices.

Serial In, Serial Out : the data is shifted serially IN and OUT of the register, one bit at a time in either a left or right direction under clock control.

Serial in, Parallel Out : the register is loaded with serial data, one bit at a time, with the stored data being available at the output in parallel form.

7.3 Coding Techniques used

7.3.1 Structural modeling

Structural Modeling is the set of interconnected components. That is, it describes the structure. The visible components are instantiated in the declarative part of the architecture body while the declared components are instantiated with their respective interface ports in the statement part of the architecture body.
This modeling is shown by implementing 8-bit Serial In, Serial Out and Serial In, Parallel Out Registers.

7.3.2 Behavioral modeling by using If statement

Behavioral Modeling deals with the functionality of an entity. Here, the set of statements are executed sequentially in a specified order, mainly specified within a process statement. The process statement is itself a concurrent statement but inside it lies a set of statements which are all sequential in nature.
This modeling is shown by implementing a 16-bit Register using 2 8-bit Serial In, Parallel Out Registers.

7.4 Simulation and Results

7.4.1 8-bit Shift-Left Register with Negative-Edge Clock, Clock Enable, Serial In, and Serial Out.

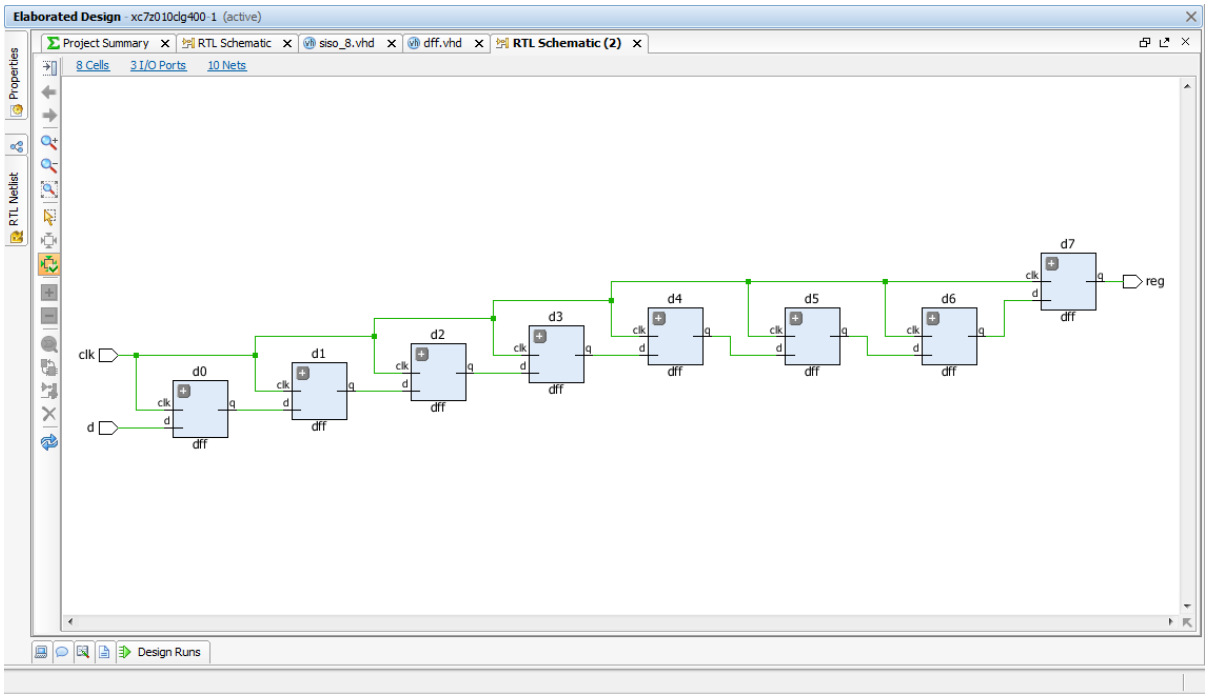

Figure 7.1 Schematic of implementing a 8-bit Shift-Left Register, SISO.

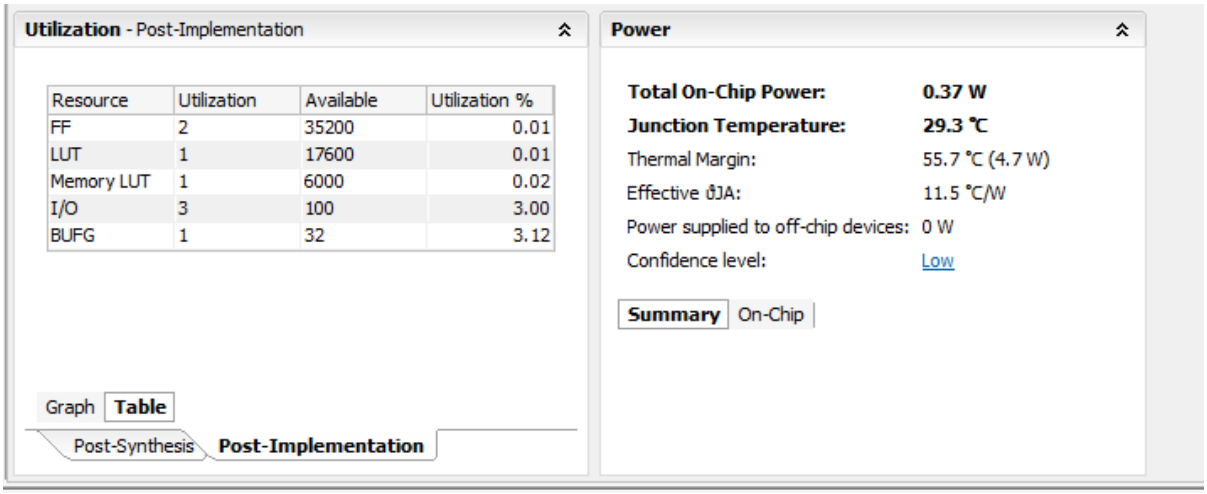

Figure 7.2 Project Summary of implementing a 8-bit Shift-Left Register, SISO.

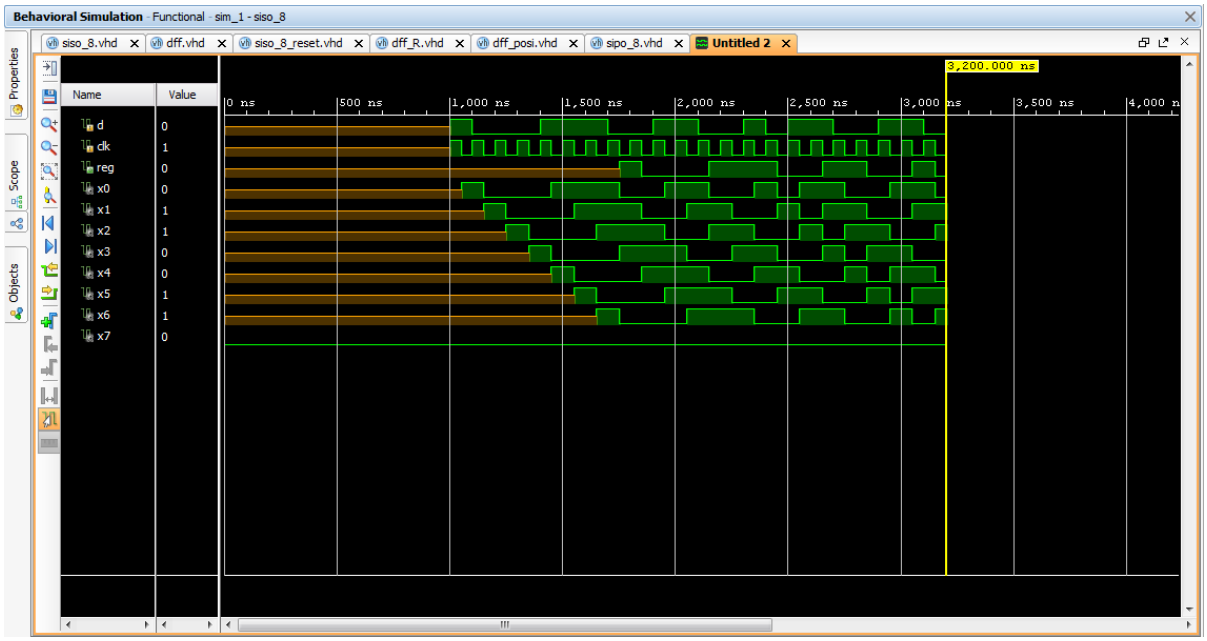

Figure 7.3 Simulation of implementing a 8-bit Shift-Left Register, SISO.

7.4.2 8-bit shift Register with Reset,Serial In and Serial Out.

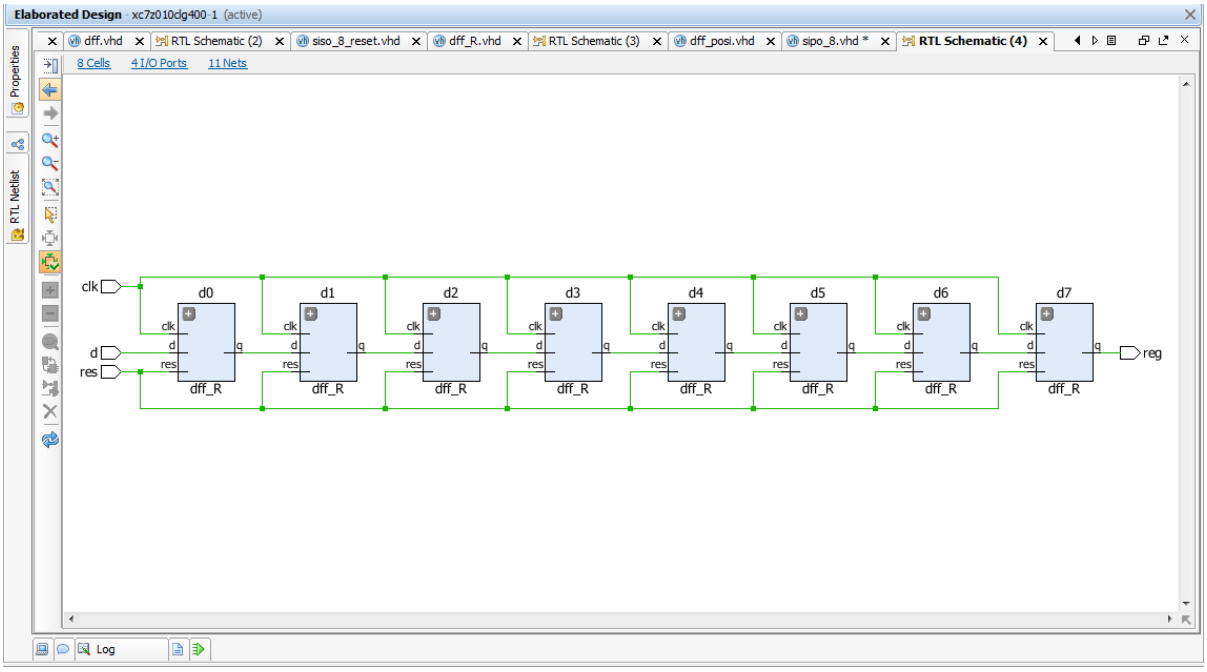

Figure 7.4 Schematic of implementing a 8-bit shift Register with Reset,SISO.

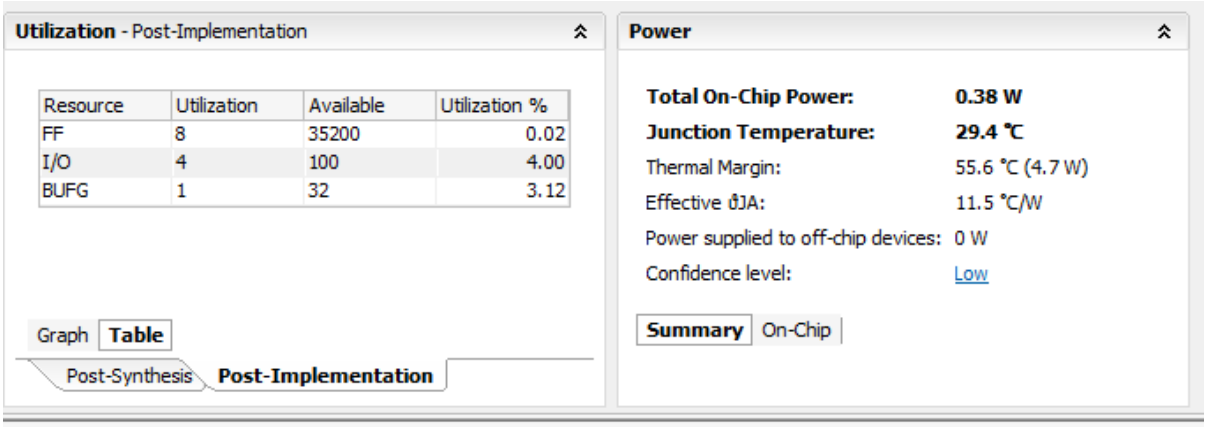

Figure 7.5 Project Summary of implementing a 8-bit shift Register with Reset,SISO.

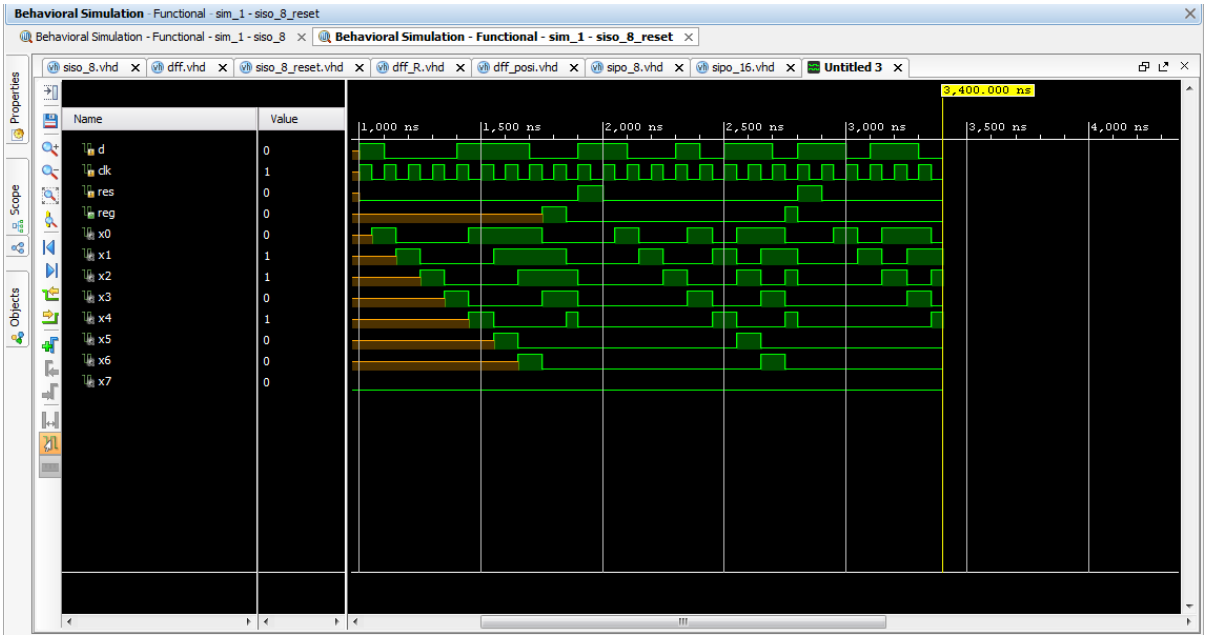

Figure 7.6 Simulation of implementing a 8-bit shift Register with Reset,SISO.

7.4.3 8-bit Shift-Left Register with Positive-Edge Clock, Serial In, and Parallel Out.

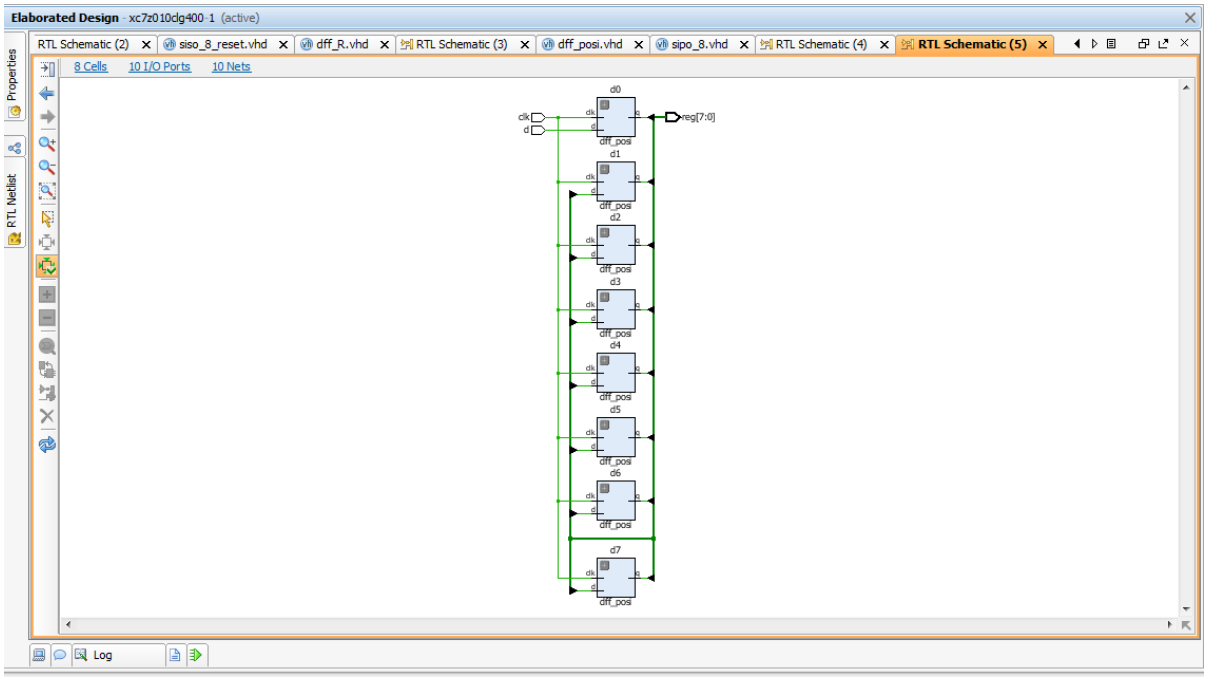

Figure 7.7 Schematic of Implementing a 8-bit Shift-Left Register, SIPO

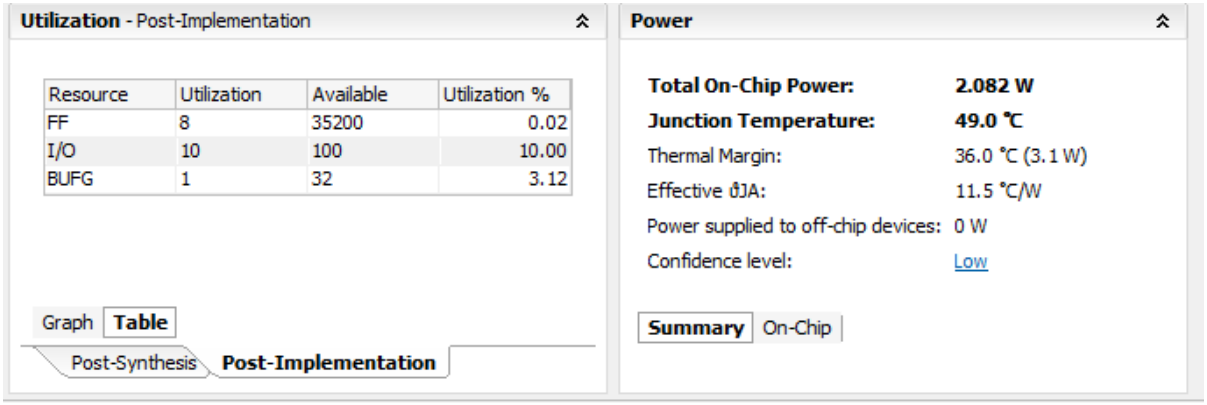

Figure 7.8 Project Summary of Implementing a 8-bit Shift-Left Register, SIPO

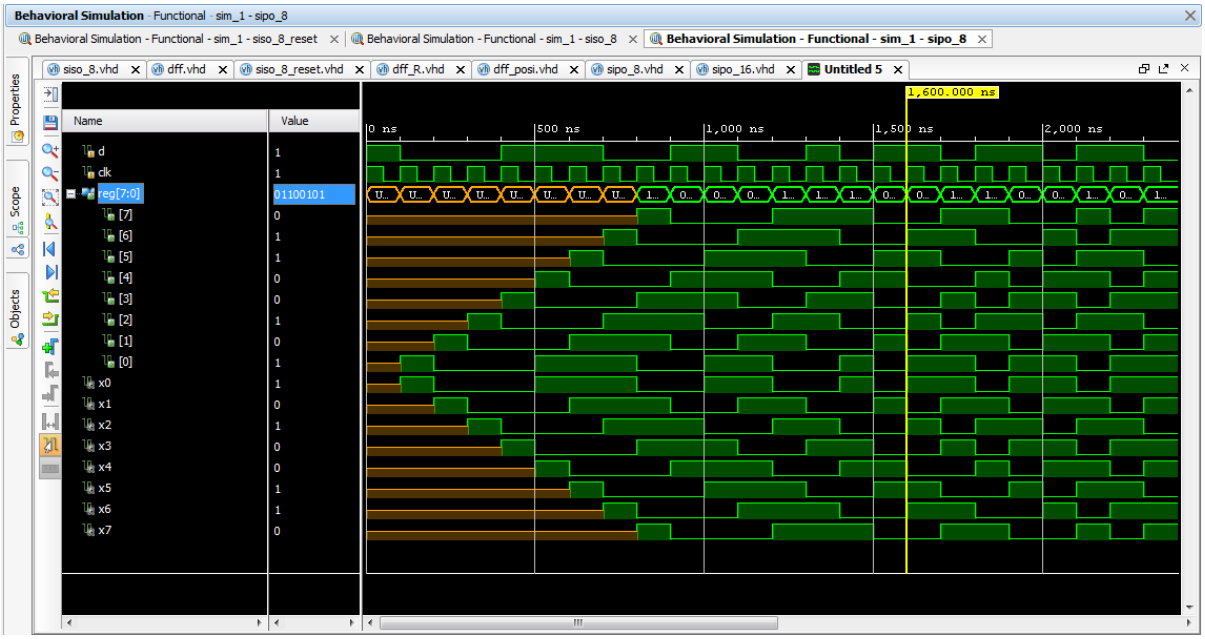

Figure 7.9 Simulation of Implementing a 8-bit Shift-Left Register, SIPO

7.4.4 16 bit Shift-Left Register with Positive-Edge Clock, Serial In, and Parallel Out using 2 8-bit Shift Registers

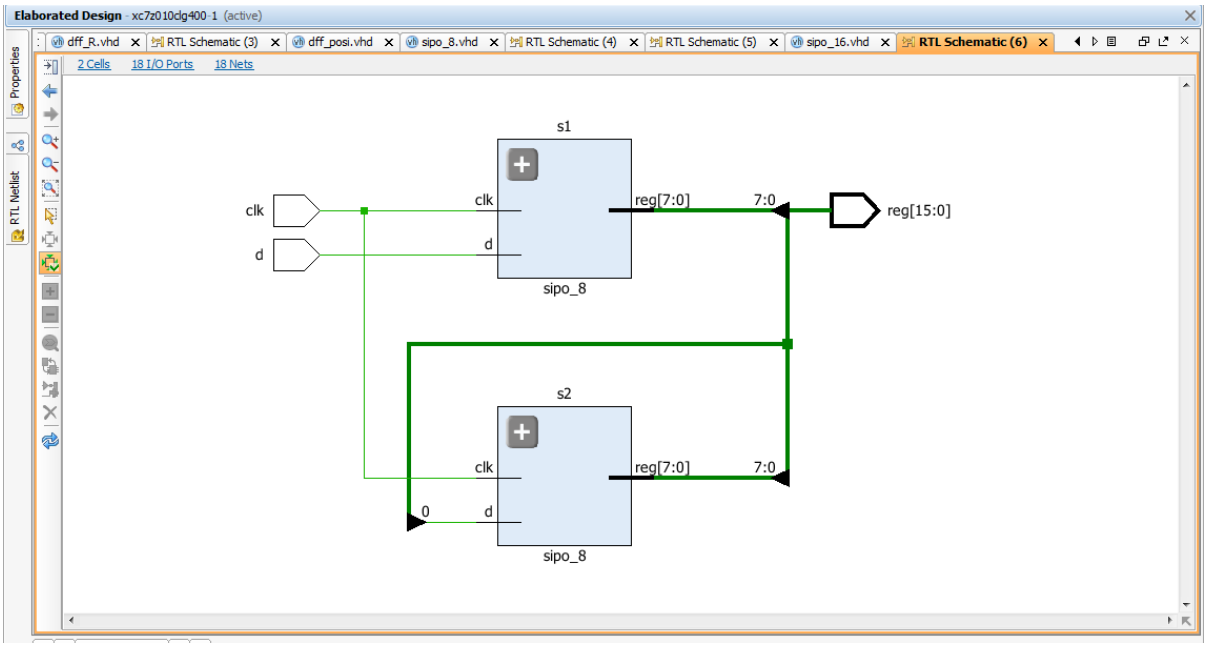

Figure 7.10 Schematic of implementing a 16 bit Shift-Left Register using Structural Modeling.

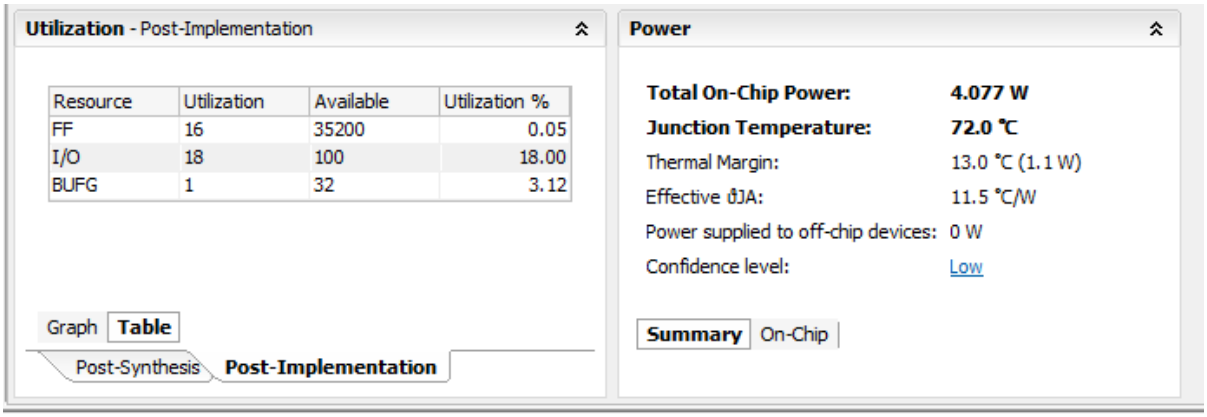

Figure 7.11 Project Summary of implementing a 16 bit Shift-Left Register using Structural Modeling.

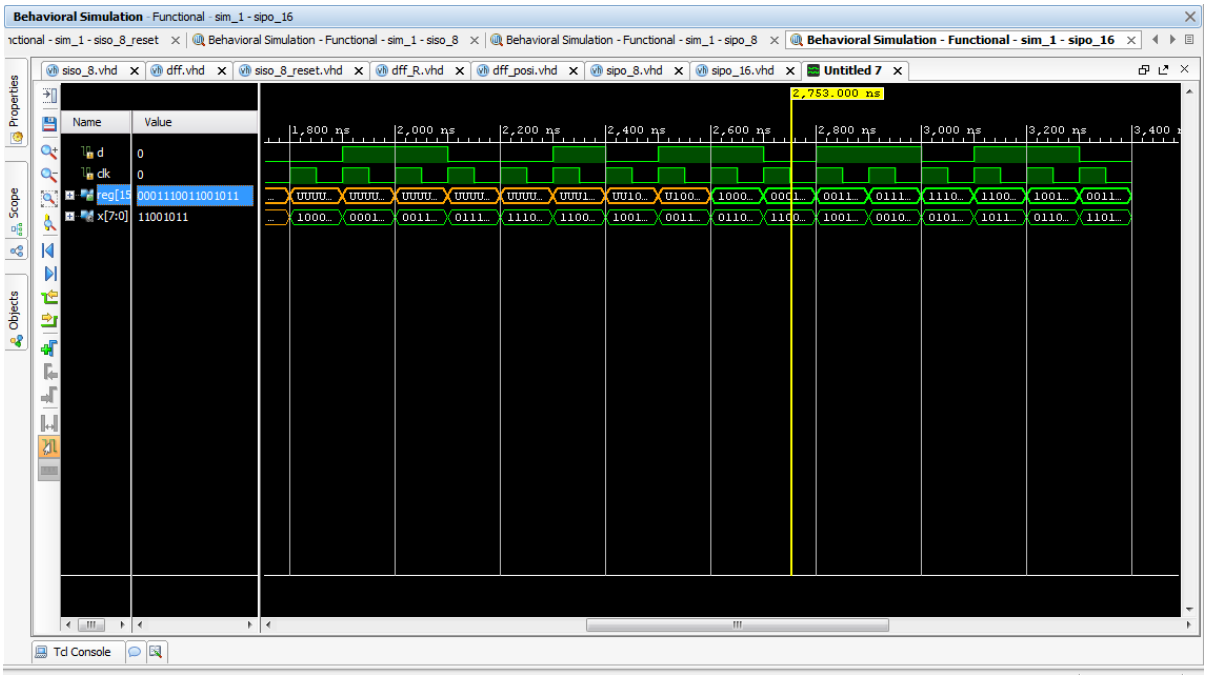

Figure 7.12 Simulation of implementing a 16 bit Shift-Left Register using Structural Modeling.

7.5 Summary

Name of the Entity	No. of FF used	Total On chip Power
Implementing a 8-bit Shift-Left Register, SISO.	2	0.37W
Implementing a 8-bit shift Register with Reset,SISO.	8	0.38W
Implementing a 8-bit Shift-Left Register, SIPO	8	2.082W
Implementing a 16 bit Shift-Left Register using Structural Modeling	16	4.077W

Table 7.1 comparision of Area and power requirements for different kinds of methods.