Digital Circuits and Systems Lab

Laboratory report submitted for the partial fulfillment
of the requirements for the degree of

Bachelor of Technology
in
Communication and Computer Engineering

by

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Contents

Chapter *1*

Experiment - 1

1.1 Name of the Experiments

Design, simulate and implement Half adder, Full adder using dataflow, behavioral and structural modeling in VHDL.

1.2 Theory

Half adders are used to take two inputs and provide two outputs in form of Sum and Carry. For inputs A and B the expression is:
Sum = A XOR B
Carry = AB

Full adders are used to take in three inputs which include the previous Carry and then provide the output in form of Sum and Carry For inputs A , B and Cin the expression is:
Sum = A XOR B XOR Cin
Carry = AB +BC + CA

1.3 Coding Techniques used

1.3.1 Data flow modeling

Dataflow Modeling includes declaration of a target signal using logical events occurring on the particular signal. Dataflow Modeling is primarily expressed using signal assignment statements.

1.3.2 Behavioral modeling by using If statement

Behavioral Modeling deals with the functionality of an entity. Here, the set of statements are executed sequentially in a specified order, mainly specified within a process statement. The process statement is itself a concurrent statement but inside it lies a set of statements which are all sequential in nature.

1.3.3 Structural modeling

Structural Modeling is the set of interconnected components. That is, it describes the structure. The visible components are instantiated in the declarative part of the architecture body while the declared components are instantiated with their respective interface ports in the statement part of the architecture body.

1.4 Simulation and Results

1.4.1 Half Adder using Dataflow

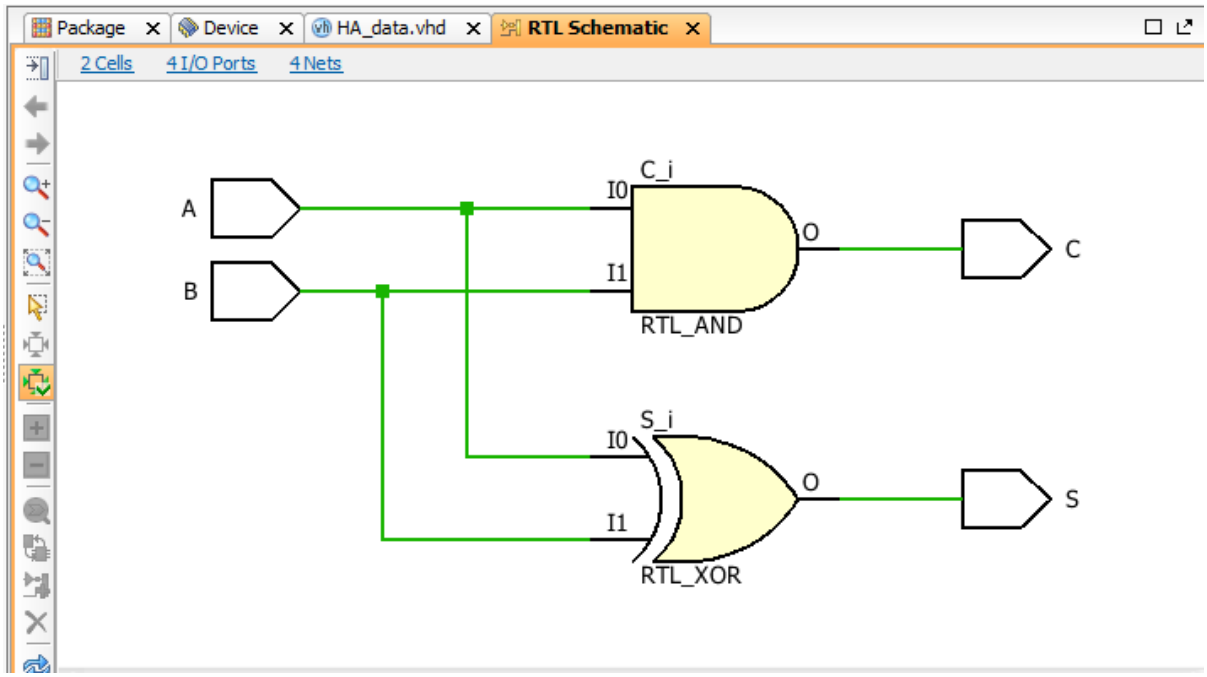

Figure 1.1 Schematic of the Half added using Dataflow modeling

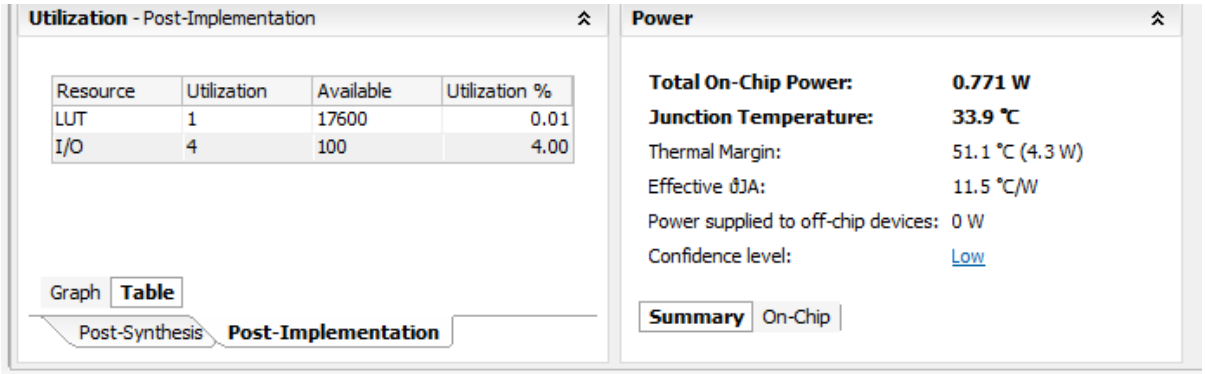

Figure 1.2 Project Summary of the Half added using Dataflow modeling

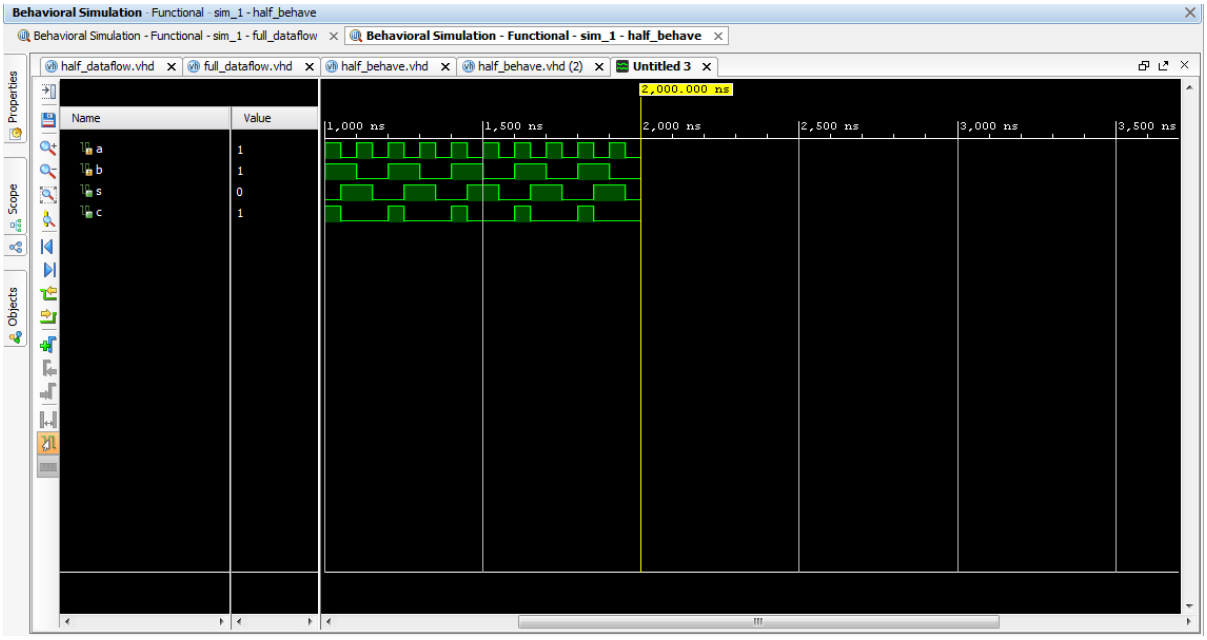

Figure 1.3 Simulation of the Half added using Dataflow modeling

1.4.2 Half Adder using Behavioural

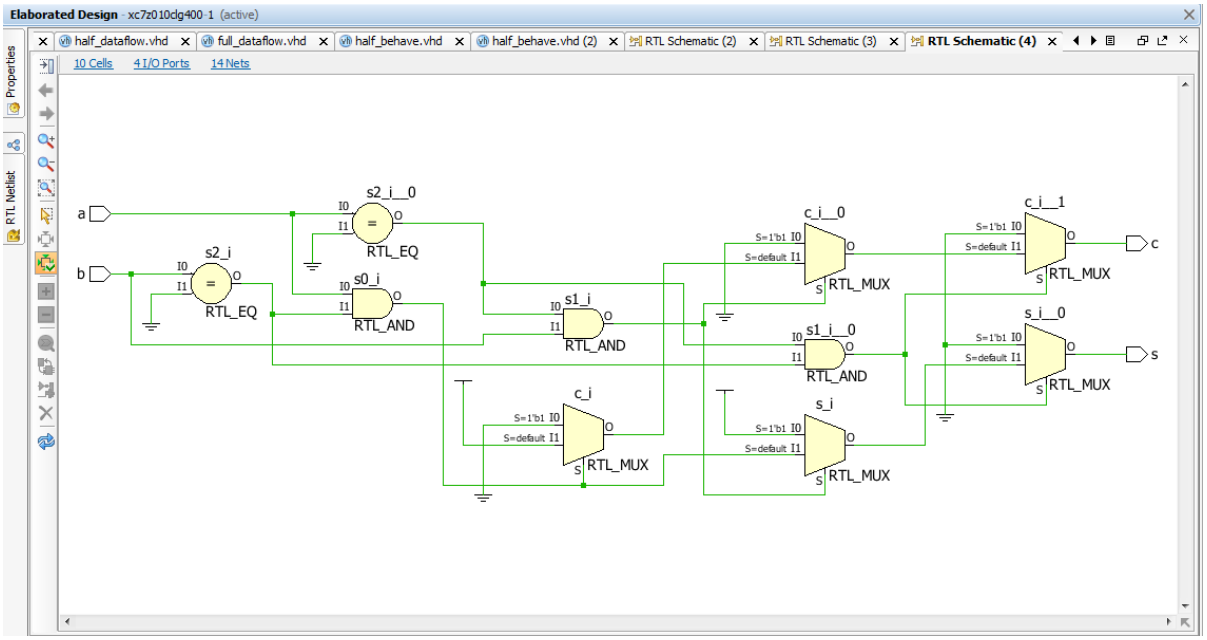

Figure 1.4 Schematic of the Half added using Behavioural modeling

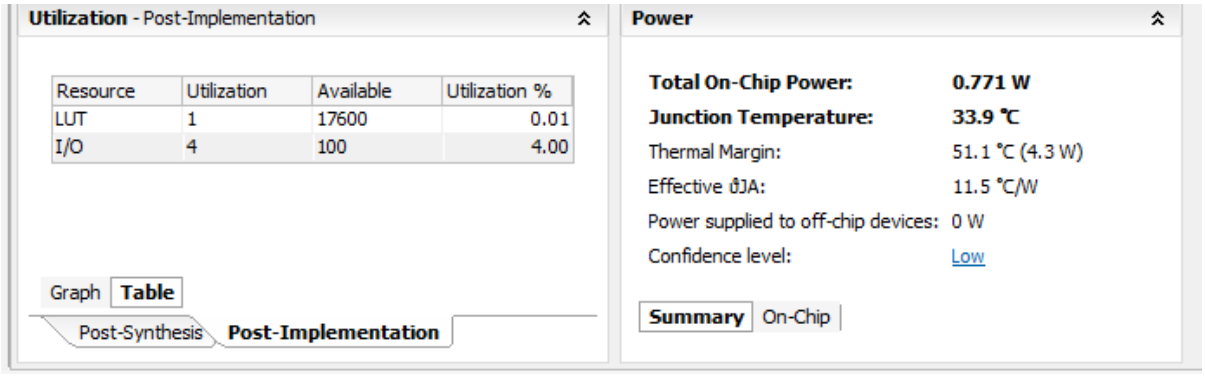

Figure 1.5 Project Summary of the Half added using Behavioural modeling

Figure 1.6 Simulation of the Half added using Dataflow modeling

1.4.3 Full adder using half adders

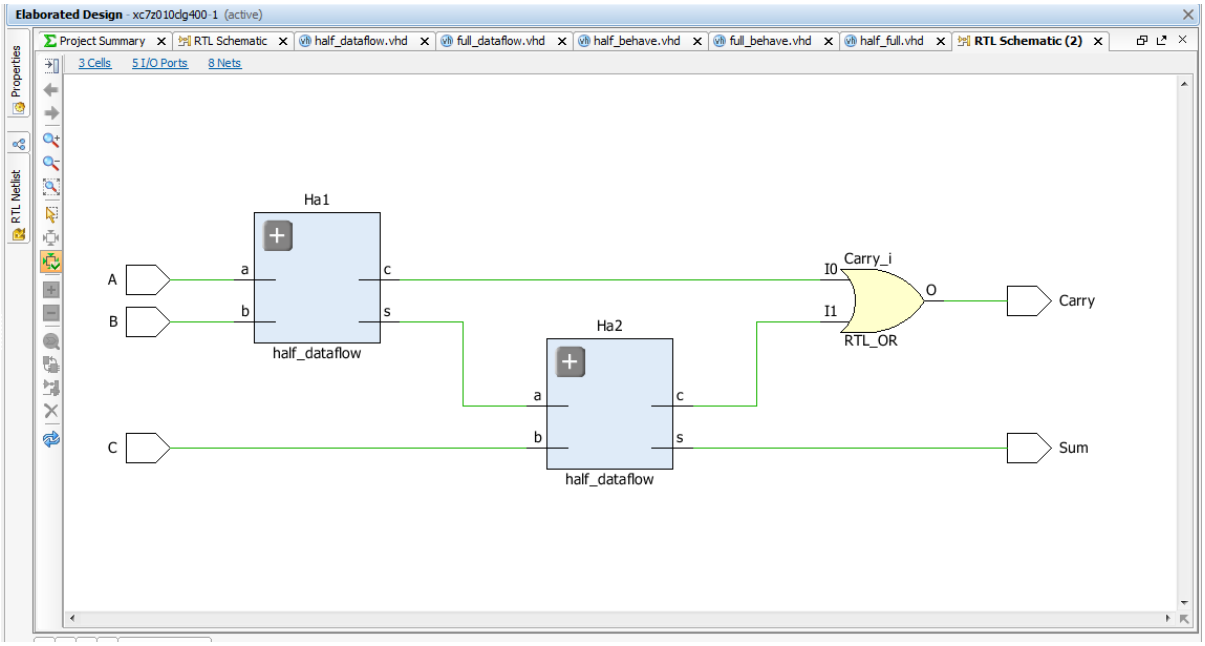

Figure 1.7 Schematic of the Full Adder using half adder

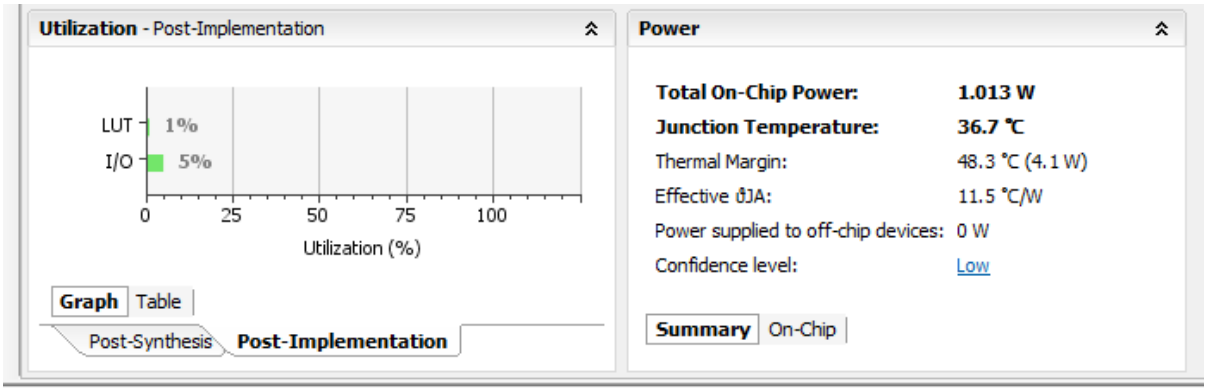

Figure 1.8 Project Summary of the Full Adder using half adder

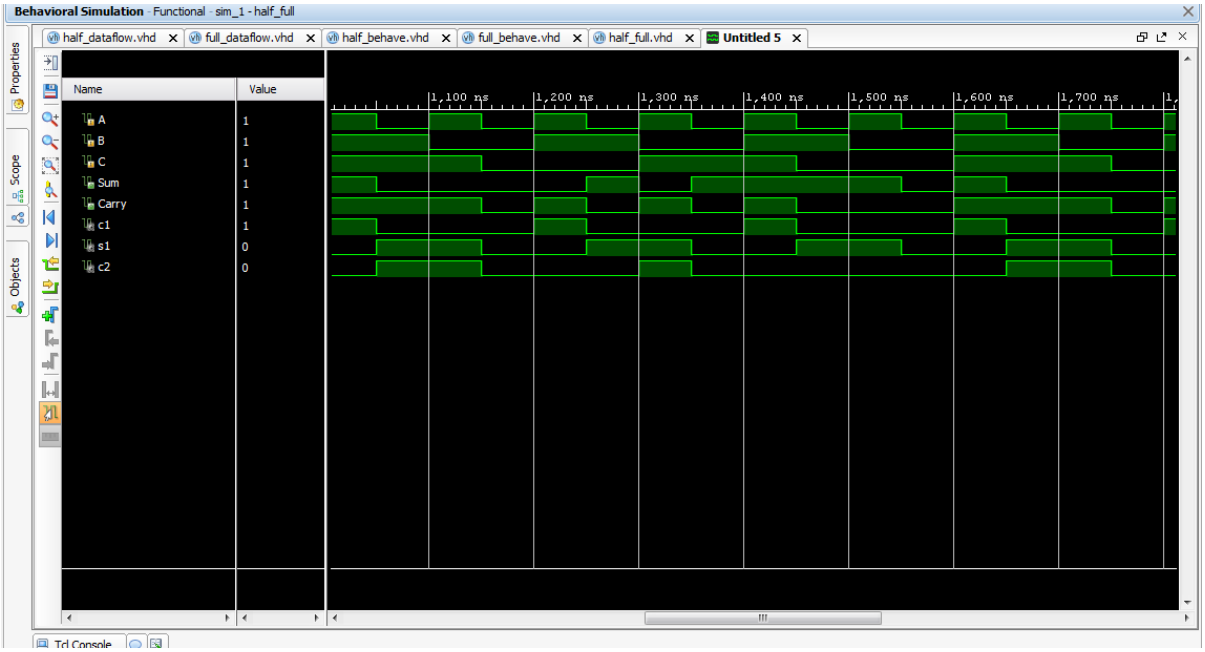

Figure 1.9 Simulation of the Full Adder using half adder

1.4.4 Full adder using Behavioural modeling

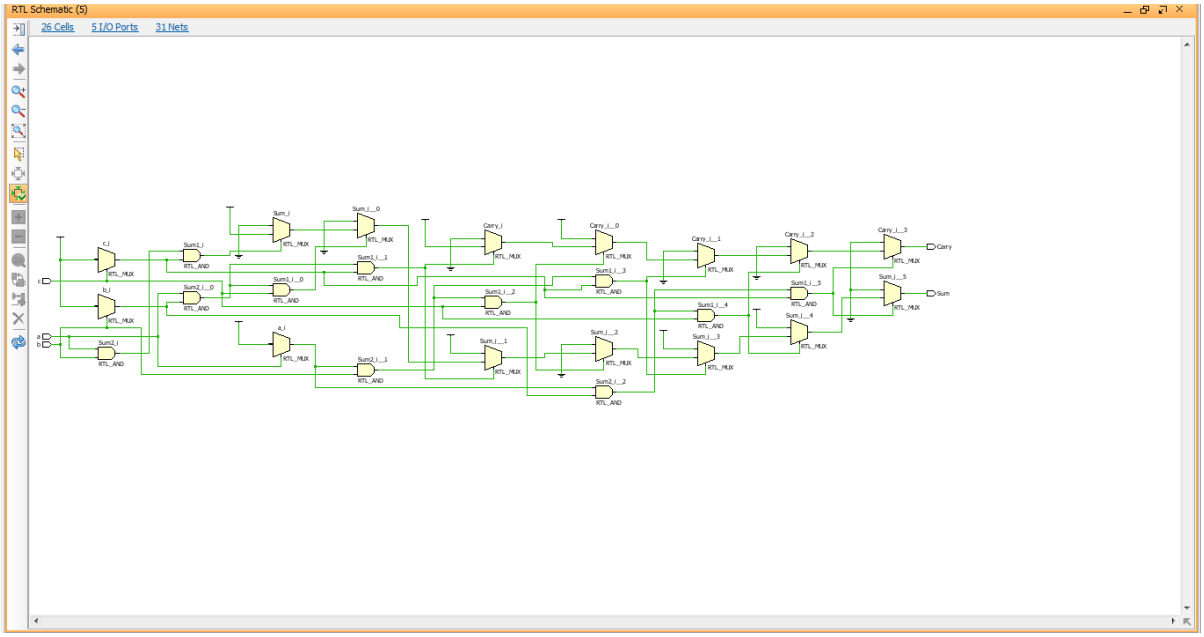

Figure 1.10 Schematic of the Full Adder using Behavioural modeling

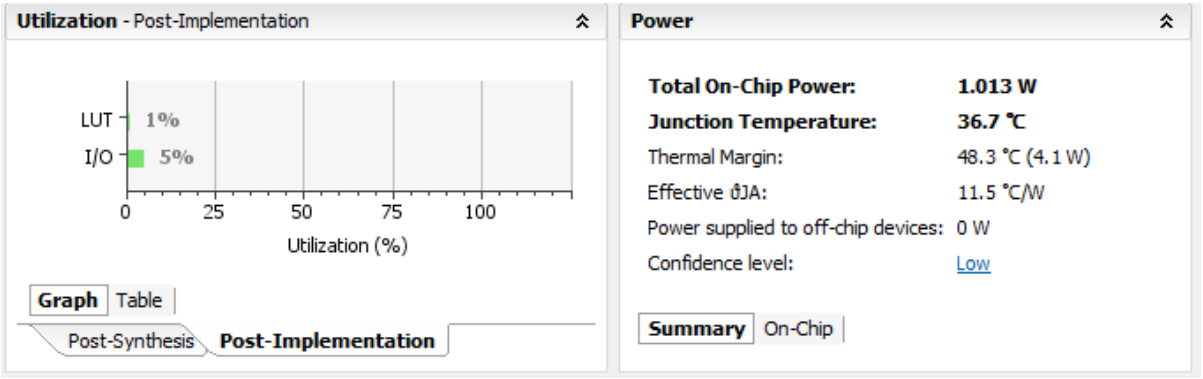

Figure 1.11 Project Summary of the Full Adder using Behavioural modeling

Figure 1.12 Simulation of the Full Adder using Behavioural modeling

1.4.5 Full adder using Data Flow Modeling

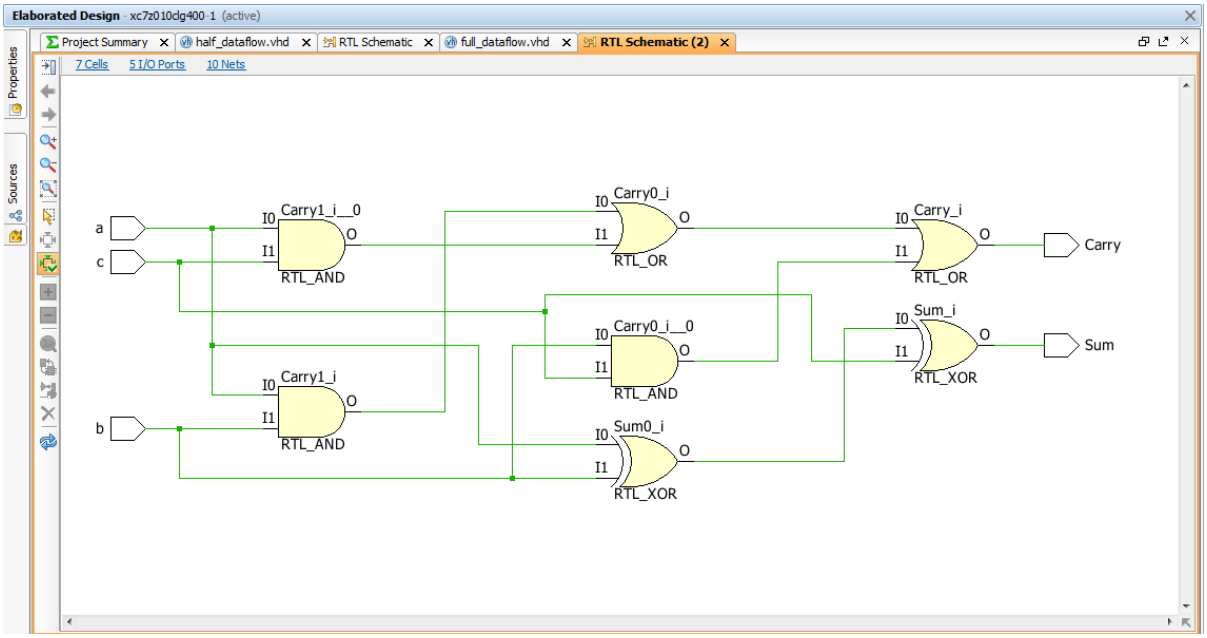

Figure 1.13 Schematic of the Full Adder using Data flow modeling

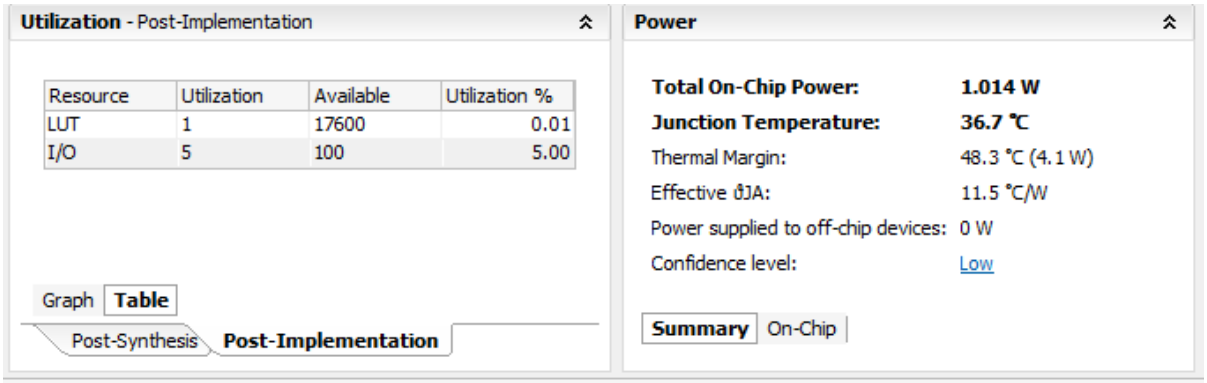

Figure 1.14 Project Summary of the Full Adder using Data flow modeling

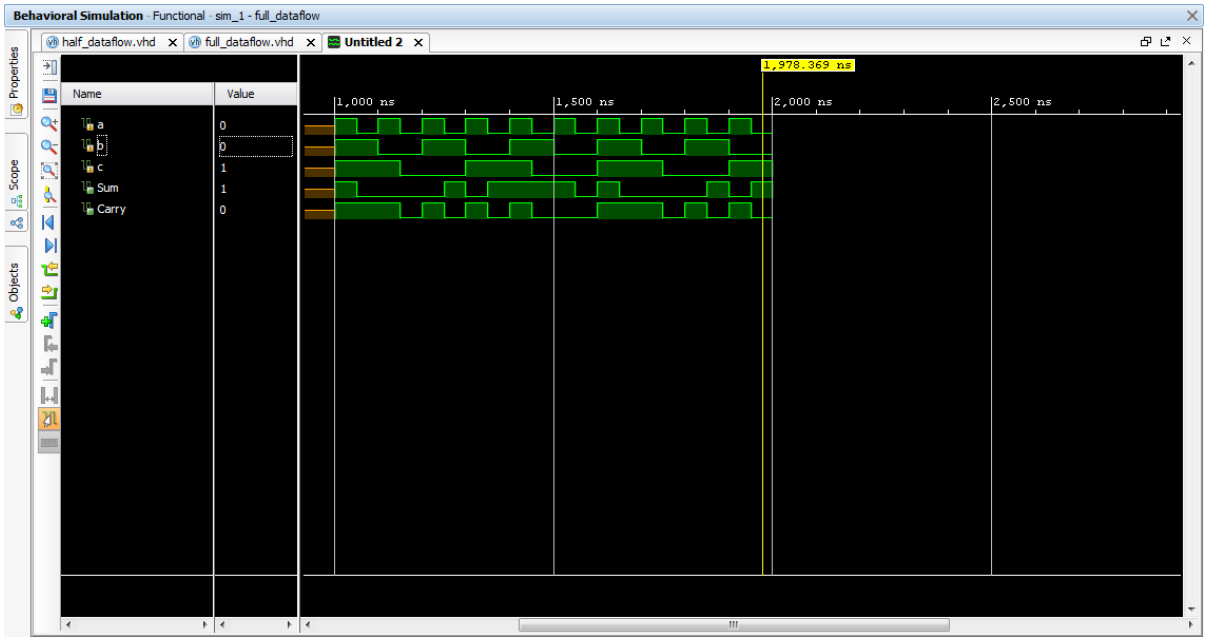

Figure 1.15 Simulation of the Full Adder using Data Flow modeling

1.5 Summary

Tabular comparison of all the codes in terms of area and power usage.

Name of the Entity	No. of LUT used	Total On chip Power
Half Adder using Dataflow	1	0.771W
Half Adder using Behavioural	1	0.771W
Full Adder using Half Adder	1	1.013W
Full Adder using Dataflow	1	1.014W
Full Adder using Behavioural	1	1.013W

Table 1.1 comparision of Area and power requirements for different kinds of adders.